TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

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ANALOGUE PREDISTORTION OF RF BIPOLAR JUNCTION TRANSISTORS USING A LOGARITHMIC AMPLIFIER

Master of Science Thesis

Examiners: University Lecturer Olli-Pekka Lunden, Lecturer Jari Kangas
Examiners and topic approved on 28 February 2018

ABSTRACT

TIMO PALDANIUS: Analogue Predistortion of RF Bipolar Junction Transistors Using a Logarithmic Amplifier
Tampere University of technology
Master of Science Thesis, 61 pages, 14 Appendix pages
September 2018
Master's Degree Programme in Electrical Engineering
Major: Electronics
Examiners: University Lecturer Olli-Pekka Lunden, Lecturer Jari Kangas

Keywords: amplifier, analogue predistortion, bipolar junction transistor, exponential, intermodulation, linear, linearization, logarithmic amplifier, nonlinear

A proof of concept study is conducted in the thesis, a new analogue predistortion linearization scheme for bipolar junction transistors is implemented and tested. Output current and voltage of a bipolar junction transistors exponentially depends on the input voltage, thus the output is distorted exponentially. We study whether a bipolar junction transistor can be linearized by cascading a logarithmic amplifier in front of the bipolar junction transistor amplifier. Logarithmic function is the inverse of the exponential function. Consequently, these two functions should cancel each other, rendering the system's output linearly dependent on the input. To verify this, the scheme is implemented in practice and measured. The measurement results confirm the viability of the scheme, the output third-order intermodulation intercept point is improved by 10 dB. Additionally, the third order intermodulation products are suppressed by 20 dB. The proposed linearization scheme is low cost and complexity and inherently broadbanded.

TIIVISTELMÄ

TIMO PALDANIUS: Radiotaajuisen bipolaaritransistorin analoginen esivääristys logaritmisella vahvistimella
Tampereen teknillinen yliopisto
Diplomityö, 61 sivua, 14 liitesivua
Syyskuu 2018
Sähkötekniikan diplomi-insinöörin tutkinto-ohjelma
Pääaine: Elektroniikka
Tarkastajat: Yliopistonlehtori Olli-Pekka Lunden, Lehtori Jari Kangas

Avainsanat: analoginen esivääristys, bipolaaritransistori, epälineaarinen, exponentiaalinen, keskinäismodulaatiosärö, lineaarinen, logaritminen vahvistin, vahvistin

Tämä opinnäytetyö on soveltuvuusselvitys, jossa toteutetaan ja testataan uusi analoginen esivääristyslinearisointimenetelmä. Bipolaaritransistorien ulostulo on exponentiaalisesti riippuvainen sisäänmenosta, joten bipolaaritransistorilla toteutetun vahvistimen ulostulossa luonnostaan esiintyy exponentiaalista säröytymistä. Ongelman korjaamiseksi vahvistimen eteen kytketään kaskadiin logaritminen vahvistin, sillä logaritmifunktio on eksponenttifunktion vastakohta. Teoriassa logaritmisen ja exponentiaalisen säröytymisen pitäisi kumota toisensa, minkä seurauksesta systeemin ulostulo riippuu lineaarisesti sisäänmenosta. Työssä tehdään käytännön toteutus, jolla menetelmän toimivuus ja käytännöllisyys todennetaan. Mittaustulokset varmentavat menetelmän toimivuuden; ulostulon kolmannen kertaluvun leikkauspiste on parantunut 10 dB:llä. Lisäksi kolmannen kertaluvun keskinäismodulaatiosärö-signaalit vaimenevat 20 dB:llä. Esitelty linearisointimenelmä on yksinkertainen ja kustannustehokas. Sen lisäksi työssä esitelty menetelmä on luonnostaan laajakaistainen.

PREFACE

First, I would like to thank the TUT electronics club TELOK and its members, especially Markus Ristiniemi and Teemu Salminen. The printed circuit board manufacturing process and the soldering (and sometimes desoldering) equipment at TELOK proved to be invaluable for the practical thesis work. Helpful advice on how to improve my layout designs, board manufacturing and soldering were also provided by members of TELOK. I would also like to acknowledge my examiners Jari Kangas and Olli-Pekka Lunden as they were almost always readily available for conferring about thesis related issues. Lastly, I would also like to thank my brother Antti for helping improve my soldering and desoldering skills that were absolutely necessary for the success of the thesis.

CONTENTS

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LIST OF SYMBOLS AND ABBREVIATIONS

ADS	Advanced Design System
BJT	Bipolar junction transistor
DSP	Digital signal processor
DUT	Device under test
IIP_3	Third order input intercept point
IP_3	Third order intercept point
IM3	Third order intermodulation
IM5	Fifth order intermodulation
LUT	Lookup table
KCL	Kirchhoff's current law
OIP_3	Third order intermodulation output intercept point
RF	Radio frequency
SPICE	Simulation program with IC emphasis
VNA	Vector network analyzer
A_F	current-controlled current source coefficient for the forward biased source
A_R	current-controlled current source coefficient for the reverse biased source
β	DC current gain
B	Bipolar junction transistor base
BC	Bipolar junction transistor base-collector interface
BE	Bipolar junction transistor base-emitter interface
C	Bipolar junction transistor collector
E	Bipolar junction transistor emitter
f	Frequency
G_T	Transducer power gain
I	Current
I_B	Base current
I_C	Collector current
I_E	Emitter current
I_F	Forward current
i_L	Load current
I_R	Reverse current
k	Boltzmann constant
q	Elementary charge
P_{1dB}	1-dB compression point for power
P_{avg}	Available power
P_L	Load power
P_{sat}	Output saturation power
R	Resistance
T	Temperature
V	Voltage
V_{BE}	Base-emitter voltage
V_{CC}	Positive supply voltage
V_{CE}	Collector-emitter voltage
V_{EE}	Negative supply voltage
V_D	Voltage over a diode

V_{ON}	Diode turn-on voltage
V_{OUT}	Output voltage
V_{REF}	Reference voltage
V_T	Thermal voltage
Z	Impedance
Z_0	Characteristics impedance
λ	Wavelength

1. INTRODUCTION

Amplifiers are crucial part of everyday electronics; for instance, consumer wireless communication systems could not function without amplification. Generally, amplifiers are designed to be linear, meaning they produce an output signal that is an amplified reproduction of the waveform at the input. However, the waveform can be inadvertently altered due to nonlinear behavior of the amplifier. Consequently, a multitude of linearization techniques have been developed for correcting nonlinear behavior. [1, 2]

Each linearization method is a trade-off between the efficacy, bandwidth, adaptability, efficiency, the added complexity, and cost. Linearization methods can be divided into two subcategories, to analogue and digital linearization methods. Perhaps the best adaptability is offered by digital linearization methods as sensors combined with microprocessor enable autonomous and instantaneous control. This allows the system to adapt to changing operation conditions such as device and ambient temperatures and dropping battery voltages. Analogue linearization methods offer a varied range of advantages and disadvantages depending on the technique. Feedforward linearization offers superior linearity and theoretically limitless bandwidth at the cost of efficiency and complexity; the technique is one of the most challenging linearization techniques to implement [3]. Cartesian feedback is a more adaptable and simpler to implement but it suffers from limited bandwidth and slightly reduced linearity when compared to the feedforward linearization. If simplicity is the deciding factor, then analogue predistortion is perhaps the best choice. [4]

Predistortion is a linearization method where the signal is distorted prior to feeding to the amplifier. Amplifiers usually distort in an identifiable manner, allowing the identification of the nonlinear characteristics. If the input were to be an inverse function of the distortion, then the two distortions would effectively cancel each other out. The system output would now be linearly dependent on the input. [3]

This thesis is a part of proof of concept study where a new analogue predistortion scheme for a radio frequency (RF) bipolar junction transistor (BJT) is presented. A BJT RF amplifier is linearized by cascading a logarithmic amplifier with the BJT RF amplifier input. The logarithmic amplifier consists of a transistor connected in negative feedback with an operational amplifier. A matched pair transistor is used, the first transistor is used in the logarithmic amplifier and the second one in the BJT RF amplifier. The best degree of linearity is achieved when the transistors are identical as possible [5].

Logarithm is the inverse function of the exponential dependence experienced by the BJT, thus the distortions are canceled out. Consequently, the amplifier output should be linearly dependent on the input. The objective of the thesis is to verify the effectiveness and the viability of the linearization method by implementing the linearization scheme for a simple BJT amplifier. Prior works related to the study include a bachelor's thesis titled "High-frequency logarithmic amplifier for predistortion (in Finnish) [6]" by Olli Hytönen and at the moment of writing this thesis an unpublished scientific article "Linearization of BJT's with Logarithmic Predistortion [5]" by Olli-Pekka Lunden. Parts of the thesis heavily rely on these two works. The results obtained in this thesis will be used in the article.

First, the thesis discussed the background including linearity and other contemporary linearization methods. Next, the source of nonlinearity in BJTs is studied and the linearization scheme for the thesis is presented. The linearization scheme implementation, measurement and simulation results are examined and presented. Additionally, side projects undertaken during the thesis are briefly discussed. Lastly, practical work done during the thesis is reviewed and an assessment of the success of the thesis and possible future work is provided.

2. BACKGROUND

Before discussing RF amplifier linearization, we must understand the fundamentals of linearity and distortion. We will examine a couple of established linearization techniques, but predistortion will be studied more thoroughly, since it is the main topic of the thesis. Implementations of analogue predistortion will be presented alongside the underlying theory.

2.1 Linearity

In electronics linearity is often a desirable feature. By definition, a function is linear if it is homogeneous and additive. For instance, Ohm's law satisfies these conditions. The voltage *V* over a resistor is dependent on the resistance *R* and the current *I* flowing through the resistor as shown by Ohm's law

$$V = RI. \tag{1}$$

We can present voltage as a function of current by assuming the resistance to be a constant

$$V(I) = RI. \tag{2}$$

Voltage is now expressed as a function of current. Scaling the current with an arbitrary factor *a* we get obtain the following function

$$V(aI) = R(aI) = aRI = aV(I). \tag{3}$$

This satisfies the homogeneity condition, as scaling the current with factor *a* directly scales the voltage with the same factor. A sum of two currents, $I_1 + I_2$ flowing to a resistor results in the subsequent formula

$$V(I_1 + I_2) = R(I_1 + I_2) = RI_1 + RI_2 = V(I_1) + V(I_2). \tag{4}$$

Additivity is clearly observed in (4). As a consequence of satisfying these conditions, linear functions adhere to the superposition principle. If a function is linear, then a plot of the function is a straight line that passes through the origin. We fall back on Ohm's law again to demonstrate this. Let us choose an arbitrary fixes resistance value of 50 Ω and plot the current as a function of voltage. [7]

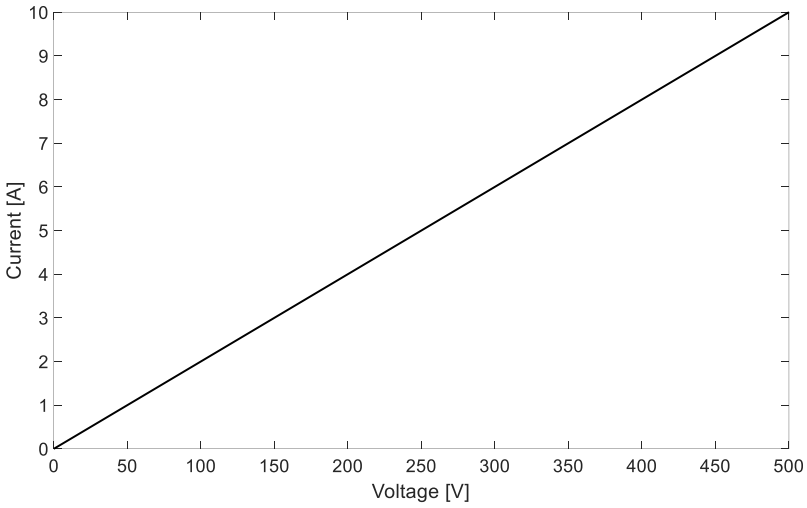

Figure 1. Current through a 50 Ω linear resistor as a function of voltage.

With a fixed arbitrary resistance value, the resulting plot of (2) is straight line as shown in Figure 1. The same applies for other linear approximations, when the relationship between different quantities is plotted, the resulting graph is always a straight line.

Generally, these factors make linearity a desirable feature in electronics. Linear systems enjoy a high degree of predictability due to output being directly related to input. In addition, nonlinear distortion is absent in linear systems. But the reality is more complicated, most, if not all systems exhibit nonlinear behavior to a certain degree. Once again, let us utilize a resistor and Ohm's law as an example. Earlier we claimed the resistance *R* is a constant. However, when current flows through a resistor, it heats up and a change in resistance is observed. Therefore, voltage over a resistive element is not only dependent on current and a constant resistance as Ohm's law dictates. Nonetheless, in most cases temperature has a negligible effect on the resistance and thus the Ohm's law is accurate enough linear approximation of reality. [7]

Linear systems are not wholly exempt from distortion, but first we must define distortion before we delve into this. Distortion is described as "the act of twisting or altering something out of its true, natural, or original state" [8]. Let us consider a two-port amplifier as an example, where one port is the input and the other is the output. If the waveform of the output is not a replica of the waveform present at the input, then the signal is distorted. Distortion itself is divided into two categories, nonlinear distortion and linear distortion. Linear systems are susceptible to the latter, as the output can be linearly dependent on the input and distorted at the same time. For instance, if a square wave input were applied, then the waveform might experience linear change due to linear filtering [9]. Nonlinear distortion is more varied, since all waveform deformations that are not linearly dependent on the input are included in this category. Additionally, nonlinear distortion can generate new frequency content. In the next chapter we will examine nonlinearity and its effects, especially intermodulation distortion. [10]

2.2 Consequences of nonlinearity

Systems that inherently exhibit strong nonlinear behavior do not have an accurate linear approximation for the entirety of the operation range. This type of system is called a nonlinear system. To illustrate how nonlinear behavior might look like, we will examine a DC characteristics of a BJT shown in Figure 2. [11]

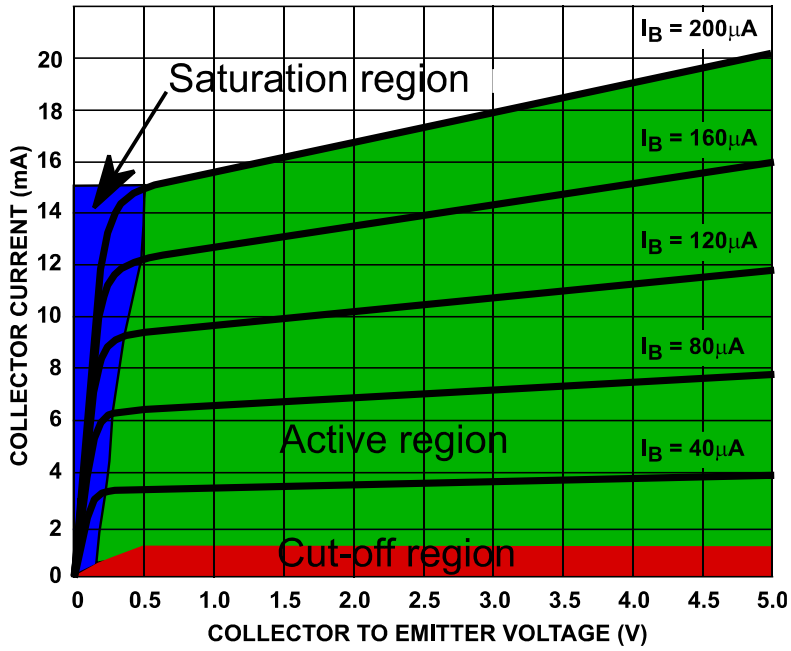

Figure 2. HFA3134 BJT characteristics curve. Modified from [12].

The relationship between current and voltage is now more complicated. There are three distinct regions in the Figure. In each region the relationship between collector current I_C and collector to emitter voltage V_{CE} is different. The regions are highlighted in the Figure: cut-off region is highlighted with red, active region is highlighted with green and the blue highlights saturation region. In the cut-off region the current remains at zero despite the voltage. The opposite applies for the saturation region, depending on the base current I_B, a small increase in V_{CE} results in huge increase in I_C. Nonetheless, the curves appear to be linear in certain areas. If only a limited part of the operation range is examined, then the device seems to exhibit linear behavior, hence linear approximation is viable in these regions. However, the prior example was limited in scope and depth. A whole host of different nonlinearities manifest, when other variable dependencies considered. Depending on the system, the consequences of nonlinear behavior vary. [13]

Distortion may cause loss of data or otherwise degrade the overall performance. To illustrate this point, we will examine amplifiers and a few common types of nonlinearities afflicting them. Ideally an amplifier should provide a constant gain regardless of the input power. However, at higher input power levels, the device is pushed into nonlinear region. Consequently, the output is distorted. This phenomenon is known as gain compression. Figure 3 illustrates this behavior. [14]

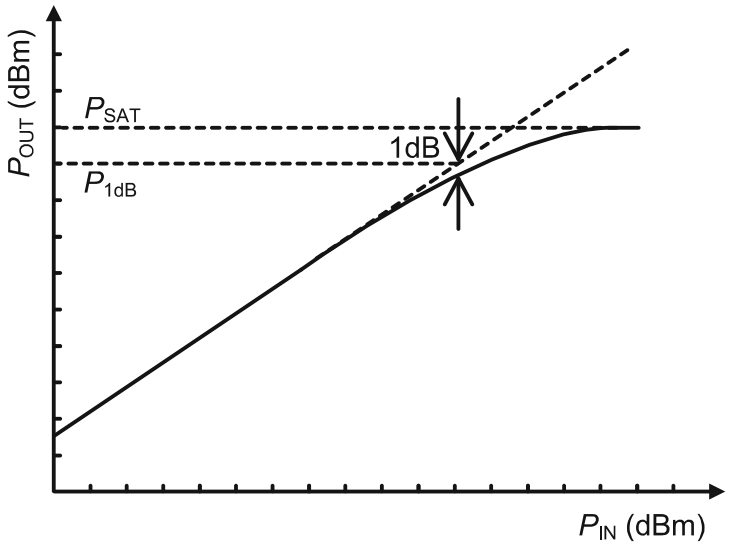

Figure 3. Gain compression. [14]

The dashed line is the ideal gain and the solid line is the actual gain. The maximum output power achieved by the amplifier is expressed by output saturation power P_{SAT} that is determined from the point where the gain plateaus. Another parameter shown in the graph is the 1-dB compression point P_{1dB}. The parameter is used as figure of merit to describe the linearity of the device. The point itself is given by the location in the graph where the difference between the extrapolated ideal gain and the actual gain is 1 dB. Operating past P_{1dB} decreases gain and introduces distortion. [14]

Intermodulation distortion is a consequence of nonlinearity. This occurs when there are two or more frequencies present at the input of a nonlinear device. The two frequencies $f_1$and f_2 mix and create intermodulation products with different frequencies. The product frequencies are $|Nf_1 + Mf_2|$, where *N* and *M* are positive or negative integers, including zero. The order of an intermodulation product is defined as $|N| + |M|$. The odd order products are especially detrimental if the frequencies are within a range where the amplifier provides a constant gain. Intermodulation orders and their respective products are compiled up to the fifth order in table 1. Note, the table does not contain all the products for each order. [15]

Table 1. Intermodulation products for the first five orders. [15, 16]

Order	Intermodulation Products				Comments
1st Order	f_1		f_2		Fundamental
2nd Order	$f_1 + f_2$		$f_2 - f_1$		Sum and difference
3rd Order	$\boldsymbol{2f_1 - f_2}$	$\boldsymbol{2f_2 - f_1}$	$2f_1 + f_2$	$2f_2 + f_1$	Primary concern
4th Order	$2f_2 + 2f_1$		$2f_2 - 2f_1$		Not of concern
5th Order	$\boldsymbol{3f_1 - 2f_2}$	$\boldsymbol{3f_2 - 2f_1}$	$3f_1 + 2f_2$	$3f_2 + 2f_2$	Secondary concern

The bolded products in the table are of interest as they are close to the fundamental frequencies. Consequently, filtering the undesired response is difficult. As an example, we study how intermodulation affects a certain nonlinear low power amplifier through two-tone intermodulation test results shown in Figure 4. [14]

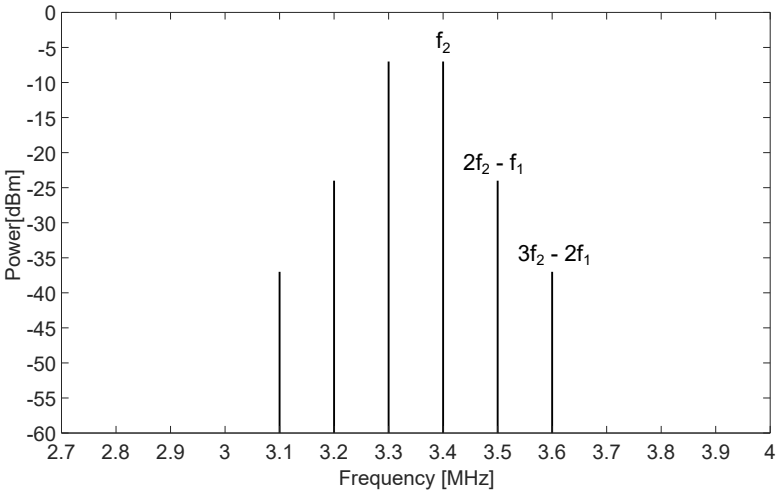

Figure 4. Intermodulation measurement results for a nonlinear low power amplifier.

Input frequencies are 3.3 MHz and 3.4 MHz. The intermodulation products are found evenly spaced at both sides of the input frequencies. The distance between the fundamental frequency and the closest third order intermodulation distortion (IM3) peak is only 100 kHz. The fifth order intermodulation distortion (IM5) products are farther away, the distance being 200 kHz. Filtering the distortion would be difficult and costly as a highly selective bandpass filter is required. If the device is to operate at multiple frequencies, then filtering might not be feasible or cost-effective. The additional frequency content generated by intermodulation is detrimental to device operation [14]. Spectral regrowth is a consequence of intermodulation; the phenomena is illustrated in Figure 5.

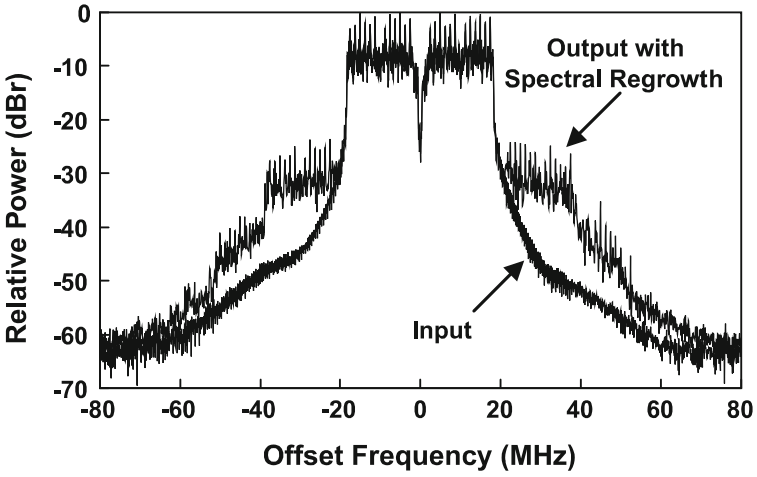

Figure 5. Spectral regrowth. [14]

The intermodulation products are interfering with the adjacent channels, reducing signal quality or in worst case, completely blocking the channel. Additionally, modulation may be affected by spectral regrowth, potentially resulting in loss of information. The relationship between input power and third order intermodulation products are shown in Figure 6. [14]

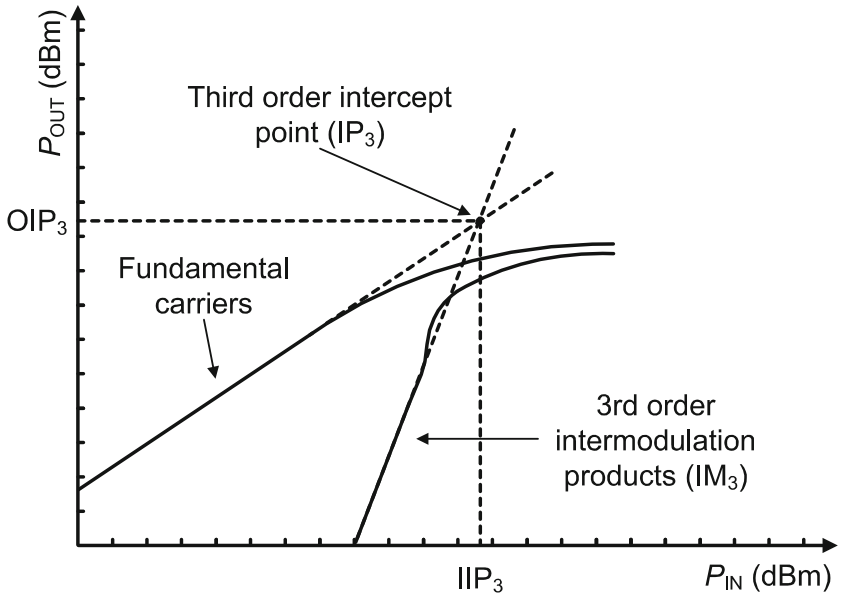

Figure 6. Third order intercept point (IP_3). Modified from [14].

IM3 becomes visible, when the device operates in the compression regime. Increasing input power beyond the 1-dB compression point results in accelerated growth of IM3. The slope of IM3 is 3:1 whereas fundamental carriers have a slope of 1:1. Therefore, after a certain point IM3 could be expected surpass the fundamental carrier. However, the distortion power plateaus due to compression before it surpasses the fundamental carrier. Nonetheless, a theoretical intercept point can be determined by performing linear extrapolation for both curves. The point where the extrapolated lines cross is called the third order intercept point IP_3. Similarly to P_{1dB}, IP_3 is also a measure of linearity. [14]

Accurate predicting of intermodulation distortion in amplifiers can prove challenging as they do not always adhere to static characteristics. Amplifiers also have dynamic characteristics that affect distortion, causing deviation from static models. The past device states influence the device behavior; the effects ranging from changes in distortion phase and amplitude to shift in frequency. This type of dynamic deviation is known as the memory effect. Self-heating and nonconstant impedances are common sources of memory effects [17]. [18]

2.3 RF amplifier linearization methods

Linearization itself is defined as a process for making a system more linear. Theoretically this should help mitigate nonlinear distortion [4]. We will study a couple of commonplace linearization techniques for RF amplifiers, including power back-off, feedforward, Cartesian Feedback and predistortion. The feasibility of a linearization method depends on the application. Wireless devices usually require high efficiency due to limited battery life [19]. On the other hand, linearity is crucial in base stations [19]. Increased linearity usually comes at a price; usually in form of decreased efficiency and increased complexity and cost [17].

It is crucial that we understand what efficiency means in the context of the thesis, before we can evaluate different linearization methods. Efficiency η is defined as the ratio of output RF power P_{OUT} and the DC power P_{DC} drawn by an amplifier

$$\eta = \frac{P_{OUT}}{P_{DC}}. \tag{5}$$

The more DC power is converted to RF power, the higher the efficiency. Linearization usually decreases efficiency as more power is required for the linearization process. [17]

2.3.1 Power back-off

An attentive reader might have inferred that external linearization circuitry might not always be an absolute necessity. What if the operation point is moved from the saturation regime to the linear region. This method is termed power back-off and it ranks as one of the most rudimentary linearization processes. The concept of power back-off is illustrated in Figure 7. [4]

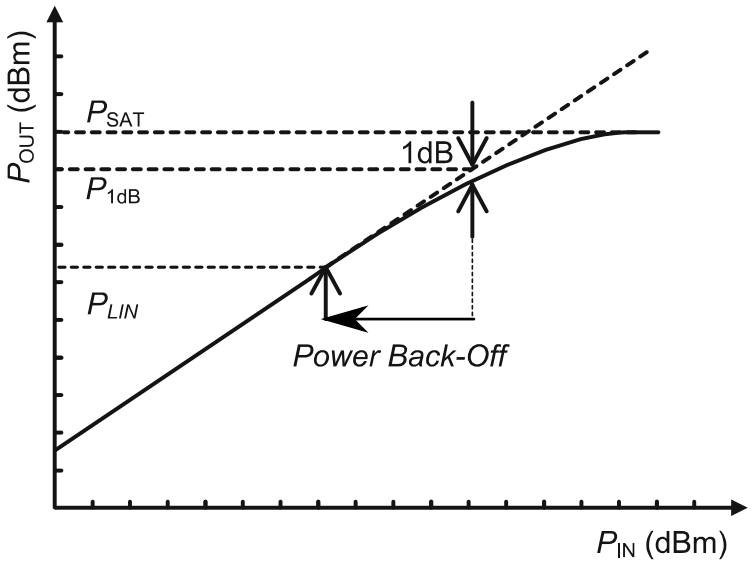

Figure 7. Power Back-off for RF amplifier. Modified from [14].

The operation point is moved from the nonlinear compression regime to a point in the curve where the behavior is still linear. The point is marked as P_{LIN} in the graph. The device now operates in more linear fashion. Another option to achieve the same result is by using a more expensive high-power amplifier. The main advantage is that external linearization circuitry is not needed. Nonetheless, power back-off is not always feasible. The amplifier is underutilized and hence the power efficiency is low. Employing this technique in wireless applications would mean considerably shorter battery life. Therefore, external linearization circuits are required if both, high degree of linearity and power efficiency are desired. [4]

2.3.2 Feedforward linearization

Feedforward linearization offers a high degree of linearity regardless of the frequency and bandwidth. The technique is based on signal splitting and coupling. A simplified feedforward linearization architecture for a RF amplifier is shown in Figure 8. [3]

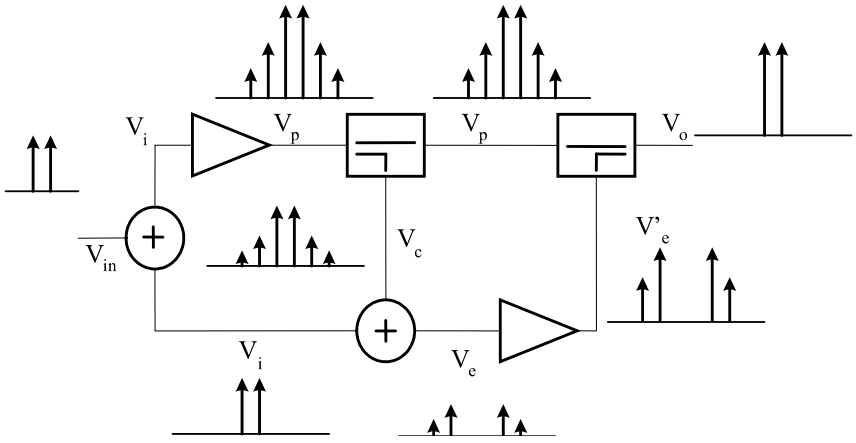

Figure 8. Two tone intermodulation with feedforward linearization. [3]

The scheme consists of two loops. A waveform that only contains the intermodulation distortion components generated by the amplifier is created in the first loop. In the second loop, the waveform is scaled and subtracted from the amplifier output, cancelling out the distortion. By utilizing feedforward linearization, it is possible to negate all the nonlinear effects. In addition, the architecture is open loop, hence the scheme is unconditionally stable regardless of frequency and bandwidth. However, feedforward linearization suffers from two significant drawbacks. The total power consumption is effectively doubled by the additional amplifier. The scheme is complex and difficult to implement. Figure 8 does not include the necessary gain and phase adjustment blocks. The linearization fails if the distortion waveform and the amplifier output are out of phase or have different power levels. Realtime phase and gain adjustments are necessary, since they are affected by changes in operating conditions. [3]

2.3.3 Cartesian feedback loop

While feedback linearization is simple and effective, it has flaws that make it unsuitable for RF application. Stability and reduction in bandwidth are major issues due to the delays introduced by the feedback loop [3]. Hence, Cartesian Feedback Loop has been developed. The issues with bandwidth and frequency are circumvented by downconverting the signals in the loop. There are two separate indirect feedback loops, one for the in-phase (I) and another for the quadrature (Q) component of the signal. A simplified Cartesian Feedback Loop scheme is shown in Figure 9. [4]

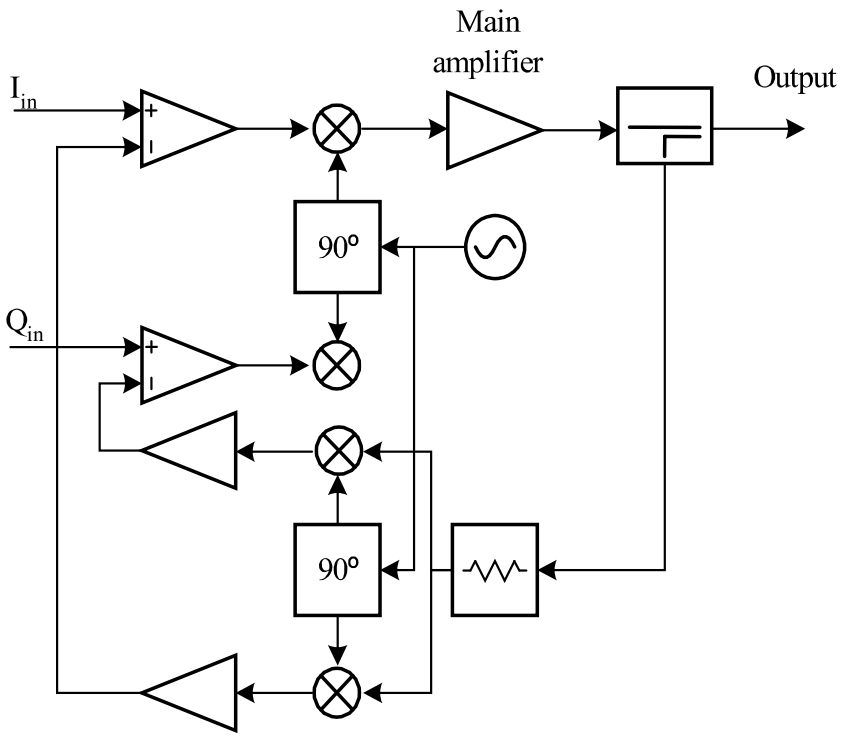

Figure 9. Simplified Cartesian Loop architecture. [3]

The feedback signal is demodulated by an I/Q demodulator, splitting the distorted signal into in-phase I' and quadrature Q' components. The input is split to I and Q signals that are fed alongside I' and Q' components from the feedback loops into differential amplifiers. The signals are compared and amplified by the differential amplifiers, resulting in amplified error signals. These signals upconverted and are fed back to the main loop, forcing a linear response. Despite the improved stability and bandwidth, Cartesian Feedback is still limited to narrowband applications. Nonetheless, Cartesian feedback is more straightforward and power efficient when compared to feedforward linearization. [4]

2.4 Predistortion

Predistortion is a linearization technique where the amplifier input is distorted so that the amplifier distortion is cancelled. This can be achieved by cascading a distorter that produces an inverse function of the distortion with the distorting amplifier. However, you need to know the distortion function before implementing a predistortion scheme, thus a model for the amplifier is required. Fortunately, finding the relationship between the amplifier input and output is enough to construct a black box behavioral model for the amplifier. [19]

Predistortion is intrinsically an open-loop linearization technique, allowing wider operating bandwidth. The method is not inherently adaptable as environmental effects and component aging are not considered. At the cost of simplicity, adaptability can be improved by employing feedback loops; this is known as dynamic or adaptive predistortion. Predistortion is divided into two main categories: analogue predistortion and digital predistortion. [19]

2.4.1 Digital predistortion

Digital predistortion is usually more suitable for adaptive control. Consequently, digital predistortion implementations able to cope with changes in the response better than their analogue counterparts. The inclusion of a digital signal processor (DSP) allows simultaneous implementation of multiple linearization methods. For example, digital predistortion can be coupled with Cartesian Feedback, further improving linearity. This is known as digital baseband adaptive predistortion. The architecture is shown in Figure 10. [3, 9]

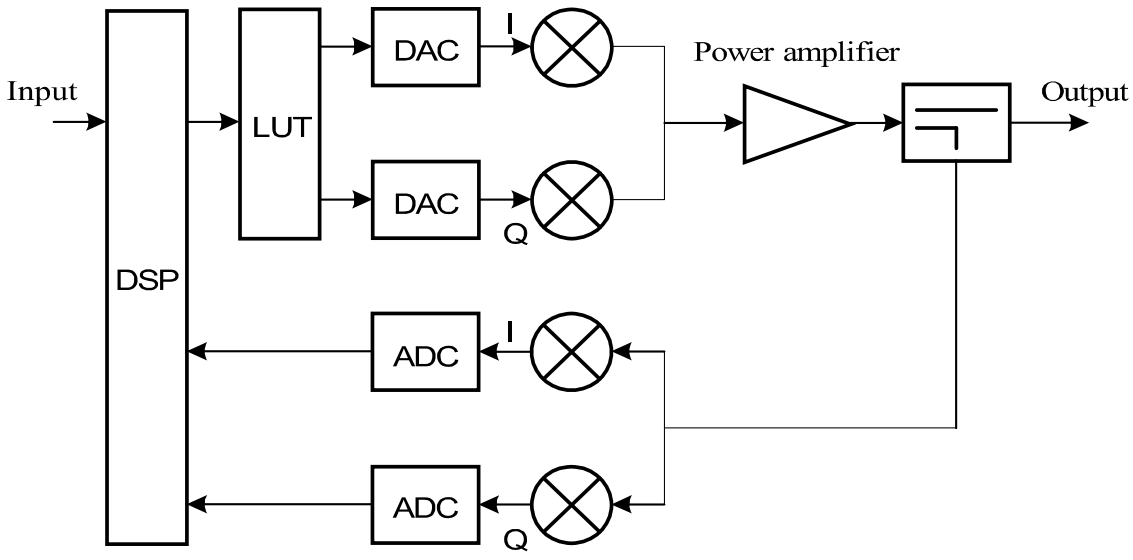

Figure 10. Digital baseband adaptive predistortion. Modified from [3].

The input is converted from analogue to digital and fed to the DSP alongside the feedback signal, enabling error correction. This mitigates the adverse effects on linearization introduced by component aging and environmental factors. The predistortion element is in the lookup table (LUT) contains a behavior model for the amplifier. The I and Q parts of the signal are converted back to analogue and fed to the amplifier. The DSP can also be utilized to deal with possible memory effects. The bandwidth and the operation frequency are limited by the Cartesian Loop and DSP. Nonetheless, baseband distortion techniques are viable in wideband applications. Digital baseband predistortion is often low cost, more easily implemented and has a higher power efficiency when compared to feedforward linearization. [3, 9]

2.4.2 Analogue predistortion

Excluding power back-off, analogue predistortion is currently perhaps the simplest linearization technique. For instance, a series diode and a parallel capacitor constitute a rudimentary predistorter [19]. Unfortunately, not every analogue predistortion scheme readily lend themselves to adaptive control. Additionally, analogue predistortion is much more application specific. Nonetheless, analogue predistortion is still, to this date, a viable approach for linearization. Bandwidth and power are practically only limited by the analogue components. Consequently, analogue predistortion is suitable for wide bandwidth and high-power applications. Furthermore, analogue predistortion generally has a low cost and complexity of implementation. [3, 9]

2.5 Analogue predistortion Implementations

The design of an analogue predistortion scheme varies greatly depending on the application. Consequently, analogue predistortion implementations are diverse. To illustrate this point, we will go through three different proposed and implemented analogue predistortion schemes.

2.5.1 A wideband analog predistortion power amplifier with multi-branch nonlinear path for memory-effect compensation

Normally amplifiers are designed to exhibit the least possible amount of memory effects. However, when an amplifier operates with wideband signals, mitigating memory effects becomes a difficult task. Conventional analogue predistorters are not able to cancel distortion effectively due to memory effects that occur with wideband signals. Therefore, the authors of the article [20] have proposed and implemented an analogue predistortion scheme that is able to compensate for memory effects. A proposed analogue predistortion scheme is shown in Figure 11. [20]

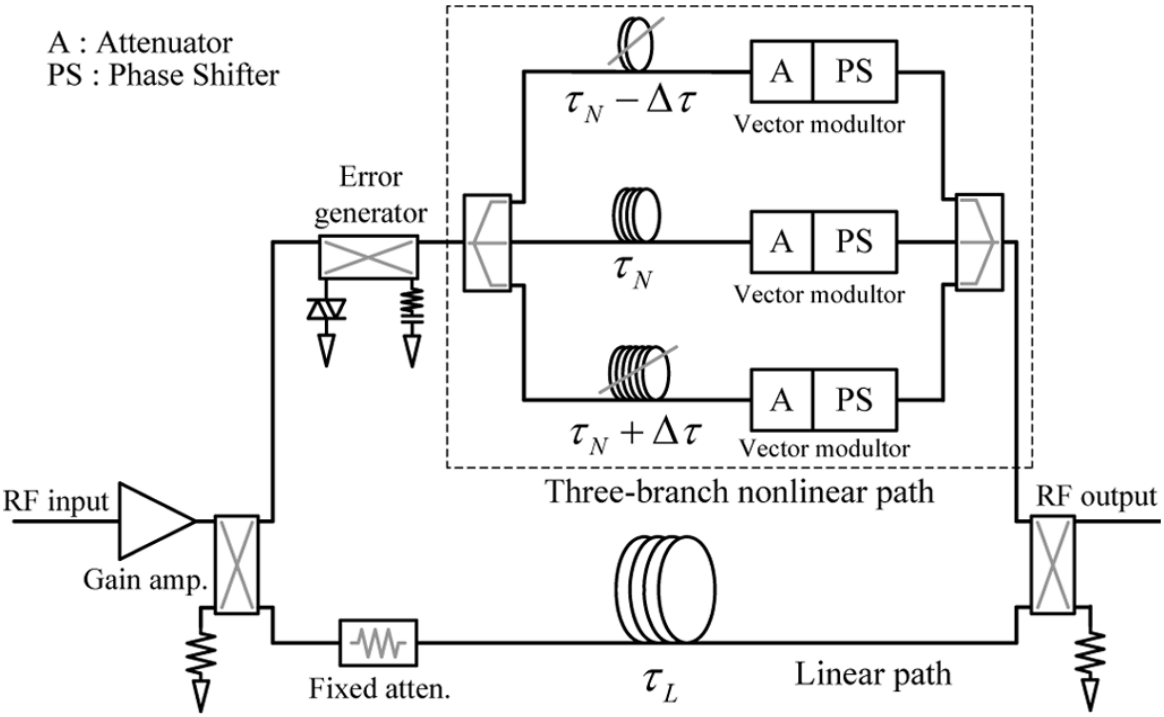

Figure 11. Multi-branch analogue predistortion schematic. [20]

There are two main paths in the scheme, a linear path and a nonlinear path that is splits into three branches. The two additional paths help mitigate memory effects. Both, the linear and nonlinear paths have a delay line to compensate for possible phase differences. Further amplitude and phase adjustments are done with an attenuator and a phase shifter. The memory effect compensating paths have additional variable Δτ in the delay line. The variable is used to either to shorten to lengthen the delay experienced in the path. By controlling the variable, the memory effects can be compensated for. It is possible to improve the design and thus the linearity by adding additional nonlinear paths with different relation to Δτ.[20]

2.5.2 Analog pre-distortion circuit for radio over fiber transmission

Compared to the last analogue predistortion example, the linearization method proposed in this article [21] is substantially less complex. The scheme is meant for radio over fiber systems and is designed to suppress third and fifth order intermodulation distortion. Broadband Schottky diodes function as the distorting elements; they are located in two separate branches in an anti-parallel configuration. A schematic for the scheme is shown in Figure 12. [21]

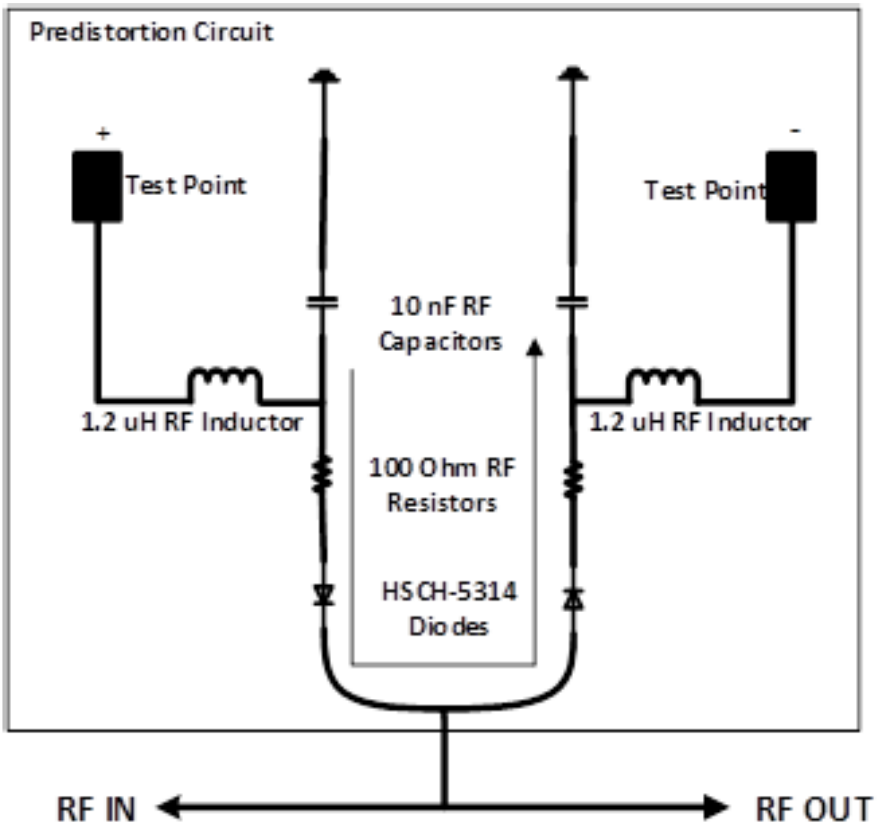

Figure 12. Predistortion circuit for radio over fiber systems. [21]

The even order distortions generated by the Schottky diodes are almost completely suppressed thanks to the push-pull configuration. Series resistors in conjunction with a DC power supply bias the current that passes through the diodes. The power supply is connected to the test points, only one power supply is required for operation. The inductors and capacitors in the circuit function as a bias tee, so the DC bias does not interfere with the RF signal and vice versa. A power divider splits the RF input signal into the both branches. This linearization scheme is simple and has low power consumption and cost implementation. [21]

2.5.3 An E-BAND analog predistorter and power amplifier MMIC chipset

This predistortion scheme [22] meant for high frequency and wide bandwidth applications; the circuit is only designed to suppress IM3. The design consists of two branches: a linear branch and a nonlinear branch. A class C error amplifier functions as the distorter. The schematic for the predistorter is shown in Figure 13.[22]

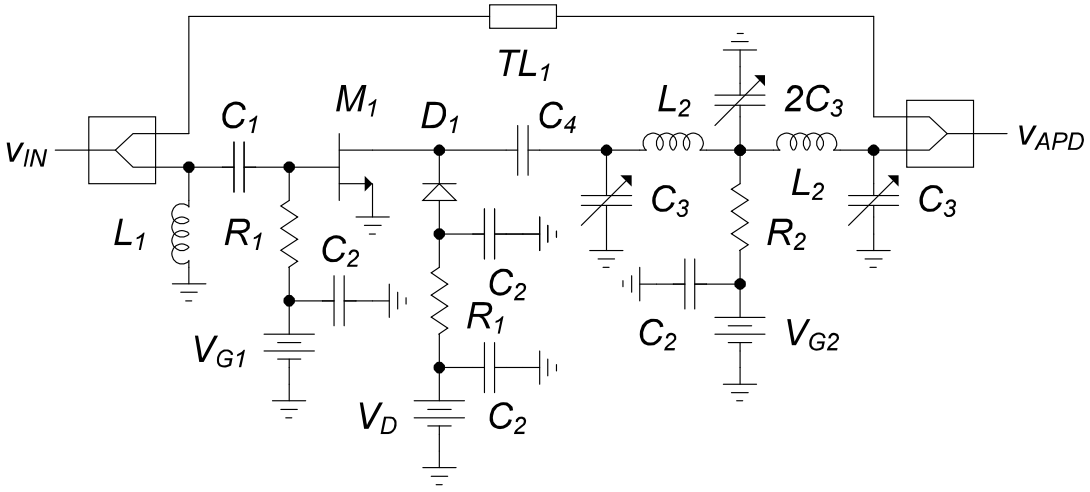

Figure 13. E-Band analogue predistorter schematic. [22]

The input and output both have an integrated Wilkinson power divider, for splitting the signal at the input and for combining at the output. Due to the high operating frequency, the dividers are realized with quarter wave transformer transmission lines. The linear path consists only of a transmission line to match the delays. To further ensure a matched delay, a variable delay line is included in the nonlinear path. The variable delay line is made of pi-section transmission lines constituting of varactors C_3 and inductors L_2. The phase in the delay line is controlled by V_{G2}. The third order predistortion coefficient is controlled by the error amplifier transistor gate bias V_{G1}. By adjusting V_{G1} and V_{G2} it is possible to adapt to outside factors such as changes in environmental temperature. However, it must be done manually due to the open-loop structure of the scheme. [22]

3. PREDISTORTION SCHEME

In the thesis, a logarithmic amplifier is used to linearize a BJT RF amplifier. The linearization technique is simple, the predistorter is cascaded with the amplifier. The scheme is shown in Figure 14.

Figure 14. Thesis predistortion scheme.

It is critical to understand the source of nonlinearity in BJTs, before the predistortion scheme is discussed. Furthermore, understanding of logarithmic amplifiers is required. Therefore, Ebers-Moll model and logarithmic amplifier are examined first.

3.1 Ebers-Moll model

Inside a BJT, there are two pn-junctions that effectively behave as diodes. The junctions are formed in between the three terminals, base B, collector C and emitter E. A simplified npn BJT is shown in Figure 15. Current directions are also shown in the figure: collector current is I_C, base current is I_B and emitter current is I_E. [23]

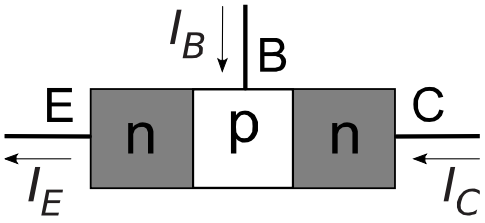

Figure 15. npn BJT consist of n and p-type semiconductor materials.

The pn-junctions are formed at the base-emitter (BE) and base-collector (BC) interfaces. As an electronic device, diode is nonlinear by nature. The current-voltage relationship in a pn-junction follows the Shockley-equation [13]. The current I_F flowing through the base-emitter pn-junction diode is expressed as the product of the reverse saturation current I_{SF} and an exponential function involving the voltage over the diode V_D, thermal voltage V_T and the ideality factor n

$$I_F = I_{SF}(e^{\frac{V_D}{nV_T}} - 1). \tag{6}$$

BJTs experience exponential dependence between voltage and current due to the pn-junctions as shown by (6). Ebers-Moll model describes a BJT as a circuit model. The model consists of two diodes that are connected back to back. The diodes represent base-emitter (BE) and base-collector (BC) pn-junctions. The base current is modelled by two current-controlled current sources and the currents I_R and I_F. One of the sources models the forward-biased operation and another one models the reverse-biased operation. The sources also have their own respective controlling coefficients, A_F for forward current I_F and A_R for the reverse current I_R. Ebers-Moll model for a npn BJT is shown in Figure 16. [23]

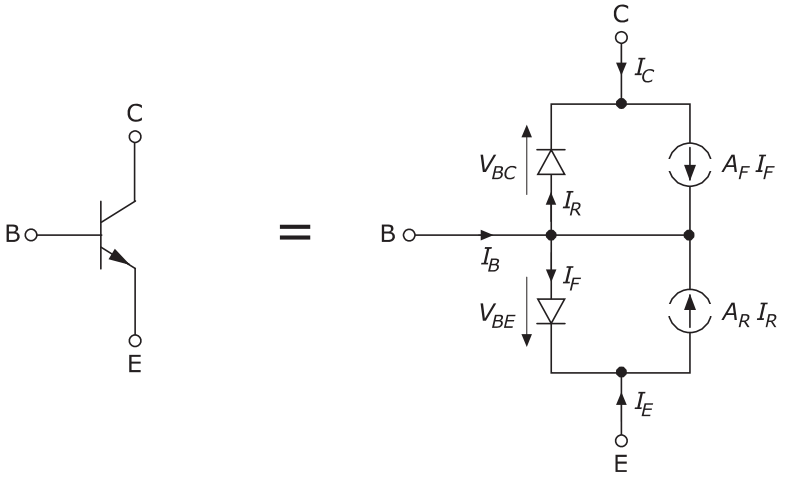

Figure 16. NPN BJT Ebers-Moll model. Modified from [23].

The currents can be expressed with the help of (6) and Kirchhoff's Current Law (KCL). The reverse current can be determined with (6) when applied to BC pn-junction

$$I_R = I_{SR}\left(e^{\frac{V_{BC}}{nV_T}} - 1\right). \tag{7}$$

The forward current has similar relationship with the BE pn-junction

$$I_F = I_{SF}(e^{\frac{V_{BE}}{nV_T}} - 1). \tag{8}$$

With KCL and equation (6) the collector and emitter currents are expressed as follows

$$I_C = A_F I_{SF}\left(e^{\frac{V_{BE}}{nV_T}} - 1\right) - I_{SR}\left(e^{\frac{V_{BC}}{nV_T}} - 1\right) = A_F I_F - I_R \tag{9}$$

$$I_E = A_R I_{SR}\left(e^{\frac{V_{BC}}{nV_T}} - 1\right) - I_{SF}\left(e^{\frac{V_{BE}}{nV_T}} - 1\right) = A_R I_R - I_F. \tag{10}$$

In forwards biased mode the current flows to the emitter, whereas in the reverse-biased mode, the current flows to the collector. Since in the thesis we are using the BJT as an amplifier, the device operates in forward-biased mode. In this mode $V_{BE} > 0$ and $V_{BC} < 0$.

Diodes have a turn-on voltage V_{ON} that is usually in range of 0.7V; if this voltage is not exceeded, then the junction is not conducting. Consequently, in the forward-biased mode the BE pn-junction conducts, while practically no current flows through the BC pn-junction

$$I_R \approx I_{SR} \approx 0. \tag{11}$$

This reduces the model to the state shown in Figure 17. [13, 23]

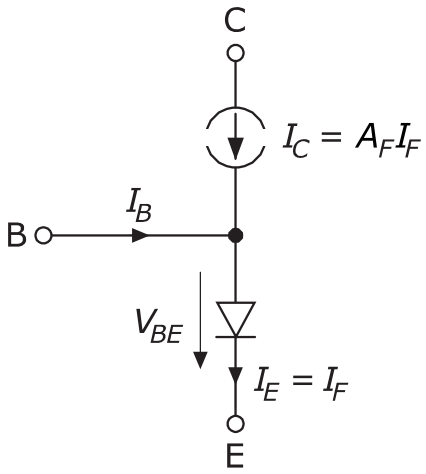

Figure 17. Reduced Ebers-Moll model for forward biased operation. Modified from [23].

Analyzing currents and voltages is now easier as we can ignore the BC pn-junction and the reverse biased source. However, this model only applies when the transistor is operating in the active region (Figure 2). The equations are simplified to

$$I_C = A_F I_{SF} \left(e^{\frac{V_{BE}}{nV_T}} - 1 \right) = A_F I_F \tag{12}$$

$$I_E = I_{SF} \left(e^{\frac{V_{BE}}{nV_T}} - 1 \right) = I_F. \tag{13}$$

The current-controlled current source coefficient for the forward biased source A_F is the ratio of the collector and emitter currents

$$A_F = \frac{I_C}{I_E}. \tag{14}$$

The emitter current in this mode of operation is the sum of the currents flowing through the base and collector

$$I_E = I_B + I_C. \tag{15}$$

The two base and collector currents are related by the DC current gain β that is typically in the range of hundreds

$$I_C = \beta I_B. \tag{16}$$

The relationship between A_F and β derived with the help of (14), (15) and (16), by first solving I_E from (14)

$$I_E = \frac{I_C}{A_F}. \tag{17}$$

Next, I_E is related to A_F and I_C by using (15) and (17)

$$I_B = I_E - I_C = \frac{I_C}{A_F} - I_C = \frac{I_C - A_F I_C}{A_F} = I_C \frac{(1-A_F)}{A_F}. \tag{18}$$

Finally, we can relate β to A_F by substituting (18) to (16) and by solving β

$$\beta = \frac{I_C}{I_B} = \frac{I_C}{I_C \frac{(1-A_F)}{A_F}} = \frac{A_F}{1-A_F}. \tag{19}$$

In forward operation A_F is a constant, since I_E is the sum of I_B and I_C, A_F is slightly smaller than 1. Additionally, $\beta \gg 1$, hence

$$I_C \gg I_B. \tag{20}$$

When (20) holds true, a gross simplification is possible in terms of emitter current:

$$I_E = I_{SF}\left(e^{\frac{V_{BE}}{nV_T}} - 1\right) \approx I_C \tag{21}$$

These simplifications make the analysis of a BJT considerably simpler. The exponential dependence is still present despite the simplifications. However, the model only applies when the device operates in the active region. With low DC operating point and high signal level, the instantaneous operation point swings out of the active region, rendering the model inaccurate. [23]

3.2 Logarithmic amplifier

Logarithmic amplifier is a nonlinear device by design; the amplifier output relates to the input logarithmically. First, we are going to examine a negative logarithmic amplifier and afterwards, a positive logarithmic amplifier. A component that exhibits logarithmic behavior is required. Conveniently, a pn-junction exhibits logarithmic behavior when examined in terms of junction voltage:

$$\frac{I_F}{I_{SF}} = e^{\frac{V_D}{nV_T}} - 1 \tag{22}$$

By rearranging the terms and taking a logarithm of each side we can solve the voltage over the junction

$$\ln(\frac{I_F}{I_{SF}} + 1) = \ln(e^{\frac{V_D}{nV_T}}). \tag{23}$$

The above equations ultimately simplifies to

$$V_D = nV_T \ln\left(\frac{I_F}{I_{SF}} + 1\right). \tag{24}$$

A logarithmic amplifier can consist of an operational amplifier and a diode that is connected as negative feedback element. The circuit is shown in Figure 18. [24]

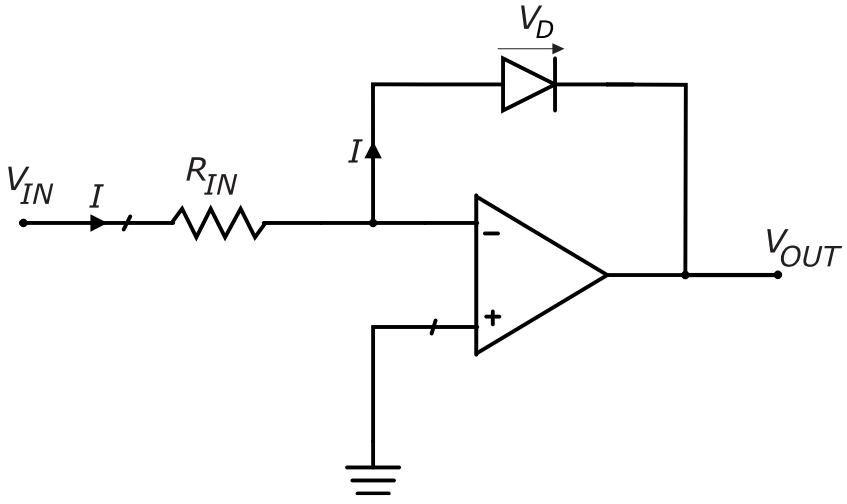

Figure 18. A negative logarithmic amplifier.

The operational amplifier attempts to keep the potential difference between the positive and negative inputs at zero, thus a virtual ground forms at the negative input. We can assume that practically all input current flows through the feedback loop as operational amplifiers have high input impedance, often in range of megaohms. Only a negligible amount of current leaks through the negative input. The anode is at greater potential than the cathode, hence the operational amplifier drives an output voltage V_{OUT}. Due to the

virtual ground, the amplifier drives equal but opposite voltage to the voltage over the diode V_D

$$V_{OUT} = -V_D. \tag{25}$$

V_D can be determined with (24) and KCL. Conveniently, the current is the same through the resistor and the diode. Subsequently, Ohm's law can be applied to (24) in addition to (25)

$$V_{OUT} = -nV_T \ln\left(\frac{V_{IN}}{R_{IN} I_{SF}} + 1\right). \tag{26}$$

The circuit can be converted into a positive logarithmic amplifier [6]. [24]

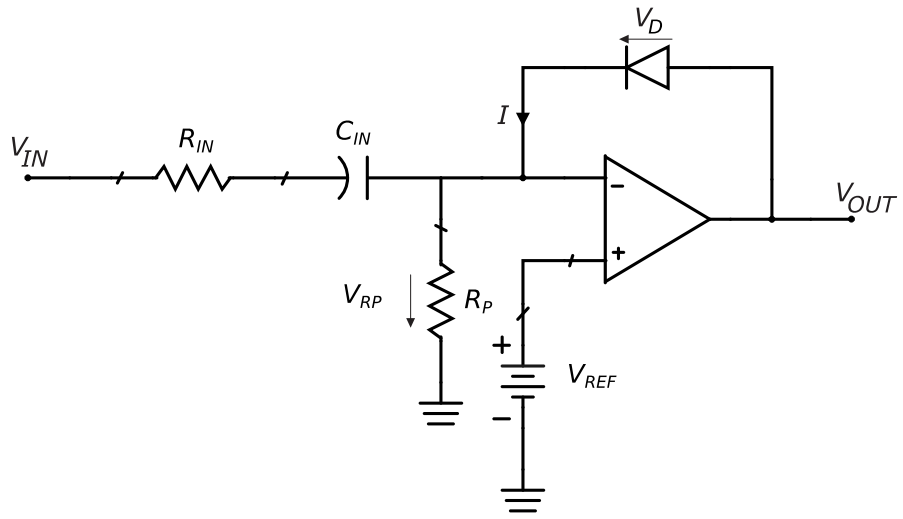

Figure 19. Positive logarithmic amplifier.

Three new components have been incorporated to the design, a DC-block capacitor C_{IN}, a reference DC-voltage source V_{REF} and a resistor R_P. Additionally, the cathode is now connected to the negative input and the anode to the output. Due to these changes, the direction of the current is now different than in Figure 18. The operational amplifier attempts to keep the potential difference between the inputs at zero. Consequently, the amplifier drives a DC-voltage equal to the reference voltage V_{REF} at the negative input.

$$V_{REF} = V_+ = V_-. \tag{27}$$

The reference voltage sets the operating point of the logarithmic amplifier. All the DC-current flows through R_P; as no DC-current passes through C_{IN} and the operational amplifier. Subsequently, the voltage V_{RP} over R_P is also equal to the reference voltage

$$V_{RP} = V_{REF}. \tag{28}$$

The AC-current flows through the input resistance R_{IN} and the diode, influencing the operating point set by V_{REF}. The input AC-current is equal but opposite to the diode current

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_{IN}} = -I_F \tag{29}$$

By utilizing KCL, we can determine the output voltage

$$V_{OUT} = V_D + V_{REF}. \tag{30}$$

Substituting (24) and (29) to (30) confirms the positive logarithmic dependence

$$V_{OUT} = nV_T \ln\left(\frac{I_F}{I_{SF}}\right) + V_{REF} = nV_T \ln\left(\frac{V_{REF} - V_{IN}}{R_{IN} I_{SF}} + 1\right) + V_{REF}. \tag{31}$$

However, the logarithm is finite and real only if the term $\frac{V_{REF} - V_{IN}}{R_{IN} I_{SF}}$ is greater than -1. Otherwise, the operational amplifier will saturate to supply voltage due to the logarithmic function approaching negative infinite. Consequently, the output is severely distorted. This can be avoided by increasing V_{REF} as this only occurs when the negative AC-voltage is exceeds the DC voltage. [6]

The diode in the logarithmic amplifier can be replaced with a transistor. Diode has a limited logarithmic dependence; ohmic resistance and temperature dependence are of concern, more so than with a transistor unless a costly "log diode" is used [24]. The logarithmic dependence may not be accurate with great input voltage variations, for instance if the input varies from picovolts to millivolts. A change in the temperature influences the thermal voltage V_T, affecting the response of the amplifier. V_T is product of the Boltzmann constant k and the temperature T divided by the elementary charge q

$$V_T = \frac{kT}{q}. \tag{32}$$

The reverse saturation current is also affected by the ambient and device temperatures. Transistors suffer from these issues to a lesser extent. Being three port devices, a wider array of configurations are available; allowing more specialized logarithmic amplifier implementations. As an additional benefit, transistors lend themselves more readily to different temperature compensation circuits. However, transistors are capable of amplifying signals. Consequently, stability issues may arise. In addition, compared to diodes, transistors are not as robust. At higher signal levels, a transistor might get damaged or destroyed. [6]

3.3 RF BJT amplifier linearization using an analogue predistortion logarithmic amplifier

The initial proposed linearization scheme is shown in Figure 20. The logarithmic amplifier is similar to the one in Figure 19, the main differences being the diode-connected transistor, the location of the reference source. Now, the positive input is grounded, and the reference source is connected to the negative input through resistor R_P. [5]

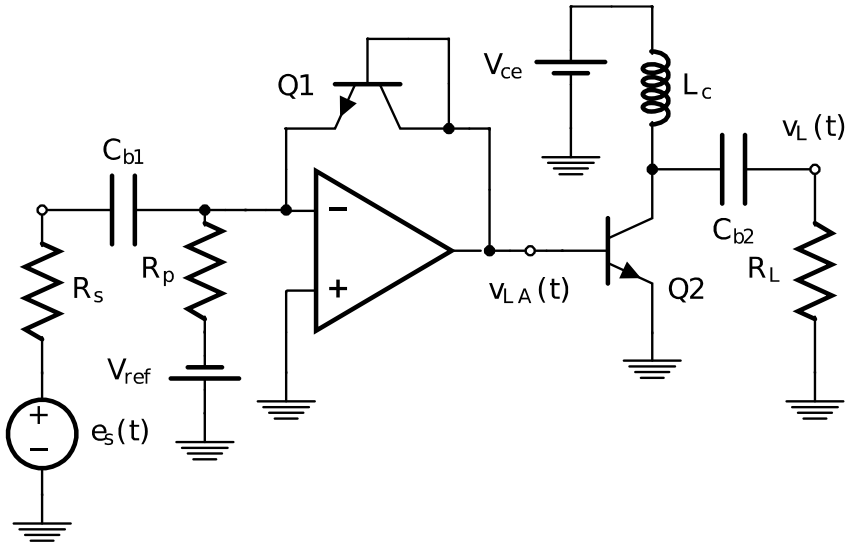

Figure 20. Proposed predistortion scheme of a BJT RF amplifier. [5]

A matched pair transistor is used [25], meaning the transistors Q1 and Q2 are almost identical. Therefore, the circuit analysis is simplified as the ideality factors and the reverse saturation currents assumed equal

$$n_1 = n_2 \tag{33}$$

$$I_{SF1} = I_{SF2}. \tag{34}$$

The DC-current gain is also in the range of 60-250 [25] , hence the gross simplification in (21) is viable. [5]

Since the positive input is connected directly to ground, a virtual ground is formed at the negative input. We can utilize (24) to determine the base-emitter voltage for Q1. The emitter current in the equation below follows the relation shown in (21)

$$V_{BE1} = n_1 V_T \ln\left(\frac{i_{E1}}{I_{SF1}} + 1\right). \tag{35}$$

The operational amplifier output is directly connected to the base of the second transistor Q2. Due to the virtual ground we can assume that the base-emitter voltages are equal

$$V_{BE1} = V_{BE2}. \tag{36}$$

The DC-currents flowing through the transistors are determined by the reference voltage and the resistor R_P

$$I_{E1} = I_{C1} = I_{C2} = \frac{V_{ref}}{R_p}. \tag{37}$$

From (37) it becomes apparent that this linearization scheme at least doubles the current consumption, as the currents through both the transistors are equal. In addition, the operational amplifier draws quiescent current. [5]

If the BJT amplifier transistor Q2 operates in the active region, in the configuration shown in Figure 20, then the collector current can be expressed with the help of (21), (35) and (36). The earlier simplifications (33) and (34) also greatly assist with the current analysis

$$i_{c2} = I_{SF2}\left(e^{\frac{V_{BE2}}{n_2 V_T}} - 1\right) \tag{38}$$

$$= I_{SF2}\left(e^{\frac{n_1 V_T \ln(\frac{i_E}{I_{SF1}}+1)}{n_2 V_T}} - 1\right) \tag{39}$$

$$= I_{SF2}\left(\frac{i_E}{I_{SF1}} + 1 - 1\right) \tag{40}$$

$$= i_{E1}. \tag{41}$$

Only AC-current flows to the load due to the decoupling capacitor at the BJT amplifier output. Consequently, the load current is completely compromised of AC-current. Due to the RF choke inductor, the load current i_L is the negative of the collector current.

$$i_L = -i_{c2} = -i_{E1} \tag{42}$$

Q1 current AC-component is the same as the system input current due to the AC-current having no other viable path; the potentials at both ends of R_P are at constant value and the input impedance of the operational amplifier is typically in range of megaohms. The input AC-current flows through the resistor R_S, no DC-current flows through the resistor due

to the decoupling capacitor at the input. Therefore, the input current can be written with the help of Ohm's law

$$i_{IN} = \frac{e_s}{R_s} = -i_{E1}. \tag{43}$$

Now the load voltage is

$$v_L = R_L * -\left(-\frac{e_s}{R_s}\right) = (\frac{R_L}{R_s})e_s. \tag{44}$$

The gain of the linearized amplifier can be estimated by determining the transducer power gain G_T. The transducer gain in decibels is the ten times the logarithm of the ratio of the load power P_L and available power than can be drawn from the source P_{avg}:

$$G_T = 10\log\left(\frac{P_L}{P_{avg}}\right)\text{dB}. \tag{45}$$

The load power can be obtained by applying (44) to the power equation:

$$P_L = V_L^2/R_L = \frac{e_s^2 R_L}{R_s^2} \tag{46}$$

The available power is square of the absolute value of the input voltage divided by four times the real part of the source impedance

$$P_{avg} = \frac{e_s^2}{4R_s}. \tag{47}$$

Now we can determine the transducer gain as

$$G_T = 10\log\left(\frac{\frac{e_s^2 R_L}{R_s^2}}{\frac{e_s^2}{4R_s}}\right)\text{dB} = 10\log\left(\frac{4R_L}{R_s}\right)\text{dB}. \tag{48}$$

The transducer gain is only affected by the load and source impedances. Other parameters such as transistor or operational amplifier parameters have no apparent effect on the gain. In a 50 Ω system $R_s = R_L = 50\ \Omega$, resulting in gain of $G_T = 6$ dB. With a different load impedance $R_L = 500\ \Omega$, the gain is $G_T = 16$ dB.

4. VERIFICATION

The system was implemented, and intermodulation measurements were conducted to verify the viability of the scheme. Target specifications were as follows: the system was to operate at 3 MHz, the current through both the transistors was chosen to be 5 mA, and the circuit was to be unconditionally stable. Additional side projects were also undertaken to facilitate the intermodulation measurements and measuring with different load impedances.

4.1 Implementation

For the implementation, BFM520 [25] was chosen as the matched pair transistor and AD8055 [26] as the operational amplifier. However, changes had to be made to the original design. The final design is shown in Figure 21.

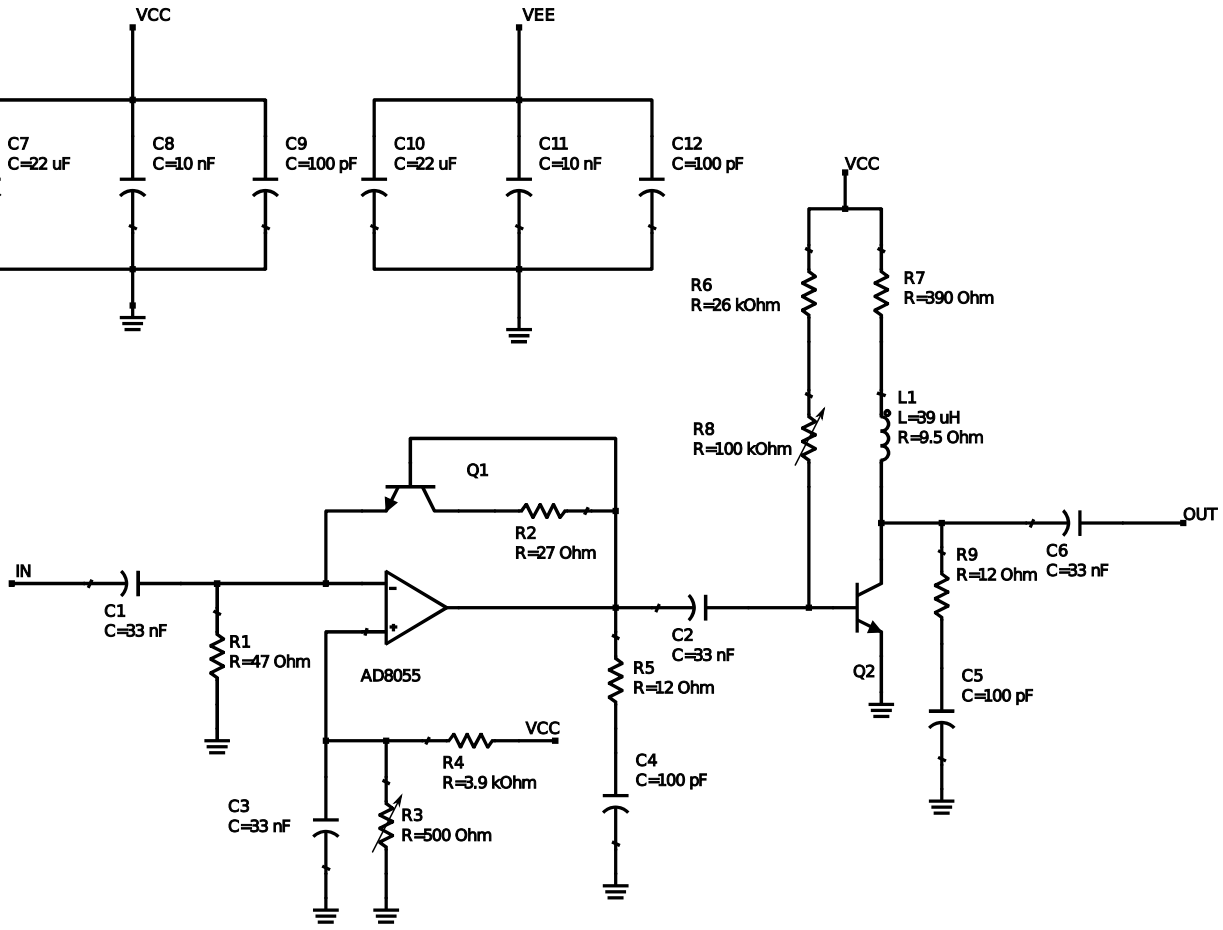

Figure 21. The final implementation of the predistortion scheme.

There are three major differences between the final and the initial designs. The BJT and logarithmic amplifier are DC-decoupled with capacitor C2, hence both amplifiers have

their own separate biasing circuitry. This approach was chosen because even though the transistors are a matched pair, they are not completely identical. Separate biasing circuitry can alleviate the situation. Furthermore, during the initial tests, it was observed that Q2 would draw current in order of hundreds of milliamps with certain logarithmic amplifier bias conditions. Absolute maximum DC collector current rating for BFM520 is 70 mA [25]. Stabilization circuitry has been incorporated to the design. Lastly, the reference source is replaced with a voltage divider circuit and moved to the positive input of the operational amplifier. Fortunately, the AC-operation is not affected as the amplifiers are DC-decoupled, thus (44) still holds true.

The operational amplifier uses dual side supply, +5 V positive supply voltage VCC and -5 V negative supply voltage VEE. Capacitors C7 – C9 filter the ripple voltage in VCC and C10 – C12 are used for VEE. For convenience, the reference voltage is supplied by a voltage divider instead of a DC-voltage source. The voltage is controlled by variable resistor *R3*

$$V_{ref} = (\frac{R3}{R3+R4})V_{CC}. \tag{49}$$

R4 is a fixed value resistor with a resistance of 3.9 kΩ, *R3* ranges from 0 Ω to 500 Ω. The minimum reference voltage is 0 V and the maximum is 568 mV. Consequently, I_C can range from 0 mA to 12 mA. The collector currents were chosen to be 5 mA, hence according to (37) V_{ref} biased to 235 mV. For the BJT RF amplified, the Collector-emitter voltage was chosen as 3 V. *R7* biases the collector current, *R6* and *R8* bias the base current. *R8* is a variable resistor with resistance ranging from 0 Ω to 100 kΩ, allowing making changes to bias conditions on the fly. However, if the resistance *R8* is too low, then AC-current could flow to the power supply. Therefore, a fixed value 26 kΩ resistor *R6* is included. The collector resistor *R7* is only 390 Ω, thus an inductor is required at the collector. The required value for *R7* was determined with Ohm's law. V_{CE} is 3 V, this leaves 2 V over the *R7* and the current through it is 5 mA: $R7 = \frac{2\text{ V}}{5\text{ mA}} = 400\ \Omega$. Closest available resistance value was 390 Ω. The DC-current gain for BFM520 ranges from 60 to 250, for calculations it was estimated that β is 120 and the V_{BE} is 0.8 V [25]. These estimates were based on prior test measurements. With Ohm's law, KCL and (14) the we can determine the total base resistance *R6* + *R8* (R_B) as follows

$$R_B = \frac{(V_{CC}-V_{BE})}{\frac{I_C}{\beta}} = \frac{\beta(V_{CC}-V_{BE})}{I_C} = \frac{120(5\text{ V}-0.8\text{ V})}{5\text{ mA}} = 100.8\text{ k}\Omega, \tag{50}$$

therefore, *R8* should be set to 74.8 k Ω.

Stabilization circuitry is incorporated to both the amplifiers. Resistor *R9* and a capacitor *C5* is introduced between Q2 collector and the ground. Identical circuitry is also introduced between the ground and the logarithmic amplifier output. Due to the capacitors, the circuitry does not affect the DC-biasing. Capacitance values are sufficiently low, so that the effect on the fundamental frequency is minimal. At 100 pF, the impedance of the stabilization circuitry approximately 3 kΩ is for a 3 MHz RF signal. The circuits help eliminate higher frequency spurious oscillations.

Despite the efforts to stabilize the circuit against high frequency spurious oscillations, the system persistently suffered from oscillation in the frequency range of 3 GHz – 7 GHz. During the thesis work, we found that a diode-connected transistor can have negative resistance when the transsusceptance is high. Consequently, at higher frequencies, the diode-connected transistor can be unstable. This is contrary to what is claimed in literature; according to [24] diode-connected transistors can not produce gain, thus stability is always achieved.. Simulations with Advanced Design System 2017 (ADS) [27] were utilized to confirm the findings. The simulation circuits are found in APPENDIX 1. Figure 22 shows that the transistor can oscillate at higher frequencies.

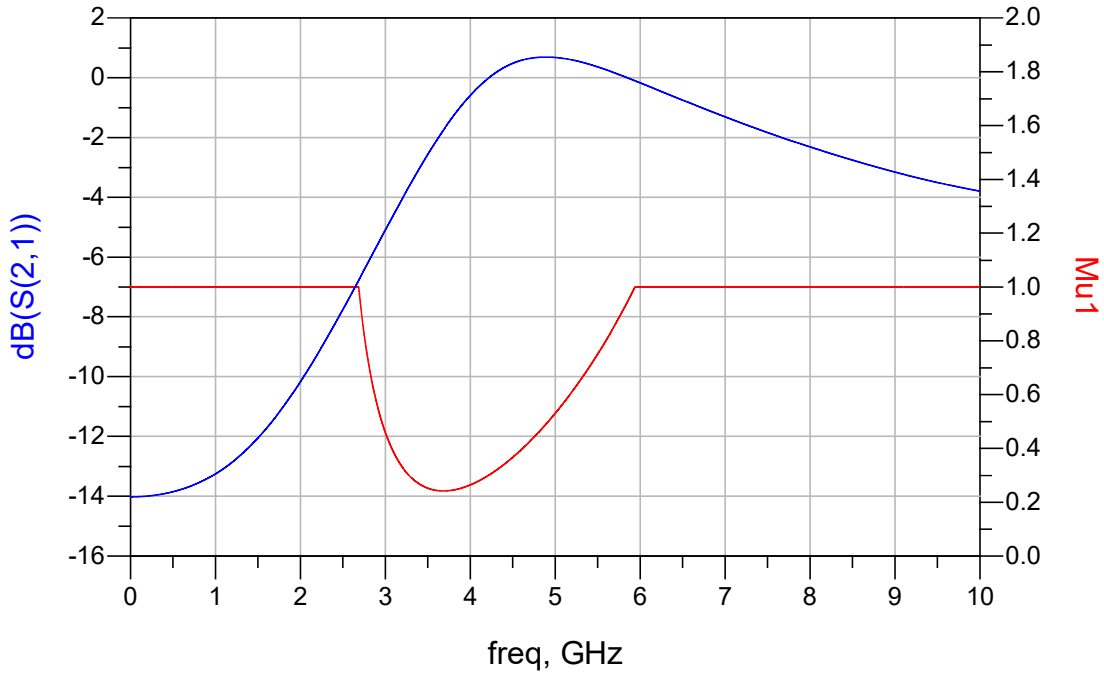

Figure 22. Simulated gain S21 and stability factor μ (Mu) for a diode-connected transistor. The circuit amplifies from 4.2 GHz to 5.85 GHz. If μ is below 1, then the circuit is potentially unstable.

As the frequency increases, the transistor attenuates less. At certain frequencies the transistor even amplifies the signal. To remedy the stability issue with minimal effect on the performance, 27 Ω resistor *R2* was connected in series with the collector. The simulation results for the stabilized diode-connected transistor are shown in Figure 23.

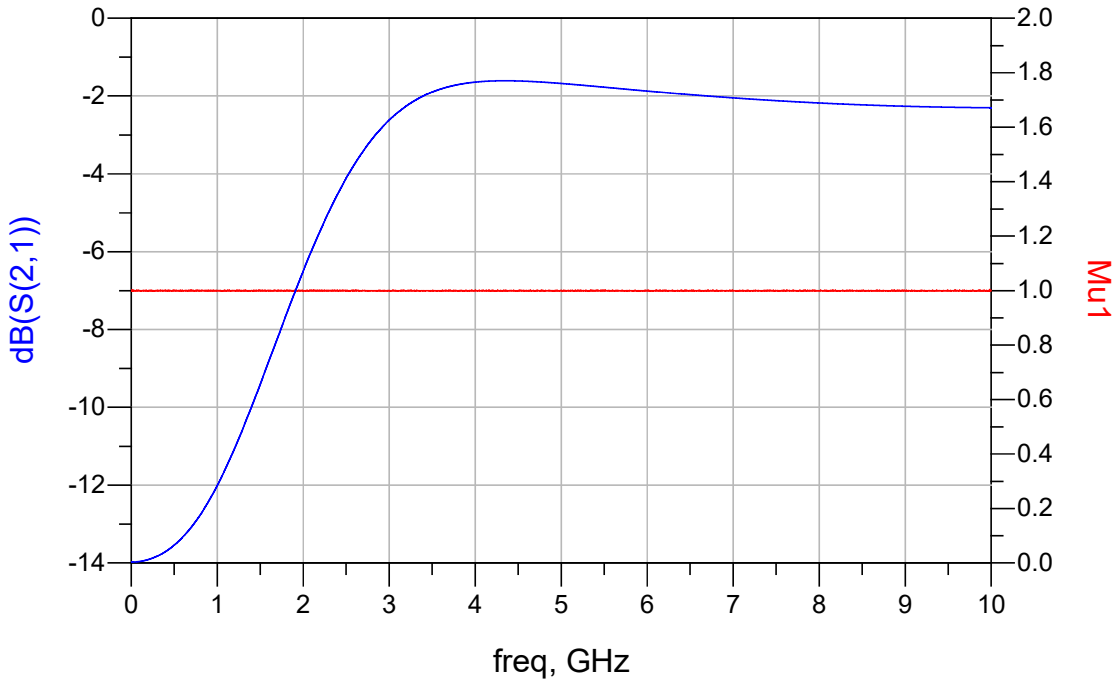

Figure 23. Simulated gain and stability factor Mu for a stabilized diode-connected transistor circuit.

The stability factor now remains at 1 regardless of the gain. In addition, the gain now does not exceed 0 dB, meaning that the transistor attenuates at all frequencies. Simulations at higher frequencies is unnecessary, since the transition frequency for BFM520 is at 9 GHz [25].

A layout was designed with EAGLE 8.3.0 [28]. Certain criteria were established for the layout. The circuit was to be built on two sided FR4 board. The RF paths on the board were to be as short as possible while maintaining hand solderability. In addition, the components were to be placed in a manner that they could be easily changed later. The top side of the layout is shown in Figure 24. The pads on the layout are related to schematic in Figure 21 by red component and signal designations. If a component pad does not have a designation in the figure, it means that particular pad was left open. Green line between pads means that pad was shorted in the final implementation. More information about the layout pads is presented in APPENDIX 2.

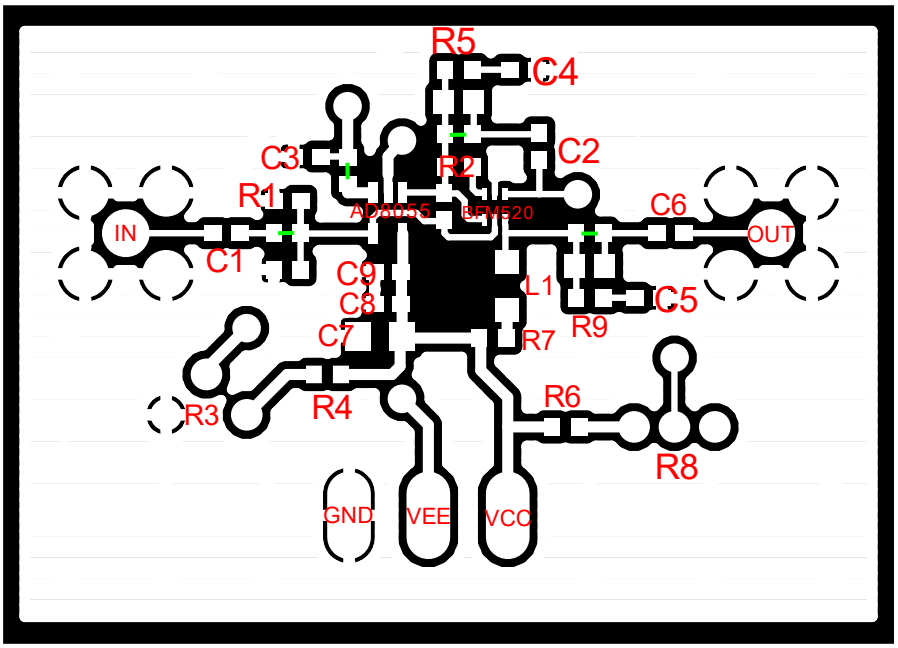

Figure 24. Top copper layer. The layout is a negative: white is copper and black is the exposed FR4 substrate. Note, the layouts in the figures are not to actual scale.

All the critical RF paths are kept on the top layer. The RF signal travels from left to right in the layout. SMA connectors serve as RF interface for coaxial cables. The supply voltages are connected through a screw terminal. Also, due to the lack of variable resistors, *R3* and *R8* are replaced with potentiometers. The bottom layer is presented in Figure 25.

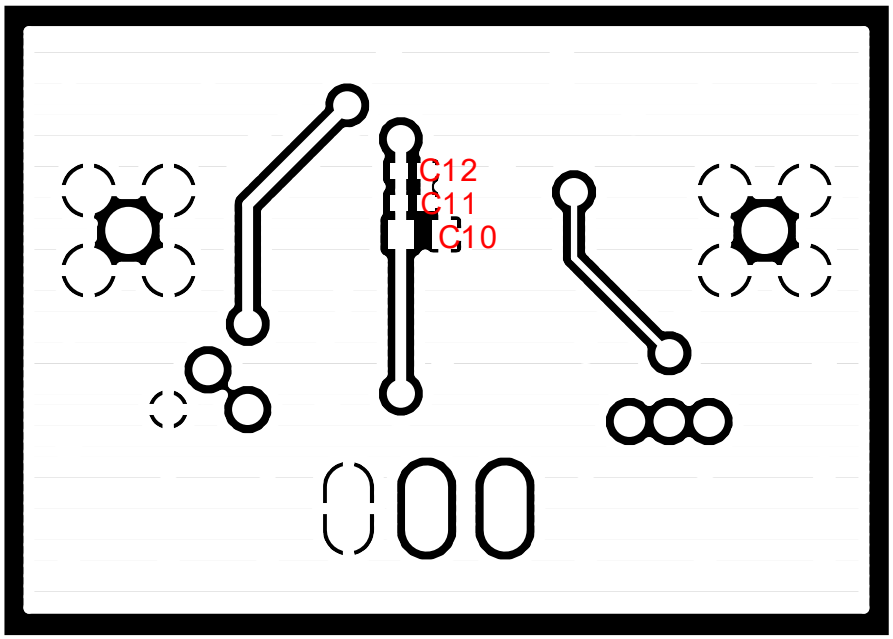

Figure 25. Bottom copper layer.

The bottom layer mostly serves as a ground plane, but due to space constraints in the top layer, part of the DC biasing traces go through the bottom. The capacitors for filtering the ripple voltage in VEE are also located on this layer. The constructed device is shown in Figure 26 and Figure 27.

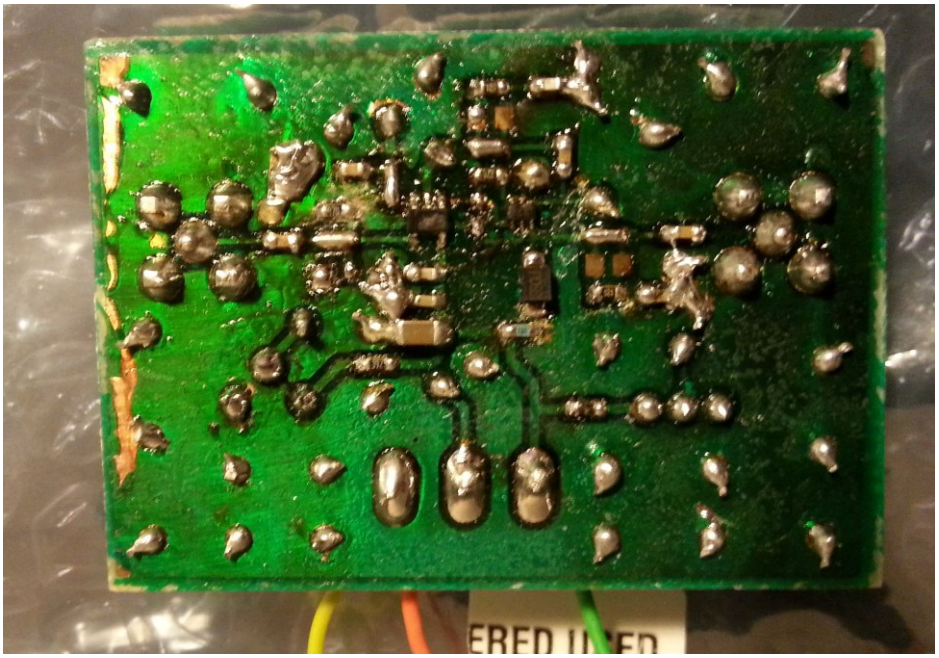

Figure 26. Top layer of the implementation.

Figure 27. Bottom layer of the implementation.

The bottom layer included all the cable interfaces, while top layer essentially has all the other components. The solder mask and drill holes were not included in the layers presented in this chapter, they are found in APPENDIX 2.

4.2 Side projects

Certain preparations had to be made before the measurements. A reference amplifier was needed to gauge the efficacy of the linearization scheme. Therefore, in addition to the linearized amplifier, a separate BJT RF amplifier was constructed. A suitable power combiner was needed for 3 MHz. Lack of an appropriate impedance converter also was an issue. Therefore, a power combiner and an impedance converter for 3 MHz were included in the thesis as necessary side projects. Lastly, the measurement setup was tested.

4.2.1 Wilkinson Power Divider

The linearity of the measurement equipment was the deciding factor when the power combiner architecture was chosen. We did not want the nonlinearities of the measurement equipment to affect the measurements. Wilkinson Power Divider has exceptional isolation between input ports. Therefore, we opted to implement a Wilkinson Power Divider. It is reciprocal since it only consists of transmission lines and passive components. Architecture for a microstrip based Wilkinson Power Divider is shown in Figure 28. [29]

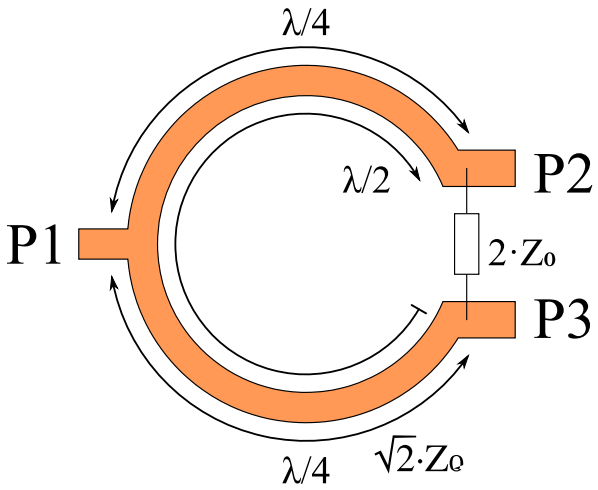

Figure 28. Wilkinson Power Divider architecture based on microstrip lines. Ports P2 and P3 are the input ports and P1 is the output port when the divider is operated as power combiner. The wavelength is denoted by λ and the characteristic impedance by Z_0. [30]

The power combiner consists of two quarter wave transformers and a resistor between the input ports. The input power is split between the output port P1 and resistor, that decouples P2 and P3 and provides impedance matching. However, part of the power might still leak from port P2 to P3 and vice versa. Since the paths from P2 to P1 and P3 to P1 are quarter wave transformers, the path between P2 and P3 is effectively a half wave

impedance transformer. Consequently, leakage through the transmission lines and the resistor have 180° phase difference and the same amplitude. Therefore, they cancel each other, ensuring complete isolation between ports P2 and P3. [29]

At 3 MHz, realizing a quarter wave transformer with a microstrip line is not feasible, since the wavelength is in the order of tens of metres which is impractical. Fortunately, a quarter wave transformer can also be implemented with passive components. A lumped element equivalent circuit for a short transmission line is shown in Figure 29. [15]

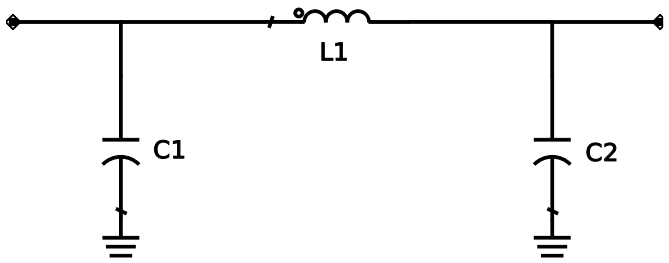

Figure 29. Lumped element model for a short transmission line.

The circuit works in both directions and is symmetrical. The measurement equipment and cables have characteristics impedance of $Z_0 = 50\ \Omega$. Therefore, we design a Wilkinson Power Divider for 50 Ω system. Impedance for a quarter wave transformer is $Z = \sqrt{2}Z_0$ [29]. We can use the capacitive and inductive reactance to determine the desired component values

$$X_C = \frac{1}{2\pi fC} = \sqrt{2}Z_0 \tag{51}$$

$$\mathrm{C} = \frac{1}{2\pi f\sqrt{2}Z_0} = \frac{1}{2\pi(3)(10^6\mathrm{Hz})(\sqrt{2})(50\ \Omega)} = 750\ \mathrm{pF} \tag{52}$$

$$X_L = 2\pi fL = \sqrt{2}Z_0 \tag{53}$$

$$L = \frac{\sqrt{2}Z_0}{2\pi f} = \frac{\sqrt{2}(50\ \Omega)}{2\pi(3)(10^6\mathrm{Hz})} = 3.75\ \mathrm{nH}. \tag{54}$$

The resistance is determined as follows [29]

$$R = 2Z_0 = 2(50\ \Omega) = 100\ \Omega. \tag{55}$$

The schematic for the Wilkinson Power Divider is presented in Figure 30. Component values are slightly different, and two capacitors have been added in series with the inductors. The additional capacitors compensate for the inductive reactance. The changes had

to be made due to lack of suitable components, as only E12 series components were available. The layout for the Wilkinson Power Divider is included in APPENDIX 3.

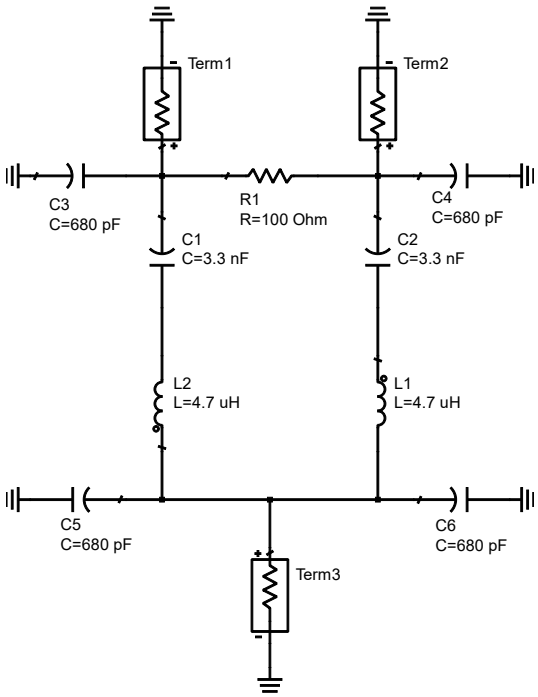

Figure 30. Wilkinson Power Divider for 3 MHz.

The measured isolation and insertion loss of the Wilkinson Power Divider are shown in Figure 31.

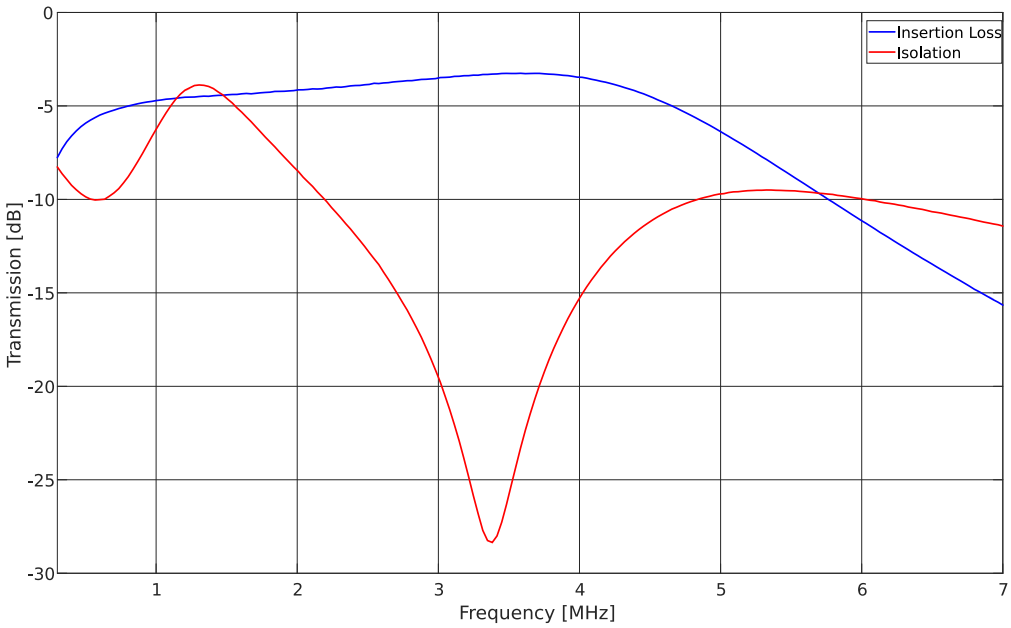

Figure 31. Measured Insertion loss and isolation for the Wilkinson Power Divider.

The maximum isolation of -28 dB is achieved at 3.3 MHz, while the insertion loss between the input and output is at its lowest at 3.6 MHz. The lowest loss being -3.25 dB. Since maximum isolation was desired for the measurements, the operation and measurement frequency for the predistorter implementation was changed to 3.3 MHz. Lastly, the impedance for each port was measured with a VNA. Only one impedance graph is included Figure 32 because the impedances were almost identical.

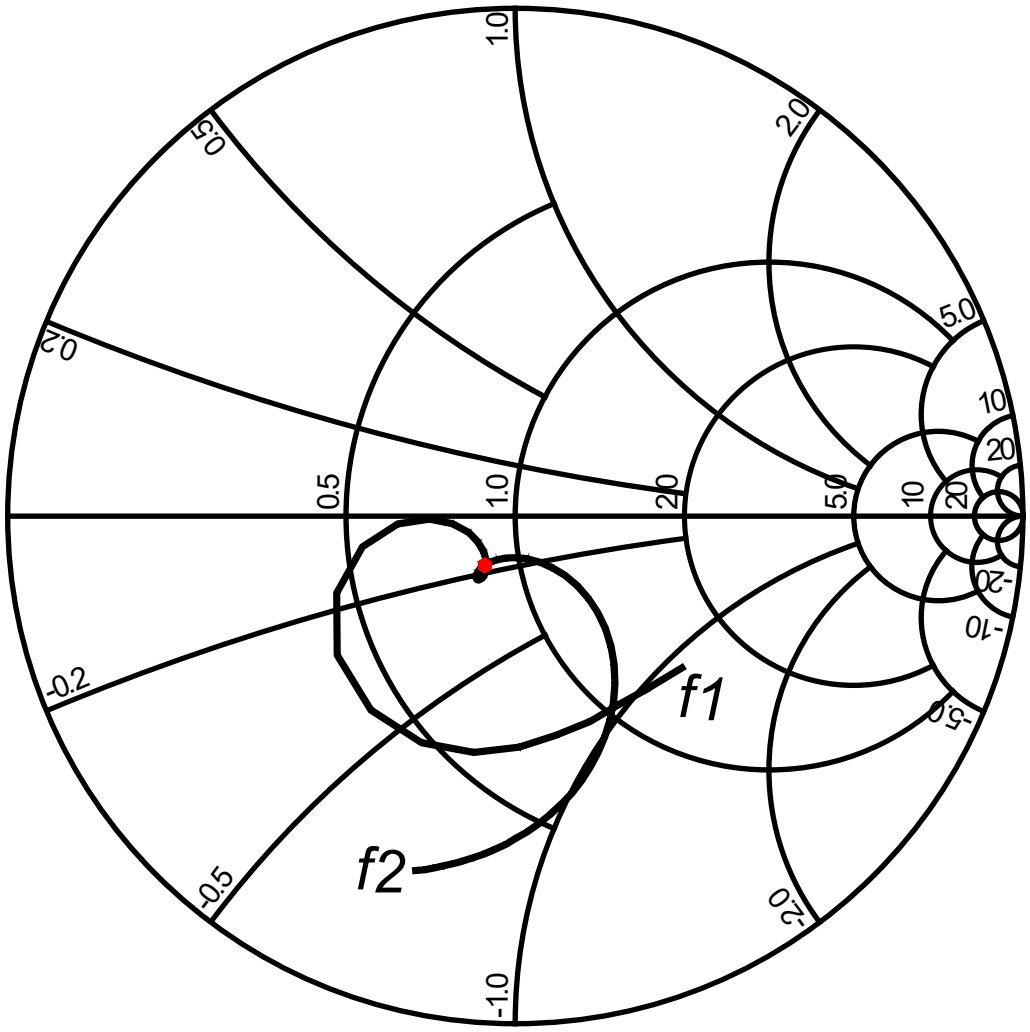

Figure 32. Wilkinson Power Divider impedance, measured impedance at 3.3 MHz is $Z = Z_0(0.870 - j0.171)$. Note, the impedance is normalized. A red dot in the chart marks the impedance at 3.3 MHz. The frequency sweep was from $f_1 = 300$ kHz to $f_2 = 7$ MHz. The graph start and end frequencies are marked shown in the plot.

The impedance match is not perfect. This becomes evident when the return loss is examined in Figure 33.

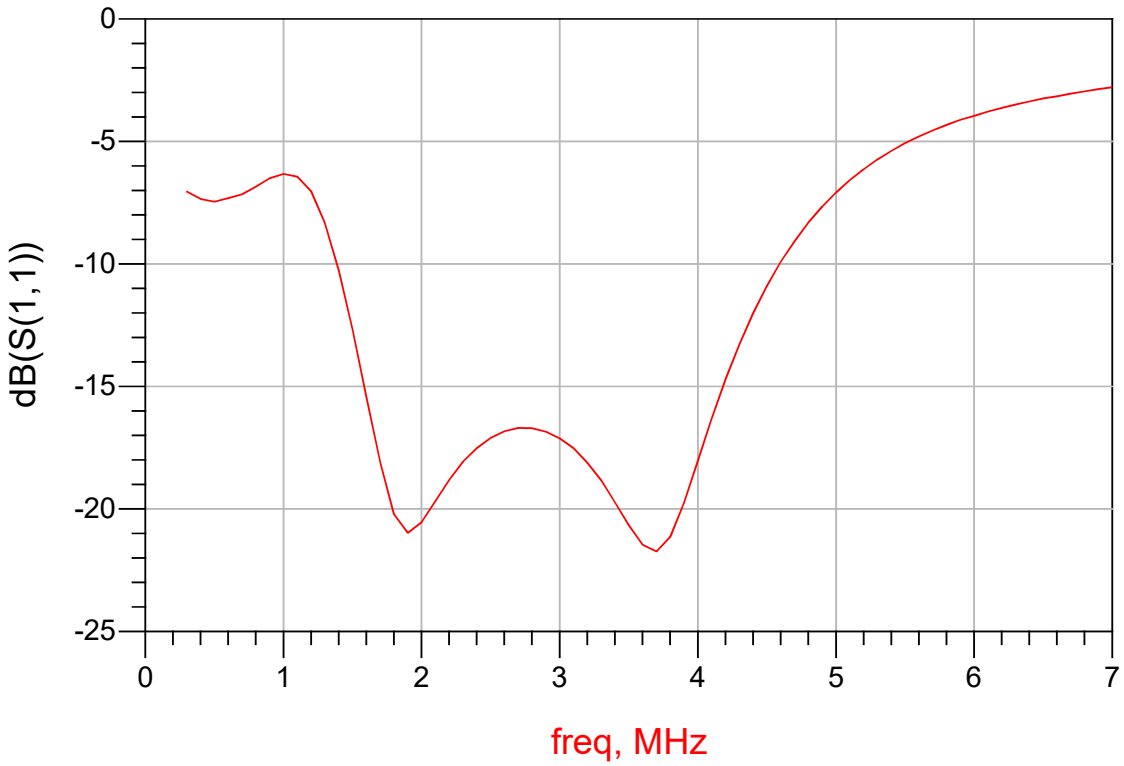

Figure 33. Return loss (S11) for the Wilkinson Power Divider.

At 3.3 MHz the returns loss is approximately -19 dB, meaning a couple percent of the incident power is reflected [15]. However, this most likely only has a negligible effect on the measurements if certain precautions are taken. These precautions will be discussed later.

4.2.2 Impedance transformer

An impedance transformer was required to verify how the system operates with different load impedances. We needed to transform the input impedance from 50 Ω to 500 Ω to verify the gain analysis performed earlier. The losses introduced by the transformer were to be kept at minimum, thus we opted for a LC high-pass impedance transformer. The circuit is shown in Figure 34. The layout is found in APPENDIX 4.

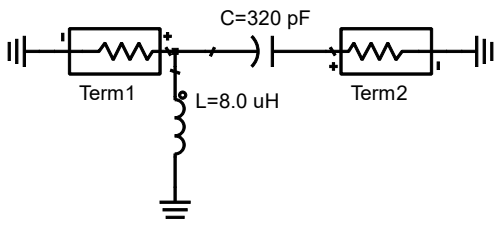

Figure 34. Schematic for the impedance transformer. The component values in the schematic are for a matching circuit that operates at 3.3 MHz.

The transformer consists of a series capacitor and a shunt inductor. A Smith's chart tool [31] was used to determine the required inductance and capacitance as seen in Figure 35.

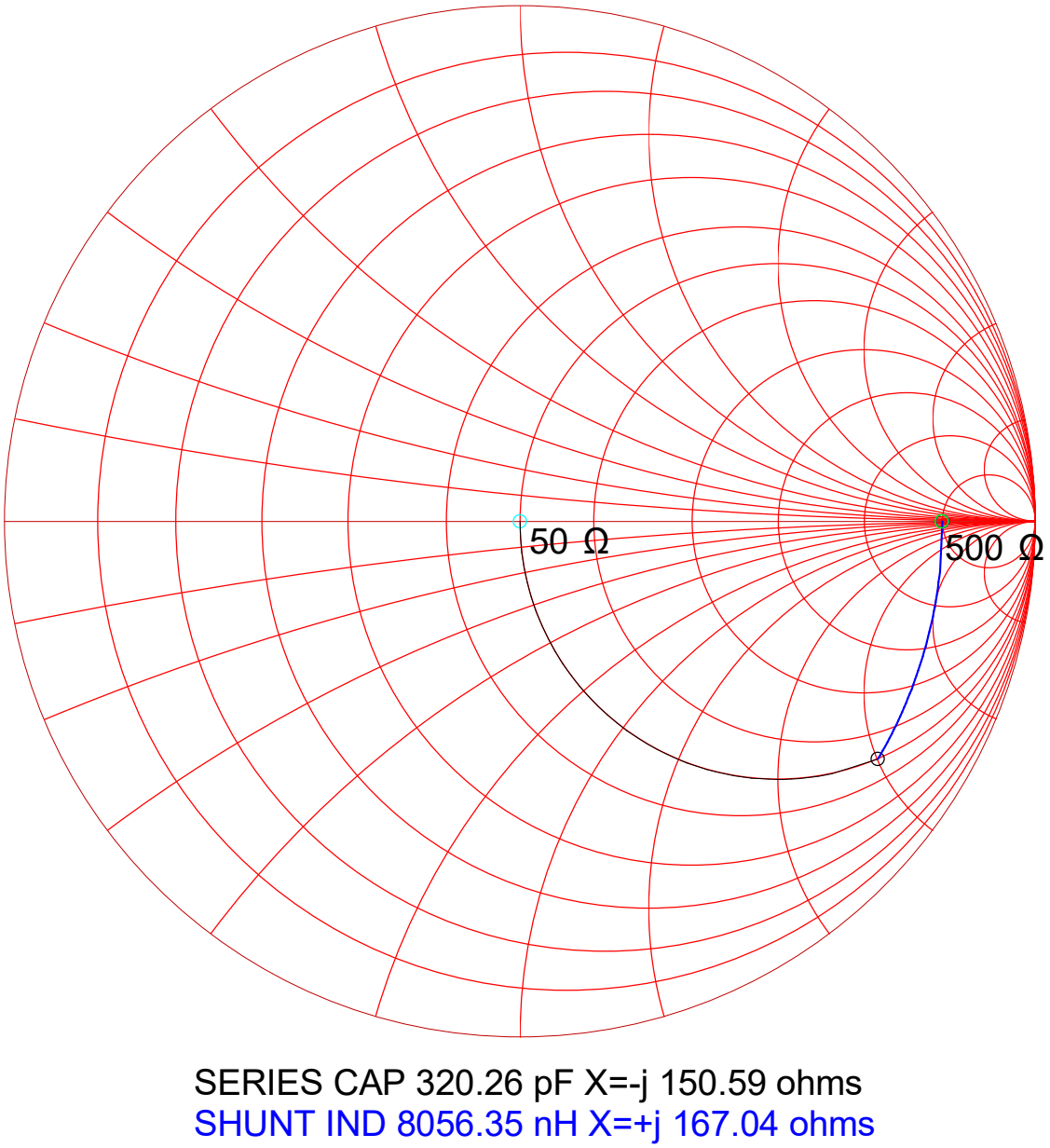

Figure 35. Determining the capacitance and inductance for the impedance transformer with Smith's chart.

The circuit was tested with a VNA after it was constructed. The measurements indicated the transformer worked as intended, the impedance is plotted in Figure 36.

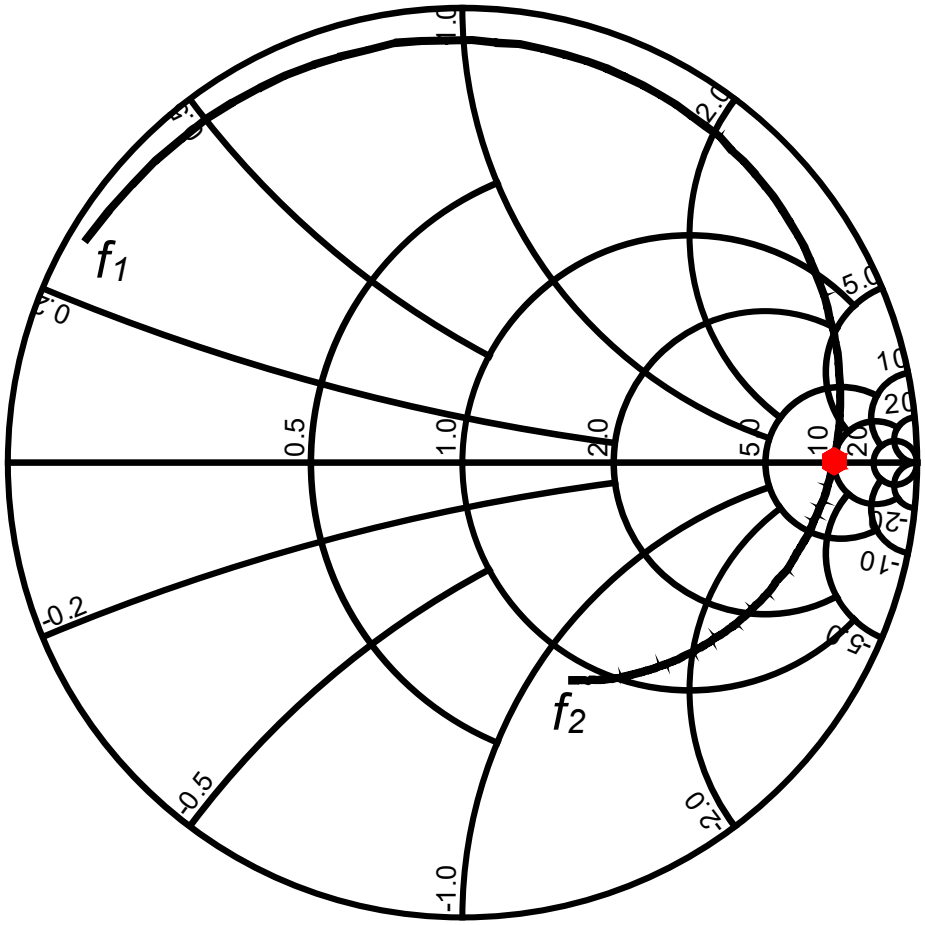

Figure 36. Measured impedance from $f_1 = 300$ kHz to $f_2 = 7$ MHz. 500 Ω impedance is marked with a red dot.

However, due to component tolerances, the desired impedance of 500 Ω was attained at 3.15 MHz. Consequently, it was decided that the measurements are to be conducted at 3.15 MHz when the system is measured with the matching circuitry.

4.2.3 Measurement setup

A block diagram of the planned measurement setup is shown in Figure 37.

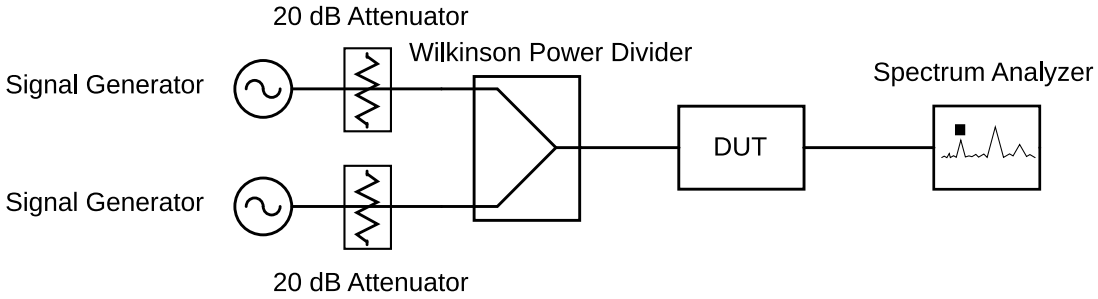

Figure 37. Block diagram for the measurement setup. DUT stands for “Device Under Test” (DUT).

Two signal generators are required for the intermodulation measurements. Generators are set to provide a 3.3 MHz signal and a 3.4 MHz signal. The attenuators between the generators and the power divider increase the path loss from one generator to another, thus minimizing the risk of intermodulation distortion occurring in the generators. With the attenuators in place, the reflections are attenuated at least by 43 dB as the divider also attenuates approximately by 3 dB. The two fundamental frequencies are combined in the power divider and fed to the DUT. The DUT is either the linearized amplifier or the reference amplifier. A spectrum analyzer is used to measure the output signal of the DUT. However, the DUT is to warm up before measurements, otherwise the change in the device temperature affect the results.

Before proceeding with the intermodulation measurements, the measurement setup itself was measured for nonlinearities. Nonlinearity of the measurement setup was gauged by removing the DUT and connecting the power divider directly to the spectrum analyzer. Input power was gradually increased until the maximum power of 14.5 dBm for the signal generator was reached. Third order intermodulation products were visible with the maximum power. They were measured to have power level of -77 dBm and -80 dBm. These values were deemed to have a negligible effect on the actual measurements as the products were only visible with the maximum power.

4.3 Measurements and simulations

Intermodulation measurements were conducted for the linearized amplifier and for the reference amplifier. However, only third order intermodulation products were measured. Fifth order products were only visible when the DUTs were behaving strongly nonlinearly. At that point, the other intermodulation products superceced the fifth order products. Gain and input power response, gain and input frequency response were measured with a vector network analyzer (VNA). Input and output impedances were also determined with a VNA. Additionally, the stability of the devices was determined based on the VNA measurement data. Simulations were also conducted for validation and comparison.

4.3.1 Intermodulation measurements

Six different intermodulation measurements were conducted. Two for the linearized amplifier and four for the reference amplifier. For each measurement the input power ranged from -50 dBm to 14.5 dBm. Note, the actual power delivered to the DUT ranges from -73 dBm to -8.5 dBm due to the attenuators and the power divider. The quantities we are measuring are third order intermodulation output intercept point (OIP_3), third order input intercept point (IIP_3) and 1-dB compression point. The measurement results for the reference amplifier when the collector current is 5mA are shown in Figure 38.

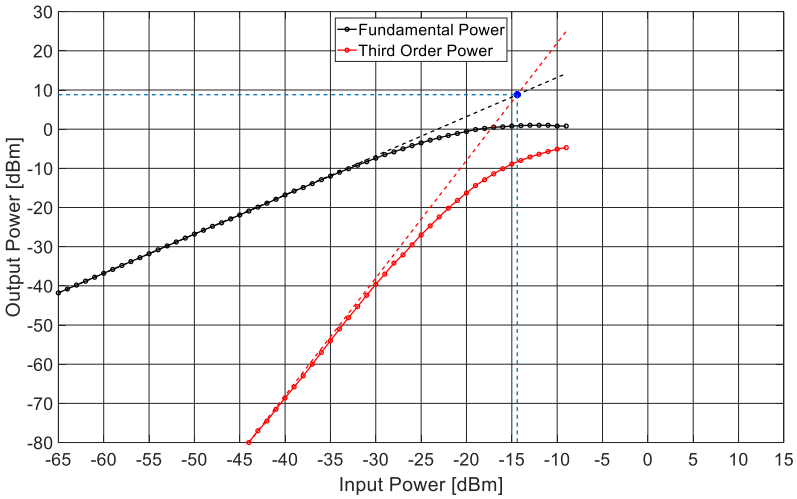

Figure 38. Reference amplifier measurement results with $I_C = 5$ mA. Each dot in the graph represents a single measurement point. The black dots are for the fundamental power and the red dots are for the third order intermodulation products. The frequencies for the third order power were measured to be 3.2 MHz and 3.5 MHz. The noise floor was at -80 dBm. OIP3and IIP_3 are shown by the blue dot and the blue dashed lines.

The fundamental power has a slope of 1 and slope for the third order power is 3, until the amplifier enters compression. Linear extrapolation is utilized to extend the linear part of graphs. Dashed lines mark the extrapolated lines. From the graph, we find that OIP_3 is 8.8 dBm and IIP_3 is -14.4 dBm. The P_{1dB} is at -4.8 dBm. During the measurements, it was also found that other products manifest themselves when -33 dBm of power is delivered to the reference amplifier. Past -26 dBm, significant intermodulation is experienced across the spectrum, even over taking IM5. The same measurements were done with the linearized amplifier, the results are shown in Figure 39.

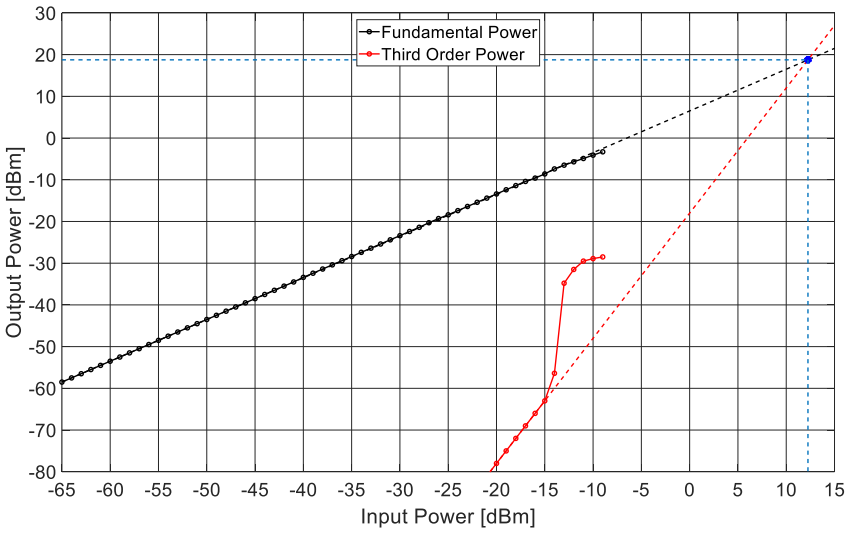

Figure 39. Intermodulation measurement results for the linearized amplifier with collector currents being 5mA.

The third order power is only visible at higher input powers, proving the linearization works. However, when the power delivered to the DUT exceeds -15 dBm, the intermodulation products increase rapidly. The linearization fails with high input power because the logarithmic amplifier saturates to the supply voltage when the logarithm becomes negative. Nonetheless, the linearity of the amplifier is still markedly improved when the predistortion scheme is utilized. OIP_3 is now 18.75 dBm and IIP_3 is 12.25 dBm. P_{1dB} cannot be determined from the Figure, as the device is not compressed enough. The predistortion scheme still has its own issues. The current consumption is effectively at least doubled due to the second transistor and the gain is significantly smaller. The reference amplifier has approximately a gain of 23 dB, while the linearized amplifier has a gain of 6 dB. This raises a question: could we not achieve the same results just by doubling the reference amplifier collector. To test this, the reference amplifier collector current was doubled from 5mA to 10mA. The results for this scenario are shown in Figure 40.

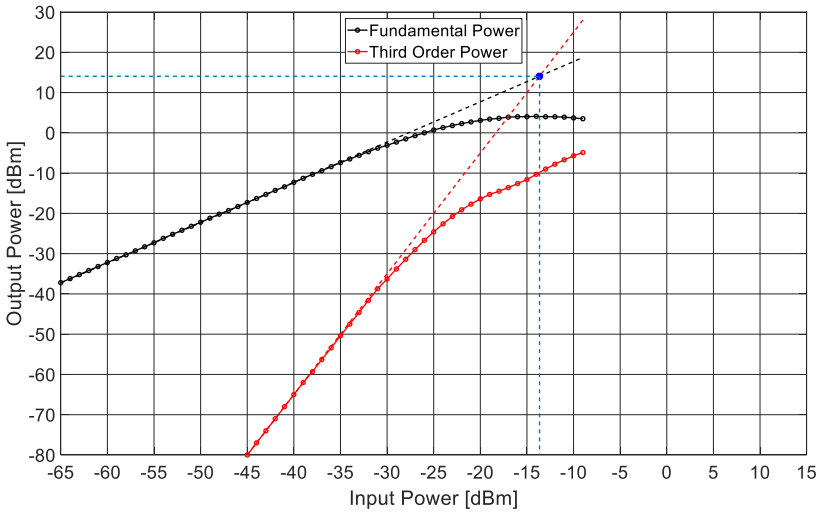

Figure 40. Intermodulation measurement results for the reference amplifier with collector current of 10mA.

The plot is quite similar to the one in Figure 38, however the linearity has slightly improved. The gain has increased to 28 dB. OIP_3 is 14.05 dBm and IIP_3 is -13.65 dBm. the 1-dB compression point is achieved at -1.3 dBm. Nonetheless, in the reference amplifier is still less linear than the linearized amplifier. As earlier, the other intermodulation products become prevalent when more than -26 dBm of power is delivered to the device. One might then ask: how does the reference amplifier perform when a 20-dB attenuator is introduced at the amplifier's input since the logarithmic amplifier clearly attenuates the signal? Figure 41 provides an answer to this question.

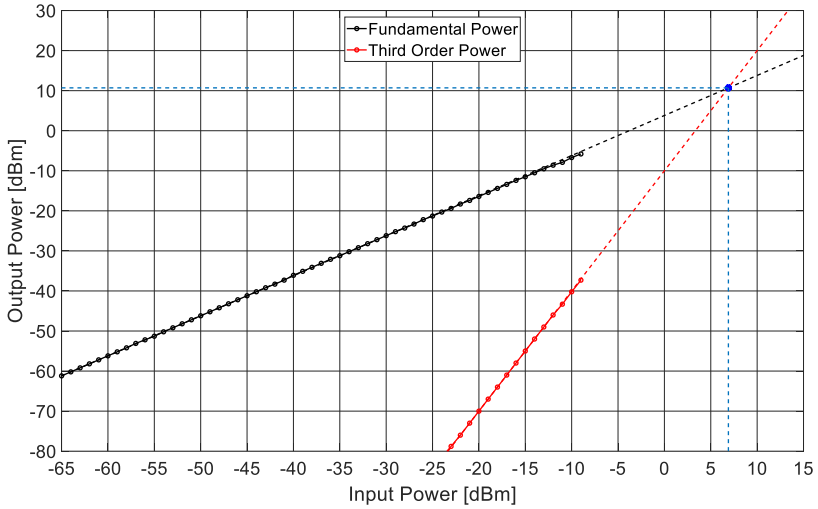

Figure 41. Results for the reference amplifier with 20 dB attenuator at the input.

A quick glance at Figure 41 may give the impression that the linearity seems to be greatly improved since the amplifier does not seem to enter compression. However, if you take a closer look at the Figure, the improvement is not remarkable. The gain is now only 3 dB, while OIP_3 is 10.7 dBm and IIP_3 is 6.9 dBm. The device behaves more nonlinearly than with the increased current consumption.

Lastly, both the reference amplifier and the linearized amplifier were measured with the impedance transformer board. The matching circuit was connected to the spectrum analyzer input. One particularly interesting effect of the transformer was the raised noise floor, it increased from -80 dBm to -70 dBm, rendering the intermodulation measurements more difficult. The results for the reference amplifier with the impedance transformer are shown in Figure 42.

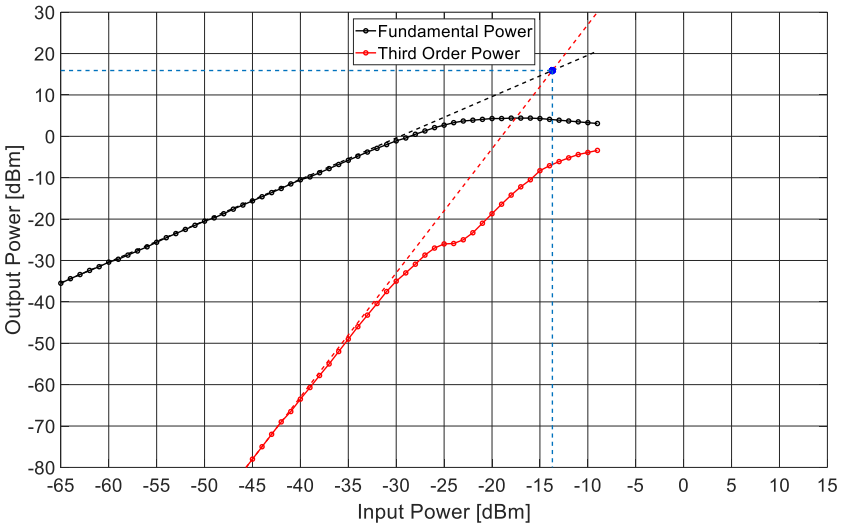

Figure 42. Intermodulation measurement results for the reference amplifier with the impedance transformer connected. Note, the collector current is 5 mA.

With the transformer board connected, the gain is now approximately 30 dB. However, OIP_3 and IIP_3 are largely unchanged, the former being -15.9 dBm and the latter -13.7 dBm. P_{1dB} has moved to 0.5 dBm. The same observations regarding the intermodulation products mostly hold as earlier with just the reference amplifier alone. There is one exception, IM3 doesn't increase for a while at -26 dBm -24 dBm. Instead it was observed that the other products rapidly increased in power at this range. Figure 43 presents the results for the same measurements with the linearized amplifier.

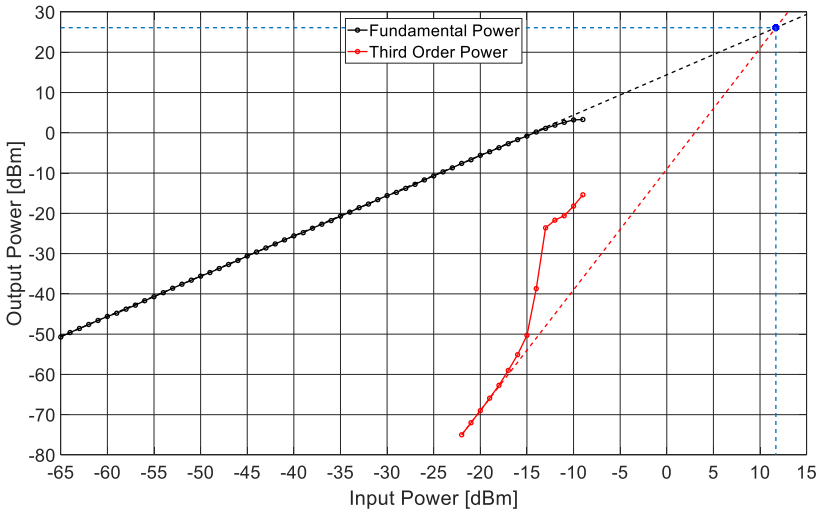

Figure 43. Linearized amplifier with the impedance transformer.

With this configuration, the gain is around 13 dB, OIP_3 is 26.1 dBm and IIP_3 is 11.7 dBm. While, the IIP_3 is almost identical to the value obtained just with the linearized amplifier, gain and OIP_3 are noticeably improved with a higher load impedance. Due to the increased gain, the linearized amplifier now experiences compression, P_{1dB} being approximately 4.2 dBm. However, the gain does not match the calculated gain, but we will later examine why this occurs. Otherwise, the behavior of the intermodulation products is similar to the behavior in the earlier measurement without the impedance matching network.

4.3.2 Gain measurements

VNA was used for gain measurements, since a spectrum analyzer is not a reliable power meter [32]. First, input power sweep was conducted with both devices, with and without the impedance transformer. Gain is plotted as function of the input power without the matching circuit in Figure 44.

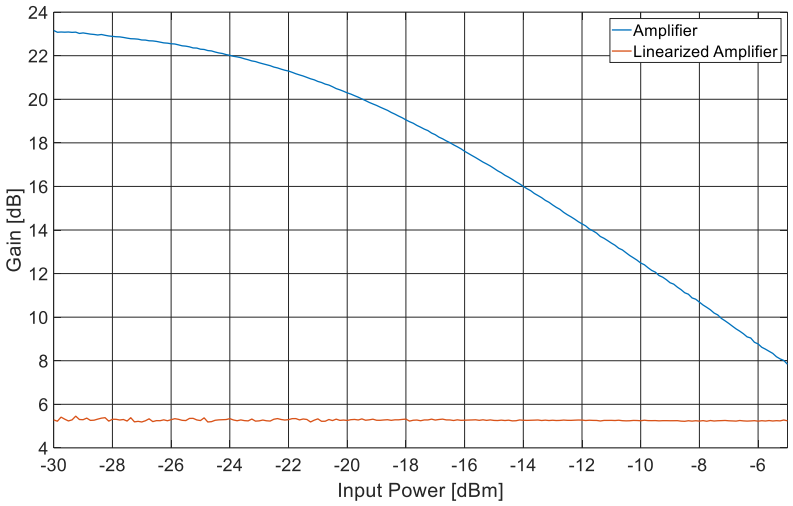

Figure 44. VNA input power sweep for the reference amplifier and the linearized amplifier.

According to the data, the linearized amplifier has a gain of 5.3 dB when the load impedance is 50 Ω. The gain remains constant regardless of the input power. The reference amplifier has a maximum gain of 23 dB that decreases as the input power increases. Unfortunately, the VNA used in the measurements had a limited output power range, capping at -5 dBm. It would have been interesting to see if the reference amplifier's gain would have been eventually less than that of the linearized amplifier's. Results for the same measurement with the impedance transformer in place are shown in Figure 45.

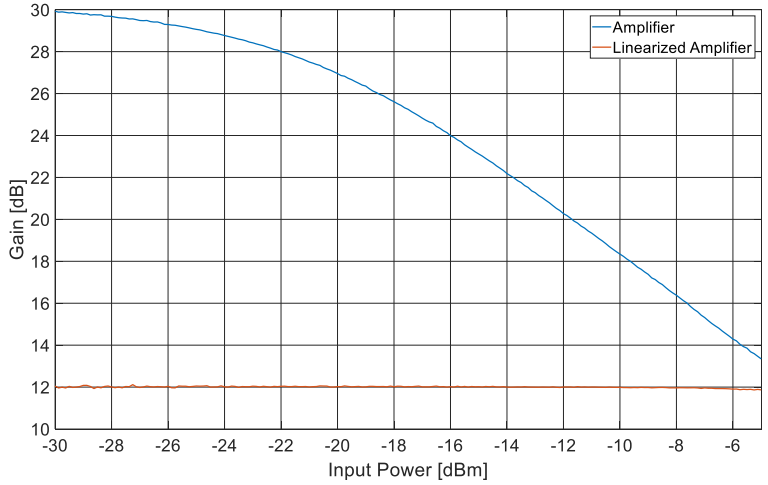

Figure 45. Gain versus input power plot for the reference amplifier and the linearized amplifier with the impedance converter connected.

The gain has similar relation to input power with the both devices as before. The only difference being increased gain due to increased load impedance. Maximum gain for the

reference amplifier is 30 dB and 12 dB for the linearized amplifier; 12 dB being substantially below the calculated gain of 16 dB. Frequency sweep results with 50 Ω load impedance are shown in Figure 46.

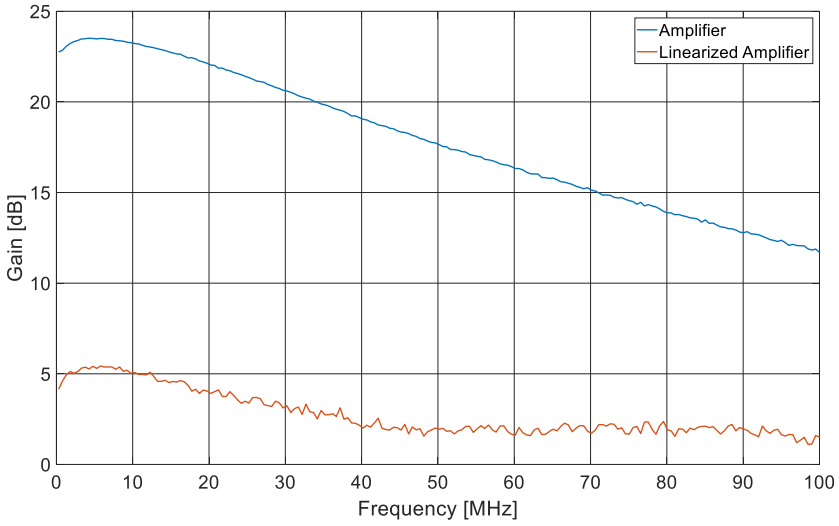

Figure 46. Frequency sweep gain measurement results with standard 50 Ω load impedance.

Both devices suffer from degrading performance as the frequency increases, there is a 10 MHz wide band, where the gain remains relatively constant. After 10 MHz input signal frequency is exceeded, the gain starts to decrease. The degradation is partly caused by the stabilization circuitry, as the 100 pF capacitors have low impedance at higher frequencies. Another major factor is the AD8055 operational amplifier, its -3 dB bandwidth is only 300 MHz [26]. The same measurement results with the matching circuit in place are shown in Figure 47.

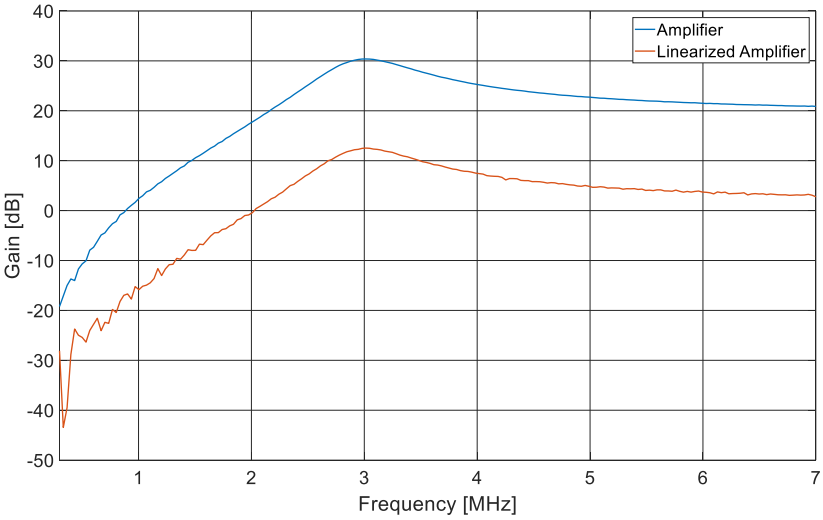

Figure 47. Frequency sweep with impedance transforming. Note, the frequency sweep was only conducted up to 7 MHz.

Due to the frequency dependence of the high pass LC impedance converter, the response is different than earlier. Hence, the frequency sweep was limited to a lower frequency range. Maximum gain is obtained when the frequency is 3.15 MHz.

4.3.3 Stability

The stability of the linearized amplifier was examined by importing VNA measurement data to ADS and using a built-in tool to calculate the stability factor μ. The stability factor is plotted as function of frequency in Figure 48. The plot is limited to 10 GHz because the transistor BFM520 has a bandwidth of 9 GHz [25]. Exceeding the cut-off frequency decreases the gain, at some point the device will even start to attenuate. Therefore, analysis for higher frequencies is not necessary. Additionally, the most problematic frequencies during the thesis work were around 3 GHz and 7 GHz, but this will be discussed later in Chapter 5.

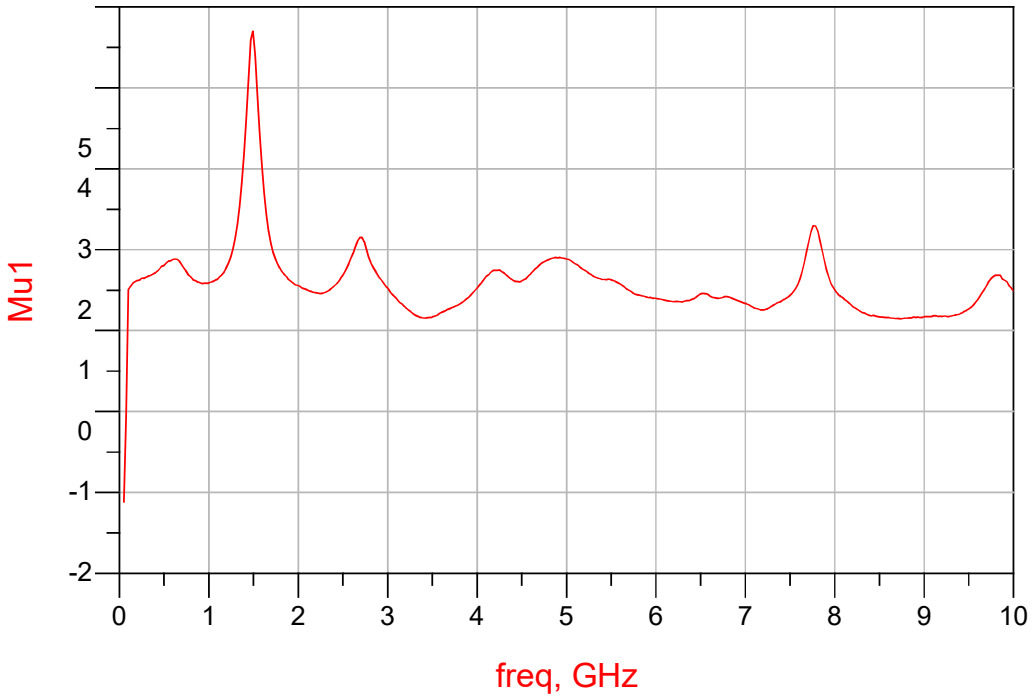

Figure 48. Stability factor Mu for the linearized amplifier.

For the most part, the device is stable. The only exceptions being the frequencies below 100 MHz. During the measurements, small scale oscillation with power of -73 dBm was present at 46 MHz. The oscillation was traced back to the operational amplifier by monitoring if the oscillation frequency changes if the supply voltage is gradually increased or decreased. It was found that tuning VEE had a noticeable effect on the oscillation frequency. The operational amplifier being the only active component on board to draw power from VEE was a likely culprit. Even though unconditional stability was one of the

target specifications, it was decided to proceed with the measurements despite the oscillation. An assumption was made that the oscillation present in the circuit only has a minimal effect on the device operation. The oscillation was low power (around 50 pW), despite the oscillation frequency was sufficiently low to pass through the circuit to the to the spectrum analyzer unimpeded.

4.3.4 Impedance measurements

Lastly, the input and output impedances were measured from 300 kHz to 7 MHz with a VNA. The impedance measurements were used to gauge the impedance matching of the device. Both, the input and output impedances are plotted in a Smith's Chart in Figure 49.

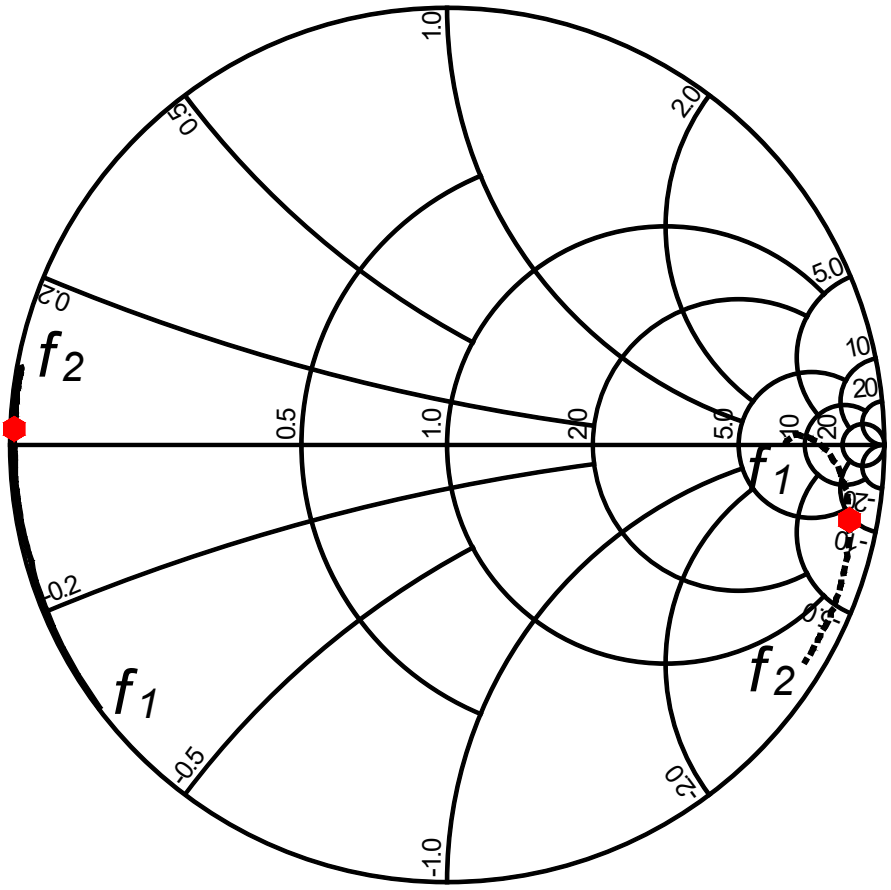

Figure 49. Impedance measurement results from $f_1 = 300$ kHz to $f_2 = 7$ MHz for the linearized amplifier. The input impedance is marked a solid line and the output impedance with a dashed line. The impedance values at 3.3 MHz are marked with red dots. At 3.3 MHz the input impedance is $Z_{IN} = Z_0(0.005 + j0.019)$ and the output impedance $Z_{OUT} = Z_0(3.438 - j9.573)$.

As shown in the Figure, the impedance matching in the constructed device is nonexistent. The input impedance is close to zero when the device is active due to the virtual ground, providing a low impedance path for current flow. The opposite applies for the output; the

RF choke provides considerable high impedance with the measured frequencies, leaving the BJT PN-junctions as only viable paths for the current. Nonetheless, these results were to be expected since the device does not include any impedance matching circuitry.

4.3.5 Simulation results

Simulations were conducted to study and find the culprit behind the discrepancies between the calculated gain and the measured gain for the linearized amplifier. Additionally, intermodulation was examined through simulations to further validate the measurement results. SPICE (simulation program with IC emphasis) models provided by the manufacturer were used for the active components. Additionally, inductor nonidealities were considered. The simulation circuits themselves are found in APPENDIX 5. The gain simulation results for the linearized amplifier with standard 50 Ω load is shown in Figure 50.

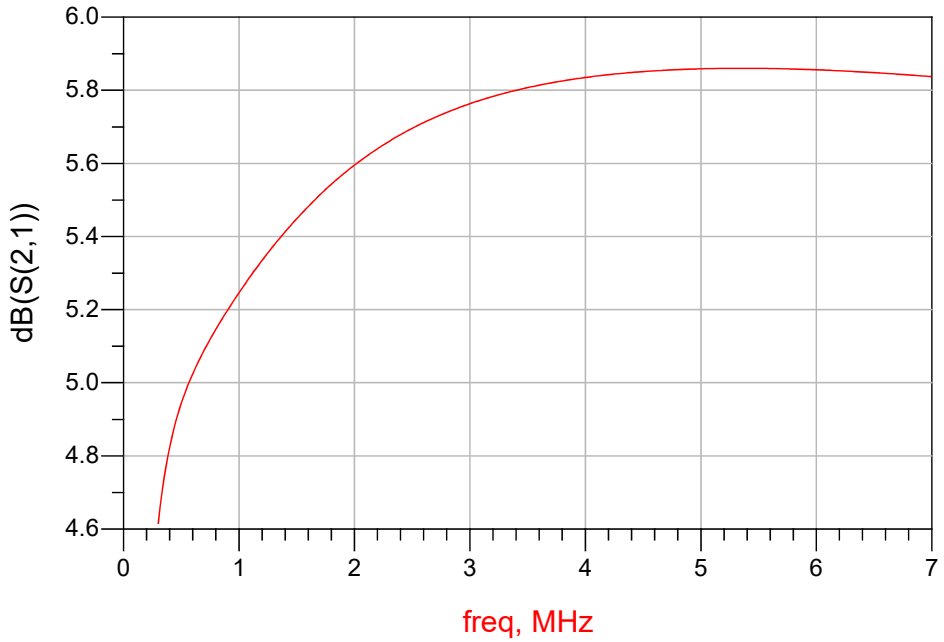

Figure 50. S21 simulation for the linearized amplifier with 50 Ω load.

At 3.3 MHz the simulated gain is approximately 5.8 dB, being quite close to the actual measured gain that was 5.3 dB. However, the simulated gain does not achieve the calculated gain of 6 dB. The simulations indicate gain is lost due to the RF power dissipated in the collector resistor because the RF choke is not ideal. The Q factor for the RF choke was 34 [33]. The gain is closer to 6 dB, when the components in the simulations are replaced with ideal components. In addition, the stabilization circuit slightly decreases the gain as part of the RF power at the operation frequency leak through the circuitry to RF ground. The simulation result with the impedance transformer in place is shown in Figure 51.

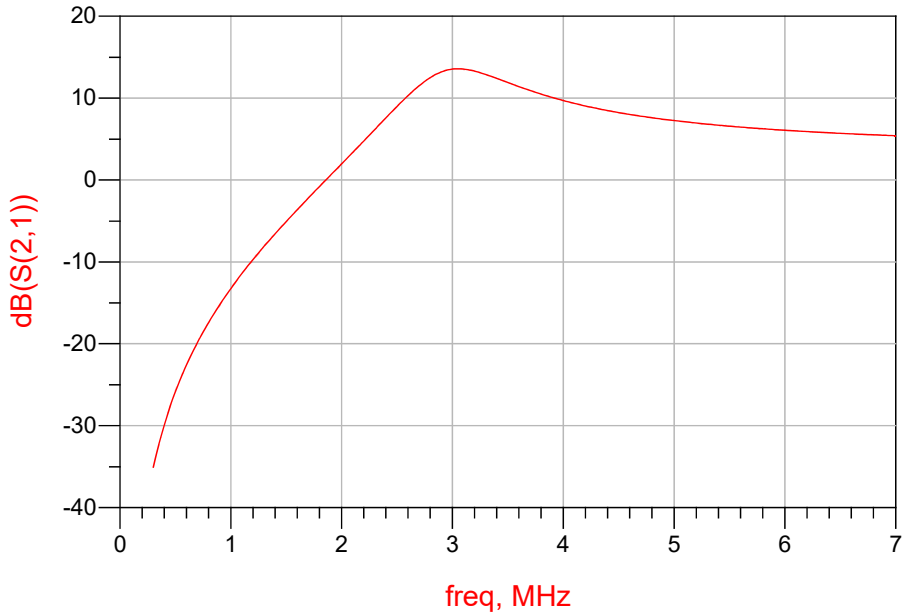

Figure 51. S21 simulation with 500 Ω load.

The simulated gain plot is almost identical to the measured gain when the component nonidealities are considered. The only major difference is that the simulated gain at 3.15 MHz is around 13 dB while the measured again is approximately 12 dB. According to the simulations most of the lost gain is due to the low Q factor of the inductor in the impedance transformer. Experimental measurements indicated the Q factor was only 24. This alone accounted to 2 dB of lost gain in the simulations. The RF choke and the stabilization circuitry account for the rest of the lost gain. 16 dB gain is only achieved in the simulations when all the components are replaced with ideal components. The intermodulation simulation results are shown in Figure 52 and in Figure 53 alongside the measurement results for ease of comparison.

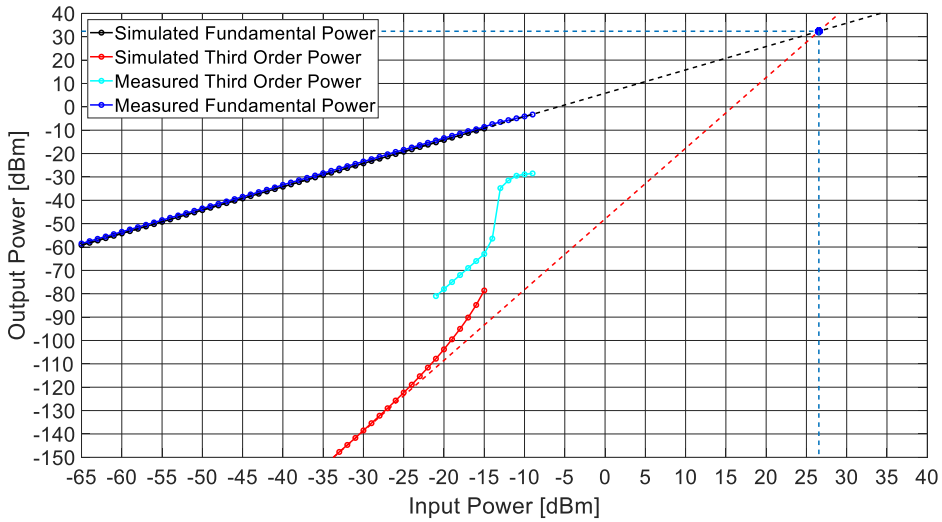

Figure 52. Intermodulation simulation and measurement results with 50 Ω load. Note, linear extrapolation has not been included for the measurement results.

The fundamental powers are almost identical; the measured power is slightly greater. However, the power was measured with a spectrum analyzer, hence the measured power is not wholly accurate [32]. The slope of the third order power experiences similar abnormalities in simulations when compared to the measurement results. The major difference being that the slope does not increase as fast as in the measurements and the increase in slope occurs earlier. However, the simulations were only conducted up to -15 dBm input power due to convergence failure after the logarithmic amplifier saturates. Consequently, it is impossible to determine the 1-dB compression point from the simulation data. Additionally, third order power is always visible in the simulations due to the absence of the noise floor. With the 50 Ω load IIP_3 was 26.5 dBm and the OIP_3 was 32.3 dBm. These values are substantially better than the intercept points determined from the measurement results. Primary explanation for this might be the active component SPICE models, especially BFM520 model. Despite being a matched pair transistor, the actual transistors inside the component case can have noticeable differences [25].

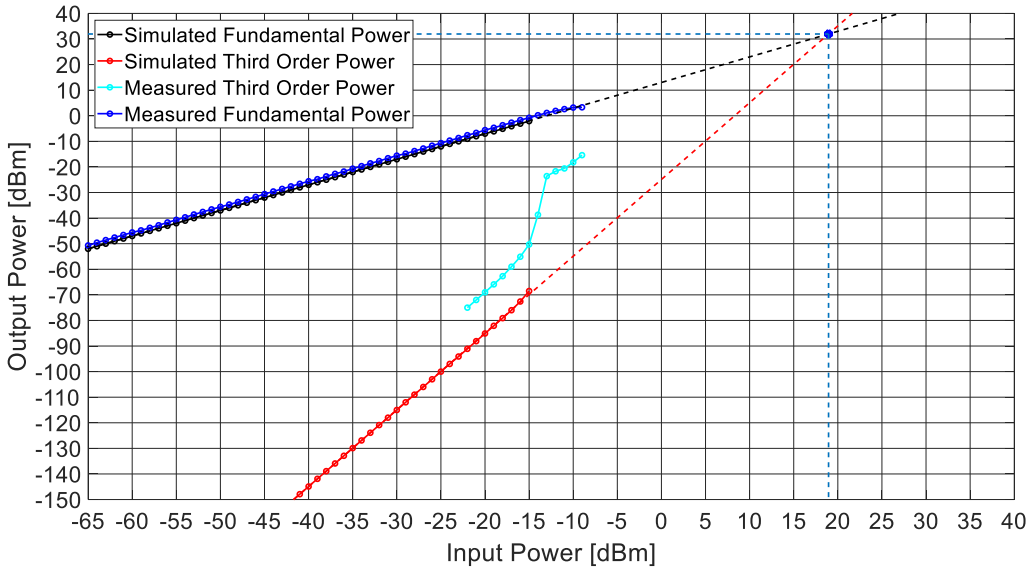

Figure 53. Intermodulation simulation and measurement results with 500 Ω load.

With the 500 Ω load the simulated third order power behaves more similarly to the measured power. Otherwise, the prior observations regarding the plots also apply here. The IIP_3 is now 19 dBm and OIP_3 is 32 dBm. One major additional difference between the simulations and the measurements becomes apparent when examining the intercept points. While in the measurements the impedance transformer had a minimal effect on the IIP_3 and OIP_3 values, in simulations the transformer severely degrades the IIP_3 value. Despite differences, the simulations largely verify the validity of the measurement results. The overall behavior of the constructed device is similar in the measurements and simulations.

5. DISCUSSION

Before concluding the thesis, a few more items are discussed in addition to the measurement results. First, the practical work done during the thesis and how it was conducted is discussed. Secondly, we will discuss the success in meeting the thesis goals. As a final item, propositions for possible future work based on the thesis are presented.

5.1 Practical work

Since the thesis was a continuation for research conducted by other researchers [5, 6], the first logical step was to carefully study prior research material. After studying the material, a logarithmic amplifier was constructed on a breadboard and tested. The logarithmic amplifier design was largely based on a design presented in the bachelor's thesis [6]. A diode was utilized as the nonlinear element in the bachelor's thesis, while a transistor was used in the test design. The initial tests were limited as they were only conducted in time-domain. In hindsight the initial tests provided a clear warning of the things to come. The tests indicated that the circuit did not behave as expected when the diode was replaced with a diode-connected RF transistor. The performance of the circuit was inconsistent and unpredictable. However, since the initial tests were limited to time domain, it proved difficult to discern the root cause of the issues. Consequently, these issues were falsely attributed to outside interference and the breadboard itself. Target goals and specifications were agreed upon after the initial tests and the design process was started. What followed was a vicious cycle that would remain unbroken for months.

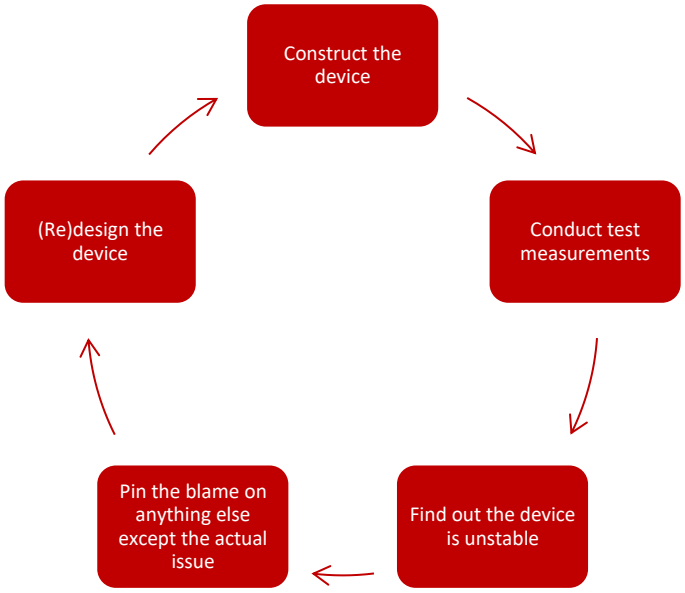

Figure 54. The vicious cycle.

The cycle proceeded as follows, first a device was designed and assembled. Test measurements were conducted, the usual observation being that the linearization scheme works but the device was unstable. At worst, oscillation at 3 GHz frequency with power of -10 dBm was observed at the output while the fundamental outpower was only in range of -20 dBm. Despite the linearization scheme working at the fundamental frequency, the results were deemed invalid as the device additional nonlinear behavior in form of oscillation. Quick fixes were attempted by changing component values or soldering on additional components on board. However, none of the fixes managed to completely remove the oscillation, at best the oscillation was slightly attenuated. The root cause of the stability issue remained unfixed. The blame with the stability issues was pinned on anything else except the actual cause behind the oscillation.

First, we suspected that the layout was inadequate for a RF device, prime suspect being the additional inductance caused by long traces and grounding paths. Consequently, the layout for the device was redesigned numerous times. Nonetheless, redesigning the layout to be more compact did not have a major effect on the results. When the layout was not considered as the culprit, the issue was deemed to be the lack of stabilization circuitry. This led to partial redesign of the device itself. Yet the stability issues persisted. As a bid to find the root cause of the oscillation, a board containing just the logarithmic amplifier was constructed.

The logarithmic amplifier was found to be the source of the oscillation. The board only had two potential components that could oscillate, the operational amplifier and the diode-connected transistor. Initially, the operational amplifier was considered as the source of the oscillation and the diode-connected transistor was ignored. A new design with additional stabilization circuitry for the operational amplifier was implemented and tested. Despite the efforts to stabilize the operational amplifier, the design still proved to be unstable. Finally, the diode-connected transistor was given more thought. Initially the idea of the diode-connected transistor being the source of oscillation was outright dismissed even though the initial tests conducted on the breadboard hinted at this. A diode-connected transistor was simulated, and we found that at higher frequencies it could amplify signals and be unstable. This finding was contrary to what earlier literature regarding diode-connected transistors claimed [24]. However, very little diode-connected transistor related literature exists, and they are quite limited in scope. For instance, circuits that use RF connected transistors or operate at higher frequencies were not considered in the literature.

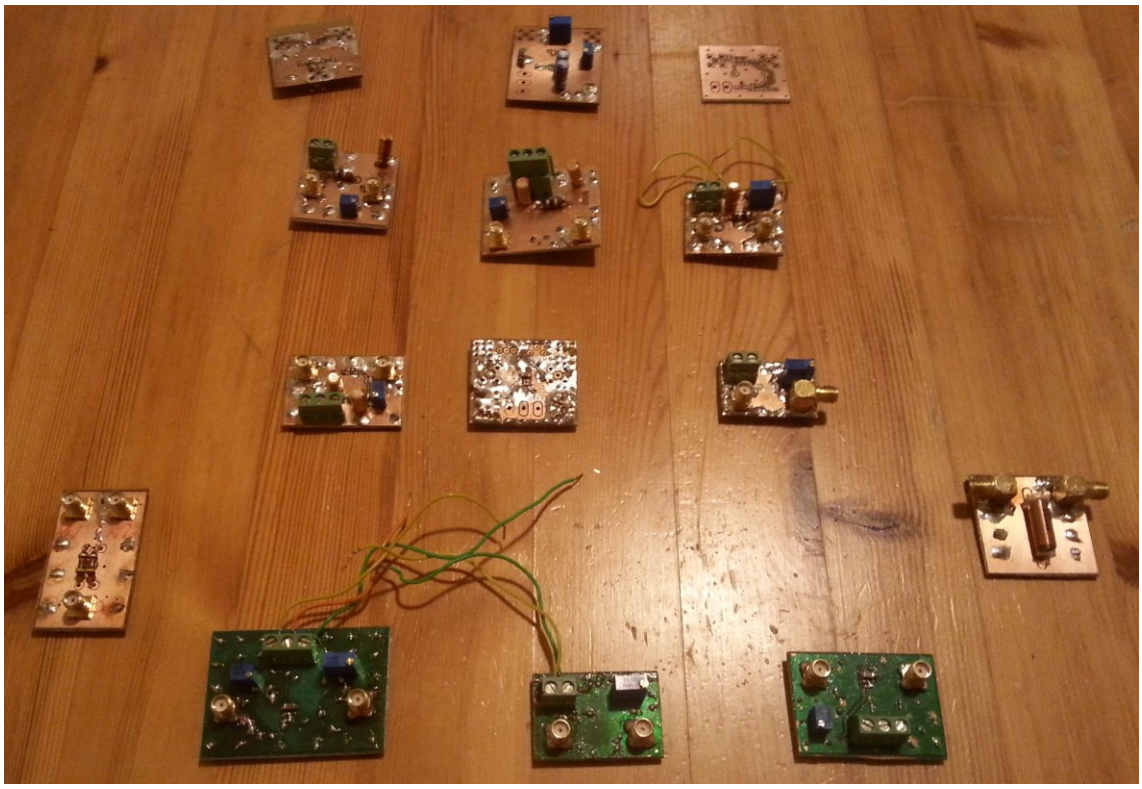

Figure 55. Boards made during the thesis work. Note, some of the boards have been salvaged for components.

After the root cause of the stability issues was identified, a final design was made, implemented, measured and verified. The vicious cycle was finally broken. A multitude of boards were made during the practical thesis work; most of the boards including the side projects made during the thesis are shown in Figure 55. With the measurements done all that remained was to process the measurement data into a presentable form and verifying the measurement data through simulations.

5.2 Assessment

The objective of the thesis was to conduct a proof of concept study regarding a simple analogue predistortion linearization scheme, where a RF BJT amplifier is linearized with a logarithmic amplifier. The aim was to prove the viability of the scheme by constructing an amplifier that is linearized with the scheme. All the relevant figures of merit from the measurements are compiled in Table 2 to help gauging the efficacy of the scheme.

Table 2. Measurement and simulation results. Ref stands for the reference amplifier, Lin. for the linearized amplifier and Imp. for the impedance transformer. Load impedance is 50 Ω and the current is 5 mA unless otherwise stated. Note, IM3 to Carrier at 50 Ω is measured when the fundamental output power is -10 dBm and with 500 Ω load when the power is -5 dBm.

Test Device	Ref.	Lin.	Ref. 10 mA	Ref. -20dB	Ref. 500Ω	Lin. 500Ω
Gain	23 dB	5.3 dB	28 dB	3 dB	30 dB	12 dB
OIP_3	8.8 dBm	18.8 dBm	14.1 dBm	10.7 dBm	16 dBm	26 dBm
IIP_3	-14.4 dBm	12.3 dBm	-13.7 dBm	6.9 dBm	-13.7 dBm	11.6 dBm
P_{1dB}	-4.8 dBm	N/A	-1.3 dBm	N/A	0.5 dBm	4.2 dBm
IM3 to Carrier	-38 dBc	-58 dBc	-39 dBc	-42 dBc	-41 dBc	-61 dBc

The results shown in the table clearly establish the efficacy of the linearization scheme. OIP_3 is improved by 10 dB when the reference amplifier operates at normal condition regardless of the load. Similar improvements are observed with IIP_3. The compression point occurs at far higher powers with the linearization in effect, with 50 Ω load P_{1dB} was not measurable with the available equipment. When the gain is increased with the higher load impedance, the compression point becomes measurable. Still, a marked improvement is observed, the compression point has been increased by 3.7 dB. Third order intermodulation products are 20 dB more below the carrier when compared to the reference amplifier. The linearized amplifier enjoys superior linearity, even when the current drawn by the reference amplifier is doubled to match current drawn by the linearized amplifier. However, considerable amount of gain is lost due to the logarithmic amplifier. Nonetheless, even if a 20-dB attenuator is introduced in front of the reference amplifier, the linearity is still superior. Additionally, the scheme is inexpensive to implement. The cost breakdown of the linearized amplifier is found in Table 3.

Table 3. Cost breakdown of the linearized amplifier. [34]

Component	Amount	Unit
SMA Connector	2	1.37 €
AD8055	1	1.89 €
BFM520	1	0.35 €
FR4 Board	22 cm^2	0.37 €
500 Ω Potentiometer	1	0.26 €
100 kΩ Potentiometer	1	2.79 €
39µH Inductor	1	0.36 €
Rest of the Passive Components	18	1.00 €
Screw Terminal	1	0.88€
Total cost		10.64€
Cost without SMA connectors		7.90€

Note, the unit cost for the rest of the passive components is an estimated sum for the total cost of the passive components, excluding the 39µH inductor. Unit cost for a single 0603 surface mount device (SMD) is low, usually in range of one cent as the SMD devices were bought in reels. Consequently, the total cost of the passive components is an over-estimation. FR4 board unit cost is an estimation based on what is the cost of a 22 cm^2 area when it is cut from a 600 cm^2 board.

The total cost of the linearized amplifier is low, being only 10.64 €. If the amplifier is assumed to be a larger system, then the cost decreases to 7.90 € as separate SMA connectors are not required. The scheme itself is simple and straightforward. It will not provide the same degree of linearity as feedforward linearization, but the scheme presented in the thesis is considerably simpler to implement [3]. The design inherently also supports a broadband implementation, but in the thesis the bandwidth is limited by the operational amplifier and the stabilization circuitry. However, the scheme is not without its own challenges, the greatest issue being the transistors. The less identical they are, the less (44) holds true, thus theoretically, the linearity of the device should deteriorate. Hence, matched pair transistors are recommended, greatly limiting the choice of available transistors. Nonetheless, the scheme is very much viable.

5.3 Future work

The two biggest issues with the current design are the impedance matching and the minor oscillation at 46 MHz. Improving the stability would most likely involve implementing stabilization circuitry for the operational amplifier. Also, the current stabilization circuitry should be replaced with a broadband alternative if the device is to operate with wide bands. Similarly, the implementation of broadband impedance matching would also improve the performance considerably, as less power is lost due to the reflections. Additionally, the linearity improves when less power is reflected. Separate impedance matching amplifiers could be employed for a broadband implementation. The operational amplifier would also have to be replaced if a wide operating bandwidth is desired.

If the gain is to be improved, a dual operational amplifier can be utilized, the first operational amplifier amplifies the input signal before it is fed to the logarithmic amplifier. Alternatively, one could try to implement the logarithmic amplifier without an operational amplifier, removing the bandwidth limit imposed by the gain-bandwidth product of the operational amplifier. With the proposed fixes implemented, further testing should be conducted. Particularly testing the device operation with wide bandwidths. Additionally, the device could be biased for higher input powers and tested with high input powers to study if the linearization still holds.

6. CONCLUSION

This thesis is part of a proof of concept study where a new analogue predistortion scheme was developed for linearizing RF BJT amplifiers. In the scheme, a logarithmic amplifier is cascaded with a RF BJT amplifier, effectively eliminating the exponential dependence experienced by the RF BJT amplifier. By design, the scheme is low cost, simple and inherently broadbanded. The linearization method was verified by implementing the scheme on a printed circuit board and measuring it. The effectiveness and the viability of the scheme was judged based on several factors. These factors ranged from the suppression of the third order intermodulation products caused by the exponential nonlinearity to the cost and simplicity of the implementation. Based on these criteria, the scheme was found to be viable and moderately effective. Additionally, one interesting finding was made during the thesis work: a diode-connected transistor may have negative resistance when the transsusceptance is high. Consequently, the transistor can amplify high frequency signaling, causing oscillation. To best of our knowledge, this finding is not supported by contemporary literature [24].

Before the linearization scheme was presented in the thesis, linearity, nonlinearity and other contemporary linearization methods were studied. Linearity is most often a desirable trait unless the device is to be nonlinear by design, for instance a logarithmic amplifier. The desirability of linearity stems from the fact that linear systems are predictable and free from nonlinear distortion. However, in reality all systems exhibit nonlinear behavior to some degree. Nonetheless, linear approximations can be applied, for example resistors can be assumed to follow Ohm's law. Active components such as transistors are different, these devices usually exhibit noticeable nonlinear dependence, especially when the input power is high. Decreasing the input power may help with the linearity but as consequence the efficiency decreases. With wireless devices this would be a major issue as most of the time battery life is critical for wireless applications. Ignoring nonlinear behavior is not an option either, in wireless communications intermodulation is prime example of this. Intermodulation occurs due to frequency mixing caused by the nonlinear dependency of the device. There are different orders of intermodulation products but usually the third order products are the most detrimental as they are high power and close to the fundamental frequency. Third order power increases three times more than the fundamental output power when the input power is increased, theoretically eventually superceding the fundamental power. Consequently, modulation is ruined, and adjacent channels are blocked due interference caused by intermodulation products. A multitude of linearization techniques have been developed to combat nonlinear behavior. Feedforward linearization being the most effective and yet the most difficult linearization scheme to implement [3]. [14]

The exponential dependence of BJT transistors can be modelled with Ebers-Moll model [23]. The model uses two current-controlled sources and two diodes to describe a BJT. The sources are used to model base current in forward and reverse bias. The diodes represent the two PN-junctions inside a BJT. Due to the PN-junctions, collector and emitter currents have an exponential dependence as shown by (21). However, the exponential dependence could be suppressed by cascading a logarithmic amplifier with the BJT. The output voltage is now linearly depending on the input voltage provided by the generator and the generator and output impedances as seen in (43). Consequently, the gain is completely determined by the source and load impedances as determined in (48). With 50 Ω load the gain is 6 dB and 500 Ω load 16 dB according to (48) when the source impedance is assumed to be the standard 50 Ω. The logarithmic amplifier itself consist of an operational amplifier and a diode-connected BJT connected as negative feedback element. The amplifier operating point is biased by tuning the voltage divider located in the positive input of the operational amplifier. To maximize the effectiveness of the linearization, the currents flowing through both transistors are to be the same. For the thesis, the current was chosen to be 5 mA and the operation frequency 3 MHz.

Intermodulation measurements were conducted with a spectrum analyzer and accurate gain measurements with a VNA. Consequently, due to the lack of suitable measurement accessories for low frequency measurements, side projects were undertaken. A Wilkinson Power Divider and a high pass LC impedance transformer were constructed for measuring at 3 MHz. Additionally, a reference amplifier was constructed as a benchmark for comparison. With all the necessary measurement equipment ready, the measurements were conducted, and the measurement data was processed. Moderate improvement was observed on the suppression of IM3, with both the 50 Ω and the 500 Ω load OIP3 was improved by 10 dB. Similarly, IM3 products were suppressed by 20 dB when compared to the reference amplifier. However, the bandwidth of the implementation was limited due to the operational amplifier gain bandwidth product and the stabilization circuitry. Nonetheless, the measurement results verify the feasibility of the linearization scheme presented in this thesis. Recommended work for future includes a broadband implementation of stabilization and impedance matching circuitry. The operational amplifier should also be replaced with a high frequency and wide bandwidth operational amplifier. With these recommended changes, the design would take better advantage of the inherent broadband capabilities of the linearization scheme.

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APPENDIX 1: DIODE-CONNECTED TRANSISTOR SIMULATIONS

Simulation circuits for the diode-connected transistors are included in this appendix. Figure 56 is for the unstable diode-connected transistor and Figure 57 for the stabilized. All the relevant simulation blocks and settings are shown in the figures. Note, a similar transistor BFG520 is used in the simulations. BFM520 is essentially a matched pair BFG520, although BFG520 is slightly more capable transistor, enjoying slightly higher performance than BFM520 gain wise [25, 35] . Nonetheless, the biasing conditions are similar to that of the actual implemented circuit.

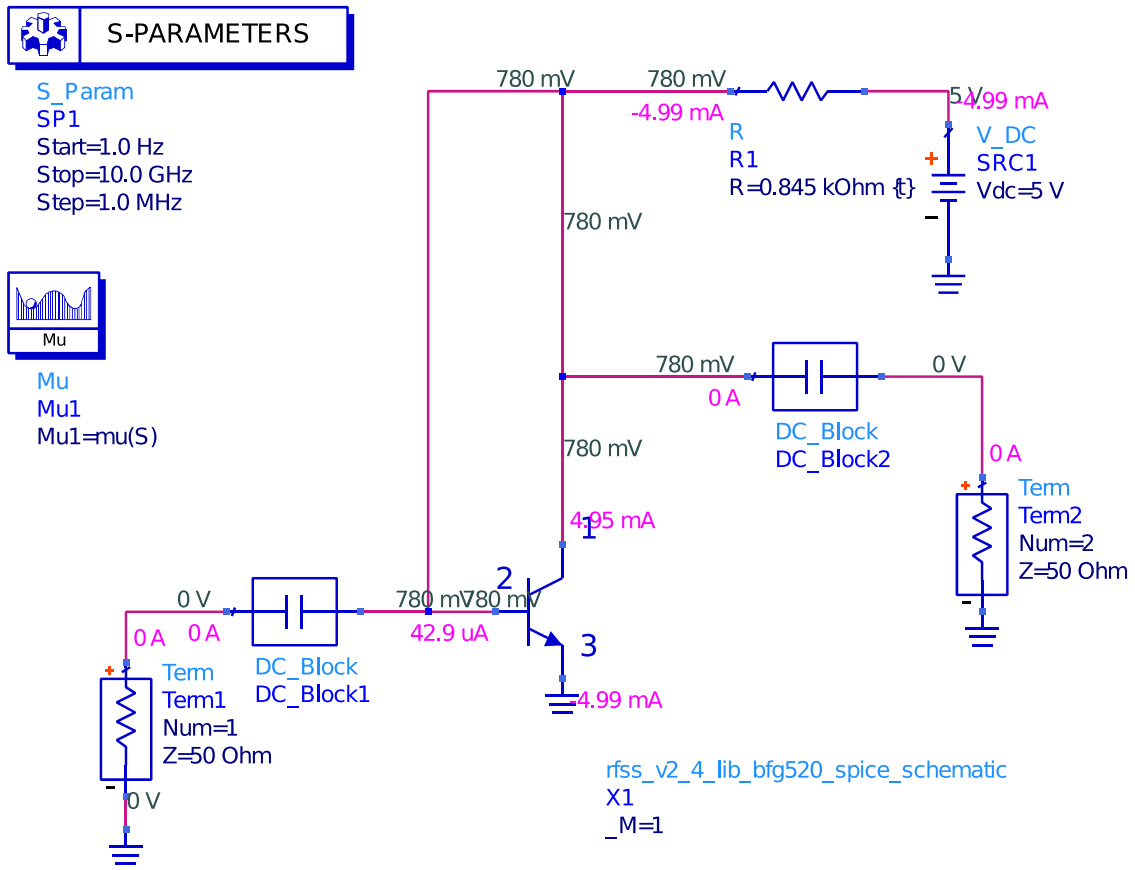

Figure 56. Unstable diode-connected transistor simulation schematic.

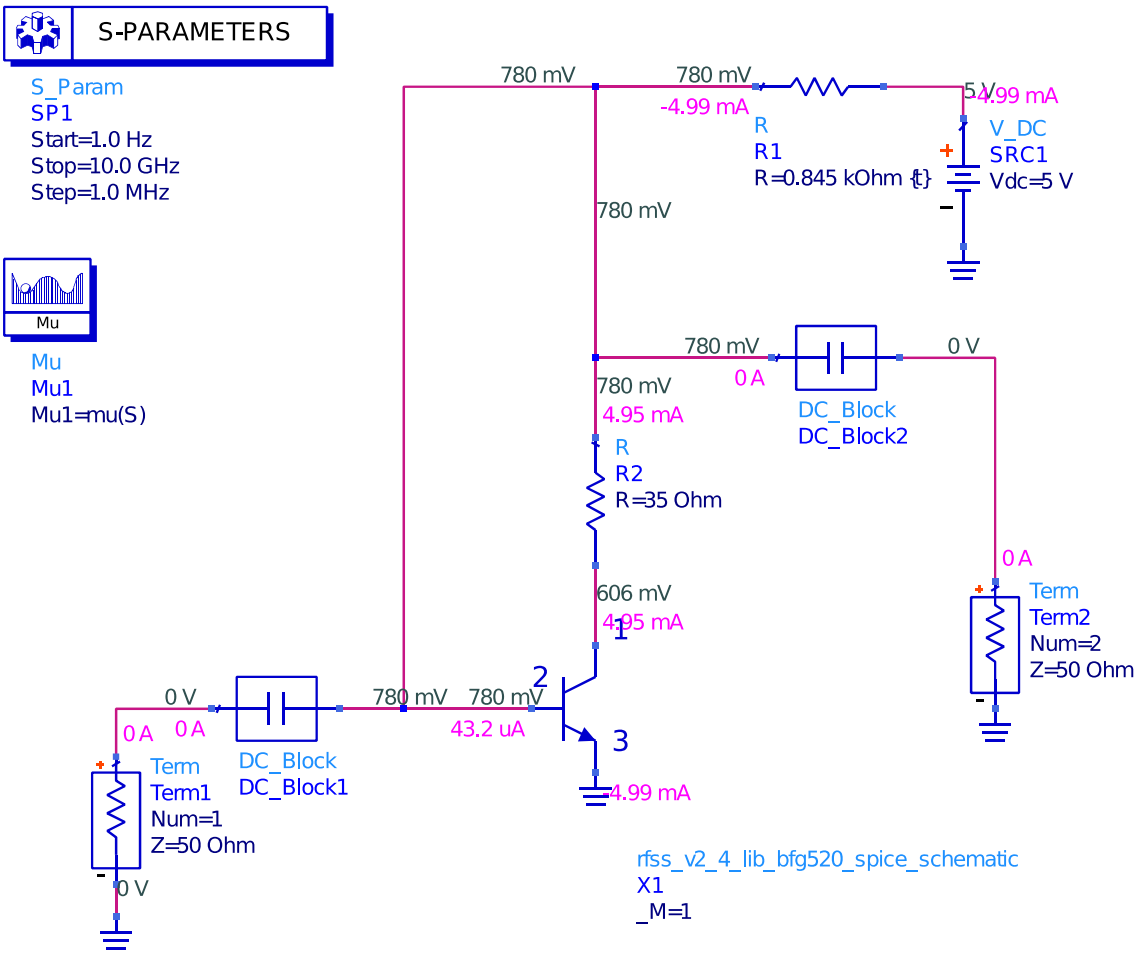

Figure 57. Simulation schematic for the stabilized diode-connected transistor.

APPENDIX 2: LAYOUT MATERIAL

The schematic used in EAGLE for creating the layout is shown in Figure 58. The solder masks are presented in Figure 59 and Figure 60. The schematic for the layout in Figure 58 is inconsistent with the Figure 21. The component naming convention is different and there are additional components that are not present in the finalimplementation. These components are meant for optional stabilization circuitry. Both the logarithmic amplifier and the BJT amplifier have at the output a resistor and an inductor in parallel. They can be used to selectively alter the output impedance. The inductor presents a low impedance to lower frequencies while being perceived as high impedance for higher frequencies. The resistor is utilized to choose the output impedance for high frequencies. Rest of the optional circuitry is for stabilizing the operational amplifier.

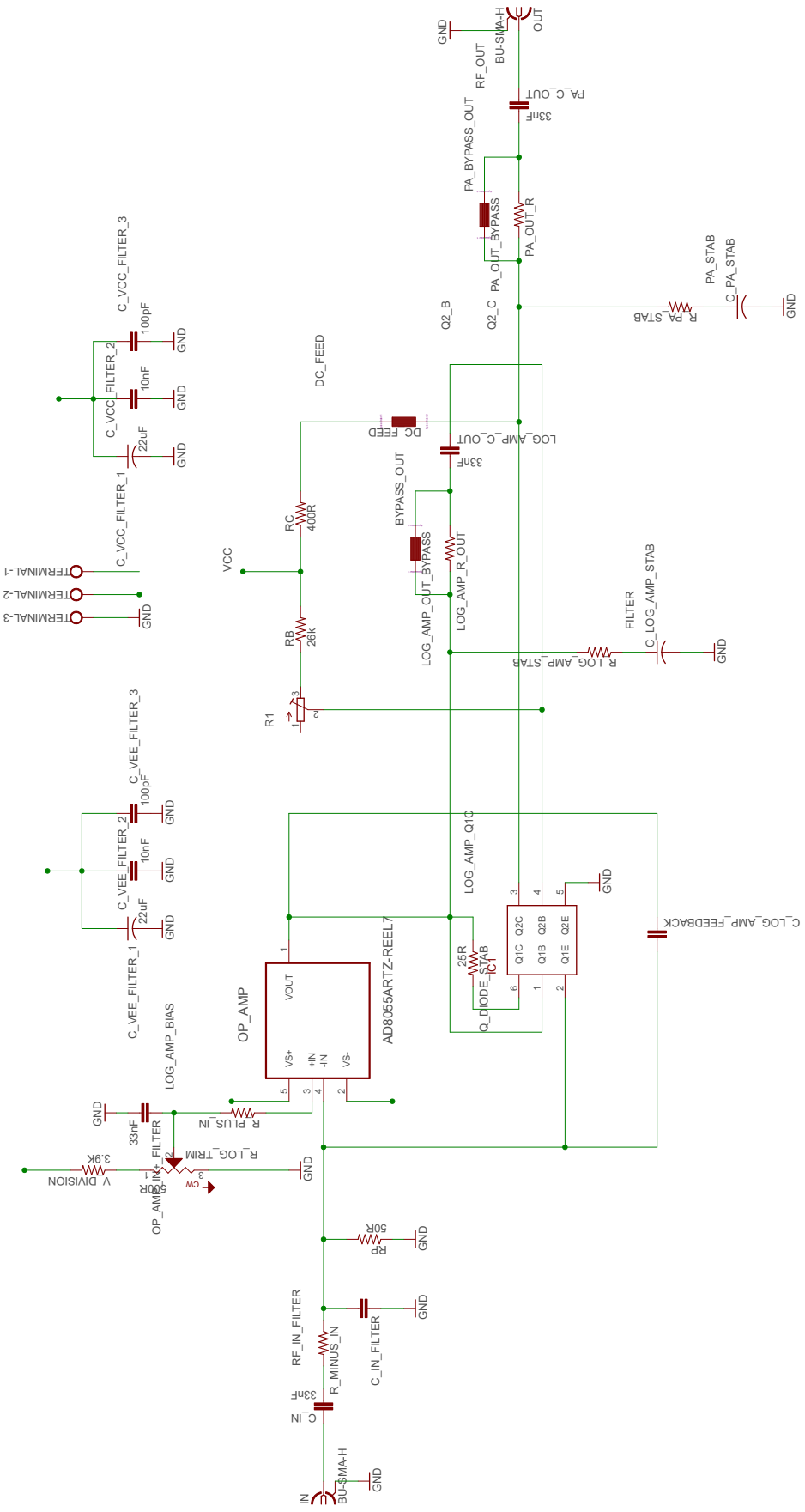

Figure 58. Linearized amplifier schematic in EAGLE.

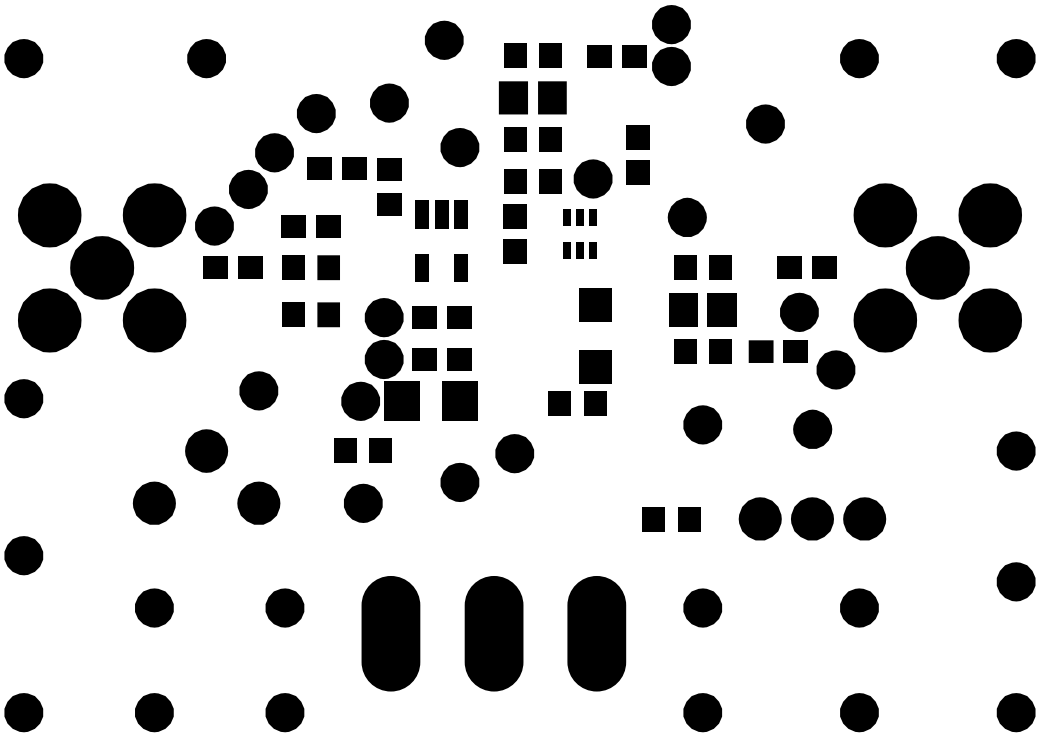

Figure 59. Top layer solder mask with drill holes included.

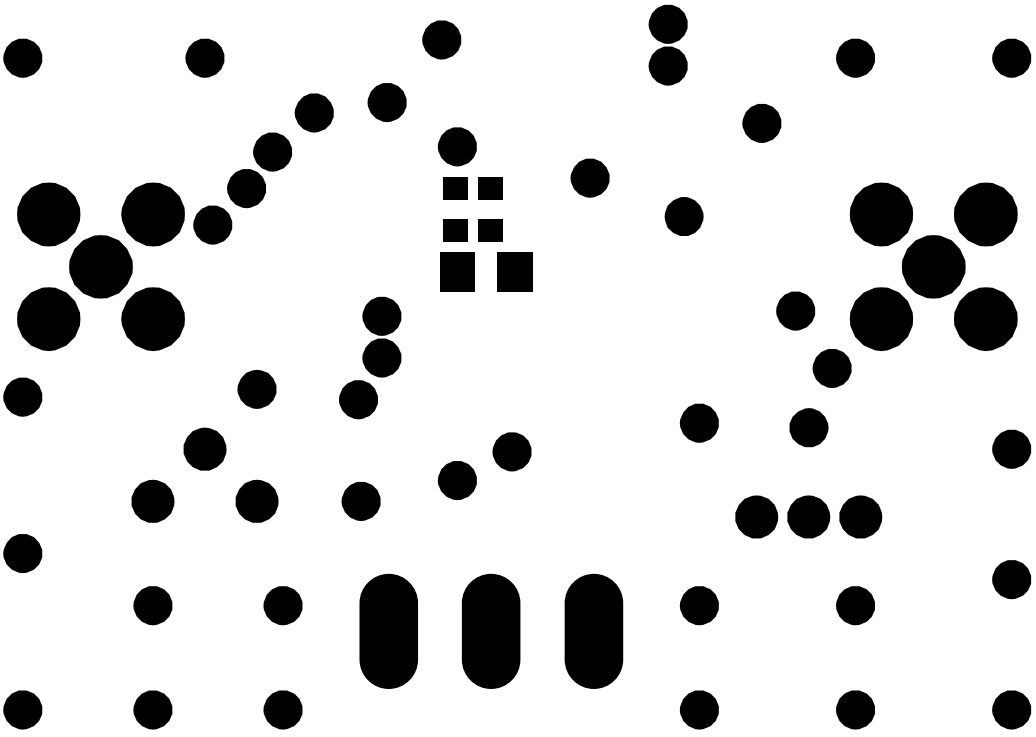

Figure 60. Bottom layer solder mask with drill holes included.

APPENDIX 3: WILKINSON POWER DIVIDER LAYOUT

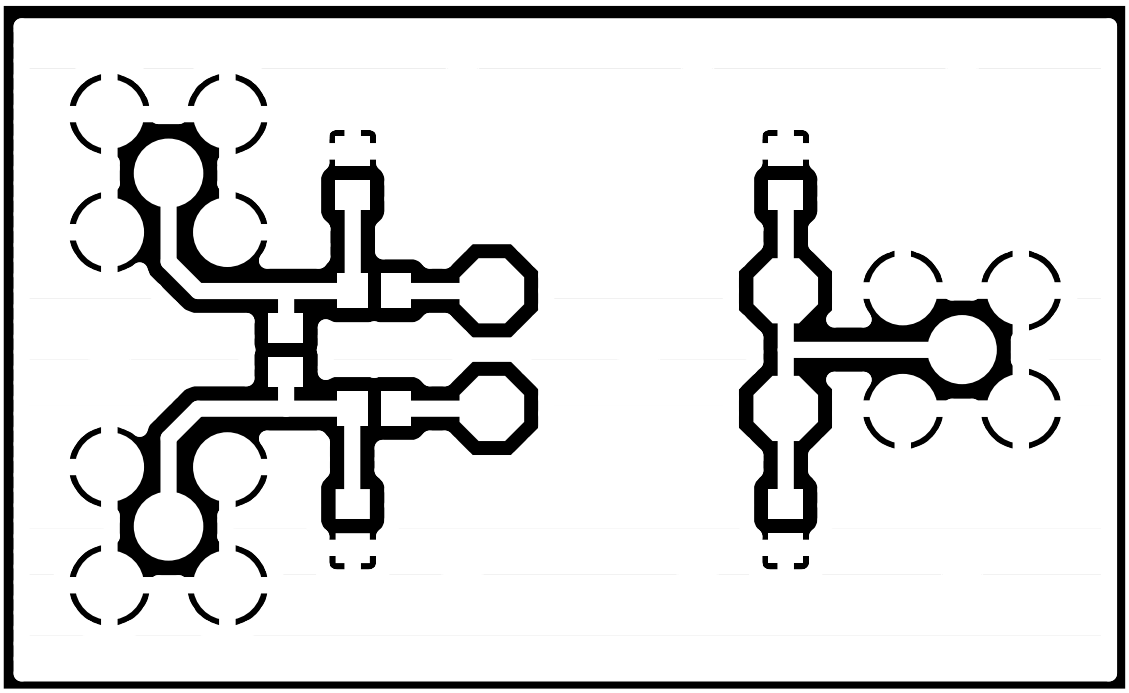

Figure 61. Wilkinson Power Divider top layer.

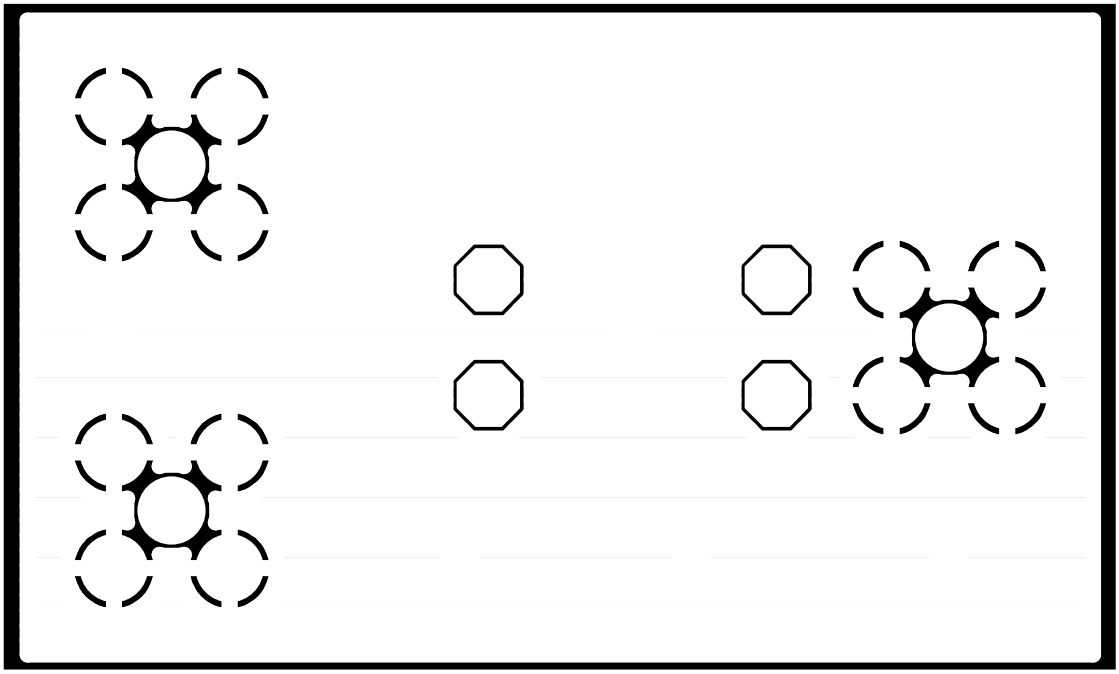

Figure 62. Wilkinson Power Divider bottom layer.

Figure 63. Picture of the top layer.

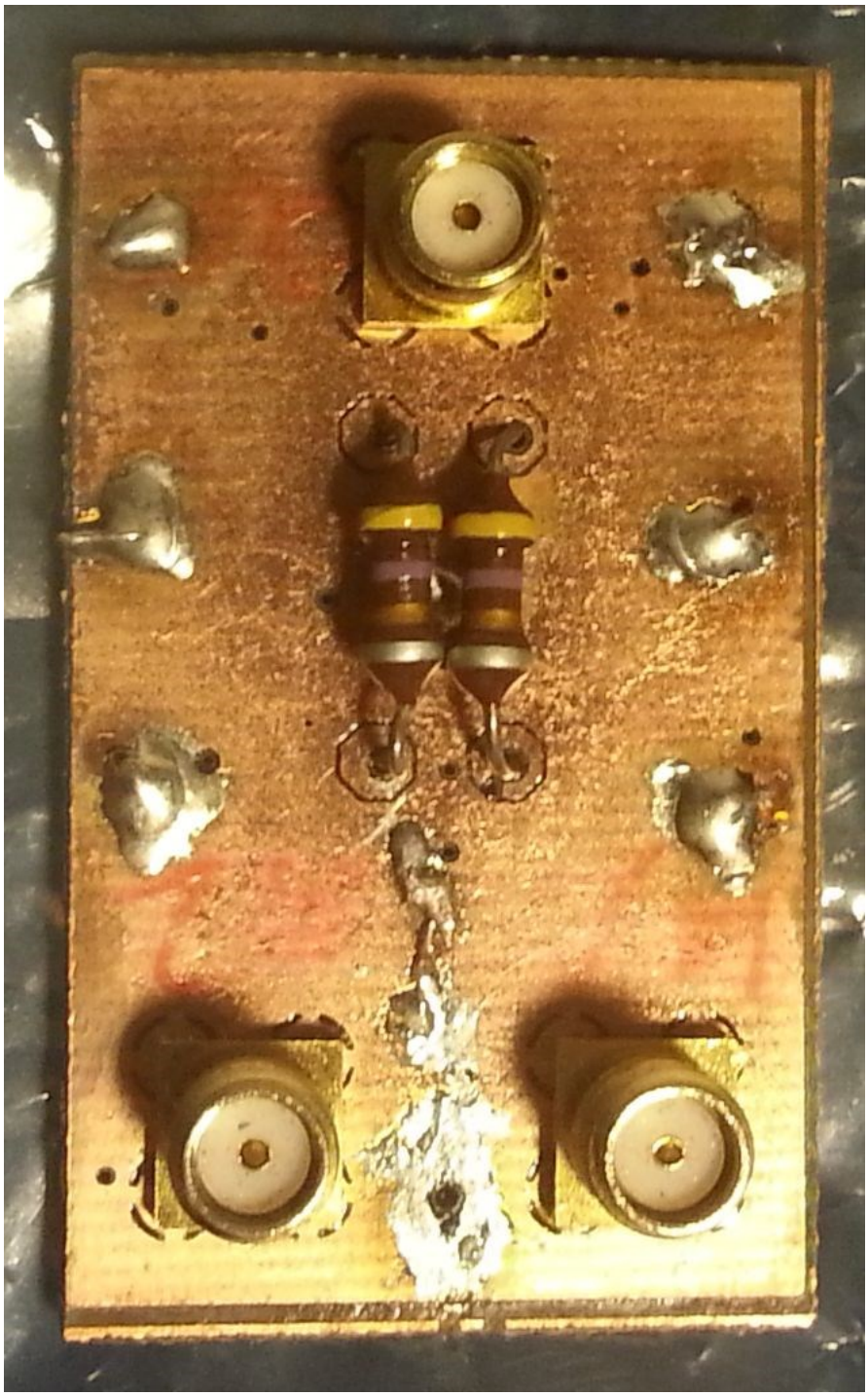

Figure 64. Picture of the bottom layer.

APPENDIX 4: IMPEDANCE TRANSFORMER LAYOUT

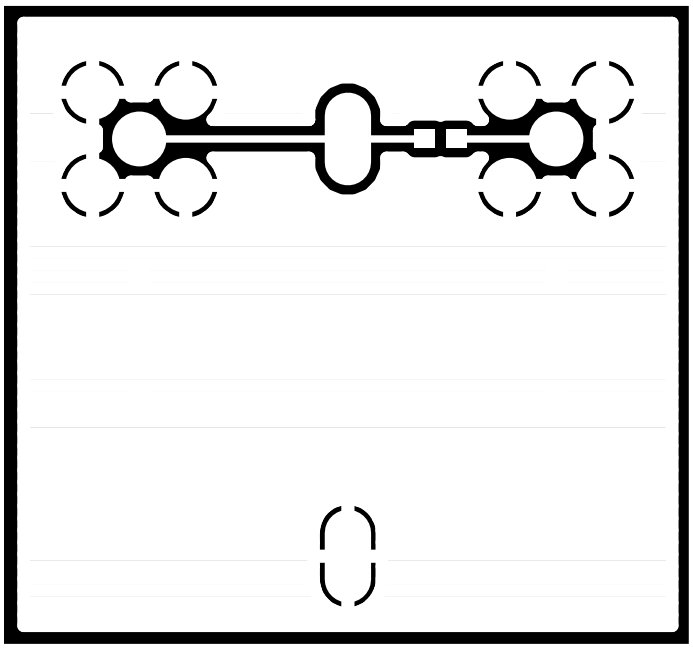

Figure 65. Impedance transformer top copper layer.

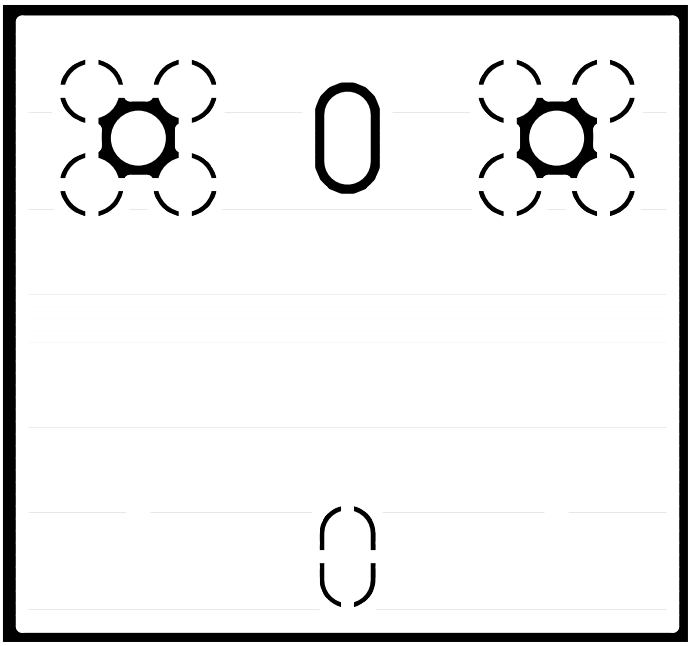

Figure 66. Impedance transformer bottom copper layer.

Figure 67. Impedance converter top layer.

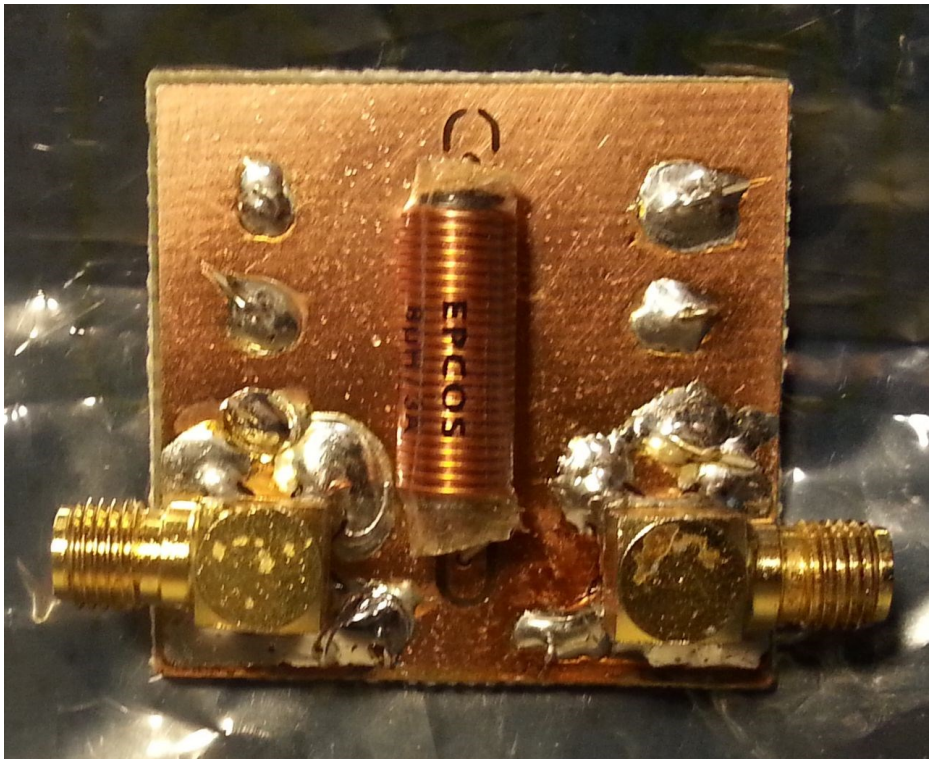

Figure 68. Impedance converter bottom layer.

APPENDIX 5: SIMULATION CIRCUITS

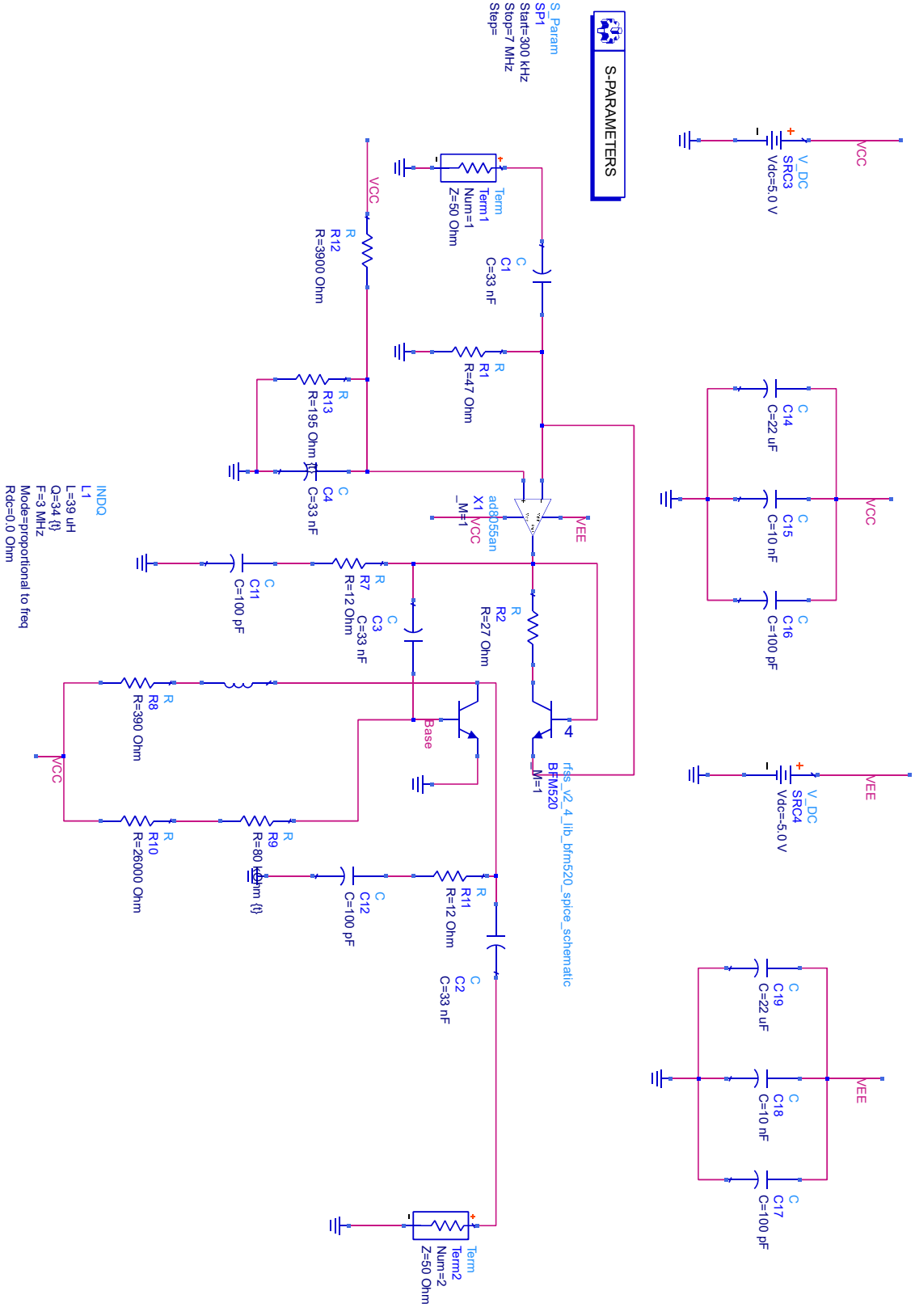

Figure 69. S21 simulation schematic with 50 Ω load.

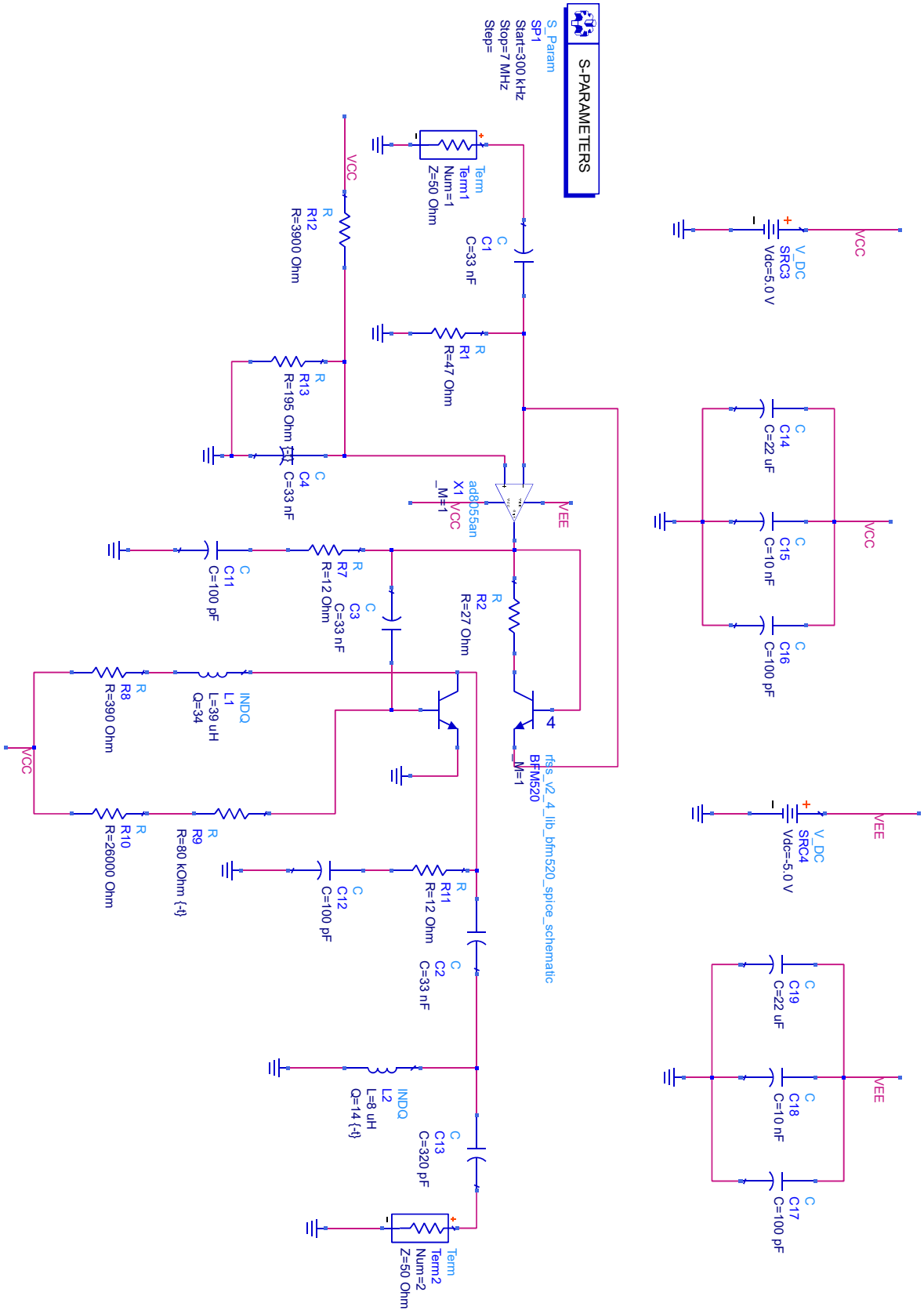

Figure 70. S21 simulation schematic with 500 Ω load.

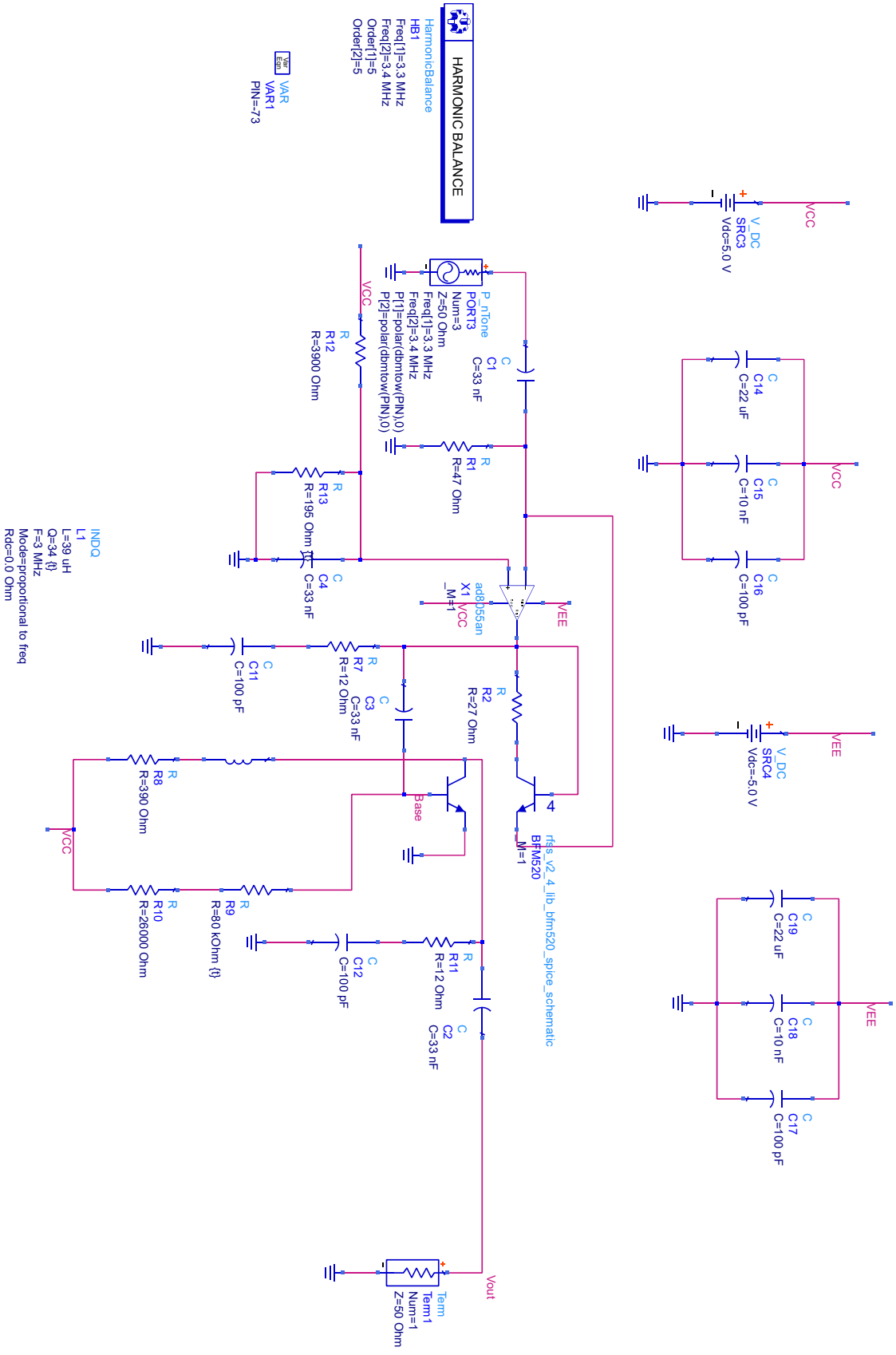

Figure 71. Intermodulation simulation schematic with 50 Ω load.

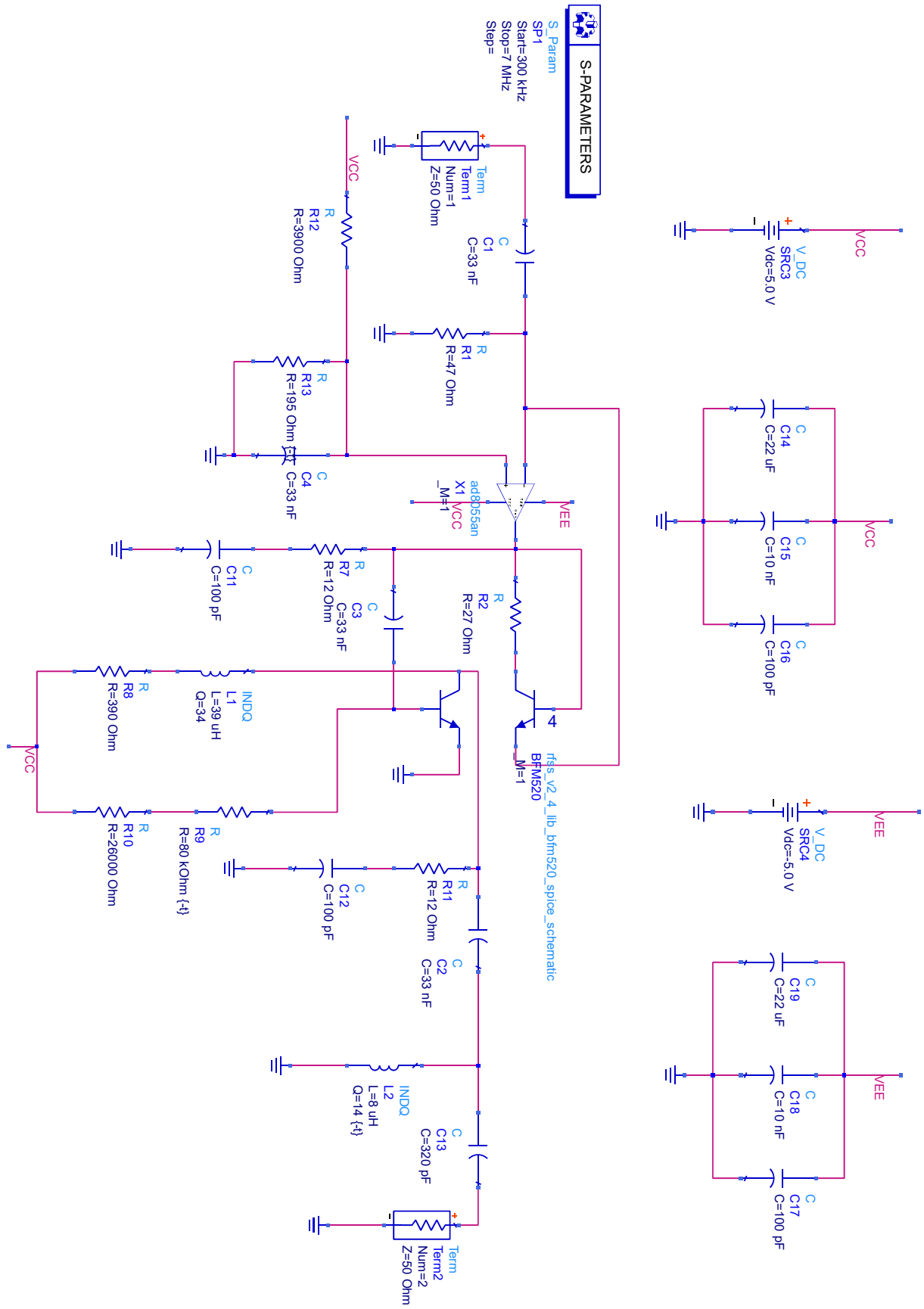

Figure 72. Intermodulation simulation schematic with 500 Ω load.