



TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

PETTERI LIIKKANEN

SIGNAL INTEGRITY ENHANCEMENTS FOR AUTOMATED LPDDR4 MEMORY TESTING SYSTEM

Master of Science thesis

The examiner and topic of the thesis was
approved by the Council of the Faculty
of Computing and Electrical Engineering
on 28 March 2018

ABSTRACT

PETTERI LIIKKANEN: Signal Integrity Enhancements for Automated LPDDR4 Memory Testing System

Tampere University of technology

Master of Science Thesis, 66 pages

March 2018

Master's Degree Program in Electrical Engineering

Major: Electronics

Examiner: Professor Karri Palovuori

Keywords: LPDDR4, PoP, memory testing, ATE, signal Integrity, mobile device

Designing a smart phone requires plenty of testing, tweaking and verification to offer flawlessly functioning high-end products for the customers. Fine-tuning and verifying the memory interface between the application processor and memory, is one important area, which ensures the reliable operation of the device over different operating conditions. Automated testing process reduces the amount of manual measurements, and speeds up the development cycle of the product.

However, because of the rising *bandwidth* (BW) of memories, the *signal integrity* (SI) properties of the currently used memory testing system have begun to interfere with the *device under test* (DUT) by causing stability issues. Also, the measured waveforms have not been corresponding to the expected results with the latest memory modules with high data rates and clock speeds. This master's thesis combines the previous experience and research about the topic, and introduces some new techniques to improve the measurement quality and to minimize the measurement system's impact to signal properties of DUT.

The final goal is to upgrade the previously used automated memory testing system with newly developed techniques to allow good measurement quality with *4th generation low power double data rate* (LPDDR4) memories. In the future, the implemented system is meant to be compatible also with upcoming LPDDR memory generations, with very slight modifications.

With implemented memory testing system, there was no more previously mentioned stability issues and measured waveforms matched well to simulations. So at the end, the system performed as expected. There was couple of observations done during the designing and testing process which could improve the system marginally even further but they were not mandatory in terms of system's operation, and could be implemented easily to next revisions of breakout *printed wiring boards* (PWB) for memories with different *ball grid array* (BGA) pinouts.

TIIVISTELMÄ

PETTERI LIIKKANEN: Signal Integrity Enhancements for Automated LPDDR4 Memory Testing System

Tampereen teknillinen yliopisto

Diplomityö, 66 sivua

Maaliskuu 2018

Sähkötekniikan diplomi-insinöörin tutkinto-ohjelma

Pääaine: Elektroniikka

Tarkastaja: professori Karri Palovuori

Avainsanat: LPDDR4, PoP, muistintestaus, automatisoitu mittaus, signaali, mobiililaite

Älypuhelimien suunnittelu vaatii paljon testausta, virittelyä ja varmennusta moitteettomasti toimivien tuotteiden tarjoamiseksi asiakkaille. Prosessorin ja keskusmuistin välisen dataväylän hienosäätö ja varmennus on yksi tärkeä alue, joka varmistaa laitteen luotettavan toiminnan erilaisissa käyttöolosuhteissa. Automatisoitu testausprosessi vähentää manuaalisesti tehtävien mittausten määrää ja nopeuttaa tuotteen kehityssykliä.

Muistien kaistanleveyden kasvaessa nykyisen muistintestausjärjestelmän signaalin eheysominaisuudet ovat alkaneet häiritä testattavaa laitetta, aiheuttaen staabiiliusongelmia. Myöskään viimeisimmistä, korkeilla kellotaajuuksilla ja datanopeuksilla toimivista muistimoduuleista mitatut aaltomuodot eivät ole vastanneet odotettuja tuloksia. Tämä diplomityö yhdistää aikaisempia kokemuksia ja tutkimusta aiheesta, ja esittelee joitakin uusia tekniikoita mittaustulosten ja mittaustulosten mittaustulosta vääristävän vaikutuksen minimoimiseksi.

Lopullisena tavoitteena on parantaa aiemmin käytettyä muistintestausjärjestelmää käyttäen uusia kehitettyjä tekniikoita, jotka mahdollistavat hyvän mittaustuloksen LPDDR4 muisteilla. Toteutetun järjestelmän on tarkoitus olla yhteensopiva tulevien LPDDR muistisukupolvien kanssa erittäin vähäisin muutoksin.

Toteutetun muistintestausjärjestelmän kanssa aiemmin mainittuja stabiiliusongelmia ei ollut ja mitatut aaltomuodot vastasivat hyvin simulointeja. Lopuksi järjestelmä toimi kuten oli odotettu. Suunnittelu- ja testausprosessin aikana tehtiin joitakin havaintoja, joilla järjestelmää voitaisiin parantaa edelleen marginaalisesti. Parannukset eivät kuitenkaan olleet pakollisia järjestelmän toiminnan kannalta, ja ne voidaan toteuttaa helposti seuraavien piirilevyversioiden yhteydessä piireille, joilla on erilainen BGA pinnijärjestys.

PREFACE

This Master's thesis extends the previously made research with automated mobile phone's memory measurement systems and allows the top quality measurements to continue with new LPDDR4 memories with high memory BW. The work has been done for the Baseband team in Microsoft Mobile Oy in Tampere.

I would like to thank my supervisors Jouni Karinen, Sunil John and Tomi Mäkinen from Microsoft Mobile. Also, I want to thank, Joonas Möykkynen, Markku Alkki, Lauri Nissinen, Mika Jäsberg, Markku Koistinen and Henri Eskola for valuable comments, guidance and assistance during the design process. Also the comments from Riku Ranta and Gary Horning helped a lot during the finalization process of this thesis work.

A lot of people from different teams from sites in Tampere and Salo were involved in this project without forgetting the support from my family. Everyone, involved in this project, would not fit into this page, so thank you to all, equally!

"To invent, you need a good imagination and a pile of junk"

- Thomas Edison (1847-1931)

Vaasa, 18.03.2018

Petteri Liikkanen

Karitie 14D 27

65230 Vaasa

+358503449552

CONTENTS

| | | |
|-----|---|----|
| 1. | INTRODUCTION | 1 |
| 2. | THEORETICAL BACKGROUND | 3 |
| 2.1 | Signal integrity | 7 |
| 2.2 | Power integrity | 16 |
| 3. | CHARACTERIZATION OF THE PREVIOUS SYSTEM | 19 |
| 4. | DESIGN IMPROVEMENTS | 26 |
| 4.1 | Signal integrity and timing measurement BoB | 26 |
| 4.2 | Current consumption measurement BoB | 32 |
| 5. | POST-PROCESSING | 34 |
| 6. | PROTOTYPING | 38 |
| 6.1 | Probing system | 40 |
| 6.2 | Mechanical considerations | 42 |
| 6.3 | Board on Board design | 43 |
| 6.4 | The final implementation | 47 |
| 7. | RESULTS | 52 |
| 8. | CONCLUSIONS | 62 |

LIST OF SYMBOLS AND ABBREVIATIONS

ABBREVIATIONS

| | |
|-------|---|
| AC | Alternating current |
| ADC | analog-to-digital converter |
| AFR | Automatic Fixture Removal |
| BGA | Ball Grid Array |
| BoB | Breakout board |
| BW | Bandwidth |
| CSP | Chip-Scale Package |
| DC | Direct Current |
| Dk | Dielectric constant |
| DRAM | Dynamic Random Access Memory |
| DUT | Device Under Test |
| FR4 | Flame Resistant PWB material with type 4 epoxy resin |
| FV3 | PWB structure with stacked and filled any layer microvias |
| GND | Ground |
| GPIO | General Purpose Interface Bus |
| HDI | High Density Interconnect |
| HW | Hardware |
| IBIS | Input / Output Buffer Information Specification |
| IC | Integrated Circuit |
| LFSR | linear feedback shift register |
| LNA | Low-Noise Amplifier |
| MEMS | Microelectromechanical Systems |
| LPDDR | Low Power Double Data Rate |
| NPTH | Non-Plated Through Hole |
| ODT | On-die termination |
| PDN | Power Delivery Network |
| PI | Power integrity |
| PoP | Package-On-Package |
| PWB | Printed Wiring Board |
| RCCu | Resin-Coated Copper |
| RF | Radio Frequency |

| | |
|-------------|--------------------------|
| SI | Signal Integrity |
| SMA | SubMiniature version A |
| SMD | Surface Mount Device |
| SNR | Signal to Noise Ratio |
| S-parameter | Scattering parameter |
| SP6T | Single-Pole Six-Throw |
| SPDT | Single-Pole Double-Throw |
| VNA | Vector Network Analyzer |

SYMBOLS

| | |
|--------------|---|
| β | Propagation constant |
| Γ | Reflection coefficient |
| δ_s | Skin depth |
| ϵ_r | Relative permittivity |
| μ_0 | Permeability of vacuum |
| σ | Conductivity loss |
| b | Height of substrate between two ground layers |
| c | Speed of light |
| G | Conductance |
| l | Length |
| RL | Return Loss |
| VF | Velocity Factor |
| W_e | Effective width of conductor |
| Z | Impedance |

1. INTRODUCTION

Performance and features of mobile phones have developed rapidly, while the size requirements are getting tighter because customers want thinner devices with good battery life and durability. These requirements set the size limit for the actual mobile phone's *printed wiring board* (PWB) and the amount and size of components that can be utilized. Two main approaches to implement memory into mobile device is to use a separate memory *integrated circuit* (IC), which communicates with processor via signal traces of the mainboard. The second, and more common approach in high-end devices is to use a *package-on-package* (PoP) stacked *application processor* (AP) and *low power double data rate* (LPDDR) memory. This thesis work presents the memory testing system for 4th generation *low power double data rate* (LPDDR4) memories but the same technique could be utilized also with different LPDDR generations and memory interface techniques with minor modifications.

Table 1 Clock frequency and core voltage comparison in different LPDDR generations. [1, p.5]

| | LPDDR | LPDDR2 | LPDDR3 | LPDDR4 |
|----------------------------------|-------|--------|--------|--------|
| Approx. year | 2005 | 2010 | 2013 | 2015 |
| IO data rate (Mbps / pin) | 400 | 1066 | 1866 | 3200+ |
| Clock frequency (MHz) | 200 | 533 | 933 | 1600+ |
| Core voltage (V) | 1.8 | 1.2 | 1.2 | 1.1 |

Memories are getting faster, but the physical size and pin count of the memory *chip-scale packages* (CSP) are still limited due to the size requirements of the mobile devices. This obviously means that the data pins of the memory must have higher data rates, or the width of the data bus needs to grow to increase the total data *bandwidth* (BW) of the memory. Table 1 presents the rapidly increasing memory data BW and other key specifications of LPDDR memory generations.

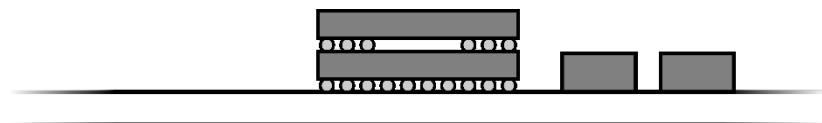


Figure 1 Side view of PWB with PoP stacked AP and LPDDR4 memory and passive components.

Logically, the state of the single data pin can be ‘1’ or ‘0’. However, due to physical properties of electricity, the transition from one logical state to another cannot be infinitely fast. The transition time, also called rise and fall time, sets the maximum limit to the highest usable data rate for a single data line. The PoP stacked AP and *dynamic random access memory* (DRAM) are reflow soldered directly to each other in the final product, as presented in Figure 1, so *signal integrity* (SI) issues related to *hardware* (HW) design are managed by IC manufacturers. However, bus transceiver and timing parameters are configurable by software [2], and the verification of software parameters is done by the manufacturer of the end product. Also, current consumption measurements are done to achieve the best possible voltage regulation characteristics and battery life of the product.

Measuring all the needed signals manually would be very time-consuming and unpractical. Previously signals have been measured by an automated, computer controlled setup which includes oscilloscope, switch matrix and PWB attached multi-position probes [4]. The currently used setup has been developed originally for LPDDR3 and lower speed grade LPDDR4 memories. However, lately the increasing clock speeds have introduced a new problem – the measurement setup interferes with the *device under test* (DUT) so much that the device becomes unstable, or even unable to power the device up at all. It also means that the measured signal is not the same as it would be without the measurement system.

The goal of this master’s thesis is to characterize the bottlenecks in the currently used automated memory testing system and introduce some new techniques to improve measured signal quality and the operation of the DUT itself. Among the other things, this thesis work introduces a new probing technique, which extends the actual probing point closer to the wanted measurement node by utilizing a carefully impedance controlled transmission line and by removing the need for an external oscilloscope probe with high input impedance. The design is improved further by introducing a new *breakout board* (BoB) component placement topology which allows the measurement system to be more invisible for the DUT. The new BoB design takes the current measurement capability to a separate BoB, which has a newly presented memory activity probing system that utilizes capacitive coupling. The interference between DUT and measurement system in a capacitively coupled probing system is negligible and the SI is very good.

The first part of this master’s thesis presents the background theory behind the newly designed improvements to the measurement system. After that, the old system is characterized in chapter three, and new design improvements, based on the previously made observations, are presented in the fourth chapter. Chapter five introduces digital post-processing techniques to improve the measurement results further. The implemented measurement system is presented in chapter six, and the performance measurements are compared to the previously used system in chapter seven. Finally, chapter eight concludes this master’s thesis.

2. THEORETICAL BACKGROUND

While the utilized frequency BW increases, transmission line theory plays a more and more significant role in any design related to data signals between the receiving and transmitting end. In high BW applications, like the memory testing system presented in this master's thesis, even minor non-idealities can affect the signal's properties quite radically. This chapter presents briefly the background theory behind the techniques, used in this LPDDR4 memory testing system.

Complex digital systems, like the memory interface between the AP and DRAM includes more than a hundred signals, in which SI must be well implemented to allow fast data transfers reliably. Basically, the DRAM interface includes parallel data signals and clock, or strobe signals, which initiate the data transfer. The total throughput of the memory interface can be increased by adding the bit width of the bus or by rising the clock frequency. However, the size and SI properties of the IC package limits the maximum reasonable amount of parallel data signals, so also the clock speeds are getting constantly higher. Single LPDDR4 CSP also includes multiple ICs, which operate in parallel. By knowing the IC and driver configuration, the amount of the measured signal can be reduced to allow a simpler measurement setup with higher measurement quality. At minimum, only one of the signals in same signal group with similar drivers and driver configurations is needed and the other signals in the same group can be expected to be similar enough with each other.

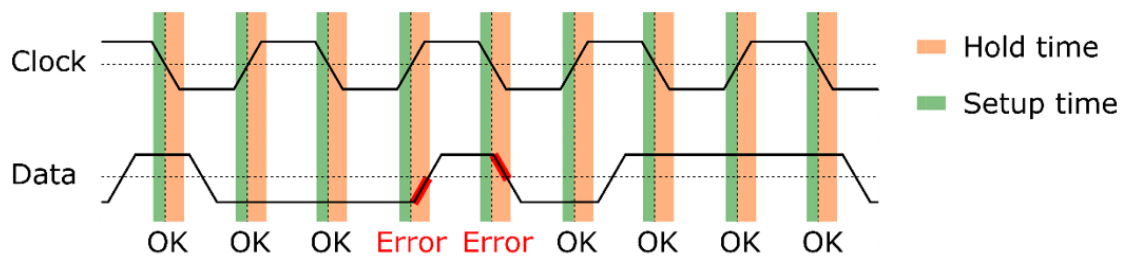


Figure 2 Illustrative figure of setup and hold time requirements regarding to typical clock and data signals in DDR system.

In simple terms, we can inspect every measured data – clock or strobe signal pair to get all the needed information. Figure 2 shows the relation between the data and strobe signals. The data signal must stay in its state at least for a specified setup time before the edge of the clock signal occurs and the data is read. Also, the signal must stay in its state at least for a specified hold time after the data strobe occurs to prove reliable data transfer. There are defined voltage threshold values for high and low status, and the transition must be fast enough to achieve the needed voltage value after the hold time but before the beginning of the setup time of the following bit. This requirement creates a relation

between the strobe signal and the data signal. If the state of the signal alters too slowly, the setup and hold time requirements are not met, and if the phase offset between these two signals is not configured properly, the system may violate the setup or hold time requirements. The competition in mobile device markets is intense and manufacturers are pushing the IC's to operate as fast as possible, and the previously explained timing tolerances are very strict. [5, p.510]

$$V(t) = V_{offset} + \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{V_{ampl} \cdot \sin(2\pi(2n-1) \cdot t \cdot f)}{2n-1} \quad (1)$$

Based on the Fourier's series theorem, an ideal square wave is composed of an infinite amount of sine waves with different amplitudes and frequencies, which can be extracted from Formula 1 [6, p. 17]. Frequency of n th harmonic component can be calculated by $(2n-1)f, n \in \mathbb{N}^+$, and the amplitude of each frequency component by $\frac{4}{\pi} \frac{A}{(2n-1)}, n \in \mathbb{N}^+$. One frequency component forms only a sine wave at the frequency to signal's base frequency. If more frequency components are included, the resulting sum signal begins to look more like a square wave, depending on the amount of utilized frequency components. Mathematically it is possible to generate an ideal square wave but in a real electronic system, the width of the usable BW and frequency components depends on the properties of components and transmission line.

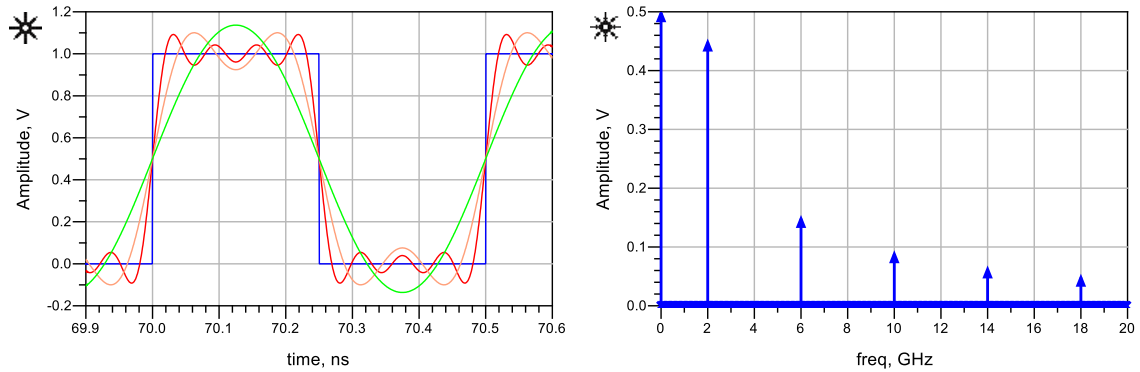


Figure 3 Ideal square wave and its harmonic frequency components in 20 GHz range. Also non-ideal square waves presented with 1, 2 and 4 frequency components included.

As stated, a signal's voltage value cannot alter infinitely fast from one level to another. It would need a transmitter with infinite BW. Figure 3 presents the ideal square wave and the corresponding frequency domain response. As can be seen, the signal transition becomes faster when there are more frequency components included.

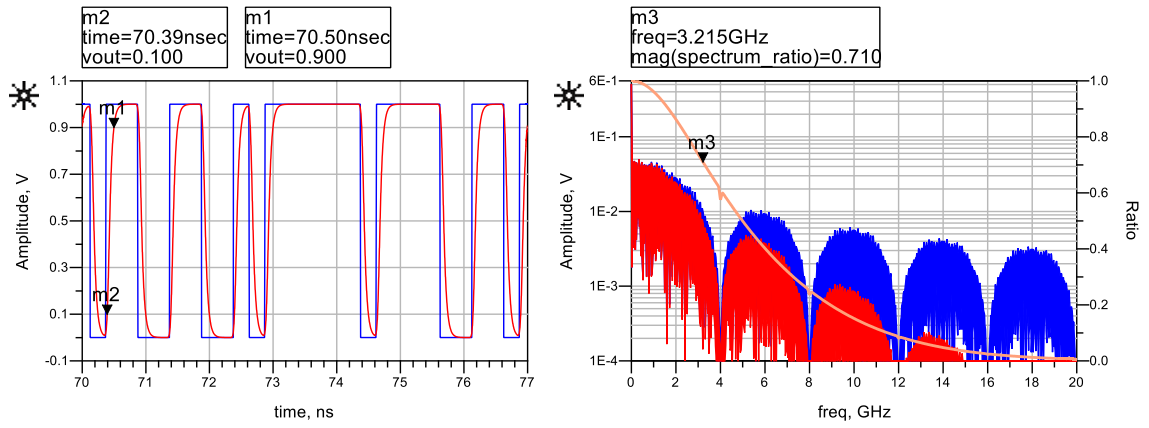


Figure 4 Frequency BW utilization comparison with ideal LFSR source and same signal with limited transition speed. The brown trace presents the amplitude ratio between the ideal and non-ideal frequency components.

Figure 4 brings the previously presented theory closer to real-world digital high-speed applications. While the first Fourier's series example had only a continuous, repeating square wave signal, the frequency spectrum would correspond quite well to continuous clock signals. However, in data signals, the time interval between level transitions will vary in discrete time steps because the data might have more than one logical one or zero in a row. Figure 4 illustrates the ideal data signal with infinitely fast rise and fall times, generated with *linear feedback shift register* (LFSR) algorithm, and another signal, which looks a lot more like a real measured signal from a high speed digital system with the signal's transition speed limited by the circuit's physical properties. Instead of utilizing infinite frequency BW, the BW of the example signal in Figure 4 signal is only approximately 3.2 GHz, as the marker at -3 dB point indicates.

$$BW = \frac{0.35}{t_{ns}} \quad (2)$$

Based on the previous explanation, the needed system's BW and rise and fall time have a relation. As Figure 4 presents, the measured rise time from 10 % to 90 % is 110 ps. Now we can use the relation [7, p.3], presented in Formula 2, to estimate the needed BW, which would be 3.2 GHz in this case. The calculated value matches the observed -3 dB point in frequency domain plot in Figure 4.

In conclusion, the measurement system must have a frequency BW wide enough to be able to capture all the needed frequency content from the inspected system. Generally, the BW of the measurement system must have a certain margin compared to the BW requirements of the DUT itself. If the signal's transition time would be out of the specification by being too fast, the measurement system must have high enough BW to be able to detect the problem. Also, the measurement system is intended to be usable in the future, with higher speed DUT's without major upgrades, so it must be taken into account in the design process.

According to Agilent's application note [8], a good rule of thumb is to have a measurement system with a BW of five times the clock frequency of a DUT. This estimation is quite rough because the estimation does not involve the signal's transition time. More precise BW value can be calculated by determining the previously mentioned fastest signal's transition speed and multiplying the BW by the factor, defined by the oscilloscope's low-pass filter's roll-off characteristics and the required measurement accuracy. For example, an oscilloscope with maximally flat frequency response and required accuracy of 3 % would induce a 6.4 GHz needed BW if the signal's fastest transition speed would be the same as in the previous example case, 110 ps. The measurement system, presented in this thesis, has an oscilloscope with four channels and analog BW of 16 GHz [9]. According to the previous example, 16 GHz maximally-flat analog BW with an accuracy of 3 % would allow signals with 44 ps, 10 – 90 % transition time.

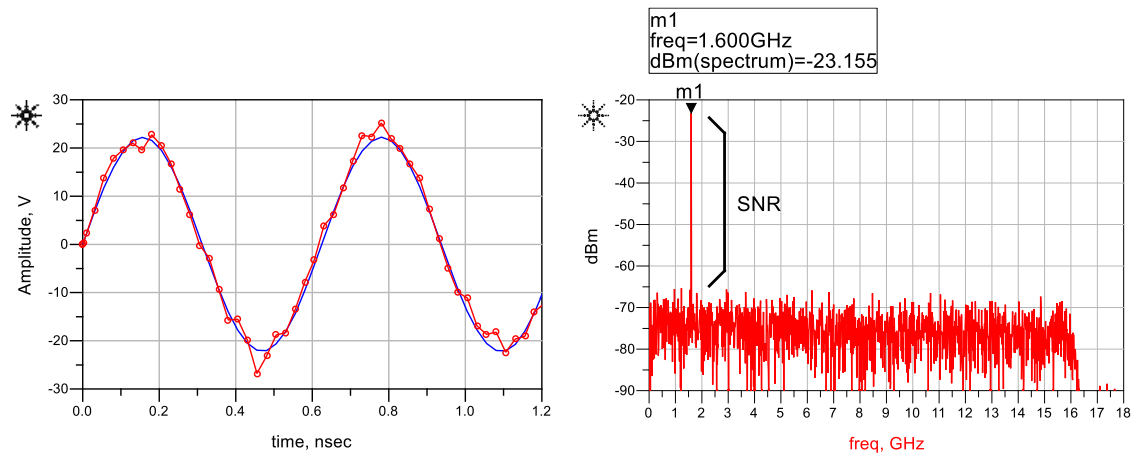


Figure 5 Blue: ideal 1.6 GHz sine wave, red: 1.6 GHz sine wave with 1.8 mV_{RMS} summed white noise. The oscilloscope's 40 GS/s sampling rate presented in red, noisy waveform. SNR can be calculated from the frequency domain presentation. Also the noise power reducing effect of the limited 16 GHz measurement BW can be seen from the frequency domain presentation.

Another important specification of the oscilloscope, is the sampling rate, which is illustrated in Figure 5. Defined by Nyquist's sampling theorem, the well-known factor of the oscilloscope's minimum sampling rate is two times the required BW. However, digital signals have also higher frequency components than the base frequency, so having just the sampling rate of two times of the clock frequency of the DUT would cause pre-shoot, over-shoot and varying edge speeds to the measurement results. According to Agilent's application note, an oscilloscope sampling rate of 4-8 times the measured clock frequency would induce accurate measurement results. [10] The oscilloscope, used in this master's thesis, has 40 GS/s sampling rate per channel when all four channels are utilized [9]. According to previously mentioned numbers, the sampling rate of the oscilloscope would be usable with digital signals up to 5 – 10 GHz clock rates.

A good measurement does not disturb the DUT by much. The measurement system, presented in this thesis work, implies the power division between the signal's receiver and the measurement system by using a *surface mount device* (SMD) resistor, which is placed in series with the measurement node. Too high of a resistance value would attenuate the signal too much between the DUT and the oscilloscope and too low of a value would disturb the DUT by taking a significant amount of power from the signal trace to the measurement node. The RMS noise floor of the oscilloscope used, is $0.35 \text{ mV}_{\text{rms}}$ at 10 mV/div setting and 16 GHz frequency BW [9]. An oscilloscope with good noise characteristics allows the usage of high resistance series resistors, while still maintaining adequate *signal-to-noise ratio* (SNR). The effect of the oscilloscope's noise level is presented in Figure 5, which also presents the effect of limited measurement BW. SNR can be calculated by knowing the total powers of fundamental signal and noise. If total power levels are not known, they can be calculated by dividing the frequency spectrum into bins and dividing the total power of signal bins with noise bins, excluding *direct current* (DC) offset and harmonic components [11]. This implies that if the measured signal does not utilize the full BW of the oscilloscope, it can be limited manually to remove extra noise content from the frequency spectrum.

2.1 Signal integrity

Good SI consists of many different aspects, which must be taken into account in the SI critical design. To inspect SI related issues, signal paths must be modelled as transmission lines with defined characteristic impedance, attenuation, propagation speed and other factors, like crosstalk to nearby signals. Analyzing the signal path starts by modelling the transmission line. A simple transmission line can be inspected analytically with relative ease but there are also powerful, computer aided tools to analyze transmission lines and the characteristics of a complex system of transmission lines. However, to understand the essence of the established problem or to make appropriate design solutions, the theory behind the curtain must be understood. [12]

Especially, the measurement system for SI critical design cannot have poor SI characteristics because then there would be uncertainty, if the perceived problem is caused by the DUT or the measurement system. Also, the timings or drive strengths cannot be fine-tuned reliably if the signal characteristics in a real product would not be very close to measured results.

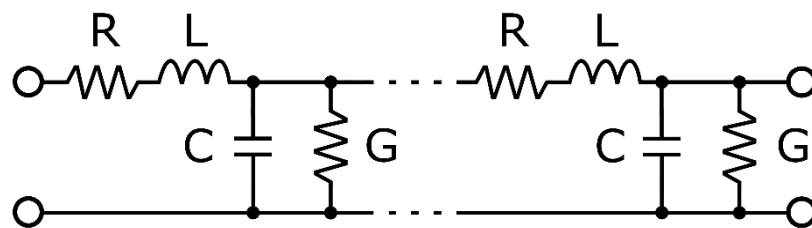


Figure 6 Equivalent circuit for lossy transmission line model.

The transmission line can be modelled as a series of equivalent circuits, presented in Figure 6. The model consists of an infinite amount of equivalent circuits, whose parameters are defined by the physical properties of the transmission line. There are different abstraction levels to inspect transmission lines. The basic model includes only a series inductance, caused by the conductor itself, and the parasitic capacitance of the return path. Also the lossy model can be used. It includes the parasitic series resistance of the conductor, and the parasitic conductance of insulator material. [13, p.48-51] Of course, the computer aided simulation tools do the lossy analysis with ease, but in analytic inspection, the latter two have often been omitted from the analysis for simplicity. In some cases, if the materials are far from ideal, or the transmission line is long, the lossy transmission line analysis must be used to get accurate results.

Every transmission line has its own characteristic impedance. In high speed signaling we are often interested in the transition points where two different transmission lines connect to each other. For example, connectors, vias or solder joints of IC's pins can cause impedance discontinuities. Also, the load impedance in the end of transmission path should be matched to the characteristic impedance of the transmission line. If the two impedances are different, part of the signal power reflects back to the opposite direction from the transition point. Most of the SI issues in high speed designs are typically a consequence of reflections, caused by impedance mismatches. For example, overshoot, undershoot, ringing and rise-time degradation are typical phenomenon, caused by reflections [12].

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (3)$$

$$RL_{dB} = 20 \log_{10} |\Gamma| \quad (4)$$

Return loss is a commonly used parameter to inspect the amount of power which is reflected from the merge point of two transmission lines, or from the end termination point of the transmission line. Formulas 3 and 4 present the reflection coefficient, which depends purely on the differences in two impedances. By using Formula 4, the same issue can be presented in decibels. For example, a return loss of 6 dB would mean that only 75 % of the power goes through the transition point, and 25 % of the power is reflected to another direction. If the reflected signal bounces again from another discontinuity in the transmission line, it starts to oscillate between these two points and causes visible ringing in the measured waveform [12].

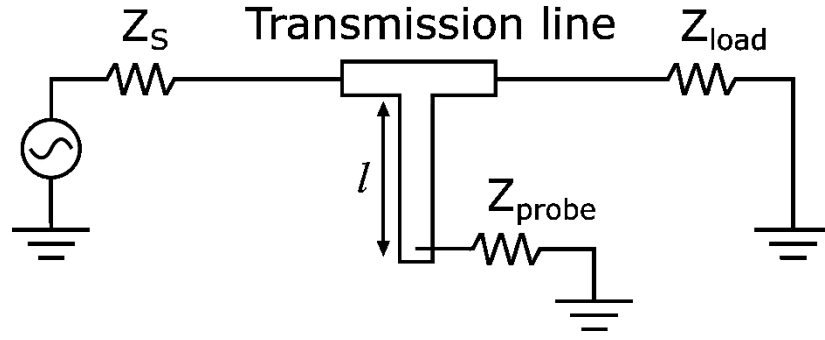


Figure 7 Simplified transmission line model of signal path between the signal transmitter and receiver with an extra branch of transmission line, which have equivalent resistance of oscilloscope probe, connected to it.

The main problem, observed in causing SI problems in the previous measurement system is presented more practically in the next chapter. To understand the root cause, we can simplify the measurement system according to Figure 7. There is a signal source, which could be for example an AP, transmitting data to the DRAM. There is a series resistor Z_s , which corresponds to the output impedance of the transmitting AP. The signal goes through the bond wires, *ball grid array* (BGA) balls and interposer PWB, which is modelled as a single transmission line. At the end, there is Z_{load} , which is the input impedance of the receiving DRAM IC. The measurement node is presented as an extra branch of the transmission line with a length of l , and then there is Z_{probe} , which presents the input impedance of the oscilloscope's probe.

At DC, the extra open-ended stub would not make any noticeable difference, but related to the previously presented transmission line theory, the reflection coefficient of an open-ended stub is 1, which means that the signal reflects completely from the open end of the transmission line.

As electricity has a finite propagation speed, the effect of the stub depends on the length of it and the frequency of the signal. At the crossing point, the signal coming from the source, and the signal which is reflected from the open-ended stub, will sum together, and the summed wave continues towards the end termination of the transmission line. If l is short and the frequency is low, then the reflected signal would be closely at the same phase at the crossing point, as the signal coming from the source, and the stub does not make any noticeable difference. On the other hand, if the wavelength of the signal would be four times the length of the stub, then the reflected signal would have exactly a 180° phase shift on the crossing point. The sum of these two is zero, so the open ended stub appears as a short circuit. [14]

$$Z_{in} = \left| Z_{load} \parallel Z_{tline} \cdot \frac{Z_{probe} + j Z_{tline} \cdot \tan(\beta L)}{Z_{tline} + j Z_{probe} \cdot \tan(\beta L)} \right|, \quad \beta L = \frac{2\pi \cdot f \cdot l}{VF \cdot c} \quad (5)$$

The characteristic impedance of the system is close to 50Ω , so in the ideal case Z_{load} and Z_{tline} would be 50Ω . The input impedance of the oscilloscope probe, Z_{probe} , varies over the frequency range. At DC, it is close to $25 \text{ k}\Omega$ but in $1 - 2 \text{ GHz}$ frequencies, we can assume it to be close to 300Ω [15]. By placing the values into Formula 5, we will notice that the oscilloscope probe with high input impedance does not affect the input impedance calculation by much, so in this case, the Z_{probe} can be omitted completely to simplify the formula. Then the stub should be assumed as open-ended. The velocity factor of the PWB trace is close to 0.5 and the length from AP – DRAM interconnection to the oscilloscope probe is $25 - 30 \text{ mm}$.

$$Z_{in} = |Z_{load} \parallel -j Z_{tline} \cdot \cot(\beta L)|$$

$$= \left(\frac{1}{Z_{load}} + \frac{1}{j Z_{tline} \cdot \cot(\beta L)} \right)^{-1} \quad (6)$$

Formula 6 describes basically the same situation, as previously presented in Figure 7 and Formula 5, but the effect of probe's impedance is omitted. The equation becomes much simpler but as stated, the difference is not significant. For accurate calculations, it should be noted that the impedance of the oscilloscope probe is not purely resistive, and also the reactive component should be noted. All in all, for accurate results, the most convenient way is to use simulator tools, which utilize all needed parameters with ease.

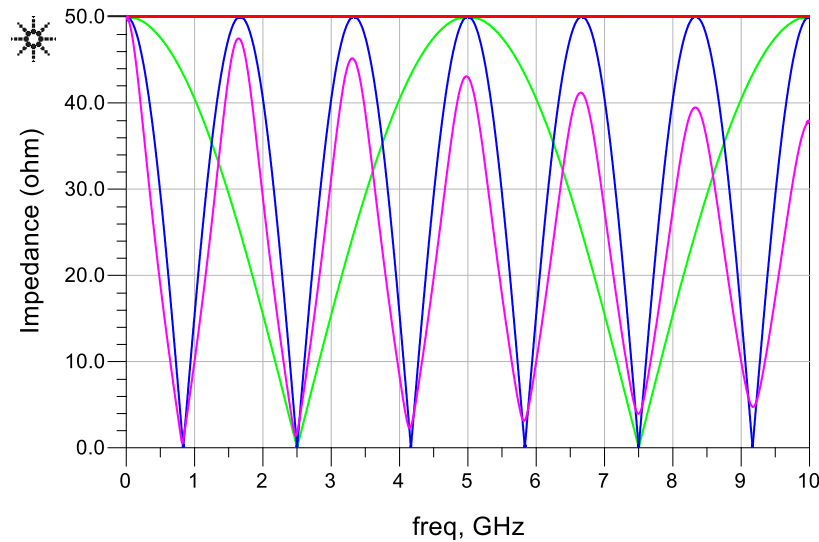


Figure 8 Impedance seen by the signal source with various stub configurations. Red: ideal 50Ω transmission line, Green: stub added with 0.1 ns electrical delay, Blue: stub added with 0.3 ns electrical delay, Magenta: stub added as realistic transmission line with lossy PWB simulation and 43 mm length.

Figure 8 illustrates the simulated impedance curves, which could be also calculated by using Formula 6. There is one transmission line without the stub. As expected, it is at the 50Ω mark over the frequency range because nothing disturbs the characteristic impedance of an ideal transmission line with proper terminations. Two of the traces are

simulated with the stub at 0.1 ns and 0.3 ns one-way electrical delays. One trace is simulated with the same configuration as the other simulation with a 0.3 ns stub, but the transmission line is done by using non-ideal, lossy PWB materials, which should correspond quite well to the characteristics of the PWB stackup, used in the implemented device. Now we can see that analytical solution gives good estimation, especially in the lower end of frequency range, but as the frequency increases, the real-world non-idealities begin to cause variations, which are taken into account with relative ease in simulation

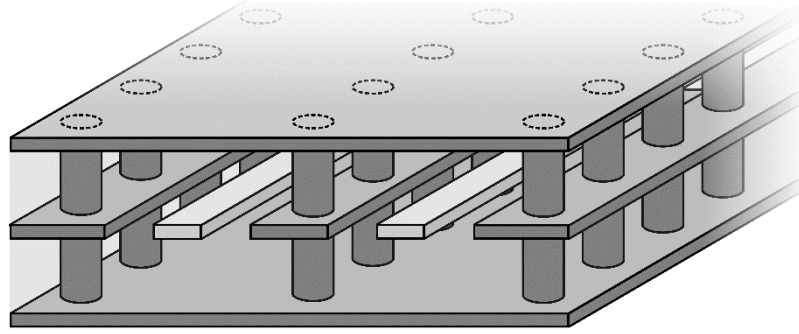


Figure 9 Cross section of PWB layer stack with two stripline signal routes and microvia ground fences.

software, if compared to analytical solution.

As stated earlier, the LPDDR memories have more than 100 signal routes which should be routed between the two IC's, and a portion of them are also routed to the measurement connector matrices, through the series resistor. The PWB should also have plenty of space for large ground and power planes. The chosen PWB stackup had ten layers, which should be enough for the BoB interposer. The stripline topology, presented in Figure 9, is the only practical way of implementing impedance critical signal paths when there are a large amount of impedance critical signal paths to route. All transmission lines are buried between two ground planes with coplanar ground planes and microvia fences. This arrangement forms a rectangular, grounded shield around the center conductor, which can also be perceived as a rectangular coaxial cable in the PWB. [16]

$$Z_0 = \frac{30 \pi}{\sqrt{\epsilon_r}} \frac{b}{W_e + 0.441b} \quad (7)$$

By using Formula 7 to get the characteristic impedance of a stripline, we will notice that compared to typical 10-layer *high density interconnect* (HDI) PWB layer dimensions, the dielectric material has to be quite thick or the trace width quite narrow to get the 50 Ω matched stripline [13, p.142]. Also, decreasing the *dielectric constant* (Dk) value of the dielectric material or reducing the copper thickness increases the characteristic impedance value of a stripline. These are well known drawbacks of microstrip transmission lines. However, by using a decent quality PWB manufacturer, tight requirements are met quite well and the impedance match will be close to the required 50 Ω . When calculating the characteristic impedance of a stripline, also the manufacturing tolerances of the PWB

manufacturer should be noted because even small variations can change the value of the characteristic impedance considerably. Many PWB manufacturers offer also an additional service for impedance matching, which could be used in impedance critical designs. By using this, the manufacturer measures the transmission lines after the boards are produced, and fine tunes the parameters so, that all the impedance critical transmission lines fit into the specified margins.

When designing the construction parameters of the previously presented stripline, the maximum allowed path loss should be noted. At low frequencies, the resistance of the copper trace will be the main attenuating factor. The obvious way to decrease the attenuation, is to increase the cross section area of the signal trace by using thicker copper or wider traces. However, at high frequencies, the current tends to flow through the surface of the conductor. This is called skin effect. The depth of effective thickness of current route depends on the frequency. The benefit, obtained by increasing the copper thickness might be very small in some cases, if the frequency is high enough. The effect of the used dielectric material typically does not matter in low frequency applications but the rapidly changing electrical field begins to rotate the dipoles in the dielectric material, and due to the friction, part of the signal's power transfers into heat. [17]

$$\delta_s = \sqrt{\frac{1}{\pi f \mu_0 \sigma}} \quad (8)$$

By using Formula 8, we can calculate the skin depth of the material. Copper's conductivity loss is $5.813 \cdot 10^7 \frac{S}{m}$ [13, p.719], so the skin depth at 100 MHz is approximately 6.6 μm . The result means that even the thinnest widely available copper layer thickness will not cause significant extra attenuation to the signal with similar BW, used in LPDDR4 memories. Of course a thicker PWB trace increases the conductor's skin area but the extra benefit is not very significant after a certain limit, defined by the skin depth. The extra copper thickness would be beneficial in power traces, because the frequency range of the specified *power delivery network* (PDN) impedance is much lower than the frequency range of data signals. Ideally, the layer could be combined so that the PWB includes thicker copper layers for power planes and thinner signal traces, which are needed in this project, based on simulations.

The layered structure of the PWB stack will not allow a perfect ground shield around the signal trace but the gap between two layers can be filled with vias, as presented in Figure 9. Via fences minimizes the parallel-plate mode, caused by the potential difference between the surrounding ground layers, and also enhances the isolation between two striplines, placed side by side on the same layer. Via fences are easy to implement in the PWB with HDI FV3 buildup technology, which allows placing a microvia between any two layers without affecting to other layers. To keep the characteristic impedance of the stripline high enough, the coplanar grounds should not be too close to the center

conductor. The preferable width of the slot around the center conductor is at least three times, and preferably 5 times the width of the center conductor. Too large of a distance will affect the electrical performance of the stripline by allowing pseudo rectangular waveguide modes, which have a cut-off frequency of $c/(2 \cdot w)$, where w is the total width of the slot around the center conductor. [16]

Another rule of thumb, considering the density of metallized vias in the via fence, is that the separation should be smaller than $1/8^{\text{th}}$ of the minimum wavelength, for which the stripline is designed to. This keeps the signal from leaking to neighbor transmission lines and the potential differences over two ground planes stays low enough. [16]

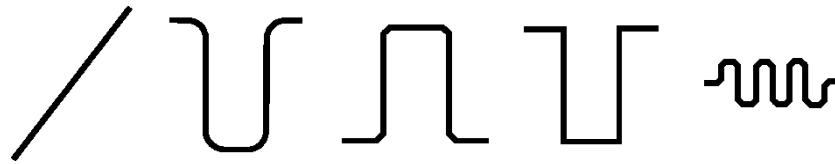


Figure 10 Simulated PWB length matching structures: straight line, smooth arcs, mitered lines, lines with 90 degree angles and meander line with mitered corners.

One part of the verification process, is to inspect the software configurable timing skew between the clock and data signals [2]. As electricity has finite propagation speed, it is important to note that the length of two different measurement paths are the same, so the measurement setup does not distract the original timing skew. Although the differences in the electrical delay of measurement paths will be characterized and compensated in post-processing, in the final measurement setup, there are three separate length matching groups in the PWB. When the length of the signal trace is defined, the next revisions of BoB interposers for different products are easier to make, and there will be no need to do new post-processing files, as the differences in length are equal in every BoB designs. When defining the length of the traces in same length matching group, the length is typically defined by the longest path, which will be routed as directly as possible. Other PWB traces in same group are lengthened to have that exact same length. Shorter distances are routed typically by doing curved PWB traces to increase the length. Figure 10 presents some techniques for increasing the length of the PWB trace.

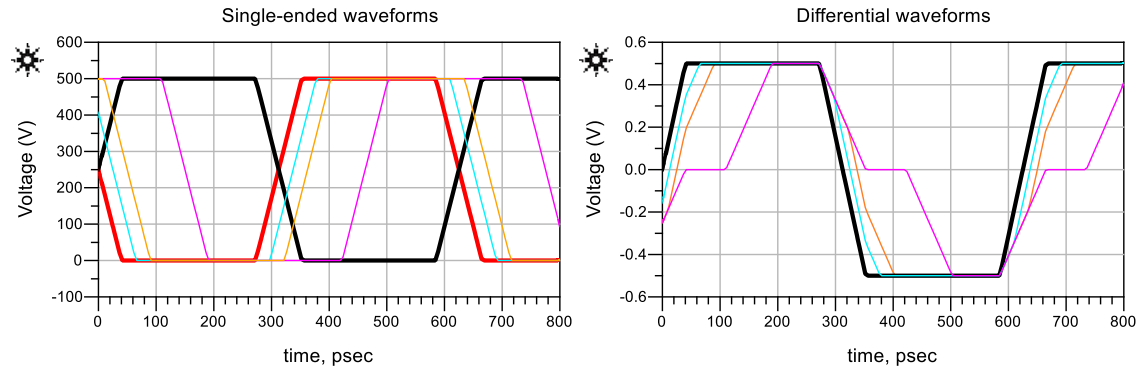


Figure 11 Effect of timing skew in differential signals. Red – Black signal pair with zero timing skew induces black differential waveform on the right side. The cyan signal has a 25 ps timing skew, orange 50 ps and magenta 150 ps timing skew. The base frequency of the signal is 1.6 GHz which corresponds to real memory interface clock rates.

However, only the timing skew of single-ended signals can be fully compensated in post-processing. Differential signals are more challenging because the signal is converted into single-ended before it can be measured with oscilloscope. Differential measurement paths can be compensated only if both of the signal paths in the differential pair are exactly the same. Figure 11 presents the effect of timing skew between the signals of the differential pair, when the signal is converted single-ended. This explains, why the measurement setup has 5 ps length matched coaxial cables in the differential pairs.

The shape of the previously presented length matching PWB structures does matter at high frequencies. The characteristic impedance of a transmission line is defined by the ratio of the capacitive and inductive properties of the trace. Tight corners will change the ratio slightly, and will cause impedance mismatches, which reflects a fraction of the signal to the opposite direction.

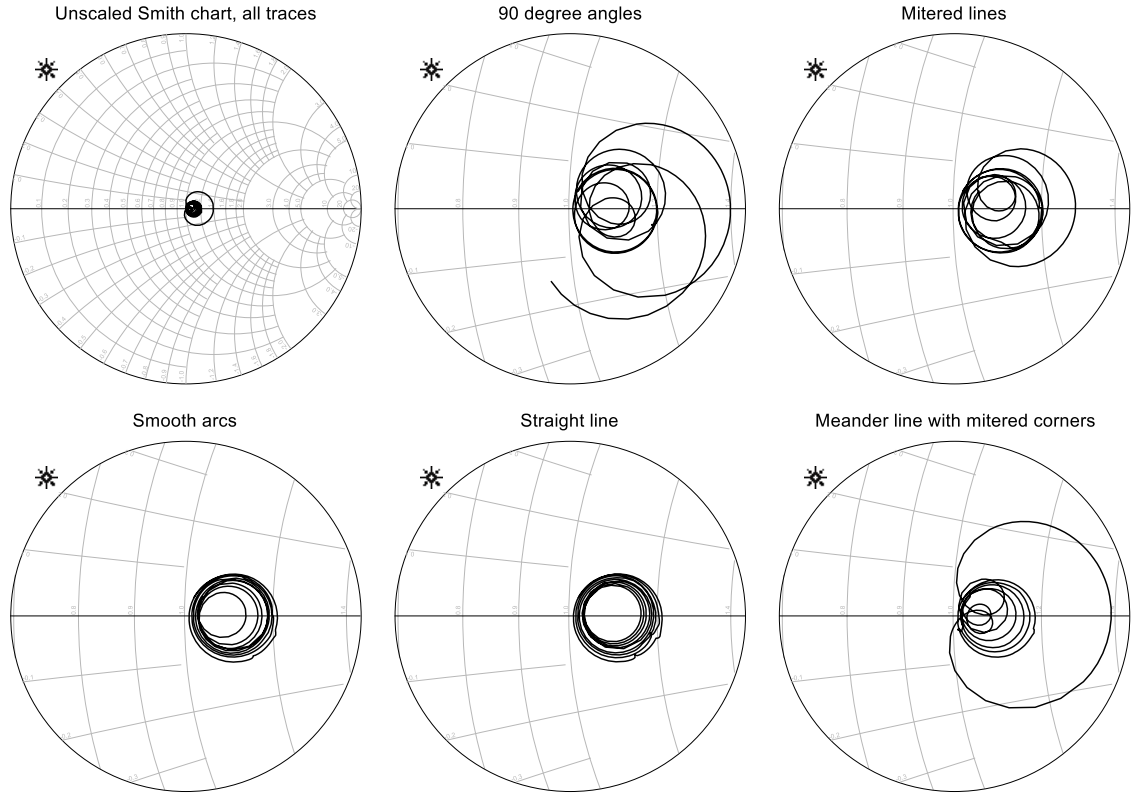


Figure 12 Corresponding Smith chart Γ -plane presentations for PWB traces with 8.1 mm electrical length, presented in Figure 10. Frequency sweep from 0.5 GHz to 80 GHz.

To analyze the effect of PWB routing and length matching technique's effect on the system's performance, a couple of different types of PWB trace length matching structures, presented in Figure 10, were simulated. Simulations were done by using a similar PWB stackup, materials and dimensions to produce a transmission line which corresponds to the real product, which is built along this thesis work. The electrical length of every stripline was 8.1 mm. Figure 12 presents the result. There were no major differences in the frequency band from 0 to 30 GHz, but extending the simulation frequency to 80 GHz, illustrates the best technique in terms of SI. A PWB trace with smooth arcs takes quite lot of PWB area, but the performance is very close to a straight PWB trace without corners. The next best option would be the trace with mitered corners. A tightly meandering trace with mitered lines is very space efficient, but the performance is not as good as with previously mentioned techniques. The worst option is a trace with 90 degree corners, which is obviously against all general PWB routing rules. The maximum usable frequency range of every technique depends on multiple factors and should be considered case by case. A very narrow trace width, which will be used in the PWB design of the SI BoB, is not very sensitive for tight corners. All in all, there is no significant impact to system performance with the utilized frequency BW and PWB routing properties. However, traces with smooth corners were used in the system that was built because by using more space efficient options, there would not have been any significant benefits. [16]

2.2 Power integrity

Good SI alone cannot ensure flawless operation of the device. Also, *power integrity* (PI) issues need to be considered. LPDDR4 memories do not consume a significant amount of power but this does not mean that there would not be PI challenges. Generally speaking, PI design can be divided into two parts – DC and *alternating current* (AC) analysis [18].

DC analysis inspects the voltage drop between the power supply and the analyzed device when the current stays constant. When the electrical current, properties of the metals used and the temperature are known, it is possible to calculate the voltage drop over the specified PDN. Low power mobile memories do not cause a significant DC voltage drop over multiple parallel supply voltage pins which are connected to uniform power planes, but at DC, the majority of the voltage loss is caused by the current shunt resistor which is used to measure the current of a specific voltage rail.

$$Z_{target} = \frac{V_{tolerance}}{I_{transient}} \quad (8)$$

Formula 8 can be used to calculate the best resistance value for the current shunt resistor. The resistance value should be as high as possible to provide a measurable amount of voltage loss over the current range of interest. When the maximum allowed voltage drop and the maximum peak current of the DUT are known, the maximum resistance value for the current shunt resistor can be calculated easily by using Ohm's law. The resistance of the PDN itself must be subtracted from the calculated value because the shunt resistor and the resistance of PDN are effectively connected in series. However, a simple DC analysis is not enough in practice, which might have very rapid and intense current peaks although the total average current consumption would be low.

AC analysis inspects the noise suppression characteristics of the PDN. With digital logic, like LPDDR memories, this is a very important issue to characterize properly. Every conductor inside the IC or on the PWB has a non-zero parasitic capacitance value. When the digital logic state toggles, the transistors pulls the conductor to *ground* (GND) or to the supply voltage. To change the voltage level fast enough, the current flow through the transistor must be high enough to charge the parasitic load capacitance. In digital IC's, voltage transitions occur in discrete time intervals and typically a vast amount of transitions occur simultaneously. This causes very significant, rapid current spikes, which causes switching noise to voltage supply rails. [19]

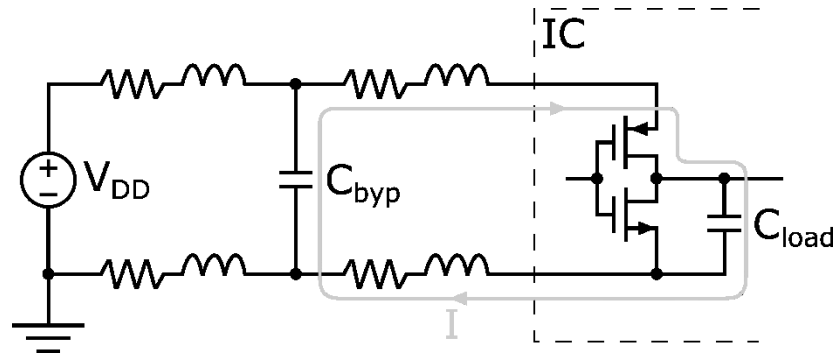


Figure 13 PDN of IC, and the path of current when the IC is driving the signal from '0' state to '1'.

At high frequencies, also the inductance of supply current loops needs to be characterized. The voltage regulator typically provides the transient response at low frequencies but at high frequencies, transient current is taken from bypass capacitors, which are located right next to the supply voltage pins of the IC. Figure 13 illustrates the previously mentioned push – pull transistor configuration, which toggles the state of signal to one or zero by charging or discharging the parasitic load capacitance. The current, required to charge C_{load} , is taken from the bypass capacitor. To minimize the current loop area and parasitic resistance, the bypass capacitor is placed always as close to the IC as possible. [19]

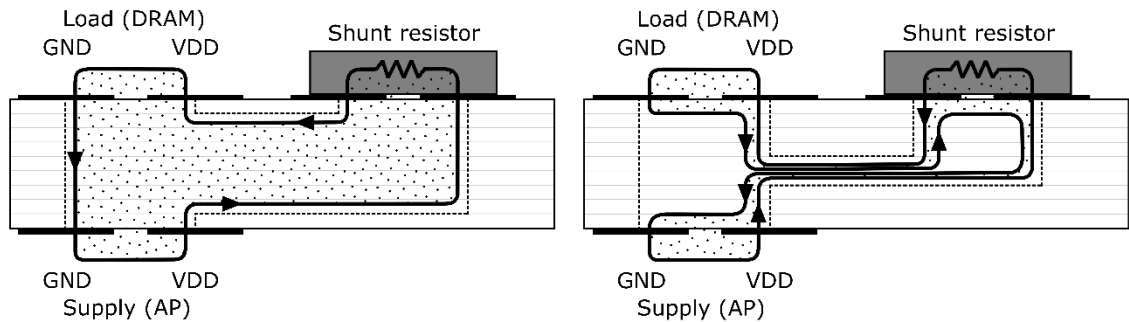


Figure 14 PWB's cross section from bad and good current measurement systems. The dotted area represents the current loop area, which should be minimized. On the left side there are top & bottom BGA pads for GND and supply voltage, and on the right side is the current shunt resistor.

Regarding to the design process of the current consumption measurement BoB and its tight voltage rail impedance requirements, also the PWB layer stackup design affects BoB's electrical performance. Large overlapping power and ground plane layers generate parasitic capacitance, which is good in power supply applications. The capacitance is not large but it is close to the IC and gives a very good transient response at high frequencies, which would be otherwise degraded by the parasitic inductance between the IC and the bypass capacitor. Also the power plane and the current's return path should be as close to each other as possible to minimize the inductance of the current loop, presented in Figure 14.

All in all, in complex digital systems, the power delivery network can be quite challenging to analyze, so the math is done often with the aid of PI simulation tools. In many cases, good PI needs a lot of PWB area and bypass capacitors. This may compromise the SI of data signals or the price of the product. Component manufacturers define specifications for their IC's, which must be met in the end product. Typically, a good product design aims certain impedance targets, however surpassing these targets by a large amount is not beneficial because of the extra cost incurred and lack of added value to the product. Bearing that in mind, the PDN of the measured DUT is already made to match the minimum requirements with a certain safety margin, so the extra interposer BoB between the AP and DRAM IC must have a very well designed PI to still meet the original PDN impedance requirements.

3. CHARACTERIZATION OF THE PREVIOUS SYSTEM

The existing system needs to be characterized carefully before starting to design the upgrades, which will extend the system's capabilities to measure the current high-end mobile devices and upcoming products. Good and well-functioning areas will be preserved and only the mandatory parts are upgraded to save effort and expenses. This chapter introduces the issues which need to be considered in order to extend the SI properties of the automated memory testing system.

In the beginning, the previous testing system was measured and simulated to detect the causes of the DUT's stability related issues, limited measurement BW and other SI issues. In general terms, the most significant issue was caused by the impedance match of the high impedance probes and the IC. Also, part of the issues were caused by the limited PWB area.

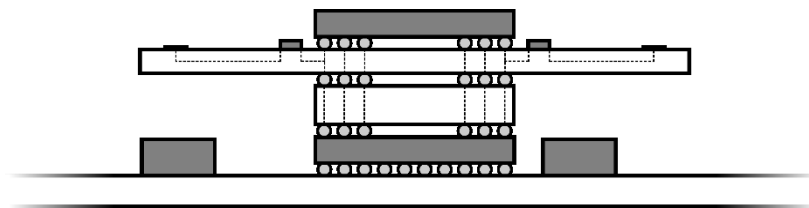


Figure 15 Cross section of the previously used memory testing system interposer stack.

As the Figure 15 shows, the AP is reflow soldered directly on the mainboard. On top of it, there is an interposer construction, which includes the riser board and the BoB. Riser board allows the required spacing between the BoB and the mainboard, so the passive components, next to the AP, will not come in contact with the BoB. At the top of the stack, there is the LPDDR memory IC.

The previous measurement system was capable of measuring almost every possible signal between the LPDDR memory and AP. There was also a current measurement capability embedded into the same BoB. The reason for that was primarily to maintain the compatibility between the existing measurement system, which connects to the interposer structure. Note that, the measurement system could not be fully compatible with the previous versions. In any case, it was also considered, if there would be any signals that does not have to be measured now, or in the future. By collaborating with memory specialists, there appeared to be a possibility to reduce a significant amount of the measured signals without notably compromising the coverage of memory verification measurement results. A reduced signal count leaves more PWB area for more ideal signal routing.

When considering the operation of a mobile device in general level, typically the memory interface have one of the highest frequency BW in the device. Any extra length in memory signal paths would eventually distort the signal, depending on the SI properties of the transmission line. Previously, the riser board had been reworked between the AP and DRAM because the removal of AP is not necessary when attaching the interposer construction on top of it. Also, the DRAM IC has typically less BGA balls with a larger pitch than the AP, so the BGA reballing needs less effort and reworking success is more probable. However, the riser board begins to distort the signal more when the utilized frequency BW increases. Based on the simulations, the riser is placed between the mainboard and the AP in the new design. The memory testing prototype device is dedicated only for memory testing, so it does not matter if the riser board slightly distorts non-memory signals, as long as it does not cause instability.

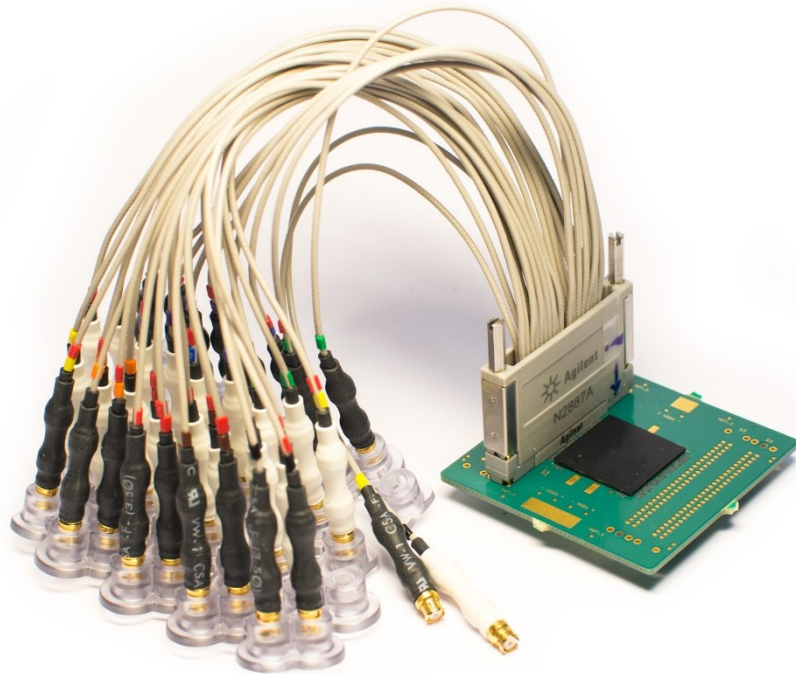


Figure 16 Agilent N2887A Probing matrix connected to the previous version of the LPDDR4 measurement BoB.

The previous background theory chapter introduced the problem caused by the combination of an extra branch of transmission line and the probe head with a high input impedance, connected to the system. The previously used Agilent's Soft touch probe head, presented in Figure 16, includes multiple probing tips, encapsulated into a small and handy connector, which allows a solderless attachment to the BoB. To inspect the system-level characteristics of the previous measurement setup, the equivalent model of one Soft touch's pin was made based on the measured electrical properties presented in product's datasheet [15].

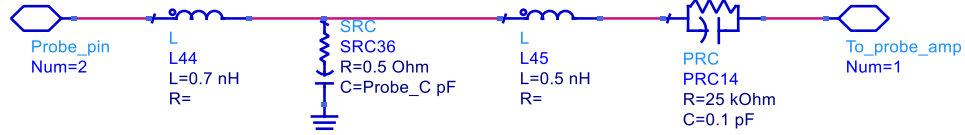


Figure 17 Equivalent circuit for a single probing pin of the Agilent N2887A Soft touch probe head.

Figure 17 presents the single-ended equivalent circuit of the Agilent N2887A Soft touch probe head. The model is based partly on the parasitic properties and the impedance plot, presented in product's datasheet [15] and partly experimentally tuned regarding to the probe's physical structure. At DC, the parasitic inductance and capacitance does not affect to the informed 25 k Ω input impedance of the probe, so there must be a 25 k Ω series resistor. The typical differential input equivalent capacitance was told to be 350 fF, which means that the single-ended equivalent load capacitance should be approximately twice that amount. Inductors L44 and L45 presents the parasitic inductances, caused by the wires and pins of the probe head. The first rough approximation was done by estimating the length of the wires and pins in the probe head and by using the rough rule of thumb – 10 mm of wire causes the inductance of 10 nH [20, p.238]. The fine tuning of the model's unknown parasitic properties was done so, that the simulated input impedance trace matches to the one, presented in the product's datasheet.

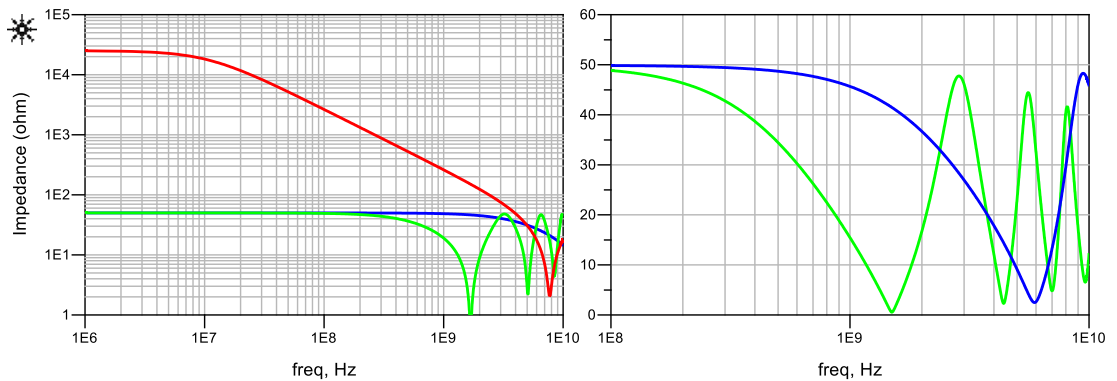


Figure 18 Impedance, seen by the signal source. On the left side, the red trace is the case where only the Agilent N2887A Soft touch probe head would be connected. In the green trace, there would be 21 mm open-ended PWB stub connected in parallel with a 50 Ω load impedance. The blue trace is the same case but with 5 mm open-ended PWB trace. Figure on the right side presents same cases but now the probe head is connected to the end of the mentioned open-ended PWB traces.

Figure 18 shows the simulated input impedance curve of the probe head only. It matches well to the one, presented in the product's datasheet [15]. However, the impedance values are halved, if compared to the differentially measured values. Figure 18 also presents the effect of the open-ended PWB branch, which is combined with the probe head. On the left side, there is just the open-ended PWB branches, simulated at different lengths. On the right side of the Figure 18 there is the same case, but the equivalent circuit of the probe head is connected to the end of the PWB branch. Although the input impedance of

the probe head begins to decrease at higher frequencies, the effect of the added probe head does not change the impedance, seen by the transmitting end by much. The obtained result corresponds well to the theory, explained in the previous chapter.

Some of the older BoB revisions had a direct PWB traces, going from the via between the AP and DRAM IC to the pads of the probing matrix connection, which are located on the sides of the BoB. In the newer models, there are series resistors added next to the LPDDR IC. Resistors were added after finding out that the newer memory models with the higher clock speeds did not operate reliably anymore. Resistors isolate the unterminated PWB trace from the signal source so, that the signal quality remains good enough for the correct operation of the device.

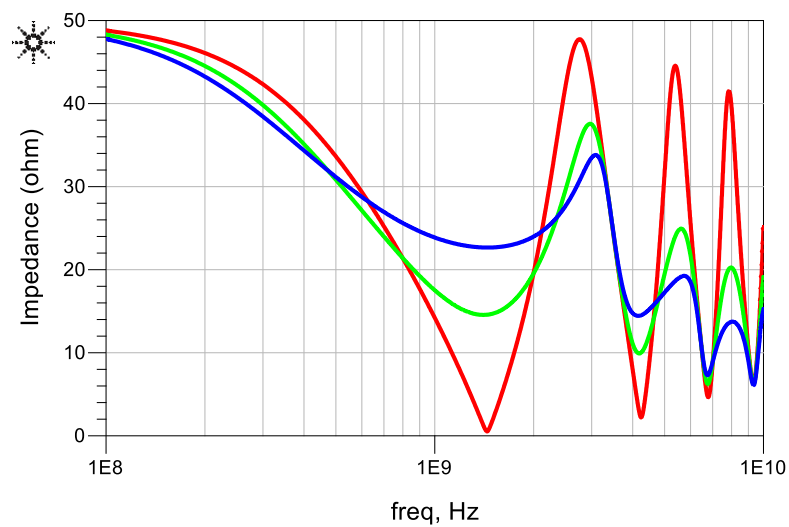


Figure 19 Impedance seen by the signal source when the measurement node includes a 3 mm transmission line, a series resistor and a 18mm transmission line, going from the series resistor to the equivalent circuit of the Soft touch probe head. Red: 0 Ω , green: 22 Ω , blue: 47 Ω

Figure 19 presents the simulated case, where there is a 3 mm PWB trace, going from the AP – DRAM interconnection to the series resistor and a 18 mm PWB trace, going from the series resistor to the measurement pads on the edge of the PWB. As can be seen, the series resistor with a higher resistance maintains the impedance, seen by the signal source, closer to ideal 50 Ω over the frequency range. In contrast, the higher series resistance value degrades the measurement quality.

However, the clock speeds with the latest LPDDR4 memories have increased to the point, where the system did not operate at designed clock speeds anymore even if the series resistors would be desoldered completely. Also, the crosstalk has become a problem lately because the higher frequency components couple more easily on to close by PWB traces.

To inspect the crosstalk performance, the BoB PWB layout was imported into the field-solver simulation software, which finds out the crosstalk parameters between the signal

traces. Based on the earlier experience, there have been a significant differences between the simulated and measured absolute crosstalk values, although the relative values have been in line with each other.

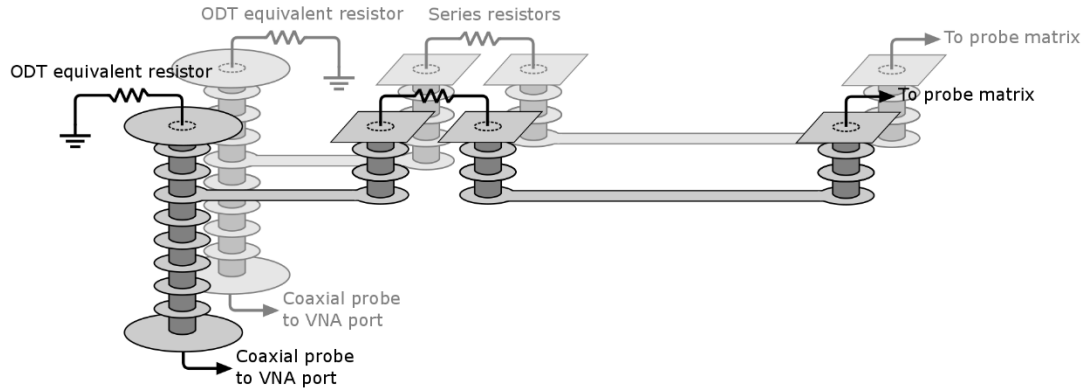


Figure 20 Illustration of the crosstalk measurement setup and the inner construction of the PWB.

Due to the above-mentioned factors, the crosstalk was measured by using a *vector network analyzer* (VNA) and a miniature solder-in coaxial probes, connected to the BGA pads of the PWB. To minimize the crosstalk, caused by the measurement system itself in relation to the crosstalk, caused by the close by PWB traces, the measured signal pair was chosen based on the worst case simulation. Also the equivalent *on-die termination* (ODT) resistors were soldered on the PWB regarding to the Figure 20.

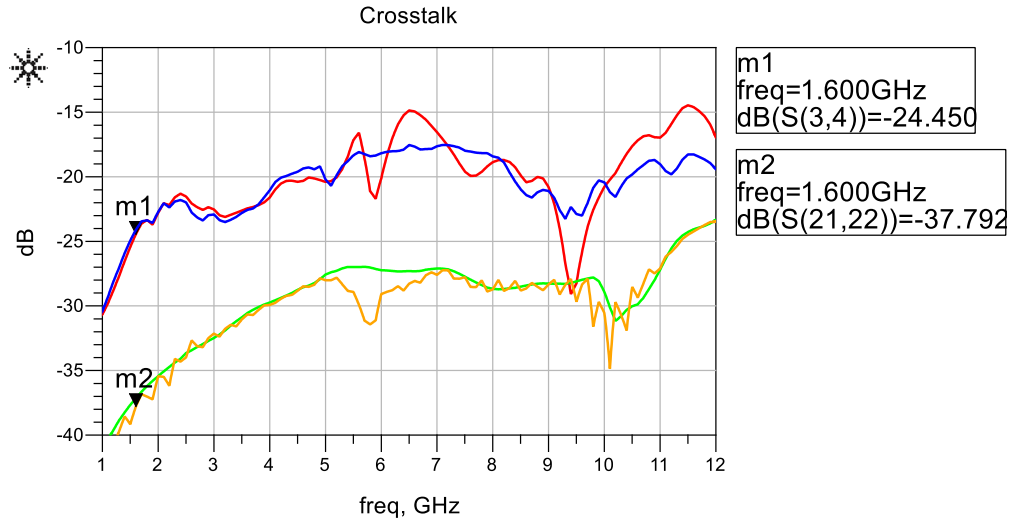


Figure 21 Worst-case crosstalk performance, measured with the VNA. Blue: previous BoB, probing system disconnected. Red: previous BoB, probing system connected. Green: newly designed BoB, probing system disconnected. Orange: newly designed BoB, probing system connected.

The measurement was done with the probe head connected and disconnected. Figure 21 presents the measured crosstalk values from the BoB, designed along this thesis work. For comparison, there is a measurement done from one of the previous LPDDR4 BoB

revisions. Regarding to the VNA measured results and observations during the earlier memory testing measurements, the crosstalk performance of the previous LPDDR4 measurement BoB was quite poor. Figure 21 presents the improvement in worst case crosstalk performance, which is 13.3 dB at 1.6 GHz.

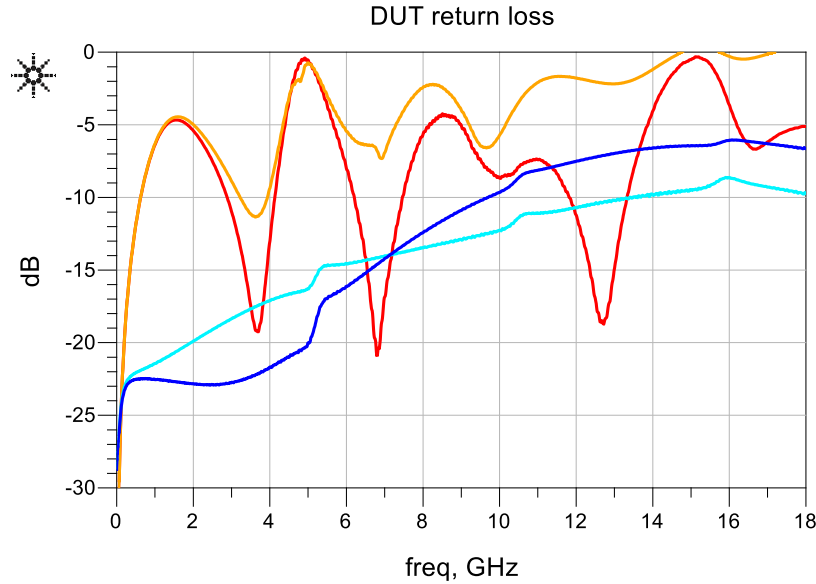


Figure 22 Return loss traces. VNA's port connected to the BGA pad of the mentioned signal sources. Equivalent ODT resistor connected to the BGA pad of the receiving end. Orange: previous system & DRAM transmits. Red: previous system & AP transmits. Cyan: new system & AP transmits. Blue: new system & DRAM transmits.

Using the same VNA measurement setup than with the above mentioned crosstalk measurements, also the improvement in return loss characteristics were inspected. The issue with signal reflections in the previous BoB designs, is clearly visible in Figure 22. The length of the improperly terminated transmission line stub defines the density of notches in frequency domain. Longer, the denser. The plot also explains, why the DUT has become unstable with the latest high speed memories. The return loss of 5 dB at 1.3 GHz would denote that approximately 30 % of the transmitted power would reflect instead of going through the system. The new BoB design does not have that same issue, caused by the open-ended PWB stub, so there is a significant improvement in return loss characteristics. During the measurements, the miniature solder-in coaxial probe measurement technique was also noted to be relatively inaccurate in higher than approximately 5 GHz frequencies.

In conclusion, most of the upgrades over the previous measurement system was done into BoB design and to the probing matrix, connected to the BoB. The RF performance of the other components in the system were already at good level. The existing computer controlled switch matrix is built by using a high grade *radio frequency* (RF) relays with an 18 GHz BW [21], and the performance characteristics of them does not limit the measurement quality significantly with current memory clock rates, nor the clock rates

that are expected in the near future with LPDDR5 memories. Also, the oscilloscope's 16 GHz analog BW and 40 GSa/s sample rate from four channels simultaneously [9] is good enough for the LPDDR4 and LPDDR5 measurements.

4. DESIGN IMPROVEMENTS

Based on the previously made research about the predecessor measurement system, there were areas, which have worked well and should not be modified, and areas which need upgrades to allow the higher measurement BW, needed by the LPDDR4 memories. This chapter presents the design improvements made over the previous system.

4.1 Signal integrity and timing measurement BoB

As stated in the previous chapter, the electrical performance of the system was limited notably by the combination of the effectively open-ended PWB stub and the Agilent N2887A probe head. Even though it would have been possible to terminate the PWB stub which goes from the probing point to the pads of the probing matrix, the limits of the Soft touch based probing system were already reached in terms of electrical performance.

Since the whole switch matrix system already had a characteristic impedance of $50\ \Omega$, the apparent choice was to extend the $50\ \Omega$ transmission line as close to the probing point as possible. To not to attenuate the signal between the AP and the DRAM IC considerably, the power division must be done so that the probing system loads the DUT as marginally as possible. Still, the signal should be strong enough at the oscilloscope's end to achieve measurement results with an acceptable SNR.

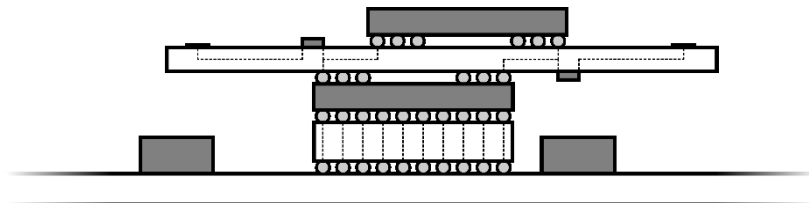


Figure 23 Cross section view of the newly designed memory testing system interposer stack.

The previous BoB design, presented in Figure 15, minimizes the length between the AP and the LPDDR IC, and the length of the extra branch to the SMD resistors is electrically quite long. Microsoft's previous internal research have shown that the previous design topology began to cause SI issues with the high-end LPDDR4 memories because of the earlier mentioned reflections, caused by the extra PWB branch. One option would have been to place a very small, 01005 sized SMD resistors between the PWB and the IC. However, resistors with the length of 0.01" and the width of 0.005" would have been quite unpractical in terms of rework and soldering. The new design, presented in Figure 23, increases the length between the AP and the LPDDR memory IC marginally, but the additional length is not a problem because the transmission line is always terminated from the receivers end, so the extra length will not increase the reflections significantly. The

new design also allows the usage of a 0201 sized resistor, which can be hand-soldered with relative ease. In the new design, the extra stub from the signal trace, between the AP and the LPDDR IC, to the series resistor has only the length of the via stack, which is approximately 0.5 mm. Also the usage of embedded resistors was investigated but the size and the high manufacturing price opted them out.

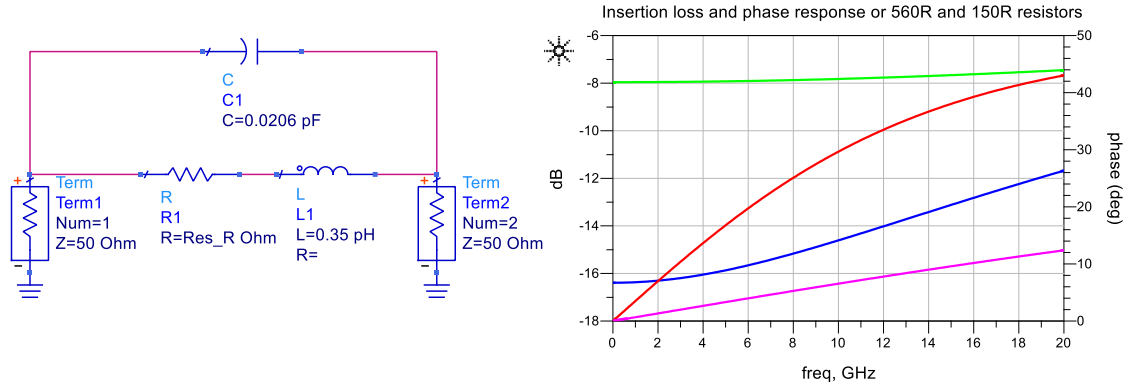


Figure 24 Simulation of a 0201 sized SMD resistor with the parasitic components included. Blue trace presents the insertion loss of a 560 Ω resistor and the red trace is the phase response of that. The green trace is the insertion loss for a 150 Ω resistor and the magenta trace is the corresponding phase response.

The physical size of the resistor also affects the system's performance. Typically small resistors are more ideal. Regarding to Vishay's research [22], the parasitic properties of the 0201 SMD resistors are already at relatively good level. As the parasitic properties of the resistors are mainly caused by the physical dimensions and the construction style, the values for the simulated 560 Ω and 150 Ω resistors were taken directly from the Vishay's technical note. There are small variations between the products of different manufacturers and the different resistor series, but the parasitic values were tested and there was no significant difference observed in the measured waveforms, if the value of the parasitic capacitance or inductance was changed slightly to a greater or a smaller value in the post-processing function, which will be described more in depth in the next chapter. The effect of the resistor's series inductance in the waveform data, was unobservable small, but the effect of the 560 Ω resistor's 20.6 fF parasitic capacitance was seen in the measured waveforms when the parasitic properties of the resistor was included into the post-processing function. The simulation, presented in Figure 24, also shows that the 120 Ω resistor appears to be more ideal over the frequency range. This is because the resistive component is more dominant in relation to the parasitic components, if compared to the 560 Ω resistor.

As stated in the previous chapter, the long, unterminated branch of the transmission line will cause notable reflections in high BW applications. Generally, the transmission line is perceived as electrically long if the signal propagates from its source to the end of the transmission line and reflects back to the source faster than the signals transition time. In a electrically short, unterminated transmission line, the possible effects caused by the

signal reflection is nominated by the rising or falling edge of the signal. The generally used rule of thumb is that if the propagation delay of the transmission line is longer than $1/6^{\text{th}}$ of the signals transition time, a termination is needed. [23]

$$l = \frac{t \cdot VF \cdot c}{6} \quad (9)$$

According to Formula 9, the application with the transition time of 100 ps and VF of 0.5 would need a termination if the length of the transmission line is longer than 2.5 mm. Although if the interconnections between the two PoP stacked CSP's are shorter than that, the bond wires in the CSP packages increase the total length from IC's die to die well over the calculated length, and a termination is needed.

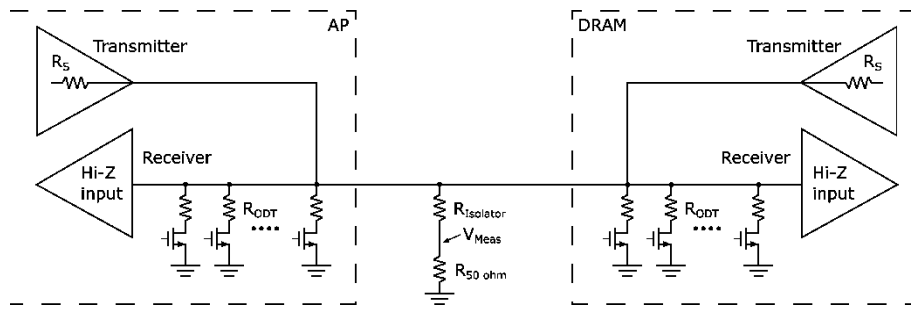


Figure 25 Illustration about the total impedance, formed by the parallel connection of the ODT and the measurement node.

Typically the termination point of the transmission line is placed physically as close to the end of the transmission line as possible to minimize reflections. In LPDDR4 memories, the termination is implemented on the silicon chip. As the Figure 25 presents, the impedance of the ODT can be set in discrete steps by switching the transistors accordingly. Active logic also allows the ODT to be turned off on the transmitting end, so it does not attenuate the signal unnecessarily. By modifying the software defined parameters, the ODT impedance can be set to match the transmission line's impedance as closely, as the discrete impedance steps allows. [2]

Figure 25 shows also the obligatory drawback of the measurement system. The series connection of the resistor on the PWB and the oscilloscope's 50Ω input impedance is connected in parallel with the ODT impedance of the receiving IC. When using the measurement system for finding the best possible ODT value, the effect of the parallel connected measurement branch must be taken into account. A high series resistance in the measurement node reduces the effect of the measurement setup but the tradeoff must be done so that the series resistance is still low enough to achieve an adequate SNR.

The previously used Agilent Soft touch probing system was very good in terms of usability because the spring loaded probing heads took a direct contact to the pads on the PWB without soldering required. To maintain the fast and easy connectivity, the probing matrix was replaced with a multi-positioned RF connector with the characteristic

impedance of 50 Ω . However, the only option found, which met the demanding requirements in terms of electrical performance, size, amount of positions and availability, had some disadvantages that needed mechanical modifications, which are presented more in depth in chapter 6.

To inspect the timing attributes reliably between two or more signals, the PWB traces in the BoB needs to be length matched, so the measured timing skew is exactly the same as it is between the AP and the DRAM IC. The previous BoB's have had every trace length matched with each other. This increases the crosstalk because there is no space to add ground fills between every signal, due to the large length matching structures. On the new design, the length matching is divided into three groups so, that every signal which goes to the same oscilloscope channel, through the switch matrix, is lengthened similarly. This way, the signal mapping to the connector's positions can be arranged to allow reasonably sized length matching structures and good SI properties in the PWB layout. Because of the difference in propagation delay between the length matching groups, the timing skew is compensated in the digital post-processing of the measurement data.

Based on the previous research [4, p.74], also the concept design about the completely new switch matrix was investigated during this master's thesis. It would have been implemented by using the *microelectromechanical systems* (MEMS) switches. This would have allowed shorter coaxial cables than the separate rack-mounted switch units. However, the crosstalk would have been a problem with the MEMS switches because they are physically small, and the isolation between the two signal paths would not have been sufficient enough for this kind of measurement setup and performance requirements. The system's performance was estimated also with the GaAs transistor switches, which would have allowed a very good crosstalk performance, but the GaAs switches, with the electrical performance high enough, were very costly and the attenuation was not low enough for this application. Also, most of the MEMS or the transistor based switches had a *single-pole double-throw* (SPDT) topology, so for example, multiplexing eight signals would have needed seven switch components, while the rack-mounted switching units with multiple *single-pole six-throw* (SP6T) Narda RF relays [21] are able to multiplex six signals with one relay component. So in the end, the rack-mounted switches with good quality cables still offers the best performance without the extra effort of designing and implementing a completely new switching system and its control software.

The temperature tolerance of the system is one important aspect. All parts, close to the interposer construction, should tolerate a wide range of operating temperatures, because the DUT will be tested in different operating conditions in a temperature controlled chamber. This basically prevents the usage of active components, like signal amplifiers, close to the DUT, because the electrical characteristics of them typically depend significantly on the operating temperature [5]. Also the electrical characteristics of the passive components varies over the temperature range, but the variation in the cables, connectors or SMD resistor's characteristics is insignificant in terms of this application.

The SI verification process of the LPDDR IC includes many different measurements. Previously, the same BoB has been used for the SI measurements and also every voltage rail had its own shunt resistor for the current consumption measurements. Both of the mentioned measurements have their own requirements. Current measurements do not need information about the data bytes but only if there is data traffic ongoing or not. The current consumption measurement board should operate at the maximum clock speeds, so the current reading corresponds to realistic use cases. Signal integrity measurements do not necessarily need all the signals to be routed out because part of them are very close to identical with each other, and only one of them needs to be measured. Also, the SI measurements should run at full clock speeds to inspect the eye diagrams and waveforms in most critical scenarios in terms of timing and SI. Of course, soldering two separate boards for the SI and the current consumption measurements needs more effort and resources, but at this point, it seems like a good compromise to be done.

The eye diagram measurements and simulations are an important and very useful way to inspect the system's response to the periodic, arbitrary data signals. The simulated transmitter sends, for example, LFSR randomized data values to the signal path, and the receiver plots them on top of each other with color grading and infinite persistence. The eye-shaped area between the transitions should not have any overlapping traces because then the data might be read incorrectly. The minimum acceptable width and height of the eye-pattern is also specified for the receiver IC.

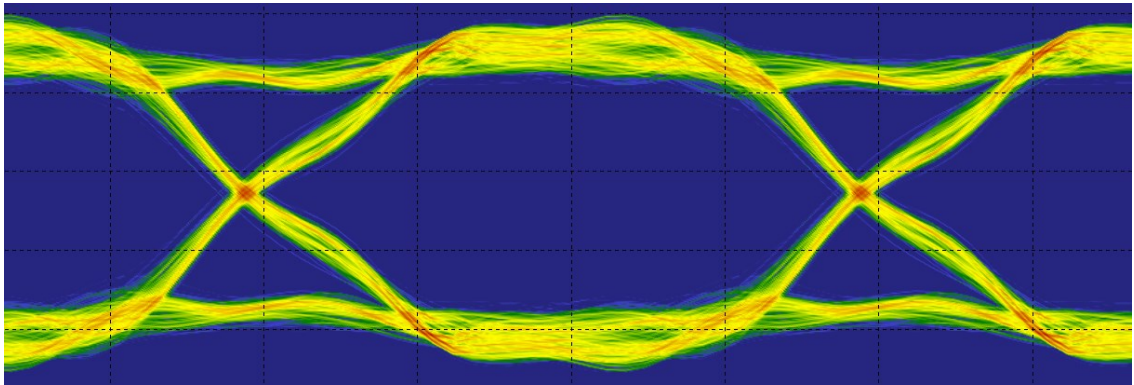


Figure 26 *An eye diagram seen by the DRAM in a simulated, unmodified PoP stack when the AP transmits.*

Figure 26 presents the simulated ideal case where the AP and DRAM are connected directly to each other without the interposer stack or the measurement system attached. The shape of the eye diagram varies depending on the pin and software configurable transceiver parameters but it does not matter in this case, as long as, every comparable simulation uses the same pin and transceiver settings. When the interposer stack is included into simulation, ideally, the IC's received eye diagram, should not change from the ideal simulation case, and also the eye diagram, seen by the measurement instrument, should look similar. If the received and measured signal would look similar to ideal simulation without the interposer stack attached, it would mean that the measurement

system is totally invisible to the DUT and the signal would not be distorted between the DUT and the oscilloscope. However, this kind of measurement system is practically impossible to implement because there must be at least a power division between the DUT and the measurement node, which affects to the amplitude of the waveform. If only a small fraction of the power is captured to the measurement node, the amplitude degradation will be insignificant.

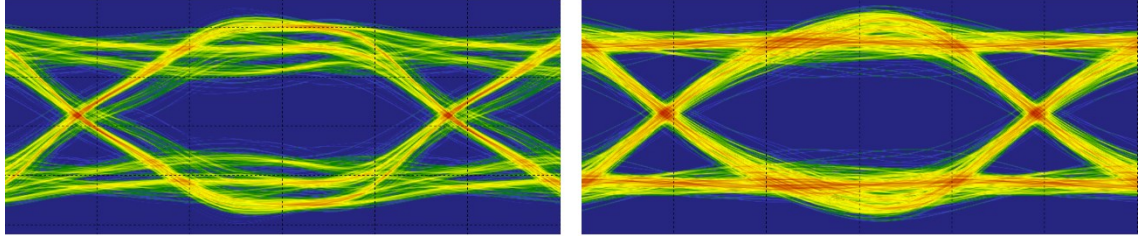


Figure 27 A simulation of the previous measurement system with the Soft touch probe head connected. Left: the eye diagram observed by the DRAM IC when the AP transmits. Right: Same setup, the eye diagram seen by the oscilloscope.

Figure 27 presents the simulated case with the previous measurement system connected. As stated, the practically open-ended PWB stub distorts the signal quite much between the AP and DRAM. Also the waveform in the oscilloscope's end looks closer to a sine wave because the system's BW is not enough for capturing the highest frequency components when the DUT is operating at maximum 3.2 Gb/s data rates.

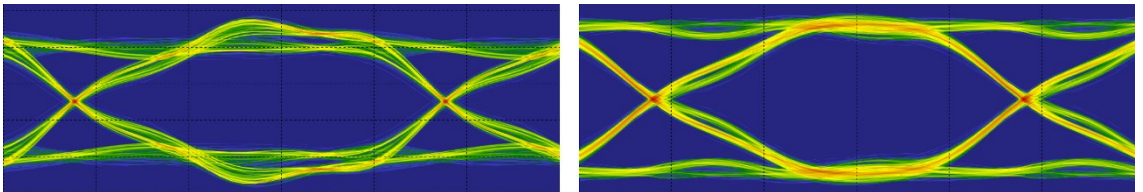


Figure 28 A simulation of the new measurement system with the connector matrix connected. Left: the eye diagram observed by the DRAM IC. Right: same setup, the eye diagram seen by the oscilloscope when the AP transmits.

The same simulation was done with the simulation model of the new system. As can be observed from the Figure 28, the eye diagram does not look exactly similar to the ideal reference simulation, without the interposer attached, but the eye-pattern seen by the DRAM has not shrunk much because of the interposer stack. Also, the measured eye-pattern does not differ significantly from the ideal case. Of course, long coaxial cables and the switch setup attenuates high frequency components more, so the transition appears to be slightly slower with the new measurement setup, if compared to the ideal simulation case. All in all, the eye diagrams of the newly designed system seems good, and the minor distortion and transition speed degradation, caused by the measurement setup, can be mostly compensated in post-processing, which is explained in the next chapter.

4.2 Current consumption measurement BoB

The current consumption of the DRAM IC varies significantly depending on the amount of data traffic and the used clock speed. To allow the best possible SI in the signal traces, they are routed directly from the top side BGA pads to the bottom side of the PWB. There is only a microvia stack between the two BGA pads. However, the current consumption measurement requires an information about the memory's activity. By placing a direct PWB branch, which would go from the clock or the data strobe trace to the probing point, would impair the SI, and possibly cause stability issues at the highest clock frequencies. To get the current consumption measurement results with respect to the amount of data transfers and active memory channels, the setup still needs those probing points for activity monitoring.

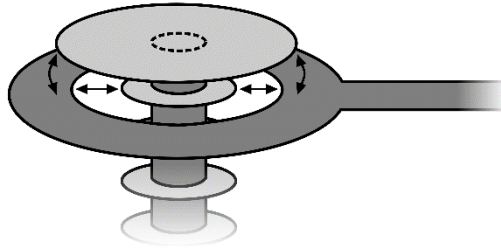


Figure 29 A BGA pad and a microvia stack which connects it to the corresponding BGA pad through the PWB. The ring-shaped trace acts a coupler which takes a very minor part of the signal to the test pad to identify if there is a data transfer going on or not.

The crosstalk is typically unwanted property between the two PWB traces but this newly designed testing technique makes use of it. By placing a ring shaped PWB trace under the BGA pad, a very small fraction of the high speed signal couples to it because of the common capacitance between the two copper traces. The ring shaped coupler trace, presented in Figure 29, is connected to a test pad, which can be measured with an oscilloscope.

The most significant concern in terms of the PWB coupler was that the PWB manufacturer's design rules set the limits for the minimum allowed clearance between the two copper areas in the PWB. The BGA pad of the DRAM IC is very small, so the size of the coupler ring is also very limited. The coupler trace does not overlap the area of the BGA pad by much, so the amount of common capacitance is very minimal. The top tier PWB manufacturers allows a very small clearances but the effect of the tolerances cannot be overlooked because they are relatively wide if compared to the minimum clearance values. Because of the manufacturing tolerances, the coupling ratio of the PWB coupler can vary significantly depending on the manufacturing process. The variation

does not matter in this application, as long as the PWB, made with the worst case manufacturing process produces the signal with a measurable amplitude.

The PWB coupler was simulated in the 3D field-solver simulator tool. The results are presented in Figure 30. Many different factors affect to the coupling ratio. The presented worst case simulations are done by reducing and increasing the distance between the copper traces and changing the Dk value of the PWB dielectric material according to the tolerance values, specified by the PWB manufacturer. Based on the simulation, the measured amplitude should be dozens of millivolts, which is enough for a reliable signal

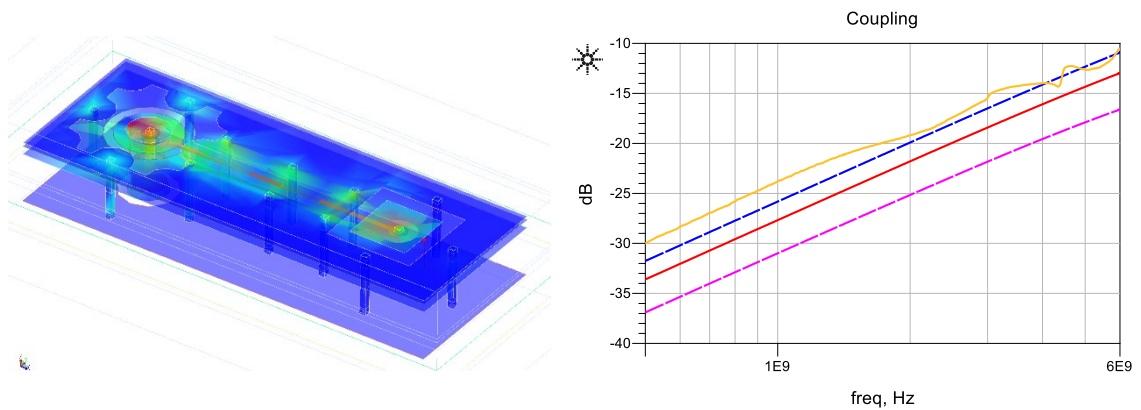


Figure 30 A 3D field-solver coupling simulation from the BGA pad to the coupler trace, which goes to the test pad. Traces on the right side present the coupling between the BGA pad and test pad. The red trace is a simulated value. The blue and magenta traces present the simulated worst case tolerances and the orange trace is a VNA measured result.

presence detection. The VNA measured coupling ratio seems to be a bit higher than the simulated best case. The slight differences between the simulated and measured results can be caused by the probing technique. A fraction of the signal's power passes through the air, directly from the tip of the VNA's coaxial probe to another. Also the ground path between the two coaxial, solder-in probes have an effect to the coupling value.

For example, an isolation of 28 dB would mean that about $1/25^{\text{th}}$ of the original signal's voltage would be measured from the test pad. This would be enough to be measurable with an oscilloscope. By setting the oscilloscope to peak-detect mode, the measured signal shows the envelope curve of the clock and data strobe signals along the current consumption [24].

5. POST-PROCESSING

Although the system is designed to perform as well as possible in the electrical sense, there are always non-idealities which will impair the measurement results. Especially in the high BW measurements, the probe and cables can distort the measured signal significantly. For that reason, some of the high-end oscilloscopes include a post-processing function, also called de-embedding. It can compensate the distorting effect of the test fixtures and other unwanted parasitic properties, caused by the testing system. This chapter introduces the de-embedding function, used to fine-tune the performance of the presented LPDDR4 measurement system.

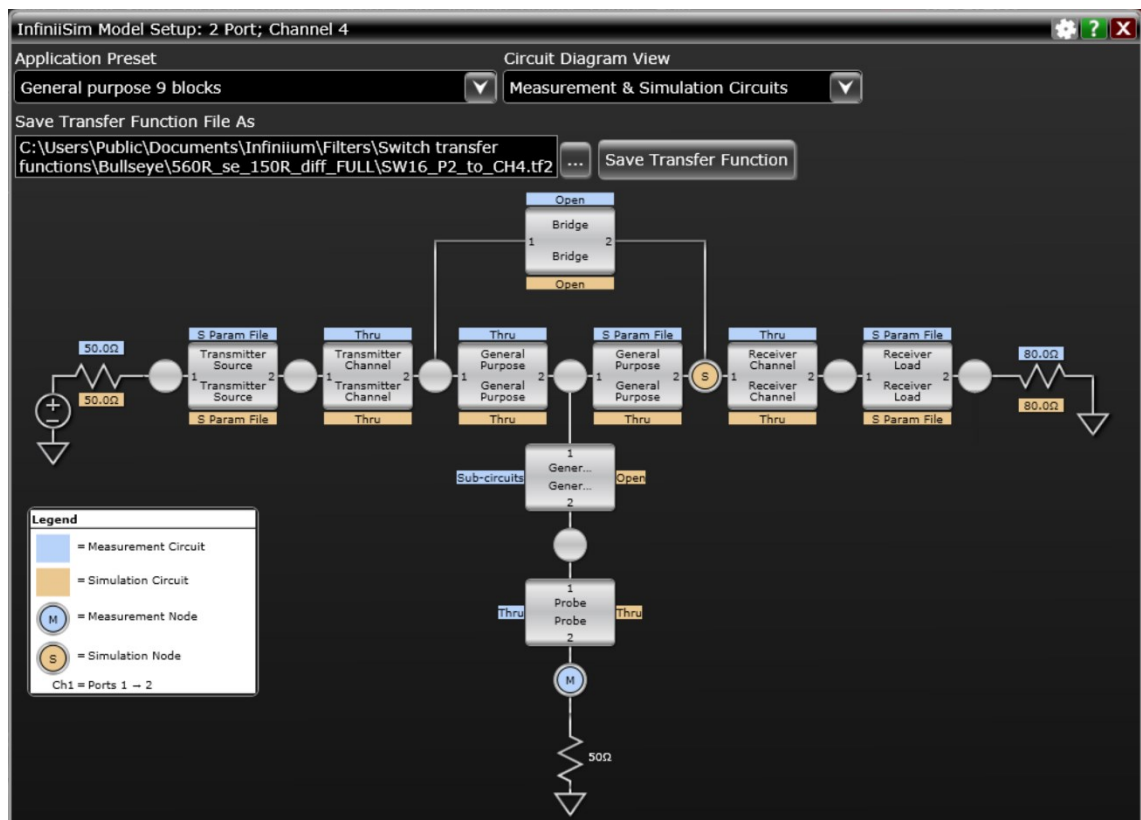


Figure 31 A view from the Keysight's InfiniiSim software, which generates the transfer function from S-parameters and other circuit blocks.

In addition to fine-tuning of the electrical performance, also the cost reduction is one important factor. For example the cable's loss or length variation can be compensated in the post processing, so there is no need to invest into the highest grade RF switches and cables with very strict length matching requirements and negligible attenuation over the utilized frequency BW. Of course, it should be always kept in mind that the de-embedding cannot compensate everything, so the electrical properties of the system should be already at a very good level, and the post-processing is meant only for fine-tuning.

For example, in the LPDDR4 measurements, the edge of the clock and the data signal have a strictly defined timing window, when the transition of the data signal should occur in relation to the clock signal to meet the specification and provide the device's reliable operation. To be able to measure the timing skew accurately enough, the signal paths of the clock and the data should have electrically equal lengths, as electricity has a finite propagation speed. In practice, most of the cables can be non-matched relative to each other because the compensation of the timing skew can be done in the de-embedding function. Differential pairs are the only exception, which must be length matched very precisely, because the positive and negative half of the signal cannot be de-embedded separately in this case.

Keysight's InfiniiSim software applies the de-embedding function to the measured waveforms at real-time. As Figure 31 presents, de-embedding uses the transfer function, which can be built by using S-parameters, RLC circuits, transmission lines and other circuit blocks [25]. S-parameter models can be measured with a VNA or they can be simulated. For example, the cables and switch matrix can be measured easily and accurately with the VNA because the coaxial connectors of the system can be connected directly to the terminals of the VNA. However, attaching the miniature solder-in probes to the BGA pads on the PWB would be challenging and very time consuming. Also the effect of the probes could distort the measurement results significantly with such small objects.

Previously, the BoB PWB was not included into the de-embedding function because the effect of it was negligible in the frequency range of interest. With LPDDR4 memories, also the PWB must be included into the de-embedding model to achieve good measurement results. Both, the measured and simulated S-parameter files for the BoB PWB were tested, but the simulated results appeared to be better, as predicted.

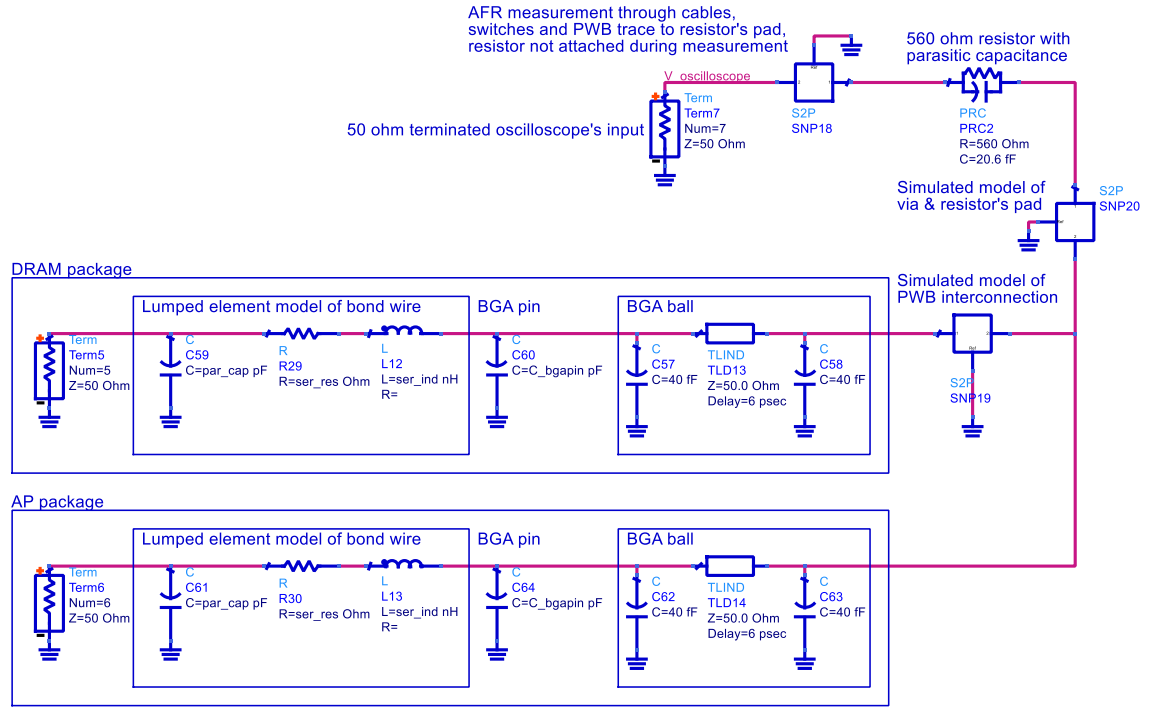


Figure 32 The electrical model of the measurement system, used in the de-embedding function.

To compensate the reflections, caused by the PWB trace between the AP and DRAM correctly at high frequencies, also the electrical characteristics of the IC's had to be modelled. The automated testing system is meant to operate correctly with various different products, so one absolutely correct electrical model, which would correlate to every memory IC, does not exist. The equivalent circuit for the IC package, shown in Figure 32, was done by taking the values of the parasitic properties from the *Input / Output Buffer Information Specification* (IBIS) models, offered by the IC manufacturers. The parasitic component values vary slightly depending on the IC, or the IC's pin, but at this frequency range, the general average model was found out to be accurate enough to provide the necessary de-embedding function. The IBIS models are explained more in-depth in the next chapter.

$$A_{DCdB} = 20 \cdot \log_{10} \left(1 + \frac{R_{isol}}{R_{term}} \right) \quad (10)$$

The new BoB design attenuates the signal, which goes to the measurement node relatively much if compared to the previous measurement system. The previous version had the Agilent Soft touch probe head with a high input impedance, while the input impedance of the newly designed system is formed by the oscilloscopes 50 Ω input impedance, which is connected in series with the SMD resistor on the BoB PWB. The attenuation of the described voltage divider can be calculated at DC by using the Formula 10.

At DC, the reactance of the transmission lines and components does not affect to attenuation, so it can be calculated by using the resistive component only. By applying $50\ \Omega\ R_{term}$ and $560\ \Omega\ R_{isol}$ to Formula 10 the attenuation is approximately 21.7 dB, which means that the measured voltage values are about 8 % of the true voltage values between the AP and DRAM. The attenuation over the frequency range of interest can be inspected with the S-parameter simulation setup, described in Figure 32.

Both ends of the frequency range can cause issues in de-embedding. The InfiniiSim tool defines the DC gain of the system by using the data point with lowest frequency, specified in the S-parameter files [25]. The S-parameters are typically obtained by using the VNA, which minimum starting frequencies are generally far from DC. Depending on the system, the DC gain might need to be measured separately and added manually to the S-parameter files. Also the high frequencies can cause issues because the effect of the measurement fixture or VNA's calibration can cause significant amount of measurement error. If the S-parameters are obtained by using simulation tools, small differences between the simulation parameters and real-world material properties, can cause significant differences at high frequencies. For example the permittivity of the PWB material can vary depending on multiple different factors. For that reason, it is not beneficial trying to de-embed frequencies that are outside from the frequency range of interest. It can cause extra noise and ringing to the measurement results.

6. PROTOTYPING

From theory to real product – the design process started by defining the specifications and requirements, which the system should meet. The interposer design introduced some new techniques, so the first revision was one kind of proof of concept design, which should perform well with current memories, but might still need some fine-tuning before implementing following BoB's with the same technique for the different memories in the future.

After characterizing the lately observed problems with the previous measurement system, the BoB design was implemented in schematic level. Before starting the layout routing, the schematic level design was simulated by using transmission line schematic components. Schematic level simulations gave a good estimation about the system's final performance.

Simulations were done mainly as frequency domain S-parameter simulations because they give a fast overall view about the system's performance. Also iterating and testing was fast. However, S-parameter models with ideal $50\ \Omega$ source and load impedances does not tell the whole truth about the behavior of the system. To inspect the system's performance more in-depth, the properties of transmitting and receiving IC needs to be understood better. Also the parasitic attributes of the package and software configured drive strength and ODT impedance affect to the waveform of the signal significantly.

Creating an accurate equivalent model for the high-speed IC pin would need quite much effort. That is why most of the manufacturers offer IBIS models, which are done by using simulated, measured, or both results combined to create an accurate equivalent model for the IC's pin. The model itself does not include all the manufacturer's confidential information about IC's inner operation, but the properties are included into standardized equivalent circuit model, which includes all the major factors that have an effect to the SI properties of the IC's pin.

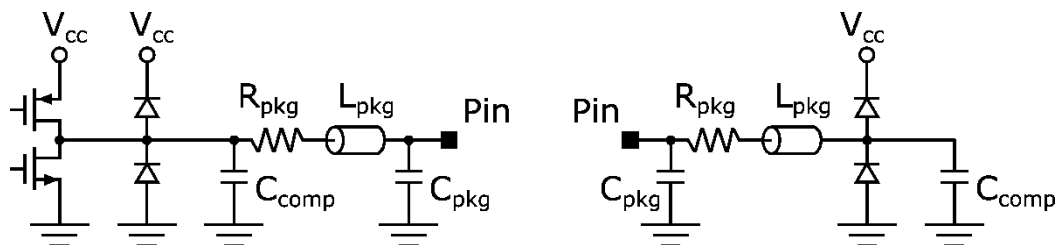


Figure 33 Transmitter and receiver IBIS equivalent circuits.

Figure 33 presents the IBIS model equivalent circuits for the transmitting and receiving IC's pins. The model includes the parasitic capacitance, inductance and resistance caused

by the IC's pin and bond wires, the parasitic capacitance caused by the silicon die, ESD clamping diodes and transistors in push-pull configuration. More of that, the model includes V/I characteristics, which are caused by the clamping diodes and pull-up or pull-down structures. Switching characteristics of the transistors are defined in $\Delta V/\Delta t$ information for rising and falling waveforms. [26]

Before designing the PWB by using chosen connector arrays, the sample order was placed to verify the electrical performance characteristics, and to get the accurate electrical model for the connector matrix. Mechanical modifications were also much easier to plan when there was already a real connector assembly available instead of just the datasheet of it.

After exploring the best achievable transmission line parameters in the schematic level, the layout of the 10-layer HDI PWBs was routed. Later, the routed design was imported into the 3D field-solver simulator tool, which estimates more accurately the reflections caused by the impedance mismatches. Also the crosstalk characteristics were simulated at this point, when the physical construction of the PWB was known. Because the schematic was already simulated extensively, there were only minor changes needed after the layout work was done.

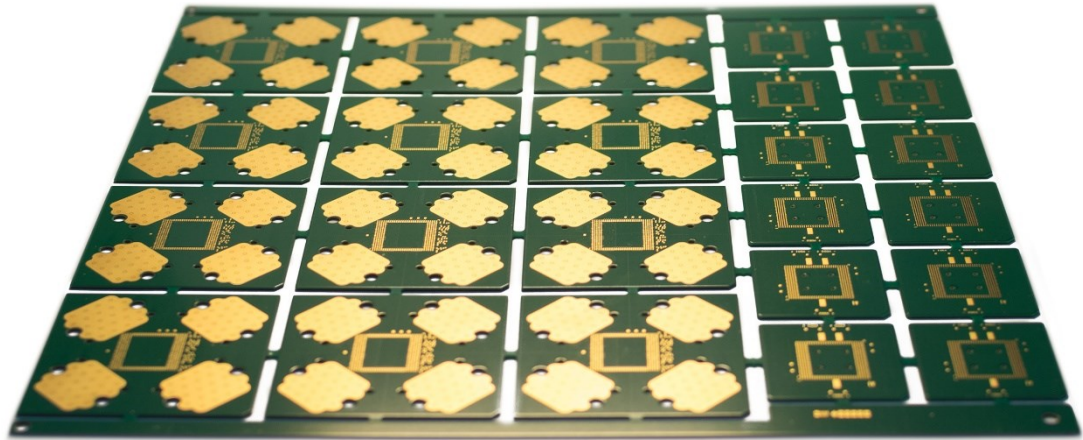


Figure 34 View of the panelized BoB designs

The final estimation about system's performance was done by combining the IBIS models, simulated BoB model, and the measured models of the existing cables and RF switches. After everything seemed fine, the PWBs were panelized and sent to the manufacturer. The finished PWB panel is presented in Figure 34.

6.1 Probing system

As declared, the old testing system with the Agilent Soft touch probe heads was very good in terms of usability because the probe head was easy to mount on the PWB, and multi-positioned probe heads allowed to measure the whole system with the small effort. Considering the new system, an off-the-shelf connector matrix solution would be the easiest and cheapest option. The connector should have enough cable positions and at least couple of extra positions reserved for the future. The physical size of the connector matrix should be small so there would not be significant length differences in routing between the closest and furthest connector's positions. Although the PWB routing is divided into three length matching groups to relieve this issue, it would be beneficial to have as similarly lengthened PWB traces as possible.

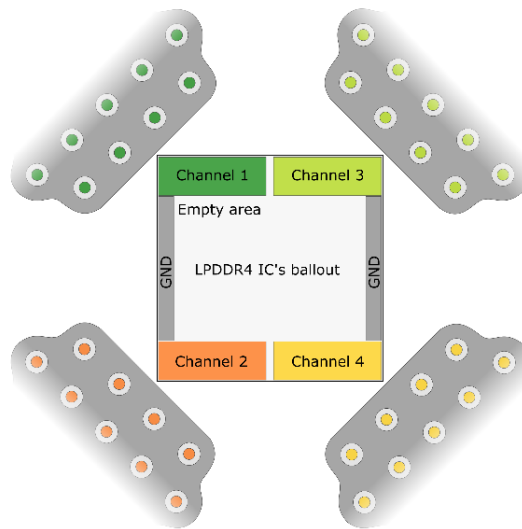


Figure 35 General view of the LPDDR4 memory IC's pinout topology, which allows the symmetrical signal grouping to the connector matrices.

The reduced amount of the traced signals also decreased the amount of needed cable positions. Three Samtec Bull's Eye BAR connector matrixes [27] would have been enough for probing all needed signals. However, the ballouts of the LPDDR4 memories are arranged so that there are four, almost identical areas for each channel, as Figure 35 illustrates. To keep all the PWB trace lengths as short and similar to each other as possible, four connector matrixes were used instead of three. This allowed the symmetrical design, and all the needed cable positions were arranged to the edge of the connector, closest to the DRAM IC.

After the suitable successor alternative for the Agilent Soft touch probing system was found, the sample order was placed, and the performance characteristics of the Samtec Bull's Eye BAR connector matrix and compatible cables was verified.

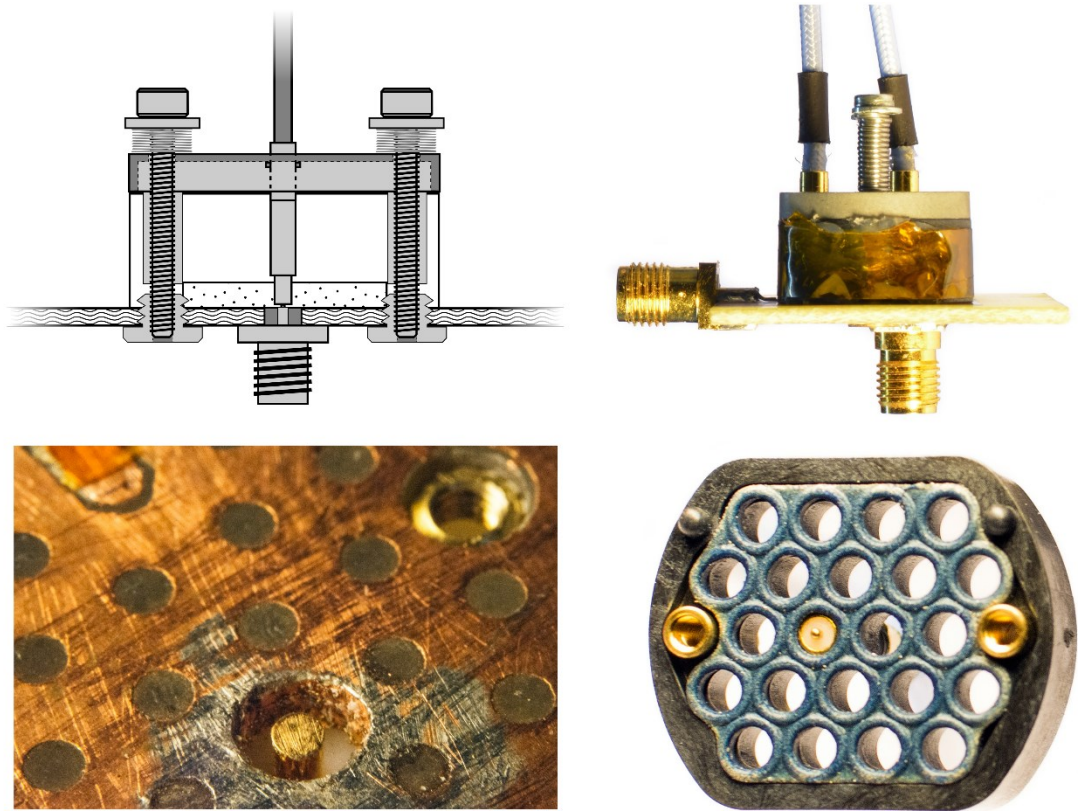


Figure 36 Designed and built performance and mechanical feasibility testing board for the Bull's Eye BAR connector matrix.

As the Samtec Bull's Eye BAR connector matrix itself does not have any counterpiece other than the PWB footprint, the testing setup needed a simple PWB, which has a footprint for the Bull's Eye connector matrix and *SubMiniature version A* (SMA) connector, which is connected to Bull's Eye connector's pin. The hand-etched PWB probably would not have as good electrical performance as the final BoB design, but at least it gives a good worst-case approximation of performance of the connector system. Figure 36 shows the testing board with the SMA connector, plated GND hole and the SMA connector's center tap, which acts as a SMD pad for the Bull's Eye RF25S coaxial cables, inserted into the Bull's Eye BAR connector matrix.

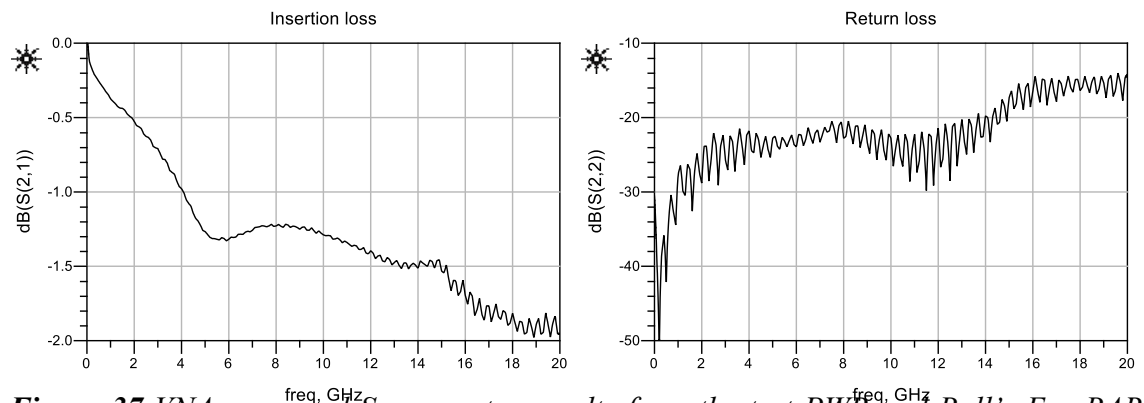


Figure 37 VNA measured S-parameter results from the test PWB and Bull's Eye BAR connector matrix.

Now, the setup had one SMA connector on the PWB and another one at the end of the coaxial cable. The return loss and attenuation was measured with the 2-port VNA. Figure 37 presents the return loss, better than -20 dB up to 12 GHz. The attenuation was also very acceptable in the frequency range of the interest. One important factor in this kind of spring loaded connections is, how the slight mechanical stress affects to the quality of the connection. The cables needed quite radical wiggle until the simultaneously measured S-parameters varied notably. So also the tolerance for the mechanical disturbances was good. The results were promising, so the decision in favor of using this connector matrix was made.

6.2 Mechanical considerations

The ideal solution would have been to find an off-the-shelf 50 Ω connector matrix with needed dimensions, number of positions and the mounting mechanism requirements. After exploring various options, Samtec Bull's Eye BAR connector system was chosen, even though, the connector matrix was not directly compatible to this measurement system, and couple of modifications had to be done.

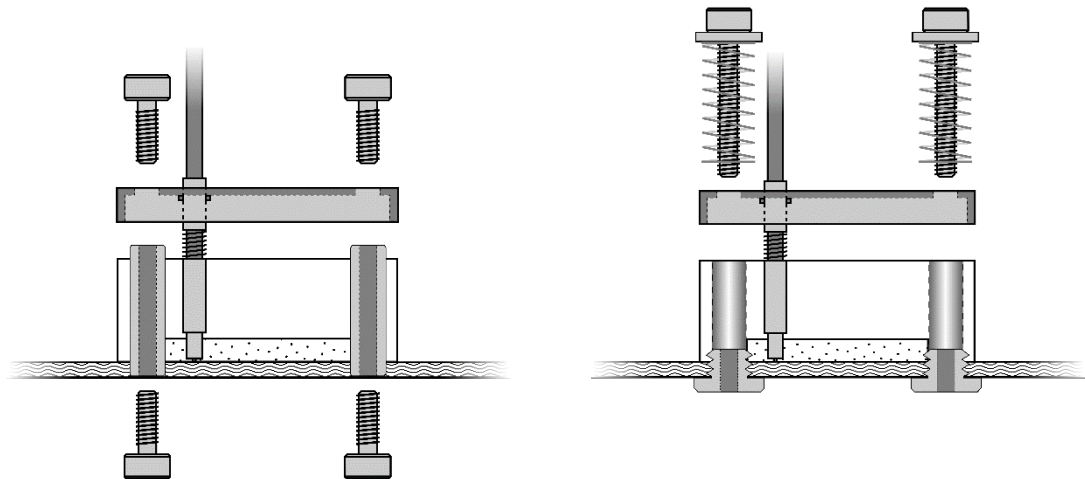


Figure 38 Left side presents the cross section of the unmodified Bull's Eye BAR connector matrix. The right side includes the implemented modifications to it.

The first issue was that originally the connector matrix had double sided mounting screws, as the Figure 38 illustrates. Two of the screws keeps the top plate attached to the connector's body and another two should be screwed from the bottom side of the PWB to the connector's body. These would keep the connector matrix firmly attached to the PWB. However, because the gap between the mainboard and BoB is only couple of millimeters, as can be seen from Figure 23, it is not possible to attach the screws from BoB's bottom side after the interposer stack is reflow soldered to the mainboard.

To allow top-side mounting of the Bull's Eye BAR connector matrix, two separate screws were replaced with the one long screw, which goes through the top plate, connector's

body and the PWB. Bull's Eye BAR connector matrix needs quite significant clamping force to make secure connections. A PWB with a threaded holes was considered but the strength of the 0.7 mm thick PWB material would not have been enough for securing the properly tightened screws. Low-profiled, threaded inserts, which were tested with the above-mentioned hand-made testing board, solved the issue. The final construction of the Bull's Eye BAR connector's mounting mechanism is presented in the Figure 38.

As mentioned, the connector matrix were placed as close to the actual probing point as possible to keep the PWB traces as short as possible. At high frequencies, every millimeter counts, so the connector matrices outer plastic was engraved to allow the connector matrix to overlap the SMD resistors and the corner of LPDDR IC slightly. Only the plastic parts were modified to make sure that the electrical performance of the connector array does not degrade because of the modifications. Although implementing the presented solution requires moderate effort but the modifications have to be done only once at the beginning, so the total amount of work required is still reasonable.

6.3 Board on Board design

In manufacturing point of view, the tooling expenses of the 10-layer HDI PWB's are very high. For that reason, both BoB designs were placed to the same PWB panel and manufactured simultaneously. The PWB stackup was built completely in favor of SI measurement BoB, because the best possible SI in it was the main goal, and the BoB for the current consumption measurements would perform well enough with less ideal PWB stackup.

All the signal traces in the PWB were matched to 50 Ω characteristic impedance to minimize the reflections caused by the impedance discontinuities. As stated, the electrical performance could be improved a bit by using dielectric materials with a low Dk value. However, based on the simulations, the difference between the *flame resistant PWB material with type 4 epoxy resin* (FR4) and the special materials was quite small at the frequency range of the interest, so the usage of the low Dk materials were decided to keep as a future plan with the memories with higher clock speeds.

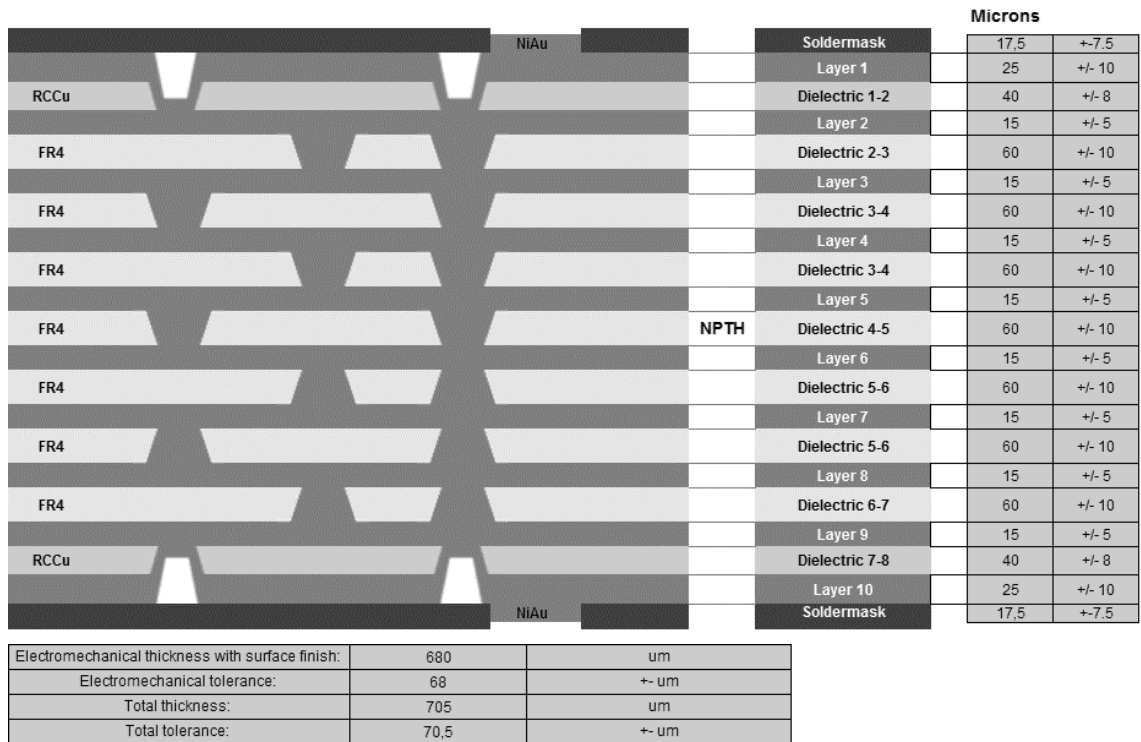


Figure 39 10 layer FV3 stackup view of the designed BoB PWB.

Thicknesses of all layers were matched so that the desirable characteristic impedance was possible to achieve with reasonable trace widths. Not too wide to prevent GND fills between the two signal traces, but not too narrow to cause significant resistive losses. The used trace width was approximately 50 μm , which equals very close to 50 Ω characteristic impedance with the stackup, described in the Figure 39. Also, the chosen trace width was enough to keep the impedance characteristics inside the wanted limits, even if the trace width would be off by the amount of maximum manufacturing tolerance, specified by the PWB manufacturer.

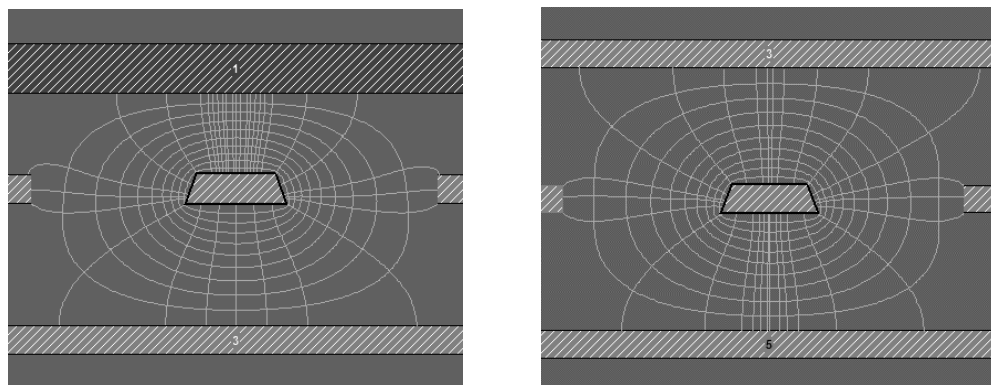


Figure 40 Figure on the left side presents the cross section view of the stripline in layers 2 and 9 with the RCCu coating on the other side, and the characteristic impedance of 45 Ω . Right side presents the stripline in other layers with homogenous FR4 dielectric layer on the both sides, and the characteristic impedance of 46 Ω . Also the lines of magnetic and electric fields are presented.

The Dk value of the FR4's dielectric material differs from the Dk value of dielectric material in *resin-coated copper* (RCCu) layer. To maintain the characteristic impedance of $50\ \Omega$ in layers 2 and 9 with similar trace widths, the thickness of the outer dielectric layers with RCCu material were reduced to $40\ \mu\text{m}$. The impedance characteristic of this combination is very close to other layer pairs. The final trace width calculations were done with the field-solver tool which takes into account different dielectric materials, distances and even the cross-sectional shape of the copper trace when it will be etched in the factory.

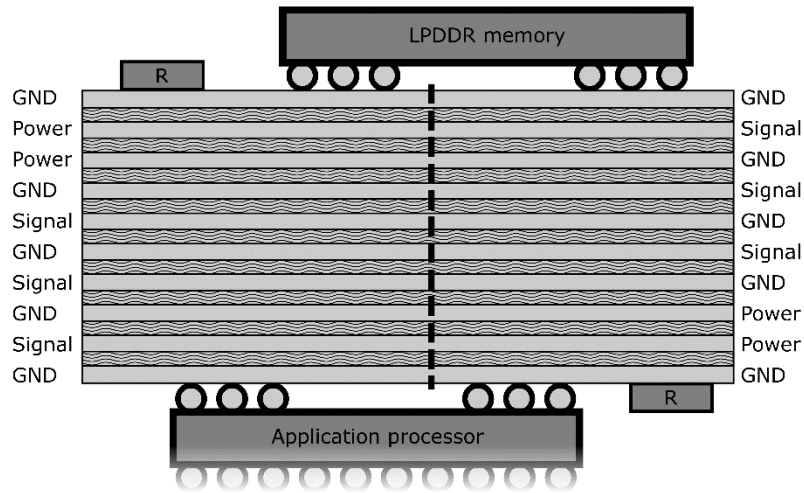


Figure 41 Cross section view of the layer utilization in new BoB design.

After the topology of component placement was decided, as shown in the Figure 41, the composition of the each layer was profiled. Typically each layer is utilized fully for the GND, power planes or signal traces, but because of the symmetrical, mirrored structure of the both sides, the PWB design was divided into two halves with opposite signal mappings, as presented in the Figure 41.

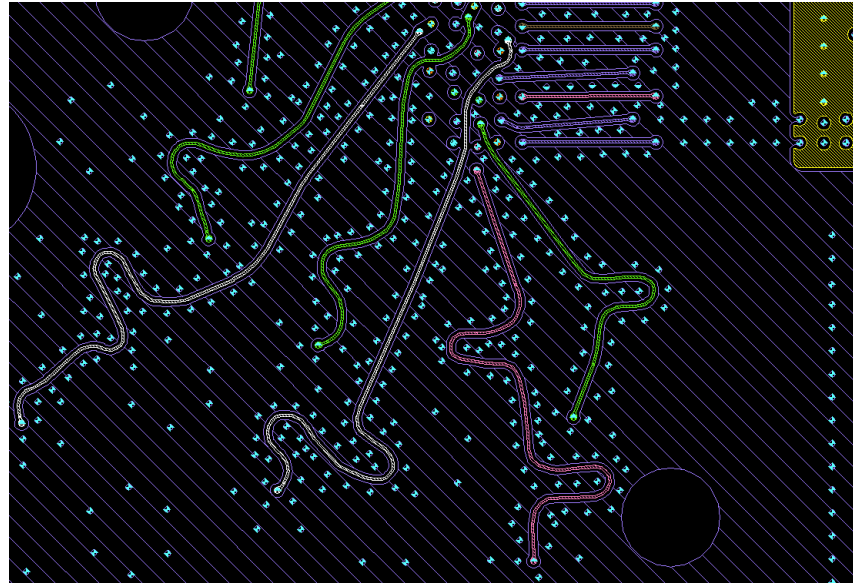


Figure 42 Layout view from layer 9, left bottom corner of the PWB.

After careful planning of the component placement and layer mapping, the layout work was done by following the previously set guidelines. Figure 42 shows the previously presented layer mapping, which is different for both halves of the PWB. On the right side there is the edge of power plane, horizontal traces at the top are interconnections between two BGA footprints, and in the middle there are signal traces going from the series resistors to the connector array. As seen, there are signal traces from different length matching groups, and the size of the length matching structures are moderate if compared to the design which would have equally matched signal traces. Space saving also allows smoother edges, which keeps the characteristic impedance of the signal trace consistent. As stated previously, the crosstalk has become a problem in previous BoB designs. The newly designed BoB has a microvia fences around every signal trace, which improves the crosstalk performance.

As presented in Figure 41 the layer mapping compromises a bit on the layers 2 and 9. Ideally, the signal traces would be completely between the two GND planes, which would cover at least 3 times the width of the trace [16]. This rule is not fully achieved in every part of these layers because of the BGA pads on the top and bottom layers, but the simulations have shown that it would not cause significant problems on the utilized frequency band.

In terms of layout design, IC to IC interconnections needs a lot of PWB area, so the power planes were fitted into two PWB layers to save space for the fully ground shielded signal traces. However, as the Figure 41 presents, there are power planes under the SMD resistors on the PWB. Power planes, especially for digital logic, can be relatively noisy, and it is not recommended to place them next to the signal layers. To reduce the coupled noise, the parasitic capacitance between the SMD pad of the resistor and the power plane

needs to be reduced. This is done by doing cut-outs to the power plane under the resistors, while keeping in mind the PI requirements and continuity of the power plane.

6.4 The final implementation

Finally, the interposer stack was soldered to the mobile device with a reworking machine. Multilayered interposer stack with the AP and DRAM is quite challenging to get operational as the ICs and the BoB PWB tends to bend under high temperatures, and the extra pressure, caused by the weight of the BoB PWB deforms the BGA balls during the soldering process. There was also a concern about the new BoB design regarding to reflow soldering, because the board itself is a bit larger and thinner than the previous boards. Also, the BGA footprint is not exactly in the center of the board, so the weight distribution could tilt the interposer stack during the soldering. However, the rework soldering of the SI BoB was not more challenging than previous BoB's.

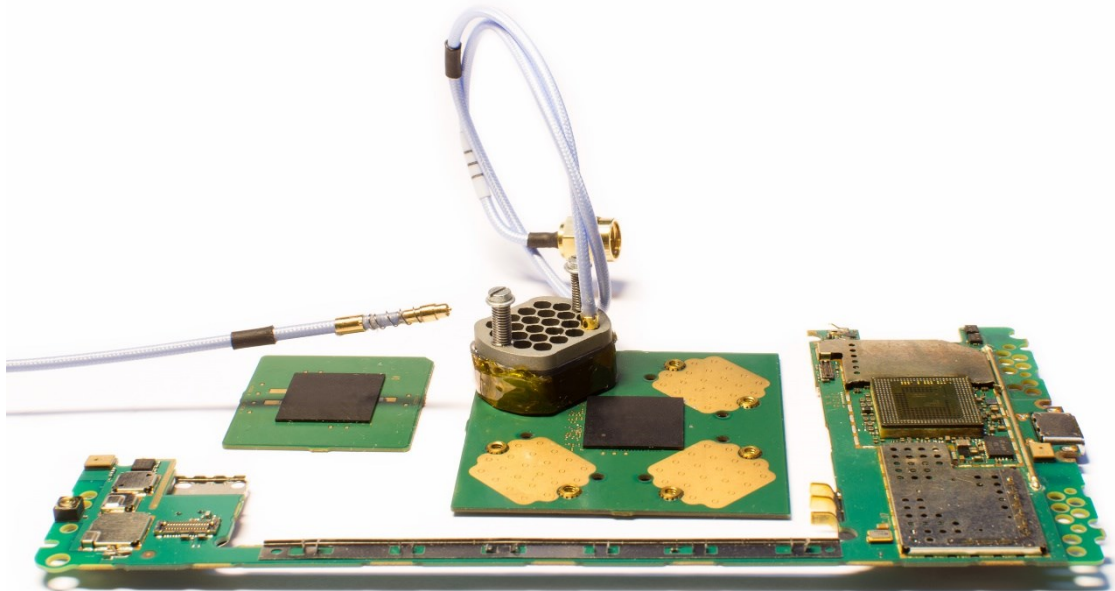


Figure 43 Microsoft Lumia 950 XL mainboard with a riser board reworked between the mainboard and AP. In the middle, there is a SI measurement board with one Bull's Eye BAR connector matrix attached, and one unconnected cable's end. On the left side, there is a current consumption measurement BoB.

The best resistance value for the series resistor was simulated, but at the beginning, there were no resistors attached during first tests to make sure that the PWB itself does not cause any issues. After initial test, the DUT was operational with no stability issues, and couple of resistors were soldered on the PWB. Also, a couple of other resistor values were tested to inspect the effect to measured signal quality. The system began to crash with a series resistor values, less than 100 Ω , because of major signal loss, caused by the measurement system. Resistor values between 100 Ω and 500 Ω worked as long as the

end of the transmission line was connected to the oscilloscope. Both BoBs and the tested mobile device is presented in Figure 43.

That lead also a new problem. When the signal is measured, it is connected to the oscilloscope and everything works. At same time there are dozens of other signals that are disconnected from oscilloscope by the switch matrix. Disconnected signals are not terminated, and the reflections, caused by the open-ended transmission lines caused stability issues to the DUT. One solution would have been to invest in new switches, which are terminated even if the signal is not connected to the common output. Especially differential clock and data strobe signals were observed to be very sensitive for the reflections. The DUT became stable with a 1 k Ω series resistors on PWB, but then the SNR level of the measured results were unacceptable because of the voltage division between the series resistor and the 50 Ω termination impedance of the oscilloscope.

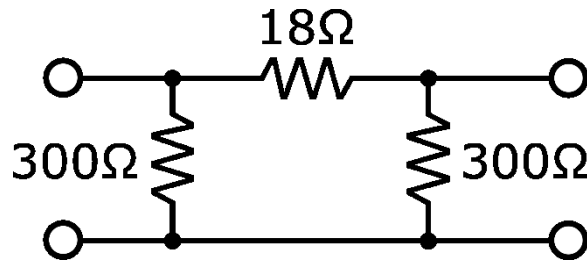


Figure 44 Equivalent circuit of the 3 dB attenuator for 50 Ω system.

As stated, the value of the series resistor on the PWB could be close to 100 Ω instead of 1 k Ω , if the transmission line would be always terminated, and there would not be any reflected signals coming back to the DUT. The problem was solved by placing a 3 dB attenuators to the input terminals of the switch matrix. As the Figure 44 presents, mentioned attenuator includes three resistors in pi configuration. When the switch is connected, the terminator provides 3 dB attenuation and 50 Ω characteristic impedance. When the switch is open, the attenuator provides termination for the signal path. The termination impedance depends on the attenuation value. The higher the attenuation, closer the value is to ideal 50 Ω when the switch is open. The 3dB attenuator provides 154 Ω termination in unconnected switch position, which is not ideal, but reduces the reflected signal significantly if compared to the completely open ended transmission line. There were no issues observed in the differential signals with 3 dB attenuator and 100 Ω series resistor on PWB. Because the resistance of the series resistor needs to be included into de-embedding function and it needs quite much effort to change the value afterwards, the resistance of the series resistor was fixed to 150 Ω to keep a certain safety margin, if the DUT's in the future are more sensitive for reflected signals.

Single-ended signals appeared to be more robust against the reflections. There was no need to invest attenuators for them because the 560 Ω series resistor on the PWB was able to maintain good SNR during the measurements and good stability when the measurement path was disconnected by the switch matrix.

The previous BoB had 01005 sized series resistors, which would have been relatively challenging to rework and solder by hand when testing different configurations. The new BoB enabled the usage of 0201 sized SMD resistors, which are hand-solderable relative easily. Finally, $150\ \Omega$ resistors were soldered to differential signals and $560\ \Omega$ resistors for single-ended signals. This configuration worked well while still maintaining certain safety margin for the DUT's in the future.

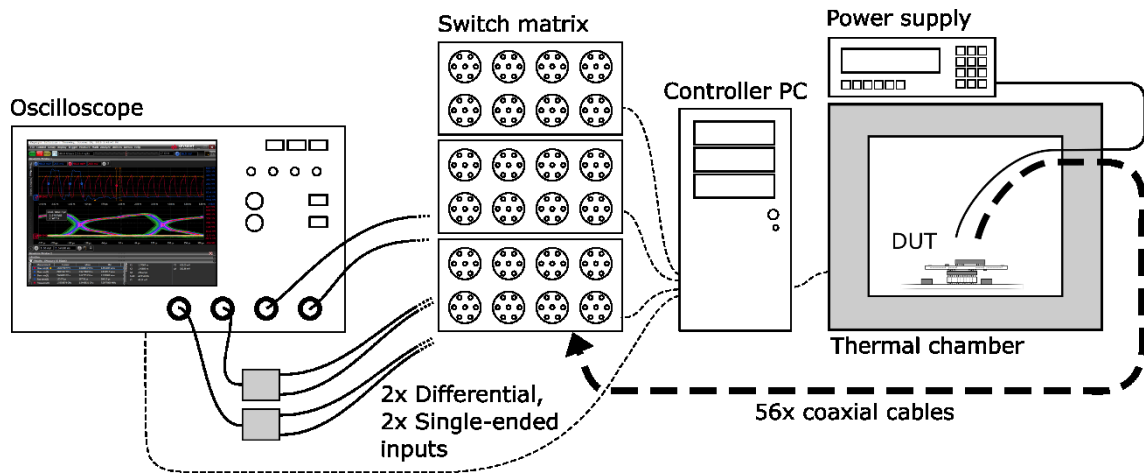


Figure 45 Illustrative picture of the complete measurement system

Measurement setup, described in the Figure 45 had been already implemented by J. Möykkynen [4]. To minimize the effort and expenses, the system was kept intact as highly as possible, and only the critical parts were upgraded. As found out in the background theory chapter, the oscilloscope with a 16 GHz analog BW [9] and the *general purpose interface bus* (GPIB) controlled switch matrix with a 18 GHz BW [21] is certainly enough when combined with a decent quality coaxial cables and digital post-processing function. Because the new system removes the need of high impedance probe head, single-ended signals do not need a probe amplifier anymore. Attenuating the signal in probe head and amplifying again by the probe amplifier would increase the noise, so it would not be beneficial.

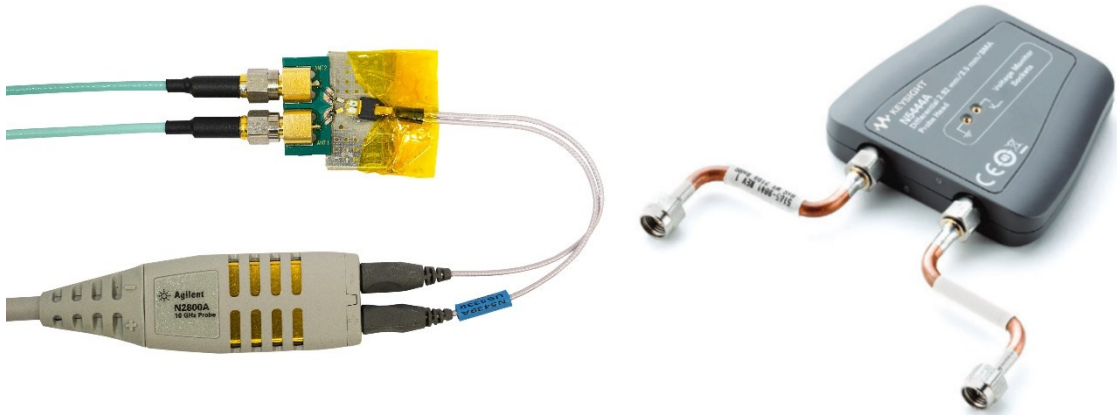


Figure 46 Self-made differential termination board, connected to the solder-in probe head with high input impedance, which is connected to probe amplifier. Keysight N5444A [28], on the right side, will replace the self-made differential terminator and solder-in probe head in the future, when the higher measurement bandwidth is required.

Differential signals utilizes two signal paths through the system. Measurement could be done by using two oscilloscope channels and math function but since there are only four oscilloscope's channels available, both differential pairs are converted into single-ended signals. Differential converters, shown in Figures 45 and 46, could be done in many ways. At the beginning, simplest experimental solution, was to use a self-made board with two SMA connectors, termination resistors and already existing Agilent N5439A solder-in differential probe head [28] with Agilent InfiniiMax III N2800A [28] probe amplifier. Initial tests indicated, that the performance of this solution was close to the case, where SMA cables were connected directly into ports of the oscilloscope and the differential conversion was done with the math function. The self-made converter was used at the beginning but the memories with clock speeds, higher than 1.6 GHz, may need a proper differential probe head with SMA terminals and termination because of the higher length matching and SI requirements. The system is easily upgradeable with a Keysight N5444A probe heads with the BW of 28 GHz [28]. Although the existing InfiniiMax III probe amplifier and oscilloscope limits the BW to 16 GHz and it is expected to be enough in the near future.

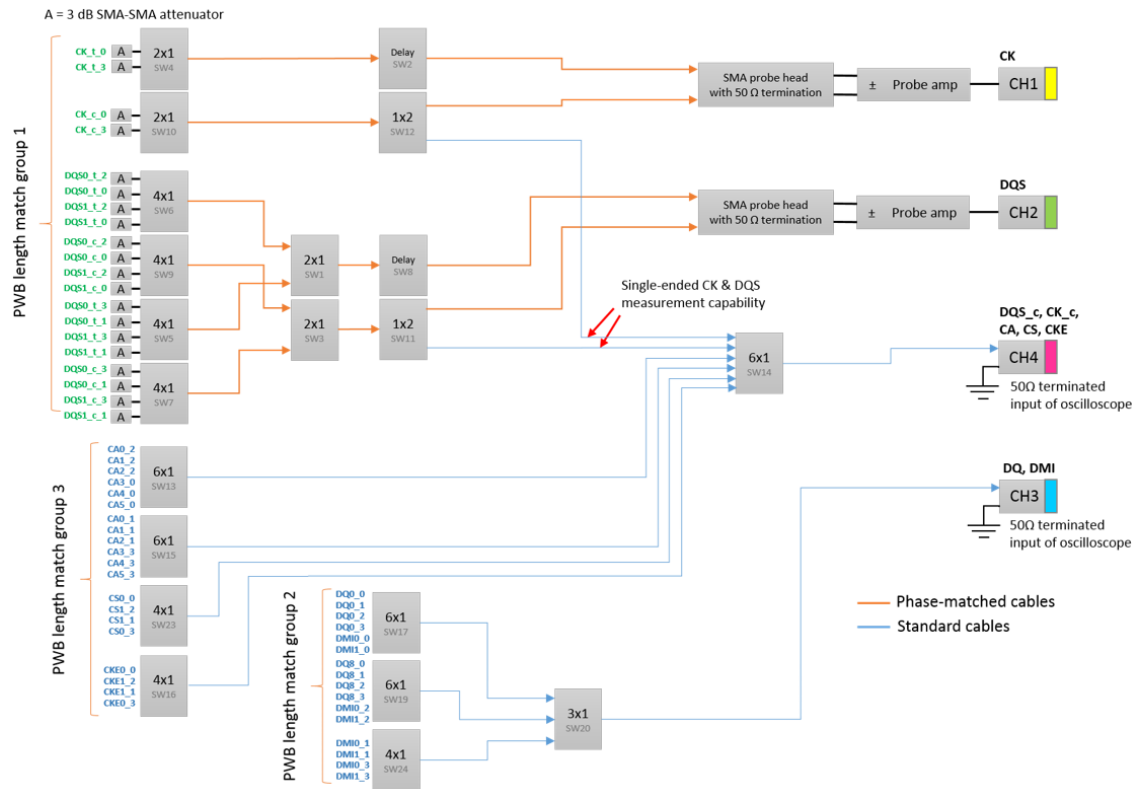


Figure 47 The switch matrix topology.

As stated, the measurement guideline was reconsidered along this thesis work, which reduced the amount of the measured signals significantly. Previously every signal was routed to the switch matrix, so the measurement had to be done in two parts to keep the amount of cables and switches reasonable. However, the new measurement guideline can be used also with older LPDDR memories, so there is no more need to maintain full backwards compatibility with the previous measurement system. If the Agilent Soft touch probing system needs to be connected again to the switch matrix at some point, signals can be connected to corresponding switches without modifying the switch control software or the switch-to-switch interconnection cabling.

7. RESULTS

After the initial tests were done, the system was built and the results were compared to the reference data to verify that the measured results matches to the expectations. This chapter presents the measured results in frequency domain, which gives a good view of system's general performance and feasibility for the upcoming, faster LPDDR memories. The system was also tested with the Microsoft Lumia 950 XL smart phone to get the time-domain measurement results with a real HW and real test cases.

As stated, the de-embedding function compensates the relatively high attenuation of the measurement path and the differences in electrical delay, caused by the switch matrix and cabling setup. To make the waveform comparison possible between the original and post-processed signal, all the time-domain waveforms, presented in this chapter, are scaled manually in terms of amplitude and timing skew. Also, some of the oscilloscope screen capture figures lacks the amplitude data and exact signal names to protect the intellectual property of Microsoft and its business partners.

Inspecting the measured results, if they look as they should, is not a trivial task because the ideally perfect reference waveforms do not exist. At the high BW applications, even small differences can change the waveform quite significantly. Also every pin of the IC package have slightly different parasitic properties and variations in the transceiver circuits and software defined parameters. The waveform comparison was done by using the simulated waveforms, measurement result from the previous memory testing system and the waveform images from the business partner's documentations.

There are two main causes that could possibly distort the measured waveform if compared to the reference waveforms. The measurement system could interfere with the DUT by causing distorted waveforms or even instability, at the worst case. Or then the signal could be still correct at the DUT's end, but the signal path between the DUT and the oscilloscope could distort the waveform. Neither of the mentioned issues cannot be removed completely, but the achieved goal was to minimize the distortion by combining a good HW design and the digital post-processing of the measurement data.

The BoB PWB increases the length of the transmission line between the receiver and the transmitter by 3 mm from its nominal length in PoP stack. Because the ODT in receiving IC is not ideal, any extra length between the transmitter and receiver will increase the reflections and ringing in the measured waveforms. The slightly degraded SI performance between the IC's, caused by the BoB, was observable from measurement results. However, the waveform had only minor changes and there was no stability issues observed. The observed distortion, caused by the BoB, was cancelled out by including the BoB's electrical model into the de-embedding function.

RF characteristics of the cabling and switch matrix can be measured with relative ease because the oscilloscope's end of the cabling have coaxial SMA connectors, which can be connected directly to the VNA. Ideally the transmission line would be connected between the two ports of the VNA. In this case, the another end of the transmission line is the PWB pad of 0201 sized resistor, so it would be very challenging to attach that to the VNA's port without compromising the measurement quality significantly. However, Keysight have created a software option for this specific issue, called *automatic fixture removal* (AFR) tool. The tool requires that one end of the transmission line is connected to the VNA's port, and the another end is completely open or shorted. The tool calculates the 2-port S-parameter file from the transmission line, based on the signal which reflects completely from the open or shorten transmission line's end and comes back to the VNA's port. Achieved S-parameters can be used in the de-embedding function but also the RF performance of the signal path can be inspected from the S-parameter data.

Keysight's AFR tool [25] created S-parameter fixture files for single-ended signals with no issues. However, the AFR algorithm did not reach very good accuracy in frequencies below 50 MHz, when there was a 3 dB attenuator along the signal path. In differential signals with attenuators, the attenuation at DC was measured with a power supply and multimeter to achieve the needed accuracy over the whole frequency range of interest. Measured DC characteristics were added to the S-parameter files manually, so the DC gain values of the transfer functions, created by Keysight's InfiniiSim software, were correct.

The properties of the measured S-parameters seemed good in terms of amplitude and phase response. Of course, there were minor non-idealities, which could be compensated by including the S-parameter files into the de-embedding function of the oscilloscope. As a sanity check, the transmission line between the DUT and the oscilloscope was also measured by removing the series resistor from the BoB, and by connecting the solder-in oscilloscope probe with a 16 GHz BW to the SMD pads of the unattached resistors. Measured waveforms from the LPDDR4 signal's matched well to ones, measured through the PWB, cables and switches. Similar results indicated that the characterization technique of the transmission line and the de-embedding function worked as intended.

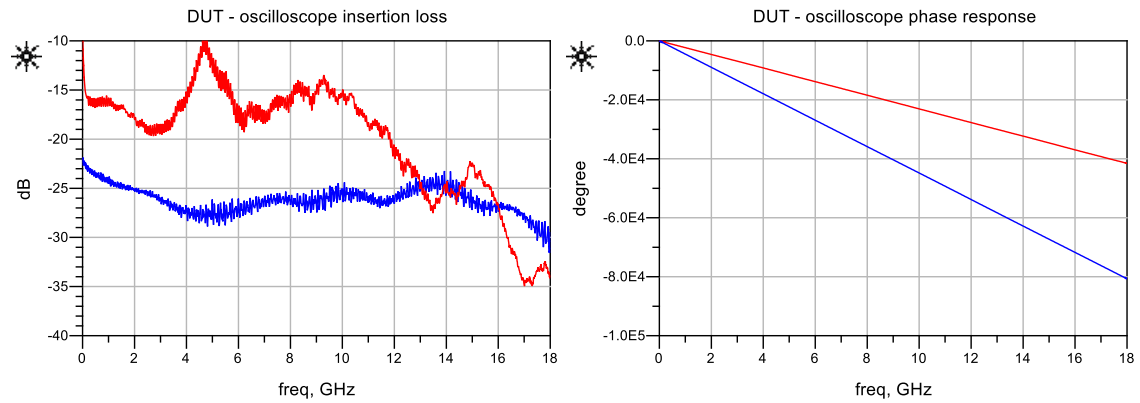


Figure 48 Insertion loss and the phase response between the DUT and the oscilloscope. Red: old system, blue: new system.

Figure 48 presents the amplitude and phase responses between the DUT's IC and the oscilloscope. Although the non-ideal insertion loss and phase response characteristics can be compensated in de-embedding, it should be kept in mind that the total attenuation through the system should be low enough to allow the oscilloscope to capture the signal with adequate SNR. The voltage scaling of the acquisition HW in the oscilloscope is set according to maximum peak voltage levels to prevent the overflow in oscilloscope's *analog-to-digital converter* (ADC). Typically the highest amplitudes are passed to the oscilloscope, on the frequencies with lowest attenuation. Every frequency component with higher attenuation will be gained digitally in the de-embedding function to linearize the amplitude response curve. Due to the dynamic range of the oscilloscope with 8-bit ADC, there cannot be huge variations in the system's amplitude response, over the frequency range or also the noise will be gained to non-acceptable levels.

Due to the new BoB design and the low loss coaxial cables, connectors and RF switches, the flatness of the amplitude response is improved from the previous testing system. Although the total attenuation through the system is greater, it is still low enough to be measurable with the oscilloscope. The Figure 48 also presents the phase response which seems to be linear in both cases, as it ideally should be.

In addition to that, it is also important to inspect, how the BoB and the measurement system affects to the SI properties between the AP and the DRAM. The transmission line between the AP and DRAM is very hard to measure with a VNA because the PWB trace is very short and the BGA pads are small, and cannot be connected directly to the VNA without the extra miniature solder-in coaxial probes attached. Such small objects can be typically modelled most accurately by using the simulation software with 3D EM field solver capabilities, if the layout data and stackup of the PWB is known. After adding the S-parameter models of the cabling, switches and PWB layout to the de-embedding function, there were still some visible reflections which were not visible in simulated reference waveforms. After adding also the IC package models to the de-embedding function, the measured results began to look similar to the reference waveforms.

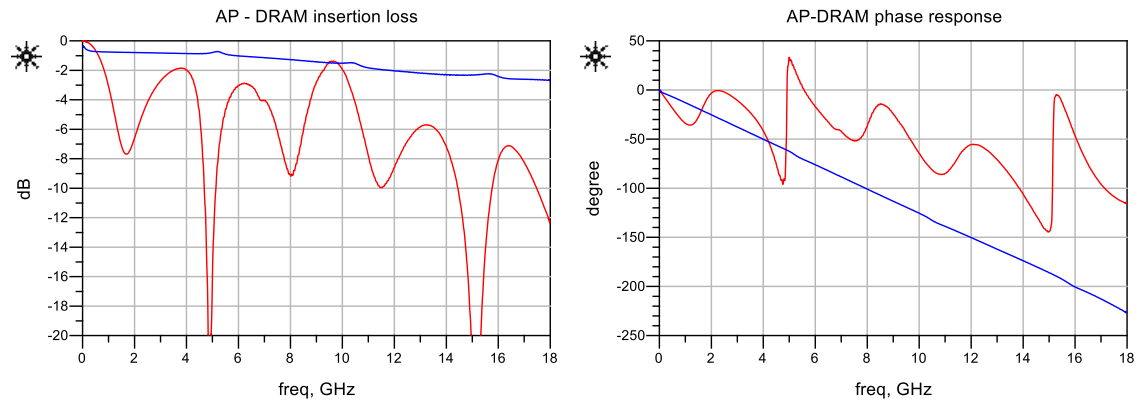


Figure 49 Insertion loss and phase response between the AP and DRAM. Red: old system, blue: new system.

The maximum stable operating frequency of the previous BoB and the measurement system was approximately 1.3 GHz. The maximum usable frequency of the new measurement system could not be fully tested because there were no devices available with high enough operating frequency to cause issues at the time, when the measurements were done. However, as the Figures 22 and 49 presents, the measurement node of the new memory testing system is well impedance matched and there is no significant reflections, which was the main issue with the previous measurement system with a high impedance oscilloscope probe. The amplitude and phase responses between the AP and DRAM appears to be significantly better if compared to the previous BoB's. Based on that, also the DUT's with a higher clock speeds should operate without problems in the future.

As previously stated, the crosstalk has been an issue with the previous BoB's. Mostly, there were no visible crosstalk issues with the new BoB design, because of the reduced amount of the signals and better ground shielding. Only couple of the signals had noticeable crosstalk issues, but the attenuation from the aggressor signal was still good enough to achieve desired measurement quality. The minor crosstalk issue was narrowed down to be caused by microvias, placed too close to the signal trace. The crosstalk performance could be improved further in the next PWB revisions for the upcoming LPDDR memories by taking this into account during the layout design process.

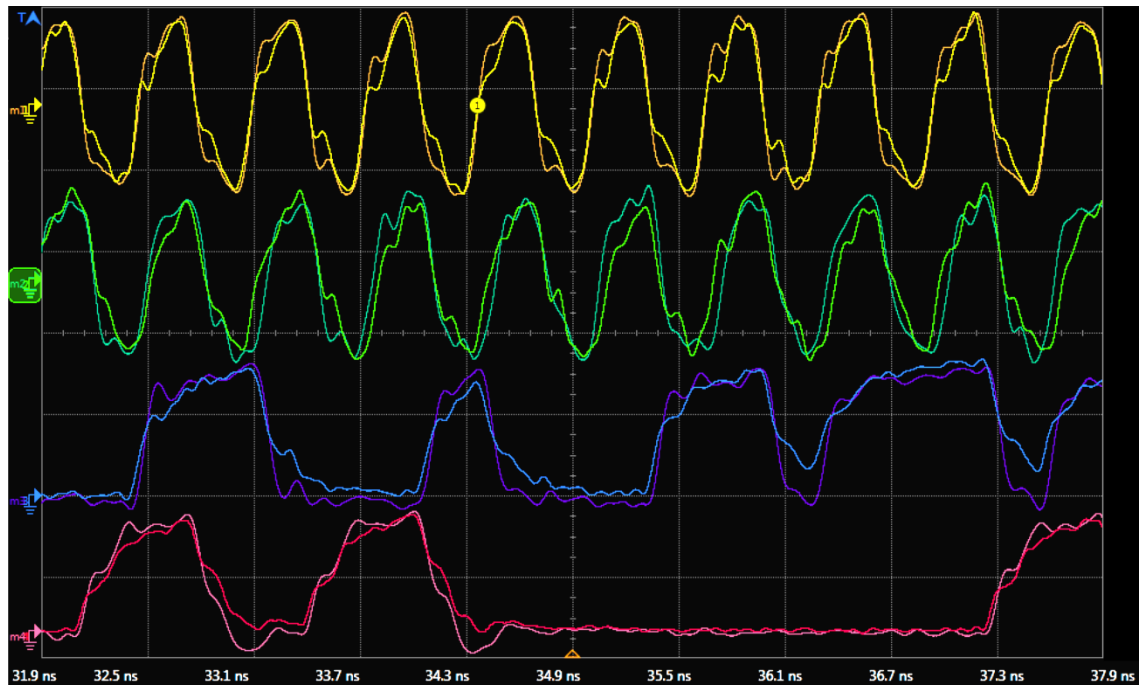


Figure 50 Four different time-domain waveforms measured simultaneously with the oscilloscope, through the switch matrix and whole measurement setup. Yellow, green, blue and red traces presents the signals without de-embedding and the other corresponding signals have de-embedding applied.

Figure 50 presents all four channels measured simultaneously with the analog BW of 16 GHz and sampling rate of 40 GS/s per channel, through the cabling and switches, presented in the Figure 47. Although the length of the cabling and amount of the switches varies depending on the measured signal, the timing skew is removed in the de-embedding function, so the relative timing of the different signals can be compared.

The waveform varies significantly depending on the direction of the data. Measurements could be done with the purposely made mobile device testing software, which only reads or writes to the memory during the test with a specified clock speed. However, the memory interface is highly software configurable, so the verification needs to be done in a high level operating system, with realistic use cases, to exclude the possibility of software configuration errors. Measuring with the unmodified software causes the operating frequency of the memory interface to be changed automatically based on the memory utilization. Also, the data traffic will include both, reads and writes, in realistic use cases. Setting the oscilloscope to trigger only to the waveforms with a specific clock frequency and data direction can be quite challenging.

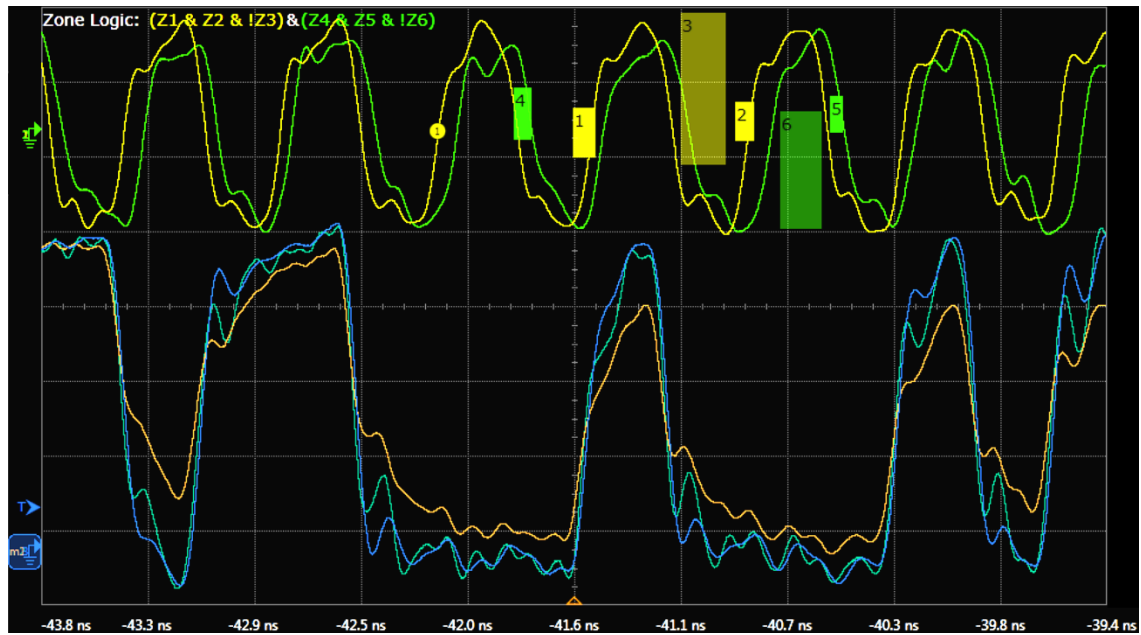


Figure 51 Zone triggering set-up to trigger for the specific memory clock frequency and data direction, based on the alignment of the green and yellow waveforms. The orange waveform presents the data signal without the de-embedding, teal trace have only the signal path from the PWB's series resistor to the oscilloscope de-embedded and the blue waveform has full de-embedding profile, which includes also the electrical models for the IC's and PWB.

Zone triggering, used by some of the modern oscilloscopes, becomes very handy in this specific case. Figure 51 illustrates the zone triggering setup, where the waveform must intersect with zones 1, 2, 4 and 5, and must not intersect with zones 3 and 6. By creating these areas correctly, the oscilloscope triggers only to the wanted frequency and data direction, which can be deduced by the relation of the signals with each other. The triggering could be done also by investing to the automated LPDDR4 compliance software add-on for the oscilloscope, which have pre-made triggers and measurement setups for the needed test cases.

Figure 51 also presents the original data signal without post-processing, and two sets of de-embedding profiles, made for the measurement system. One de-embedding profile includes only the effect of series resistor on the PWB, and the rest of the system between the resistors and oscilloscope. This is general purpose profile, which could be used also with other IC's than LPDDR4 memory and with different PWB constructions. For the best measurement quality with the LPDDR4 memories and the designed BoB PWB, there is also a profile, which includes the AP – DRAM PWB interconnection and the parasitic properties of IC the packages. The general purpose profile gives fairly good results but has still some reflections and ringing, which are partly caused by the BoB PWB. The profile with lower abstraction level and more specific electrical model of the system, reduces the ringing and reflections a bit, and the waveforms corresponds better to the simulated case, where is no BoB PWB attached between the AP and DRAM.

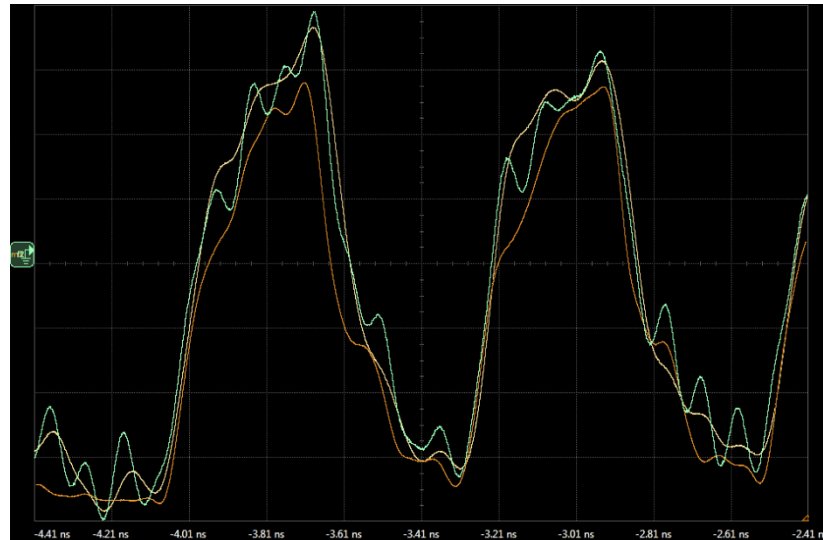


Figure 52 The orange trace presents the measurement with a series resistor on the PWB unattached and the solder-in oscilloscope probe with a 16 GHz BW attached to the SMD pads of the resistor. The teal trace is measured through the final measurement system with only the signal path from the PWB's series resistor to the oscilloscope de-embedded. The brown trace presents the fully de-embedded measurement result.

One of the reference waveforms were measured by removing the series resistor from the PWB and by attaching a high performance solder-in oscilloscope probe to the PWB pads of the unattached resistor. As stated, measuring the signal without distorting the original signal at all, is impossible in practice, but this setup was as close to the ideal measurement case as could have been achieved reasonably with the available measurement equipment. As the Figure 52 presents, the measured waveform matches relatively well to the results, which were achieved by using the automated memory testing system with de-embedding.

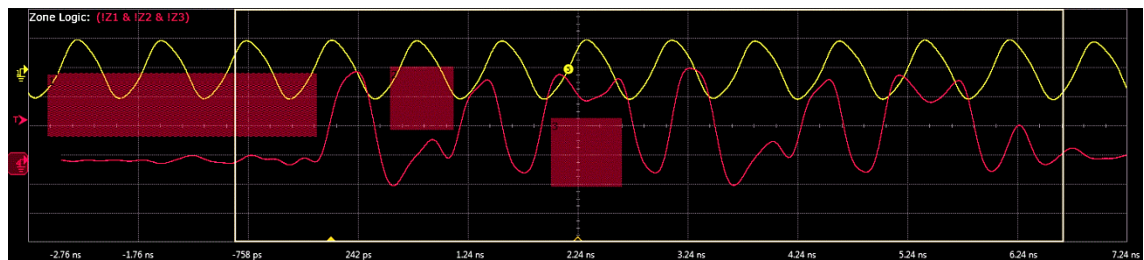


Figure 53 Waveform measured with previous measurement system at 1.3 GHz clock speed. This measurement utilizes standard de-embedding profile without digital extension of the frequency BW of probe head.

Originally, the Agilent N2887A probe head limited the usable frequency BW of the previous measurement system up to 4 GHz. The Figure 53 presents one of the measurements, done by using the original de-embedding profile. Although it have been working as intended with the earlier LPDDR generations, the waveform results does not match to the reference waveforms anymore with the LPDDR4 memories. Top of the limited transition speed of the signal, there is also a significant amount of ringing and

over and undershoot in the measurement results, done with the previous measurement system and LPDDR4 memories.

Later, the original de-embedding profile of the previous measurement system with a frequency BW of 4 GHz, was extended to 10 GHz. Because of physical limits of the probing head, the extensive digital amplification of the high frequency components causes significant amount of noise and also amplitude errors to the measurement results.

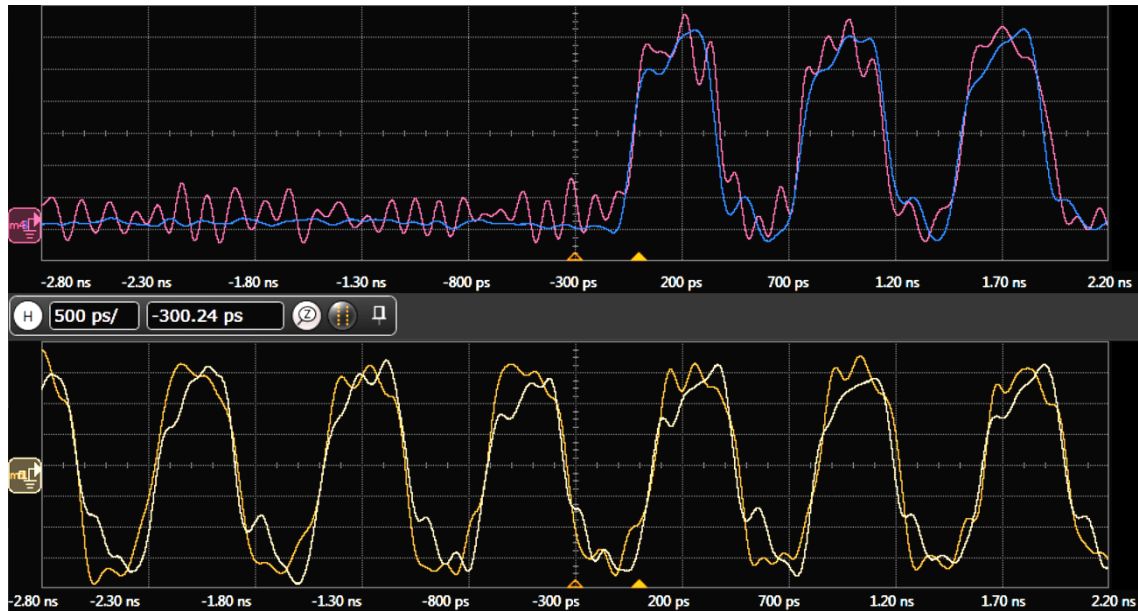


Figure 54 Fully de-embedded results compared to the waveforms, measured with the previous measurement system with the Soft touch probes. The orange and magenta waveforms presents the results, measured with the previous measurement system.

Figure 54 presents the waveforms, measured with the previous testing system, with digitally compensated probe profiles that extends the measurement BW from 4 GHz to 10 GHz. To prevent the stability issues with the old measurement setup, the clock frequency of the DUT was limited to 1.3 GHz. As a comparison, the same waveforms were measured with the new testing system. There were no problems with the under and overshoot, ringing and noise performance with the new measurement system. After de-embedding, there is still some minor reflections, ringing, over and undershoot in the measured results, with the new testing system. This is mainly because the signal transceivers and transmission lines in the AP and DRAM are not ideal, and these effects are present also in unmodified devices.

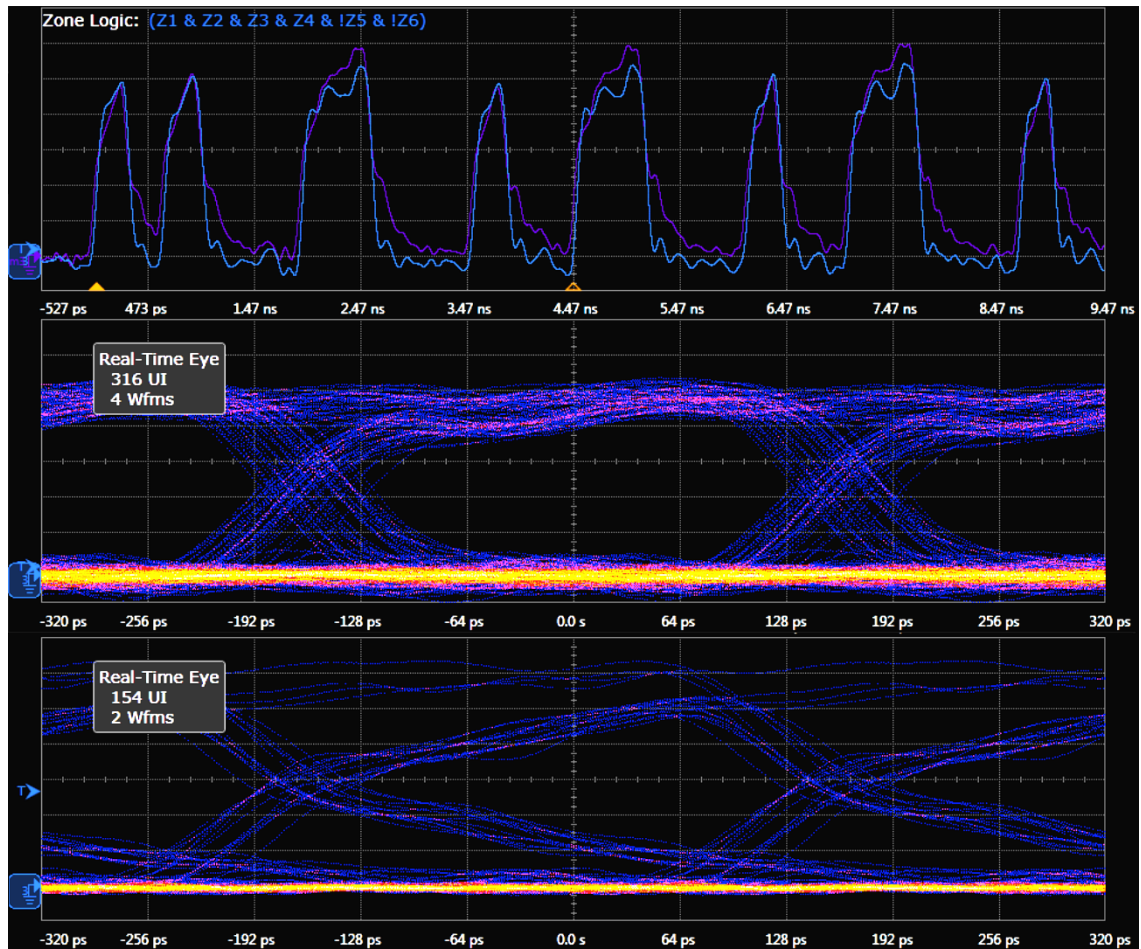


Figure 55 Eye diagram comparison with the de-embedded and not de-embedded measurement data at 1.6 GHz clock frequency. The blue signal trace and upper eye diagram figure have the de-embedding function applied.

As stated in the fourth chapter, the eye diagram measurements are important part of the verification of the high-speed signal bus. Now the previously simulated eye diagram case was measured from the real HW. Figure 55 presents the achieved waveform from the same signal, at the same data rate, that was simulated in the chapter 4. As can be observed, the eye diagram without de-embedding have noticeably degraded signal transition speed, which mainly denotes that the high frequency components are attenuated along the signal path more than the base frequency component. After applying the de-embedding, the eye diagram looks similar to the expected results. The most notable difference to the simulated ideal case, presented in the Figure 26 is, that the measurement have fair amount of jitter, which was not included into the simulated signal source to clarify the BoB's effect to the SI properties of the system.

Jitter tells the deviation in signal's timing. The total jitter and its probability function can be deducted from the eye diagram. Total jitter is the sum from the random jitter with Gaussian deviation and the deterministic jitter with non-Gaussian probability density function. Jitter narrows the eye area of the eye diagram. In the worst case it can cause errors in data transactions if the bit's timing varies more than the specification allows. A

good eye diagram measurement need lots of captured waveform to cover also the most improbable worst case events. [29]

8. CONCLUSIONS

The previous automated memory testing system has been working with the LPDDR2, LPDDR3, and also with the lower-end LPDDR4 memories. Now, due to the increase in memory clock speeds and signal transition times, the measurement capabilities of the system began to cause stability issues for the DUT, and captured signals did not match very well to the reference waveforms with latest LPDDR4 memories. The scope of this thesis work was to characterize the old system carefully to find out the reasons for observed issues, and to improve the system to be able to operate with the current LPDDR4 memories and the next memory generations. The final goal was to implement the designed upgrades to the automated memory testing system to allow accurate and reliable verification measurement results for the mobile devices in the future.

The design was based on the existing measurement system, developed and upgraded by multiple persons during last ten years. In previous years, M. Heikkilä [3] and J. Möykkynen [4] have done their master's thesis work to enhance the system. In conclusion, the most important enhancement done, along this thesis work, was to minimize the length of the transmission line with a non-controlled impedance. This required the replacement of the previously used high input impedance probing array with the similar, easily swappable, connector matrix with a characteristic impedance of 50 Ω . The modification extended the beginning of the 50 Ω transmission line very close to the AP and DRAM. The modification was possible because of the newly presented PWB design, which has a slight offset in IC's positioning. This allowed the series resistors to be located very close to the AP – DRAM interconnection without using impractically costly embedded resistors. Also circular miniature couplers were newly presented along this MSc thesis. Those were greatly beneficial in PI measurement setup, in signal presence detection.

To allow an accurate measurement results for the signals with high BW, also the post-processing method had to be modified. Now, instead of coaxial cables, switches and connector matrix, also the PWB and IC packages were included into the de-embedding profile, which removes the effect of the measurement setup from the measured waveforms.

As the measured results indicated, the implemented system seemed to perform very well at the wide frequency range. During the characterization of the built system, couple of minor observations were made that could improve the performance of the BoB even further. As the first revision worked already decently with the high-end Microsoft Lumia 950 XL smart phone, there was no need to design the 2nd PWB revision. All the improvements could be done easily in the future if the next PWB revisions are needed for the memories, with different pinouts.

The newly upgraded probing system could be used also in other purposes than memory testing. The BoB could be designed for example for the AP or mass-storage IC. The best resistance value for series resistor varies a bit depending on the signal transceiver properties of the DUT. Also, if the DUT has signals with weak pull-ups, the termination technique or the resistance of the series resistor must be changed. One option would be to use the AC termination at the oscilloscope's end or the series resistors with significantly higher resistance and a broadband *low-noise amplifier* (LNA) at the oscilloscope's end to amplify the signal to measurable levels. Either of the compromising options to achieve high input impedance, would not be as good in terms of SI, as the designed LPDDR4 memory testing system but they would allow measurement of the signals which are sensitive to the probe's loading effect. In the general level, the most sensitive signals in mobile devices does not typically have very high clock speeds, so the compromised frequency BW of the measurement system, would not necessarily reduce the measurement quality significantly.

The selected connector matrix topology has plenty of extra positions, which could be utilized in the future if more traceable signals are needed. As M. Heikkilä mentioned in his thesis work [3], also the option for the higher grade PWB material could be utilized if the needed frequency BW of the memories increases considerably in the future. Usage of the MEMS or GaAs transistor based switches were investigated during the concept level designing of the implemented system. Although they would have allowed very short cables with low loss, the crosstalk properties and the attenuation of the miniaturized switches were not suitable for the implemented system. Usage of the different switch types could have been reconsidered later if there will be major development in the miniature RF switch technology.

REFERENCES

- [1] “High Performance & Low Power Memory Trend,” SK Hynix Semiconwest 2013 seminar material, CA, USA. [Online]. Available: http://www.semiconwest.org/sites/semiconwest.org/files/docs/SW2013_Minho%20Kim_SK%20Hynix.pdf
- [2] JESD209-4. Low Power Double Data Rate 4 (LPDDR4). Arlington 2014. JEDEC Solid State Technology Association. 196 p.
- [3] M. Heikkilä, “Advanced Measurement System for the Verification of POP Memories,” M. Sc. (eng.) thesis, Tampere University of Technology, Tampere, Finland, June 2006.
- [4] J. Möykkynen, “Automated switch matrix solution for signal integrity and timing measurements of a mobile device,” M. Sc. (eng.) thesis, Tampere University of Technology, Tampere, Finland, March 2014.
- [5] P. Horowitz, W. Hill, The Art of Electronics, 2nd edition, USA: Cambridge University Press, 1989.
- [6] Prof. B. Osgood, “Lecture Notes for EE 261 The Fourier Transform and its Applications,” Stanford University, USA, 2007. [Online]. Available: <https://see.stanford.edu/materials/lsoftae261/book-fall-07.pdf>
- [7] “Measurement System Signal Integrity: Important Factors to Consider,” Tektronix, Technical Brief, USA, 2010. [Online]. Available: www.tek.com/dl/55W-18024-3.pdf
- [8] “Evaluating Oscilloscope Bandwidths for Your Application,” Agilent Technologies, Application note, USA, April 2014. [Online]. Available: <http://cp.literature.agilent.com/litweb/pdf/5989-5733EN.pdf>
- [9] “Agilent Infiniium 90000 X-series Oscilloscopes,” Agilent Technologies, Data sheet, USA, April 2014. [Online]. Available: <http://cp.literature.agilent.com/litweb/pdf/5990-5271EN.pdf>
- [10] “Evaluating Oscilloscope Sample Rates vs. Sampling Fidelity,” Agilent Technologies, USA, April 2014. [Online]. Available: <http://cp.literature.agilent.com/litweb/pdf/5989-5732EN.pdf>

-
- [11] “Measuring of dynamic figures: SNR, THD, SFDR,” Strategic Test, Application note. [Online]. Available:
<http://www.cse.psu.edu/~chip/course/analog/lecture/SFDR1.pdf>
- [12] “Understanding Signal Integrity,” Agilent Technologies, Application note, USA, April 2002. [Online]. Available:
<http://cp.literature.agilent.com/litweb/pdf/5988-5978EN.pdf>
- [13] D. M. Pozar, Microwave Engineering, 4th edition. USA: Wiley, 2012.
- [14] “Impedance Matching and Smith Charts,” J. Staples, LBNL, lecture material. 2007. [Online]. Available:
http://uspas.fnal.gov/materials/08UCSC/mml13_matching+smith_chart.pdf
- [15] “Agilent N2887A and N2888A InfiniiMax Soft touch Probe Head,” Agilent Technologies, Datasheet, USA, 2011. [Online]. Available:
<http://cp.literature.agilent.com/litweb/pdf/5990-6481EN.pdf>
- [16] I. Rosu, “Microstrip, stripline, and CPW design,” Technical Article, April 2012. [Online]. Available:
http://www.qsl.net/va3iul/Microstrip_Stripline_CPW_Design/Microstrip_Stripline_and_CPW_Design.pdf
- [17] E. Bogatin. Essential Principles of Signal Integrity. IEEE Microwave Magazine [Electronic journal]. 11(2011), pp. 34 – 41. [accessed on 4.12.2015]. Available:
<http://ieeexplore.ieee.org>
- [18] “How a Team-Based Approach to PCB Power Integrity Analysis Yields Better Results,” Cadence Design Systems, white paper. [Online]. Available:
https://www.cadence.com/rl/Resources/white_papers/PCB_Power_Integrity_WP.pdf
- [19] “Application Manual for Power Supply Noise Suppression and Decoupling for Digital ICs,” Murata Manufacturing, Application manual, Japan, July 2010. [Online]. Available:
<http://www.murata.com/~media/webrenewal/support/library/catalog/products/emc/emifil/c39e.ashx>
- [20] M. Thompson, Intuitive Analog Circuit Design, 1st edition. USA: Elsevier, 2006

-
- [21] “Stocked Electro-Mechanical Switches, SP6T SEM Series,” Narda, Datasheet, USA. [Online]. Available: https://www.miteq.com/product-spec/219-SP6T_SEMSwitch.pdf
- [22] “Frequency Response of Thin Film Chip Resistors,” Vishay, Technical note, February 2009. [Online]. Available: <http://www.vishay.com/docs/60107/freqresp.pdf>
- [23] B. Olney, “Impedance Matching: Terminations,” The PCB Design Magazine, October 2013, pp. 36 – 43. Available at: http://www.icd.com.au/articles/Terminations_PCBDesign-Oct2013.pdf
- [24] “TDS5000B, TDS6000B, TDS/CSA7000B Series Acquisition Modes,” Tektronix, Application note, USA, March 2004. [Online]. Available: http://www.tek.com/dl/55W_17443_2.pdf
- [25] “Keysight N5465A InfiniiSim Waveform Transformation Toolset Software,” User’s guide, USA, April 2015. [Online]. Available: http://www.keysight.com/upload/cmc_upload/All/InfiniiSim_User_Guide.pdf
- [26] “Application Note 1111 An Introduction to IBIS (I/O Buffer Information Specification) Modeling,” Texas Instruments, Application note, Texas, 2011. [Online]. Available: <http://www.ti.com/lit/an/snla046/snla046.pdf>
- [27] Samtec Bull’s eye product catalog [WWW]. [accessed on 14.1.2016] <<https://www.samtec.com/cables/high-speed/test/bulls-eye>>
- [28] “Keysight InfiniiMax III/III+ Probing System,” Data sheet, USA, February 2015. [Online]. Available: <http://literature.cdn.keysight.com/litweb/pdf/5990-5653EN.pdf?id=1887900>
- [29] “Application note 1916 An Introduction to Jitter in Communications Systems,” Maxim Integrated, Application note, 2003. [Online]. Available: <http://pdfserv.maximintegrated.com/en/an/AN1916.pdf>