TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

MANU KUJALA

RELIABILITY OF SCREEN-PRINTED VIAS FOR A FLEXIBLE ENERGY HARVESTING AND STORAGE MODULE DESIGNED FOR INTERNET OF EVERYTHING -APPLICATIONS

Master of Science Thesis

Examiners: Prof. Matti Mäntysalo and Prof. Donald Lupo

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ABSTRACT

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Internet of Things (IoT) and Internet of Everything (IoE) concepts will have significant impact on the electronics market. These concepts require high volume and cheap electronics fabrication methods, which should be environmentally friendly as well. Printed Electronics (PE) enables novel materials on various substrates, that can be thin, light, flexible or stretchable. In the future, electronics can be implemented in the surroundings and are available whenever users need it. The vision is that all surrounded electronics are connected to the internet and are energy autonomous. Electronic devices can then gather energy from the environment and store it.

This thesis introduces an energy module, which can gather energy from ambient light with an organic solar cell and store it into an electrolytic double layer capacitor, also known as ultra- or supercapacitor. Both components can be printed on flexible substrates with PE methods. These components share the same substrate and the interconnection between them is done with a printed through-hole via and silver ink. The printed through hole via's printability and reliability is evaluated with a direct screen-printing method and cyclic bending test.

The results show that supercapacitor and organic solar cell -energy module can power up low energy electronic devices for short time periods. Roll-to-roll processing of the energy module is evaluated and a proposal of the energy module design is given. In the through-hole interconnection study, it is shown that the lower viscosity silver ink does not fill the via properly, but only to the sidewall of the via. This might lead to a poor interconnection between top and bottom of the substrate. Higher viscosity silver paste fills the via better and with 100 µm via size 100 % yield (n = 1010 vias) is achieved with this direct screen-printing method. The cyclic bending test showed no critical breakdown of the via even after 500 000 bending cycles. Using the direct screen-printing method in the roll-to-roll process enables multi-layered PE devices.

TIIVISTELMÄ

MANU KUJALA: Silkkipainettujen läpivientien luotettavuus taivutettavaan energian harvestointi ja tallennus –moduuliin, joka on suunniteltu kaiken internet sovelluksiin
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Asioiden internet (IoT) ja kaiken internet (IoE) konspetit tulevat mullistamaan elektroniikkamarkkinat. Nämä konseptit vaativat ympärilleen muun muassa laajan skaalan- ja halpoja tuotantomenetelmiä elektroniikkatuotteille, jotka ovat myös ympäristöystävällisiä. Painettu elektroniikka (PE) mahdollistaa uusien materiaalien ja alustojen käytön, jotka ovat kevyitä, ohuita ja taivutettavia tai venytettäviä. Elektroniikka pyritään saamaan sulautettua ympäristöön siten, että se on aina käyttäjän saatavilla, kun hän sitä tarvitsee. Kaikki ympäröivä elektroniikka on yhteydessä internetiin ja on energia-autonominen. Täten elektroniikkatuotteet voivat kerätä energiaa ympäristöstään ja varastoida sen.

Tämä diplomityö esittelee energiamoduulin, joka kerää energiaa ympäröivästä valosta orgaanisella aurinkokennolla ja varastoi sen elektrolyyttiseen kaksoiskerros kondensaattoriin, joka tunnetaan myös nimellä ultra- tai superkondensaattori. Molemmat komponentit on tehty PE menetelmillä. Nämä komponentit jakavat saman alustan, eli substraatin, ja yhteys näiden komponenttien välillä on tehty silkkipainetulla läpiviennillä, joka on täytetty hopemusteella silkkipainon yhteydessä. Tulostetun läpiviennin tulostettavuutta ja luotettavuutta on arvioitu suoralla silkkipainomenetelmällä sekä syklisellä taivutuskokeella.

Tehtyjen tulosten perusteella voidaan päätellä, että superkondensaattori ja orgaaninen aurinkokenno voivat antaa energiaa pienenergisille IoT laitteille lyhyillä aikaintervalleilla. Energiamoduulin tuotteistamista on arvioitu laajan skaalan rullalta-rulle tuotantolinjalla tässä diplomityössä. Lisäksi diplomityössä on ehdotus energiamoduulin rakenteesta. Silkkipainetun läpiviennin tulostuksessa matalamman viskositeetin hopeamuste ei täyttänyt läpivientiä perusteellisesti. Tämä tulkittiin olevan epäluotettava yhteys substraatin ylä- ja alapuolen sähköisen yhteyden muodostamisessa, sillä ainoastaan läpiviennin seinämissä oli hopeamustetta. Korkeamman viskositeein muste täytti läpiviennin paremmin ja 100 µm läpivientikoolla saavutettiin 100 %:n saanto (n = 1010 läpivientiä) suoralla silkkipainotulostusmenetelmällä. Tällä läpivientipainotekniikalla voidaan tuottaa rullalta-rullalle -painomenetelmällä monikerros PE tuotteita.

PREFACE

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Tampere, 16.03.2018

Manu Kujala

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LIST OF SYMBOLS AND ABBREVIATIONS

4PP	four-point-probe
AC	Activated Carbon
EDLC	Electric Double Layer Capacitor
EHP	Electron-hole -pair
ESR	Equivalent Series Resistance
IoE	Internet of Everything
IoT	Internet of Things
ITO	Indium Tin Oxide
LED	Light Emitting Diode
LPWAN	Low Power Wide Area Network
OPV	Organic Photovoltaic Cell
PCE	Power Conversion Efficiency
PE	Printed Electronics
P3HT:PCBM	poly(3-hexylthiophene):phenyl-C_{61}-butyric acid methyl ester
PEDOT:PSS	poly(3,4-ethylenedioxythiophehe):poly(styrenesulfonate)
PET	Polyethylene Terephthalate
PTAA	Poly(triarylamine)
R2B	Research-to-business
R2R	Roll-to-roll
R&D	Research and development
S2S	Sheet-to-sheet
SEM	Scanning Electron Microscope
TDP	Towards Digital Paradise
TUT	Tampere University of Technology
VTT	Valtion Teknillinen Tutkimuskeskus

ρ	resistivity
ϵ_0	permittivity of vacuum
ϵ_r	relative permittivity
A	Area
C	Capacitance
d	distance
E	Energy
I	Current
$I_{discharge}$	Current used to discharge a supercapacitor
l	length
m	mass
P	Power
R	Resistance
r	radius
R_s	Sheet resistance
t	thickness
V	Voltage
V_{drop}	Voltage drop at the beginning of supercapacitor discharge
W	Width

1. INTRODUCTION

Nowadays electronic devices are gadget centric. A user must have either a mobile phone or a computer in order to be connected to the internet. As the Internet of Things (IoT) comes into reality, a question might arise that is the gadget centric perspective unwieldy in the future. An alternative solution is to have user centric electronic devices, so that the electronics are integrated into surroundings and will be available whenever it is needed. When the electronic devices are integrated into the surroundings, number of the electronic devices will increase drastically. These devices then need to function at low energies and even be energy autonomous, meaning that they can gather energy from their surroundings.

The IoT and Internet of Everything (IoE) are future concepts, where objects have sensors, which collect data to the internet. All devices and even surroundings are then connected to each other with an internet connection. Such as table, coffee machine and clothes can be connected to each other. This interconnectivity will revolutionize the world as we see it, since connection to the internet does not require expensive electronic devices such as mobile phones or computers. However, the IoT is not fully utilized because of privacy and security issues, lack of infrastructure and resources, data integrity and management [1] and environmental issues [2].

Printed electronics (PE) has given enablers to manufacture electronic devices in a low cost and a high-volume way with gravure-, flexo- and screen-printing methods. The fabrication method is additive instead of subtracting, temperature is lower than in conventional silicon based electronics, manufactured devices can be flexible or stretchable and materials used can environmentally friendly. On the other hand, PE currently lacks calculation speed. The benefit that PE can give to future IoT devices is still the use of new materials on various surfaces with fast and high volume fabrication.

1.1 Towards Digital Paradise Project

This thesis is done for a project called Towards Digital Paradise (TDP). The project works in a research-to-business -model (R2B), which creates more user-centric devices rather than gadget-centric and establish then more business cases enabling new markets. TDP is funded through Business Finland.

TDP is divided into three work packages:

- Ecosystem and innovation activities
- Smart South
- **Nearables**

Tampere University of Technology (TUT) contributes into the project by working on the nearables, which are small electronic devices that provide smart surroundings and functionalized surfaces. This thesis introduces an energy harvesting module, which harvests energy from ambient light with an organic photovoltaic (OPV) and stores the energy into an electric double-layer capacitor (EDLC), also known as supercapacitor, for the nearable devices. The end vision is to print the whole energy module monolithically, meaning that the fabrication process is optimized so that the energy module can be printed in one fabrication process. An illustration of the vision is shown in Figure 1.

Figure 1: The vision to print energy module monolithically. Adapted from [3].

The monolithic printing of the energy module is challenging and thus requires well defined materials, fabrication and design. The step before monolithic printing is monolithic integration, where all the components can be printed into one substrate with printed silver lines. The monolithic integration removes unnecessary materials to combine components and increases the total reliability of the device with sophisticated design [4].

1.2 Thesis objectives

The goal of this thesis is to produce steps to fabricate an OPV and supercapacitor combined structure using printed electronics. The goal also includes combining the structures by monolithically printing by roll-to-roll fabrication line. The steps to achieve monolithically printed energy module is evaluated in the thesis. The monolithic printing is separated into four main objectives, which are stated in Table 1.

The Table 1 shows the working order to achieve the final report of the fully printed energy module. However, screen-printed via and its reliability measurement were the main focus of the research and thesis. Other objectives then follow consistently each

other and the wanted report to print monolithically the energy harvesting module is given.

Table 1: Objectives of the monolithically printed energy module.

Objective	Working order
Screen printed through-hole via	1
Screen printed through-hole via and supercapacitor integration	2
Connection of supercapacitor and OPV using a screen printed through-hole via	3
Report on fabrication process of fully monolithically printed energy module	4

Both energy harvest and -storage components of the energy module are manufactured with PE methods and materials. The components share one plastic polyethylene terephthalate (PET) substrate and are electrically connected to each other with silver ink and through-hole via. The electrical interconnection is done by filling the via with conductive silver ink by screen-printing. The screen-printed through-hole via interconnection is researched by finding an optimal solution for via diameter and used ink combination. The interconnection is tested by utilizing a bending reliability test. The first objective is to evaluate the fabrication of through-hole via interconnection with screen-printing.

Second objective is to combine the supercapacitor and screen-printed via into one structure. The supercapacitor stores the energy that comes from the OPV and releases the energy when the nearable device needs it. The supercapacitors working principle, materials, dimensions, energy output and integration with the screen-printed via are presented in the thesis.

At the end, the OPV is integrated into the final structure of supercapacitor and screen-printed via structure and then tested. The OPV's general working principle, architecture, integration to the supercapacitor and screen-printed via is shown in the thesis. A prototype was built by combining a supercapacitor and an OPV into one structure by using the screen-printed vias. The prototype had a simple application, where a light emitting diode (LED) emitted light when supercapacitor was charged by the OPV. The final report to fully print the energy module monolithically is then evaluated as the 4th and final objective of the thesis. A proposal for the energy module design is also given.

The thesis is divided into six parts. The introduction shows the motivation and vision behind the fully printed energy module. After that is more specific literature review on printed- and organic electronics and the energy module component description in chapter two. On chapter three is described all methods, research and materials to fulfill objectives 1-3 in Table 1. Chapter four then shows the test results from the research stated

in section three and finally chapter five gives a proposal structure of the fully monolithically printed energy module. Chapter 6 concludes the thesis by looking back what was done, summarizes the research results and states future work that is needed for the energy module to be used in IoT devices.

2. BACKGROUND: PRINTED AND ORGANIC ELECTRONICS

This chapter introduces the background and theory, which is related to the energy module. First the printed electronics is discussed in chapter 2.1 and then organic electronic components, which are used in the energy module, are discussed in chapter 2.2.

2.1 Printed Electronics

The term printed electronics was used already in the early 1900s, when Thomas Edison demonstrated a way to produce conductors on paper [5]. In 1947 and 1948 Cledo Brunetti and Roger W. Curtis were able to print resistors, capacitors, inductors and their combinations. They described 26 different methods to print circuits and one of the methods was to print conductors using silver paint and traditional newspaper printing approach [6]. The technology here presented is then fairly old, but adapted nowadays as "new", since it was forgotten in the shadow of etching process for a long time. Etching is the most used process to create circuitry. The biggest difference between etching and printing is that printing is additive- and etching subtracting process.

PE has multiple methods to build circuitry by printing onto different substrates. PE requires ink and optimal surface properties of the substrate, so that electrical connectivity is ensured and the ink is spread properly throughout the substrate without leaving pinholes to the wanted pattern. Various kinds of inks and substrates have been produced for PE. A few substrate choices and their suitability for some PE applications are shown in Table 2.

Table 2: Substrate choices for PE and their suitability for some PE applications. "-" represents not recommended option. Adapted from [6].

Application	Glass	Metal	Paper	PET
Organic thin film transistor	Good	Good	-	Good
Organic light emitting diode/ Display	Good	-	Ok	Good
Printed Battery	-	Good	-	Ok
OPV	Ok	Ok	-	Good
Sensor	-	-	Good	Good

PE deliver large variety of new approaches to manufacture electronics. PE can be manufactured by large area, cost-effective and environmentally friendly process creating thin, lightweight, flexible or stretchable devices. Hence, this enables novel applications and markets. However, PE cannot compete with silicon based electronics in terms of

switching speed and high-resolution circuitry. The combination of silicon-based electronics and PE is called hybrid electronics. The interconnection between rigid silicon components and flexible substrates and traces in hybrid electronics are found to be challenging in terms of bendability [7, 8].

Since the PE is opening doors for new markets, it is an interesting area of research for future applications. The IoT and IoE concepts are closer to be accomplished with the manufacturing methods and applications of PE. Other interesting areas are in smart packaging, transparent electronics and wearable electronics. PE manufacturing methods are being used in organic light emitting diodes (OLED), but is also founding its way to automotive, healthcare and consumer electronics [9].

2.1.1 Printing Methods

Printing in general is a transfer process to place ink onto a substrate. Various printing methods for printed electronics are listed in Table 3. The optimal solution for printing technique is chosen for the end application. Options are whether to have a high resolution - low throughput or low resolution - high throughput methods. Thickness of the print varies between different methods. The ink viscosity and inks resistance to flow needs to be also suitable for each technique. A few printing methods and their characteristics in terms of resolution, throughput, print thickness and suitable ink viscosity for the method are listed in Table 3.

Table 3: Printing methods for standard quality production process. Adapted from [6, 9, 10]

Method	**Resolution** (µm)	**Throughput** (m/min)	**Print thickness** (µm)	**Ink viscosity** (cP)
Screen printing	50 - 100	70	5-100	500-5000
Gravure printing	10 - 50	1000	1	100-1000
Flexographic printing	40 - 100	500	>1	50-500
Offset printing	10 - 50	1000	10	100-10 000
Inkjet printing	20 - 100	10	1	10-20

Most simple methods are screen- and inkjet printing. Screen-printing pushes the ink through a mesh to a substrate with a squeegee shown in Figure 2. Another method, which highly resembles the screen-printing method, is stencil printing. The main difference between stencil- and screen-printing is that in stencil printing the print mask touches the substrate all the time during printing and the stencil does not necessarily require a mesh. Stencil printing is beneficial for low resolution prints and inks that tend to dry in ambient air, since the screen printers screen mesh gets clogged easily.

The throughput with screen-printing is high, but the resolution can be lower than other methods. Better resolution is achieved with inkjet printing technique, which is a digital

fabrication technique to drop droplets of ink to the substrate by demand. Inkjet printing pattern is all computer controllable while screen-printed pattern can be changed by changing the screen mask. Inkjet printing uses low viscosity inks, which are more thinner inks than high viscosity ink pastes.

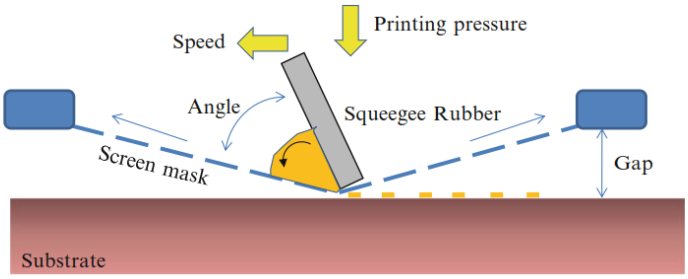


Figure 2: Screen-printing technique [10].

Other common techniques are gravure-, flexo- and offset printing, which are more sophisticated techniques. They are operated in very high throughput sheet-to-sheet (S2S) or roll-to-roll (R2R) large area applications. In gravure printing, a gravure cylinder spins and gathers ink from an ink bath reservoir to the engraved areas of the cylinder. Then impression cylinder transfers a substrate next to gravure cylinder, which pushes the ink from the ink filled engraved areas to the substrate. Gravure printing is shown in Figure 3.

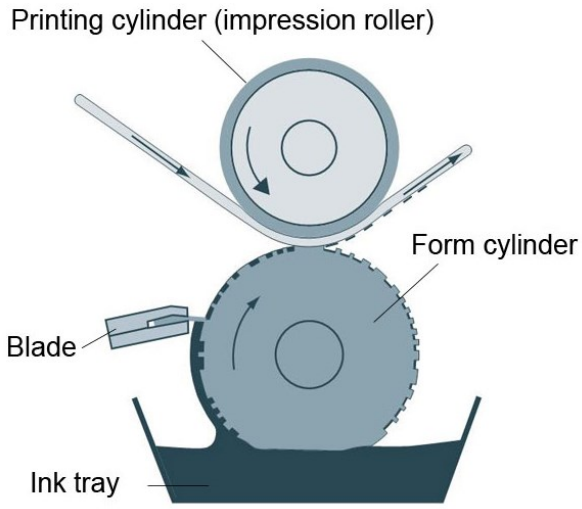


Figure 3: Gravure printing [11].

Other highly used method is the flexographic printing, which resembles highly the gravure printing method. The main difference between these two methods is that gravure printer's pattern roll has the wanted pattern embedded into the roll and flexographic printer's pattern roll has the pattern on the outside of the pattern roll. Flexographic printing is shown in Figure 4.

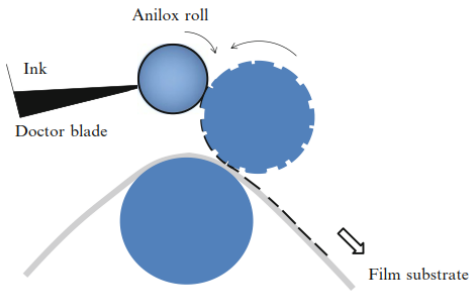


Figure 4: Flexographic printing [10].

Gravure printing uses higher pressure to transfer ink to the substrate. It is more suitable for high viscosity inks as seen from Table 3. Flexographic printing uses lower pressure and is then more suitable for low viscosity inks. With flexographic printing, the print thickness tends to get low because of low ink viscosity.

Other highly used method is the slot-die coating, where a micrometer thick film can be deposited onto the substrate with a die. The die is very precise since the thickness of the coating needs to be uniform. Slot-die coating is also a high throughput and cost-effective way to print in the R2R process [12].

2.1.2 Materials

Various inks and substrates are used in PE. The ink used can be a conductor, semiconductor or insulator. Some widely used substrates were pointed out in Table 2, but Table 4 lists a few ink materials and their cost, conductivity, flexibility and printability are compared. The poly(3,4-ethylenedioxythiophehe):poly(styrenesulfonate) (PEDOT:PSS) material is further introduced in section 2.2.2.

Table 4: Materials and inks used in PE. Adapted from [6].

Material & Inks	Costs	Conductivity	Flexibility	Printability
Gold inks	++++	+++	++	+++
Silver inks	+++	+++	++	+++
Copper inks	++	++	++	++
Graphite inks	+	+++	+++	+++
PEDOT:PSS	++	+	++++	++

The inks for printed electronics can be then any common conductive metal from copper, silver or gold. Other materials can be for example organic of coil based. Copper is very sensible to oxidize in atmosphere and requires special treatment to use it in PE. Silver inks are more common in printed electronics because of their antimicrobial properties and well-known manufacturing process [10].

The inks are produced first by having the metals as nanoparticles and mixing them with a solvent. The solvents effect highly on the properties of the inks viscosity, which further effects on printing and the suitable method to use. The metal particles can be flakes, sheets or nanowires, which all effect on the conductivity of the ink [10]. In this thesis, the inks that are used to fill a through-hole via are silver flake inks with different properties. The inks used in the thesis are introduced in Table 5.

Table 5: Two different inks introduced to fill the laser cut vias [13, 14].

Ink	**Viscosity** (cP)	**Silver content** (%)	**Solvent**	**Sheet resistance** (mΩ/□)	**Line thickness** (µm)
Asahi LS411AW	20 000 – 30 000	75-78	Butyl cellosolve acetate, Isophorone	<40	10
DuPont 5064H	10 000 – 20 000	63-66	C11 -ketone	<14	25

The conductivity of the ink is a basic value, which defines how well the electricity flows in the conductor line. Ohm's law defines resistance as

$$R = \frac{U}{I}, \tag{1}$$

where R is the resistance in ohms, U is the voltage difference between conductor line in volts and I is the current supplied to the conductor in amperes [15]. Resistance of any conductor line is calculated by

$$R = \frac{\rho l}{Wt}, \tag{2}$$

where ρ is the material resistivity and l is the length, W is width and t is the thickness of the conductor. Sheet resistance is calculated by

$$R_s = \frac{\rho}{t}, \tag{3}$$

Where R_s is the sheet resistance in ohm/square, ρ is the resistivity and t is the thickness of the material [16]. Sheet resistance is dependent on the dimensions of the conductor line and is easy to measure with a four point probe (4PP) technique. The conductivity of a material is usually given in siemens per meter, which is a reciprocal for resistivity. The resistivity is bound to the material conductivity, resistance is the cause of resistivity and sheet resistance is more related to thin film conductors, such as printed conductor lines.

The two inks in Table 5 have slightly different conductivity values. When the resistivity value is lower, the better the conductivity. The resistivity can be calculated for the inks

stated in Table 5 with equation (3). The resistivity values are $4*10^{-7}$ Ωm for 40 µm line thickness and $3{,}5*10^{-7}$ Ωm for 25 µm line thickness for Asahi and DuPont inks respectively . The DuPont ink has larger flake particles, which results to a better conductivity [17]. The sheet resistances of the two inks were measured and calculated with the 4PP - method in section 4.1.2.

Other important factors of the ink are its flexibility and stress durability since they are printed on thin substrates, which are easy to bend. The research area is fairly new and there is no clear standard to measure the inks stress durability. However, many studies have been made in this research topic. Some guidelines are also done to measure the flexibility of inks and standard proposals are in the process [8, 17-20].

In this thesis, the flexibility of a through-hole via is studied. Flexibility is combined with a quantity called strain, which describes the physical deformation of a shape. The strain is a unitless quantity and can be calculated by dividing the starting dimensions of a shape with the dimension change. The deformations of a shape causes crack formation in the printed line and interfacial delamination between substrate and the printed line. When a device is bent, two sides of the substrate face different bending strain. The outer side of the substrate faces tensile stress and the inner side faces compressive stress [21]. An illustration of a thin film bending is shown in Figure 5.

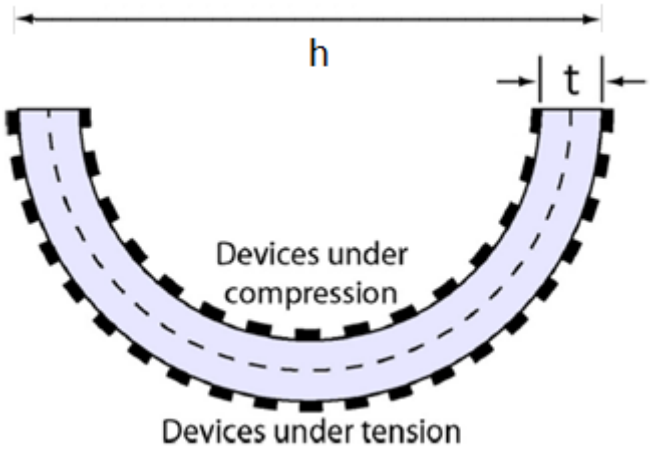


Figure 5: Flexible substrate bent. Devices under compressive and tensile stress [21].

In Figure 5, the symbol *t* represents thickness of the substrate and *h* represents the bending diameter. The dashed line in the middle of the substrate represents a mechanically neutral plane, where the material does not face tensile nor compressive stress. The biggest strains occur at the surfaces of the bent line, resulting more strain to thicker substrates and line thicknesses. Compressive and tensile stress leads to the ink delamination from the substrate and form cracks to the ink. These effects causes conductor line's resistance to rise under cyclic bending [17, 21].

2.1.3 Multi-layered structures

PE can be a high-volume way to produce electronics, but the resolution of stays relatively low in high volume manufacture. It is then beneficial to use stacked structures to save space. More importantly, printing different material layers on top of each other can utilize new devices. For example, the OPV is a multi-layered structure.

A multi-layered structure can also done by using both sides of the substrate. This requires an electrical connection between them, which is made with a through-hole via. In flexible circuits, the through-hole is mainly done by mechanical punching or laser cutting and can be as small as 25 – 50 µm sized [6].

After the hole formation, the hole is filled with conductive ink or -adhesive. After the via filling, rest of the circuit is printed on both sides of the substrate [22, 23]. The via can also be filled in the printing process. This method does not create as reliable results, since the ink only covers sidewalls of the via and leaves airlocks trapped inside the via as seen in Figure 6 from the work of Shi *et. al* [22].

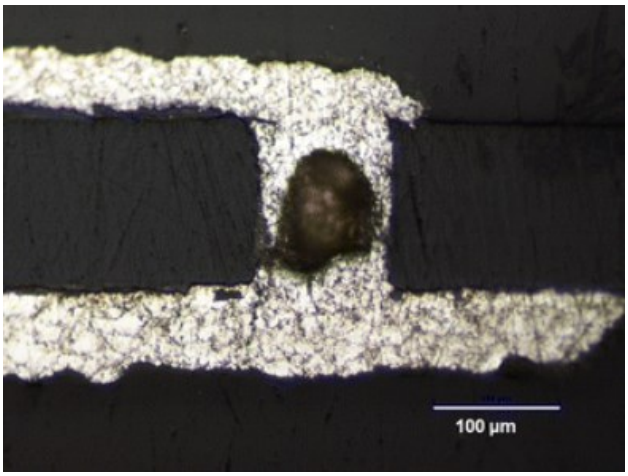


Figure 6: Cross section image of an interconnection between top and bottom of substrate. Via was done by punching and via was filled in the printing process [22].

Some research has been made to investigate the through-hole via bending. Since the substrate has a mechanically neutral plane on the middle, the ink inside the through hole does not face a remarkable stress. The stress hotspots gather on the via edge as seen in Figure 7, where the via bending is modelled.

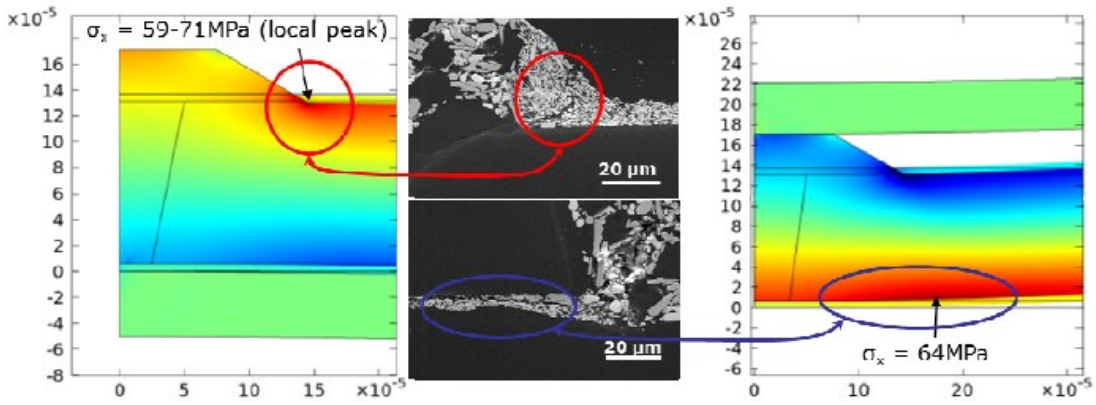


Figure 7: Modelling of the through hole via bending. On the left, the via is bent downwards and on the right, the via is bent upwards [23].

In this thesis, the bending stress of a via was investigated with a printed conductor line, which goes on top and bottom of the substrate. The interconnection was made with the through-hole vias filled with silver ink. The printed conductor line is also called as a daisy-chain structure. The daisy-chain structure was then compared to a reference line, which was printed on one side of the substrate and did not have through-hole vias. Both tensile and compressive stressed reference lines were compared to the daisy-chain structure and an estimation of the effect of via bending is evaluated.

2.2 Organic Electronics

Organic materials provide new semiconductor types. The organic semiconductors can be formulated into inks, which are printed on almost any kind of substrate. For example functional transistors have been produced by printing and enables to create analog or digital circuits [12]. Most used organic semiconductor application is the organic light emitting diode, which is used in the newest mobile phone displays because of its high resolution and lower energy consumption. The next chapter introduces three other organic electronics applications: supercapacitor, OPV and printed diode, which are used in the energy module.

2.2.1 Supercapacitor

Most electronic devices run with energy that comes from a battery. One battery consists at least from two electrodes and an electrolyte, what is called an electrochemical cell. Usually a battery has multiple cells. Two electrodes generate potential asymmetry in aqueous electrolyte, also known as electromotive force. Current is then created to the load by this electromotive force. At the end, electrons travel from the other electrode to another through the load and redox reactions occur in the electrodes. To summarize, battery creates energy by chemical redox reactions. After the cells are in their electrochemical equilibrium, the redox reactions stop [24].

Batteries are categorized into primary and secondary batteries. Secondary batteries can be recharged while primary batteries cannot. Batteries can give a lot of energy despite their small size. Recharging the secondary battery can take from minutes to hours. Redox reactions erode battery's electrodes slowly and thus limits the amount of times that the battery can be recharged. The amount of times battery can be used and recharged before its capacity is weakened is called cycle life [24].

Capacitors on the other hand use a different energy storing principle than electrochemical reactions. The capacitor has also at least two electrodes and it stores energy into an electric field between the electrodes, which can be two solid metal plates facing each other. Electric field is generated if the plates are in different voltage potential. This can be achieved by charging the plates [25].

Capacitor is a passive and cheap energy-storing component. The capacitor can store an electric charge between its plates. The energy storing phenomenon is also called capacitance. Capacitance between two plates is calculated by

$$C = \epsilon_0 \epsilon_r \frac{A}{d}, \tag{4}$$

where C is capacitance, ϵ_0 is permittivity of vacuum (8,85 * 10^{-12} F/m), ϵ_r is relative permittivity of dielectric material between plates, A is the area of the plates facing each other and d is the distance between plates. Capacitance's unit is Farad. The energy that capacitor can store is calculated as

$$E = \frac{1}{2} C V^2, \tag{5}$$

where E is the energy in Joules, C is capacitance and V is voltage difference between plates. Unfortunately, capacitors cannot store as much energy as batteries since dielectric material between the plates have voltage restrictions and capacitance is small due to the area limitations set by equation 1. Capacitors are not used as a primary energy source in most cases [25].

As can be seen from equations 1 and 2, the energy that a capacitor can store is relative to plate distance and the area of the plates. Electrolytic double layer capacitor (EDLC), also known as supercapacitor, has a large plate area and very small distance between plates. The supercapacitor uses ion liquid as electrolyte and porous materials as electrodes. Ions then organize themselves near to the porous electrode at distance below nanometers. As the electrode is porous, ions can penetrate to the smallest pores of the electrode. The EDLC structure is demonstrated in Figure 8.

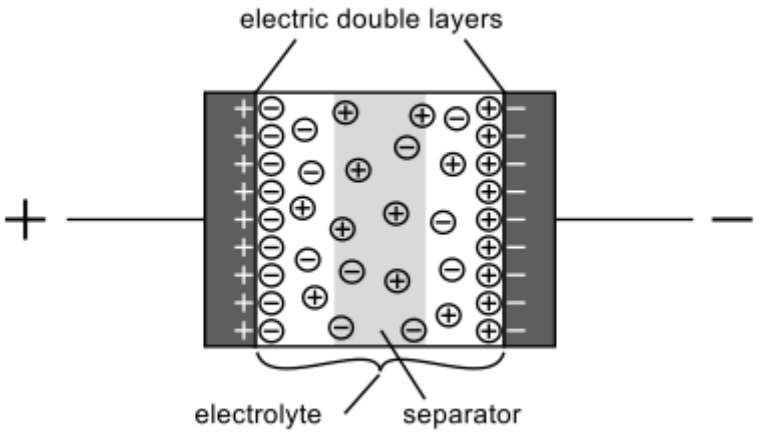


Figure 8: Electrolytic double layer capacitor layout [26].

It can be seen from Figure 8 that one supercapacitor structure creates two capacitors in series, one in the negatively charged electrode and positively charged cations and another in the positively charged electrode and negatively charged anions. This reduces the total capacitance of the EDLC by formula

$$C_{EDLC} = \frac{C_1 C_2}{C_1 + C_2}, \tag{6}$$

where C_{EDLC} is the total capacitance of the supercapacitor, C_1 is the capacitance formed by the other electrodes and anions and C_2 is the capacitance formed by the second electrodes and cations. Even though the whole capacitance is reduced because of this two in series connected capacitor nature, normal supercapacitor has capacitance values up to 10 000 times larger than conventional capacitors described previously. Supercapacitors have better cycle life than batteries, since they don't depend on chemical reactions, and can be charged faster than batteries. On the contrary, batteries have higher specific energy values. Batteries and supercapacitors are often used together as a hybrid component for example to increase cycle life or efficiency [27].

Supercapacitors have been used in some applications as primary energy source for example in a bus [28]. Supercapacitors can be charged fast and they can be built on flexible substrates and from environmentally friendly materials such as carbon and salt water. When the organic photovoltaic cell is combined with the supercapacitor, they can provide enough energy for an energy autonomous device [29]. These are the main benefits of supercapacitor components compared to batteries. Supercapacitors are then promising solution for IoE -applications.

As do capacitors dielectric material have voltage restrictions, so does Supercapacitors have voltage restrictions caused by the electrolyte. It is an aqueous or organic liquid, where the ions move freely in the solvent. When voltage is applied between the elec-

trodes, ions organize themselves near to the electrode material forming a capacitor. Supercapacitors can be made environmentally friendly with low cost by using water based electrolytes. However, the can be used only at maximum of 1,23 V, since water molecules start to split at voltages over 1,23 V. Other solutions are organic and ionic liquids which can go to 2,7 V and 4 V respectively. Although, organic and ionic liquids are not as environmentally friendly as water based electrolytes. They also have higher manufacturing costs compared to water based electrolytes [27]. Other studies have shown that supercapacitors with water-based electrolytes can be used in energy harvesting applications [26]. For this module, the low-cost fabrication and environmentally friendly materials were the main criteria, so the electrolyte was chosen to be water-based.

The electrolyte used in this thesis' supercapacitors is water-based. Metal electrode corrodes slowly in the water-based electrolyte. Other electrode material choices organic inks such as carbon inks. Most common electrode for supercapacitors are activated carbons (AC), because it is highly porous and thus has high surface area and is highly conductive [27]. For this module, AC was also used for electrode material. For the measuring point of view, AC is brittle and will be cracked when measurement alligator clips are attached onto it. A current collector material, graphite, is then printed beneath the AC. A separator, that prevents short circuit between electrodes, can be any paper, where ions can pass through the separator. An illustration of the supercapacitor structure utilized in this thesis is shown in Figure 9.

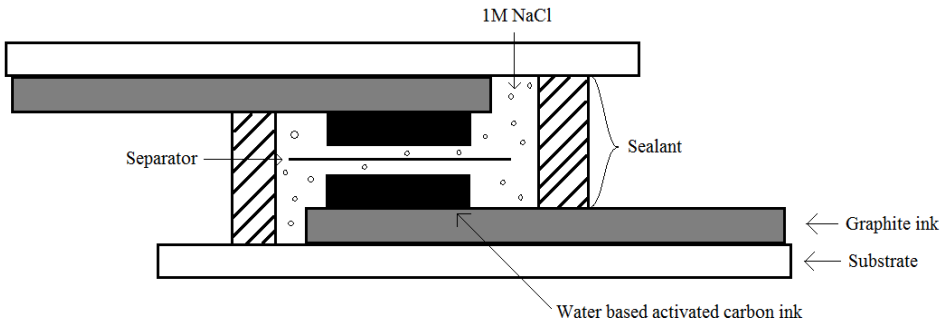


Figure 9: Supercapacitor structure.

Some low energy microcontrollers can be powered up with the supercapacitor. A few low energy Bluetooth controllers, which are high energy demand components, are listed in Table 6. Other extremely low energy consumption microcontrollers, which can be used in autonomous sensors, are shown in Table 7. The Table 6 and Table 7 components are meant for IoT applications and can be used in low power wide area network (LPWAN), which is the area network used in IoT [30]. Finland started building the LPWANs on 2016 and now a few base stations have been produced in the metropolitan area [31].

Table 6: Low energy Bluetooth microcontrollers.

Name	Operating Voltage	Current (Average)	Ref
nRF8001	1.9V - 3.6V	9µA sleep 12.8mA Active	[32]
QN9022	1.8V - 3.6V	3µA sleep 9.25mA Read	[33]
nRF52832	1.7V - 3.6V	5.3mA Transmit 5.4mA Read	[34]
nRF51422	1.8 V - 3.6 V	6.3mA Transmit 9.7mA Read	[35]

Table 7: Low energy microcontrollers for autonomous sensing. Adapted from [36].

Name	Operating voltage	Current (Average)	Ref
TI, MSP430x11x2	1.8 – 3.6V	0,1µA sleep 200µA Active	[37]
Atmel, AT-tiny24A	1,8 – 5,5V	0,1µA sleep 210µA Active	[38]
Microchip, PIC16LF72X	1.8 – 3.6V	0.02µA Sleep 110µA Active	[39]

The operating voltages that the Table 6 and Table 7 microcontrollers use are from 1,7V to 3,6V. The maximum operating voltage of the water-based supercapacitors can be raised by putting the supercapacitors in series. However, this will lower the whole capacitance by formula

$$\frac{1}{C_{whole}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_N}, \tag{8}$$

where C_{whole} is the total capacitance of the capacitors in series and C_1 to C_N are individual supercapacitors in the series structure. However, the voltage does not divide equally amongst the capacitors in series if the capacitance values vary in the series structure. In this case the voltage over one individual capacitor can rise over 1,23 V and create overvoltage, if the capacitors are not identical. Maximum number of capacitors in this study is restricted to three in series to ensure safe operating voltage window for the supercapacitors.

Supercapacitor is not an ideal component and has a lot of losses. Most critical losses are the equivalent series resistance (ESR) and current leakage. The ESR creates voltage losses by equation (1). Most of the ESR comes from the current collector material. In

this case it is the graphite ink. The ESR can be calculated for the graphite layer with equation (2) and (3), if the sheet resistance is measured and dimensions of the current collector are known. The ESR can also be measured from the supercapacitor by charging it to a certain value and then discharging it with a specific current. In the beginning of supercapacitor discharge a voltage drop occurs. The ESR is calculated by

$$ESR = \frac{V_{drop}}{I_{discharge}}, \tag{9}$$

where *ESR* is the equivalent series resistance, V_{drop} is the voltage drop in the beginning of discharge and $I_{discharge}$ is the used current to discharge the supercapacitor [27].

The other main loss factor is the current leakage, where the supercapacitor discharges itself spontaneously. The current leakage comes from overcharging the electrolyte material, impurities in the electrolyte or leakage pathways, which are mainly caused by poor sealing of the supercapacitor [27]. The fabricated supercapacitors capacitance, ESR and current leakage were measured in this thesis.

2.2.2 Organic solar cell

A solar cell can convert light to electrical energy by capturing the energy from light photons and turning them to electron-hole -pairs (EHP), which are further separated to charge carriers. The charge carriers then create electrical energy. The EHP formation is called photovoltaic effect. Solar cells created current and voltage depend on the energy of the photon (wavelength) and photon quantity creating EHPs (light intensity) [40].

The materials for solar cells can be inorganic or organic. Inorganic solar cells are usually made from highly purified crystalline silicon, which is a rigid solid-state material. The organic materials can be printed on flexible substrates making the whole solar cell flexible. The organic semiconductor materials for OPVs are mainly polymers. A solar cell, that has both inorganic and organic materials, is called a hybrid solar cell [40].

The manufacturing of crystalline silicon has a high carbon footprint and requires high temperatures. Organic semiconductor materials compete with their low temperature printing process, which is roll-to-roll compatible. OPVs are then intriguing option for energy harvesting devices. However, the power conversion efficiency (PCE) from light to electrical energy is much lower with OPVs compared to inorganic solar cells. Other limiting factors of OPVs are their materials sensitivity to water, oxygen, high temperature and light. These environmental factors limit the lifetime of OPVs [12, 40].

The most common OPV architecture is called bulk heterojunction, which has usually five different functional interfacial layers: anode and cathode, electron- and hole transport layers and donor/acceptor material mixture layer. A planar heterojunction

OPV has the donor and acceptor materials as separate layers [12]. The bulk heterojunction architecture is shown in Figure 10 with materials that are used in this thesis. The anode in this case is silver, cathode indium tin oxide (ITO), electron transport layer Zinc oxide (ZnO) hole transport layer PEDOT:PSS and donor acceptor material poly(3-hexylthiophene): phenyl-C_{61}-butyric acid methyl ester (P3HT:PCBM).

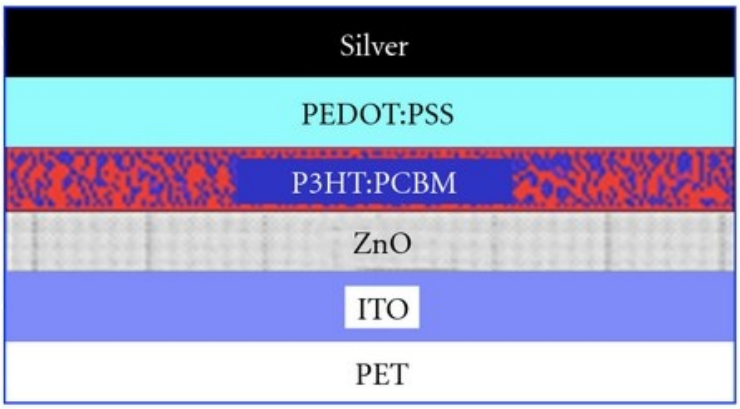


Figure 10: Inverted OPV architecture with commonly used active layer and charge transport layers [41].

When light is introduced to P3HT:PCBM, photons are absorbed and excitons are generated. Excitons are bound EHPs. Excitons then separate into charge carriers and travel whether through hole or electron transport layer into the electrodes of the solar cell. Charge carriers finally create the electrical energy [12]. All the functional interfacial layers of the OPV seen in Figure 10 can be printed by R2R printing methods. The PCE of R2R screen- and gravure printed OPV can be 2% and slot-die coated over 5% [42-44].

2.2.3 Printed diode

A diode is a component which passes the current mainly on one direction. The diode has two terminals, anode and cathode, and the current flows only from anode to cathode, unless the breakthrough voltage of the diode is exceeded. Different kind of diodes are available for different applications, for example zener, pin and varactor diodes [45]. The diode component is essential for the energy module, since the supercapacitor can discharge itself through the OPV, if the current is not blocked. Then the diode must be placed so, that the current flows only from the OPV to the supercapacitor is blocked in the other direction.

The diode used for the energy module prototype in this thesis is a through-hole 1N4148 diode component. The threshold voltage of the diode is 0,7 V, which means the lowest amount of voltage before the diode is conducting [46]. The threshold voltage varies between different diodes and materials.

Although the diode was chosen to be a through-hole component, the diode should be printed for the energy module in order to achieve the final vision goal stated in the introduction all printed energy module. Organic and printed diodes have been researched and more well understood for the past 20 years and various architectures to perform a working diode has been made [47]. Screen and gravure printed components have also been utilized [48, 49].

For simplification, in schottky diodes a semiconductor material is printed between two metal inks. The metals act as anode and cathode. The metal and semiconductor interface is either blocking or conducting based on the charge flow direction. This is caused by the different energy levels of metal and semiconductor materials [50].

A well working printed diode is created with copper and silver metals and poly(triarylamine) (PTAA) organic semiconductor. An illustration of the printed diode is shown in Figure 11.

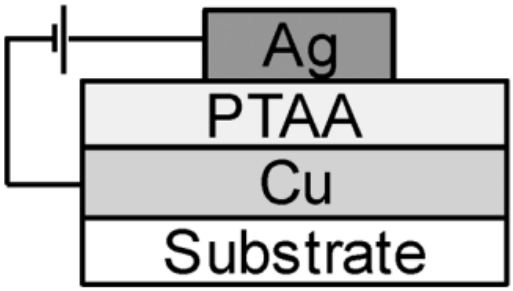


Figure 11: Printed diode structure [51].

The architecture in Figure 11 can be used in the energy module. However, the leakage current from cathode to anode of the copper-PTAA-silver –diode is relatively high compared to the 1N4148 diode. The printed diode has a leakage of 30 $\mu A/cm^2$ at 5 V and 1N4148 has 25 nA at 20 V [46, 48]. The OPV open circuit voltage then needs to be adjusted appropriately for the final energy module structure.

3. METHODS

As stated in the introduction, the goal of this thesis is to produce steps to fabricate an OPV and supercapacitor combined structure using printed electronics. The goal also includes combining the structures by monolithically printing by roll-to-roll fabrication line. In the energy module both sides of the substrate are used. This includes doing a through-hole via to the substrate and creating circuitry to both sides of the substrate with conductive ink. The through-hole printed via's fabrication and reliability is then investigated and analyzed. The proof of principle is done with the supercapacitor and through-hole via combined structure and is being evaluated. After the proof of principle, a prototype was made to evaluate the combined structure performance. This chapter introduces the equipment and methods that were used in the measurements and evaluation.

3.1 Printed through-hole via

To be able to form monolithically printed systems on R2R process, via filling with ink is important to be able to use both sides of the substrate. The trough-hole vias' reliability were investigated to create monolithically printed systems. Other screen-printed and micropipette via filling of the through-hole via on flexible substrate has been investigated in previous studies [22, 52]. Shi *et al.* have studied direct screen print filling of via. Challenges in this study was found out to be the uniformity of the printed area and airlocks inside the via seen in Figure 6. Airlocks were eliminated by filling vias and printing traces of wanted circuit separately [22].

In this study, a printed daisy chain structure was designed. A direct screen printing approach was utilized, which filled the vias with ink during the print process. Commercially available inks Asahi LS-411AW silver paste and DuPont 5064H silver ink were used as the conductive trace material, which are introduced in Table 5, and 125 µm thick Melinex ST506 PET as the substrate. Through-hole vias were cut with a laser beam by Ekspla Atlantic, DPL 015 3 –laser in VTT premises. The laser wavelength was 355 nm, pulse duration 9 ps, repetition range 100 kHz - 500 kHz with 8 W max beam power. The laser's scanner head used was galvanometer driven laser scanning mirror Intelli SCAN III14. Different via sizes were investigated and their reliability to bending stress with a bending test. Other similar bending tests have been made by Péter *et al.* with through-hole vias that were produced by printing vias with isotropic conductive adhesive and then print conductive traces with silver ink on both sides of the substrate separately [23].

3.1.1 Via fabrication

Nominal via sizes that were cut to the substrate by the laser beam were 50 µm, 100 µm, 150 µm and 200 µm. All substrates were put into an ultrasonic bath for 20 - 30 min to remove residual substrate from the corners of the via that were formed by the laser beam. After the sonication, all substrates were characterized with an optical microscope.

3.1.2 Test structure

A specific test structure was designed with PADS logic and -layout software programs to measure the bending reliability of the screen-printed vias. The test structure is a daisy-chain structure, where a 400 µm width conductor line passes on both sides of the substrate. The printed silver diameter around the via is 2000 µm. A reference line is also printed on the test structure to eliminate the conductor bending from via bending from the data. The reference line is printed only on one side of the substrate and does not have through-hole vias in the structure. The test structure is shown in Figure 12.

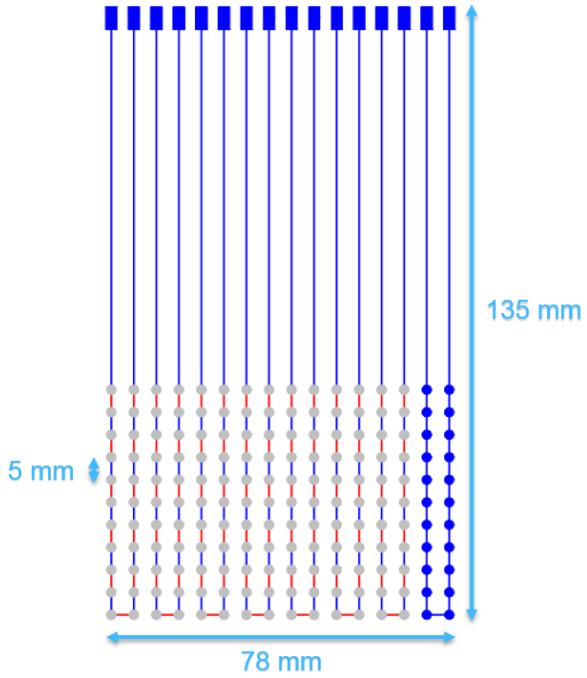


Figure 12: Via bending test structure with dimensions. Top side print is marked as blue, bottom side print is marked as red. Grey indicates via collar and is printed on both sides.

As seen from Figure 12, the collar size of via is much larger than the conductor line. This was to ease screen-printing alignment, since it was done manually and the accuracy of screen-printing is ±500 µm. Seven daisy-chain structures were printed in total to the substrate and one printed as a reference. Seven 22 via daisy-chain structure lines were printed into one sample substrate.

The screens also had a sample structure, with printed current collector, to combine a supercapacitor and screen-printed via. The supercapacitor's current collector (graphite) was printed on top of a silver pad, which was connected to the screen-printed via. Combination with via structure is shown in Figure 13.

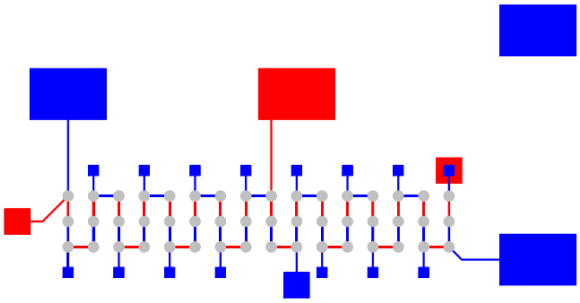


Figure 13: Supercapacitor combination with via structure.

The printed structure had four 4PP printed structure in both sides for sheet resistance measurements and alignment crosses in three corners of the substrate. Used screen designs are shown in Figure 15.

3.1.3 Printing

A direct screen printing approach was utilized to fill the vias with ink during the print process. Semi-automatic screen printer (TICSFC 300 DE screen printer from Eickmeyer) was used to print on the laser cut substrates. The screen printer is shown in Figure 14. Squeegee's pressure, mask height and alignment can be adjusted on the printer manually. A screen print mask UX79-45 with an aluminum frame was used and ordered from Finnseri Oy. The screen material is a super high modulus polyester monofilament with 79 mesh count per centimeter and 68 µm mesh thickness. The mask is both water- and solvent resistant [53].

Two screens were then used both top and bottom sides of the substrate and they were printed separately. The filling of the via was done during the printing process. First the top side of the pattern was printed shown in Figure 15 A and then sintered in 150°C for 20 minutes with Asahi ink and 130°C for 20 minutes with DuPont ink. Both inks were sintered in an oven. Subsequently, the bottom side of the pattern was printed shown in Figure 15 B and sintered in the same conditions as the top print.

After printing both sides of the substrate, an optical characterization was done to determine the optimal via size and via filling rate. Before and after bending analyses were made to the vias. The 4PP structures were used to determine ink's sheet resistance, since top and bottom prints of the substrate faced different sintering conditions. Top print is sintered two times and bottom print only once.

Different variables in the printing process were the used ink and through-hole via's diameter. Different samples are listed in Table 8.

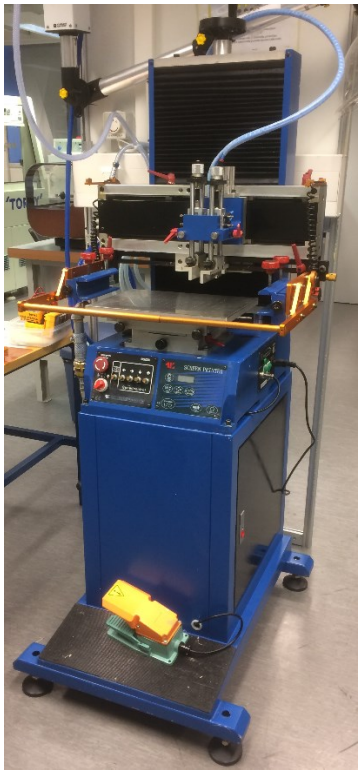


Figure 14: Semi-automatic screen printer.

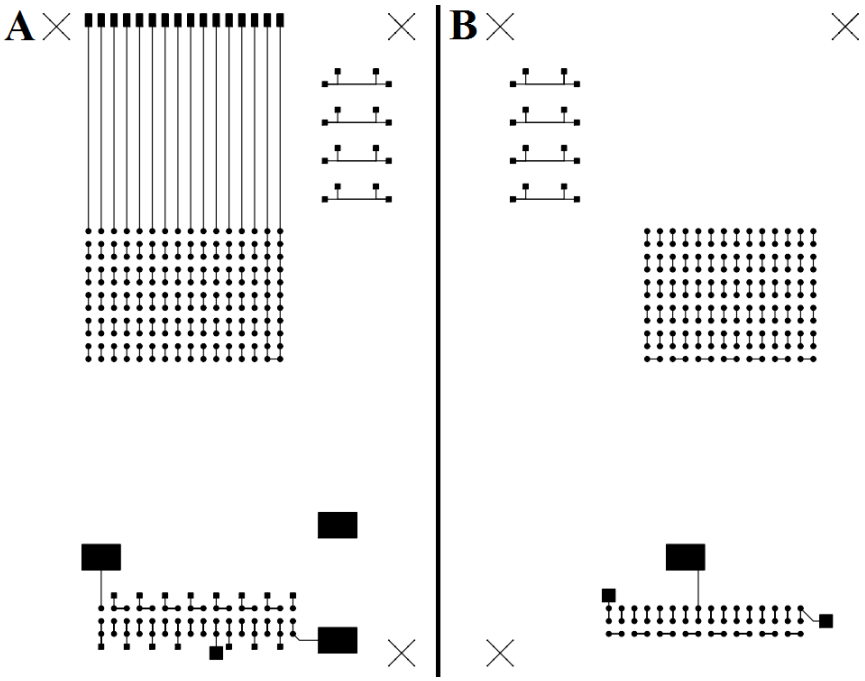


Figure 15: Mask A for top print of the substrate and mask B for bottom print of the substrate.

Table 8: Sample chart.

Via size	Ink	Samples printed	Number of vias printed
50µm	Asahi LS411AW	5	1010
100µm	Asahi LS411AW	5	1010
150µm	Asahi LS411AW	5	1010
200µm	Asahi LS411AW	5	1010
50µm	DuPont 5064H	8	1616
100µm	DuPont 5064H	8	1616
150µm	DuPont 5064H	7	1414
200µm	DuPont 5064H	5	1010

Total number of 48 samples were made to evaluate the filling of the via with different via sizes different inks. One sample substrate had in total 202 printed vias. Ink conductivity was measured with a 4PP method. Conductivity was evaluated from eight 4PP patterns, four printed to top side of substrate and other four to the bottom of the substrate. Top and bottom ink conductivity was then evaluated.

3.1.4 Via characterization

Microscope images were taken from the laser cut vias from top and bottom of the substrate before printing. Via size was measured by fitting a line in the microscope image from bottom left corner of the via to the upper right corner of the via. Measurement line fitting is shown in Figure 16.

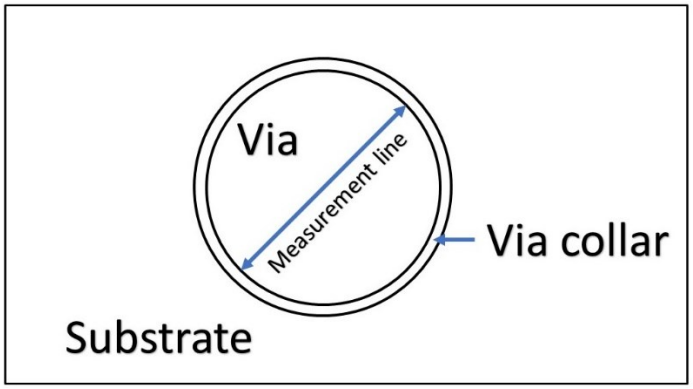


Figure 16: Via size measurement method explanatory image. Images were taken with a microscope at 20x magnification.

A cross-section microscope images of the vias were taken to evaluate the filling of the via with ink. The substrates were carefully cut with scissors through the via and placed on to the microscope platform. Another cross section was also taken for high quality inspection of the filling by setting a sample of the printed via structure to a resin mold. The mold was grinded to a point, where a cross section was visible from the sample.

Only a few images from one sample was taken with the current method. The mold and grind -approach could not be used with the smallest, 50 µm, via size. The 50 µm samples were sent to Top Analytica, where the sample was cross cut with a broad ion beam.

The resistance of the screen-printed through-hole vias were electrically characterized with a multimeter to determine their connectivity. The resistance of the via was measured to ensure connection from top to bottom of the substrate. The vias were characterized as pass, poor or failed via. The categorization of via based on its resistance is shown in Table 9.

Table 9: Characterization of vias by their electrical conductivity.

Grade	Criteria
Pass via	< 1 Ω
Poor via	1 Ω < via resistance < 10 Ω
Failed via	> 10 Ω or no connection

3.1.5 Ink characterization

The printed ink was characterized electrically by measuring the sheet resistance of the 4PP pattern with a Keithley 2425 source meter. Four probes were carefully dropped onto the pattern, where two of the probes fed current to the printed line and two of the probes measured voltage. 10 mA current was used to determine the sheet resistance.

The used 4PP pattern is shown in Figure 15 mask. On both sides of the substrate four 4PP patterns were printed and an average from them was taken. The measured 4PP's line width and length were 0,4 cm and 1,5 cm respectively. The sheet resistance of the line was calculated by using formulas (1), (2) and (3). The sheet resistance was then calculated by

$$R_s = \left(\frac{V}{I} / \frac{W}{l}\right) \tag{10}$$

where R_s is the sheet resistance, I is the current fed to the conductor line, which was 10 mA, V is the measured voltage of the conductor line, W is the width and l is the length of the conductor line, which were 0,4 cm and 1,5 cm respectively. In the sheet resistance measurement, voltage was measured and formula (10) was used to determine the sheet resistance value.

3.1.6 Cyclic bending test

A bending test was then engaged when the vias were characterized. Since the PE bending reliability is a novel research area, there has not been developed a standard to do a bending test for these kinds of structures. In earlier research, the bending apparatus is

custom built. The basic principle is to plot either bending cycles and the performance of the device under stress, for example time that the sample is under bending stress, or bending stress and resistance. Both before and after measurement bending measurements or continuous measurement while bending has been done [17, 54].

In the reliability measurements, samples were placed on a custom made pneumatically controlled bending machine. Machine has two parallel plates and the upper moving plate bends the sample that is attached. The distance between plates varied between tests from 2 cm to 1 cm. The bending device and measurement setup is shown in Figure 17. The test apparatus has been used in other cyclic bending reliability measurement setups [55].

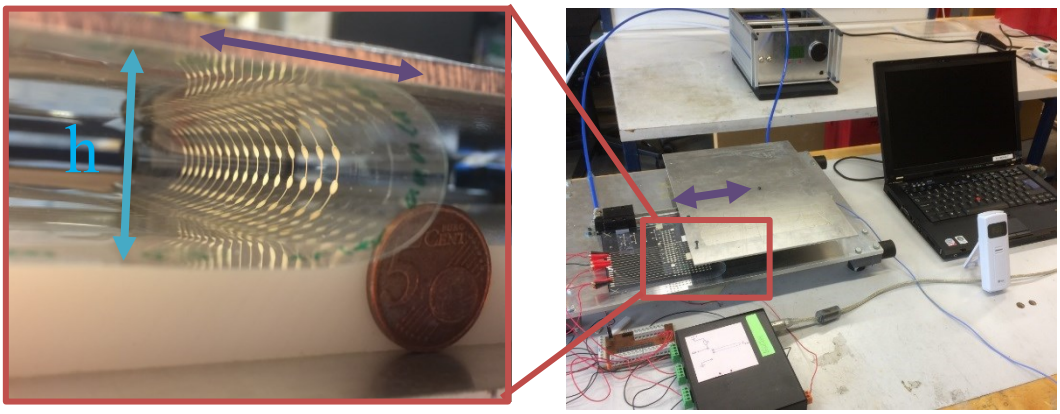


Figure 17: Bending test setup on the right and zoomed in image of sample being bent on the left. The symbol h represents the bending diameter, which is constant during the measurement. The purple line represents the back and forth -movement of the upper plate.

An iCraft AD-converter and iPlotter software were used to convert bend cycle and resistance reading into a same chart. Resistance was calculated by feeding 4,92 V voltage across a 1 kΩ pull up resistor and the sample line. The sample line's voltage was measured and calculated with voltage division. The device collected voltage reading into a conventional computer with 9,2 Hz sampling rate at maximum.

Different samples were measured in the cyclic bending test. All different samples are shown in Table 8. Three daisy-chain structures were measured along with one reference sample to eliminate micro crack effect in the silver lines from the possible deformations on the via. Various tests were made to the printed structures and are shown in Table 10, Table 11 and Table 12.

Table 10: Performed bending tests to evaluate via sizes and inks.

Ink	Via size (µm)	Bending cycles	Plate distance (cm)	Notes
Asahi	50	30 000	2	Reference compress stressed
Asahi	100	30 000	2	Reference compress stressed
Asahi	150	30 000	2	Reference compress stressed
Asahi	200	30 000	2	Reference compress stressed
DuPont	50	30 000	2	Reference compress stressed
DuPont	100	30 000	2	Reference compress stressed
DuPont	150	30 000	2	Reference compress stressed
DuPont	200	30 000	2	Reference compress stressed

Table 11: Smallest via sizes bent. Reference tensile stressed.

Ink	Via size (µm)	Bending cycles	Plate distance (cm)	Notes
Asahi	50	30 000	2	Reference tensile stressed
Asahi	100	30 000	2	Reference tensile stressed
DuPont	50	30 000	2	Reference tensile stressed
DuPont	100	30 000	2	Reference tensile stressed

Table 12: Additional measurements. Longer bending cycle test, cycle-rest-cycle–, smaller plate distance- and post anneal tests.

Ink	Via size (µm)	Bending cycles	Plate distance (cm)	Notes
DuPont	100	500 000	2	Reference tensile stressed
Asahi	50	Cycle-Rest-Cycle	2	Reference compress stressed
DuPont	50	Cycle-Rest-Cycle	2	Reference compress stressed
Asahi	100	30 000	1	Reference tensile stressed
DuPont	100	30 000	1	Reference tensile stressed
Asahi	100	30 000	2	Cycle-anneal-cycle -test
DuPont	100	30 000	2	Cycle-anneal-cycle -test

A total number of bending measurements is then 19, where 17 samples were bent in total, since the cycle-anneal-cycle -test used the previously bent samples. Three of the daisy-chain samples were chosen for each measurement from the bending structure, because of limited amount of measurement inputs in the iCraft AD/DA converter device. Total number of vias bent is 17 samples times three daisy-chain lines in one measurement times 22 vias in one daisy-chain line, which equals 1122 bent vias.

3.2 Supercapacitor

In this thesis, the supercapacitors were made in TUT by stencil printing. The performance of the supercapacitors were measured and evaluated with and without silver printed through-hole vias.

3.2.1 Fabrication method

The supercapacitors were made by stencil printing since the activated carbon is easy to dry onto screen-printer's screen. Stencil printing method is shown in Figure 18.

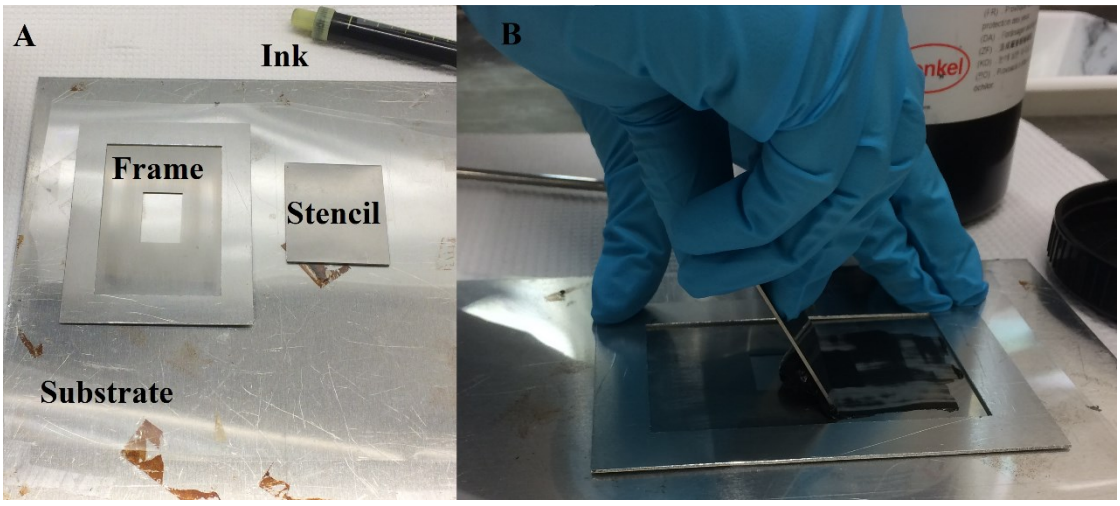


Figure 18: Stencil printing method. A: Equipment and B: Method shown.

In reference supercapacitor samples, a graphite layer was first printed on top of Melinex ST506 substrate. The graphite used was Loctite Edag PF 407C [56]. In through-hole via samples, graphite was printed partly on top of a silver pad. The silver pad was connected to a printed through-hole via, which lead to the other side of the substrate. The same substrate and graphite ink was used as the reference. The silver pads are shown in Figure 13. Graphite ink was sintered first in a 120°C oven for 15 min and after a cool down another print layer of graphite was printed and sintered in the same conditions as the first layer. Double layer of graphite decreases ESR. Dimensions of the graphite layer was 2 cm x 3 cm and the silver pads dimensions were 1,5 cm x 1 cm.

After the graphite layer printing, activated carbon layer was printed on top of the graphite to maximize the supercapacitor area. AC ink was made in TUT with Kuraray YP-80F activated carbon powder, shrimp shell chitosan, acetic acid and water. Dimensions of the activated carbon layer was 1,8 cm x 1 cm. Same AC layer was also printed on to graphite layer that lead to a silver pad and other side of the substrate. The activated carbon ink was left to dry at ambient air for at least four hours after printing.

After graphite and activated carbon printing, the supercapacitor was assembled. Two electrodes were chosen and the substrate was cut into 4 cm x 4 cm pieces with the reference samples, so that the graphite layer was visible. A reference sample structure is shown in Figure 9. Substrates were bigger with the silver interconnects, since the silver pad was visible on the other side of the substrate and graphite layer can be left under the other electrode's substrate. Few droplets of 1 mol/l NaCl electrolyte was put on top of both electrode's activated carbon. Then a separator paper Dreamweaver Titanium 40 AR 40 was placed on top of either one of the AC, which was soaked with NaCl. Then the both electrodes were combined AC layers facing each other and sealed with 3M 468MP 200MP acrylic adhesive. After assembling, supercapacitors were characterized electrically. Process diagram of assembling a reference supercapacitor is shown in Figure 19.

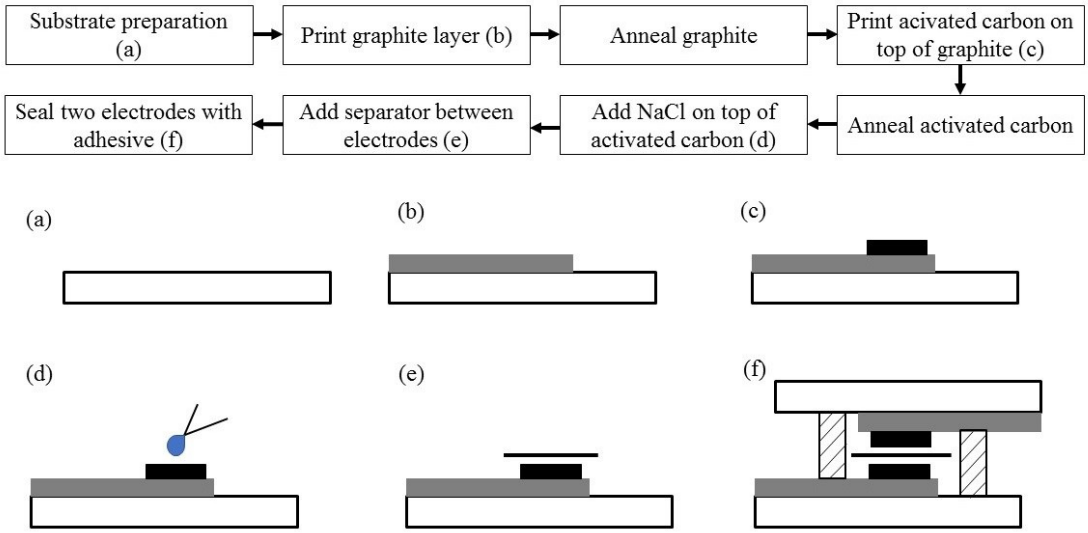


Figure 19: Processing diagram of fabricating and assembling a supercapacitor.

3.2.2 Characterization

The supercapacitors in this study were characterized with charge-discharge cycles with a Maccor 4300 device. In each measurement, the supercapacitor under test was charged to 0,9 V with 1 mA current three times. After that, the voltage was charged to 0,9 V and held in that voltage for 30 min and discharged at 1 mA, then charged again to 0,9 V and held there for one hour and discharged at 1 mA. At the end, supercapacitor was charged and discharged to 0,9 V with 3 mA and 10 mA currents for three times.

The capacitance of the supercapacitor was determined from 1 mA discharge after 30 min hold with a formula

$$C = -\frac{I}{dV/dt}. \tag{11}$$

According to an IEC standard 62391-1:2006, the capacitance is calculated between 80% and 40% of the maximum voltage [57].

The supercapacitors used in this study have relatively high losses caused by the graphite ink. Equivalent series resistance (ESR) mainly causes the losses of the supercapacitor. ESR is calculated from the supercapacitor discharge curve. When supercapacitor is discharged, a voltage drop appears. From the voltage drop can be calculated the ESR with equation (9).

The supercapacitor's ESR is calculated from the 1 mA discharge after the 30 min voltage hold. Graphite layer's thickness and dimensions play a key role in the ESR calculation, which is discussed in section 4.2.1.

Final key parameter that is calculated from the supercapacitor is the current leakage, which is the current drawn from the supercapacitor spontaneously. Current leakage is calculated from the 30 min hold period in the program. All three key parameters, capacitance, ESR and current leakage, were calculated from the measurement results with a Matlab program.

3.3 Energy module prototype

An energy module prototype was assembled with infinityPV organic photovoltaic, three supercapacitors in series, which also had screen printed vias in contact electrodes, and two conventional 1N4148 through-hole diode components. Diodes were attached between the supercapacitor and OPV positive terminals to prevent supercapacitor from discharging itself through OPV when there is no light available. The maximum voltage of three supercapacitors in series is 1,23 V * 3 V = 3,69 V and the maximum voltage of the OPV was approximately 5 V. Diode's threshold voltage was 0,7 V. Two diodes were connected in series to limit the maximum voltage coming to the supercapacitors. A light emitting diode (LED) was also connected between supercapacitor terminals to limit the maximum voltage of the supercapacitors and to show a simple application of the energy module capabilities. Circuit from the prototype is shown in Figure 20.

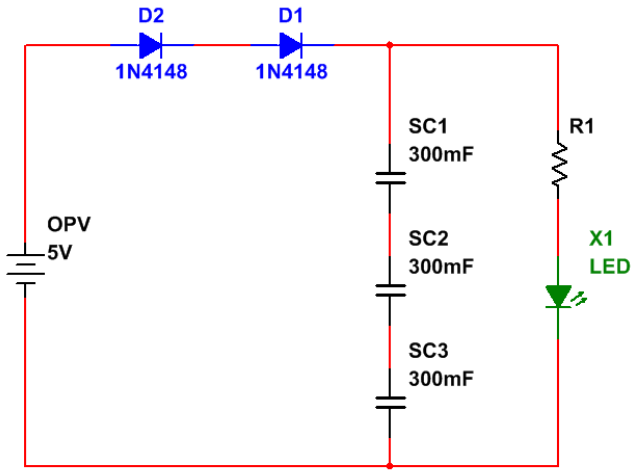


Figure 20: Circuit from the assembled prototype.

3.3.1 Fabrication

The prototype's supercapacitors were assembled with the same method as stated in section 3.2.1. OPV, LED and diodes were ordered from different companies. The supercapacitors, diode and supercapacitors were attached to each other with silver conductive epoxy adhesive. The epoxy was a two-part adhesive, which were mixed in 1:1 ratio. The adhesive was highly conductive and cured at room temperature in 24 hours [58].

The LED was a sticker-like component, which had a surface mounted LED and a pull-up resistor. Two bigger contact pads were in the sticker for easy assembling. Sticker was attached to the middle of the three-supercapacitor energy storage. A conductive paint was used to draw a line from the energy storage silver contact pads to the LED sticker's contact pads. The conductive paint was from bareconductive.com and dried in ambient air in 15 minutes.

3.3.2 Electrical measurement

The prototype's electrical performance was measured with a multimeter and a bright light. Measurement started from a dark room and completely discharged supercapacitors. Multimeter was attached to the contact pads of the energy harvester and set to voltage measurement mode. Then the light was turned on and the voltage was recorder first after 10 second time periods and then after one minute time periods. The prototype was charged with light for 15 minutes with two different illumination values and discharged for over 15 minutes through the LED.

4. RESULTS AND DISCUSSION

4.1 Screen printed via

This chapter introduces the measurement results from screen-printed vias, which were filled with silver ink in the direct two-step screen-printing process. Some discussion and aspects are also provided after the results.

4.1.1 Optical characterization

The via sizes were measured with an optical microscope. Measured via sizes with standard deviations are shown in Table 13. A typical 100 µm via size laser drilled hole is shown in Figure 21.

Table 13: Measured via sizes

Nominal via size (µm)	Measured via size average top (µm)	Standard deviation (µm)	Measured via size average bottom (µm)	Standard deviation (µm)	Sampling rate, (N)
50	125	± 13	67	± 9	29
100	173	± 15	120	± 5	26
150	232	± 18	172	± 10	24
200	281	± 16	224	± 11	26

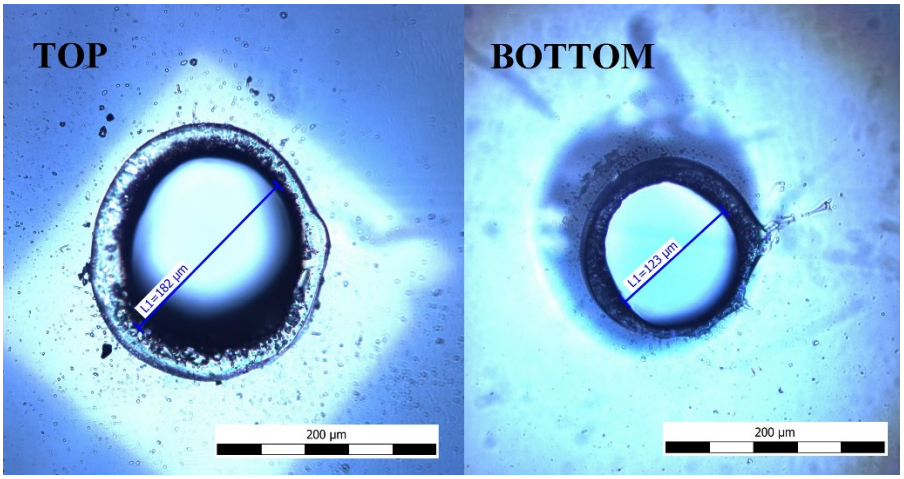


Figure 21: 100 µm via top and bottom images.

As seen from Table 13 values and Figure 21, the laser cut via is bigger on the top than in the bottom. This implies that the cross section of the via was then cone shaped instead cylindrical. The measured via size values vary from the nominal values, which results

from an offset in the laser focal point and the thickness of PET and conduction deformations from the heat applied. Microscope image of a cross section from the via before printing is shown in Figure 22.

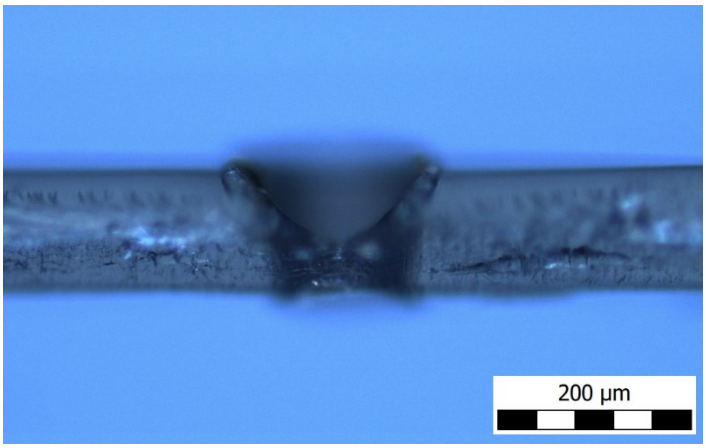


Figure 22: Cross-section image of a laser cut through-hole via.

Before the printing process all substrates were cleaned and ultrasonicated. Ultrasonicator cleaned the corners of the via from small plastic pieces. The effect of ultrasonication is shown in Figure 23. 50 µm vias were sonicated for 30 minutes and all the other substrates were sonicated for 20 minutes.

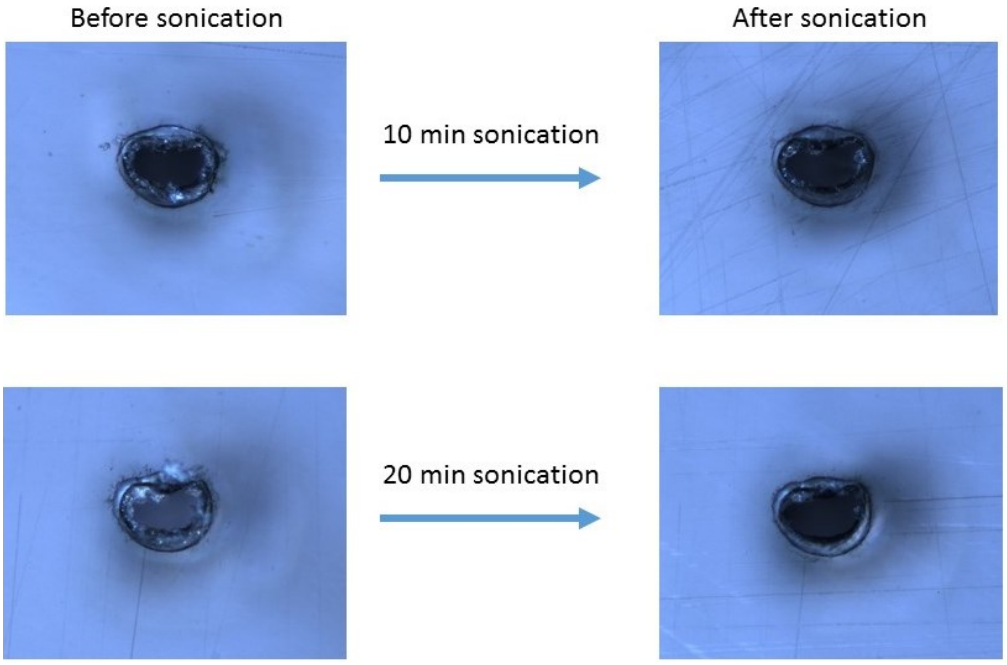
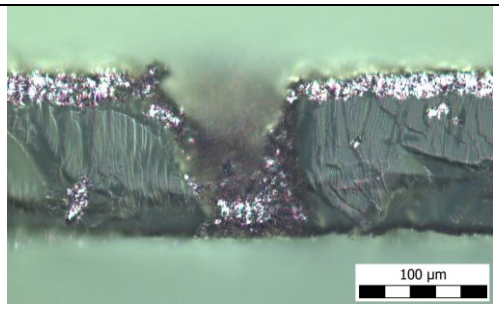
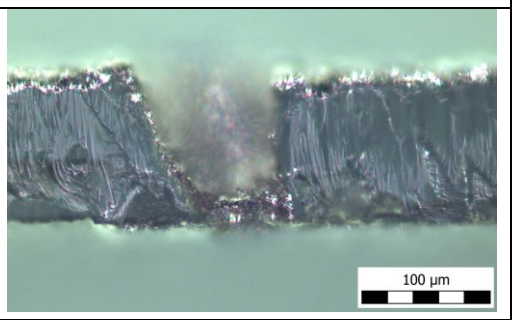
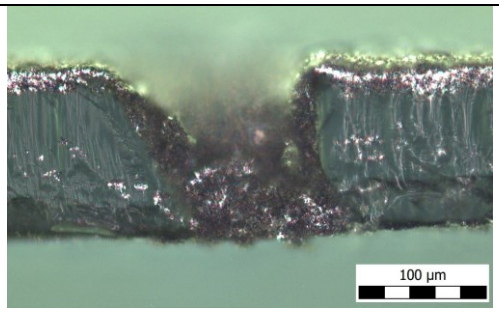
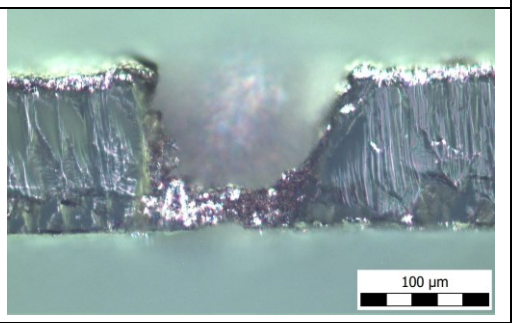
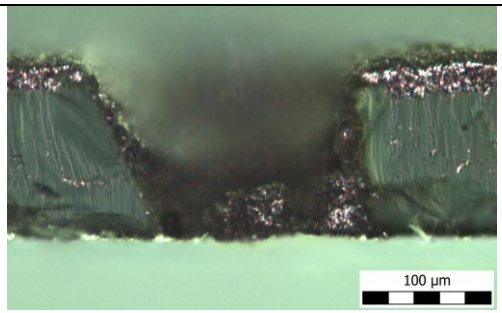
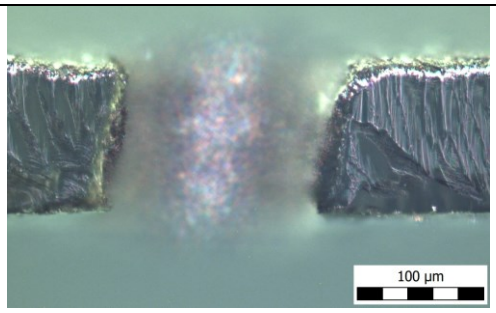
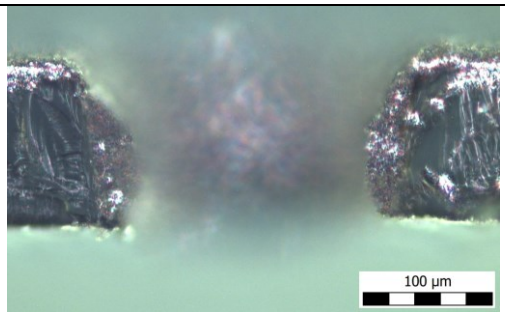
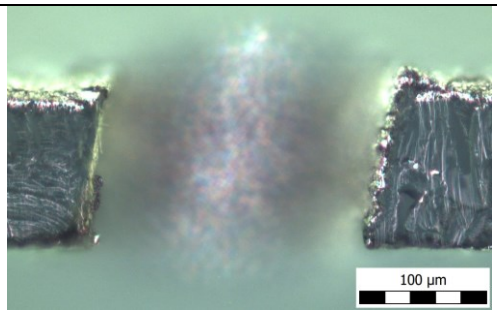


Figure 23: Effect of ultrasonication to the vias.

Following via printing, cross sections of the vias were taken to evaluate the ink filling properties. The images of the cross sections after printing are shown in Table 14.

Table 14: Cross sections of vias after printing process.

Via size	20x microscope image Asahi	20x microscope image DuPont
50 µm		
100 µm		
150 µm		
200 µm		

In all cases, Table 14 illustrates that the that the via is only partly filled in the printing process. via is only partially filled during the printing process. However, a reliable electrical connection is still possible. It is also evident that the DuPont ink's filling mechanism is less effective than the Asahi ink. In addition, the ink fills larger via sizes poorly and mainly only coats the via sidewalls. When the ink is on the sidewalls, a less reliable connection was noticed. The unreliability is attributed to the top and bottom ink layers not forming a continuous structure inside the via as seen in Figure 24.

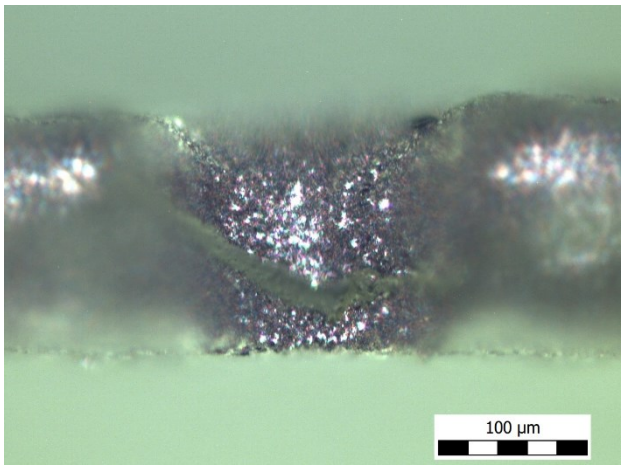


Figure 24: Cross section image of a non-conducting via (150 µm nominal via size).

For more high quality cross section images, the samples were set into a resin mold and grinded onto the height, when the via cross section was visible. However, The grinding approach was challenging to execute with the 50 µm via size, since the grinder can pass the via in the mold easily. The 50 µm via samples were sent to Top Analytica, where the cross section was cut with a broad ion beam cutter. The final image was taken with scanning electron microscope (SEM). The 50 µm via size images cut with a broad ion beam are shown in Table 15. The cross section images of samples in resin mold by grinding were taken from 100 µm, 150 µm and 200 µm via sizes using both inks. The images are shown in Table 16.

Table 15: Cross section images from 50 µm nominal size vias using Asahi and DuPont inks. The cross section were made with a broad ion beam and the images were taken with SEM. Samples were prepared and the images were taken in Top Analytica.

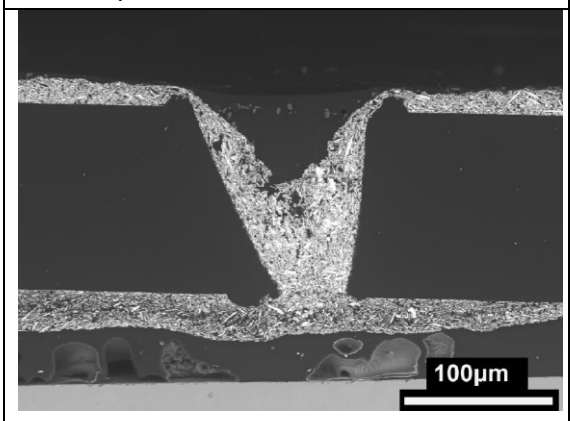
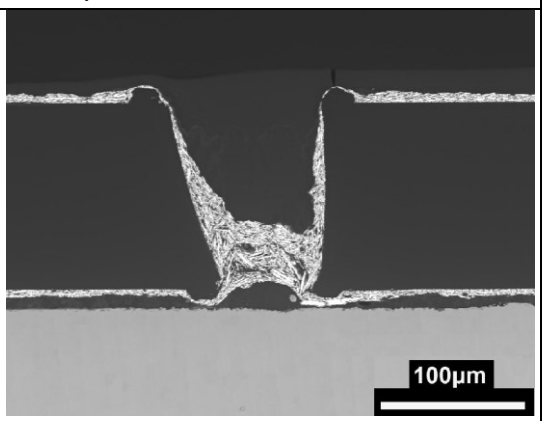
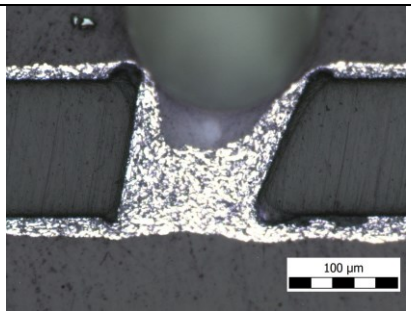
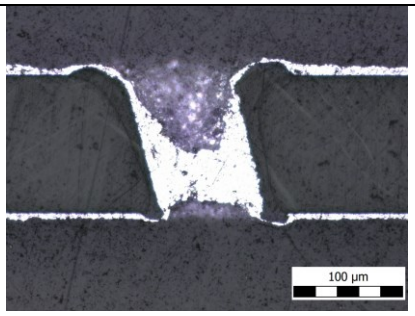
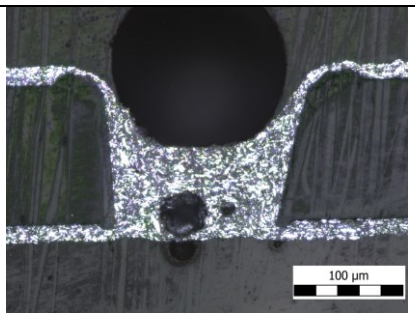
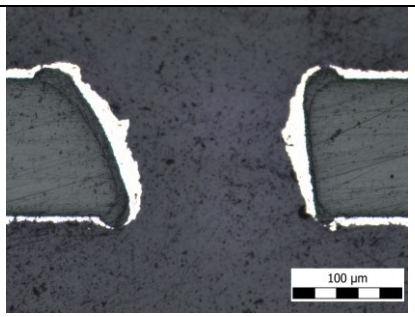
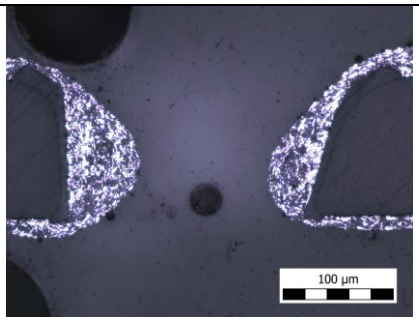
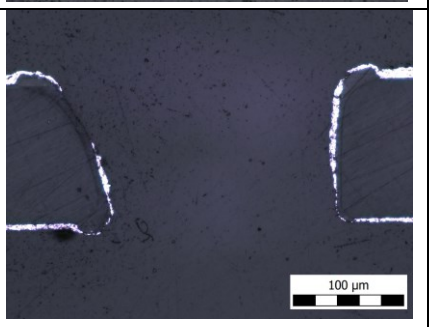
50 µm via filled with Asahi ink	**50 µm via filled with DuPont ink**
	

Table 16: Optical microscope images of cross sections of vias after print process in resin mould.

Via size	Asahi	DuPont
100µm		
150µm		
200µm		

The Table 14, Table 15 and Table 16 images have similar results. The Table 15 and Table 16 show a higher quality inspection of the ink filling the via.

4.1.2 Electrical characterization

First, electrical conductivity of the ink was measured to ensure repeatability and adequate curing conditions. A four point probe (4PP) pattern for sheet resistance (Rs) was measured with the 4PP protocol at a 10 mA current. Four patterns with 400 µm line widths were printed on the top and bottom of the PET. The results are shown in Table 17.

Table 17: Sheet resistance of the inks in 4PP structures of samples.

Ink	Mean R_s, Top (mΩ/□)	Mean R_s, Bottom (mΩ/□)	Number of 4PP patterns
Asahi	20,3 ± 4,7	29,5 ± 6	Top: 84, Bottom: 84
DuPont	31,4 ± 22,6	26,67 ± 14,2	Top: 96, Bottom: 132

As seen from Table 17 results, DuPont ink has more deviation in the sheet resistance values compared to Asahi ink's results. The high resistance deviation proves that the print process was not as optimal for the DuPont ink as for the Asahi ink. It was noticed during the print process that the screen was clogged from some parts of the pattern and the sheet resistance could not even get measured in some of the samples. That is why top and bottom sampling rates are not equal with DuPont. Fortunately, printing with DuPont did not affect the filling of the via, since the collar size was large enough and was not clogged. With the Asahi ink, all 4PP patterns were measured and the sheet resistance values are according to datasheet value, which is lower than 40 mΩ/□ [13]. The DuPont ink's sheet resistance should be lower than 14 mΩ/□ for 25 µm line thickness [14].

After the ink conductivity measurements, the electrical connection of the vias were determined. Results from printed vias in all eight cases are shown in Figure 25. The criteria for pass, poor or failed vias are stated in Table 9 and total population of vias for each case are shown in Table 8.

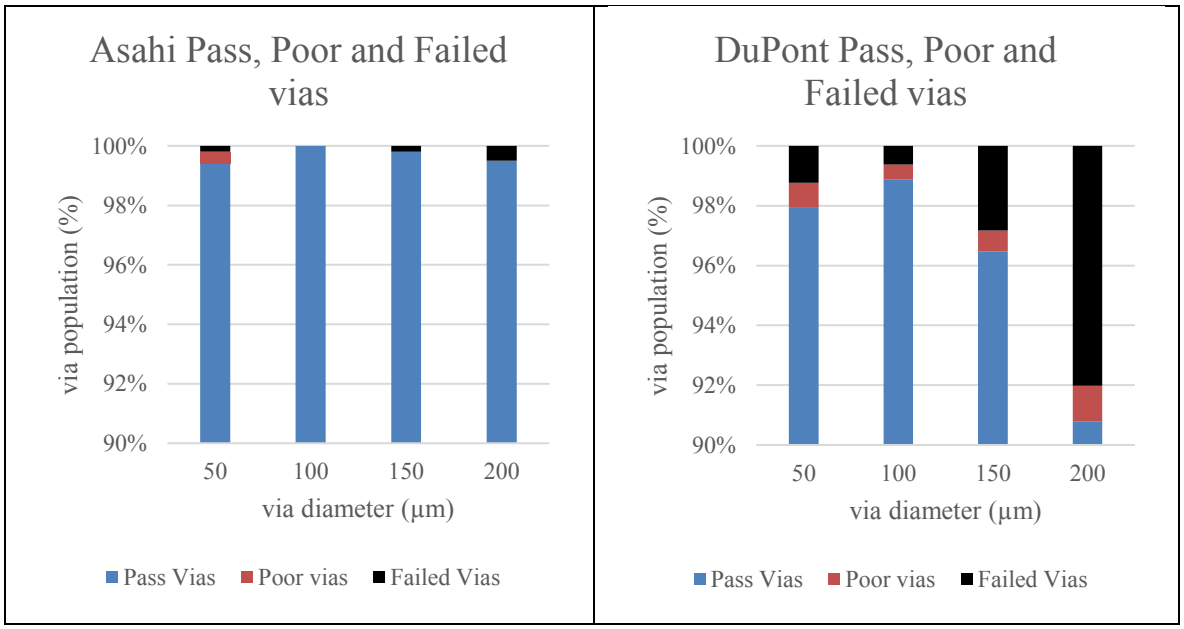


Figure 25: Asahi and DuPont pass, poor and failed vias chart. Populations of vias are as follows: Asahi 50µm 1010, Asahi 100µm 1010, Asahi 150µm 1010, Asahi 200µm 1010, DuPont 50µm 1616, DuPont 100µm 1616, DuPont 150µm 1414, DuPont 200µm 1010.

As seen from Figure 25, the best ink filling results were achieved with the 100 µm nominal via diameter with both inks. With both inks, the 200 µm vias had the lowest reliability due to the reduced aspect ratio. The 50 µm nominal via size had a high number of poor vias compared to failed vias. It was noticed that with larger via sizes the ink passes the via and lays on the screen stage coating the sidewalls of the via instead of filling and creating a reliable connection. With smaller via sizes, the via is filled properly and stays inside the via creating a more reliable connection. On the other hand, the smallest via sizes might limit the amount of ink penetration. The optimal via size in this study was the 100 µm via diameters. When comparing the two inks, it is believed that the Asahi fills the via more effectively, since it has higher viscosity. However, the transferred ink might vary between samples and distort the results with DuPont ink, since the process was not as well optimized for DuPont compared to Asahi ink. More modelling of the ink flow and filling of the via could bring more essential information to search the most efficient via diameter and ink combination.

An approximation of the via resistance was calculated by measuring first all the resistance values of bending structure lines. Then distracting from the bending structure line the reference line and dividing the result with the amount of vias in the bending structure line. A theoretical value for the via resistance can also be calculated. If we assume that the via is completely filled, via is cone shaped, where radius of the via is the average from top and bottom of the via and ink resistivity is the maximum sheet resistance collected from the datasheet from each ink. The theoretical values to calculate via resistance is shown in equation (12). The via's resistance for each via size and ink are calculated and measured in Table 18. The theoretical via resistance is calculated by

$$R_{via} = \rho_{ink}\frac{l}{A} = R_s t_{ink}\frac{t}{\pi r^2}, \tag{12}$$

where R_s is the maximum sheet resistance, t_{ink} is the thickness of ink at the maximum sheet resistance value, t is the thickness of the substrate or height of the via and r is the via average radius.

Table 18: Measured and calculated via resistances using two different inks.

	Asahi		*DuPont*	
Via size (µm)	**Measured** $\mathbf{R_{via}}$ (mΩ)	**Theoretical** $\mathbf{R_{via}}$ (mΩ)	**Measured via** $\mathbf{R_{via}}$ (mΩ)	**Theoretical** $\mathbf{R_{via}}$ (mΩ)
50	109,56	1,73	115,3	1,51
100	92,86	0,74	43,8	0,65
150	80,02	0,39	101,7	0,34
200	77,84	0,25	83,1	0,22

In Table 18 the theoretical via resistances are approximately 100 times smaller compared to the measured values. However, the highly rough estimation of via filling fully

is false acquisition in this measurement as seen in Table 14 images. Other factors affecting to the measured via resistances is that the daisy-chain structure's resistance can vary from the reference structures resistance. For example, the thickness of both structures can be different and vary from the theoretical thickness. All the structures are still done within the same screen printer's squeegee stroke and face the same circumstances in the printing. One final note is the via resistance decreasing in bigger via sizes. In bigger via sizes the via has more ink and more silver particles to create conductivity. It can be seen with the Asahi ink, that the via resistance decreases when going to larger via sizes, but with DuPont the smallest via resistance is achieved with 100 µm nominal via size. The effect can be explained by looking Figure 25 results, since 100 µm via diameter results have the lowest amount of poor vias, which rises the average via resistance higher. With DuPont 100 µm samples, the relation between poor and pass vias is lowest compared to other samples' results'.

When looking closer to the print process, we can notice that some of the broken vias occur in the same location. The printed structure can be placed into a matrix and record all the broken vias in printed samples. The sample structure divided into a matrix is shown in Figure 26 and the broken via matrix in the printed sample is shown in Figure 27. The Asahi matrix shows all broken vias within 20 samples and DuPont matrix shows all broken vias within 28 samples.

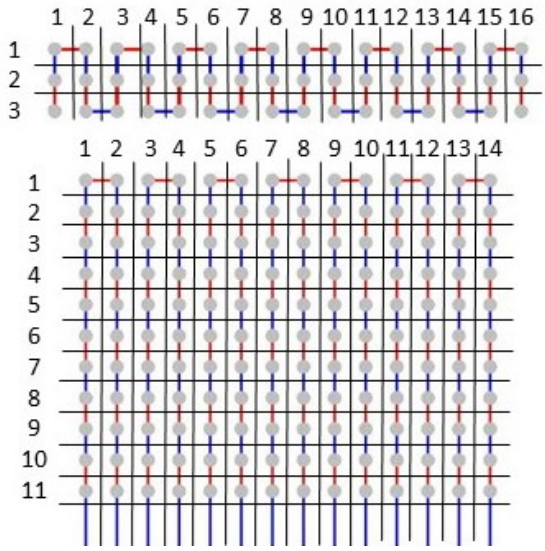


Figure 26: Sample structure, seen in Figure 15, divided into matrix.

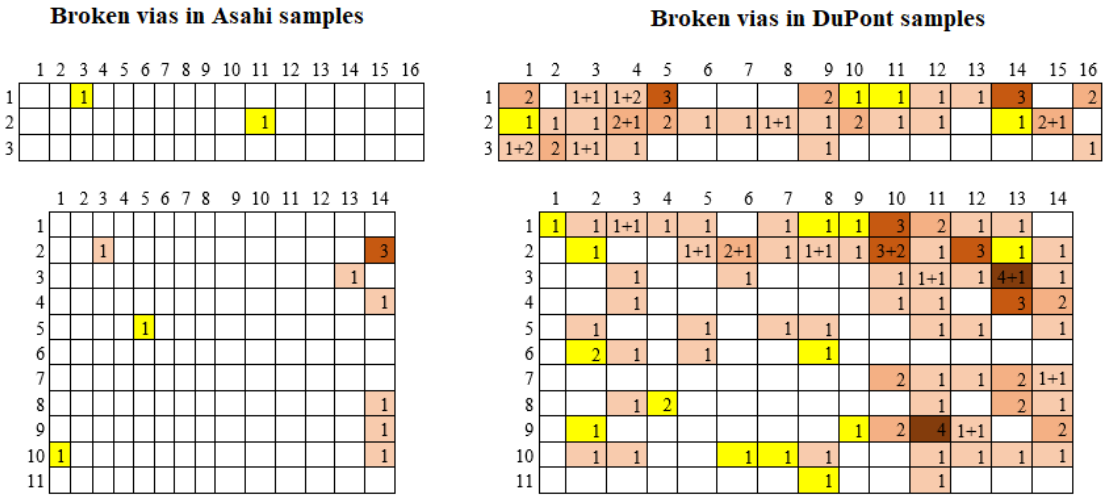


Figure 27: Broken via matrix with two different inks. Yellow blocks represent poor via connections and red blocks not connected vias. Two numbers represent not connected + poor vias.

In Figure 27 can be noticed that the right corner of the bending structure has large quantity of broken vias with both used inks. The DuPont ink also has overall more broken vias in the proof of principle structure. This might be due to manually optimized printing parameters.

4.1.3 Via bending results

The first cyclic bending tests were to see the differences between inks and via sizes. The results from Table 10 tests are shown in Figure 28 without considering the reference sample bending. In each measurement three of the daisy chain structures were measured and one reference line measured. In Figure 28, average is taken from the three daisy chain structures that were bent. Each of the samples faced 30 000 bending cycles.

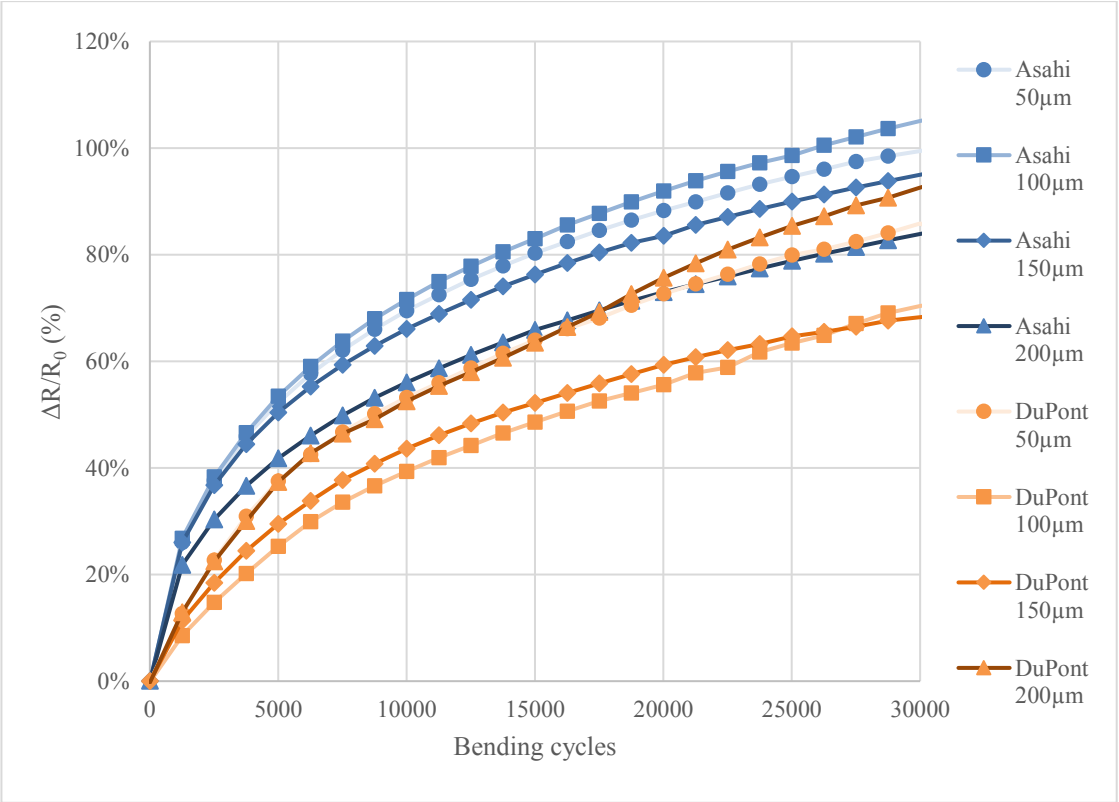


Figure 28: Cyclic bending test for each via size and two different inks.

It can be seen from Figure 28, that the resistance of the printed silver line rises when cyclic bent and in some of the cases the resistance nearly doubles. If the via is broke during the measurement, resistance becomes infinity because of an open circuit. When an open circuit occurs in the measurement setup, the resistance of the sample line oscillates between the maximum and minimum value rapidly. One via in the measurement broke during the measurement and was left out from inspection in Figure 28. The sample was done using DuPont ink and 50 µm via size. It was noticed that the via was considered poor in the initial electrical characterization. The broken sample line measurement is shown in Figure 29, which was left out from the Figure 28 inspection. The poor connection was considered unreliable.

Remarkable notice from Figure 28 results is that the DuPont samples seem to be more resilient to bending compared to Asahi samples. This is might be due that the printed silver line is thinner with DuPont ink, polymer composition of inks or because the DuPont ink has a larger silver particle size compared to Asahi ink [17, 21].

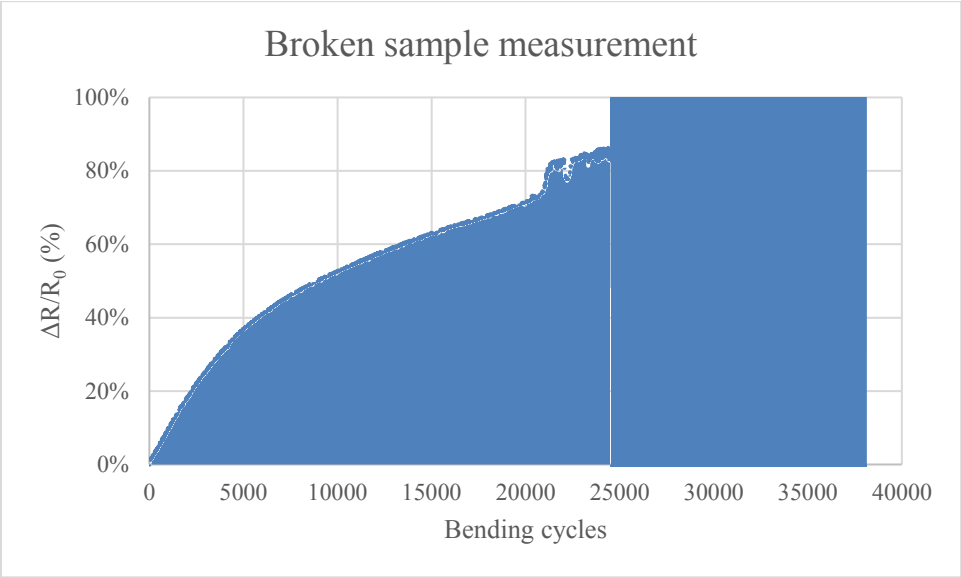


Figure 29: Broken sample line measurement with DuPont ink and 50µm via size. One via failed in the measurement, which was poorly conductive in the initial electrical characterization.

In the cyclic bending test reference line faces whether compressive or tensile stress. These two different bending stresses have different effect on the printed line. The daisy chain structure lines face both compressive and tensile stress. The effect of tensile and compressive stresses are shown Figure 30. In Figure 31 and Figure 32 are shown the same 30 000 cycle bending results with both inks, but also taken into account the reference line bending in both tensile stress and compressive stress cases. The daisy-chain samples' resistance change (ΔR) caused from cyclic bending is shown in Figure 31 and Figure 32 for Asahi and DuPont inks respectively. The average reference values were taken from four compressive stressed samples and two tensile stressed samples for both inks. Both tensile and compressive stressed reference samples are in the chart to help differentiate the via bending effect from the interconnection stress.

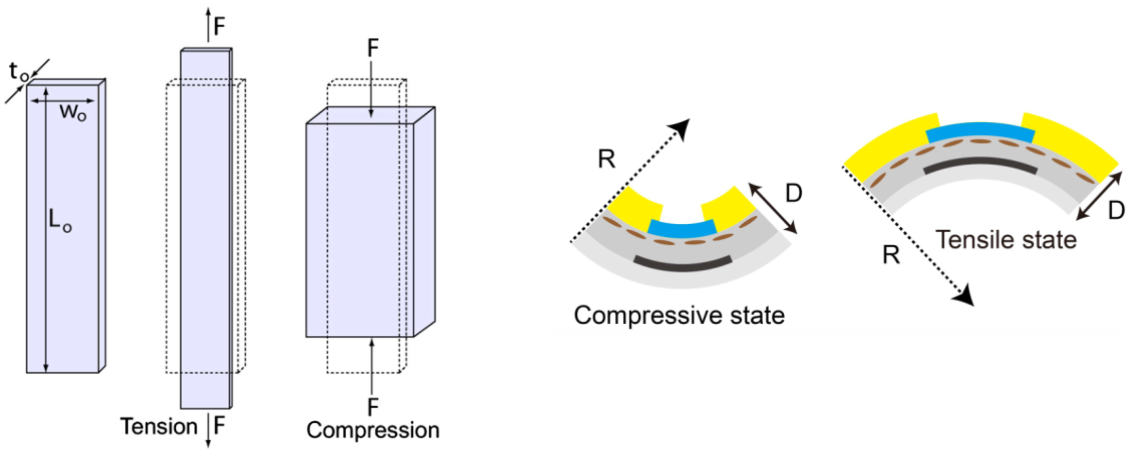


Figure 30: The effect of tensile and compressive stress for the dimensions of conductor line. Adapted from [21, 59].

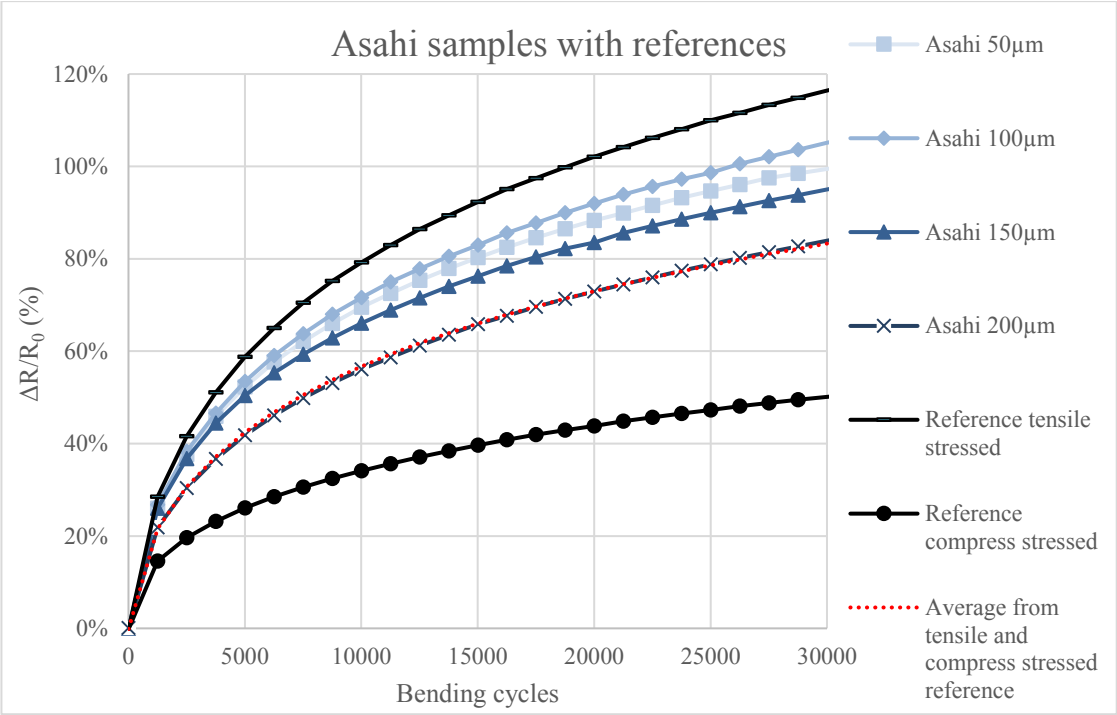


Figure 31: Asahi samples bending with reference samples. Initial resistance (R_0) for each case: 50µm 13,4 Ω; 100µm 12,8 Ω; 150µm 11,9 Ω; 200µm 11,5 Ω; Reference tensile 10,7 Ω; Reference compress 10,5 Ω.

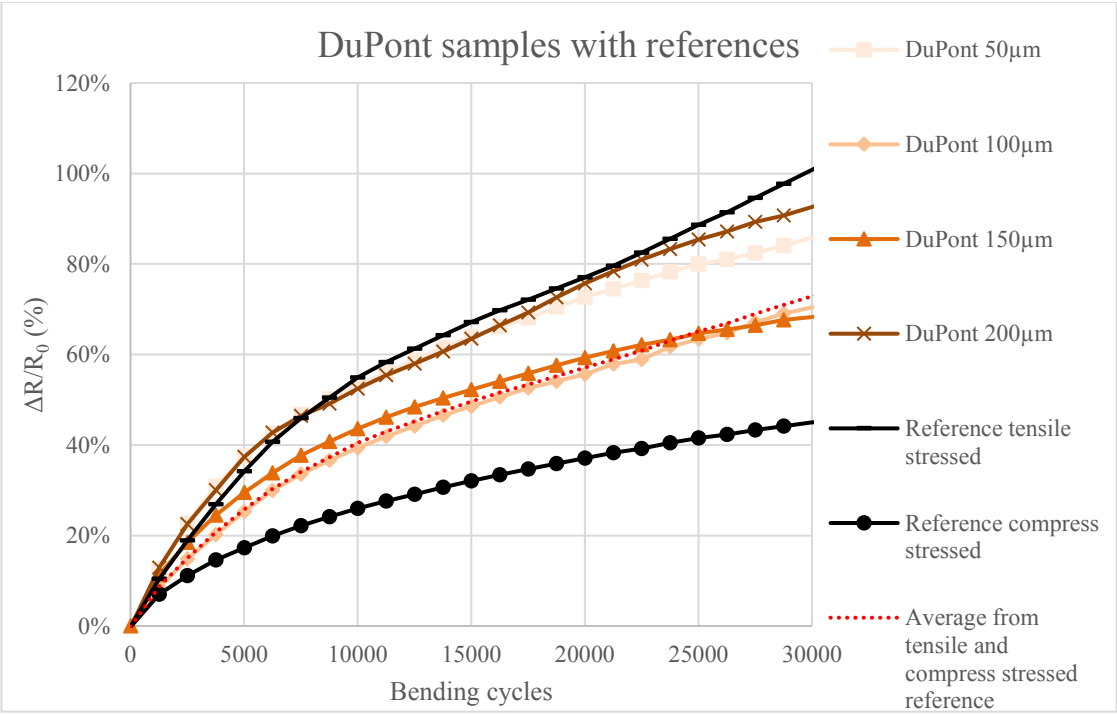


Figure 32: DuPont samples bending with reference samples. Initial resistance (R_0) for each case: 50µm 16,9 Ω; 100µm 17,6 Ω; 150µm 20,0 Ω; 200µm 12,3 Ω; Reference tensile 9,9 Ω; Reference compress 15,5 Ω.

The daisy-chain structure faces both compressive and tensile stress and thus is between the reference lines' ΔR. The sample lines do still have different ΔR when comparing different via sizes, which is caused by the via bending. A rough estimation from individual via bending can be given by comparing the daisy-chain structure bending to the fitted compressive and tensile stressed reference average and dividing the results by the number of vias in the daisy-chain structure. The cyclic bending effect estimation to each via size and ink is shown in Figure 33.

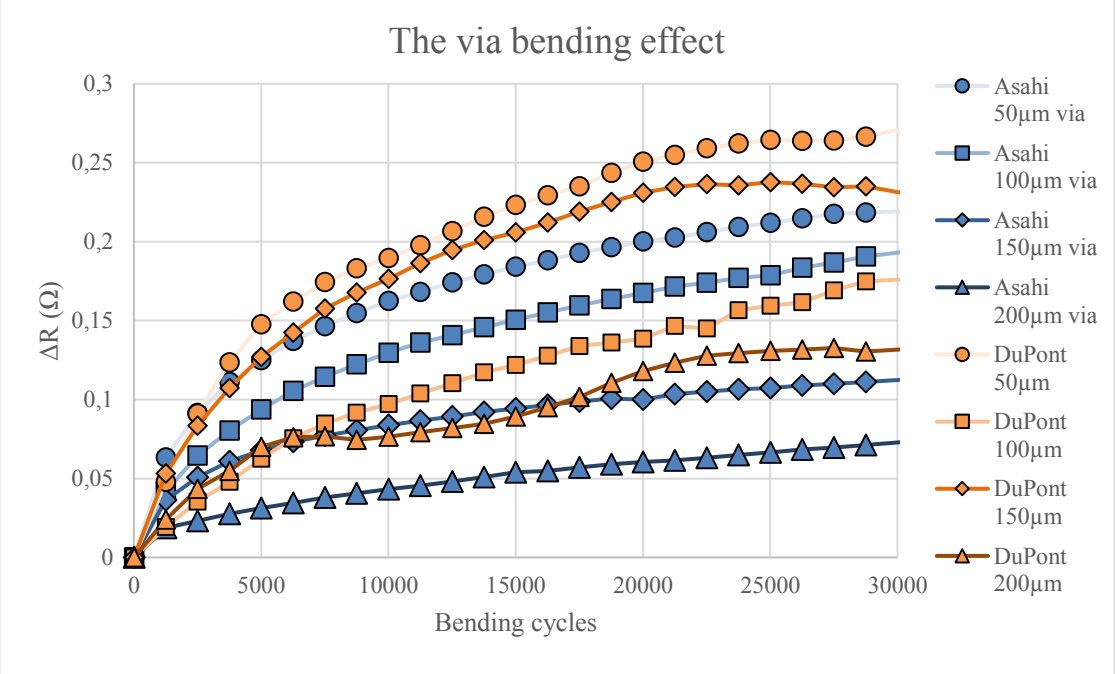


Figure 33: The effect of 22 vias bending for two different inks and four different via sizes.

Figure 33 illustrates the absolute resistance change in comparison to the fitted reference lines. In this case, the starting resistance values becomes significant. The error that comes from the reference lines is lower with Asahi than with DuPont, since the reference line starting values are closer to each other seen in Figure 31 and Figure 32 captions. However, the Figure 33 shows clear dependencies between the via sizes and used inks.

It can be seen from Figure 33, that the Asahi sample vias are more resilient to bending compared to DuPont sample vias, since the via is filled better using Asahi ink. Largest via sizes are the most resilient to bending with Asahi samples. With DuPont samples on the other hand, 150 µm via size seems to be more unreliable compared to 100 µm via size. This effect were ought to be because of high starting resistance value of DuPont 150 µm sample seen in Figure 32 caption. Smaller via sizes were thought to have more bending strain to the collar of the via, since the collar is smaller and larger strain is focused on it. Larger via sizes have larger collars respectively, which is beneficial in terms of the bending strain as this spreads the bending strain and causes smaller resistance change.

An acceptable resistance change depends on multiple factors such as the application of use. For example, other scientific publications have set the failure criterion to 20 % resistance change, which is achieved after 1555 bending cycles [54]. The failure criterion corresponds to the results that were gathered.

A longer cyclic bending test was done to see whether an open circuit occurs in higher stress. This would mean a via breakdown and connection lost between top and bottom layer. A 100 µm nominal via size sample printed with DuPont ink was chosen for the longer bending cycle test. The result of the longer bending cycle test is shown in Figure 34.

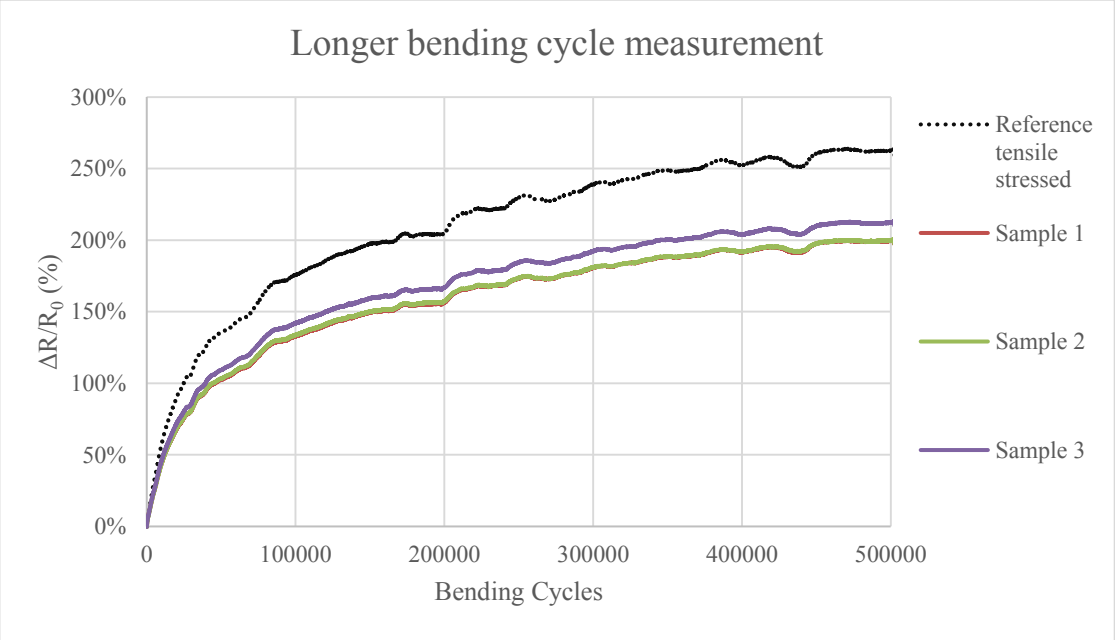


Figure 34: Longer bending cycle test for 100 µm DuPont sample.

The 500 000 bending cycles shown in Figure 34 lasted over 11 days. The most remarkable founding was that no via breakdown occurred in the measurement. The reference has a larger variance in resistance compared to daisy-chain structure lines since it was tensile stressed. The resistance value in daisy-chain structure lines seems to level approximately onto triple times compared to the starting resistance value. It can be also seen that the resistance value fluctuates in the measurement and at some parts even lowers down a little. In these sections the ambient climate conditions changed. For example, after approximately 420 000 cycles the humidity of the laboratory was 16 % and near the 500 000th cycle humidity was 25 %. Temperature was seen almost constant 22 °C with 0,4 °C deviation. The ink was then seen to be climate change dependent.

All the measurements done above were bent between plate distance of 2 cm. The plate distance was dropped down to 1 cm and measured again with two different samples, which had the same via size of 100 µm but comparing again the two different inks. The measurement results from the smaller plate distance are shown in Figure 35.

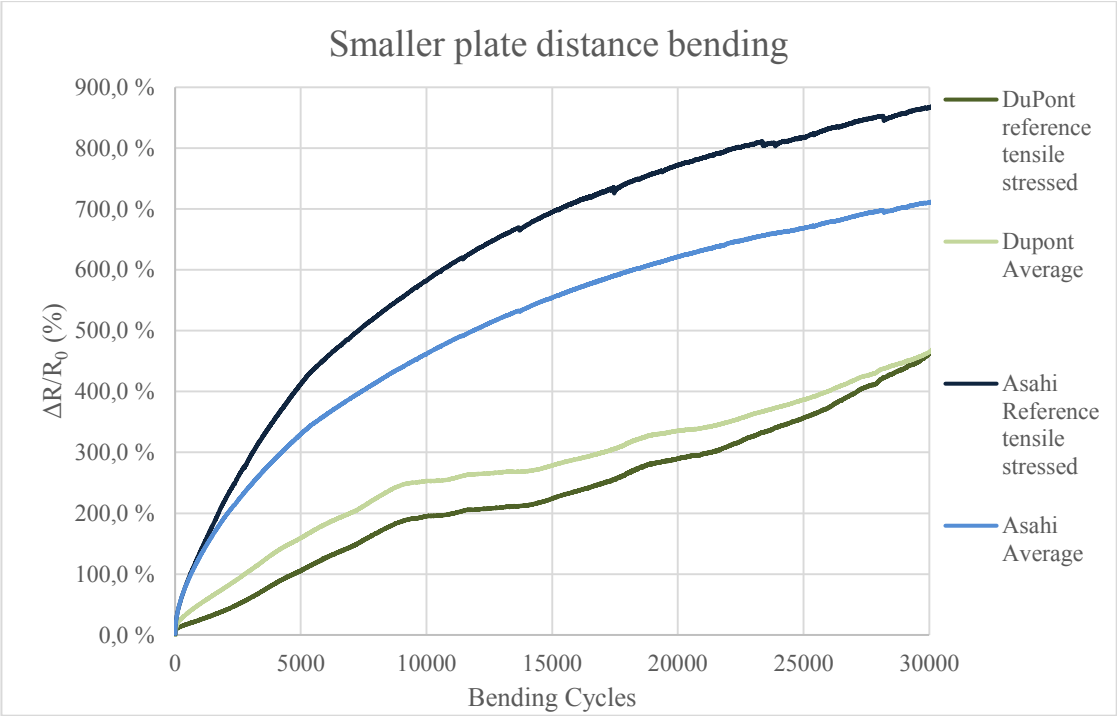


Figure 35: Smaller 1 cm plate distance bending with two different inks.

The smaller 1 cm plate distance effects to the printed lines resistance dramatically compared to 2 cm plate distance. After 30 000 bending cycles DuPont inks resistance has grown almost six times larger compared to the starting resistance value and with Asahi, the value is almost tenfold. Vias were not broken during the measurement. However, with DuPont one of the daisy chain sample lines had one via breakdown after the measurement was over. This might be the reason why the tensile stressed reference line had smaller resistance change compared to the three daisy chain structures average value.

The resistance of the reference and daisy-chain structures were still measured after the cyclic bending was stopped and the sample line was laying straight on the bending device platform. The resistance dropped after the bending in every case. A 90 minute after measurement in each of the cases shown in Figure 28 is seen in Figure 36.

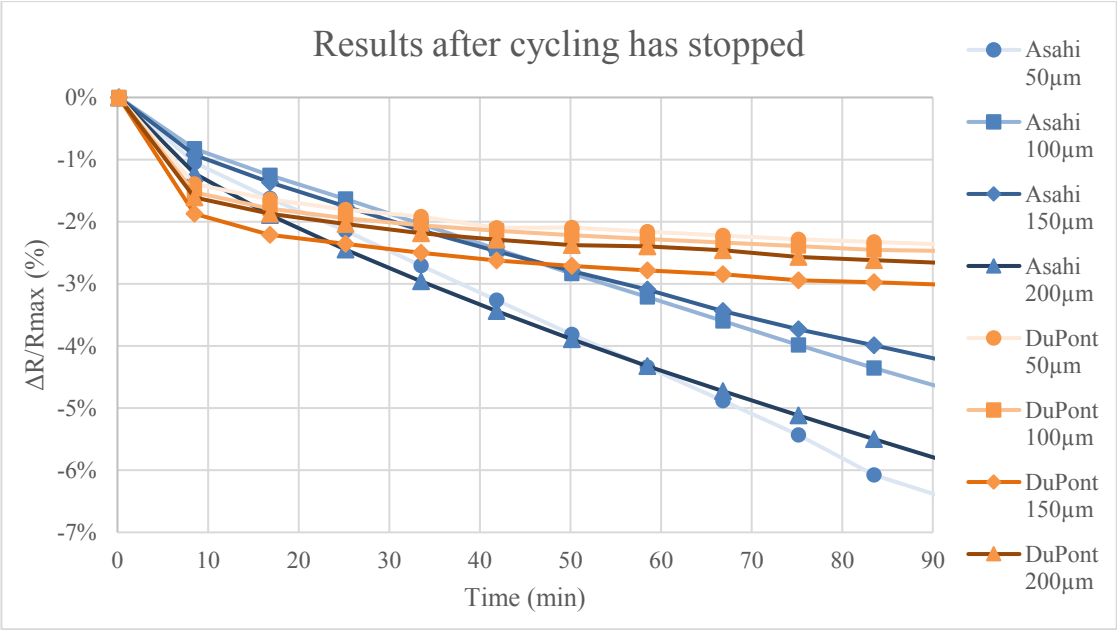


Figure 36: Resistance change after cycling was over.

To further research the effect of a sample repairing effect, a cycle-rest-cycle measurement was utilized. In the cycle-rest-cycle –measurement, the sample structures faced first approximately 3000 bending cycles and then left rest for 45 minutes, then cycled again for 3000 cycles and so forth for three times. The cycle-rest-cycle –measurement results are shown in Figure 37.

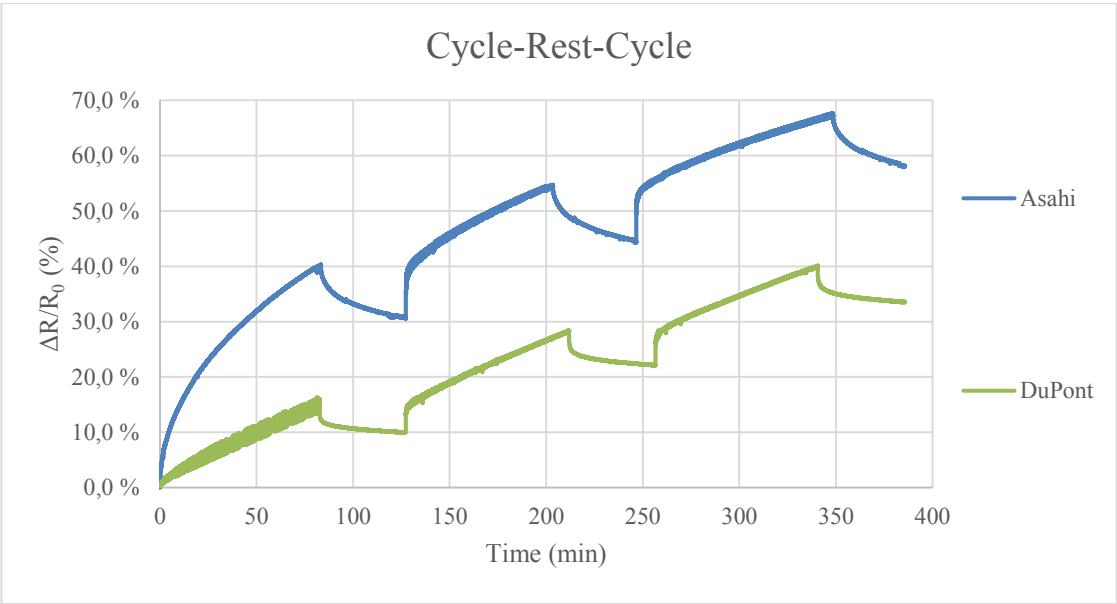


Figure 37: Cycle-Rest-Cycle -measurement with two different inks.

It can be seen from Figure 36 and Figure 37 that the resistance is dropping after the cyclic bending has stopped. However, the resistance quickly returns to the resistance value that it once achieved and starts to rise again when the cycling starts. The ink then has a bending memory. An intriguing fact is that the two inks behave differently after

the cycling stops. DuPont has a clear slope after the cycling stops and levels relatively fast. The Asahi inks resistance drops almost linearly after the cycling stops.

The self-healing of a conductor line was further researched. The resistance change is due to the tensile and compressive stress that the conductor line faces and forms delamination and cracks to the printed line. The resistance rise was also ought to cause by the rearrangement of silver flakes in the conductor. The silver flakes were thought to arrange again if the conductor line was annealed again after bending and the ink's polymer compound is then softened and silver flakes are again closer to each other. The hypothesis was then tested with a post anneal test. The samples were bent for 30 000 bending cycles and then left to rest in ambient air for at least five days. Then the resistance was again measured after the rest period, annealed for 20 minutes in circulated oven at 150 °C or 130 °C for Asahi and DuPont inks respectively. After the post annealing the resistance was measured again. The results from conductor post anneal test is shown in Figure 38.

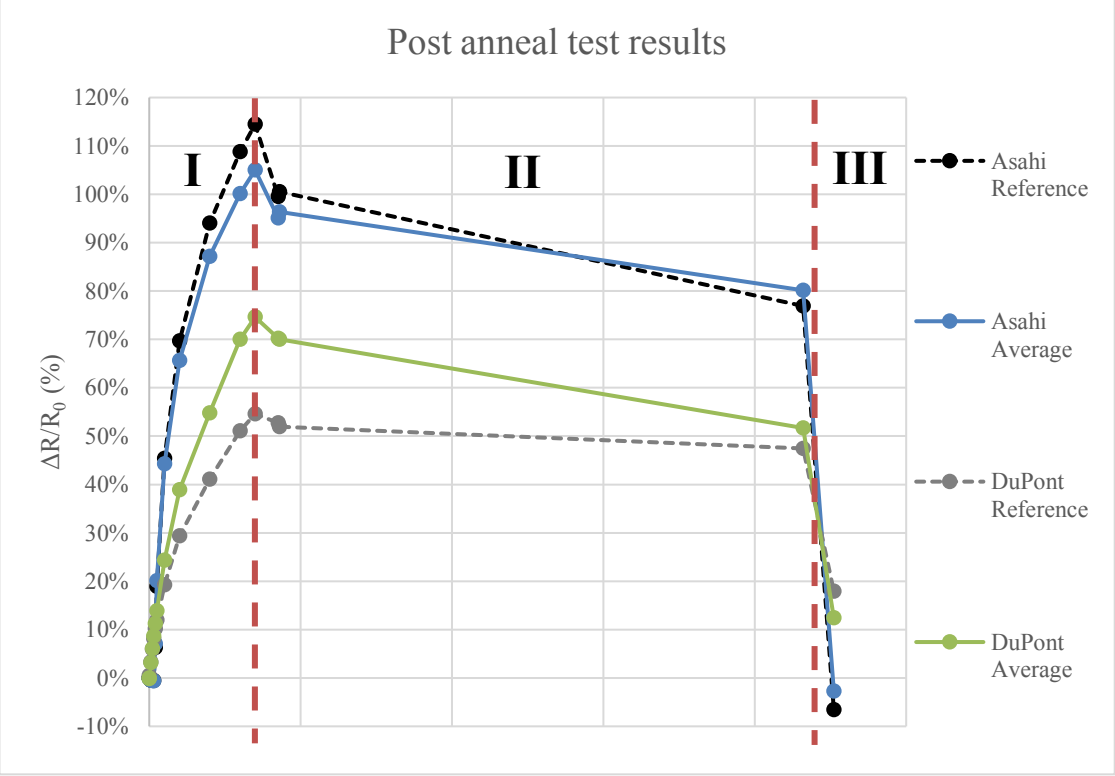


Figure 38: Post anneal test results. Area I stands for bending period, II is the ambient air rest period and III is the after anneal period.

In the post anneal test was found out that the resistance drops after longer wait period in ambient air and lowers down considerably after annealing again. The starting hypothesis of silver flakes rearranging seems to be valid. However, the resistance can rise dramatically again, when the sample line is being again cycle bent when looking at the results from the cycle-rest-cycle -measurement. The effect of cyclic bending again for a

post-annealed sample was then tested. The results of two rounds bent daisy-chain sample lines are shown in Figure 39, with the first cyclic bent results shown as a comparison.

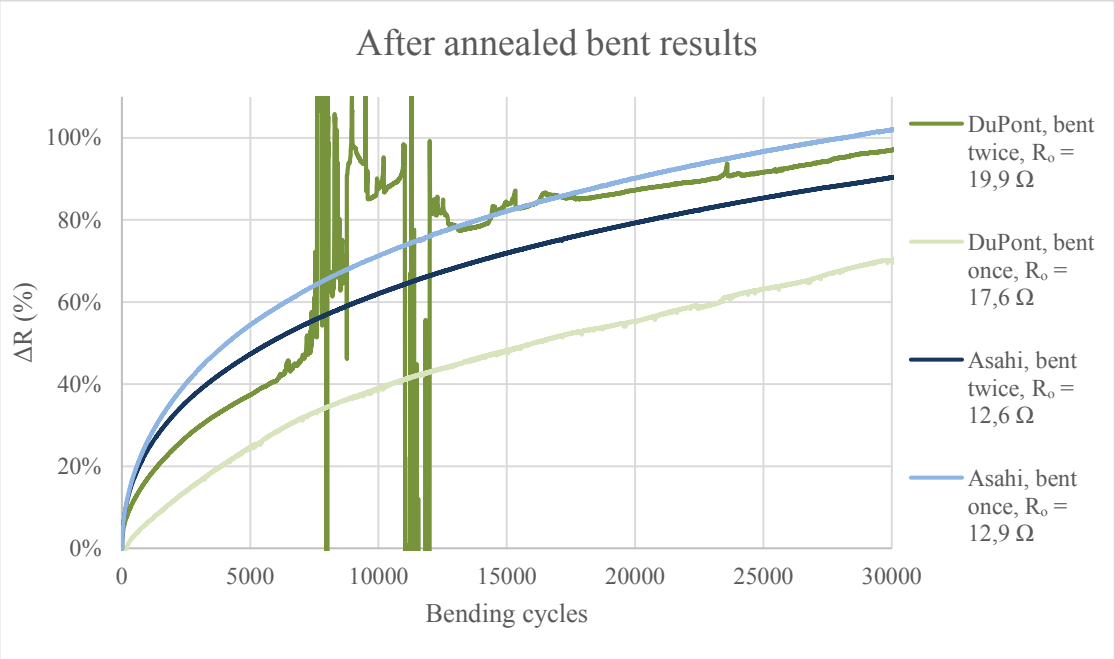


Figure 39: Cycle-annealed-cycle -measurement results.

The bending after bending and annealing shows that both of the inks can restore well after cyclic bending. When the sample is cycled again, the resistance does not have the same kind of effect as in the cycle-rest-cycle –measurement. However, the ink is not as bendable as before when using the DuPont ink and two of the vias from one of the sample line broke during the measurement. The interconnection starts to break after 8000 bending cycles and breaks completely shortly after the shown 30 000 bending cycles. The Asahi ink on the other hand restores almost completely to the starting value of the measurement and the resistance change follows the same trend as the first cyclic bending measurement. It seems that the bending memory can then be erased by annealing again with Asahi ink.

The second time bent samples were again annealed and characterized with a multimeter. The results of bent samples are gathered in Table 19.

Table 19: Bend-anneal-bend-anneal results measured with a multimeter.

Sample	R_0 (Ω)	After bending 1 (Ω)	After anneal 1 (Ω)	After bending 2 (Ω)	After anneal 2 (Ω)
Asahi	13	25,4	12,6	23,1	13,7
DuPont	17,7	29,6	19,6	36,4	26,6

The bending and annealing results show that the first post bend annealing lowers the resistance near the starting resistance value with Asahi ink. With DuPont the resistance

value also lowers, but is clearly higher than the starting value. During the second bending and annealing cycle, the trend is the same as in the first bend and anneal cycle, but the resistance does not drop to the starting resistance value. With DuPont ink, the resistance value rises after each post anneal compared to the starting value. Asahi ink on the other hand heals completely during the first annealing, but on the second anneal, the resistance is higher compared to the starting value. This case study revealed silver conductor ink healing capabilities, which requires another study to understand the phenomena. Y. Han and J. Dong have also showed the self-healing capability of a conductor line in their work using molten low melting point metal alloy and electrohydrodynamic printing method [60].

To summarize the bending tests, 1122 vias were bent and measured. Four of the vias broke in the measurements, where one of the vias was considered a poor via in the initial electrical analysis, one broke after the bending was over in the smaller plate distance measurement and two were broken in the cycle-anneal-cycle measurement. All the broken vias were noticed using the DuPont ink and nominal via diameters of 50 and 100 µm. The resistance of a conductor line rose in every cyclic bending measurement, but lowers when at rest and heals well when annealed again. A single via resistance change after 30 000 bending cycles is between 0,05 – 0,3 Ω, depending on the via size and ink used. Smaller via sizes have smaller collar and stronger strain is focused on it resulting higher resistance change.

4.1.4 Optical characterization of bent via

Scanning electron microscope (SEM) images were taken from the bent vias and compared to non-bent reference sample. The images were taken on top of the via from the tensile stressed side. The SEM images showed clear difference between non-bent and bent sample and are shown in Figure 40.

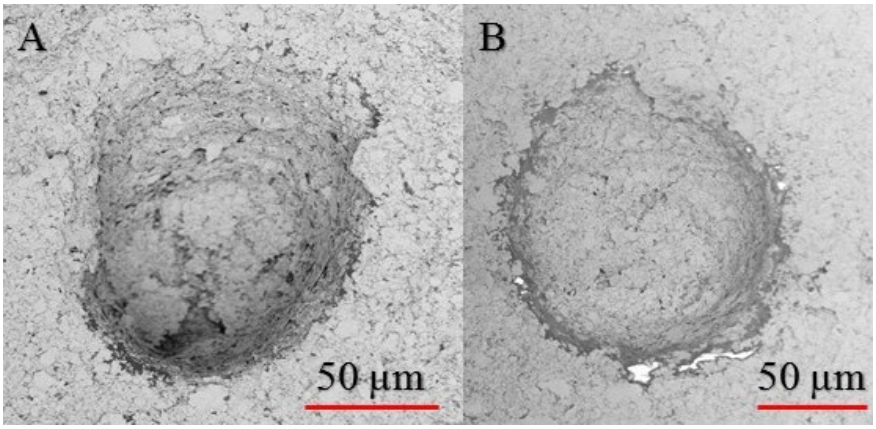


Figure 40: Before bent (A) and after bent (B) sample images with DuPont 100 µm via diameter.

The SEM images in Figure 40 show increased dissociation of silver micro particles (flakes) around the via collar. The local stretching strain of the collar ink relative to the perpendicularly oriented via induces microcraks around the via cavity. This in turn lead to increased resistance of the via seen in Figure 33. This observed effect is corroborated by the theoretical modelling performed by Petér *et. al.* shown in Figure 7.

4.2 Supercapacitor

The next chapter introduces the supercapacitor characterization results. Supercapacitors were assembled the method stated in section 3.2.1 and measured. The supercapacitors were assembled with and without screen printed vias.

4.2.1 Supercapacitor characterization results

The reference supercapacitor in the measurement device is shown in Figure 41. Four probes are attached to the electrode where two of the probes feed current to the super-capacitor and two other probes measure the voltage over the capacitor.

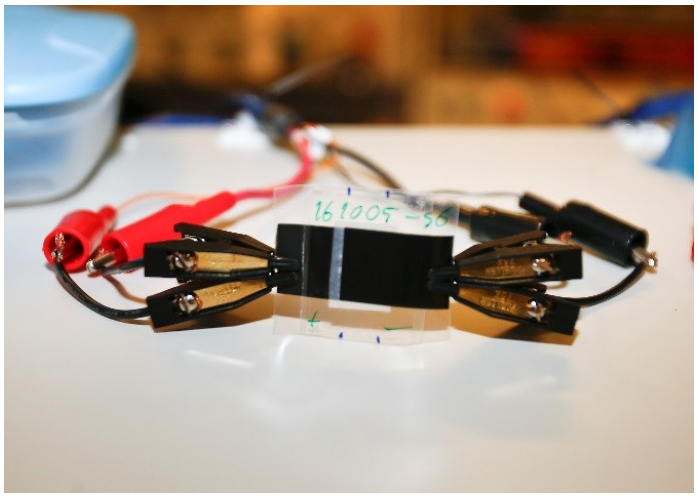


Figure 41: Reference supercapacitor attached to the measurement device.

The measurement results of the reference samples are shown in Table 20. The Table 20 has information of supercapacitors capacitance, ESR and current leakage

Table 20: Measurement results from reference supercapacitors.

Sample	**Capacitance** (mF)	**ESR** (Ω)	**Current leakage** (µA)
Sample 1	309,4	35,7	8,1
Sample 2	313,0	14,9	8,6
Sample 3	425,3	16,9	12,8
Sample 4	404,8	14,1	9,9

It was noticed from the measurement results, that the capacitance varied a little, since the AC layers were printed onto electrode by hand seen in Figure 18. The current leakage and ESR values stay relatively same as in other same material and structure supercapacitors [61].

4.2.2 Supercapacitor design with printed through-hole via

The supercapacitor's graphite layer was printed on top of a silver pad, which led to a printed through hole via. The same electrical properties were measured with the combined structure of screen printed via and supercapacitor as the reference supercapacitors. A supercapacitor, which was connected with a through-hole via is shown in Figure 42.

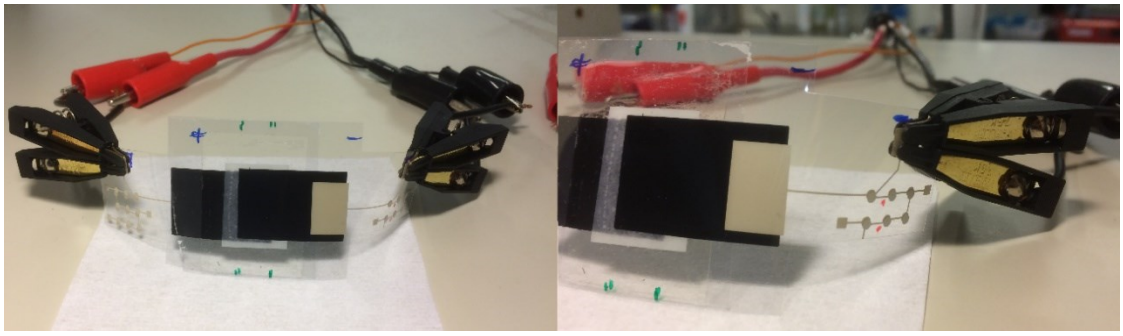


Figure 42: Supercapacitor with through hole via.

The supercapacitors were combined with vias in positive, negative or positive and negative electrodes. The Asahi and DuPont inks were again compared to each other by creating the supercapacitor and screen printed via structure with both inks. Since the resistance of the vias were not as high as the resistance of the graphite current collector, the silver lines could have multiple vias attached. The results from the supercapacitor and printed through hole via structure are shown in Table 21.

Table 21: Supercapacitor and screen-printed through hole via combined structure measurement results. The location of vias indicates on which side the via was between positively and/or negatively charged electrode.

Sample (ink)	**Capacitance** (mF)	**ESR** (Ω)	**Current leakage** (µA)	**Number and location of vias**
Sample 5 (Asahi)	339,5	23,8	9,8	+:1 via
Sample 6 (Asahi)	385,2	22,2	10,9	-:1 via
Sample 7 (Asahi)	335,8	26,8	7,7	+:3 vias, -: 1 via
Sample 8 (DuPont)	371,9	30,5	11,2	+:1 vias
Sample 9 (DuPont)	315,2	15,5	8,7	-:1 vias
Sample 10 (DuPont)	339,9	21,9	9,0	+:3 vias, -: 3 via

The comparison between Table 20 and Table 21 results shows that there is not much of a difference in the electrical properties in the via combined structure. However, the ESR values are a few ohms higher in average compared to reference supercapacitors. This is mainly due to the increased resistance of the silver conductor line where the measurement probe is attached.

The measurement was done to proof that the screen printed via can be used together with the supercapacitor electrodes. The combined structure is beneficial for R2R manufacturing of the energy module. The printed through hole vias also help to assemble a fully sealed supercapacitor structure as will be discussed in section 5.2.1.

4.3 Energy module prototype

Finally, a prototype of the energy module was built with all the necessary components, OPV, supercapacitor, printed through hole via and diode. All other components in the prototype can be R2R manufactured except the diode. The energy module was also attached onto a LED which emitted light after its threshold voltage of 2,4 V. The built prototype is shown in Figure 43.

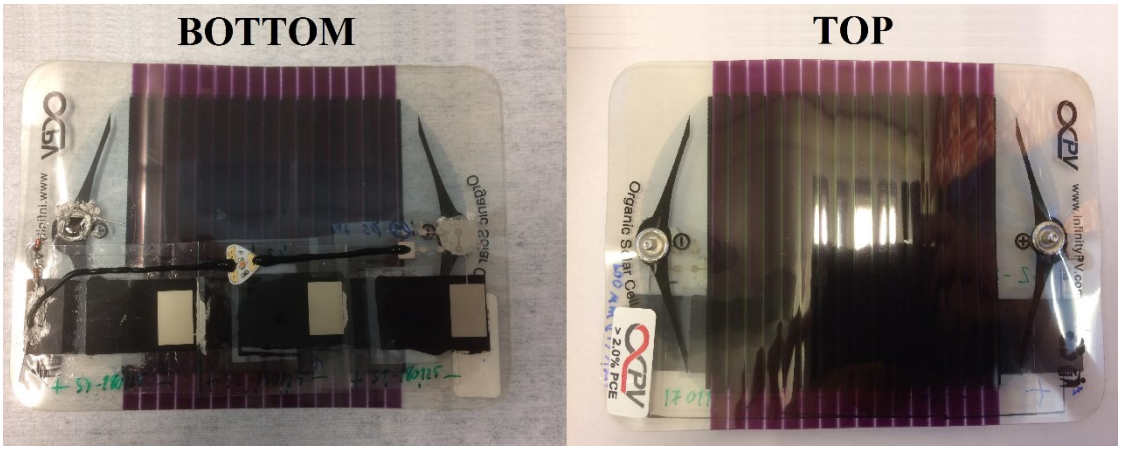


Figure 43: Built prototype of the energy module.

4.3.1 Electrical performance

First the three-supercapacitor structure was measured to ensure the combined structure's electrical properties. Two reference samples and one screen printed via and supercapacitor combined structure sample were chosen for the energy module. The measurement was utilized the same way as the reference samples and the screen-printed via and supercapacitor combined structure. The measurement results are shown in Table 22.

Table 22: Measurement results from the three supercapacitors in series structure.

Capacitance (mF)	**ESR** (Ω)	**Current leakage** (µA)
97,5	46,57	4,0

The built prototype was measured with a voltage multimeter. The energy module was charged with a lamp with 20 cm and 40 cm distances. These two different distances were used to charge the energy module for 15 minutes and then left in the dark. After 15 minutes, the energy module's supercapacitors discharged through the LED and it illuminated light. The measurement results of the prototype charging and discharging are shown in Figure 44.

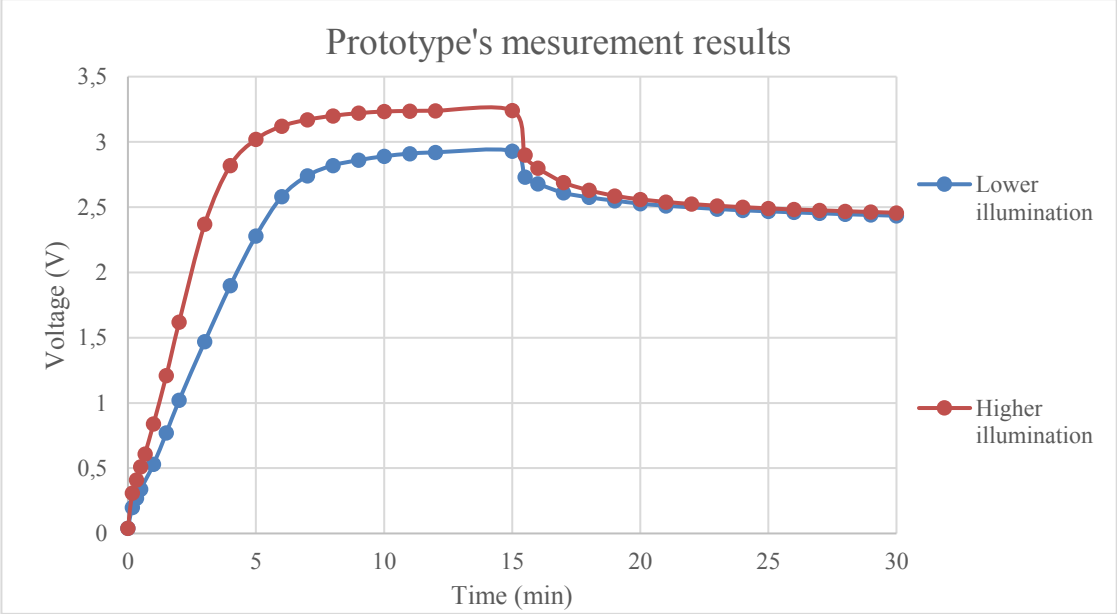


Figure 44: Built energy module's measurement results. The illumination was stopped after 15 minutes in the measurement.

The energy module's voltage seems to level down to almost 3 V with the lower illumination and approximately 3,2 V with the higher illumination measurement when charging, according to Figure 44. After the lights are turned off, at 15 minutes in the measurement, the voltage starts to drop rapidly mainly because of the discharge through the connected LED. The voltage seems to level approximately to 2,4 V, which is the threshold voltage of the LED. After that, the LED does not need current and only component drawing power from the supercapacitors is the non-idealities of the supercapacitors, which is the leakage current. This measurement proves that the energy module is capable of charging supercapacitors with light and discharging the energy through an external application.

The energy module's maximum voltage is limited by the supercapacitors. In this case, the maximum voltage is 3 * 1,23 V = 3,69 V. This voltage is not exceeded in the measurement. However, the voltage is divided slightly differently among supercapacitors if

the supercapacitors capacitances are unequal. The maximum voltage of 3,69 is in reality even less. The maximum energy calculations are provided in the section 5.1.

5. ENERGY MODULE DESIGN

The next chapter introduces some basic calculations that can be made from the energy module. In chapter 5.2 the materials and methods for the energy module are listed. Finally, a directional proposal for the energy module is given to produce it in the R2R monolithically integrated and printed fabrication process.

5.1 Energy characteristics

The prototype has three supercapacitors in series in the energy storage. The energy storage's maximum voltage is then three times the maximum voltage value over one capacitor, which is 1,23 V using aqueous electrolyte. Maximum voltage is then 3,69 V. However, the voltage can divide differently among series connected supercapacitors, if the capacitance values are not equal in the series connection. Safety margin is then necessary and the maximum voltage can thought to be 3,3 V.

Low energy microcontrollers work in voltages between 3,6 V – 1,8 V, according to Table 6 and Table 7. The operating voltage range is then between maximum voltage of the supercapacitors and minimum voltage of the microcontrollers

$$V_{SC_{MAX}} - V_{Controller_{MIN}} = 3{,}3V - 1{,}8V = 1{,}5\,V. \tag{12}$$

Losses of the energy storage depends on the ESR value and current. Losses limit the time that the energy storage can provide current in the voltage range. Time that the energy storage can provide energy can be calculated from the voltage over supercapacitors and energy loss from the ESR:

$$V_{operation} = \frac{I * t}{C} + I * ESR \leftrightarrow t = \frac{C\left(V_{operation} - I * ESR\right)}{I}. \tag{13}$$

In the prototype, capacitance was 100 mF and maximum voltage 3,3 V. We can lock these two values and plot ESR versus time chart with a few different current values. The plot is shown in Figure 45.

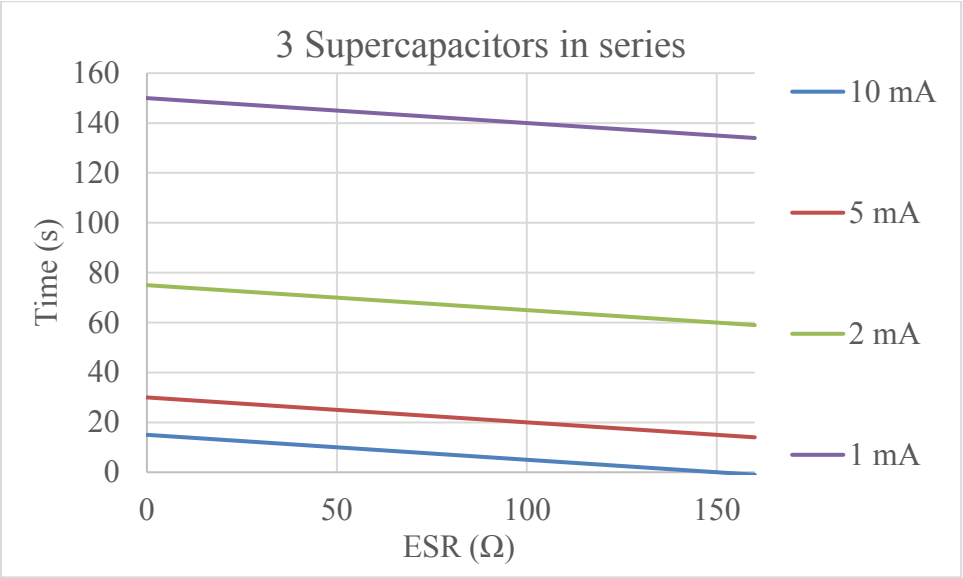


Figure 45: Theoretical time that 100mF supercapacitor can provide energy with different ESR values in four different current cases.

It can be seen from Figure 45, that the built prototype, with ESR value 45 Ω, can release 1 mA current for over two minutes, 2 mA current for over one minute, 5mA current for over 20 seconds and 10 mA current for less than 10 seconds, when the energy storage has been loaded for its maximum capacity. The end use application for nearables concept is ought to be a few second 1 mA – 10 mA current peaks every now and then. The nearables energy demands are then fulfilled by the prototype's energy storage. However, the low energy wireless transceiver protocol, ZigBee, requires approximately 35 mA current for 63,5 ms time interval [36]. This requirement is too high for the prototype, when calculating it with the equation (13). If the end use application is meant for autonomous sensing, the energy requirements according to Table 7 is only 0,21 – 0,11 mA. Then the prototype can provide energy for the microcontroller in active mode for 21 to 11 minutes according to equation (13).

Most of the energy is drawn by the losses of the ESR in high current values. ESR can be dropped by thickening the graphite layer, having silver pad next to the AC or extending the width of the graphite layer. More energy can be provided with larger capacitor values or assembling fourth supercapacitor in series to the structure. However, these will increase the total ESR value, since the capacitor area is enlarged or fourth supercapacitor is placed. Overall, maximum energy is achieved with high capacitance values and low ESR values.

The harvested energy from the OPV comes from the ambient office light. A general office space lighting has 300-500 lux of light [62]. In these cases, the energy harvested is 3 – 5 W/m^2 or 300 – 500 $\mu W/cm^2$ [63]. The PCE of the prototype's OPV was 2%. In well lighted office this means 500 $\mu W/cm^2$ * 0,02 = 10 $\mu W/cm^2$. The prototype effective area of the OPV was measured to be 8 cm * 8 cm = 16 cm^2. This means the harvested

energy of 10 µW/cm^2 * 16 cm^2 = 160 µW. The supercapacitors will be fully charged by dividing the maximum energy of the supercapacitors with the harvested power from the OPV:

$$time = \frac{E}{P} = \frac{\frac{1}{2}CU^2}{P} = \frac{\frac{1}{2} * 0{,}1F * 3{,}3V^2}{160\ \mu W} \approx 3400s = 57\ min. \quad (14)$$

where E is the maximum energy of the supercapacitors and P is the power that comes from the OPV when illuminated with office light. The prototype's supercapacitors are charged into their maximum capacity in an hour at regular office lighting. The end-use application determines heavily whether the harvested power is sufficient. For example, if the device needs to be operated during nighttime using an internal clock, then the supercapacitor needs to have better energy storing properties. At daytime, the excess power from the OPV is charged to the supercapacitors and both components can provide energy to the end application.

Other energy calculations with the OPV and supercapacitor energy module have been made in [63] with promising results. Rinne *et. al.* researched the reliability of OPV and supercapacitor components using supercapacitor with 0,5 F capacitance, OPV with 4 cm^2 area and efficiency of 3 % and 10 % and with different light illuminations between 200 – 1000 lx. The energy drawn was taken from IEEE 802.11ah path loss model for indoor case [64]. The results show that one day operation is achieved [63].

For practical perspective, the energy module needs to be placed so that the open circuit voltage of the OPV does not exceed the supercapacitor maximum voltage. The used diode can also help to drop voltage into a sufficient level. In this case the energy module light input should be almost constant, which means that the energy module can not be moved around since that the intensity of light changes. More research should be done to overcome this obstacle for example to use a charge pump, which rises the voltage to a sufficient level even with low light intensity. Other components that can be used are a zener diode or a regulator, which prevents overvoltage situation. The zener diode is like a normal diode, but it starts to conduct from cathode to anode when enough voltage is applied between the terminals of the zener. The regulator keeps the voltage on a certain level. Regulators can also be used in the application side, since the voltage from the supercapacitors drops down linearly and some microcontrollers require a steady voltage. Regulator also prevents the overvoltage situation. However, regulators are much more complex components compared to zener diodes.

5.2 Roll-to-Roll manufacturing

All the energy module components need to be printed. The basic R2R produced inverted OPV architecture is shown in Figure 10. The materials for OPV can be whether gravure

and screen printed or slot die coated [3, 44]. Supercapacitor electrodes have been produced earlier in the screen printing process, shown in Figure 46, but a machine has not assembled them previously. The separator and electrolyte placing are difficult to execute in an assembly line. However, the paper separator can be placed with another printable material such as a hydrogel [65]. The materials and methods to produce supercapacitor, OPV and the needed diode are shown in Table 23.

Table 23: Materials and methods for energy module fabrication.

Component	Materials	Printing method
Organic photovoltaic cell	- PET-ITO - ZnO - P3HT:PCBM - PEDOT:PSS - Silver ink	- Gravure- and screen printing or slot die-coating
Supercapacitor	- Graphite - Activated carbon - Dreamweaver separator or starch gelatin hydrogel - 1 mol/l NaCl	- Screen print - Pick & place
Diode	- Copper - PTAA - Silver ink	- Evaporation - Gravure printing

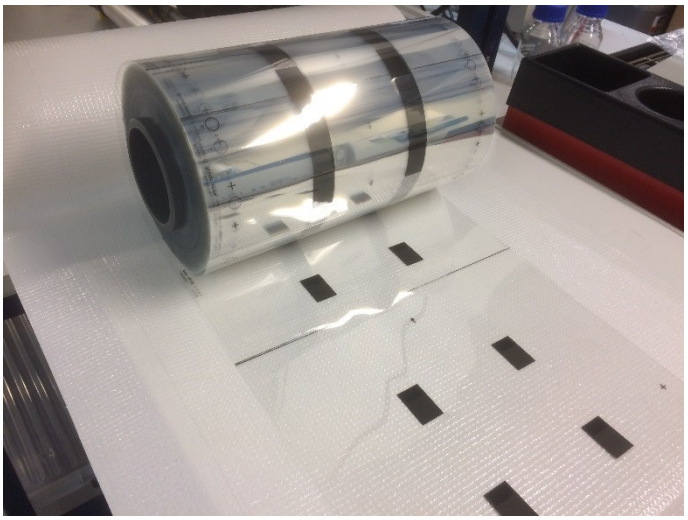


Figure 46: R2R screen printed supercapacitor electrodes.

All the materials can be printed on the substrate except the copper, which needs to be evaporated. The copper can be evaporated into the substrate before the substrate goes to the assembly line. The through hole vias also need to be laser-cut onto the substrate before printing process can begin.

5.2.1 Proposal for energy module design and manufacture

The supercapacitor reference structure is shown in Figure 9. An all sealed structure can be made using the printed through hole via. A silver pad can be printed on top of the graphite electrode or beneath the graphite layer, which both then lead to a screen printed via. A structure from the all sealed structure is shown in Figure 47.

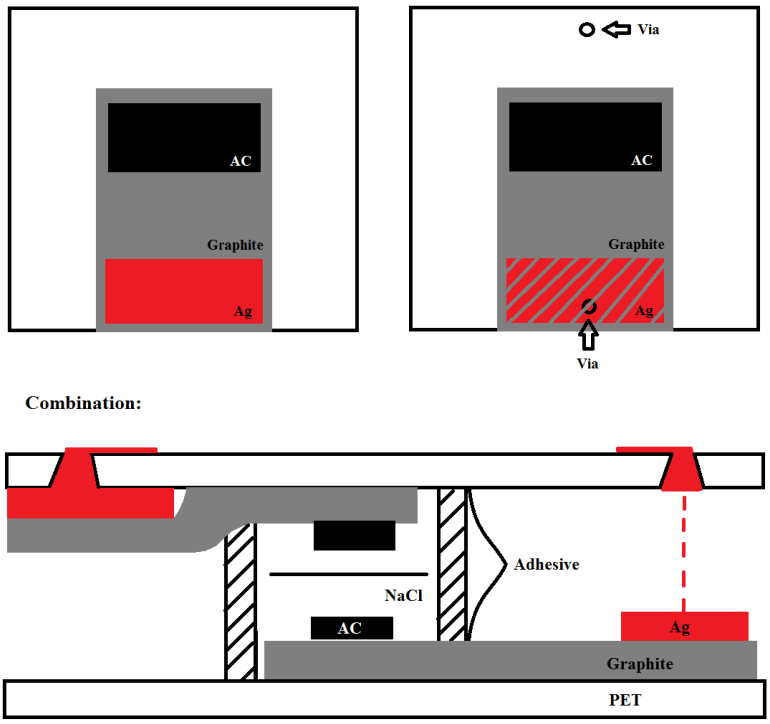


Figure 47: Proposal for supercapacitor with corresponding printed through-hole vias.

The supercapacitors can be further chained in series with the screen-printed vias by monolithic integration. When the supercapacitors are an even number, then only one via is needed in the other electrode instead of having a via in top of the electrode as seen in Figure 47. A chained structure with two and three supercapacitors in series using screen-printed vias is shown in Figure 48.

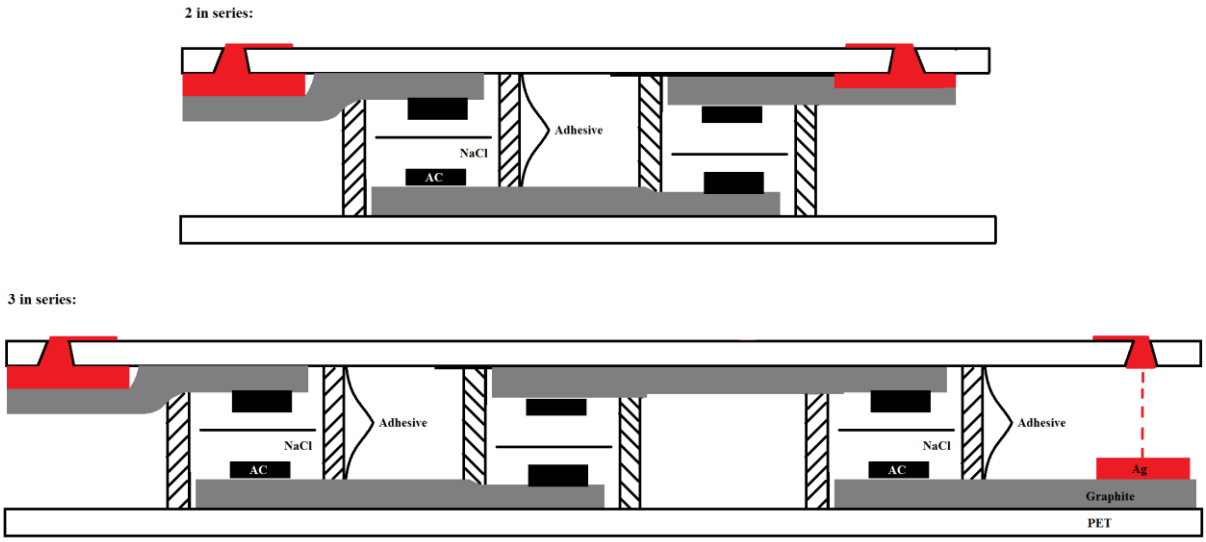


Figure 48: A proposed structure of two and three supercapacitors connected monolithically integrated in series with the screen-printed through-hole vias.

The supercapacitor and OPV interconnection can be done using the screen printed through-hole via. The diode needs to be placed between the positive electrodes of the OPV and supercapacitors. A proposal for the energy module is shown in Figure 49.

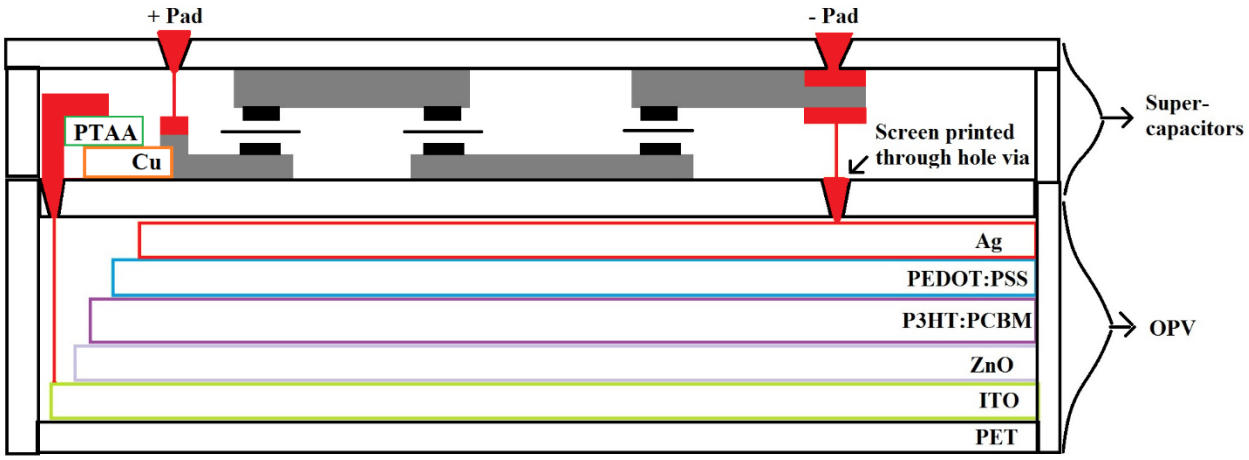


Figure 49: Proposed monolithically integrated energy module structure.

If the energy module is needed to print monolithically, then the assembling of the module can be done separately. First three substrates are prepared. One of the substrates has the patterned ITO layer, second substrate has two laser-cut vias on marked spots and the diode's copper layer evaporated on it and the third substrate has two laser-cut vias cut on specific spots. The OPV stacked structure is printed on top of PET-ITO substrate in the first substrate. Then to the second substrate, supercapacitor silver pads, graphite electrodes, diode's PTAA and silver layers are printed. Then the first and second substrate are connected to each other with adhesive- and sealing foil. The screen-printed vias are then printed on top of second substrate to create connection between both OPV's

ITO and diode's copper layer and OPV's silver layer and supercapacitor structures negative terminal. Since the OPV is vulnerable to water and oxygen, the structure is sealed together in 300 newton high pressure. Finally, the third substrate's silver pads and supercapacitor's graphite layers and AC layers are printed. Then all the substrates are connected to each other by first applying the NaCl electrolyte and separator to the supercapacitors. The substrates are again connected using adhesive foil. The final energy module can have two silver pads printed on top of the top electrode for external application.

The sintering of each layer needs to be done after each printing process. This might lead to thermal crossovers and complications in the materials. For example, if all the layers are stacked on top of each other and sintered after each print, lowest layers face multiple thermal cycles, which might lead to ink material poor adhesion. That is why the printing to each substrate is beneficial to do separately and combined in the last stage.

The main idea of the proposal is to give perspective to the energy module fabrication. However, more research is required for placing the energy module into a fabrication line. For example, the alignment and ink dimensions should be considered.

6. CONCLUSION

The IoT and IoE devices require energy autonomy with environmentally sustainable materials. The thesis described an energy module, which was done with a supercapacitor energy storage component and an OPV energy harvesting component. The two components have a diode separating them to prevent supercapacitor spontaneous discharge. All components can be fabricated using printed electronics and environmentally friendly materials. These components were proposed to connect together using a screen-printed through-hole via to achieve a fully printed energy module fabrication process. A prototype of the energy module was fabricated with all main components that were required to the module. The prototype was measured and calculations were made to evaluate its energy capabilities in the IoT and IoE applications. The long-term vision is to print the whole energy module in one R2R fabrication process and a design proposal for the R2R printed energy module is shown in the thesis.

The screen-printed through-hole via fabrication was evaluated with two different silver inks and four different via sizes and reliability of the interconnection was assured with a cyclic bending test. The screen-printed through-hole via was filled during the screen-printing process. A thicker Asahi LS411AW paste performed better in the printing process compared to thinner DuPont 5064H ink. The Asahi ink's yield of fully functional vias was 99,67% and DuPont's was 96,57%. Four different nominal via sizes: 50 µm, 100 µm, 150 µm and 200 µm were compared to each other, where 100 µm had the best yield with both used inks.

In the bending analysis of the screen-printed via, printed sample structure with vias was attached into a pneumatic bending machine and resistance of the daisy-chain sample structure line was measured while being cyclic bent. The resistance of a printed line rose in every cyclic bending measurement. A clear connection breakdown limit between the substrate's top and bottom side prints was not found in the bending tests despite doing longer bending cycle tests or by having the printed line face more stress by downsizing the bending radii. Four connection breakdowns occurred in 1122 bent vias, and the four broken vias were found using the lower viscosity DuPont ink. The via bending had a little effect on the overall resistance change in the sample line. However, larger via sizes were seen to perform better while bent. The DuPont ink performed better over Asahi ink during bending probably due to thinner print line or larger silver particle size.

A supercapacitor and a screen-printed through-hole via combined structure was tested as a proof of principle before the energy module prototype fabrication. The results show that the screen-printed vias can be used together with the supercapacitor. After the proof of principle, a prototype of the energy module was fabricated. The prototype had a commercially available OPV, in TUT fabricated supercapacitors and commercially available

diode combined with screen-printed through-hole vias. The prototype was charged with a lamp and the collected energy was stored to the supercapacitors. After charging for a while, the lights were turned off and the energy was discharged through a LED, which emitted light.

The energy module prototype calculations showed that it can produce enough energy for low energy IoT microcontrollers, which require quick current peaks in longer time intervals. The fabrication process of the energy module was considered in a R2R process. A proposal for the energy module structure was given and was evaluated. The proposal provides guidance for future research and how the energy module can further be developed.

6.1 Future work

The main research topic in this thesis was the screen-printed vias. The vias were managed to fabricate and their reliability was good after all. More research should be done to determine the most optimized ink and via diameter combination. The viscosity was ought to be a key parameter in the reliable via filling. Modelling could provide more information of how the via is filled in the fabrication process.

An intriguing side study was found during the bending tests, which was the self-healing of a cyclic bent conductor line. The conductor line's resistance rose, when cyclic bent, but drops back down to the non-bent resistance value after the sample was annealed. The self-healing effect of a printed line could be useful in electronics, which are cyclic bent into a point that it is no longer useful because of high resistance value. The annealing could make the application useful again. More studies than a case study could be made to provide more information about the self-healing and rearrangement of silver particles. For example, a measurement with thorough cycle-anneal measurements with various inks could give sufficient information of self-healing.

The final dimensions of each component in the energy module needs to be considered for the end-use application more thorough. For example, the end-use application energy requirements demand certain specifications for the quality of power that the energy module should provide. In most cases, the microcontroller, that controls the application, requires a steady voltage for stable operation. However, the supercapacitor's voltage drops linearly when discharged. The voltage can be kept steady by regulating the voltage with an external circuit or regulator.

If the illumination is high, the supercapacitor might face overvoltage, which causes high leakage current in the supercapacitor. An overvoltage protection could be useful, if the illumination of light is not well controlled or is not constant. The overvoltage protection can be made by, for example, adding a zener diode in parallel with the supercapacitors.

This thesis introduced a reasonable architecture for the energy module to work with low energy IoT and nearable devices. However, feasibility of a fully printed structure can be challenging. For example, the accurate alignment of printed layers, the electrical connection between multiple substrates, and other concrete details to fabricate the energy module were not researched in the thesis.

One final note is the OPV's durability to withstand air humidity, which can penetrate through the screen-printed via structure. Further studies should be done to bring more information of how the humidity and oxygen can penetrate through the ink. The study could tell how long the OPV lasts in the proposed structure.

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