TAMPEREEN TEKNILLINEN YLIOPISTO
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PASI HEINONEN

FABRICATION OF ORGANIC TUNNEL DIODES WITH ULTRA-THIN TiO_2 INTERFACIAL LAYERS

Master of Science Thesis

Examiners: Professor Donald Lupo
Professor Nikolai Tkachenko
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ABSTRACT

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Organic tunnel diodes that exhibit negative differential resistance (NDR) at room temperature offer novel opportunities for organic logic circuits and memories. These devices could be utilized e.g. in printed logic circuits with the advantage of lower power consumption and reduced amount of devices required. Reproducible, room temperature NDR has been shown for organic devices with ultra-thin titanium dioxide interfacial layers incorporated into an otherwise conventional Schottky diode structure. However, for industrial applications, the device fabrication process should be suitable for high-throughput processes. The specific issue is the fabrication of the interfacial oxide layers.

In this work, two methods to fabricate the oxide layers were utilized: anodic oxidation and atomic layer deposition (ALD). The aims of this study were: to successfully fabricate the oxide layers, to characterize the layers, to fabricate organic tunnel diode devices with these oxide layers and to characterize the device electric properties. The ultra-thin oxide layers were fabricated on rigid indium-tin-oxide (ITO) substrates. Vertical ITO/TiO_2/semiconductor/aluminum -device structures were fabricated. The oxide layers were analyzed with x-ray photoelectron spectroscopy (XPS) and Mott Schottky analysis. Current-voltage (I-V) measurements were performed for the fabricated devices.

TiO_2 layers of different thicknesses with high defect density as required for the tunneling process were successfully fabricated with the anodic oxidation method. The dielectric constant and defect density were 18 and 5×10^{19} cm^{-3}, respectively, for the anodized layers. Fabricated devices with anodized oxide layers showed an N-shaped I-V characteristic with room temperature NDR. Observed peak-to-valley current ratio (PVCR) was up to 3.2, which is enough for some novel logic circuits. The oxide thickness didn't affect the results significantly, except for the thickest layer, which might have been incompletely oxidized. The ALD grown layers had high impurity content due to unsuitable patterning method, but the ALD process itself proved very promising for these oxide layers. The devices with the ALD grown layers showed stronger NDR than the devices with the anodized layers. The exact cause for this is still unclear. A lot of work is still required in the research of the devices. Device operation reliability and air stability needs to be improved. In addition, the exact operational principle of the devices remains unclear. Experiments with different semiconductors and electrodes could be highly useful for future work.

TIIVISTELMÄ

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Orgaaniset tunnelidiodit, joilla esiintyy negatiivinen differentiaalinen resistanssi (NDR) huoneenlämpötilassa, tarjoavat uusia mahdollisuuksia orgaanisten logiikkapiirien ja muistien kehittämiseen. Näitä elektroniikan komponentteja voitaisiin hyödyntää esim. painettavissa logiikkapiireissä, jolloin voitaisiin saavuttaa pienempi tehon kulutus ja pienempi tarvittavien komponenttien määrä. Toistettava, huoneenlämpötilassa toimiva NDR on havaittu orgaanisille komponenteille, joissa muuten tavalliseen Schottky diodiin on lisätty erittäin ohut titaanidioksidi-rajapintakerros. Nämä komponentit tulisi kuitenkin valmistaa suurtuotantoon soveltuvin keinoin, jolloin erityisen ongelman aiheuttaa olennaisen titaanidioksidikerroksen valmistus.

Tässä työssä käytettiin kahta eri menetelmää mainittujen TiO_2 kalvojen valmistamiseksi: elektrokemiallista hapettamista ja ALD:tä (*eng. atomic layer deposition*). Työn tavoitteina oli: valmistaa oksidikerrokset onnistuneesti, tutkia oksidikerrosten ominaisuuksia ja valmistaa orgaanisia tunnelidiodeja. Ohuet oksidikerrokset valmistettiin jäykkien indium-tina-oksidi (ITO) substraattien päälle. Diodit valmistettiin vertikaalisina ITO/TiO_2/orgaaninen puolijohde/alumiini -kerrosrakenteina. Oksidikerroksia tutkittiin röntgensäde-fotoelektronispektroskopialla (XPS) ja Mott-Schottky analyysillä. Valmistettujen diodien käyttäytymistä tutkittiin virta-jännite (I-V) mittauksilla.

Elektrokemiallisella hapettamisella valmistettiin onnistuneesti eri paksuuden omaavia TiO_2-kalvoja, jotka sisälsivät paljon defektejä. Kalvoille mitattu dielektrisyysvakio oli 18 ja defektitiheys oli 5×10^{19} cm^{-3}. Hapetetut oksidikerrokset sisältävillä diodeilla havaittiin huoneenlämpötilassa N-muotoinen I-V riippuvuus, jossa esiintyi NDR alue. Mitatut PVCR-arvot (*eng. peak-to-valley current ratio*) olivat enimmillään 3,2; mikä on riittävä arvo mahdollisiin logiikkapiirisovelluksiin. Oksidikerroksen paksuus ei vaikuttanut käyttäytymiseen huomattavasti paitsi paksuimmalla kerroksella, joka ei tosin ollut välttämättä täysin hapettunut. ALD:llä kasvatetut kalvot sisälsivät paljon epäpuhtauksia johtuen käytetystä soveltumattomasta tavasta valmistella näytteet. Kuitenkin, itse ALD-prosessin hyvä soveltuvuus kyseisten oksidikerrosten valmistamiseen kävi ilmi. Diodeissa, jotka sisälsivät ALD valmisteiset oksidikalvot, havaittiin voimakkaampi NDR kuin aiemmin mainituissa, mutta tarkkaa selitystä tähän ei tiedetä. Orgaanisissa tunnelidiodeissa riittää vielä paljon tutkittavaa ja kehitettävää. Diodien toimintaluotettavuutta ja ilmastabiiliutta pitäisi parantaa. Lisäksi, diodien tarkkaa toimintaperitaatetta ei vielä tunneta.

PREFACE

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Tampere, May 18th 2015

Pasi Heinonen

CONTENTS

LIST OF ABBREVIATIONS AND SYMBOLS

AE	auxiliary electrode
CB	conduction band
CE	counter electrode
CVD	chemical vapor deposition
C-V	capacitance-voltage
DC	direct-current
DI	deionized
EC	equivalent circuit
EIS	electrochemical impedance spectroscopy
ESCA	electron spectroscopy for chemical analysis
HOMO	the highest occupied molecular orbital
IPA	isopropanol
ITO	indium tin oxide
I-V	current-voltage
LUMO	the lowest unoccupied molecular orbital
MEH-PPV	poly[2-methoxy-5-(2'ethyl-hexyloxy)-1,4-phenylenevinylene]
OCP	open circuit potential
OSC	organic semiconductor
PPV	polyphenylenevinylene
PSI	phase shifting interferometry
PVD	physical vapor deposition
PVCR	peak-to-valley current ratio
R2R	roll-to-roll
RC	resistor-capacitor
RE	reference electrode
RT	room temperature
SCR	space-charge region
SHE	standard hydrogen potential
TDMAT	tetrakis(dimethylamino) titanium
UHV	ultrahigh vacuum
UV	ultraviolet
VB	valence band
WE	working electrode
XPS	x-ray photoelectron spectroscopy

A	active area of the working electrode
A_{sc}	area of the semiconductor-electrode interface in C-V measurement
C_{dl}	capacitance of the electrical double layer
C_{tot}	total capacitance
C_{scr}	capacitance of the space charge region
d	anodized oxide thickness
d_{native}	native oxide thickness
d_{tot}	total oxide thickness
E	electric potential
E_0	energy of the potential barrier
E_B	binding energy of a photoelectron

E_C	conduction band edge energy
E_F	Fermi level energy
E^o	standard reduction potential
E^o_{ox}	standard oxidation potential
E_k	kinetic energy of a photoelectron
E_n	energy of a particle
E_V	valence band edge energy
E_{Vac}	vacuum level
e	elementary charge
F	electric field strength
f	frequency
h	Planck's constant
$\hbar$	reduced Planck's constant
I	electric current
I_0	amplitude of sinusoidal current response
I_p	peak tunneling current
I_v	valley current
i	sinusoidal current response signal
J_p	peak current density
J_v	valley current density
k_B	Boltzmann's constant
m	mass
M	molar mass
N_D	doping density
N_{Def}	defect density
n	electron density
p	hole density
Q	electric charge
R	resistance
R_{el}	electrolyte resistance
S	slope of the Mott-Schottky plot
T	absolute temperature
T_t	transmission coefficient
t	time
V	cell voltage
V_0	amplitude of sinusoidal voltage signal
V_p	peak voltage
v	sinusoidal excitation voltage signal
V_{fb}	flat-band potential
W	depletion region width
W_{scr}	width of the space charge region
Z	impedance
Z'	real part of impedance
Z''	imaginary part of impedance
z	valency number of ion
ε_0	permittivity of vacuum
ε_r	dielectric constant
κ^{-1}	decay length
ρ	density
ρ_c	charge density

Φ	potential difference
ϕ	phase angle
ϕ_{spec}	work function of the spectrometer
φ	work function
φ_m	metal work function
φ_s	semiconductor work function
Ψ	wavefunction
ω	radial frequency

1. INTRODUCTION

Since the discovery of almost metallic level of conductivity in organic polymers in the 1970's [1], the field of conducting polymers has gained much attention. Later on, Heeger, MacDiarmid and Shirakawa were awarded the Nobel Prize in Chemistry in 2000 for the significance of this early work [2]. Conducting polymers are integral for the interdisciplinary fields of organic, printed and flexible electronics. Altogether, these fields are expected to reach a market worth of over $73B by 2025 [3]. The key advantage of organic semiconductors and conductors is that they combine some of the best parts of conventional polymers and inorganic semiconductors. Organic semiconductor devices are typically cheaper, lighter, more flexible and easier to fabricate than inorganic semiconductor devices. These materials are often solution processable, which enables the use of cheap high-throughput low-temperature fabrication methods such as printing methods. Organic devices can't compete with inorganic ones in conventional applications, but their advantages are especially suited for large-area and flexible applications. The most researched organic electronic devices include OLEDs [4] and solar cells [5].

Printing methods are a viable way to fabricate organic electronic devices. For example, radio frequency identification (RFID) tags based on printed circuits are one possible application [6]. Large footprint and complex circuit design are big issues with printed components. Some applications such as smartcard technology require onboard memory and logic circuits. Polymer based tunnel diodes have been shown to allow novel opportunities in memory and logic circuit design [7], because of their N-shaped current-voltage (I-V) characteristics. These circuit designs reduce the required amount of devices drastically in the logic circuits. In addition, the power consumption is decreased in these circuits. Therefore, organic tunnel diode based circuits offer significant advantages for printed circuits.

Tunnel diodes are electronic devices which exhibit negative differential resistance (NDR) in their I-V characteristic. This phenomenon is caused by quantum mechanical tunneling. Yoon *et al.* [7] demonstrated reproducible, room temperature NDR in organic diode devices, with interfacial ultra-thin TiO_2 layers. These organic tunnel diodes were, however, fabricated on rigid substrates with methods unsuitable for high-throughput fabrication on flexible substrates. Fabrication of the integral interfacial oxide layer is the specific issue. Since then, effort has been made to fabricate these devices with high-throughput suitable methods. Wolff *et al.* [8] and Heljo *et al.* [9] studied the suitability of anodic oxidation of thin titanium layers as the fabrication method. The method proved promising and NDR behavior was observed for fabricated devices [9]. However,

the precise operational principle of the devices remains unknown and various issues remains to be solved before these devices can be incorporated to printed circuits.

The objective of this work was to fabricate organic tunnel diode devices using two different fabrication methods for the interfacial oxide layers: anodic oxidation and atomic layer deposition (ALD). The effect of the oxide layer thickness on the device behavior was investigated. The fabricated oxide layer properties and the overall device characteristics were also studied. Section 2 reviews the theoretical background for organic semiconductors and tunnel diodes. Sections 3 and 4 cover the methods used for the interfacial oxide fabrication. The theoretical background of the oxide property characterization methods are explained in Section 5. Section 6 describes the execution of the experimental work with the obtained results and conclusions are presented in Section 7.

2. BACKGROUND FOR ORGANIC TUNNEL DIODES

This section covers the theoretical background for the organic tunnel diodes studied in this work. The subjects of organic semiconductors, Schottky diodes and tunnel diodes will be briefly introduced.

2.1 Organic semiconductors

Organic semiconductors (OSC) and conductors form the basis for organic and printed electronics. Both organic small molecules and polymeric materials can exhibit semiconducting or conducting properties. Although these materials can differ significantly in chemical structure and especially in molecule size, they share a structural feature that gives rise to their electric properties: *conjugation* of the alternating single and double bonds of their organic carbon backbone [10, p.14][11, pp. 369–370]. Examples of conducting organic compounds are presented in Figure 2.1 [12, pp. 6–8].

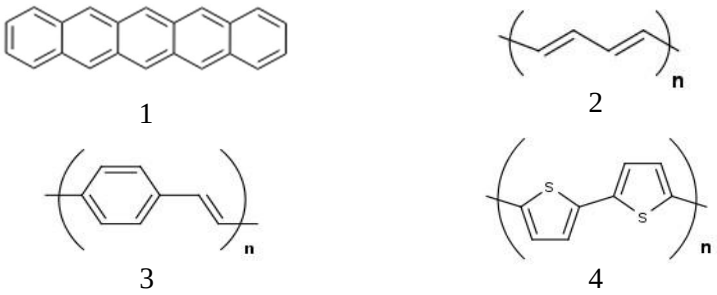

Figure 2.1 *Examples of conducting organic compounds. 1: pentacene, 2: polyacetylene, 3: polyphenylene vinylene (PPV), 4: polytiophene.*

Semiconducting organic compounds typically differ by the number of benzene rings (or other repeating conjugated units) fused together in their structures, different sidechains and the substitution of foreign atoms, e.g. nitrogen and sulphur, into the carbon chain. Polymers with a conjugated carbon chain are often called *conducting polymers*. The following discussion will be limited to conducting polymers. [12, p. 371]

2.1.1 The chemical structure of organic semiconductors

Conducting polymers have a carbon chain structure where the atoms are sp^2-hybridized and joined together with alternating single and double bonds, i.e. conjugated. Carbon

atoms with their 6 electrons have a full 1s atomic orbital and four valence electrons distributed between 2s, $2p_x$, $2p_y$ and $2p_z$ atomic orbitals. In sp^2-hybridization, three of these electrons lie at the three half-filled sp^2 hybrid orbitals of equal energy, which are formed by the hybridization of 2s, $2p_y$ and $2p_z$ atomic orbitals. One electron lies at a higher energy at the remaining $2p_x$ orbital, which is perpendicular to the plane of the hybrid orbitals [13, p. 101]. The three hybrid orbitals can overlap with three other orbitals in neighboring atoms to form three σ *molecular orbitals*, i.e. covalent bonds, in a trigonal planar formation [14, pp. 452–453]. In addition, the p orbitals in adjacent sp^2-hybridized carbons overlap to form a π bond. The σ and π molecular orbitals can be either bonding (σ, π) or anti-bonding (σ^*, π^*) depending on whether the p atomic orbitals overlap in-phase or out-of-phase, respectively [13, p. 142]. Formation of the molecular orbitals and their energy levels are depicted in Figure 2.2 for ethylene. Since electrons occupy orbitals with the lowest possible energy levels, the concept of *the highest occupied molecular orbital* (HOMO) and *the lowest unoccupied molecular orbital* (LUMO) arises. The HOMO and LUMO levels are indicated in Figure 2.2 b) for ethylene.

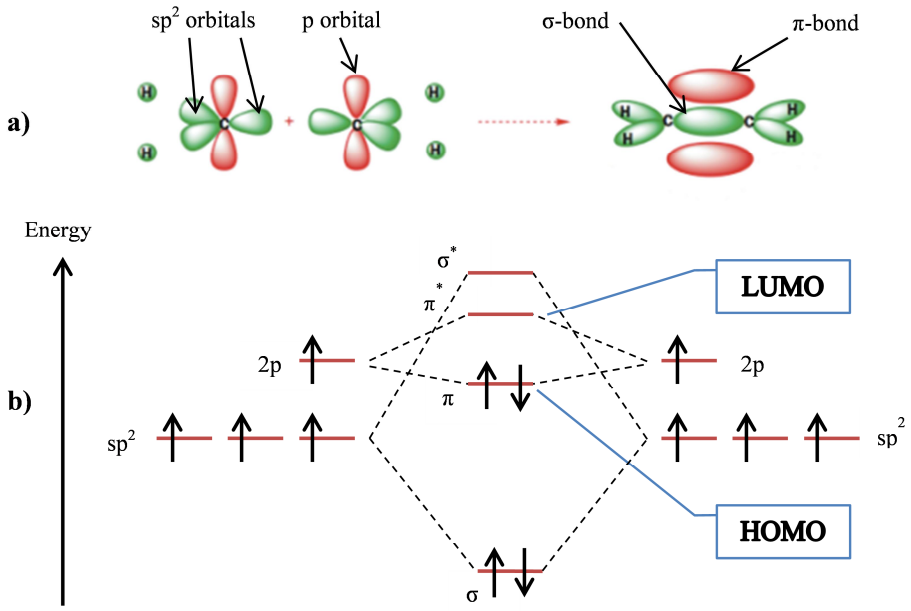

Figure 2.2 *a) Depiction of the orbitals in sp^2 hybridized carbon atoms and molecular orbitals in ethylene. Overlap of the sp^2 hybrid orbitals forms an σ bond between the carbons. A π bond is formed from the overlap of the p orbitals. b) Energy levels of the orbitals in the sp^2 hybridized carbon atoms and molecular orbitals between the carbons in ethylene. π^* and σ^* are anti-bonding orbitals, the arrows indicate electrons and their spins. Adapted from [13, p. 101]*

As can be seen in Figure 2.2(b), combining two p atomic orbitals creates two molecular orbitals (π and π^*) with different energies. Increasing the amount of sp^2 hybridized carbons in the carbon chain increases the amount of p orbitals that will overlap. This leads

to the creation of an equal amount of new π orbitals, which is depicted in Figure 2.3 [15, p. 296], where the energy levels are based on the *Hückel model*. Increasing the length of the carbon chain, hence, creates more available molecular orbital energy levels and decreases the energy difference between them. With an infinitely long chain the discrete energy levels become effectively a continuous energy band with no band gap.

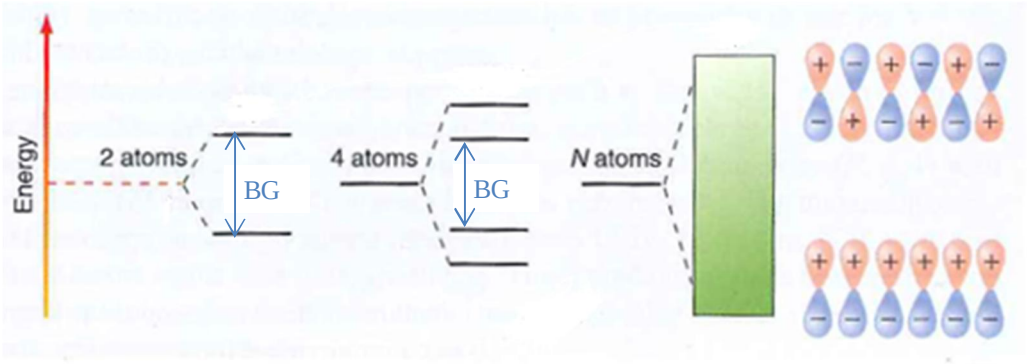

Figure 2.3 *Molecular orbitals generated with the Hückel model. When the length of the conjugated carbon chain increases towards infinity, the energy spectrum becomes continuous. On the far right: the atomic orbitals can combine in different phases (i.e. the wavefunction depicting said orbital is either positive or negative), resulting in different possible energy levels for the molecular orbitals. BG = band gap.*

According to the Hückel model the π electrons in the sp^2 hybridized carbon backbone form a continuous π molecular orbital due to the overlapping of the p orbitals in each consecutive carbon atom [15, pp. 289–290]. The π electrons of the carbon chain are said to be *delocalized* and not bound to any specific atom. With complete delocalization of the π electrons, the carbon atoms would be bonded with equal bond lengths and each carbon would have an unpaired electron. A material like this could be described as a quasi-one-dimensional metal according to solid-state physics and could exhibit metallic conductivity, because of half-filled orbitals [16, p. 34]. However, in reality, e.g. for polyacetylene (depicted in Fig. 2.1), a phenomenon called the *Peierls instability* prevents the complete delocalization of the π electrons. As a result, the valence electrons fill the orbitals that form the *valence band* (VB), which is separated from the higher-energy empty orbitals of the *conduction band* (CB) by a forbidden zone, the so called *band gap* [16, p. 34–35]. The Peierls instability happens in polyacetylene, because of its degenerate ground state, i.e. there are two possible and energetically equal ways to construct the carbon chain with alternating single and double bonds. These *resonance structures* are energetically more favorable than the structure with equal bond lengths. The Peierls distortions affect polyaromatic molecules (e.g. PPV in Fig. 2.1) as well, causing unequal resonance structures: an aromatic structure and a quinoid structure [16, pp. 36–37]. Due to the Peierls instability, conjugated polymers have a similar band gap between the VB and CB as inorganic semiconductors and insulators. Hence, conjugated polymers are either semiconductors or insulators in their undoped state [17, p. 513].

Conjugated polymer macromolecules generally consist of hundreds of monomer units [16, pp. 1–2]. A conjugated carbon chain leads to a reasonably stiff polymer molecule, because the carbon atoms linked with double bonds cannot rotate around each other. Due to the chain stiffness, conjugated polymers are in general less soluble and tractable as conventional polymers, e.g. polyethylene. In addition, they can also be non-fusible, i.e. they decompose before they melt. This is problematic, because easy solution or melt processing is generally an advantage of polymers. However, the processability problems have been mostly addressed by synthesizing new conjugated polymers, which are usually some derivations of the simple conjugated polymers, like the ones shown in Figure 2.1. Substitution of different side chains into to the polymers is often utilized. As an example PPV is insoluble in organic solvents, but its derivative MEH-PPV, poly[2-methoxy-5-(2'-ethylhexyloxy)-p-phenylene vinylene], can be used in solution processes [11, p. 371]. In general, the vast arsenal of organic synthesis techniques and methods can be applied for conjugated polymers as well, which allows the synthesis of OSCs with properties designed for specific applications [10, p. 123].

The synthesis methods and particularly the side chains affect many other essential properties of conjugated polymers. The band gap of OSCs gives rise to their color. When the band gap energy is similar to the energy of visible light, the material can have specific colors. The band gap can be tailored with synthetic methods [18]. Typically increasing the length of the side chains in conjugated polymers leads to a more flexible and tougher material [19], which is important in the field of stretchable electronics [20]. In general, what makes these materials attractive for many diverse applications is the thought of combining the electric and optical properties of semiconductors with the processability and mechanical properties of conventional polymers.

2.1.2 Charge transport in organic semiconductors

Conjugated polymers can be used as semiconductors in their *undoped* state. In addition, their electric conductivity can be enhanced with a *doping process*, analogously with inorganic semiconductors. Their doping processes are, however, quite different. Inorganic semiconductors are doped by introducing certain impurity atoms into the crystal lattice of the material. In contrast, conjugated polymers are typically doped with an oxidation process, where the polymer chains become charged. The doping can be accomplished with electrochemical oxidation and chemical oxidation (i.e. with the use of oxidants) processes. Counter ions will transfer from the reaction medium (e.g. electrolyte) into the polymer matrix to maintain electro neutrality. [17, pp. 526–528]

The charge transport and doping in conjugated polymers is typically explained with the *Bipolaron model* [21, p. 4736]. According to this model, charging of the polymer chains will create radical cations that are accompanied by lattice distortions. A radical cation along with its lattice distortions is called a *polaron*. A polaron will turn into a dication called *bipolaron* with further oxidation. These quasiparticles act as the charge carriers in

the polymer. The formation of polarons and bipolarons by oxidation of chains is depicted for PPP in Figure 2.4. In place of oxidative doping, electron injection between a conducting polymer and an electrode causes similar charging of the polymer chains.

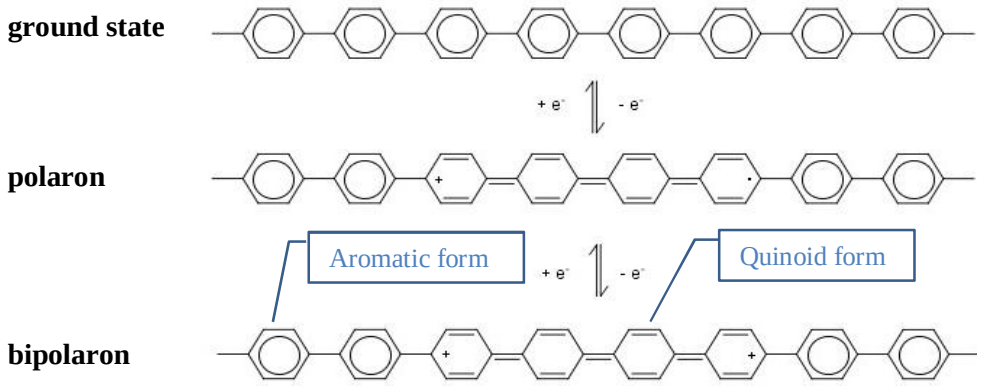

Figure 2.4 *Formation of the polaron and bipolaron states in poly(p-phenylene)(PPP). In polyaromatic molecules, the radical cations and dications change the structure into a quinoid form. Adapted from [17, p. 527].*

The polarons and bipolarons are quite localized in the polymer chains. Conducting polymers are typically classified as disordered semiconductors, due to the presence of much energetic disorder [22]. The disorder originates e.g. from their amorphous or semicrystalline structure, sp^3 defects in the chain and chemical impurities. The disorder is a hindrance for the delocalization of the charge carriers. In contrast, the periodic long-range order in inorganic crystalline semiconductors leads to efficient delocalization of charge carriers [23].

For OSC, the charge transport along the polymer chains and also between the different molecules needs to be distinguished. When the polymer chains are long and contain little defects, the conductivity along the chains can be very high. The rate determining step is usually the interchain conductivity. Because of the localization of the charge carriers, the conductivity is typically thought to occur by phonon-assisted *hopping* and *tunneling* processes [10, p. 182]. The hopping mechanism is dominant at room temperature [24]. The conductivity increases with temperature, because of the thermal activation of the hopping process. However, the temperature dependency is largely dependent on the doping level of the polymer: a polymer can show metallic conductivity (i.e. conductivity rises as temperature lowers) at high doping levels [17, pp. 533–534].

OSC are usually classified into n-type and p-type semiconductors, as are inorganic semiconductors. For OSC, this classification usually refers to the relative ability to carry charges (electrons or holes), because materials in standard OSC devices are generally intrinsic. N-type: electrons are the dominant charge carriers. P-type: holes are the dominant charge carriers. Doping by chemical or electrochemical oxidation leads to p-type

conductivity. A hole, in this case, means the positively charged polaron or bipolaron formed in the chain. [24]

2.2 Semiconductor-metal contacts

In many semiconductor devices, such as diodes and transistors, the interfaces between semiconductors and metal electrodes are of utmost importance. A *diode* is most often a two terminal semiconductor device that has a low resistance in one direction (*forward direction*) and a high resistance in the other direction (*reverse direction*). A p-n junction, i.e. a junction between p-type and n-type semiconductors, is typically used in inorganic semiconductor diodes. Diodes can also consist solely of one semiconductor along with a suitable metal electrode. These diodes are called *Schottky diodes* and their operation is based on the formation of a *Schottky barrier* at the semiconductor-metal interface. [25]

Before the examination of the semiconductor-metal junctions, a few terms will be defined. The *vacuum level* is defined as an energy level where an electron is free i.e. no longer bound to an atomic nucleus and has zero kinetic energy. The *Fermi level*, E_F, is the electrochemical potential of electrons in a given material and represents the potential of an electron to do electrical or nonmechanical work [25, p. 321]. The *work function*, φ, is the minimal energy required to liberate an electron from a metal (or a semiconductor), i.e. the difference between the vacuum level and the Fermi level [26, p. 68].

2.2.1 Schottky contact

When a metal and a semiconductor material have different Fermi levels, electrons within them have different electrochemical potentials. When these materials are brought together, the phases would not be in thermodynamic equilibrium. Therefore, upon contact, an immediate electron transfer across the interface will occur. This leads to equilibrium and a uniform electrochemical potential across the phases. The electron transfer occurs from higher electrochemical potential to the lower, i.e. from the material with the smaller work function to the one with the larger. This process is analogous to bringing a hot and a cold object together, where a net heat is transferred from the higher temperature object to the lower. [25, p. 321]

The semiconductor-metal contacts will be considered only for a p-type semiconductor, because organic semiconductors are typically hole-transporting materials. Depending on the work functions of the materials, two types of contacts are possible: a *Schottky contact* or an *ohmic contact* [25, pp. 436–445]. A Schottky contact happens when the n-type semiconductor has a larger work function than the metal. The Fermi level of a semiconductor lies between its VB and CB. For a p-type semiconductor, it lies at a level little higher than the VB. To equilibrate the two phases, electron transfer occurs from the metal into the semiconductor until the Fermi level of the metal, φ_m, and the Fermi

level of the semiconductor, φ_s, are equal, i.e. no electrochemical potential gradient exists. Since the transferred particles are charged, the metal gains a positive charge and the semiconductor a negative charge. A *depletion region* forms in the p-type semiconductor, where ionized acceptors are left uncompensated by the holes. [25, 26]

The depletion region results in a built-in field and a build-in potential, i.e. contact potential. In addition, *band bending* happens at the metal-semiconductor interface. The band bending and the depletion region are illustrated in Figure 2.5. A *Schottky barrier* is formed at the interface due to the band bending and acts as an energy barrier for the transport of holes from the semiconductor to the interface [26, p. 70].

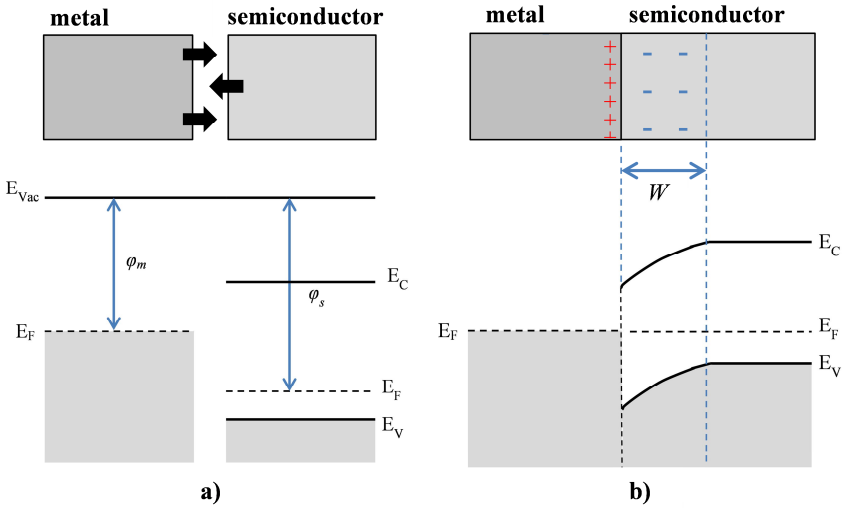

Figure 2.5 *Schottky barrier formation due to band bending in a p-type semiconductor-metal junction. a) Metal and semiconductor not yet in contact. b) Upon contact, the Fermi levels align and a depletion region arises in the semiconductor. The depletion region causes band bending and the formation of the Schottky barrier at the interface.* E_C *= conduction band edge energy,* E_F *= Fermi level energy,* E_V *= valence band edge energy,* E_{Vac} *= vacuum level,* W *= depletion region width,* φ_m *= metal work function,* φ_s *= semiconductor work function.*

Under open circuit conditions, no net current flows through the junction and the *Schottky barrier height* is governed by the difference in the work functions [25, p. 437]. The depletion region width and the barrier height can be controlled with the applied voltage. The applied voltage changes the electrochemical potential of the electrons in a material and hence the Fermi level. For a Schottky junction, a *forward bias voltage* is an externally applied voltage that lowers the potential barrier at the junction and promotes carrier transport. Under forward bias, the metal side is hence connected to the negative terminal and the semiconductor to the positive, i.e. oppositely to the build-in voltage. A *reverse bias voltage* has the opposite effect: it makes the potential barrier higher at the junction. Hence, under reverse bias, the holes require more energy to get from the semiconductor to the interface. [25, pp. 437–440][26, pp. 71–72]

2.2.2 Ohmic contact

Another type of a metal-semiconductor junction is an *ohmic contact*. An ohmic contact does not limit the current flow across the junction [27, p. 241]. Ohmic contacts are formed between metals and p-type semiconductors when the metal has a greater work function than the semiconductor. The Fermi levels of the two materials align by an electron transfer, which happens now to the opposite direction compared to a Schottky contact. An *accumulation region* of major carriers, i.e. holes, will form in the semiconductor side, which becomes positively charged. Formation of an ohmic contact is depicted in Figure 2.6.

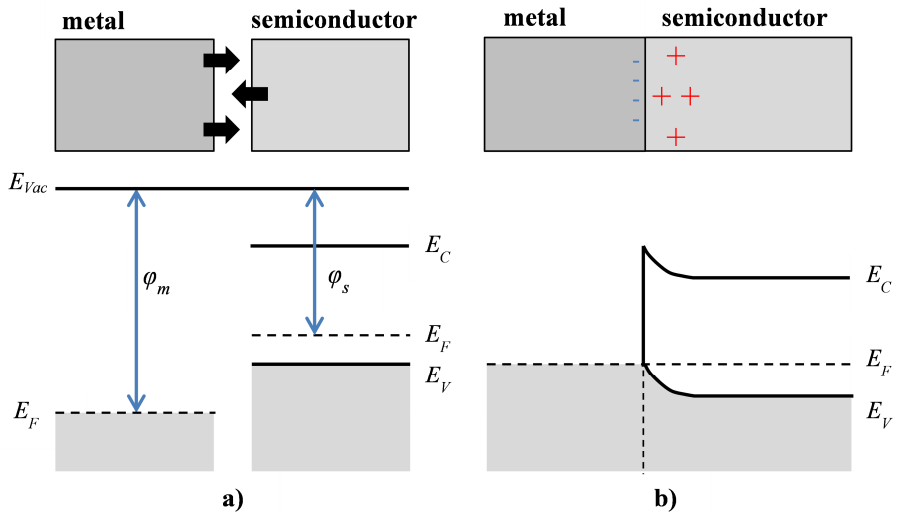

Figure 2.6 *An ohmic contact between a metal and a p-type semiconductor. An accumulation region of holes forms in the semiconductor.*

The description of the two contacts above where for inorganic semiconductors. The contact formation works similarly for organic semiconductors, but is more difficult to depict. For a p-type organic semiconductor, the Fermi level lies close to the HOMO level. This means that, to achieve a Schottky contact the work function of the metal should be significantly smaller than the HOMO energy level. For an ohmic contact, the work function should be a little greater than the HOMO energy level.

2.2.3 Schottky diodes

Schottky diodes are two terminal devices, where a semiconductor is connected to two electrodes. One electrode junction is a Schottky contact and the other an ohmic contact. Under reverse bias, only a small current, i.e. *leakage current*, is observed. In the forward direction, the current increases exponentially as the voltage increases. Schottky diodes show *rectifying* behavior. [25, pp. 435–440]

It is sometimes more appropriate to consider organic diodes as metal-insulator-metal devices, because of the low charge carrier density and low charge mobility of undoped OSC materials. The depletion layer that forms in an organic semiconductor-metal interface can be thicker than the device itself and, hence, the semiconductor is fully depleted [28, pp. 1–11]. Under voltage bias, charge injection from an electrode creates charge carriers in the OSC layer as described in Section 2.1.2. However, the I-V characteristics of organic diodes are, in general, similar to conventional metal-semiconductor diodes.

Organic Schottky diodes are typically fabricated as vertical structures, because it is easier to fabricate thin film semiconductor layers vertically. Suitable methods for the fabrication of thin film OSC layers are for example printing methods (gravure printing etc.) and spin coating. The metallic electrodes can be fabricated for example by evaporation, but also by printing using special conductive metal inks. [6]

2.3 Tunnel diodes

Besides the Schottky diode, another diode type of interest in this work is the *tunnel diode*. The traditional tunnel diodes are inorganic pn-junction diodes often referred to as *Esaki diodes*. A depletion region forms in a pn-junction, much like in a Schottky junction. In an Esaki diode, the p- and n-type semiconductors are highly doped, which makes the depletion region very narrow due to the high major carrier concentration. In this situation, filled and empty electron states are separated by a narrow potential barrier (i.e. the depletion region) at the junction. Hence, the conditions are eligible for *quantum-mechanical tunneling* phenomenon, where electrons can tunnel through the potential barrier even though their energy is less than the potential energy barrier [29, p. 42–43]. This *tunneling* process causes a peculiar IV-characteristic: a region of *negative differential resistance* (NDR). [29, pp. 486–487]

2.3.1 Quantum mechanical tunneling

According to quantum mechanics, particles (such as electrons) have wave characteristics. The *wavefunction*, Ψ, of an electron indicates the *probability* of finding the electron at certain region of space, which cannot be known precisely as explained by the uncertainty principle [14, pp. 279–282]. The *Schrödinger equation* is a fundamental equation at the heart of quantum mechanics and describes the probability distribution and energy of an electron in a system with certain boundary conditions [25, pp. 208–210].

An electron contained in a one-dimensional potential well with infinite potential barriers is a system called *the particle-in-a-box*. Infinite potential energy at the barriers means that the electron has no chance of escaping the well. The wavefunction of the electron is zero at the barriers. Solution of the Schrödinger's equation (with boundary conditions) reveals the acceptable wavefunctions and energies of the electron in the well [14, p.

292]. Each wavefunction corresponds to a specific energy and these are quantized, i.e. the electron can only occupy certain discrete energy levels [25, p. 214].

However, if a potential barrier in the potential well has a finite energy, E_0, the situation is different. The wavefunction of the electron is not zero at a finite potential barrier, which indicates a possibility of the electron to occupy spaces outside the well [14, p. 296–297]. The wavefunction *decays exponentially* with distance x inside the barrier that has a width of a. This is depicted in Figure 2.7. With these definitions, the wavefunction inside the barrier, Ψ, is

$$\Psi(x) = A_1 e^{\kappa x} + A_2 e^{-\kappa x} \quad , \tag{2.1}$$

where A_1 and A_2 are constants from a solution of the Schrödinger's equation [25, p. 222]. The first term in the equation is an exponentially rising function and the second term an exponentially decaying function.

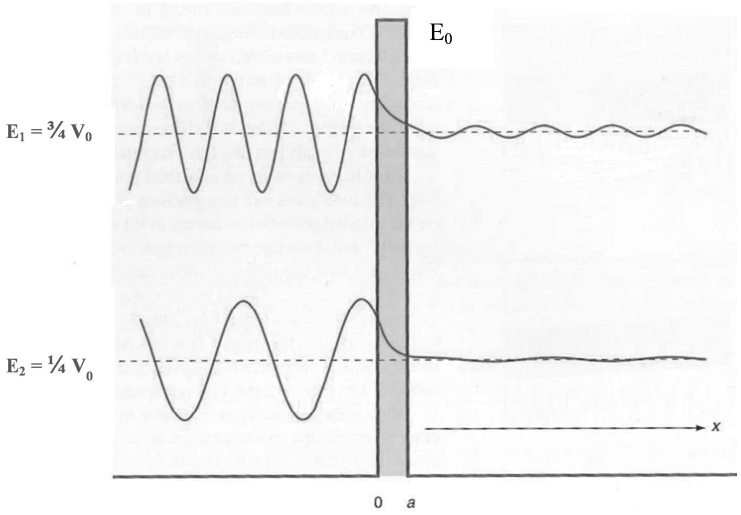

Figure 2.7 *Two incident wavefunctions of an electron corresponding to two different energies, E_1 and E_2, which are lower than the energy of the potential barrier, V_0. The wavefunction amplitude decays inside the barrier, but is not zero after the barrier. When the barrier is narrow enough, a non-negligible wavefunction exists at the other side of the barrier, i.e. the electron has a probability to exist at the other side of the barrier. The probability is greater when the electron has higher energy, i.e. when $E = E_1$. Adapted from [15, p. 68]*

The reciprocal of κ is called the *decay length* and is given by

$$\frac{1}{\kappa} = \sqrt{\frac{\hbar^2}{2m(V_0 - E_n)}} \quad , \tag{2.2}$$

where $\hbar$ is the reduced Planck constant. m and E_n are the mass and the energy of the particle, respectively [15, p. 68]. When the decay length is larger, the wavefunction of

the electron decays slower inside the barrier. This happens when the electron is at a higher energy state as can been seen from Figure 2.7. Similar results are obtained when the energy of the potential barrier is lower as can be deduced from Equation 2.2.

It can be seen from Figure 2.7, that a particle has different wavefunctions at the different sides of the barrier, i.e. the incident and the transmitted waves. This also means that the electron has a probability to exist at both sides of the barrier, even though the electron doesn't have the required energy to cross the barrier in the classical sense [14, p. 298]. This quantum mechanical phenomenon is called *tunneling* and is a real world phenomenon. The relative probability for the electron to tunnel through the barrier is called the transmission coefficent, T_t, and can be [25, pp. 222–223] expressed for a wide barrier as

$$T_t = T_0 e^{-2\kappa a} \quad , \tag{2.3}$$

where

$$T_0 = \frac{16E_n(V_0 - E_n)}{V_0^2} \quad . \tag{2.4}$$

According to Equations 2.3 and 2.4, the probability for tunneling through the barrier increases as the potential barrier becomes narrower (i.e. a becomes smaller) and lower in energy. Tunneling is a significant phenomenon only over very small distances. If the barrier is wider, the effect of tunneling becomes negligible [29, p.43]. Tunneling proceeds with constant energy [15, p. 69], which is shown in Figure 2.7 by the dashed line. This means that tunneling requires filled and empty electron energy states (at the same energy) at the different sides of the barrier.

2.3.2 Negative differential resistance

In an Esaki diode, application of a small voltage bias causes band bending and brings filled and empty energy states to the same level at different sides of the barrier. A tunneling current will flow across the barrier. Magnitude of the current depends on the applied voltage. A typical IV-characteristic of an Esaki diode is shown in Figure 2.8 [29, p. 490]. The plot features a current peak at low voltage and a valley at higher voltage. Certain values can be defined from the plot: *peak tunneling current*, I_p, peak voltage, V_p, and *valley current*, I_v.

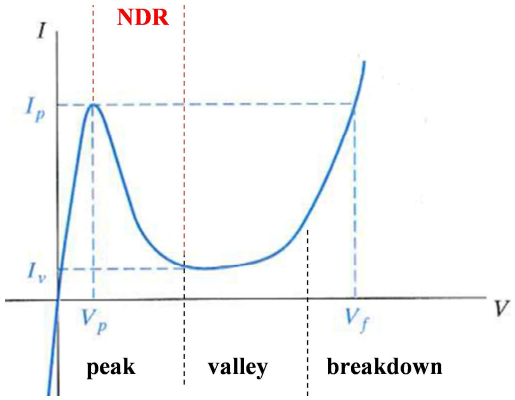

Figure 2.8 *Typical IV-characteristic of a tunnel diode. Negative differential resistance (NDR) is observed between the peak and the valley.*

As can be seen from Figure 2.8, the tunneling current begins to fall when the voltage exceeds the V_p. When the voltage exceeds this limit, the number of aligned empty and filled energy states across the barrier begins to decrease. This causes a region of *negative differential resistance* (NDR), where an increase in voltage causes a decrease in current. When the voltage has increased enough, current due to tunneling becomes negligible and a *valley region* has been reached. In the valley region, there is a small leakage current and the device behaves like a conventional diode. When the voltage is further increased some different charge transport process begins to dominate the tunneling transport and the current increases again. [29, p. 489]

A numerical value referred to as the *peak-to-valley current ratio* (PVCR) is often used for tunnel diodes to describe the magnitude of the NDR. PVCR is defined as the ratio of the peak current density, J_p, and the valley current density, J_v, and can be [7] expressed as

$$PVCR = \frac{J_p}{J_v} \quad . \tag{2.5}$$

It has to be mentioned, that NDR is not a phenomenon unique to just tunnel diodes. Also, tunneling is not the only possible cause for NDR behavior. For example, the Gunn diode also exhibits NDR, but not due to tunneling. [29, p. 486]

2.3.3 Organic tunnel diode

The Esaki diode is an inorganic semiconductor device. These tunnel diodes have found some use in high-speed electric circuits and at high frequency operations. However, they have not achieved widespread application [29, p. 490].

In 2005, Yoon *et. al.* [7] presented a novel *organic tunnel diode* that showed reproducible NDR at room temperature (RT). These diodes consisted of an *indium-tin-oxide* (ITO) electrode, an *ultra-thin TiO_2 barrier film*, OSC thin film and an aluminum top

electrode. The OSC used in these diodes was MEH-PPV that has the chemical structure shown in Figure 2.9(a) [7]. The diodes were fabricated as a vertical structure illustrated in Figure 2.9(c). The TiO_2 ultra-thin films were fabricated with a two-step process: first, an evaporation of titanium layers, with varying thicknesses (2-20 nm) onto the ITO coated glass substrates. Secondly, the oxidation of the titanium layers using an inductively coupled plasma reactive ion etching (ICP-RIE), with oxygen plasma and the substrate at room temperature. The MEH-PPV layers (nominally 25 nm thick) were spin coated and the aluminum top electrode (250 nm thick) was evaporated through a shadow mask. The flat band energy level diagram for the device is presented in Figure 2.9(b). These diodes are typical Schottky diodes except for the interfacial oxide layer.

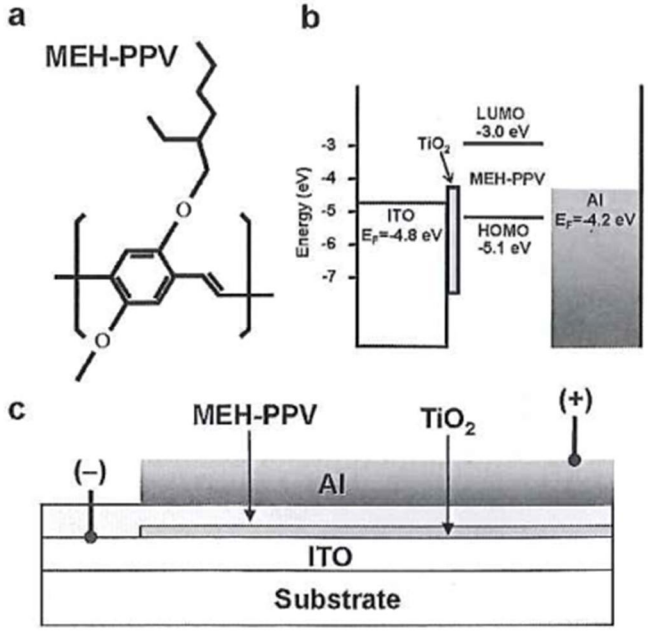

Figure 2.9 *The device structure and materials for the organic tunnel diodes presented by Yoon et. al. [7]. a) The structure of the OSC MEH-PPV. b) The flat band energy level diagram for the organic tunnel diode. c) The vertical structure of the organic tunnel diode and the electric contacts for the ITO and aluminum electrodes.*

The NDR occurred in these devices under reverse voltage bias, with a PVCR as high as 53. The largest NDR was obtained in devices with 4 nm thick TiO_2 layers. When the TiO_2 layer thickness was decreased to 2 nm, the observed NDR was significantly weaker and the J_p smaller. This should not be the case, if the TiO_2 is considered as a traditional tunneling barrier. With a traditional tunneling barrier, as described in Section 2.3.1, the tunneling peak current should diminish as the barrier width increases. Yoon *et al.* [2.20] suggested that the NDR occurs by tunneling through localized defect sites in the TiO_2. It was speculated that the NDR under reverse bias occurred via the tunneling of the electrons, which were injected from the ITO (n-type semiconductor), through the

defect sites of the TiO_2 to the LUMO level of the MEH-PPV. Devices that were otherwise similar but lacked the TiO_2 interfacial layer didn't show NDR behavior. [7]

The significance of these NDR devices was also demonstrated by Yoon *et al.* [7]. Combining two tunnel diodes in series with one transistor formed a memory cell. Organic tunnel diodes offer the possibility of novel logic circuits for organic electronics. These circuits based on tunnel diodes would require fewer devices and lower power consumption than conventional logic circuits. In printed electronics, fewer devices would be a great advantage due to less complex circuitry. The requirements for the tunnel diodes in these logic circuit applications would be a reliable NDR operation at room temperature with a reasonably high PVCR (> 3) [7]. Organic tunnel diode based circuitry has potential applications as memory elements in large-area electronics i.e. in printed electronics. However, these devices would have to be suitable for high-throughput fabrication, which is one of the main advantages of large-area electronics and printed electronics.

2.3.4 High-throughput fabrication of organic tunnel diodes

The work done for this thesis is part of a larger project, where the main objective is to fabricate these organic tunnel diodes on *flexible substrates* with *high-throughput fabrication* methods. Development and research of a high-throughput suitable fabrication method is one of the primary focus points of the project. Flexible ITO coated polymer substrates are widely available. The whole fabrication process needs to be suitable for low temperature processing due to the polymer materials. Deposition of the metallic top-electrode and the OSC layer are possible with roll-to roll (R2R) suitable methods e.g. printing methods at low temperatures and high-throughputs. The main problem is the deposition of the interfacial oxide layer. At the moment, two fabrication methods are looked into in this project: *anodic oxidation* and *atomic layer deposition* (ALD). Currently, these devices have been studied only on rigid glass/ITO substrates. Only rigid substrates will be used in this work as well.

Previous work on this project includes the work done by Wolff *et al.* [8] and Heljo *et al.* [9]. Wolff *et al.* [8] studied the anodic oxidation of ultra-thin titanium films on ITO substrates. The anodic oxidation is one of the researched deposition methods for the interfacial TiO_2 films. Heljo *et al.* [9] continued the previously mentioned work by studying the anodic oxidation further and fabricating organic tunnel diodes based on it. These diodes were quite similar to the ones mentioned in Section 2.3.3. These devices had a vertical structure of ITO/TiO_2/OSC/Al. The TiO_2 film was anodized and 4.4 nm thick. The observed room temperature NDR had a PVCR of 3.6, significantly lower than in the devices studied by Yoon *et al.* [7]. However, the operational principle of these devices still remained unknown. The anodic oxidation showed promise as a fabrication method for the interfacial layers. In this thesis, the anodic oxidation process will be used to fabricate different TiO_2 layer thicknesses. NDR devices will be fabricated similarly to

the previously mentioned work and the effect of the interfacial oxide thickness on the current-voltage behavior will be studied.

Atomic layer deposition has become a very interesting method for the deposition of high quality thin films, *e.g.* for the deposition of metal oxides [30]. In addition to anodic oxidation, ALD will be utilized to fabricate the TiO_2 films for the studied devices.

3. ELECTROCHEMICAL ANODIC OXIDATION

This section covers electrochemical anodic oxidation, which is one of the two methods used in this work to fabricate ultra-thin TiO_2. The basics of the method will be introduced along with some previously done work on anodic oxidation of titanium.

3.1 The basics of anodic oxidation

The electrochemical anodic oxidation, also called *anodization*, is an electrochemical method, which allows controlled formation of oxide layers on metal surfaces. Anodic oxidation can be used to control the thickness of the oxide layer on titanium surfaces [31]. In addition, anodization has suitability for high throughput fabrication of TiO_2 layers.

Anodizations are carried out in an electrochemical cell, where a non-spontaneous oxidation reaction is driven by an external power source, i.e. in an electrolytic cell. Basically, an electrolytic cell consists of at least two metal electrodes (connected by an external circuit) immersed in an electrolyte, which is usually an ionic solution [32, p. 25]. During anodic oxidation a sufficiently high voltage is maintained between the electrodes to initiate the desired electrochemical reactions. The oxidation reaction happens at the positive *anode* electrode and reduction at the negative cathode electrode. The oxidation of a metal electrode (M) leads to the formation of metal cations (M^{z+}) by the following general reaction [33, p. 2908]:

$$M \rightarrow M^{z+} + z\,e^{-}\,. \tag{3.1}$$

In general, the oxidation of a metal anode leads to three possible outcomes [33, p. 2908]: 1) the formed metal cations (M^{z+}) dissolve into the electrolyte (the metal anode dissolves); 2) the cations react with O^{2-}(a species in the aqueous electrolyte) to form a *compact oxide layer*; 3) a porous oxide layer can form, if there is a competition between the dissolution and the oxide formation. The outcome depends on the electrolyte, the metal anode and the anodization parameters (such as voltage).

According to *the classical anodization scheme* [33, p. 2909] the metal cations formed at the anode (Eq. 3.1) react with O^{2-} to form the compact oxide layer ($MO_{z/2}$) at the anode-electrolyte interface. The O^{2-} ions are created in the aqueous electrolyte by *electric field-aided deprotonation* of H_2O or OH^- ions. The overall reactions for the oxide ($MO_{z/2}$) formation are:

$$M + \frac{z}{2} H_2O \rightarrow MO_{z/2} + z\,H^+ + z\,e^- \quad , \tag{3.2}$$

$$M^{z+} + z\,H_2O \rightarrow M(OH)_z + z\,H^+ \quad , \tag{3.3}$$

$$M(OH)_z \rightarrow MO_{z/2} + \frac{z}{2} H_2O \quad . \tag{3.4}$$

The counter reaction, which is typically the reduction of protons (H^+), proceeds at the cathode electrode. The reduction leads to the formation of gaseous hydrogen (H_2) according to the following reaction:

$$z\,H^+ + z\,e^- \rightarrow \frac{z}{2} H_2\,(g) \quad . \tag{3.5}$$

The formation of the compact oxide layer separates the electrolyte and metal (anode) phases. The metal cations and/or the O^{2-} anions need to move through the grown oxide layer to be able to react with each other, as shown in Figure 3.1.

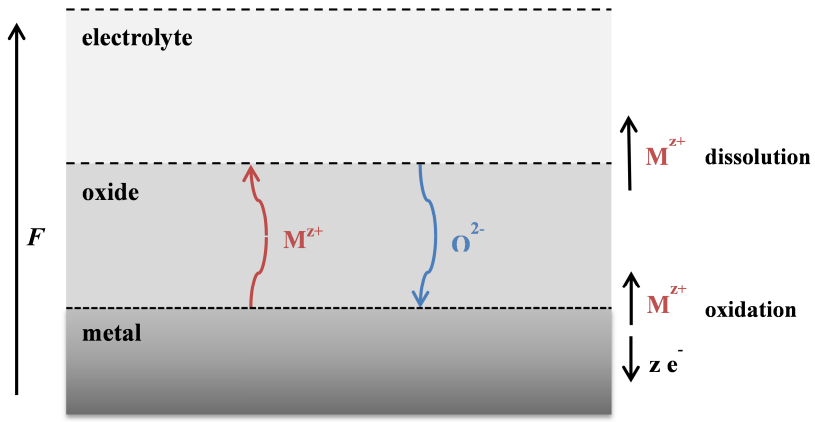

Figure 3.1 *Field-aided transport of the ions (M^{z+}, O^{2-}) at the anode during anodic oxidation. The metal cations are created by oxidation at the metal surface and O^{2-} ions by field-aided deprotonation of water in the electrolyte. Dissolution of the oxide is possible at the oxide-electrolyte interface. F = electric field.*

The transport of the ions (M^{z+}, O^{2-}) through the oxide is aided by the electric field (E) between the electrodes. The growth of the oxide can then occur at the electrolyte interface or the metal interface of the oxide depending on the migration rates of the ions. [33, p. 2909]

3.1.1 Potential and electrochemical cell

The electric potential, E, of the metallic anode affects the energy of the electrons in the metal. According to the band theory of solids, the electrons in the metal fill the energy levels up to the Fermi level [25, p. 295]. The Fermi level can be controlled with the applied potential. When the cathode electrode potential is made more negative, the Fermi

level can become high enough to reach the same level as an empty (atomic/molecular) orbital of a species present in the electrolyte. An electron flow from the cathode to the electroactive species (such as the H^+ -ions) is then possible, leading to a reduction reaction at the cathode. At the anode electrode, a more positive potential decreases the Fermi level of the metal enabling the oxidation of a suitable electroactive species. If there are no electroactive species in the electrolyte that can undergo oxidation, the anode itself can oxidize. The required potential for the oxidation of the anode depends on its standard reduction potential, E^o. [34, p. 15]

A working electrolytic cell requires two electrodes: a *working electrode* (WE) and a *counter electrode* (CE). The electrochemical reaction of interest proceeds at the WE. In the case of anodization of a metal, the WE is the anode electrode. A reduction reaction occurs at the CE to keep the electro neutrality of the electrolyte. To carry out the anodic oxidation process, the WE potential needs to be controlled accurately. However, the absolute potential of an electrode is not easily measured. Instead, the potential difference between two electrodes, referred to as cell voltage (V), can easily be measured experimentally. [34, pp. 16–17]

The measured cell voltage includes a potential term, the *ohmic drop*, in addition to the electrode potentials at each electrode. The ohmic drop arises from the intrinsic resistance of the electrolyte and is equal to the product of the cell current and the electrolyte resistance, R_{el}, between the electrodes [34, p. 17]. During the anodization process the WE potential can be controlled with the cell voltage, if the cell has a negligibly small ohmic drop and the CE potential is known and remains constant. Changes in the cell voltage are then equal to the changes in the WE potential [35, pp. 59–60]. The issues arising from the electrolyte resistance and the variable CE potential can be minimized by using a *three electrode cell* –experimental set-up.

A three electrode cell consists of a WE, a CE (also called auxiliary electrode, AE) and a *reference electrode* (RE). The reference electrode has a known potential relative to *the standard hydrogen potential* (SHE). The WE potential is measured against the RE potential. The potential of a RE remains nearly unaffected by the passage of current through it. The current passing through the RE is minimized, because of high impedance of the voltage measurement circuit. The major part of the cell current runs through the WE and the CE. The properties of the CE do not matter, since only the WE reactions are of interest. The ohmic drop due to the electrolyte resistance can be mostly compensated by placing the RE close to the WE. [34, pp. 17–20][35, pp. 25–27]

The WE potential can be easily controlled with the three electrode cell set-up, which enables the control of the anode reactions during the anodization process. The passage of an anodic current through the WE, at suitable WE potentials, leads to the formation of the oxide layer.

3.1.2 Faradaic and non-faradaic currents

The electrode reactions discussed above (oxidation, reduction) involve charge-transfer across the electrode-electrolyte interface. These types of reactions are called *faradaic processes*, since they obey *Faraday's law*. Faraday's law states that when current flows through an electrode, the amount of electricity (i.e. charge, *Q*) passed through is proportional to the amount of reaction product formed in the electrode reactions [35, p. 9]. It can be represented with the following equation [34, p. 14]:

$$Q = z\,F\,n \quad , \tag{3.6}$$

where *z* is the valency number of ion, *F* is the Faraday constant and *n* (mol) is the amount of reaction product formed in the electrode reaction caused by the flow of current. In *non-faradaic processes* no charge is transferred across the electrode-electrolyte interface, however, external currents can still flow. These currents, which do not obey Faraday's law, are called *non-faradaic currents*. Non-faradaic currents arise from phenomena such as adsorption, desorption and capacitive charging of the electrode-electrolyte interface. Faradaic processes at the WE are of the most interest during an anodization process. However, non-faradaic currents can be problematic from an analytical perspective. [35, pp. 9–10]

The electrode-electrolyte interface can charge similarly to a plate capacitor, because of the so called *electrical double layer*, i.e. the collection of all the charged species (ions) and oriented dipoles (solvent molecules) at the interface [35, p. 12]. The structure of the double layer consists of the charge at the metallic electrode, which is concentrated very close to the electrode surface, and several layers of the electrolyte with varying compositions [34, p. 45]. The structure is explained by the Stern model [36, 37].

3.2 Anodic oxidation of titanium

Titanium belongs to the group IV-B of the periodic table and behaves as a valve metal. Titanium is a very active metal and oxidizes spontaneously in the presence of oxygen or water to form a *passive oxide layer* [38, p. 1]. Several oxidation reactions [39] are possible for titanium and its cations. These are presented in the following equations with their respective *standard oxidation potentials*, $E^o{}_{ox}$:

$$\mathrm{Ti\,(s)} \rightarrow \mathrm{Ti^{2+} + 2\,e^-} \qquad E^o{}_{ox} = +1.628\,\mathrm{V} \quad , \tag{3.7}$$

$$\mathrm{Ti^{2+}} \rightarrow \mathrm{Ti^{3+} + e^-} \qquad E^o{}_{ox} = +0.369\,\mathrm{V} \quad , \tag{3.8}$$

$$\mathrm{Ti\,(s)} \rightarrow \mathrm{Ti^{3+} + 3\,e^-} \qquad E^o{}_{ox} = +1.209\,\mathrm{V} \quad , \tag{3.9}$$

$$\mathrm{Ti^{2+} + 2\,H_2O} \rightarrow \mathrm{TiO_2\,(s) + 4\,H^+ + 2\,e^-} \qquad E^o{}_{ox} = +0.502\,\mathrm{V} \quad . \tag{3.10}$$

The positive oxidation potentials for the oxidation reactions in Equations 3.7–3.10 indicate the tendency of titanium to undergo spontaneous oxidation. A compact oxide layer is formed on titanium surfaces, when exposed to air or water. This spontaneously formed oxide is often referred to as the *native oxide*.

At RT, oxygen can oxidize titanium to oxidation states +2, +3 and +4 creating different cations (Ti^{2+}, Ti^{3+} and Ti^{4+} respectively). Depth profiling experiments [40] have shown, that the inner native oxide layer (nearest to the metal-oxide interface) is made of Ti^{2+} species while the outermost oxide layer consists of Ti^{4+} and Ti^{3+} species. Therefore, the native oxide does not consist solely of TiO_2. Various *suboxides* (e.g. TiO) are possible. The compact native oxide layer formed from exposure to air has a thickness of 2–6 nm and is *amorphous* at RT [41].

Anodic oxidation of titanium has been studied extensively as a method to control or form TiO_2 layers [31, 33, 38, 41]. Usually the anodization has been carried out using titanium foils and high cell voltages to produce thick TiO_2 layers, with thicknesses of several tens of nanometers. The anodization has generally been accomplished with a constant voltage, i.e. by potentiostatic method. A method based on fluoride containing electrolytes has been used to fabricate porous TiO_2 layers and nanotubes [42, 43]

Anodic oxidation of titanium carried out in the absence of fluoride ions leads to the formation of a compact TiO_2 layer. The titanium dioxide formation can be presented with the classical anodization scheme shown in Equations 3.2–3.4, where in this case M = Ti and $z = 4$. The overall reaction for the oxide formation [38, p. 19] is

$$Ti + 2\,H_2O \rightarrow TiO_2 + 4\,H^+ + 4\,e^- \quad . \tag{3.11}$$

An anodized TiO_2 layer is generally obtained in an amorphous form. However, with long anodization times and high voltages the amorphous oxide can be converted to crystalline structures. [33, p. 2917]

Research papers [44, 46] involving the anodization of titanium have shown that the obtained titanium dioxide is an *n-type semiconductor*. The anodized TiO_2 layers behave like highly defective n-type semiconductors when amorphous, and like highly doped n-type semiconductors when annealed to a crystalline form. Amorphous TiO_2 has a band gap of 3.2–3.5 eV [46]. The CB edge is defined by the Ti 3d electron energy levels and the VB edge by the O 2p energy levels, which are the lowest empty energy levels and the highest occupied energy levels, respectively. [33, pp. 2918–2920]

The electrical properties of TiO_2 are heavily influenced by the presence and the amount of *structural defects* at the surface of the oxide or in the bulk. The most important defects in TiO_2 are the Ti^{3+} states and O^{2-} vacancies, which act as donors in the n-type semiconductor oxide layers. At low temperatures or low oxygen partial pressures the oxygen vacancies are considered to be the most relevant defects [47]. [33, p. 2917]

3.2.1 Anodic oxidation of titanium on indium-tin-oxide substrates

Although, the anodization of TiO_2 is usually carried out with thick titanium layers or foils, some applications require completely oxidized ultra-thin TiO_2 layers with no residual metallic titanium. For the organic tunnel diode discussed in Section 2.3.3, a few nanometers thin oxide layer needs to be fabricated directly onto a conductive ITO electrode. The anodic oxidation of valve metals on ITO substrates has been studied in some works [9, 48, 49]. Delamination of the oxide layers during anodization on ITO substrates has been a problem.

Wolff *et al.* [8] studied the anodic oxidation of ultra-thin titanium layers on conducting substrates, including ITO. *Galvanostatic* (constant current density) and *potentiodynamic* (linear potential ramp) anodization methods were studied. The anodization of thicker films (> 10 nm) on ITO seemed to differ substantially from the anodization of foils, with the process stopping early on. However, thinner titanium layers were successfully and completely oxidized. A layer breakdown was observed with voltages higher than 3 V.

Heljo *et al.* [9] studied the anodization of Ti on ITO substrates further. A potentiodynamic method proved to allow good control of the anodization process. Ultra-thin titanium layers (3 nm thick) were evaporated on ITO substrates and then completely oxidized by anodic oxidation. The layers consisted mainly of TiO_2, with large *defect densities*, N_{Def}, ($> 10^{19}$ cm^{-3}). However, oxide layer breakdown occurred with high enough voltages. The layer breakdown was proposed to happen via the growth of pores through the oxide and subsequent electrochemical reactions of the ITO with the electrolyte. The pore formation was thought to be caused by electric field enhanced dissolution of the oxide at higher voltages *i.e.* at higher field strengths.

3.2.2 The effect of process parameters

Heljo *et al.* [9] also studied the effect of the different anodization parameters on the properties of the anodized oxide. Dielectric constant and defect density were determined for the fabricated oxide layers with *Mott-Schottky analysis*. These properties didn't change significantly with respect to changes made in the electrolyte pH and sweep rate of the potentiodynamic process. The observed changes in the properties were within the reproducibility of the measurement. However, the layer breakdown voltage was observed to decrease significantly upon increasing the electrolyte temperature. This was proposed to occur due to the enhanced dissolution of the oxide at higher temperatures.

In this work, the same anodic oxidation method used in the previously mentioned work will be utilized. The aim is to fabricate different oxide thicknesses and study the effect on device behavior. Different oxide thicknesses can be reached by using different evap-

orated titanium layer thicknesses. Different anodization voltages are then required for the complete oxidation of the layers. However, the voltage should not exceed the break-down voltage.

4. INTRODUCTION TO ATOMIC LAYER DEPOSITION

This section serves as an introduction to atomic layer deposition, which is used in this work as a deposition method for the ultra-thin TiO_2 interfacial films.

4.1 Introduction

Atomic layer deposition (ALD) is a reasonably new and promising thin film deposition method for metal oxide semiconductors and insulators. Although, it has similarities with conventional *chemical vapor deposition* (CVD) techniques, there is a significant difference: In CVD, the reactants co-exist simultaneously in gas phase above the substrate and chemical reactions occur at the surface and in the gas phase. However, in ALD the substrate is exposed to the reactants sequentially and reactions occur only at the surface via *self-limiting reactions*. The self-limited nature of the deposition reaction allows excellent precision for the deposition process, effectively allowing deposition one atomic layer at a time. [30, p. 1]

After its invention in the 1970s, ALD has seen much research. Interest in ALD has been particularly high during the last two decades, mostly because of a need to produce ever thinner semiconductor and insulator layers in the semiconductor industry [50, p. 2960]. ALD is a suitable method to produce uniform and pin-hole free ultra-thin films with thicknesses in the region of tens of Å. ALD has traditionally been seen as a slow deposition process, which has been detrimental to industrial applications. However, developments in the ALD process and reactors have led to productivity increases. As an example, a roll-to-roll technique has been developed for ALD. [50, pp. 2992–2993]

4.2 Principle and chemistry of ALD

In ALD, the thin films are grown in a number of cycles. The resulting layer thickness is dependent on the amount of cycles used and the thickness deposited each cycle. Each cycle grows the film by 0.1 to several Å [30, p. 1] depending on the substrate, the reactants i.e. precursor gasses and processing conditions. A cycle typically consists of four steps, which are illustrated in Figure 4.1. The thin films are grown atop a substrate, which has a number of active surface sites such as hydroxyl-groups. In the first step, a precursor gas A reacts with the active sites at the substrate, until the surface is saturated. Secondly, any excess precursor A is removed from the substrate with a purge or evacuation step. Inert purge gasses e.g. nitrogen are used. Thirdly, a precursor B reacts with

the reaction product of precursor A at the substrate surface forming the first monolayer of the deposited compound. The last step is another purge phase, where the surface is made ready for another deposition cycle. [50, p. 2960]

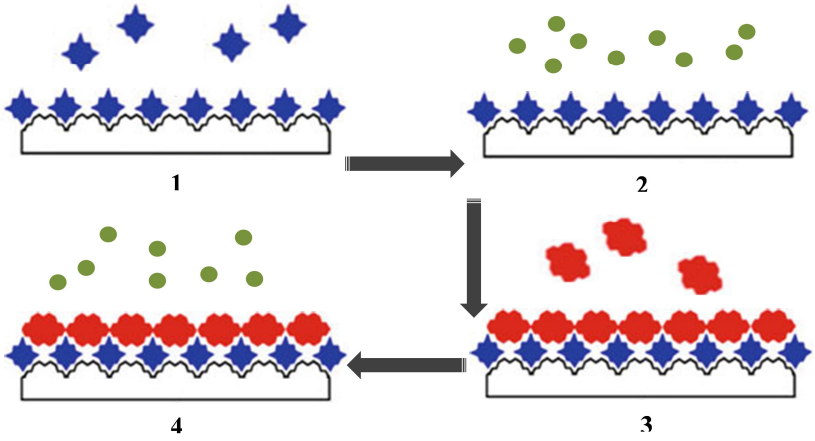

Figure 4.1 *One ALD deposition cycle consists of four steps: 1) saturation of the substrate surface with precursor gas A, 2) purge of excess precursor with purge gas, 3) self-limited reaction between precursors, 4) purge of excess precursor. Adapted from [50, p. 2961]*

Each cycle deposits the same amount of the desired substance. The cycle time is defined by the combined duration of the individual steps. The precursor gasses and purge gas are inserted as separate pressure pulses, which ensure that the precursors do not contact in the gas phase. The pulses for the precursors last just long enough to saturate the surface. The purging steps need to be long enough to remove all excess precursor gas. The cycle time for a given system (i.e. reactor, precursors, substrate, temperature, etc.) can be under one second or up to minutes [30, p. 5]. Because a large number of cycles are often required to reach the desired film thickness, the deposition rate of a typical ALD process is 100–300 nm per hour [51]. Slow deposition is the major disadvantage of ALD, but not crucial in applications were ultra-thin films are required.

Along with the gas pulse times and pressures, deposition temperature is a crucial parameter that needs to be controlled. The ALD reactions are thermally activated and also temperature-dependent. With a too low temperature, the reactants have insufficient energy to react and chemisorb with the surface active sites. In addition, the gaseous reactants could condense in the ALD reactor. If the temperature is too high, the precursors might decompose. In either case, the deposition rate declines and impurity content can increase. The optimal temperature range is between these and is typically wide in ALD compared to CVD, which is more temperature-dependent. The deposition rate remains close to constant in the optimal temperature range. Overall, ALD is a low temperature deposition technique with typical temperatures from 200ºC to 400ºC. Deposition is also

possible at much lower temperatures, enabling the use of polymer substrates. [30, p. 12][50, p. 2962, 2974]

The precursors are critical for the success of the ALD process. The precursors need to be volatile to ensure efficient transport into the ALD reactor and fast saturation of the surface. The precursors are typically gasses and volatile liquids, which can be supplied into the reactor from external cylinders [51]. The precursors need to be highly reactive towards each other to achieve fast saturation of the reactions. In addition, they need to react irreversibly and with a self-limiting reaction [30, p. 5]. They also require sufficient thermal stability at the process temperature to prevent thermal decomposition.

The chemistry of the precursors decides what material is obtained from the ALD process. Typically, one precursor brings a metallic species into the substrate and the other precursor brings a non-metal species, such as oxygen or nitrogen [30, p. 5]. The metallic precursors are generally *metal complexes*, such as $Al(CH_3)_3$ i.e. trimethylaluminum (TMA). In TMA, aluminum has three methyl ligands. The metal can react with hydroxyl groups of the substrate surface in an exchange reaction, where a bond is formed between the metal and the surface oxygen and one methyl ligand produces methane. The reaction happens until the surface is saturated. This reaction is shown for TMA [30, p. 6] in the following equation:

$$-OH + Al(CH_3)_3 \rightarrow -OAl(CH_3)_2 + CH_4 \quad . \tag{4.1}$$

Ideally, the reaction by-products, methane in the above case, are not trapped within the film. The remaining ligands of the metal complex act as passivating groups and prevent any excess TMA in the gas phase from reacting with the substrate. This feature makes the ALD reactions self-limited. [30, p. 5–6]

The excess precursor and reaction by-products are removed in a following purging step [51]. After the purge, it's time for the second precursor pulse. The second precursor is chosen so that it reacts with the passivating ligands of the already formed film. If metal oxides are desired to be deposited, water can be used as a precursor. For methyl ligands, water can react with the passivating methyl groups in a transfer reaction to produce methane, as shown below [30, p. 6]:

$$-OAl(CH_3)_2 + 2\,H_2O \rightarrow -OAl(OH)_2 + 2\,CH_4 \quad . \tag{4.2}$$

Passivating hydroxyl ligands will also be formed at the aluminum atoms. Upon saturation, all the methyl ligands have been changed into hydroxyl ligands. The hydroxyl ligands will then act as the functional surface sites for the next cycle and react with TMA. This explains the self-limiting nature of an ALD process. In addition, the passivating ligands explain why a layer thickness of much less than 1 Å can be deposited each cycle: the passivating ligands take space and the resulting steric effects limit the reactants from reacting with the substrate. [30, pp. 6–8]

The reactions depicted above for TMA and water lead to the formation of Al_2O_3. Other metal oxides can be obtained with different metal complex precursors. Besides oxides, also metal nitrides, metal fluorides and even elemental films can be obtained with ALD [50, p. 2966]. For this work, ALD will be used to fabricate ultra-thin TiO_2 films.

4.2.1 Deposition of titanium dioxide

Many different precursors have been used to fabricate TiO_2 layers with ALD. These include the titanium halides $TiCl_4$ and TiI_4, which produce corrosive hydrogen halides upon reaction with water [51]. Titanium alkoxides, for example titanium ethoxyde $Ti(OEt)_4$, are also used [52]. Thermal decomposition has been a problem for the alkoxides. Another titanium precursor is the *tetrakis(dimethylamino) titanium* (TDMAT) [52] shown in Figure 4.2. The oxygen containing precursor is typically water, but also hydrogen peroxide and ozone has been used.

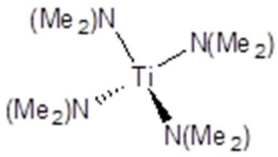

Figure 4.2 *Chemical structure of tetrakis(dimethylamino) titanium (TDMAT) used as a titanium precursor for ALD. Me = methyl group.*

Generally, ALD produces thin films with reasonably low defect levels, impurities and with good uniformity. When using water as the oxygen source, hydroxyl groups are trapped in the oxide as impurities. For TiO_2, the deposition temperature affects the resulting oxide structure. According to Jin *et al*. [52], at low temperatures in a TDMAT process, an *amorphous* structure is obtained, whereas at a temperature of 250ºC *anatase* crystal phase can be observed.

4.3 High-throughput ALD process

Most of the existing ALD reactors have been designed mostly for basic research, with only small outputs possible, for example single wafer at a time. However, there are two types of newish reactor types in use or in development, that offer high-throughput production needed for many industrial applications: the batch reactor and the spatial reactor. The idea of the batch reactor is to simply increase the reactor scale so that large batches or large areas can be deposited more economically. [50, p. 2980]

In a spatial reactor, the precursors are inserted continuously, but at different physical locations so that they won’t react in gas phase. There are purge gas flows located be-

tween these precursor gas inlets. Either the substrate or the gas inlets are moved translationally in relation to the other. The result is a continuous deposition process [50, pp. 2983–2984]. The spatial reactors can be designed suitable for flexible substrates and R2R processes. For example TNO has designed a R2R ALD technology for flexible substrates that can deposit > 1 nm/s [53]. Since ALD is suitable for both flexible substrates and low temperatures, it is a promising deposition method in flexible electronics e.g. for barrier layers, semiconductors and dielectrics.

5. CHARACTERIZATION OF THE OXIDE LAYER

In this section the methods used for the characterization of the fabricated TiO_2 layers are introduced. In this work, the main properties of interest were the oxide thickness, defect density (of the n-type semiconducting oxide) and chemical composition. *Mott-Schottky analysis* was used to determine the defect densities and *x-ray photoelectron spectroscopy* (XPS) to analyze the chemical composition.

5.1 Thickness of the oxide layer

The amount of reaction product formed at an electrode can be calculated with the Faraday's law (Equation 3.6), when the amount of electric charge passed through the electrode is known. In the case of anodic oxidation, the amount of anodized oxide formed at the anode is directly proportional to the thickness of the oxide layer. Heljo *et al.* [9] used the Faraday's law to calculate the anodized TiO_2 layer thickness. The result was consistent with thickness measurements performed using x-ray photoelectron spectroscopy (XPS), based on inelastic electron energy-loss background analysis.

Using the overall reaction for anodic oxidation of titanium (Equation 3.11), Faraday's law (Equation 3.6) can be expressed as

$$Q = z\,F\,n = z\,F\,\frac{m}{M} \quad , \tag{5.1}$$

where n (mol) is the amount, m (g) is the mass and M (g mol^{-1}) is the molar mass of the anodic TiO_2 formed. Mass of a substance depends on its volume and density, ρ. If the anodic oxide is a uniform layer, it has a volume defined by its thickness, d, and the surface area of the oxide. The surface area of the oxide is equal to the active area of the WE, A, where the oxide is formed. Using these relationships with Equation 5.1, the following equation for the thickness of the anodized oxide, d, can be derived:

$$Q = z\,F\,\frac{\rho A d}{M}$$

$$\Leftrightarrow \qquad d = \frac{Q\,M}{zF\rho A} \quad . \tag{5.2}$$

The variation of electric charge, dQ, with time, dt, is defined as the electric current [35, p. 14]:

$$I = \frac{dQ}{dt} \quad . \tag{5.3}$$

Charge transferred at the anode can, therefore, be calculated from the time integral of the measured cell current during the anodic oxidation:

$$Q = \int_0^t I \, dt \quad . \tag{5.4}$$

Inserting Equation 5.4 to Equation 5.2 gives the following equation:

$$d = \frac{M}{zF\rho A} \int_0^t I \, dt \quad . \tag{5.5}$$

The thickness of the anodized oxide can be calculated from Equation 5.5, if the cell current is measured as a function of time. The WE needs to have a well-defined area, where the anodization proceeds, in order for the equation to be suitable. Equation 5.5 assumes that the oxidation of titanium is the only reaction happening at the anode. If, however, other faradaic reactions are possible at the anode simultaneously, only a fraction of the total current goes to the studied oxidation process. With such simultaneous reactions, an efficiency term is needed in Equation 5.5. This term ensures that only the fraction of the charge, which is involved in the studied oxidation process, is used in the calculations. [36, p. 421]

In addition to the anodized oxide, the total oxide layer contains a native oxide layer, which forms spontaneously during air exposure. Heljo *et al.* [9] demonstrated, that the following equation

$$d_{tot} = d + d_{native} \tag{5.6}$$

gives a result for the total oxide thickness, d_{tot}, that is consistent with other measurements. d_{native} is the thickness of the native oxide layer and d is the thickness of the anodized oxide layer.

5.2 Mott-Schottky analysis

Among other methods, *capacitance-voltage* (C-V) measurements are often used to determine the doping density of a semiconductor. The C-V technique utilizes the dependency between the *space-charge region* (SCR) width of a semiconductor junction and the applied reverse-biased voltage. The SCR required in the method is formed when a suitable electrode is connected to the semiconductor, so that a Schottky barrier contact forms. A Schottky barrier contact with the semiconductor can be achieved for example with a deposited metal electrode or a liquid electrolyte contact. [54, pp. 61–62]

One way to determine the doping density, based on C-V measurements, is to perform the Mott-Schottky analysis. In the Mott-Schottky analysis, the *doping density* can be

calculated from the capacitance of the space charge region by using the so called Mott-Schottky relationship. The following Sections 5.2.1–5.2.3 examines more closely the Mott-Schottky analysis used in this work for the determination of the doping density of the fabricated TiO_2 layers.

5.2.1 The space-charge region at a liquid contact

Using an electrolyte contact to form the Schottky barrier in the semiconductor enables the C-V measurement to be carried out in an electrochemical cell similar to the anodization cell. A space charge region can form in a semiconductor, when brought into contact with an electrolyte. For the two phases (semiconductor and solution) to be in equilibrium, the electrochemical potential of the phases need to be identical. The electrochemical potential of the electrolyte is defined by *the redox potential of the electrolyte*. The electrochemical potential of the semiconductor is the Fermi level, which lies just below the CB for an n-type semiconductor. A movement of electrons across the semiconductor-electrolyte interface evens out the difference between the Fermi level and the electrolyte redox potential, similarly to when a metal electrode is immersed in an electrolyte. However, with a semiconductor the excess charge is not located only at the material surface, but instead extends in to the bulk of the material. This is the cause of the space charge region. [36, pp. 62–63][55]

The Fermi level of an n-type semiconductor, being close to the CB, is usually higher than the redox potential of the electrolyte. Equilibrium between the two phases is, therefore, reached by transport of electrons from the semiconductor to the electrolyte. The SCR formed in the n-type semiconductor is then positively charged. Formation of the SCR is presented in Figure 5.1. The SCR can also be called *the depletion region*, since it is emptied of the majority carriers. [55]

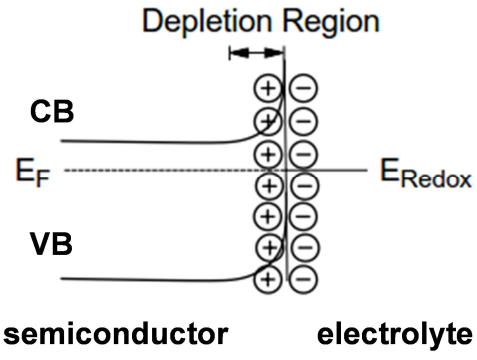

Figure 5.1 *The depletion region, i.e. space charge region, formed in an n-type semiconductor in equilibrium with an electrolyte solution. The space charge region causes upward bending of the CB and the VB of the semiconductor resulting in a Schottky barrier at the interface. E_F = Fermi level, E_{Redox} = Redox potential of the electrolyte, CB = conduction band, VB = valence band. Adapted from [55].*

A positively charged space charge region bends the CB and VB edges of the semiconductor upwards. This results in a Schottky barrier in the semiconductor electrode at open circuit. The Fermi level of the semiconductor can be controlled with an applied voltage bias. However, the applied voltage bias does not change the energy level of the bands at the interface (in the space charge region). Therefore, the applied potential, *V*, determines the magnitude of the *band bending* and the *width of the depletion region*. This is depicted in Figure 5.2.

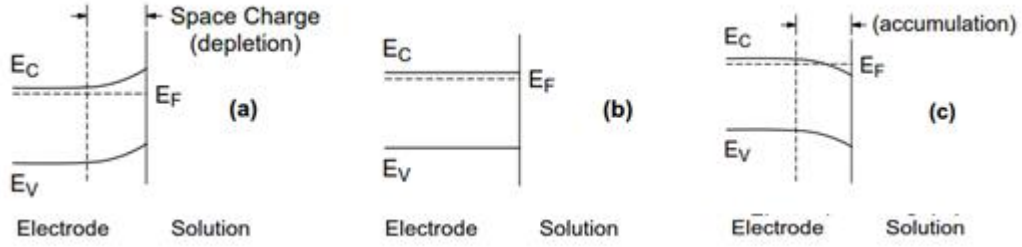

Figure 5.2 *Band bending for an n-type semiconductor immersed in an electrolyte solution. a) $V > V_{fb}$ a depletion region arises, b) $V = V_{fb}$ no band bending, c) $V < V_{fb}$ an accumulation region arises. V = applied potential at the semiconductor, V_{fb} = flat-band potential. Adapted from [55].*

When a suitably negative potential is applied to the semiconductor electrode, no band bending happens (Fig. 5.2(b)). This applied potential is referred to as *the flat-band potential*, V_{fb}. When the flat-band potential is applied, the semiconductor Fermi level is adjusted to the exact level of the electrolyte redox potential and no transfer of electrons across the interface happens. With potentials higher than the flat-band potential, a space charge region forms (Fig. 5.2(a)). With more negative potentials, an excess of majority carriers at the electrode forms an accumulation region (Fig. 5.2(c)) [54]. The flat-band potential defined here appears in *the Mott-Schottky equation* presented in Section 5.2.2. By controlling the applied voltage bias of the electrodes, the potential of the semiconductor and hence the width of the space charge region can be controlled, which lies at the hearth of the Mott-Schottky analysis.

5.2.2 The Mott-Schottky equation

The theory of the Mott-Schottky equation discussed below is considered for an n-type semiconductor with a Schottky barrier at a liquid interface. The semiconductor has a doping density, N_D. Figure 5.3 depicts the resulting space-charge region in the n-type semiconductor, when a reverse-bias DC voltage is applied. The SCR has a width of W_{scr}. The figure resembles a Schottky diode with metallic electrode (at the Schottky contact), but the following theory is for liquid contacts.

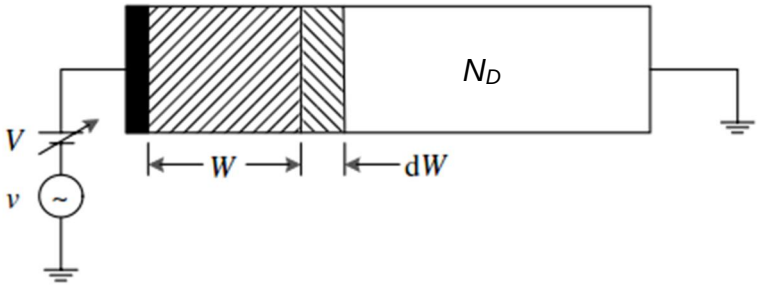

Figure 5.3 *A Schottky diode is reverse-biased with a DC voltage of V. W is the width of the resulting space-charge region. A small amplitude AC voltage, v, is superimposed on the DC voltage and increases the SCR width by an increment, dW, while at positive phase. Adapted from [54, p.62]*

The capacitance of the space-charge region, C_{scr}, when considered as parallel plate capacitor is

$$C_{scr} = \frac{\varepsilon_r \varepsilon_0 A_{sc}}{W} \quad , \tag{5.7}$$

where ε_r is *the dielectric constant* of the semiconductor, ε_0 is the permittivity of vacuum and A_{sc} is the area of the semiconductor-electrode interface [54, p.63]. Equation 5.7 shows how the capacitance of the SCR is determined by its width.

The definition of differential capacitance is

$$C = \frac{dQ}{dV} \quad , \tag{5.8}$$

where *dQ* is the electric charge stored when a voltage *dV* is applied to a capacitor. The differential capacitance of the space charge region can be measured, when an AC voltage of small amplitude and high frequency is superimposed onto the reverse-bias DC voltage. This sinusoidal AC voltage, when at negative phase, adds a charge increment of *-dQ* to the metal electrode. For charge neutrality, an increment of *+dQ* needs to be stored at the semiconductor resulting in a change in the differential capacitance. [54, p. 62–64]

The Mott-Schottky equation enables the calculation of the doping density, when the differential capacitance of the space charge region is measured as a function of the applied voltage [56]. This equation is derived from Poisson's equation in one dimension

$$\frac{d^2\Phi}{dx^2} = -\frac{\rho}{\varepsilon_r \varepsilon_0} \quad , \tag{5.9}$$

where Φ is the potential difference and ρ is the charge density a distance x away from the semiconductor surface [57]. Equation 5.9 relates the charge density of the semiconductor to the potential drop in the SCR of the semiconductor. The complete derivation of the Mott-Schottky equation is presented in the Supplemental Material part of Reference [57], and will not be covered here. By using Boltzmann distribution for the electrons at the SCR and Gauss' law for the electric field caused by the charge in the SCR, Equation 5.9 can be solved to yield the Mott-Schottky equation:

$$\frac{1}{{C_{scr}}^2} = \frac{2}{\varepsilon_r \varepsilon_0 {A_{sc}}^2 e N_D} \left(V_{el} - V_{fb} - \frac{k_B T}{e} \right) \quad . \tag{5.10}$$

In Equation 5.10, C_{scr} is *the differential capacitance of the space charge region*, e is the elementary charge, V_{el} is the applied electrode potential (of a semiconductor electrode in an electrolyte), k_B is Boltzmann's constant and T is the absolute temperature [57].

Equation 5.10 shows a linear dependency between C_{scr}^{-2} and the applied electrode potential, V_{el}. Hence, a Mott-Schottky plot can be constructed by plotting C_{scr}^{-2} as a function of the applied potential, which yields a straight line. The slope of the line can used to determine the doping density of the semiconductor. An ideal Mott-Schottky plot for an n-type semiconductor is presented in Figure 5.4. The flat-band potential can be determined by extrapolating the straight line to the potential axis.

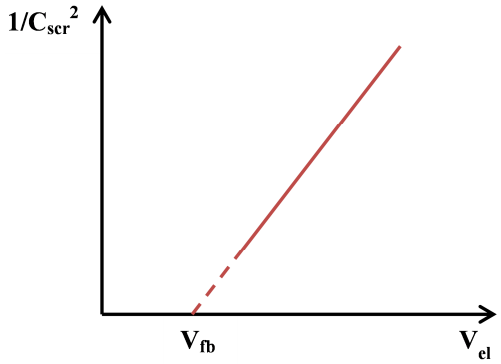

Figure 5.4 *Ideal Mott-Schottky plot for an n-type semiconductor. Doping density of the semiconductor can be determined from the slope of the line. V_{fb} = flat-band potential.*

The doping density can be calculated from the slope, S, of the Mott-Schottky plot. Based on Equation 5.10, the doping density can be expressed as:

$$N_D = \frac{2}{\varepsilon_r \varepsilon_0 e} S^{-1} \quad , \tag{5.11}$$

where

$$S = \frac{d(C_{scr}/A)^{-2}}{dV_{el}} \quad .$$

Mott-Schottky analysis consists of C-V measurements and subsequent construction of Mott-Schottky plots, which should yield a straight line according to Equation 5.10. The doping density of the semiconductor can be calculated from the slope of the line with Equation 5.11. The measurement of the differential capacitance of the space charge region is discussed in the following section.

5.2.3 Measuring the space-charge region capacitance

In general, electrochemical cells do not show *a linear electric behavior*, i.e. doubling the cell voltage does not necessarily double the cell current. However, by using small AC excitation potentials, electrochemical cells show *pseudo-linear behavior*. In pseudo-linear behavior, a small sinusoidal excitation potential leads to a sinusoidal current response, with the same *radial frequency, ω,* but in different phase [58]. The sinusoidal excitation signal (i.e. AC voltage), *v*, can be expressed as

$$v = V_0 \sin(\omega t) \quad , \tag{5.12}$$

where V_0 is the signal amplitude. The current response signal, *i*, can be defined similarly as

$$i = I_0 \sin(\omega t + \phi) \quad , \tag{5.13}$$

where ϕ is the phase angle and defines the magnitude and direction of the phase shift between the excitation and response signals [36, pp. 370–371].

The total impedance, Z, of an electric system can be represented as

$$Z = Z' - jZ'' \quad , \tag{5.14}$$

where Z' and Z'' are the real and the imaginary parts of the impedance, respectively [36, p. 373]. An electrochemical cell can be thought of as impedance against small sinusoidal excitations (AC voltage or current). Therefore, electrochemical cells can be represented with *equivalent circuits* (ECs) of resistors and capacitors, which give the same current response (amplitude and phase) under AC voltage excitation compared to the actual cell [36 p. 376]. An electrochemical cell consisting of a semiconductor electrode in an electrolyte has typically been simplified to an EC of a resistor and a capacitor connected in series [48, 9, 55]. However, this simplification only applies at certain high enough frequencies. A series RC-circuit is depicted in Figure 5.5.

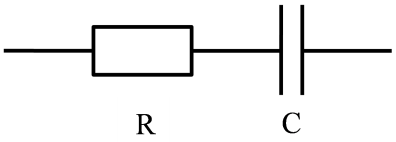

Figure 5.5 *A series RC circuit used as the equivalent circuit for some electrochemical cells.*

The applicability of an EC for an electrochemical system can be determined with *electrochemical impedance spectroscopy* (EIS). In EIS, the electrochemical impedance of a system is measured as a function of *the AC voltage frequency*, *f*. The resulting EIS data can be analyzed by fitting it to an EC model. In the work of van de Krol *et al.* [56] TiO_2 layers grown on ITO substrates were analyzed with EIS. It was found that at excitation frequencies over 10 kHz, the electrochemical system could be accurately described with the series RC circuit. A resistor does not have an *imaginary impedance component* [58]. Its impedance, i.e. its resistance *R*, is independent of frequency. In contrast, a capacitor only has an imaginary impedance component. Therefore, if the series RC equivalent circuit is applicable, the total capacitance of the system, C_{tot}, can be easily determined from the imaginary part of the impedance [55] with the equation:

$$Z'' = \frac{1}{\omega C_{tot}} = \frac{1}{2\pi f C_{tot}} \quad . \tag{5.15}$$

A space charge region and the related SCR capacitance, C_{scr}, arise when a semiconductor is immersed in an electrolyte as discussed in Section 5.2.1. However, other capacitive elements may exist at the semiconductor-electrolyte interface as well. The other main contributor to the capacitance is *the double layer capacitance* mentioned in Section 3.1.2. The two capacitances can be considered to be connected in series and, hence, the total capacitance is

$$\frac{1}{C_{tot}} = \frac{1}{C_{scr}} + \frac{1}{C_{dl}} \quad , \tag{5.16}$$

where C_{dl} is the capacitance of the electrical double layer [48]. The double layer capacitance is in general 2-3 orders of magnitude larger than the SCR capacitance, and consequently it has a negligible influence to the total capacitance [55]. The measured capacitance of the electrochemical system can, therefore, be assumed to be the space charge region capacitance of the semiconductor. However, the series RC equivalent circuit must be applicable to the electrochemical cell with the frequencies used in the C-V measurements.

5.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is one of the most common tools for surface analysis, especially chemical analysis. It is also called *electron spectroscopy for chemical analysis* (ESCA). The basis of this analytical method is *the photoelectric effect* [59, pp. 201–202]. A photon with a suitable energy (*hf*), *h* being Planck's constant and *f* the frequency, can interact with the electrons of an atom, which leads to the emission of this electron as a photoelectron with a measurable kinetic energy, E_k [15, pp. 5–6]. X-rays, with energies in the region of 1 keV, interact with the core-level electrons (i.e. inner electron orbitals) of atoms. The kinetic energy of the emitted photoelectron depends on the energy of the absorbed quantum and *the binding energy* of the electron, E_B. The binding energy is defined as the energy required in removing the electron from its electron orbital to infinity with zero kinetic energy, i.e. to the vacuum level. With XPS, E_B can be determined relative to the Fermi level of the specimen as

$$E_B = hf - E_k - \phi_{spec} \quad , \tag{5.17}$$

where ϕ_{spec} is the work function of the spectrometer, which affects the kinetic energy of the detected photoelectron. [59, pp. 203–204]

Equation 5.17 shows, that it is possible to calculate the binding energy when the kinetic energy of the emitted photoelectron is measured. The binding energies are characteristic to the orbitals from which the photoelectrons are removed. Therefore, studying the emitted photoelectrons from a specimen exposed to X-ray radiation, leads to a lot of information about the chemical nature of the specimen. *Photoelectron energy spectrums* (where energy axis is the binding energy) can be constructed and are basically a ''chemical fingerprint'' of the specimen. At a simple level, qualitative elemental identification can be accomplished with a so-called survey scan, which covers a large range of binding energies. *High resolution spectra* acquired at specific binding energy ranges can lead to information about the chemical state (e.g. oxidation state) of the atoms and quantitative elemental analysis in the near-surface region. [60, p. 485–486]

5.3.1 Instrumentation

A schematic design of an X-ray photoelectron spectrometer is depicted in Figure 5.6 [60, p. 487]. The X-ray radiation is generated at the source, typically, when an electron flow from a cathode hits the target anode surface. X-rays produced at the anode have characteristic energies that depend on the anode material. In XPS the X-rays should have larger energies than the examined binding energies and also a small linewidth *i.e.* a very narrow energy range. The most common X-ray sources (anodes) are Mg K_α and Al K_α with X-ray photon energies of 1253.6 eV and 1486.6 eV, respectively. [59, p. 200]

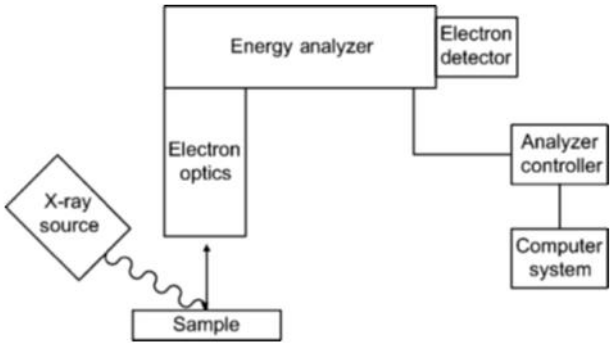

Figure 5.6 *A scheme of an X-ray photoelectron spectrometer.*

The emitted photoelectrons are captured with electron optics. The energy analyzer sorts the photoelectrons based on their kinetic energy. The intensity of the photoelectrons is determined with an electron detector and this data is later processed into an energy spectrum. The XPS experiments are carried out in *ultrahigh vacuum* (UHV) conditions to ensure clean sample surfaces and to prevent the scattering of the photoelectrons by gas molecules. [60, p. 487–488]

The X-ray beam penetrates the sample material to a certain depth. This depth together with the beam diameter (which can range from 1 μm to 5 mm) defines the volume where the specimen electrons are excited. Photoelectrons are emitted from this entire volume. However, because of the typical kinetic energies of the photoelectrons and the short inelastic mean free path inside the material, characteristic energies will be observed only for the photoelectrons generated a few nanometers from the surface. The photoelectrons generated in the deeper regions contribute to the background emission. [60, p. 487]

6. MATERIALS AND METHODS

This section covers the materials used in this work, the fabrication process of the devices and the measurements and methods used. The experimental work done for this thesis is a continuation to the work done by Heljo *et al.* [9]. The fabricated vertical diodes are from now on referred to as the devices. The devices were fabricated similarly with the previously mentioned work utilizing existing equipment. Some small changes were made to the fabrication process.

6.1 Materials

ITO coated polished float glass substrates were purchased from Delta Technologies. The substrate dimensions were 25 x 25 x 1.1 mm with an ITO coating on one surface. According to the manufacturer, the substrates had a sheet resistance of 15–25 Ω/sq and a nominal ITO coating thickness of 60–100 nm.

Organic solvents were used during various process steps. The solvents were purchased from VWR International. The organic semiconductor used in the devices was Livilux PDY-132, also known as Superyellow, purchased from Merck. Superyellow is a PPV derivative. The chemical structure proposed in the literature [61][62] for Superyellow is shown in Figure 6.1. The semiconductor was delivered as a powder. A semiconductor solution of 4 mg of Superyellow per ml of solvent was prepared. The solvent was toluene (AnalarNormapur grade, from VWR) and semiconductor dissolution was ensured by magnetic stirring overnight. The Super yellow solutions used for devices were reasonably fresh and stored appropriately (protected from light).

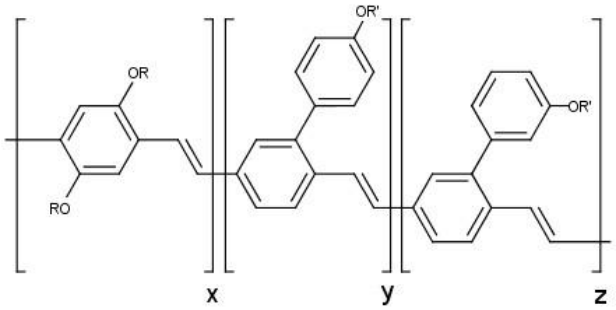

Figure 6.1 *The chemical structure of Superyellow proposed in literature [61][62].*

Using the anodic oxidation method, the TiO_2 layers were fabricated by oxidation of thin titanium layers. The devices also required an aluminum top-electrode layer. These thin metal layers were deposited by evaporation of pure metal sources. The aluminum and

titanium metals were purchased from Kurt J. Lesker Company as pellets with purities of 99.995% and 99.999%, respectively. TDMAT (see Section 4.2.1) and water were used as the precursor gases in the ALD process.

6.2 Fabrication and characterization of the TiO_2 layers

Two methods were used to fabricate the TiO_2 films on top of the ITO: anodic oxidation of titanium films and ALD. The first step in the device fabrication process is the cleaning of the ITO/glass substrates. As delivered, the substrates had visible smears and a careful cleaning is also recommended by the manufacturer. The substrate cleaning was done in several steps inside a cleanroom. The cleaning process consisted of: acetone rinse, ultra-sonication in acetone bath for 10 minutes, isopropanol (IPA) rinse, ultra-sonication in IPA bath for 10 minutes, deionized (DI) water rinse, blow dry with clean air and UV-ozone treatment for 10 minutes.

The intention of the chosen procedure was to get rid of contaminant particles and organic substances by a combined mechanical-chemical cleaning. All smears were visibly removed from the clear, transparent substrates and no water spotting was observed. Conductivity of the ITO was retained or even enhanced by the cleaning as observed with an ohmmeter.

6.2.1 Anodic oxidation of thin titanium layers

The TiO_2 layer fabrication consisted of deposition of a thin titanium layer and subsequent oxidation of the layer. The titanium layers were evaporated on to the cleaned ITO substrates. The evaporation was carried out immediately after the UV-ozone treatment of the cleaning process. All evaporations were carried out with the Leybold L560E electron beam evaporator (Fig. 6.2). Electron beam evaporation is a physical vapor deposition (PVD) method where an electron beam bombardment is used to vaporize a target material inside a vacuum chamber. The vapors will then precipitate into solid, coating the vacuum chamber and target substrates. Desired coating patterns can be made with a shadow mask.

A vacuum pressure of 10^{-7} mbar and an evaporation rate of 0.5 Å/s were used to deposit different titanium layers (2, 3 and 4 nm) onto the cleaned ITO substrates. The deposition pattern was a square (22 x 22 mm) in the center of the ITO surface. The deposited layer thickness was measured by a calibrated quartz crystal microbalance during the evaporation. When the substrates were removed from the vacuum after the evaporation, they were exposed to air. For titanium, air exposure leads to the formation of a passive TiO_2 layer, i.e. the native oxide. The complete oxidation of the titanium layer was achieved via anodic oxidation.

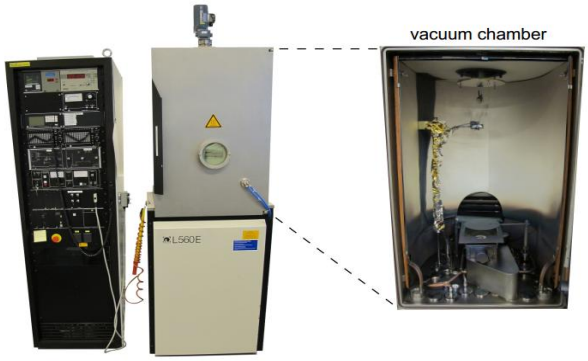

Figure 6.2 *Electron beam evaporator (Leybold L560E) used in the experimental work.*

All the electrochemical experiments were performed with Zahner Zennium Electrochemical Workstation (Zahner Elektrik GmbH), referred from now on as the potentiostat. Figure 6.3 represents the experimental set-up used in the anodic oxidations. The experimental set-up consisted of: a custom made sample holder, a reference electrode (RE) and a counter electrode (CE). These were immersed in an electrolyte solution and connected to the potentiostat. The potentiostat was controlled with a PC through the Thales software. The sample holder allowed electric contact from the WE, the ITO layer, to the electrolyte only through the Ti/TiO_2 layers. The contact area was defined as a circular area of 2.4 cm^2. Electrolyte flow into the sample holder was prevented with rubber seals. Electric connection from the ITO to the potentiostat was achieved with spring loaded gold contacts and electric wiring.

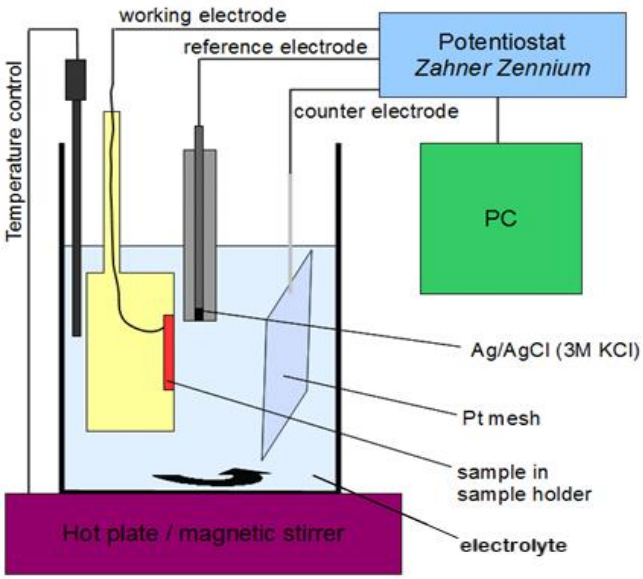

Figure 6.3 *An illustration of the experimental set-up used for anodic oxidation and related electrochemical measurements.*

A platinum mesh, with an effective surface area of 25 cm^2, was used as the CE and was fixed at a distance of 18 mm from the WE. The RE was installed between the WE and the CE, as close as possible to the WE. Ag/AgCl in 3 M KCl –electrode (purchased from SI Analytics) was used as the RE. All potentials shown in this work are either defined versus the standard hydrogen electrode (SHE) or versus the Ag/AgCl in 3 M KCl –electrode (at the electrolyte temperature). The RE in use has potential of +0.21 V vs SHE at 25°C [63].

The anodic oxidations were performed 48 hours after the beginning of the air exposure for each sample. This was done to ensure that a similar native oxide layer thickness had been reached. The anodizations were carried out similar to the work of Heljo *et al.* [9] with a potentiodynamic mode. The potentiodynamic anodization process is depicted in Figure 6.4. The process consisted of four steps. First, no current is allowed through the cell for one minute and the open circuit potential (OCP) of the WE is measured. In the second phase, the WE potential is linearly ramped up to the maximum cell potential, V_{max}, with a sweep rate of 50 mVs^{-1}. The V_{max} is then kept for two minutes. Lastly, the circuit is again opened and the OCP measured for one minute. The actual anodic oxidation happens during the dynamic phase. The constant potential phase and the OCP phases give qualitative information about the success of the anodization process.

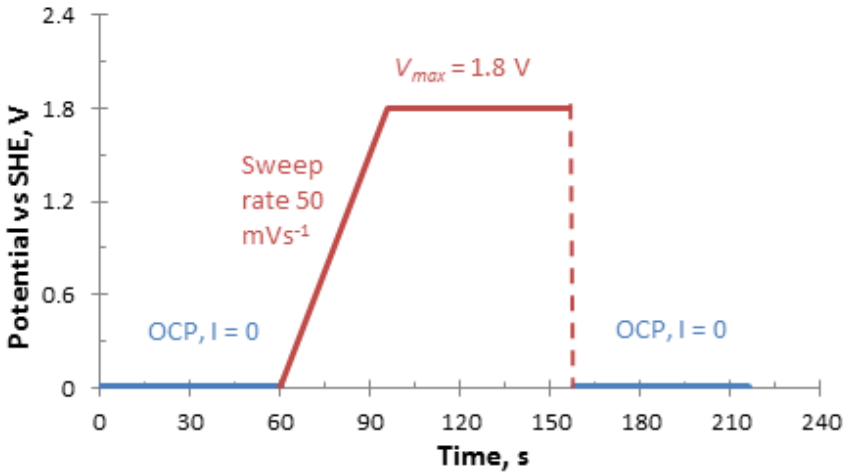

Figure 6.4 *The potentiodynamic anodization process used. In this case,* V_{max} = 1.8 V. *Sweep rate of the linear ramp up of potential is 50* mVs^{-1}.

The anodizations were carried out in 0.10 M Na_2SO_4 electrolyte at room temperature with constant magnetic stirring. Different V_{max} values were used depending on the electrolyte temperature and evaporated titanium layer thickness.

6.2.2 ALD of ultra-thin TiO_2 films

Ultra-thin films of TiO_2 were also grown with ALD onto the glass/ITO substrates. The substrates were cleaned as mentioned before. Due to the following electrical measure-

ments, an electric contact point to the ITO was required. The surfaces also required a specific pattern, shown in Section 6.3, to achieve the vertical diode structure. For initial tests, the sample surfaces were masked with heat-resistant Kapton tape.

The atomic layer depositions were outsourced to the Surface Science Laboratory, TUT. The ALD system was Picosun Sunale ALD R200 Advanced reactor. TDMAT and water were used as precursors. Deposition temperatures of 100ºC, 150ºC and 200ºC were used. The aim was to reach a deposition thickness of ~ 4.5 nm (similar to previous anodized samples) by using previously determined cycle recipes and suitable number of cycles.

6.2.3 EIS and C-V measurements

In order to use the RC equivalent circuit for C-V measurements, the electrochemical system should behave like an RC-circuit at this frequency. EIS measurements were performed with a frequency range of 40 Hz - 10 kHz to determine the applicability of the RC model to the electrochemical cell under study. The experimental set-up was the same as in anodic oxidation. However, the electrolyte was not stirred and measurements were carried out in 0.40 M Na_2SO_4 electrolyte at room temperature. A constant potential bias of 0.4 V and AC amplitude of 5 mV were used in the measurements. The results of the EIS measurements are presented in Section 7.3.3. Based on these results; the RC equivalent model is suitable at a frequencies above 2 kHz. EIS measurements were performed only for some samples.

C-V measurements were performed for each ITO/TiO_2 sample using a frequency of 3 kHz. The objective was to determine the defect density of the oxide film, based on the Mott-Schottky analysis described in Section 5.2. The measurement set-up was exactly like in the EIS measurements. The AC amplitude was 10 mV. In general, the voltage was swept from -0.3 V to 1.0 V with steps of 0.01 V or 0.02 V. A delay time of 6 s was used for measurements at each step. After the measurements were done, each sample was rinsed with DI water and blow dried.

6.2.4 XPS measurement

X-ray photoelectron spectroscopy was used to investigate the chemical composition and structure of the oxides. The analysis was carried out for ALD grown layers, one anodized sample and one native oxide sample. The anodized sample was prepared as described above with an evaporated 3 nm thick titanium film. The titanium film was anodized with the previously mentioned potentiodynamic mode and V_{max} = 1.80 V (Fig. 6.4). The native oxide sample had an evaporated 3 nm Ti layer, but was not anodized and only had the native oxide formed via oxidation in air.

The XPS measurements were outsourced to the Surface Science Laboratory, TUT. Measurements were made with VG Microtech Multilab system. The experiments were carried out in 45° emission and the detection area was ~600 µm in diameter. Excitation was achieved with non-monochromatized Mg K_α X-rays, with energy of 1253.6 eV. In addition to survey scans, high-resolution spectra were analyzed for C 1s, O 1s, Ti 2p, In 3d, Sn 3d, Cu 2p and S 2p. The sampling depth is over 5 nm for Ti 2p and In 3d XPS signals. In the compositional analysis, a Shirley type or linear background was subtracted from the spectral components and a combination of Gaussian and Lorentzian line shapes were fitted.

Inelastic electron energy-loss background analysis [64][65] was used for the determination of the oxide film thickness. For this method, spectra of pure overlayer and substrate were measured, respectively, from TiO_2 and ITO reference samples.

6.3 Device fabrication

The overall device fabrication process is presented in Figure 6.5 for the anodized samples. Steps 1 and 2 do not exist for the ALD samples. For the ALD samples, etching (step 4) is performed before the ALD process and the TiO_2 is grown on top of the etched ITO pattern.

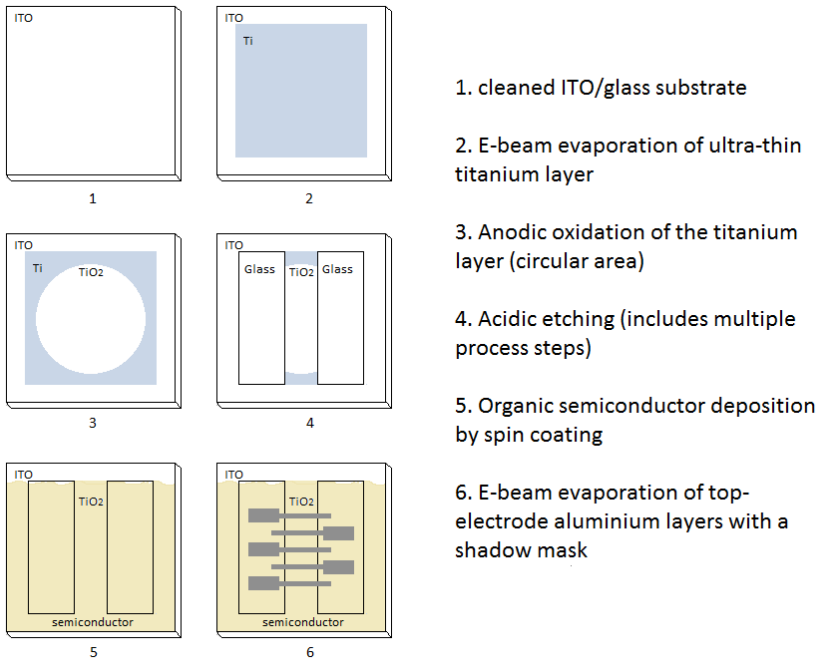

Figure 6.5 *The main steps in the device fabrication process for an anodized sample.*

Steps 1, 2 and 3 have already been covered in Section 6.2. The next step for the anodized samples is the wet etching process, where the desired ITO/TiO_2 pattern is obtained. Then, the organic semiconductor and the top-electrode layers can be deposited.

By using these process steps, vertical diode structures with well-defined effective areas can be fabricated.

6.3.1 Photolithographic patterning and wet etching

Photolithography was used to pattern the samples for the subsequent wet etching process (step 4 in Fig. 6.5). The samples were cleaned with acetone and IPA rinses and blow dried. In addition, the samples were kept at 90°C for 15 minutes for further drying. AZ ECI 3027 (from MicroChemicals), a positive photoresist solution was spin coated with a rotation speed of 2000 rpm for 60 s. Spin coated samples were baked in the oven at 90°C for 15 minutes. Light exposure of the resist was minimized. The desired coating pattern was achieved by a 60 s UV-exposure from one side through a photo mask and development in 0.20 M NaOH solution. During the development, the photoresist dissolved completely from the areas exposed to UV light. Unexposed areas were visibly intact.

The wet etching was accomplished with a prepared acid mixture. DI water, concentrated HNO_3 (70 w-%) and concentrated HCl (36 w-%) were mixed with a volume ratio of 25:2:23, respectively. The acid mixture was heated to 60°C on a hotplate. Samples were etched for 10 minutes. The etching result was examined visually and with an ohmmeter from the etched areas, to make sure that the conductive ITO had been completely etched. The remaining photoresist mask was removed with acetone rinse and the samples were carefully cleaned with acetone, IPA and DI-water rinses.

6.3.2 Semiconductor and top-electrode deposition

The organic semiconductor, Superyellow, an alkoxy PPV manufactured by Merck, was deposited by spin coating. A Superyellow solution of 4 mg/ml in toluene was used. By using different rotation speeds of the spin coater various semiconductor thicknesses can be achieved. In general, a speed of 2500 rpm was used for 60 s. These parameters are similar to the ones used by Heljo *et al.* [9]. Instantly after the spin coating, the samples were baked in oven at 90°C for 5 minutes in order to remove any remaining solvent. A cloth soaked in acetone was used to gently wipe the semiconductor off from the edge of the sample (shown in steps 5 of Fig. 6.5). The purpose was to reveal the ITO surface so that an electrical contact can later be made to the ITO-electrode.

A 200 nm thick aluminum top-electrode was deposited with the Leybold L560E evaporator. The spin coated samples were installed into the vacuum chamber and were kept under vacuum for at least 12 hours before evaporation. A shadow mask was used to get the desired electrode pattern. The evaporation rate was 3 Å s^{-1} and the vacuum level 10^{-8} mbar. The evaporation of the aluminum layer completes the device fabrication process. Current-voltage (I-V) measurements were then made to examine the behavior of the devices.

In addition to the aforementioned devices, reference devices without the TiO_2 layer were also fabricated. The fabrication process for the reference devices was the same as for the anodized samples except without the titanium evaporation and oxidation.

6.4 Device characterization

A finished sample is shown in Figure 6.6. One sample contained 14 individual devices with the vertical diode structure shown.

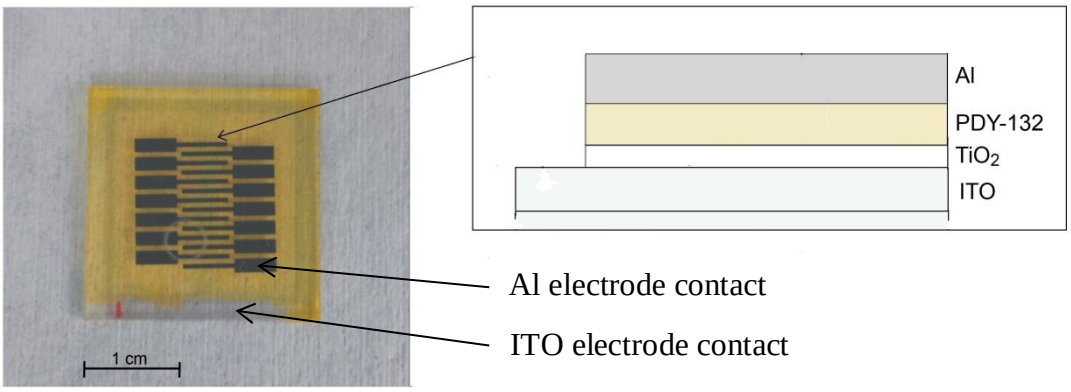

Figure 6.6 *A top-view picture of a finished sample shows the evaporated aluminum electrode pattern and electrical contact points for the ITO electrode and Al-electrode of a single device. Scheme on the right depicts the vertical diode structure of the devices (not in scale).*

The devices had an active area of ~ 1 mm^2, defined by the width of the patterned ITO line, ~ 2 mm, and the width of the Al-electrode patterns, ~ 0.5 mm. These dimensions were measured accurately with an optical microscope (Olympus BX 51), with the results presented in Section 7.4.

6.4.1 Electrical measurements

All electrical measurements were performed with the Zahner Zennium workstation, with the same set-up used by Heljo *et al.* [9]. The Zennium instrument was operated in the two-electrode configuration. ITO layer was connected as the WE and Al as the CE in the devices. Electrical connections from the Zennium were achieved with coaxial cables and cantilever-type mechanical probes. A device under test and the contact probes is shown in Figure 6.7. The measurements were carried out inside a grounded metal box under darkness.

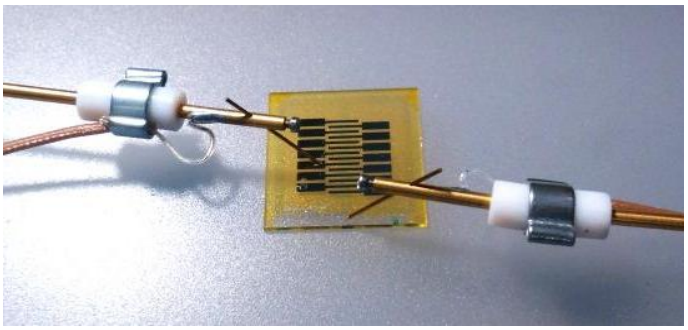

Figure 6.7 *A fabricated diode under test. Probes are placed in contact with the device electrodes.*

I-V characteristics of the devices were recorded at room temperature. It was observed that the device behavior was dependent on air exposure. Therefore, I-V measurements were performed swiftly and immediately after a sample had been taken out from the vacuum chamber of the evaporator. Measurements were carried out in the reverse bias, i.e. with ITO electrode negatively biased, with a typical voltage range of -20 V to 0 V. The voltage was swept to both directions with a typical scan rate of 500 mV s^{-1}.

6.4.2 Semiconductor thickness measurements

In general, interferometers utilize the wave character of light to analyze height differences in a sample surface. Two light beams follow different paths: the first path includes a reference surface; the second includes the studied surface. The beams are later recombined and *interference* occurs. The intensity of the resulting beam depends on the differences in the path lengths. In *phase shifting interferometry* (PSI), the phase of the interference is directly proportional to the surface height. [66, pp. 167–168]

The thickness of the spin coated OSC film was determined for several samples with an optical profilometer (Wyko NT1100, from Veeco). The measurements were made utilizing PSI mode. In PSI mode, the vertical resolution of the instrument is < 0.1 nm. However, the measurement requires a physical height step in the film for film thickness determination. These steps were produced by gently scratching thin lines on the sample surface with a scalpel. The OSC film was removed from these lines forming a measurable height step between the OSC and the exposed TiO_2 surfaces.

7. RESULTS AND DISCUSSION

The most important results of the performed experiments are covered in this section. In addition, the conclusions drawn from the results are presented.

7.1 Reference devices

I-V measurements were made for the ITO/Superyellow/Al reference devices. I-V plot for a device is presented in Figure 7.1. No significant differences were observed between several reference devices with similar structures. The measurements were made with a scan rate of 500 mV s^{-1} at room temperature and room air.

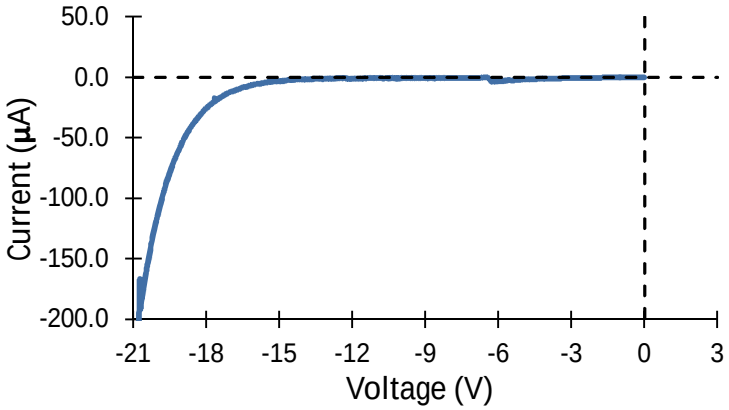

Figure 7.1 *I-V plot for a reverse biased (ITO is negative) reference device with the structure ITO/Superyellow/Al. This is the studied organic tunnel diode structure without the interfacial TiO_2 layer.*

The reference devices behave like conventional diodes when reverse biased. Plots recorded for a same device in both scan directions were almost identical, indicating no hysteresis. The reference diodes showed nearly constant and small leakage current, approx. 5 µA, at low negative voltages. When the negative voltage exceeds -15 V, the reverse current starts to increase rapidly, *i.e.* diode breakdown occurs. This is a reasonable behavior for the diode structure used [9].

7.2 Semiconductor layer thickness

The thickness of the semiconductor layer was measured from the diode area with an optical profilometer utilizing phase shifting interferometry. An example of the measurement data is presented in Appendix A. Thickness measurements were made from five fabricated samples with multiple measurements for each sample. The spin coated

semiconductor layer was fabricated similarly for each sample: 4 mg/ml Superyellow-toluene solution, rotation speed of 2500 rpm for 60 seconds and solvent evaporation in oven at 90ºC for 5 minutes. Results are presented in Table 7.1.

Table 7.1 Compilation of the semiconductor thickness measurement results. Average thickness for each sample based on at least three separate measurements.

Sample	Average thickness (nm)	Standard deviation (nm)
1	34.0	1.8
2	34.0	1.7
3	34.5	2.2
4	33.1	2.5
5	31.4	0.9

Based on the results, a spin coated semiconductor layer is highly uniform in a sample. Therefore, there exist only slight differences between the layer thicknesses of separate diode devices on the same sample. The highest measured standard deviation for a sample was 2.5 nm. The differences can arise from the specific topography of the ITO/glass substrate.

Layer thickness differences between samples were also small, within a few nanometers. These differences can be explained in part by very small differences in the concentration of the semiconductor solutions used. Based on all separate measurements, an average thickness of ~34 nm was obtained for the mentioned spin coating process. For similar organic tunnel diode devices, Yoon *et al.* [7] and Heljo *et al.* [9] used nominally 25 nm thick OSC layers and 40 nm thick layers, respectively.

7.3 Fabrication of TiO_2 layers with anodic oxidation

The initial focus of the experimental work was to replicate the experiments done by Heljo *et al.* [9] and obtain the same results. The exact same experimental set-up was used. The intention was to repeat the electrochemical anodic oxidation experiments and the fabrication and I-V characterization of the tunnel diodes.

7.3.1 Initial anodization

The anodic oxidations were initially carried out for samples with evaporated 3 nm thick titanium layers. A native oxide layer had formed during a constant 48 hour air exposure at RT. Full oxidation was completed by anodic oxidation. The potentiodynamic anodization process shown in Figure 6.4 was used. The current-time plot for a typical sample is shown in Figure 7.2.

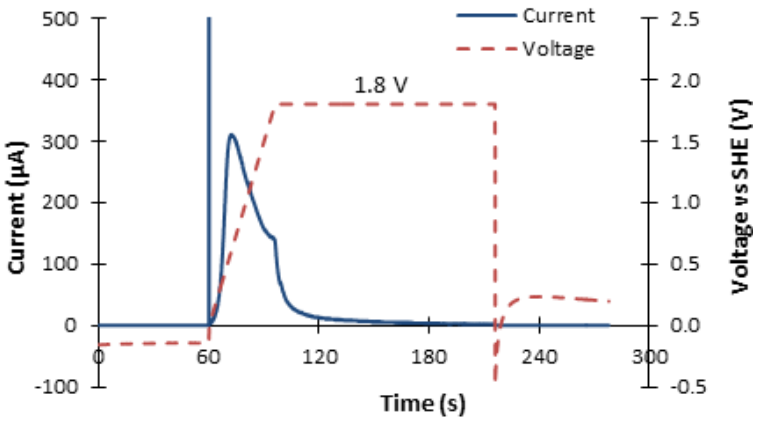

Figure 7.2 *Cell current and voltage plotted versus time for the anodic oxidation of an evaporated 3 nm thick titanium sample. The voltage plot represents the potentiodynamic process where voltage is controlled. OCP is measured during the first and last minute of the process. The anodic current occurs mainly during the voltage ramp up.*

A very high current peak can be observed at the start of the dynamic phase of the process (at t = 60 s in Figure 7.2). This anodic current peak is caused by the charging of the electric double layer as the WE polarity changes from negative to positive. The charging lasts only for a fraction of a second. The anodization current occurs mainly during the linear voltage ramp up (60 s $\leq t \leq$ 96 s). At first, the voltage has to increase a little until the current begins to increase rapidly. This short delay in the anodization is likely caused by the already formed native oxide layer. The native oxide inhibits the migration of ions from the electrolyte to the metal-oxide interface, where the oxide growth occurs under most experimental conditions [33, p. 2909].

The anodic current reaches a peak value at a relatively low voltage and then begins to fall steadily. This happens due to the ultra-thin, finite nature of the anodized films. A constant saturated current would run in an ideal potentiodynamic process for thick layers. For Figure 7.2, the peak current is 310 µA at 0.61 V. When t < 96 s, the constant voltage phase starts and the current begins to decrease rapidly. The current falls to a level of ~1-5 µA during the two minute hold-time.

If a higher V_{max} value was used in the process, the current began to increase at the end of the dynamic phase. This indicates the start of a different redox process. A likely possibility is the electrolysis of water. The electrolysis of water is possible above 1.23 V based on the standard reduction potentials of the half reactions [39]. In Figure 7.2, a negligible current flows during the constant voltage hold-time. However, this current increased dramatically whenever higher V_{max} values were used, which seems to indicate increasing electrolysis of water.

The shape of the current-time plot has a very good reproducibility. It was found out that the evaporation of the titanium layers was crucial on the behavior. Titanium layers that were evaporated in the same batch showed negligible differences during the anodic oxi-

dation. However, samples from different evaporation batches exhibited some differences even though the evaporation was carried out with the same parameters. This seems to indicate that the evaporated titanium layer thickness slightly varies between different evaporations. The calibrated quartz crystal microbalance, used in the thickness measurement during evaporation, might be sensitive to a thermal shock during the beginning of the unconventionally short evaporation process.

The charge transferred at the WE can be determined by taking the integral of the current-time plot (Eq. 5.4). For the sample of Figure 7.2, the transferred charge was 0.006436 C. The density of the amorphous TiO_2 will be assumed to be 3.8 g cm^{-3} as in the work of Heljo *et al.* [9]. The thickness of the anodized oxide, *d*, can be determined with equation 5.5. Assuming 100 % efficiency, the anodized thickness for the sample in Figure 7.2 is

$$d = \frac{M}{zF\rho A}\int_0^t I\,dt = \frac{79.88\ \frac{\text{g}}{\text{mol}}}{4 \times 96485\ \frac{\text{C}}{\text{mol}} \times 3.8\ \times 10^{6}\ \frac{\text{g}}{\text{m}^3} \times 2.4\ \times 10^{-4}\ \text{m}^2} \times 0.006436\ \text{C} \approx 1.5\ \text{nm}\ .$$

Using the same fabrication process and process parameters as mentioned above, the measured anodized oxide thickness varied from 1 nm to 1.5 nm between samples. This variation is thought to occur due to differences in the evaporated titanium layer thicknesses as previously mentioned.

7.3.2 X-ray photoelectron spectroscopy

XPS was utilized for the chemical analysis of the ultra-thin TiO_2 films and to determine the thickness of the oxide layer. A native oxide sample and an anodized oxide sample were studied. Survey scans and Ti 2p and In 3d high-resolution spectra are presented in Appendix B. Table 7.2 contains the determined relative concentrations of elements in the studied samples. Table 7.3 lists the relative concentrations of the detected elements in different chemical states, *e.g.* different oxidation states. The different states can be observed based on the different kinetic energies of the emitted photoelectrons.

Table 7.2 *Relative concentrations of elements in the studied oxide samples determined with XPS.*

Sample	Relative concentrations of elements (at. %)						
	C	O	Ti	In	Cu	S	Sn
Anodized oxide	14.24	56.91	25.29	3.10	-	-	0.46
Native oxide	10.66	58.95	24.68	5.71	-	-	-

Table 7.3 *The relative concentrations of elements in different chemical states detected with different binding energies.*

	Relative concentrations of components (at. %)		Component binding energy (eV)	
	Anodized	Native	Anodized	Native
C-C/H	9.59	6.03	285.0	285.0
C-O	2.84	3.25	286.6	286.2
(O-)C=O	1.81	1.38	289.3	289.5
O-M	49.48	50.45	530.7	530.8
O-C/=C	7.42	8.49	532.0	532.2
Ti^{4+}	23.08	21.75	459.0	459.1
$Ti^{2+/3+}$	2.21	2.93	457.7	457.6
In^{3+}	3.10	5.71	445.4	445.5
Sn^{4+}	0.46	-	487.2	-

The XPS signal is acquired also from the underlying ITO substrate, because of the ultra-thin oxide layers. This is the cause for the detected indium and tin concentrations. Carbon contaminants captured from air are detected at the surface of the samples. The most important findings from these results were: no metallic Ti was found in either sample, roughly one tenth of the titanium was at an oxidation state lower than Ti^{4+} and that no impurities (above detection limit) were detected. The native oxide contained relatively more titanium at lower oxidation levels. The oxidation states Ti^{2+} and Ti^{3+} seems to indicate the presence of oxygen vacancies *i.e.* defects in the oxides. Alternatively, suboxides, i.e. TiO_{2-x}, might be present. However, the ratio of the Ti^{2+} and Ti^{3+} states and the depth distribution of the vacancies couldn't be determined.

Inelastic electron energy-loss background analysis was utilized to determine the thickness of the oxide layer on the studied samples. The obtained results are depicted in Appendix C. The thickness of the native oxide was 26 Å and the total oxide thickness for the anodized sample was 34 Å. Assuming identical native oxide formations in the two samples, the anodization leads to a thickness increase of 0.8 nm. Calculating the anodized thickness based on Faraday's law and the current response during the anodization gives this sample a thickness value of 1.1 nm.

The thickness values determined with the two previously mentioned methods differ. The XPS analysis is likely more accurate than the calculations from the electrochemical process. It could be possible that a portion of the anodic current is due to non-faradaic processes or an unaccounted redox reaction e.g. electrolysis of water. In the work of Heljo *et al.* [9], these same methods produced results with better correspondence. In future work it might be better to use e.g. ellipsometry for the oxide thickness measure-

ments. In addition, it could be possible to determine the efficiency factor for the anodization with empirical methods to increase the accuracy of the calculations.

7.3.3 Electrochemical impedance spectroscopy

EIS was used to determine a suitable frequency range where the electrochemical system under study behaves like an RC equivalent circuit. An RC equivalent circuit makes the following Mott-Schottky analysis simpler. A Bode plot and a Nyquist plot are presented in Figure 7.3 for a typical anodized sample.

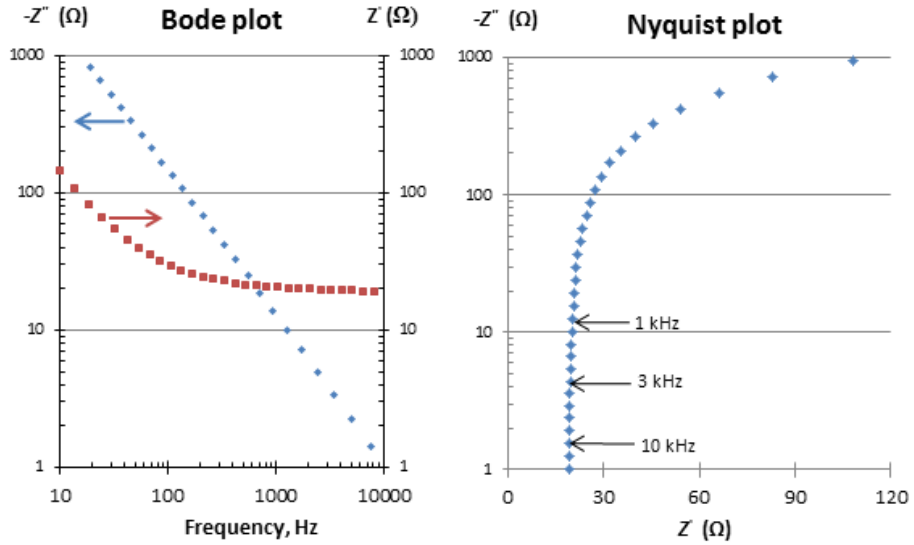

Figure 7.3 *Bode and Nyquist plots constructed for one typical anodized sample. These plots are based on EIS measurements.* Z' *= real part of impedance,* Z'' = imaginary part of impedance.

The Bode plot presents the real and imaginary parts of the impedance versus frequency. The real part of impedance approaches a constant value as frequency increases. The Nyquist plot presents measured imaginary and real parts of the impedance against each other. Each data point on the Nyquist plot represents one measurement frequency. The ideal behavior of an RC equivalent circuit is a vertical line on the Nyquist plot [58], where Z' has no frequency dependency. Figure 7.3 show that the studied electrochemical cell approaches ideal RC behavior as frequency increases.

The Thales software (used with the Zahner Zennium potentiostat) was used to fit an RC equivalent circuit into the measurement data. A picture of the user interface and fitting result is shown in Appendix D. The fitting of the RC series circuit was adequate when a frequency range 2–5 kHz was used. At this frequency range, a resistance of 19 Ω and a capacitance of 9.2 µF were obtained from the fit. Higher frequencies are, in theory, better for the applicability of the equivalent circuit, but could result in measurement errors due to e.g. stray capacitance and reflections with used electrochemical measurement set-

up. A frequency of 3 kHz was chosen for the C-V measurements based on the EIS analysis.

7.3.4 Mott-Schottky analysis

Mott-Schottky analysis was used to determine the defect density of the semiconducting oxide. This method is based on C-V measurements. An RC equivalent circuit was assumed, which meant that the total capacitance of the system could be calculated from the measured imaginary component of the impedance with Equation 5.14. The total capacitance of the system was assumed to be the space charge layer capacitance of the oxide, as mentioned in Section 5.2.3. Figure 7.4 represents the Mott-Schottky plot for the sample of Figure 7.2 for which an anodized layer thickness of 1.5 nm was calculated.

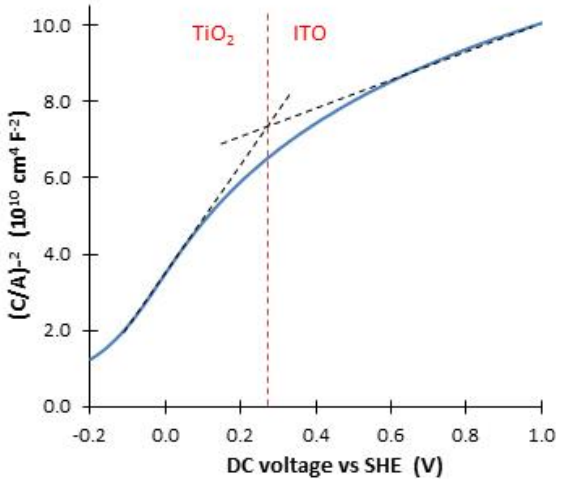

Figure 7.4 *A Mott-Schottky plot for an anodized TiO_2 layer. The space charge layer eventually extends into the ITO as the voltage increases. This causes a change in the slope of the curve. Two ascending linear regions are apparent, which correspond to the n-type semiconductors TiO_2 and ITO.*

The Mott-Schottky plot in Figure 7.4 differs from the ideal plot shown in Figure 5.4 for an n-type semiconductor. Instead of a linear relationship, two separate linear regimes can be observed in Figure 7.4. During the C-V measurement, a space charge region extends from the semiconductor-electrolyte interface towards the semiconductor-electrode interface when the DC voltage bias is increased. The space charge region will, eventually, reach this interface when the semiconductor layer is ultra-thin. Since the ITO substrate/electrode is an n-type semiconductor, the space charge region will then extend into the ITO, if the voltage bias is increased further. Krol *et al.* [56] demonstrated for an anatase TiO_2/ITO system that when the space charge region extends into the ITO the linear slope of the curve is only dependent on the defect density and dielectric constant of the ITO. Therefore, the first linear regime in Figure 7.4 is due to the TiO_2 and the

second one is due to the ITO. The change of the slope in the Mott-Schottky plot occurs at a voltage range and not completely abruptly. This behavior is probably caused by the surface roughness of the substrate and small local differences in the oxide thickness.

This sample (Figure 7.4) had an anodized oxide thickness of 1.5 nm. The native oxide thickness can be assumed to be 2.6 nm, which was measured with the XPS for a similarly prepared sample. The total thickness of the TiO_2 layer was then (with Eq. 5.6) 4.1 nm. Straight lines fitted to the linear regimes of the Mott-Schottky plot intercept at 0.27 V. It will be assumed that at this voltage the space charge region has just extended to the TiO_2/ITO interface. Therefore, the width of the space charge region is W = 4.1 nm. The measured capacitance at this voltage was C_{scr} = 9.412 x10^{-6} F. The dielectric constant of the TiO_2 layer can be calculated based on Equation 5.7 with previously mentioned values:

$$\varepsilon_r = \frac{C_{scr} W}{\varepsilon_0 A} = \frac{9{,}412 \times 10^{-6}\ \mathrm{F} \times 4.1 \times 10^{-9}\mathrm{m}}{8.85419 \times 10^{-12}\ \frac{\mathrm{F}}{\mathrm{m}} \times 2.4 \times 10^{-4}\ \mathrm{m}^2} = 18.159 \quad .$$

The defect density can be calculated from Equation 5.11. The slope of the fitted straight line was S = 1.44089 x10^{11} $F^{-2}cm^4V^{-1}$. The defect density is then:

$$N_D = \frac{2}{\varepsilon_r \varepsilon_0 e} S^{-1} = \frac{2}{18.159 \times 8.85419 \times 10^{-14}\ \frac{\mathrm{F}}{\mathrm{cm}} \times 1.60218 \times 10^{-19}\mathrm{C}} \times \frac{1}{1.44089 \times 10^{11}\ \frac{\mathrm{cm}^4}{\mathrm{F}^2\mathrm{V}}}$$

$$\Leftrightarrow N_D = 5.376 \times 10^{19}\ \frac{1}{\mathrm{cm}^3} \quad .$$

The calculated defect density and dielectric constant, 5 × 10^{19} cm^{-3} and 18 respectively, are similar to the ones determined by Heljo *et al.* [9] (5 × 10^{19} cm^{-3} and 21). Differing values (dielectric constant of 48 and defect density of 2.9 × 10^{17} cm^{-3}) are reported for 40 nm thick (crystalline) anatase TiO_2 prepared via evaporation and annealing steps [56]. However, they also observed that the defect density increased with decreasing oxide film thickness. The dielectric constant is an indicator for crystallinity and the obtained low values are consistent with the fact that anodization leads to amorphous TiO_2 at low cell voltages.

The Mott-Schottky analysis is sometimes regarded as a semi-quantitative method, because of the assumptions made in the theory [47, pp. 8–9]. The studied oxide layers are extremely thin and highly defective, which makes the space charge region capacitance relatively high. Therefore, the capacitance of the electric double layer might not be entirely negligible (as mentioned in Section 5.2.3). However, the electric double layer capacitance was increased in an effort to minimize its effect by using a more concentrated (0.4 M) electrolyte for the C-V measurements. In addition, the uncertainty of the oxide thickness measurement based on calculation with the Faraday's law is another source of

error in the performed Mott-Schottky analysis. The dielectric constant and the defect density calculations require a thickness value. Overall, the calculated defect densities and dielectric constants should be regarded more as rough levels than accurate values. To increase the accuracy of the used method, the oxide thicknesses should be determined accurately e.g. with ellipsometry and the effect of the double layer capacitance should be studied.

7.3.5 Effect of the evaporated titanium layer thickness

Different titanium layer thicknesses (2–4 nm) were evaporated on ITO substrates and were subsequently anodized. The native oxide formation occurred for these samples in the same conditions and duration (48 hours). It will be assumed that the native oxide thickness in all these samples were equal to the measured 2.6 nm (see Section 7.3.2), which was determined for a sample with evaporated 3 nm thickness. Anodic oxidation was carried out identically for the samples, except the V_{max} was changed depending on the Ti layer thickness. Heljo *et al.* [9] showed that during anodization on ITO substrate the breakdown voltage of the anodized layer depends on the Ti thickness. The used V_{max} values were 1.0, 1.8 and 2.0 V, respectively for 2, 3 and 4 nm layers. These voltages were well below the breakdown voltages reported in the previously mentioned work. I-t plots for the anodizations are presented in Figure 7.5(a). Figure 7.5(b) presents the current-time plot for the potentiodynamic anodization of a 4 nm titanium sample with a linearly increasing voltage up to 3.5 V.

As can be seen from Figure 7.5(b), a second anodic current peak occurs when the voltage increases over 2 V. The current begins to increase rapidly around 3 V with increasing voltage. The oxide layer breakdown occurs at this voltage. This increase in current is most likely due to the electrolysis of water. Heljo *et al.* [9] proposed that the oxide layer breakdown on ITO substrate happens via electric-field enhanced pore formation through the oxide and subsequent electrochemical reaction between the ITO and the electrolyte. If this is true, then the observed current peak between 2–3 V could be related to the pore growth, increasing electrolysis and reactions of the ITO. Anodic oxidations for the 4 nm layers were, hence, only carried out with V_{max} = 2.0 V. As a result, these thicker titanium layers were not necessarily completely oxidized. However, the bluish color of the evaporated Ti layer was completely gone from the anodized area.

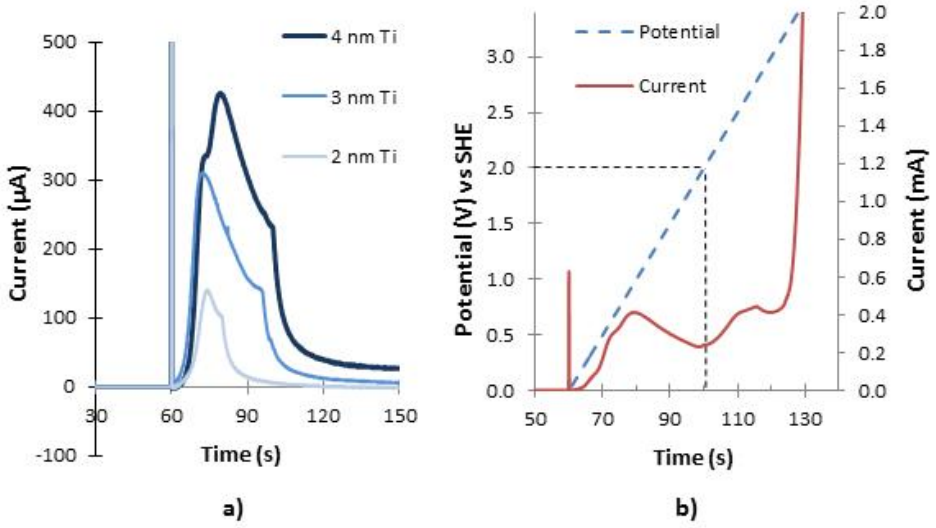

Figure 7.5 *a) current-time plots for Ti/ITO samples with different evaporated titanium layer thicknesses (2–4 nm). b) Potentiodynamic anodization for 4 nm thick titanium layer on ITO. Layer breakdown occurs near 3 V.*

Figure 7.5(a) shows a clear difference in the anodization of the different layers. The curves are similar in shape, but the transferred charge (*i.e.* area) increases with thickness as expected. The slope of the onset is nearly identical due to the similar kinetics of the anodization. The decrease in the current begins sooner for thinner layers. In addition, a significantly higher current is observed for the 4 nm layer during the constant voltage phase (t > 100 s), likely because of increased electrolysis due to higher voltage. The shape of the curves and the curve area were very reproducible.

The transferred charge was 0.001290 C and 0.010174 C for the evaporated 2 nm and 4 nm layers, respectively. Calculating the anodized thickness as in Section 7.3.1 gives thickness values 0.3 nm and 2.3 nm. Therefore, the evaporated titanium layer thicknesses of 2 and 4 nm give total oxide thicknesses of 2.9 and 4.9 nm. These values likely include significant error as described in previous sections. However, it can be clearly seen based on the anodization behavior that the oxide layers differ in thickness. Based on the molar masses and densities (3.8 and 4.5 g/cm^3 respectively for Ti and TiO_2), 1 nm of Ti should oxidize into 2 nm of TiO_2. In this work this ratio was significantly smaller. One possibility for this could be the dissolution of the oxide during the electrochemical processes. However, the dissolution of TiO_2 in H_2SO_4 solutions has been shown to be very slow [47, p. 4]. The previously proposed error in the evaporated layer thickness measurements is a reasonable explanation. Therefore, there could be a systematic error in the evaporated layer thickness values. It was also assumed that the native oxide thickness was even in all the samples, which might not be true.

7.4 Devices with anodized TiO_2 layers

I-V measurements were performed for the fabricated devices. The measurements were made at RT with the devices exposed to room air. The measured current values were divided with the effective diode area to obtain current density values. The area of the fabricated vertical diodes was measured from photomicrographs (shown in Appendix E). The average area was 0.89 mm^2. Devices were fabricated from anodized samples with evaporated titanium layers of 2, 3 and 4 nm.

7.4.1 Initial I-V measurements

Figure 7.6 presents the I-V plots for devices where the evaporated titanium layers were 3 nm thick. These devices are structurally similar to the ones presented by Heljo *et al.* [9]. Measurements were made from -20 V to 0 V with a sweep rate 300 mV/s.

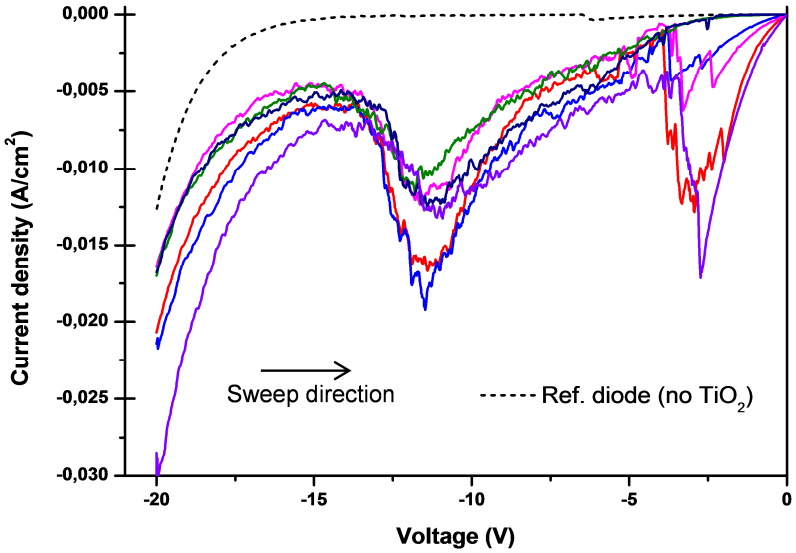

Figure 7.6 *I-V characteristics of the fabricated diodes where the evaporated titanium layers were 3 nm thick. Dotted line represents the characteristics of a fabricated diode without the TiO_2 barrier layer.*

Two different kinds of NDR peaks were observed: A reproducible NDR at -12 V…-14 V range and more arbitrary NDR peaks near -3 V. However, the peaks near -3 V were not observed for all diodes whether a diode showed any NDR or not. In the work of Heljo *et al.* [9], NDR was observed only for voltages from -12 V to -15 V.

NDR didn't occur for all measured diodes and the yield was relatively poor. However, in a working sample nearly all the devices operated with observable NDR. The reason why some devices, and sometimes the entire device set of a sample, failed to work is likely due to the fabrication process, which is not entirely optimal for the devices. The devices are highly sensitive to any kind of scratches and to dust particles as well. One

cause for failure for these devices is thought to be pinholes in the TiO_2 barrier layer. Since the anodized layers are ultra-thin, pinholes and pores are possible.

The measured NDR devices had a significant variation in their valley current densities and peak current densities with observed ranges of 0.0045–0.0069 A/cm^2 and 0.0113–0.0192 A/cm^2, respectively. The variation in the results might be due to small variations in the oxide barrier thickness for each device. The RMS surface roughness of these ITO/glass substrates has been measured to be 6.9 nm [9]. The highest observed PVCR was 3.3, which can be calculated with Eq. 2.5:

$$PVCR = \frac{J_p}{J_v} = \frac{0.0192\ \frac{A}{cm^2}}{0.0059\ \frac{A}{cm^2}} = 3.254 \quad .$$

The observed PVCR was typically in the range from 2 to 3. PVCR up to 3.6 was reported by Heljo *et al.* [9] for similar devices.

However, the observed NDR was not stable in these devices in the measurement environment: room temperature and air atmosphere. After the Al top electrode was evaporated, it didn't matter for the measurements how long the samples were kept inside the evaporator under vacuum. The observed NDR was diminished and eventually lost in devices that were exposed to the measurement environment. The device I-V characteristic began to resemble the characteristic of a reference device. This happened within 1–2 hours. The exact reason is unknown, but could be related to the oxidation of the Al-Superyellow interface, which might affect the injection of holes from the electrode. Longer measurements couldn't be made for the devices due to the unstable nature of the devices in the measurement environment. In addition, this was problematic for the reproducibility of the measurements. Only devices measured relatively quickly after the start of the air exposure are presented in this work.

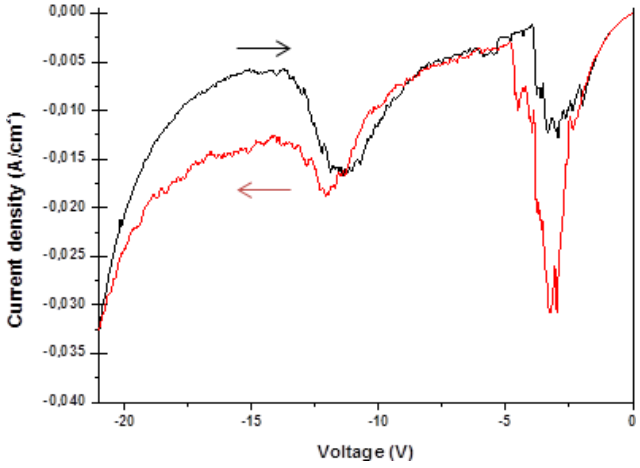

Figure 7.7 *Typical hysteresis observed for the devices. Arrows indicate the sweep direction of the measurement.*

The devices showed high hysteresis with the current density changing based on the sweep direction of the measurement. A typical observed hysteresis is presented in Figure 7.7 for a single device. It was also noticed that the NDR peaks near -3 V were generally stronger and occurred more frequently when the sweep direction was from 0 V to -20 V. High hysteresis was reported by Heljo *et al.* [9] for similar devices.

7.4.2 Effect of the oxide thickness

The effect of the oxide layer thickness on the device behavior was studied. Different titanium oxide layers were fabricated by evaporating titanium layer thicknesses of 2, 3 and 4 nm, which were subsequently anodized. Different titanium oxide thicknesses were clearly reached based on the anodization results presented in Section 7.3.5. The current-voltage characteristics of the devices are presented in Figure 7.8.

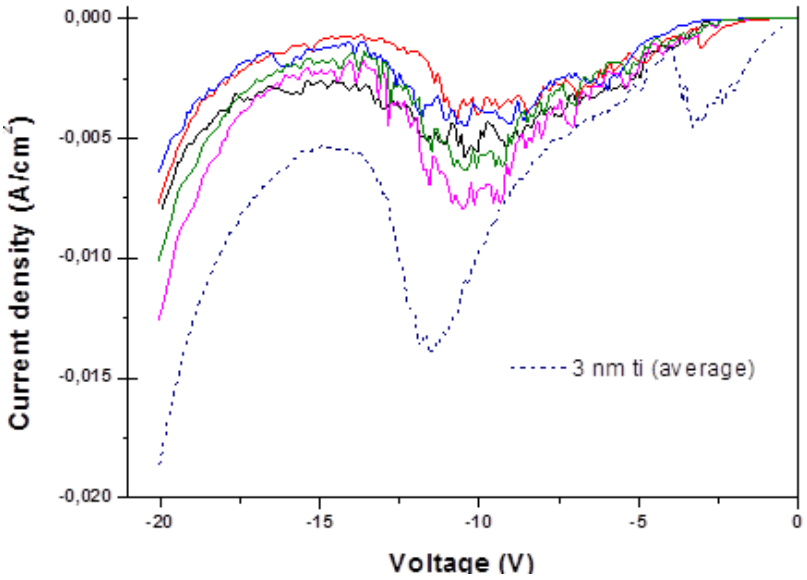

Figure 7.8 *Current-voltage curves for devices with an evaporated 2 nm titanium layer (solid lines). Dashed line represents the average behavior of five (working) devices with evaporated 3 nm thick titanium layers.*

The devices with the evaporated 4 nm titanium layers didn't show clear NDR at voltage range -12…-14 V. They showed arbitrary NDR peaks around -3 V, otherwise the behavior resembled the reference devices under reverse bias. Devices with the evaporated 2 nm Ti layers showed a NDR behavior similar to the devices presented in Section 7.4.1. The observed currents were lower for the devices with thinner oxide, but PVCR was 2–3 for these devices as well. The operating principle of these devices remains uncertain. Yoon *et al.* [7] proposed a defect assisted tunneling process as the explanation for quite similar NDR devices. The devices studied in this work contain a high amount of defects, which could be suitable for the mentioned process. However, the oxide thickness didn't change the NDR behavior considerably.

The observed NDR might be due to other processes such as resistive switching, where the resistance of a material/system changes based on the applied voltage. Resistive switching is a highly researched phenomenon used in organic non-volatile memory devices [67]. There are many known causes for resistive switching such as formation and rupture of conductive filaments, ionic migration and charge trapping. TiO_2 is well known to exhibit resistive switching properties in some device structures. The switching in TiO_2 devices is often explained by the formation of conductive filaments [67]. In addition, switching is reported in literature for devices with aluminum electrode/s. In these devices, the switching can happen due to filamentary conduction caused by the native aluminum oxide layer typically found on the surface of an aluminum electrode [68]. However, the reference devices studied in this work showed no NDR behavior, which means that the observed NDR is caused by the TiO_2 layer rather than the aluminum oxide alone. NDR peaks have been interpreted as dynamic programming of the device between a high conductivity state and a low conductivity state [69]. If the studied NDR devices operate with a resistive switching instead of a tunneling mechanism, these devices should be able to store conductivity states and could act as nonvolatile memory devices.

The NDR mechanism of these devices needs to be studied further to be able to optimize the devices. One concern is the instability of the devices in air atmosphere. This problem could be potentially solved by changing the top electrode material and/or semiconductor. Another possibility is to encapsulate the devices to prevent air exposure. The use of different electrodes and organic semiconductors might also be vital to understand the device operation mechanism.

7.5 ALD of TiO_2 and devices

The ALD grown TiO_2 layers were analyzed with XPS based on high-resolution spectra similarly to the anodized sample. The relative concentrations of elements for the studied samples are presented in Table 7.4 for different deposition temperatures. Some of the samples were masked with Kapton tape in order to retain ITO contacts in the samples for electrical measurements.

As can be seen from the table, the samples masked with the Kapton tape contained a great amount of Si impurities. It was also determined that the oxide samples had roughly one tenth of the titanium at lower oxidation states than 4+, similar to the anodized samples. The layer thickness was determined with inelastic electron energy-loss background analysis similarly to the anodized sample. It was found out that the aimed 4.5 nm thickness was reached with the unmasked sample. Using the same amount of cycles and the same process for the masked samples only resulted in a thickness of ~2 nm at temperatures 100°C and 150°C. At 200ºC, barely any oxide was deposited as can be seen from the very small titanium concentration in Table 7.4. The most probable cause for this behavior is outgassing of compounds from the Kapton tape. The Kapton tape

used had a silicone adhesive layer that was the likely source for the Si impurities. In theory, the outgassing should increase with temperature, which would explain the temperature behavior of the depositions.

Table 7.4 Relative concentrations of elements in the studied ALD grown oxide samples determined with XPS using components of C 1s, O 1s, Ti 2p, In 3d, S 2p, Sn 3d, N 1s and Si 2s spectra.

Sample	Relative concentrations of elements (at. %)							
	C	O	Ti	In	S	Sn	N	Si
200°C, unmasked	24.73	48.26	21.03	4.89	-	1.08	-	-
100°C, masked	28.24	42.11	12.77	9.38	-	1.64	0.82	5.04
150°C, masked	21.67	47.98	12.24	10.11	-	1.96	-	6.05
200°C, masked	23.36	44.01	4.12	17.35	-	2.95	-	8.22

Therefore, to obtain high quality oxide layers the samples should be masked with another method. A stainless steel mask was fabricated for this purpose, but unfortunately wasn't used in this work due to time constraints. However, these initial ALD grown TiO_2 layers with high impurities showed promising NDR behavior when fabricated for devices with the previously mentioned process.

The Mott-Schottky analysis wasn't successful for the ALD grown oxide layers. The measured oxide layers were probably too thin and had a too small defect density. In this case the C-V measurement could be too insensitive.

7.5.1 I-V characteristics

I-V curves were recorded for the devices, with the ALD grown TiO_2 layers. The samples with the 200ºC deposition temperature were not fabricated for diodes nor measured. I-V measurements were carried out similarly to the anodized samples, while the devices were exposed to air. Figure 7.9 presents a compilation of several measured I-V plots for these devices. These devices seemed sensitive to air exposure, similarly to the anodized samples. A typical hysteresis behavior observed for these devices is depicted in Figure 7.10.

These diodes showed surprisingly strong NDR behavior. The NDR occurred at a voltage range from -12 V to -15 V, a similar range was observed for the anodized samples presented in this work and in the work of Heljo *et al.* [9]. Some diodes, but not all, showed similar current peaks near -3 V than the diodes presented previously in this work. The cause of this behavior might be the same as in those diodes, i.e. the peaks

could be caused by tunneling or resistive switching. The observed hysteresis for the devices (Fig. 7.10) is similar to the previously presented devices.

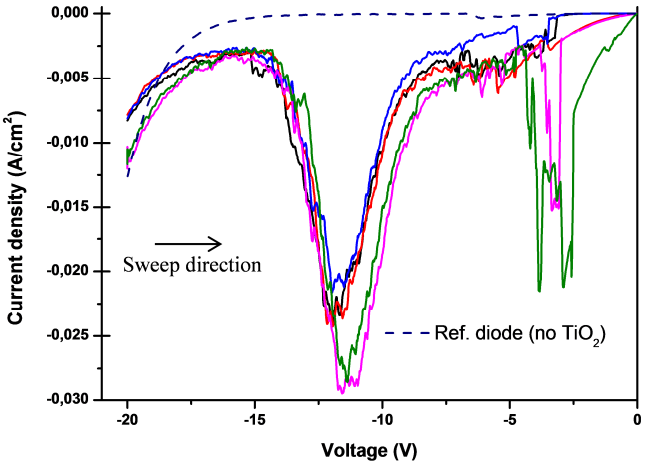

Figure 7.9 *A compilation of measured I-V curves for the fabricated diodes with ALD grown TiO_2 layers. These diodes had a similar vertical structure as the previously presented diodes with anodized TiO_2 layers, except the oxide thickness was ~2 nm opposite to ~4 nm.*

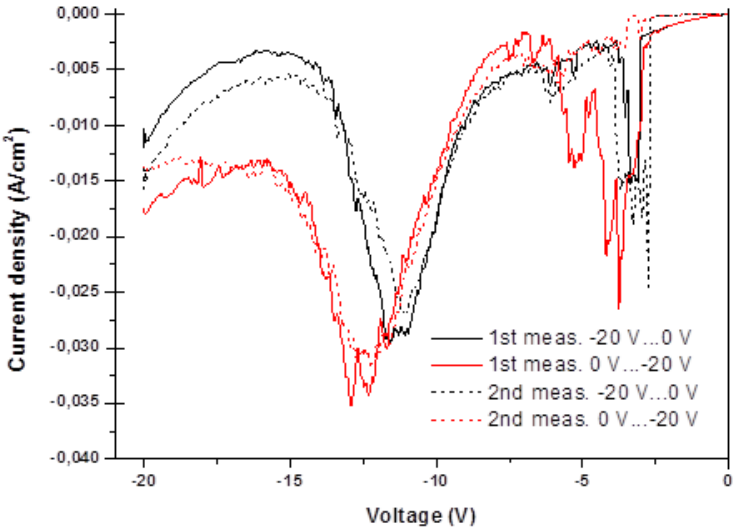

Figure 7.10 *Two consecutive I-V measurements for the same device (ALD grown oxide) with voltage sweeps to both directions. Strong hysteresis is observed for the devices. The second measurement (dotted lines) gives nearly identical I-V curve compared to the first measurement, except for the ``arbitrary´´ current peaks observed around -4 V.*

A typical valley current density for these devices was ~0.004 A/cm^2. The highest observed peak current density was 0.029 A/cm^2, corresponding to a PVCR of 7. The observed PVCR is twice as large as the ones observed for the anodized samples. However, direct comparisons are not meaningful since there is a large difference in the interfacial oxide layer thicknesses. In addition, since the exact mechanism of the NDR behavior in

these NDR devices is not known, it can’t be said that the NDR is caused by the same phenomenon in the different devices. The Si impurities might have a role in the observed NDR. The Si atoms could act as doping atoms for the titanium oxide.

Due to the promising initial results, ALD is a method that should be studied more for the fabrication of the interfacial oxide layers. ALD offers straightforward means to control the oxide layer thickness accurately which is a bit problematic for the anodic oxidation with ultra-thin layers. In addition, the devices with the ALD grown oxide layers had far better yield than the devices where the oxide was anodized. This is probably due to the pinhole-free film deposition of ALD.

8. SUMMARY

This work is part of a larger ongoing research project focused on organic tunnel diodes. An ultra-thin TiO_2 interfacial layer is an integral part for the studied devices. The aim of the research is to study these devices and develop a high-throughput fabrication process for them. The main objective of this thesis was to fabricate ultra-thin TiO_2 interfacial oxide layers on rigid ITO substrates for the organic tunnel diode devices with two promising methods: anodic oxidation and atomic layer deposition. Anodic oxidation has already been utilized in the project, but in this work the method was used to fabricate different oxide thicknesses for the devices.

The anodic oxidation proved to have a good reproducibility for the fabrication of the oxide layers. The TiO_2 layers were oxidized from evaporated titanium layers. The final thickness of the oxide can be controlled with the evaporated layer thickness. Accurate measurement and control of the evaporated layer is the key. The measured thickness values for the oxide layers based on XPS measurements and calculations from Faraday's law didn't correspond completely. The larger value obtained from the electrochemical calculations likely contains significant error due to the unaccounted electrolysis of water. However, oxide layers with clearly different thicknesses, based on the anodization behavior, were successfully fabricated. To improve the oxide thickness control, the effect of the water electrolysis could be accounted with empirical study. In addition, another thickness measurement method would be useful e.g. ellipsometry.

Mott-Schottky analysis was used to determine the dielectric constants and defect densities of the fabricated oxide layers. The analysis was carried out based on capacitance-voltage measurements in an electrochemical cell. The applicability of the method was confirmed with electrochemical impedance spectroscopy. A dielectric constant of 18 and a defect density of 5×10^{19} cm^{-3} were measured for a typical oxide layer with some deviation in the results. These values correspond well to other reported values and indicate the amorphous and highly defective nature of the anodized films. The Mott-Schottky analysis is considered a semi-quantitative method. To increase the accuracy of the method, the influence of the double layer capacitance should be studied and accounted.

XPS measurements confirmed the chemical composition of a typical anodized oxide film as TiO_2. No metallic titanium was detected from the XPS sampling depth, *i.e.* the layer was fully oxidized. One tenth of the titanium was at a lower oxidation level than +4, which might indicate the presence of either oxygen vacancies or suboxides. No significant impurities were detected.

The atomic layer deposition of the ultra-thin TiO_2 layers was outsourced. Titanium dioxide layers were successfully grown on ITO with ALD at temperatures 100, 150 and 200°C. ALD offers a more accurate and straightforward control of the oxide thickness compared to the anodic oxidation. In general, ALD produces thin films with low defect densities. The TiO_2 layers need to be patterned on the ITO substrates to use them in the device fabrication process. The wet etching process used for the anodized samples was not successful for the ALD grown films. The deposition of the oxide layers with ALD using Kapton tape as a sort of patterning mask was not entirely successful. A lower oxide thickness was reached than what was aimed for. In addition, the layers had high silicon impurity contents. The most likely reason for these problems was the outgassing of compounds from the Kapton tape. Mott-Schottky analysis was not successful for these oxide layers probably due to too thin oxide thickness. Future work with the atomic layer deposition should be carried out with *e.g.* a stainless steel mask assembly to ensure correct growth pattern is obtained with no outgassing and impurities.

Vertical diode structures were fabricated on top of the TiO_2/ITO samples. Photolithography and wet etching was successfully utilized to obtain a patterned structure for the anodized samples. An organic semiconductor, PDY-132 ``Superyellow´´, was spin coated onto the samples. An average thickness of 34 nm was reached for the OSC layer with little deviation. The layer thickness was measured with an optical profilometer utilizing phase-shifting interferometry. The device fabrication was completed with an e-beam evaporation of a 200 nm thick aluminum top-electrode. Devices with a vertical structure of ITO/TiO_2/PDY-132/Al were fabricated. The devices had a well specified effective area of 0.89 mm^2 on average, based on measurements from photomicrographs.

The fabricated devices were characterized with current-voltage measurements. Measurements were carried out in the reverse bias (ITO negative) range of -20…0 V at room temperature and air atmosphere. The devices with the anodized TiO_2 interfacial layers showed two separate NDR peaks while reverse biased. A reproducible NDR occurred near -13 V and an arbitrary NDR peak was sometimes observed near -3 V. The cause of the NDR behavior is still unknown. Defect assisted tunneling and resistive switching phenomena are being considered. A PVCR up to 3.2 was observed for the anodized samples. Fabricated reference samples without the TiO_2 showed no NDR behavior, which indicates that the TiO_2 is integral for the NDR. The different anodized oxide layer thicknesses gave some differing results. Nominally 2 nm and 3 nm thick evaporated Ti layers gave the above mentioned NDR behavior. No significant PVCR or I-V behavior difference was observed between them. However, samples with nominally 4 nm thick evaporated layers didn't show clear and reproducible NDR. This could be caused by the incomplete oxidation of the titanium. Another reason could be that the oxide acts as a too wide barrier, in this case. The devices with the ALD grown oxide layers (nominally 2 nm thick) showed similar NDR behavior to the above mentioned, except the NDR was stronger. PVCR up to 7 were recorded for these devices. It is unclear what the

cause of the stronger NDR behavior is. The high silicon impurity content could be related.

All of the studied NDR devices were unstable in the measurement environment (air, room temperature). The NDR behavior was lost in a couple of hours upon exposing the devices for the environment after the evaporation of the Al top-electrode. The exact reason is unknown, but is thought to be the oxidation of the aluminum electrode at the OSC/aluminum interface. In future work, different top electrodes should be experimented with. Device fabrication and characterization could be carried out in an inert `glovebox´ in order to run longer measurements. Encapsulation is potential solution for the air instability.

The anodic oxidation and ALD seem promising as fabrication methods for ultra-thin titanium dioxide interfacial films. Both of these methods are suitable for low temperature and high-throughput fabrication. These processes should be suitable for flexible substrates too. Room temperature NDR with PVCR > 3 were observed for devices, which is enough for specific logic circuit applications. However, some problems exist with the devices including air instability of the device and operating reliability. In addition, the operation principle of these NDR devices remains uncertain.

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APPENDIX A: PROFILOMETER MEASUREMENTS

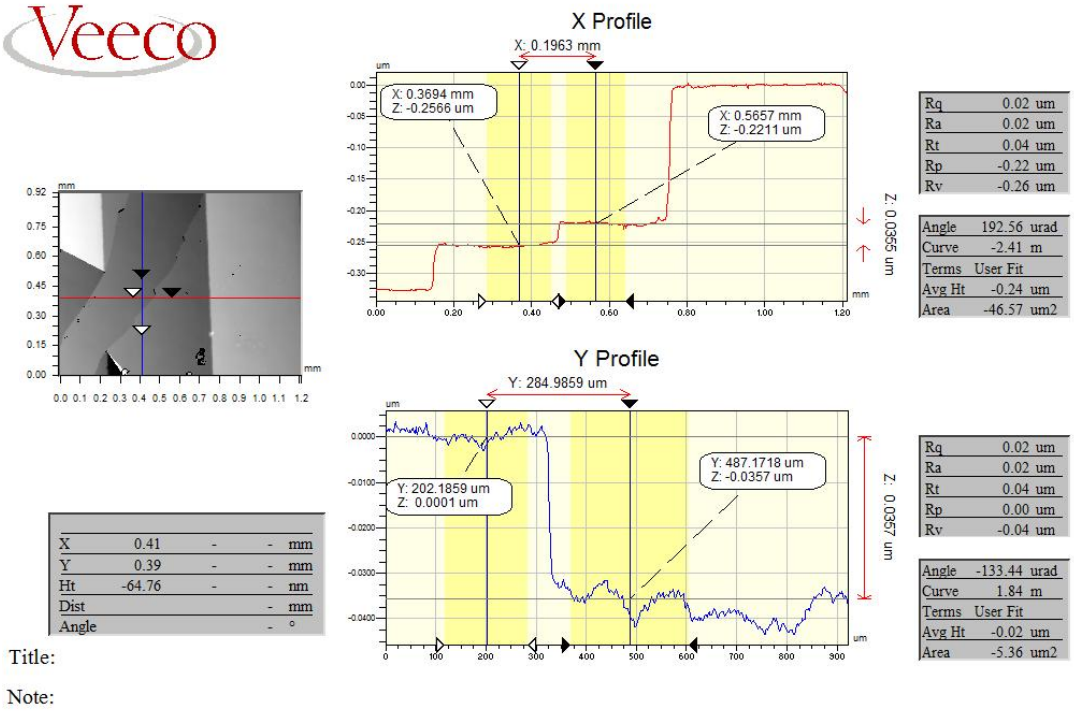

Figure A.1 *User interface of the Vision measurement software for the optical profilometer. One thickness measurement is presented in two dimensions.*

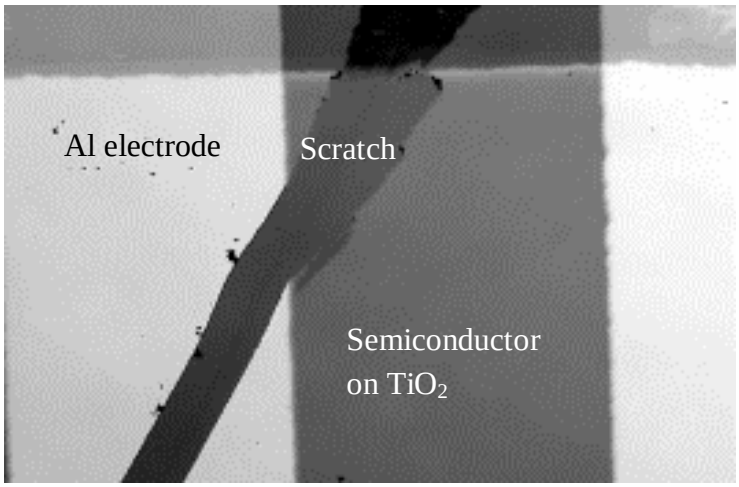

Figure A.2 *The height map generated with the optical profilometer for one measurement site on a sample. Semiconductor thickness can be measured from the height step at the scratch edge.*

APPENDIX B: XPS SPECTRA

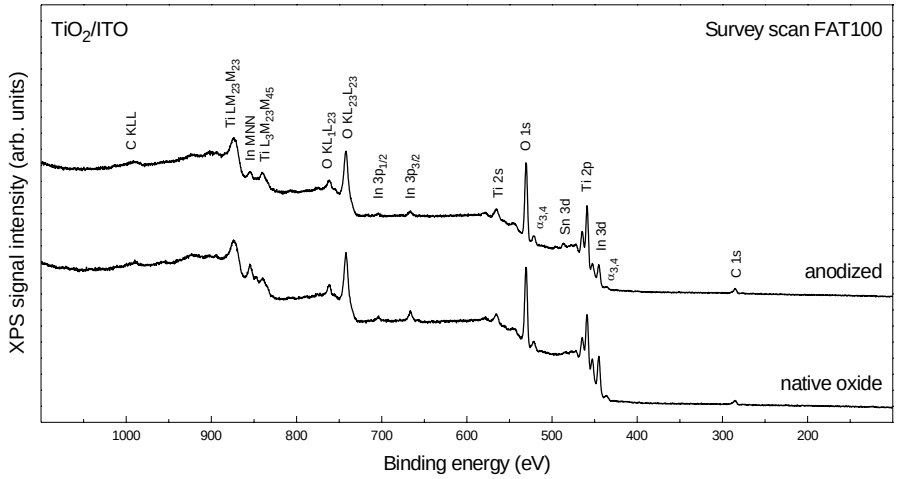

Figure B.1 *XPS Survey scan spectra for the studied samples (anodized and native oxide).*

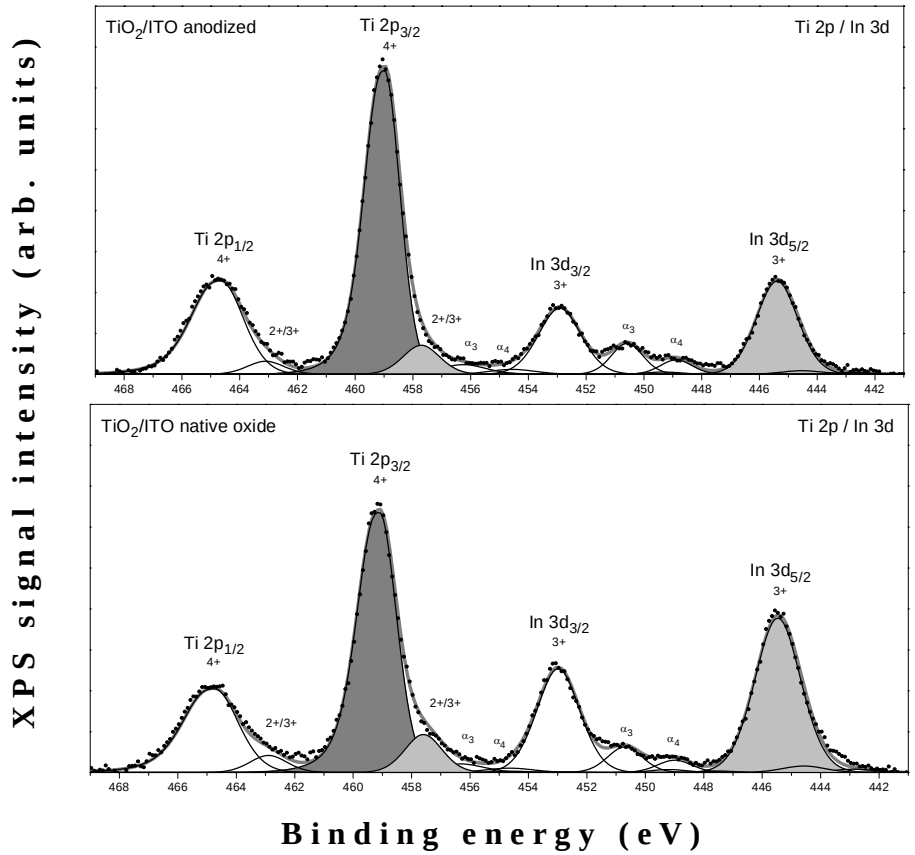

Figure B.2 *XPS Ti 2p and In 3d high-resolution spectra for the studied samples.*

APPENDIX C: INELASTIC ELECTRON ENERGY-LOSS BACKGROUND ANALYSIS

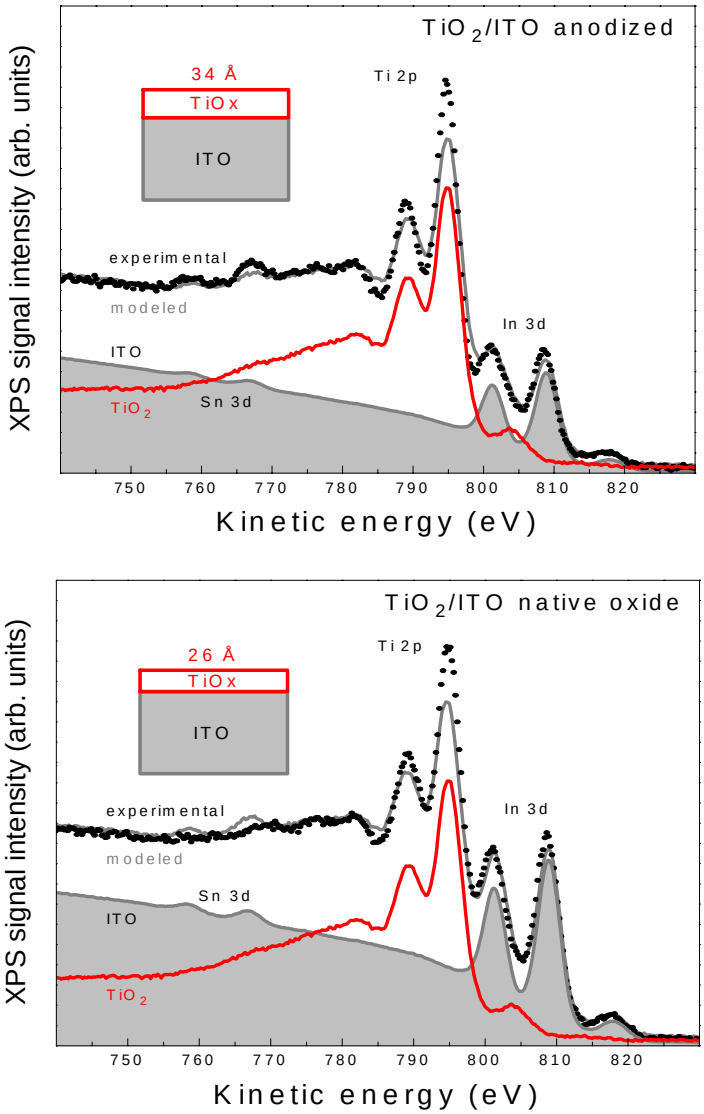

Figure C.1 *The oxide layer thickness for the studied anodized and native oxide samples determined with inelastic electron energy-loss background analysis. The In 3d signal (808.5 eV) from the ITO substrate diminishes exponentially with increasing TiOx over-layer thickness. With this method, the correct morphology (thickness) of the oxide is acquired when the modeled spectrum overlaps with the experimental spectrum (studied sample). The modeled spectrum is a combination of the measured pure TiO_2 and ITO reference spectra, whose intensity has been recalculated to overlap the experimental spectrum (i.e. modeled thickness matches the thickness of the sample).*

APPENDIX D: EIS DATA

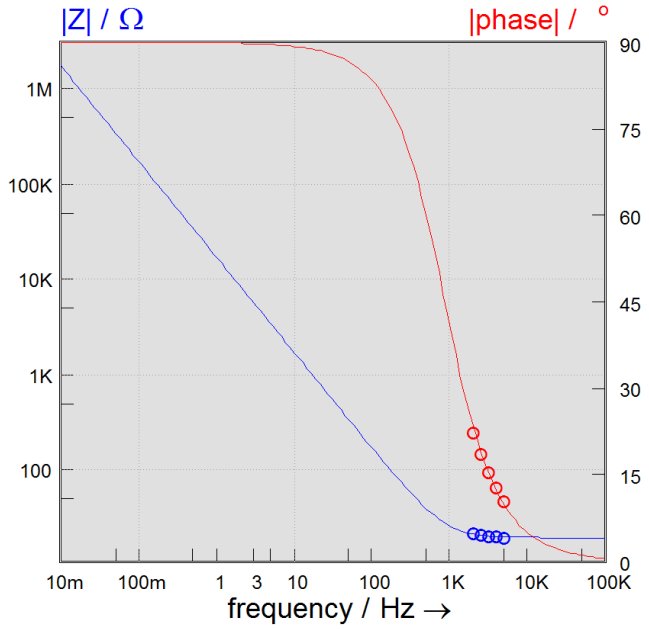

Figure D.1 *EIS experiment data fitted in the frequency range 2–5 kHz with an RC series equivalent circuit. Fitting is performed with the Thales software using ``complex non-linear regression least squares fitting´´ method. Circles represent fitted data points.*

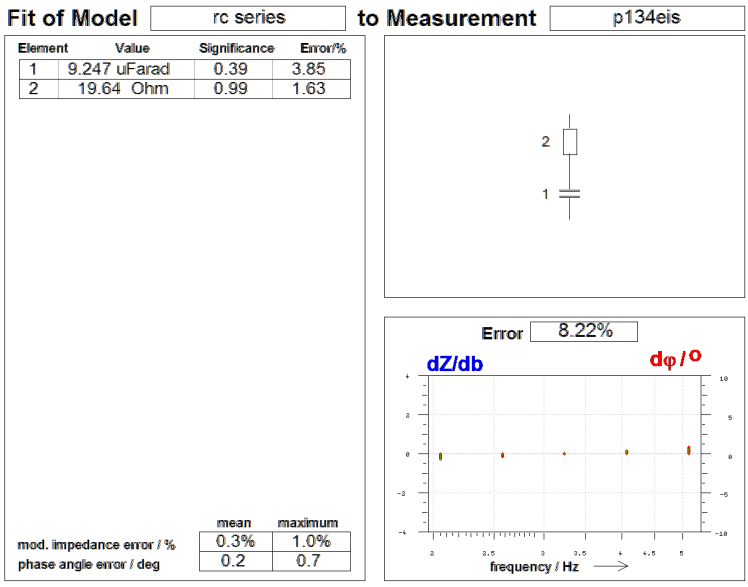

Figure D.2 *The fitter window of the Thales software shows the equivalent circuit used, the parameters of the fitted circuit and the errors. Final quality of the fit is obtained from the error statistics box at lower-left corner.*

APPENDIX E: DIODE PHOTOMICROGRAPHS

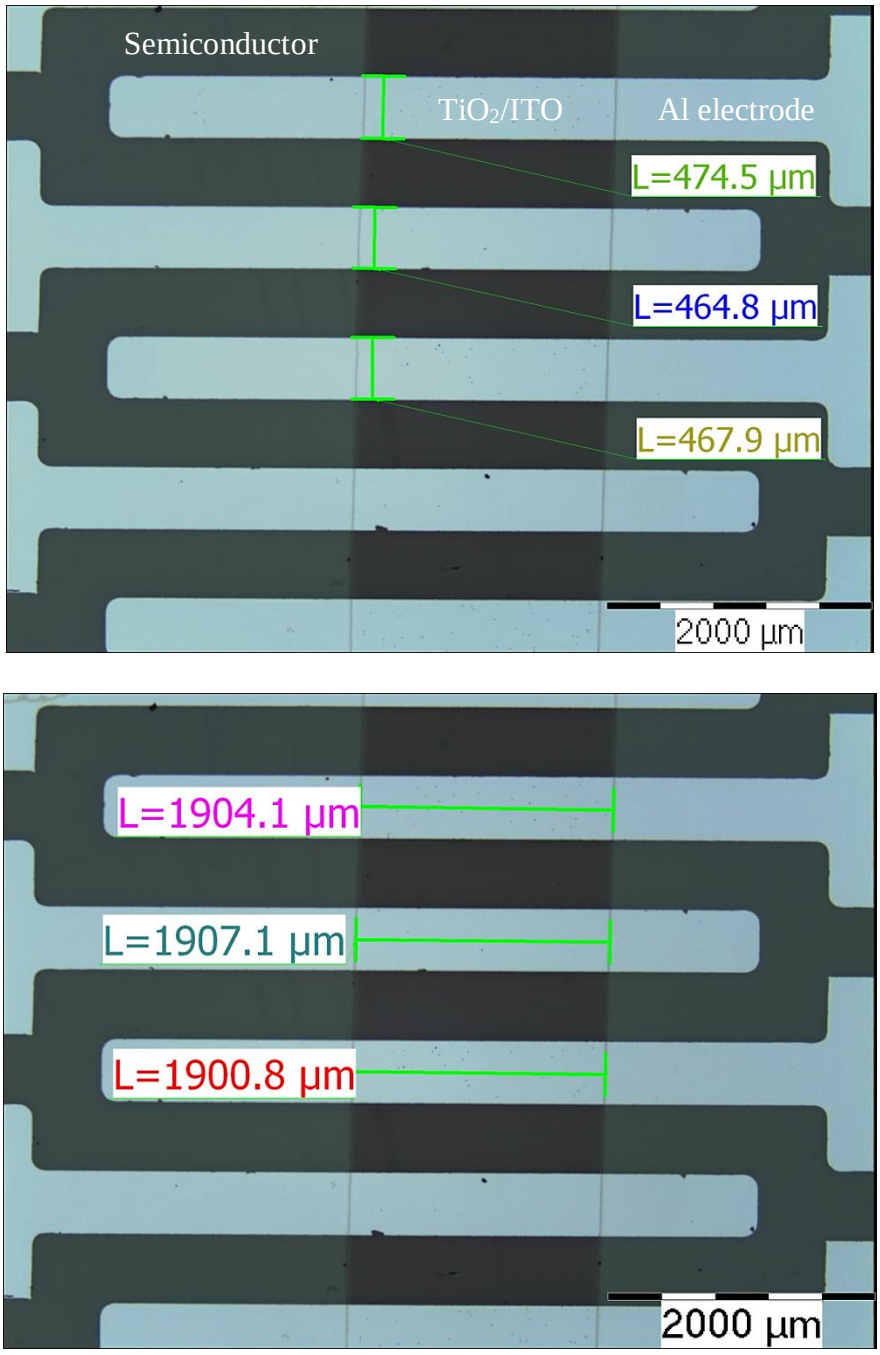

Figure D.1 *Photomicrographs of the fabricated vertical diode structures taken with Olympus BX51 optical microscope. The measured dimensions define the effective area of the diode.*