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48V Super Cap Power Management Unit
Kabir Md.Khyrul
Master's Thesis

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Examiner and topic approved by the
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PREFACE

This Thesis paper was done under RF Integrated Circuits Laboratory (RFIC), Tampere University of Technology (TUT). I would like to thank everybody from the RFIC group to help me to complete my thesis. I would like to give special thanks to Professor Nikolay T. Tchamov, for his guidance and the opportunity he gave me to conduct research to finish my thesis successfully in RFCC laboratory. I want to also mention the name of Jani J… for his kind support.

I would like to thank my family and friends who gave me the great encourage and motivation to complete this thesis.

ABSTRACT

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Power management unit is one of the major parts in energy storage sector. Dynamic power management unit is comprised of multiple super capacitor cell connected in series. Desired output voltage mainly depends on performance and energy production ability of the capacitor pack. Adaptive power management unit is responsible to observe and control the capacitor pack in real time. Life cycle length of the capacitor also depends on the performance and working principles of the PMU. Another key issue of the performance is safety of the capacitor pack as well as the whole system. Due to the fast charging and discharging rate of the rechargeable super capacitor is more compatible than other battery technologies to design PMU. Here 48V PMU is designed with 24 super capacitors pack for wide range of power supply. To increase efficiency of the PMU, proper balancing is done by internal balancing technique of MAX11068 interface board.

The main target of thesis is to achieve 48V output voltage and monitor the voltages & state of charge (SoC) of the capacitor pack. Here 24 super capacitors are connected in series to get 48V output voltage. To monitor/regulate the output voltage, MAX11068 battery pack monitoring board is used. PMU monitors the voltages and SoC of the whole capacitor pack and individual capacitor cell .With the help of java programming and MAX1168 board, voltage and SoC of the capacitor pack is observed. A user friendly graphical user interface also used to show all measurement result at real time. From the result window user can easily get the idea of the capacitor performance and how to control the system. This thesis is a versatile smart power management system, some of the idea can use in future thorough research project. Two Arduino microcontrollers helps to better control on grounds problem and MAX11068 board.

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ABBREVIATIONS

ADC	Analog Digital Converter
BMS	Battery Manaegment System
PMU	Power Management Unit
GUI	Geraphical User Interface
I^2C	Inter Integrated Circuit
SoC	State Of Charge
SoH	State Of Health
CCCV	Constant current constant voltage
SDA	Serial data line
SCL	Serial clock
PFM	Pulse Width Modulation
OCV	Open Circuit Voltage

1. INTRODUCTION

Numerous energy storage technologies have been already available in the market to improve the power quality of electrical power and energy systems. Super Capacitor has developed incomparably over the last decade and come up with the potential to facilitate major change in energy storage .Super Capacitor is utilized as short term energy source to meet dynamic performance of any electronic vehicle system while battery is used as midterm energy storage. Quick energy delivery is possible from capacitor and can be recharged in minutes or even seconds. Capacitor is also able to eliminate the problem of temperature variations, shocks and vibrations. Capacitor has limited energy storage capacity and the best version of capacitor energy system is ultra-capacitor. Super capacitor PMU is applicable for electric vehicle, GPS, automated system also compatible as auxiliary power sources that complement main energy sources such as secondary batteries and fuel cells.

In this thesis we explore on revolution of energy storage system for super capacitors in comparison with battery management system. This PMU is designed in both hardware and software way. A User friendly GUI is made to verify the measurements from software infrastructure. Measurement results from GUI prove that PMU achieves all function and the results are accurate. Our aim is to design a PMU which is accurate & safe and also able to provide 48V output voltage with all performance statistics including individual voltage & SoC, total voltage & SoC of the capacitor pack in different charging and discharging condition. In chapter 2 we explained the background study of ordinary capacitor and Super capacitor. Chapter 3 deals with power management unit for super capacitors which includes balancing and comparison with other BMS system. Chapter 3 also demonstrate the design target and function of PMU. In the chapter 4 we narrated about MAX1168 battery pack monitoring board which has important roles in this whole system and comparison between MAXIM and LTC interface board. In chapter 5 we showed the detail structure of software infrastructure and how the measurement data incorporate with it. We used java programming to build a GUI. In chapter 6 we discussed about the system architecture and measurement. Here we also explained about the result and discussion about the result. Accuracy of the result is checked by comparing the result with the measurement result from multimeter in this chapter. Finally, discussion section gives an idea about prospective research on BMS. This PMU can be turned into bigger power management unit which is explained elaborately in the discussion chapter. This PMU is designed to use for electric vehicles as parallel power management unit with other battery management system.

2. THEORETICAL BACKGROUND

2.1. Capacitance and Charge

Conventional capacitors comprise of two parallel conducting plates and they are detached by insulating dielectric material. When the voltage applied to these plates an electrical current flows charging up one plate with a positive charge with respect to the supply voltage and the other plate with an equal and opposite negative charge. The charges are isolated from each other plates by a dielectric metal thus producing electric field and energy stored to the capacitor.

Capacitor also has the ability to store charge Q (units in coulomb) of electrons. A potential difference is form up when the capacitor is fully charged up. Capacitance and amount of stored energy depends on few factor such as the smaller distance difference between the plates, area of the plates.

The electrical charges (Q) storage potentiality between the plates is proportional the applied voltage. Capacitor capacitance defines as Farads. Capacitance always positive and can't be negative. Ability of storing charge to capacitor controlled by amount of applied voltage [1].

Charge on a Capacitor

$$Q = C \times V$$

Where,

Q= Charge in Coulombs.
C= Capacitance in Farads.
V= Voltage in Volts.

Capacitance is can be defined as the ratio between accumulated positive charge Q and the voltage V applied,

$$C = \frac{Q}{V}$$

Generally C directly proportional to the surface area A of the each plates and inversely proportional to the distance D between the plates.

$$C = \varepsilon_r \varepsilon_0 \frac{A}{D}$$

Proportionality constant

ε_0= Dielectric constant or Permittivity of free space
ε_r= Dielectric constant of insulating material between the plates

2.2. Types of Capacitor

Capacitor mainly two types polarized and non-polarized. Polarized capacitor has higher value (1uF+) than non-polarized capacitors (up to 1uF). Electrolytic and Tantalum capacitors are polarized type. In inverting voltage condition polarized capacitor has higher leakage current. Polarized capacitor used in DC application and Non-polarized capacitor used in AC application.

There are also different types of capacitor

Dielectric Capacitor

For transmitters, receivers and transistor radios require a continuous variance capacitance which is provided by dielectric capacitor. The maximum capacitance value depends on moving position of rotating plates and fixed plates. Range of break down voltage can be regulated by large spacing or air gaps between the plates [1].

Ceramic Capacitor

For high frequency RF, audio circuit ceramic capacitor is the best choice for high frequency compensation. Relatively low cost, better control and wide range of temperature coefficients, lower impedance and good high frequency characteristics. Made by two sides coating of a small porcelain or silvered ceramic disc and then combined together to make a capacitor. Another name is disc capacitor. By changing the thickness of the used ceramic disc we can change the capacitance value. It has lower tolerance level [3].

Electrolytic Capacitor

Higher capacitance value application system used electrolytic capacitor. Here capacitance value raised by replacing the thin metallic film layer by a semi-liquid electrolyte solution in the form of jelly or paste is used which acts as second electrode. It offers above 1uF capacitance level. Electrolytic capacitor used for low frequency applications such as power supplies, decoupling and audio coupling system ,when the frequency limit is around 100kHz. Aluminium and tantalum are most common electrolytic capacitor.

Tantalum capacitors have higher value and better performance for limited number of applications. Better capacitance strength and lower leakage current than aluminium type capacitor which makes them suitable for obstructing, decoupling and filtering applications. The main advantageous application sectors of tantalum type capacitor are volumetric efficiency, good characteristics and high reliability, wide temperature range, compatible with modern production method. Higher ripple current ratings and Demerits is more expensive.

Higher capacitance value can be achieved with aluminium type capacitor by increasing the thickness of aluminium oxide film and heightened breakdown voltage. There are several merits of aluminium type capacitor like low cost, large capacitance per unit volume, impedance and ESR in stayed minimum for certain level of MHz for capacitor < 100uF. It has also poor tolerance level and temperature, frequency dependency [1].

2.3. Capacitor Energy

The fundamental aspect of capacitor is consisting of energy density and power density. Density measured as quantity per unit volume and energy E directly proportional to the capacitance. When capacitor charged up from the power supply and the energy stored by the established electrostatic field. It's express in Joules. The amount of energy E stored by electrostatic field is equal to the supply voltage V.

$$E = \frac{1}{2} CV^2$$

As we know Power is the energy expended per unit time. To determine power of capacitor, we have to consider the capacitor as a circuit in series with a load resistance R as is shown in Figure: 1.

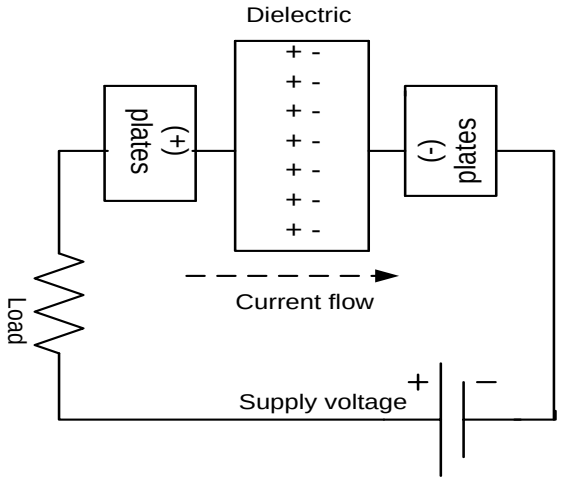


Figure 2.1: Schematic of charging circuit.

The internal components of capacitor (electrodes, collector current, dialectic material) also participates to the resistance and the measurement taken by a technique known as equivalent series resistance (ESR). This resistance determined the voltage during discharging. The maximum power of the capacitor evaluated by the impedance e matching between load R and ESR. The maximum power P_{max} of a capacitor is given by

$$P_{max} = \frac{V^2}{4 \times ESR}$$

From the equations we can assume how ESR limits the minimum power of capacitor [1].

2.4. Charging and Discharging of Capacitor

The main purpose of capacitor charging and discharging is measure the potential difference across the capacitor. Capacitors charging depends on two factors the capacitance and the resistor of the circuit through which capacitor being charged or discharged.

First of all we need to connect the positive terminal of the battery to one capacitor plate and negative terminal with other capacitor plate. During charging when the battery or power supply connected across the capacitor, current flows and the potential difference across the capacitor begins to increase. When more charge accumulated on the capacitor plate, at this point the current and potential difference starts to decline. Because of electrons movement between battery and capacitor with same force but opposite direction, Current flow will be stopped and supply voltage and potential difference of the capacitor will be equal and opposite magnitude. At this point capacitor is fully charged.

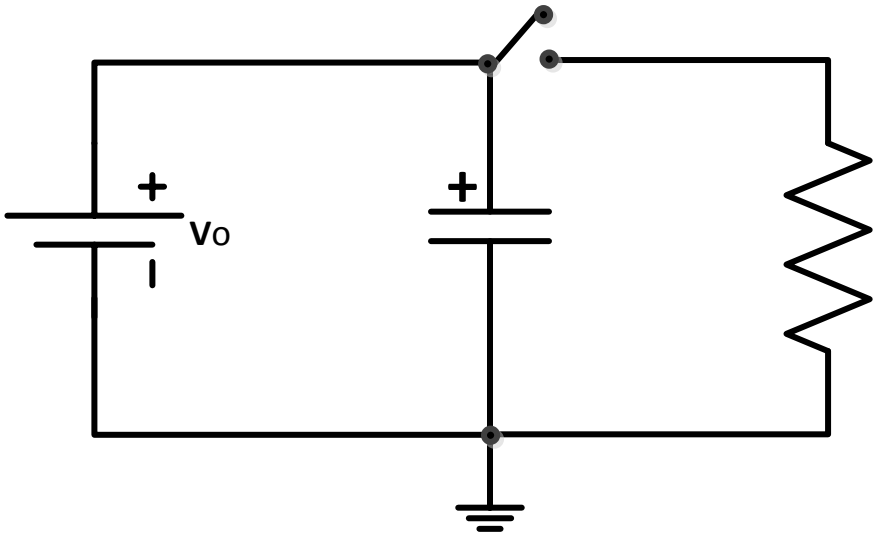


Figure 2.2: Schematic of charging circuit [19].

The primary objective capacitor of discharging of a capacitor is to nullify the charges between the two conducting plate. During discharging huge amount of current begins to flow through the load. Potential difference across the capacitor starts to reduce. Charged becomes inactive because of charge flowing from one plate to other through resistor. At this point the disoriented electrons are returned to their normal positions and the collected energy is returned to the circuit. Therefore reduced the current flow rate and decrease rate of potential difference. Eventually the charge on the plates is zero so current and potential difference also zero. Capacitor fully discharged. Discharge rate depends on value of resistor.

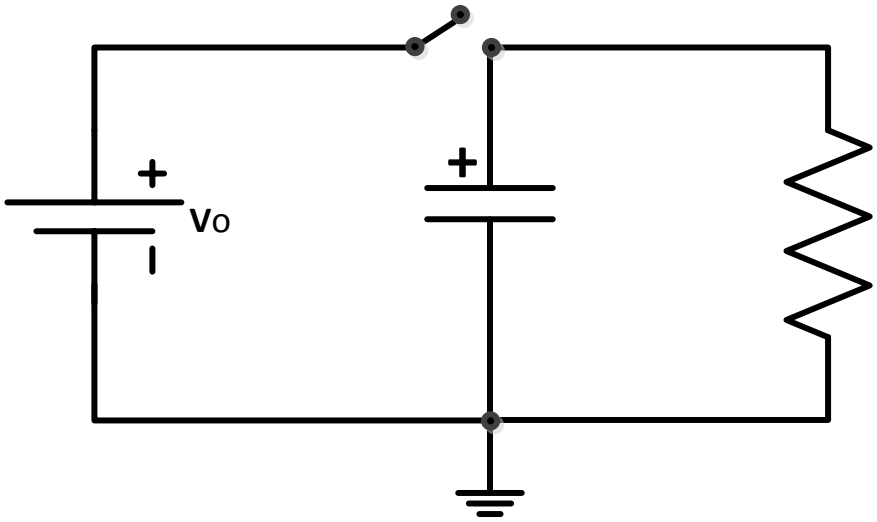


Figure 2.3: Schematic of Discharging circuit [19].

2.5. Capacitor and Super-Capacitor

The Electric Double layer capacitor significantly changed the energy storage system principle. Basic difference between capacitor and super capacitor is super capacitor is more competent to store more charges as well as energy compared to capacitor because of energy density. Both of them highly applicable in complex circuit design

Generally electrolytic capacitors are made by electrolytic semi liquid solution and metallic films. Extensive capacitance is created by big surface area and rolled up materials. The main property of capacitor is capacitance that expresses how much charge a capacitor can store without discharging. Due to the conductive solution and second electrode, the extended oxide layer in metallic film use to prevent shorting the electrolytic solution by metallic film. The capacitance of the electrolytic capacitor rapidly increases because of very narrow dielectric film. Primary limitations of electrolytic capacitor are polarization and voltage ratings. Assure the connections are correct to rescue the capacitor from destruction due to wrong connection. Low voltage rating up to several hundred. Capacitance can be improved by boosting the area and decline the gap between electrodes or more permittivity dielectric medium [5].

Super-Capacitor or Electric double layer capacitors are so called super-cap. Super-cap has two or three times more capacitance than normal capacitor. So the energy density of the super-cap is better. Voltage limit of super-cap is about 2.5 to 2.7V. Higher voltage can achieve with service life reduction. Super –cap can charge and discharge unlimited number of times. Bit expensive in terms of cost per watt. By connecting several super-caps in series, we can get higher voltage but that will causes capacitance reduction. It's not application for AC circuit's application because it has high internal resistance. It has super recyclability. It offers more than 500 000 recharge cycles on the other hand

declarable battery offers only 1000.they can be charged up very quickly. Possible to manufacture in any size [5].

Super cap is more expensive compared to electrolytic capacitor. Super-cap employ two dielectric material separated by thin insulator where normal capacitor use only one. Super-cap has impressive low temperature and discharge performance, high specific power and high load current. No end of charge termination is required for Super-cap. Linear discharge system of Super-cap declines to use full energy spectrum and requires series connection for cell balancing. the self-discharge compared to normal capacitor and battery[4].

2.6. Capacitor and Battery

In Electrical circuit power is provided by battery. A direct current (DC) and potential difference between positive and negative terminal is supplied by battery. An inverter can convert the DC batteries into AC.

Battery stored the energy as chemical energy, then its converts into electrical energy. When a battery is connected to a circuit a current flows between positive and negative electrode. It's known as discharging function. If the discharging cycle is too high, the chemical energy becomes almost zero. So rechargeable battery should be charged up again. Batteries discharge rate lower than capacitor. Substantially battery depends on chemical compositions of metal and acid to determine the capacity, resistance, voltage and recharge ability.

Capacitor has lower energy density compared to battery. Instant charge and discharge flexibility. Possible to manufacture in any required voltage. For battery high energy density and limited charge and discharge depending on the chemistry and design. Limited number of charge and discharge cycles. Voltage determine by chemistry [5].

2.7. Super Capacitor and other Battery Technologies

Super Capacitor is always well known for long life cycle, faster charging and discharging rate. Batteries are temperature sensitive. Also reduce the efficiency with degrading temperature and increasing with temperature increases. Higher temperature also affect the life cycles of battery by factor two with every 10°C temperature above 25-30°C increase. Even batteries are not allowed to charge in cold temperature, needs minimum moderate temperature. Based on manufacturer's specifications batteries are allowed to charge below the moderate temperature with lowest charging current. For faster charging need to take blanket support for heating. Electrical short circuit may happen due to cell reversal to minimize over discharging. Large battery system may require preventing big repetitive discharge cycle. Suitable DC discharge option is better

than pulse and aggregated loads for battery. At high frequency battery behaves like capacitor during discharging. Produce higher current more than with the DC load. With heavy loads lead acid is inactive and needs few seconds to recover.

On the other hand Nickel-cadmium (NiCd) has several advantages. Rapid and easier charging option. Able to provide 1000 charge/discharge cycle with convenient maintenance. Performance with load is better and also rough to abuse protection. Possible to preserve in discharge state with long shelf life. No regulatory control is necessary. Better performance with low temperature. Cheaper in price according to the cost per cycles. Different size and specification performance options. Major demerits are Lower energy in comparison with new battery product. Due to the memory effect need to continue after every certain period. Contains cadmium toxic metal and harmful for landfills and Because of self-discharging need to charge again storage. Nickel-metal-hydride (NiMH) merits are higher (30%-40%) capacity than NiCd. Less memory problem and Contains mild toxic metal. Demerits are Narrow service life due to higher discharging. Complicated algorithms necessary for charging. No overcharging absorption is present so keep the tickle charge as low as possible. During rapid charging and high load discharging consumes heat. Battery chemistry contributes to reduce the self-discharge and Performance degradation might occur due to storage temperature. Should be stored with 40% state of charge. Lithium-ion Merits are higher energy density. Lower self-discharge, half in comparison with NiCad and NiMH. Less maintenance, no memory issue and no periodic discharge. Demerits are to limit voltage and current additional protection circuit is necessary and Aging problem even if it's kept as unused.
Super capacitor able to consume very high capacitance as ultra-capacitor or double layer capacitor. Capacitance level defines the difference between regular capacitor and super capacitor. Merits are limitless cycle life and possible to cycle millions of time. High load current provided by low resistance and specified high power. Without end of charge termination possible to charge in a second. No overcharging problem and easier charging. Abuse protection and secured and Shows wonderful charge and discharge performance at low temperature. Demerits are low specific energy. Continuous discharge voltage can't allow using full energy spectrum. Self-discharge is higher than most of the battery system. Serial connection is required with the voltage balancing due to low cell voltage and more expensive.

The following table shows the performance comparison between super capacitor and Li-ion batteries.
Table 2.1: Comparison between Super capacitor and Lithium-ion Battery [4].

Function	**Supercapacitor**	**Lithium-ion (general)**
Charge time	1–10 seconds	10–60 minutes
Cycle life	1 million or 30,000h	500 and higher

Cell voltage	2.3 to 2.75V	3.6 to 3.7V
Specific energy (Wh/kg)	5 (typical)	100–200
Specific power (W/kg)	Up to 10,000	1,000 to 3,000
Cost per Wh	$20 (typical)	$0.50-$1.00 (large system)
Service life (in vehicle)	10 to 15 years	5 to 10 years
Charge temperature	–40 to 65°C (–40 to 149°F)	0 to 45°C (32°to 113°F)
Discharge temperature	–40 to 65°C (–40 to 149°F)	–20 to 60°C (–4 to 140°F)

When the capacitor is charged, charges are automatically spreader in positive and negative ion within the layer. Capacitor doesn't have electrochemical reaction like battery, it has only electric charges consumption and deception during charging and discharging. Primary advantages of super capacitor are high charge and discharge current, less maintenance, long cycle life and other many advantages. It's possible to 95% efficiency and due to small amount of leakage current it can consume more energy for long time. Storages power depends on double layer electrolyte capacity and additional benefit is contains no harmful elements for environment [11].

2.8. Characteristics of Super Capacitor

Super capacitor has higher capacitance and higher energy density in comparison with normal capacitor. It has better power densities compared to batteries.

Making Process of Super Capacitor

Generally super capacitors are made from carbon electrodes with also consume high surface area. Super capacitor made by an aqueous or organic an electrolyte and a separator, this separator provide electronic insulation between the electrodes by transferring ions. Due to the applied voltage, ions in the electrolyte solution diffuse across the separator into the pores of the electrode of opposite charge. Due to the double layer phenomenon that occurs between a conductive solid and a liquid solution interface, charge collects at the interface between the electrodes and the electrolyte. Accumulated charge forms two charge layers with a separation of several angstroms. The distance between the electrode surface and centre of the ion layer is indicated by d.
Charge separation in the interface causes the double layer capacitance. According to the capacitance is proportional to the surface area and the reciprocal of the distance between the layers. In this high capacitance is achieved for super capacitor. Super capacitor accumulate the electric charge electrostatically and no reaction between the electrodes and layers. For this reason electrochemical capacitor can undergo hundreds of thousands of charge and discharge cycle [23].

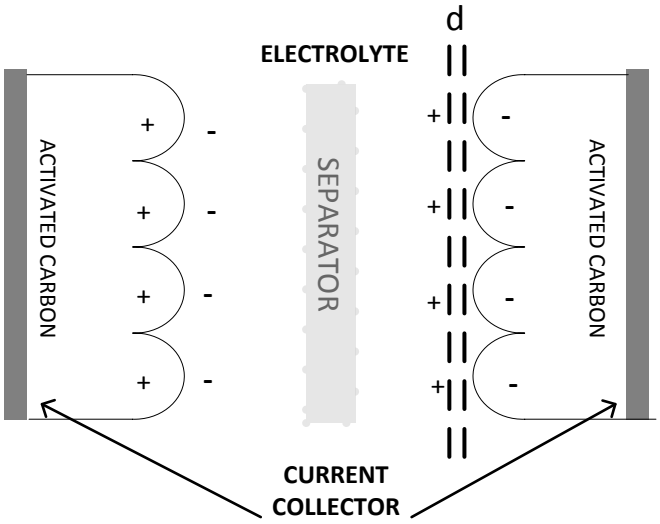


Figure 2.4 : Internal Schematic of Super capacitor [23]

Super capacitors are unique electrical storage devices that can store much more energy than conventional capacitors, and offer higher power density than batteries.

Table 2.2 : Differences between organic and aqueous super capacitors [24].

	Aqueous	Organic
Voltage per cell	Maximum = 1V	Maximum = 2.7V, with limited range flexibility
Manufacture	Simple	Difficult
Cost	Low price	High price
Balancing circuit	Usually not required	Required
Leakage current	Quick stabilization	Lengthy stabilization required
Environmentally friendly	Green product	Not a green product

Electrical Characteristics

Discharge Cycle

Higher capacitance of the super capacitor causes large number of charge and discharge cycles almost millions. During the operating life of the super capacitor there is no disposal part which makes it environment friendly. Super capacitor act as charge conditioner and storing energy from other sources for load balancing purpose and then using excess energy to charge the capacitor only at perfect time [24].

Low Internal resistance

Compared to other battery technologies super capacitors exhibits low internal resistance or ESR, high efficiency (up to 97% - 98%), maximum output power, lowest heating

levels and better safety. The specific power of a super capacitor can up to 6kW/kg at 95% efficiency [24].

Double Layer Capacitance

Super capacitors charging and energy storing capacity is higher density than standard capacitors. Super capacitor energy measured in farad where normal capacitors energy estimated in nano or micro-farads. Amount of energy depends on stored charges between the plates. Dielectric material quality determines the charge potentials. On the other hand in case of double layer capacitor dielectric material is blocked into a carbon material with higher surface area and rendering the dielectric medium so thin. To produce high charge potential as well as capacitance, the large area combined with a narrow medium. Capacitor with double layer is conductive and low tolerance for voltage. Voltage reception can also increase by connecting multiple super capacitors in series. Used materials also affect the efficiency of the capacitor. Carbon has ore surface area than aluminium and which is commonly used in capacitors. There are many differences in design, application and cost between super capacitor and other capacitors [12].

Pseudocapacitance

Repetitive behaviour of RuO_2 DSA produces stable anodes for commercial CI_2 production. It has a response of a capacitor under linear voltage sweep modulation. Pseduocapacitance is concerned with under potential deposition of adatoms of H and later of the metal atoms. Duo to the passing of the charge through an electro sorption process or in quasi two dimensional intercalation process or surface redox process as with RuO_2 as a function of electrode potential. Duo to the capacitance a derivative is introduce dq/dV. This type of faradaic capacitance originates with potential dependent electrostatic charge as like double layer capacitor. It's usually called pseduocapacitance with faradaic charging [20].

Electrode Materials

Electrode material depends on chemical reactions which is consist of several types of metal oxides like RuO_2, IrO_2,Fe_2O_3,MnO_2 and NiO ,conducting polymers and Polyanilines and their derivatives. Also different types of carbon materials. Carbon based super cap is most commonly used. Carbons material has much bigger surface region around 1000 to 2000m2g. Basal plane and edge plane capacity is about 10-40uFcm and 50-70uFcm respectively. During carbonization, physical and chemical activation higher surface and position can be achieved. Metal oxides based material also used besides carbon based electrodes. The RuO_2 electrode has dimensionally stable anodes. RuO_2 electrodes provides better cyclic voltammetry (CV) curve and exhibits best capacitor characteristics in comparison with other transition metal oxides. In the market there are polymer based super cap and hybrid Nano composite based super cap [21].

2.9. Characteristics of Aluminium Electrolytic Capacitor

In this project we used Aluminium electrolytic capacitor as super capacitor. The main properties of this capacitor are stated here. In the appendix we also represent the Specifications of Aluminium Electrolytic Capacitor.

Polarised capacitor is another name of Electrolytic capacitor. Because of polarization the positive and negative lead of the capacitor must be carefully connected to circuit's polarity. It has higher capacitance compared to non-electrolytic capacitors.

Aluminium electrolytic capacitor made by comprised of aluminium foil with surface of dielectric oxidation. Here the surface act has a semiconductor characteristic which helps to block current flow between the electrodes. An electrolyte impregnated paper also placed between the electrodes to aver short circuits. To increase the surface area of the aluminium foil etched the surfaces. High capacitance of the capacitor controlled by the matching between size dielectric medium and bigger surface area [6].

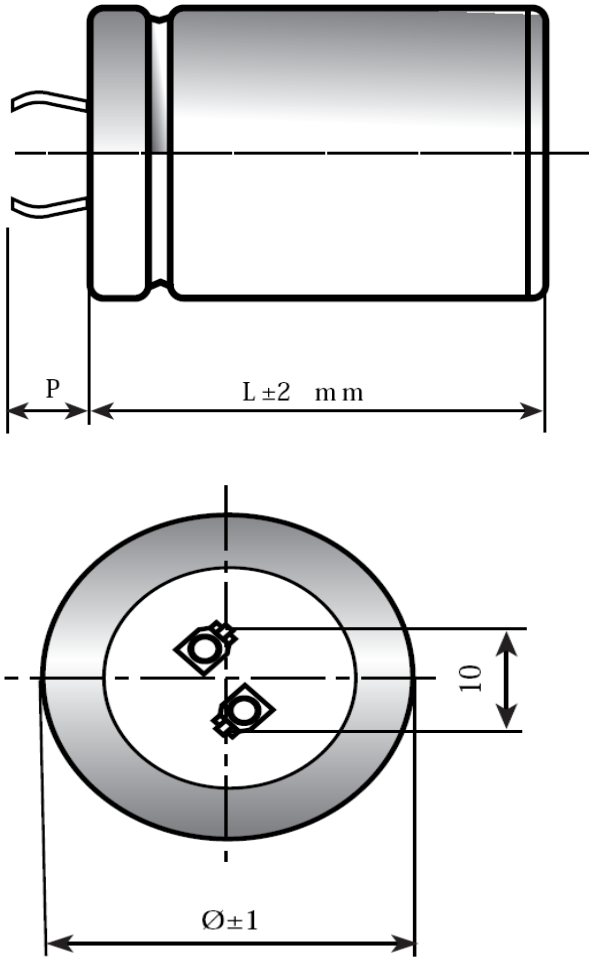


Figure 2.5: Two Pin Capacitor Dimension in mm

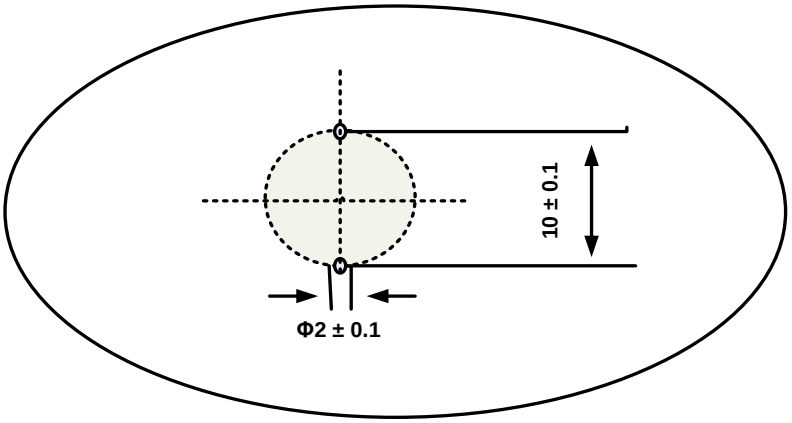


Figure 2.6: Circuit Board Hole Dimensions [20].

Making Process of Electrolytic Capacitor

The manufacturing processes of Electrolytic capacitor divide into following steps

Etching

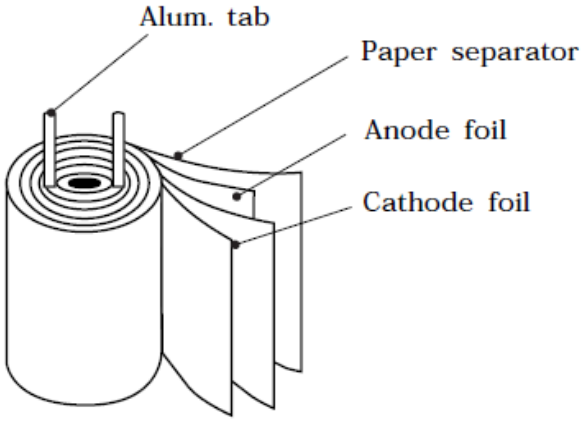


Figure 2.7: Elements of capacitor [6].

High purities electrodes are consist of narrow aluminium foil 0.05 to 0.1 mm thickness. Ultimate capacitance can be gained by etching process, dissolving the metals and maximize the surface area same as dense network of microscopic channels. Run the aluminium foil through a chloride solution and apply AC, DC or AC/DC voltage between the etch solution and aluminium foil. Almost 100 times better active surface area can be improved. The dielectric medium consists of aluminium oxide (AI2O3).The relation between thickness of the dielectric medium and applied voltage can de express as

$$\text{Capacitance} \times \text{Forming voltage} = \text{Constant}$$

Winding

Every capacitor has two foils namely cathode and anode with a separator paper and place into a cylinder. Separator paper acts as protector of contact with other and short circuits. Winding process attaches the anode and cathode with aluminium foils. The product is called capacitor ELEMENT formed by etched together with separator paper [6].

Impregnation

The main step of this process is providing the winding element by vacuum/pressure cycle with or without applied heat or through absorption. Ethylene glycol and ammonium borate are main elements of electrolyte. Various choice of electrolyte can change the characteristics capacitor such as temperature range, frequency response, shelf and load life.

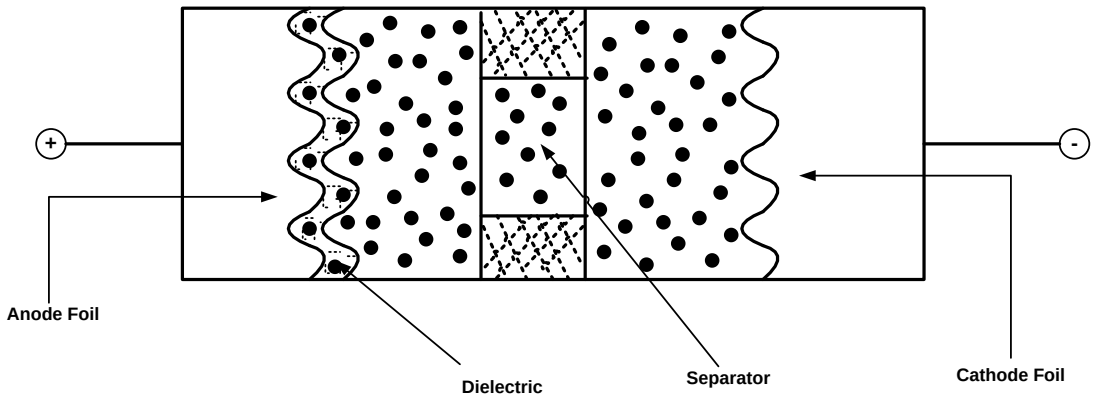


Figure 2.8: Cross Section of a typical element [6].

Sealing

Rubber/Bakelite or phenolic plastic use as sealing deck to seal into aluminium can.

Ageing

Last step before production chain. Aging and testing should be done carefully before packing. Greater than rated voltage applied at high temperature to reform the oxide film and therefore decreased the leakage current to a reasonable level [6].

Production Inspection

100% has been done in ageing step. Automated testing system used to check all the electrical specifications. Visually inspected capacitors are allowed for packaging.

Electrical Characteristics

Rated Capacitance

An equivalent circuit with series connected capacitance and resistance that define at 100Hz and 20˚C. Rated capacitance indicates the AC capacitance of the capacitor has been manufactured. Indicated in micro Farads (uF).

Rated Voltage (V_r)

Operating voltage within the temperature range the capacitor can sustain and work properly. The total voltage of peak AC voltage and DC voltage must be below the rated voltage. Before superimpose AC and DC voltage. Voltage association is different when capacitors are series connected. Because of DC leakage distribution there are two

choices use capacitor with high rated voltage or connect a series resistance with every capacitor.

Surge Voltage (V_p)

Maximal voltage for short period of time includes DC, peak AC is considering for the capacitors up to 5 times for 1 minute per hour. According to the specifications along with maximum operating temperature and current limiting resistor about 1000Ω is used to perform the measurement. Hold the charge for 1000 cycles for 30 seconds after that capacitor is allowed for discharge without load for 5 minutes. For aluminium electrolytic capacitor surge voltage and rated voltage are allocated as below

Table 2.3: Surge voltage and Rated voltage Distribution [6].

	V_p=1.15 V_r										V_p=1.10V_r			V_p=1.05V_r	
Rated Voltage	16	25	40	50	63	75	100	160	200	250	350	400	450	500	550
Surge Voltage	18	29	46	57	72	86	115	184	230	287	385	440	495	525	578

Equivalent Series Resistance (ESR)

Resistive component of the equivalent series circuit. ESR value depends on paper foil, electrolyte, aluminium foil and tabs. To alternate the flow of the current direction. Observed at 100Hz of 20˚C. ESR has temperature and frequency and also related with dissipation factor can be express as

$$\text{ESR} = \frac{\tan \sigma}{\text{w } C_s}$$

Where,

C_s Equivalent series capacitance F.

W Dissipation factor.

For calculating ESR the rated capacitance also taken into account.

The Kendeil production technology remarkably reduces the ESR value [6].

Leakage Current

Due to Dielectric characteristics of aluminium oxide layer small current flows, after the DC voltage application. Leakage current flows provide confirmation that the dielectric is working well. These current flows continue in declining direction until to get a small constant level. It's observed at 20˚C after 5minutes rated voltage. Leakage current has voltage and temperature dependency. To avoid the exceeding rated voltage its suggested to connect a series resistance of 100Ω for <100VDC and 1000 Ω for >100VDC [6].

Dissipation Factor tanσ

Dissipation factor or loss tangent tanσ are used to evaluate the loss of energy when the capacitor is in oscillatory mode. It can be defined as ratio of effective or dissipated power to reactive power or equivalent series resistance to the capacitive component.

$$\mathbf{Tan\ \sigma = 2\ \pi\ f\ C\ ESR}$$

Where,

f= Frequency

C=Capacitance

ESR= Equivalent series resistance

Inductance

Few tens of nH valued inductance used in aluminium electrolytic capacitors.

Impedance

The following equivalent circuit forms the impedance of electrolytic capacitor.

Figure 2.9: Equivalent Circuit of Electrolytic Capacitor[6].

$$\mathbf{Z = \sqrt{ESR^2 + (X_L - X_C)^2}}$$

At the point of series resistance Z-ESR, Low frequencies capacitive reactance ($\boldsymbol{X_C}$) and high frequencies inductive reactance ($\boldsymbol{X_L}$) primly controlled the impedance.

Ripple Current

Pulsating or ripple voltage causes alternating current flow through the capacitor .the RMS value of the current is called ripple current. Simply sinusoidal alternating current at 100Hz. Peak ripple current depends on ESR, dissipation factor, heat dissipation or surface area, ambient temperature and AC frequency. This entire factor affects the operating life of capacitor.

Shelf Life

Without reducing reliability of the capacitor and it can be stored at temperature up to 50˚C. Even when the leakage current flow will raise the ESR, capacitance, impedance will show good performance.

In practical this feature can be expressed as below

Three years	Two years
≤100V DC	≥100V DC

For longer period it might cross rated voltage and at this stage before output measurement randomization is necessary.

3. POWER MANAGEMENT SYSTEM FOR SUPER CAPACITORS

3.1. Functions and Design Target of PMU

PMU is smart version of BMS system. The primary function of BMS system is providing maximum SoC with battery cells protection and cell balancing. In BMS battery cell always operated in a reasonable range. On the other hand PMU has ability to control charging and discharging of the capacitor cell. PMU is able to measure and represent the result like Voltages, SoC, SoH and temperature level during charging and discharging. There are many options for charging and discharging super capacitor. Super capacitor can be charged and discharged at same rate, which is useful for energy recovery system. There are constant current charging, constant voltage charging and isolated AC line charging method to charge super capacitor. Besides other various options Linear Technology also provides of linear, switching and switched capacitor ICs designed to charge super capacitors. That includes input or output current limiting, automatic cell balancing and a range of protection features that make them uniquely suited to super cap charging [22]. Here we are using MAX11068 interface board. More about controlled charging and discharging of super capacitor is described in chapter 6. Testing the faults of super cap there are numerous options to check it out. Constant current charge/discharge to check the capacitance and resistance discharge timing, pulse test to determine resistance, constant power charge/discharge to check the range curve for power densities etc.

In this thesis the PMU is designed to measure and show the voltage and SoC. With the help of java programming a user interface is created to measure and represent the voltages and SoC. Also shows the total voltage, total SoC and maximum and minimum cell voltage. This PMU also able to control cell balancing. For future research this PMU can be extended to measure SoH and temperature variations.

3.2. Balancing of PMU for Super Capacitors

Capacitive power management system consists of large number capacitors connected in series. Capacitor is low voltage device with highest possible voltage 2.7V. Number of cells is depends on the how much voltage is desirable. All capacitor voltage capacity is not equal and due to the frequent charge and discharge. At some point some of the cell might start to discharge very fast. This fast rate of discharging may damage the cell. To prevent this continuous balancing is necessary. There are numerous ways to balance the cell, one of them is moderately charge capacitor until get the peak point. All cells are not going to damage because of overcharging but repeatedly charging will shorten their life cycle [13].

MAX11068 has its own cell balancing technique. Internal 6Ω register and external register controls the cell balancing and provides an equalize discharge current based on cell voltage. MAX11068 also have external cell balancing flexibility. It's interconnected with internal switch to control the biasing of external transistor/MOSFET. When the internal switch is off through external bias resistor turn on the external transistor/MOSFET. The discharge current is limited by an external resister.

Most well-known and applicable balancing systems are active and passive balancing. The main drawback of these balancing methods is extra cost and energy losses. The main balancing principle of passive balancing system is remove the extra charge from highly charged capacitor through some passive elements, (resistor) until these charge will match with the charge of other capacitor in the pack. In the active balancing system charge from highly charged capacitor is transfer to lower charged capacitor until their charge is in same level. Selection of balancing technique is depends on element used for storing the energy such as capacitor or inductor and also depends on switches or converter used to control [14]. The circuit represent as below is one of the least expensive passive balancing system where extra charge dissipate through resistor and balance current dissipate as heat.

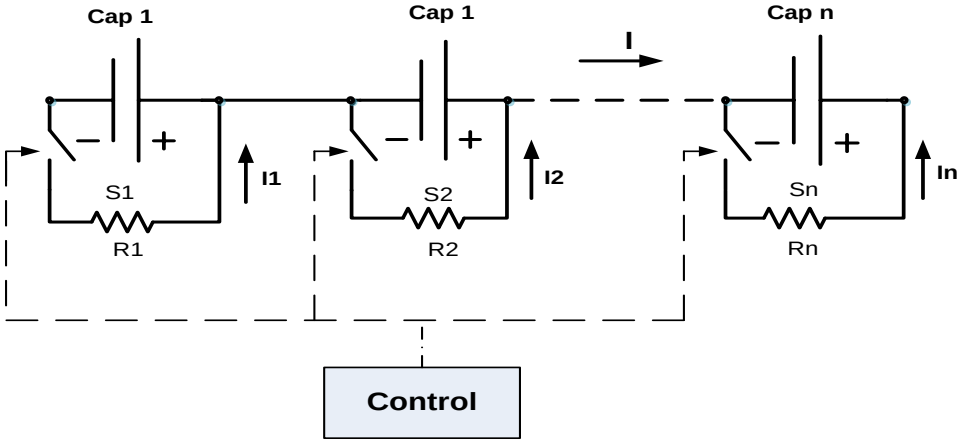


Figure 3.1: Passive balancing with Resistor [15].

The circuit below is capacitive active balancing circuit. Where capacitors are used to store the energy.

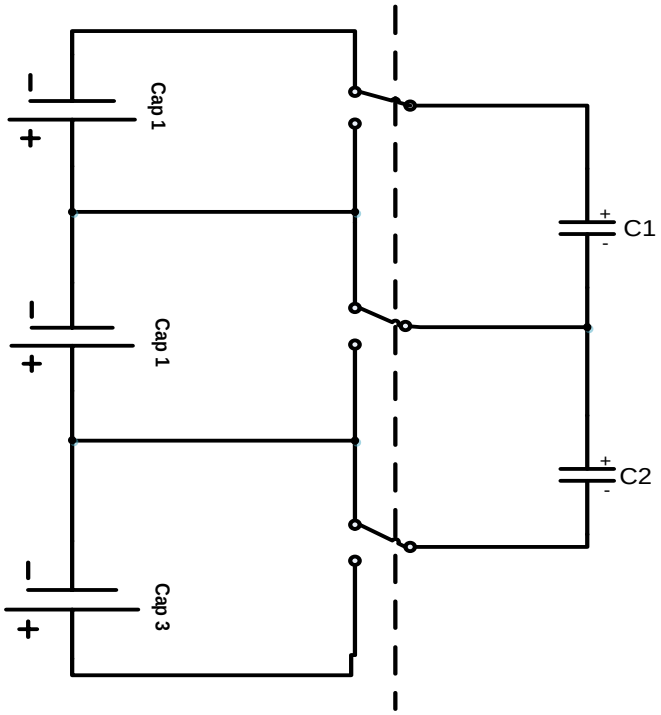


Figure 3.2: Active balancing circuit[15].

3.3. State of Charge (SoC)

State of charge estimation is one of main fundamental parameter for batter managements system and also for super capacitor. Its express the amount of residual capacity of the capacitor. For proper management and maintenance of capacitor, SoC information is necessary. For capacitive power management based electric vehicle miles information also can deduct from state of charge of the capacitor. There are several techniques to estimate state of charge includes ampere hour method (Ah method) based on current Integral, open circuit voltage method based on battery terminal voltage, neural network based on lots of experiment data and state space model method. There is also some general estimation technique with less accuracy voltage method, Hydrometer, Coulomb counting, Impedance spectroscopy and Quantum magnetism. For our capacitor sate of charge estimation is differ from ideal capacitor because charging and discharging characteristics comply with battery system [16].

Voltage method

Easiest method to estimate the SoC of capacitor or battery. Error can be occurred due to several factors including the chemicals of the battery or capacitor characteristics, temperature plays an important role and last not the least charging and discharging event. Temperature variations vary the open circuit voltage. Charging and discharging can disorient the proper SoC estimation. Accuracy of the voltage based SoC estimation depends on stabilization of the battery or capacitor. Each battery has individual discharging orientation so estimate the SoC needs a tailored model. This method express full charge and low charge and unable to notify large middle section. Without

load floating voltage of the battery or capacitor is the first condition for measuring with open circuit method. Parasitic load makes this method into closed circuit voltage (CCV) that helps to take inaccurate estimation. During calculation of SoC in the CCV state with load adjustment is necessary. Though the estimation is not totally accurate but still it's the most popular method because of simplicity [4].

Coulomb counting

Another method to measure SoC of the battery or capacitor. In this method measure the current flow through the capacitor. Energy level should be equal during charging and discharging. The available energy is always less than what had been fed to the battery, and compensation corrects the shortage [4].

Impedance spectroscopy

Based the impedance and Randles model this method estimate the SoC. This method also works for flooded and sealed lead acid. Like in voltage method resting of battery is not necessary and parasitic load has no effect on the result. More accurate than other methods [4].

Quantum magnetism

Better technique to estimate the SoC especially for lead acid batteries. During discharging of a battery exchange the negative plate lead to lead sulphate. This plate contains different susceptibility to lead. The changes of magnetic field causes produce the linear SoC information due the magnetism of the sensor connected to magnetic field [4].

3.4. State of Health (SoH)

Generally SoH of the battery or capacitor can be obtained as the ratio of maximum charge capacity of an aged battery to the maximum charge capacity of a newest battery. To make an assumption about the performance and life time of the battery, SoH plays an important role. It is determined by several different battery parameters, such as internal resistance, self-discharge, charge acceptance and chemical change. When its SoH drops below the threshold value, this battery cell reaches the end of its useful life. Useful life prediction of capacitor also can estimate by Kalman filter framework and an empirical degradation model. The data from the measurement is used to predict the remaining life cycle calculation. Finally from the empirical degradation model we can estimate the life cycle [17].

$$\text{SoH} = \frac{\text{Aged Energy Capacity}}{\text{Rated Energy Capacity}}$$

3.5. PMU Architecture

To build a high power supply unit multiple number of battery or capacitor can be assembled in series or matrix composition. The important advantage of this modules system are can be used in different architecture, flexible and easy to detect fault. The voltage can be increased by adding more battery cell in series and able to provide sufficient power to the required load. For MAX11068 board maximum number of cell is 12 with minimal voltage 6.0V. To reach 6.0V six capacitor cells per module is enough. Battery pack can be composed of multiple numbers of battery technologies and capacitor. Especially capacitive cells are suitable choice for regenerative energy storage. There are two types of battery management system compatible with MAX11068 distributed and SMBus laddered module communication. In distributed system each battery has point to point connection to a main microcontroller. Due to the high voltage system, galvanic isolation necessary to communicate with main microcontroller. Other SMBus system has a serial bus and that can reach each battery cell. This model reduces cost and one galvanic isolation is enough between high voltages batteries and main power net. Low voltage doesn't need galvanic isolation [8]. BMS portion of the PMU unit will be explained in more detail in the next chapter.

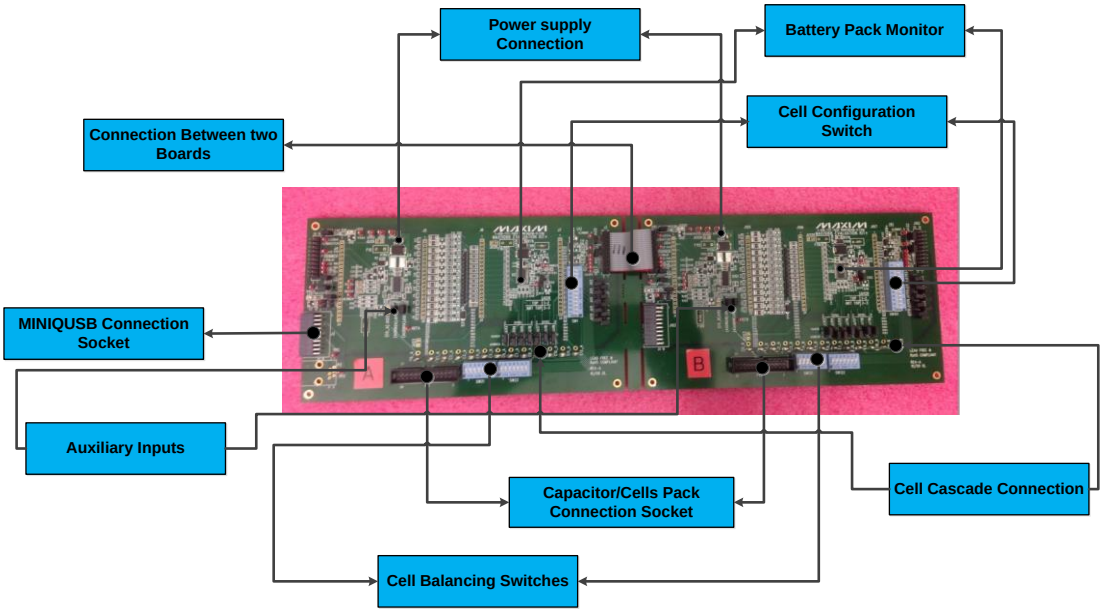


Figure 3.3: Demo Board of MAX11068 [10].

4. MAXIM SMART INTERFACE BOARD

Main application of maxim interface board is to monitor high voltage measurement with maximum accuracy and also for monitoring capacitive power management unit. We used here MAX10680 interface board. It has cell balancing flexibility and to measure thermal overload. Each board has 12 built-in cells balancing or discharge switches it can support up to 200mA discharge current and maximum ambient temperature +75˚C. It's also possible to activate all cell balancing switches at a time to check the open circuit connections. I^2C Interface controls the chips connection. Los cost, reliable communication developed because of the built-in level shifting and predefined command protocol. Internal oscillator provides ±3% accuracy with oscillated 6.0MHz signal [8].

Applications Sectors of MAX11068

- SuperCap Power Management Systems.
- High Voltage and Multicell Series Stacked Battery systems.
- Hybrid Electric Vehicle (HEV) Battery Packs.
- Electric Bikes.
- Power Tools and High Voltage Battery Backup Systems.

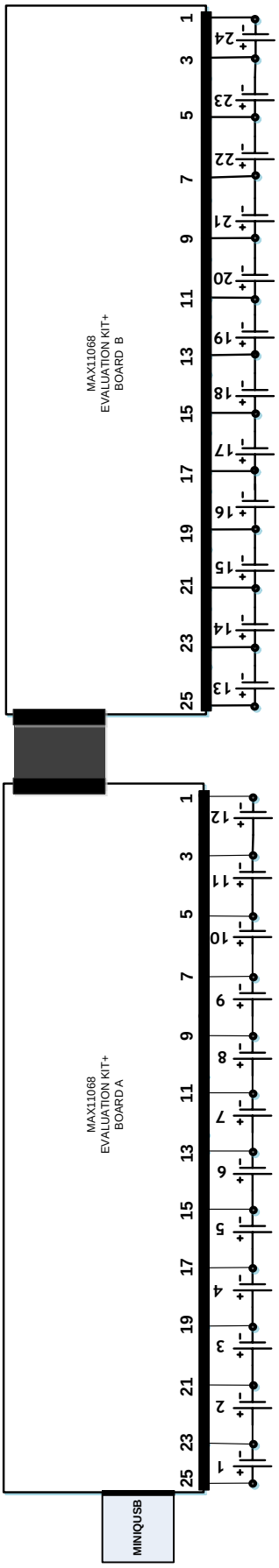


Figure 4.1: MAX11068 connections with 24-cells Capacitor pack [8].

Aspect of MAX11068 is capable of up to12-Cell Super-Capacitor Cells voltage Measurement with Temperature Monitoring and also two Auxiliary Analogue Inputs for Temperature Measurement. It has ≤ 5mV Offset Voltage with ±0.25% Voltage-Measurement Accuracy. This demo board also facilitate with 12-Bit Precision, High-Speed SAR ADC and 12 Cell Voltages Measured Within 107µs. It also able to detect Overvoltage and under voltage, Cell Sense Line Open-Circuit and High/Low Temperature. 12 Integrated Cell-Equalization Switches Support Up to 200mA, Integrated 6V to 70V Input Linear Regulator, Integrated 25ppm/°C, 2.5V Precision Reference and Integrated Level-Shifted, I^2C-Compliant SMBus Ladder Interface and Three General-Purpose Digital I/O Lines with Ultra-Low Power Dissipation. It has Operating Temperature Ranges -40˚C to +105˚C and 38-pin, Lead-Free/RoHS compliant TSSOP Package.

4.1. Functional Diagram of MAX11068

The following figure represents the functions of each block of the board. C0-C12 is the 12 cell connection. Here equalization connects with switch bank multiplexer. Linear regulator and reference block form the LDO and REF section. LDO mainly generates the input supply from the DCIN pin within the range 6.0V to +70V.but only 3.3V is requires to run voltage measurement, control logic, low side communication interface. Acquisition function maintained by 12-Bit ADC and INSTR AMP. Control and status block controlled the whole system. In the right hand side three blocks is responsible for communications namely I^2C UPPER PORT, LEVEL SHIFT and I^2C LOWER PORT.

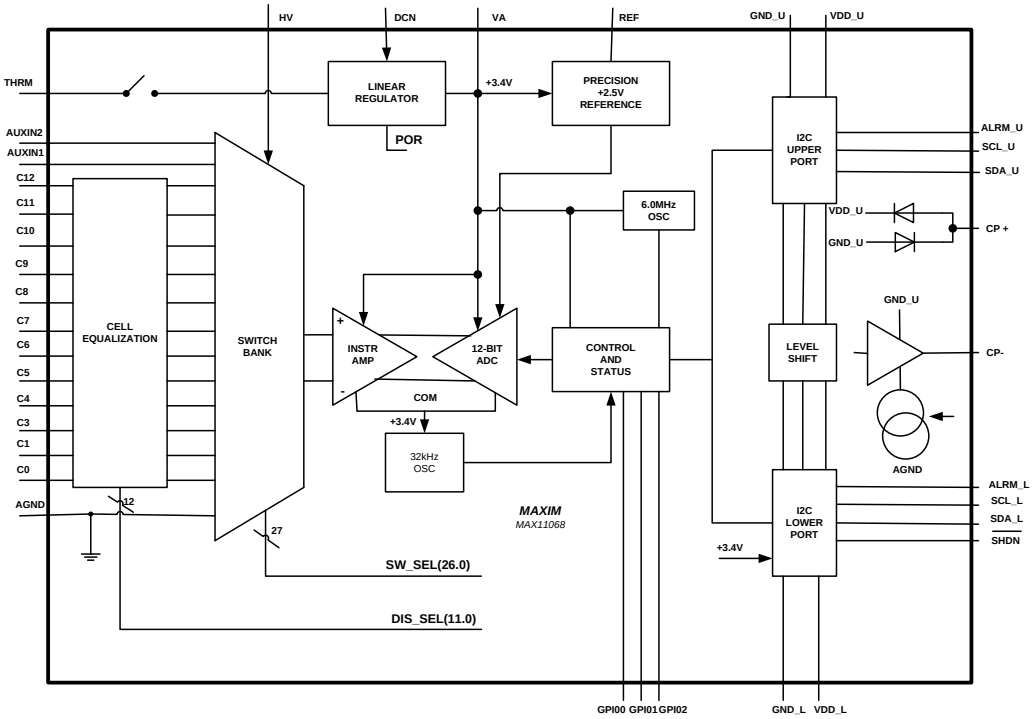


Figure 4.2: Functional Diagram of MAX11068 [8].

4.1.1. Cell Inputs C0-C12

MAX11068 has 13 analog input pins that also used to measure the 12 battery cells. Measurement of the cells are done differentially and level down shifted by internal with high voltage MUX and ADC preamp. Common range for C1 is set by 7V and for C0 range within 50mV of AGND for proper measurement. RC filtering used for each cell input. Resistor values are selected based on target of cell balancing. Capacitor is connecting with the resistor to build the RC filter for ADC measurement. Cell position between C1 and C0 must be implemented with minimum voltage 500mV. ADC specification defines the accuracy of the measurement [8].

4.1.2. Measurement Scanning

CELLEN register enable the acquisition and scheduled conversion of the differential input. Conversion starts with the settling of the SCAN bit in the SCANCTRL register. WRITEALL command and WRITEDEVICE command sets the setting of the SCAN bit based on timing of the conversion. Command will be ignored if the ADC is still busy with previous task. Measurements scan cycle start after getting the scan signal. The measurement sequence is performing as below.

1. All enabled cell inputs phase 1, descending order (12-1).
2. All enabled cell inputs phase 2, descending order (12-1).
3. Self-diagnostic measurement phase 1, if enabled.
4. Self-diagnostic measurement phase 2, if enabled.
5. All enabled auxiliary inputs 1, ascending order (AUXIN1, AUXIN2).

Two steps of cell voltage acquisition cycle can be represented as below

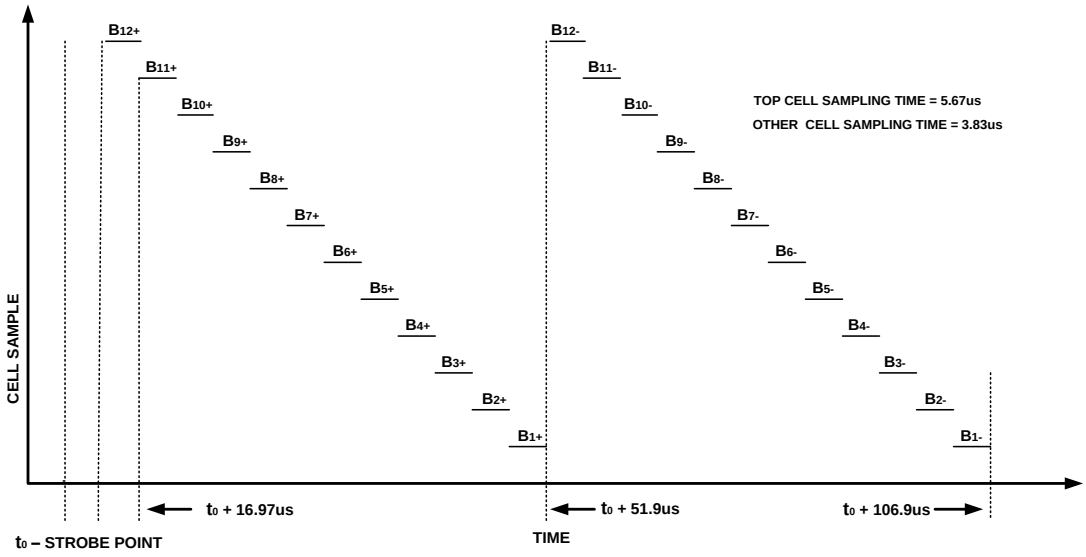


Figure 4.3: Cell Scanning Timing [8].

In the first stage acquisition of raw cell voltage and in next step starting with highest cell ADC scans through all the enabled cell input channels.

4.1.3. Overvoltage and Undervoltage

MAX11068 provides the flexibility to observe cell voltage and notify if alert or alarm of the cell status in necessary situation. Cell data register stores the data after ADC conversion. Depends on previous updated measurement data only enable the data register for particular cell position. Other cells data remain same as before. Over and under voltage always estimated based on minimum, maximum and total cell voltage values. 12bits MAXCELL and MINCELL register stores the minimum and maximum cell voltage. In case of over lapping minimum and maximum cell voltage values, only highest cell position will be counted. Enabled registers cell voltage will be stored in TOTAL register as 16 bit value. Cell voltage also compared with programmable cell over voltage and under voltage thresholds. The following figure illustrates the programmable overvoltage and under voltage thresholds.

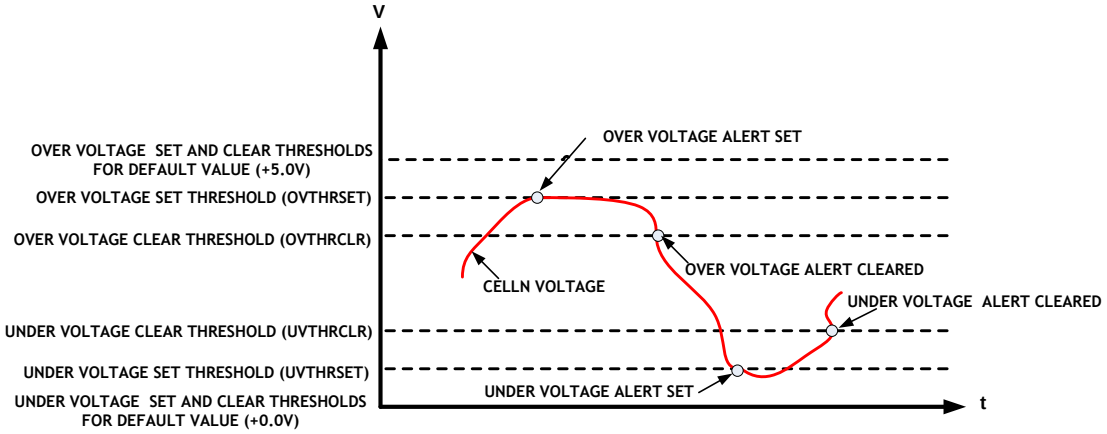


Figure 4.4: Programmable Overvoltages and Undervoltage Thresholds Diagram [8].

4.1.4. Cell Balancing

Internal 6Ω resister and external resister controls the cell balancing and provides an equalize discharge current based on cell voltage. The following figure shows the basic circuit of cell balancing.

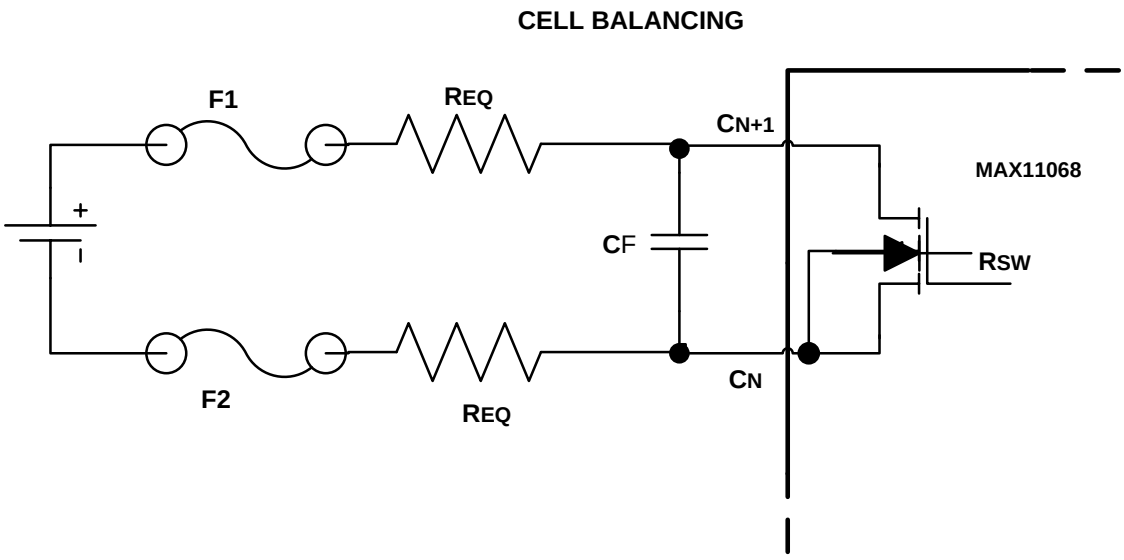


Figure 4.5: Cell-Balancing Switch Network [8].

Cell balancing must be count the following limitations Package allowed maximum power dissipation, Measurement during cell balancing and Enabled cell switches vary the current. Protection from open circuit faults in the battery pack destroying the MAX11068

4.2. I^2C Interface

Connection between the host system and module to module with the help of I^2C command protocol. I^2C Physical interface is actually a SMBus ladder. Every device has two I^2C ports, one is configure as master and another one is slave. Slave port is defined as chip ground and slave port is the lower port. Master port is defined as level shifted and referenced as GND_U. One bridge digital controller used to work together the two ports and it has two separate sequence links. Physical communication can be built by microcontroller and I/O pins with firmware. High noise rejection can be achieved with level shifted dual port scheme. It has resistor map for each cell [8].

Basic I^2C Infrastructure

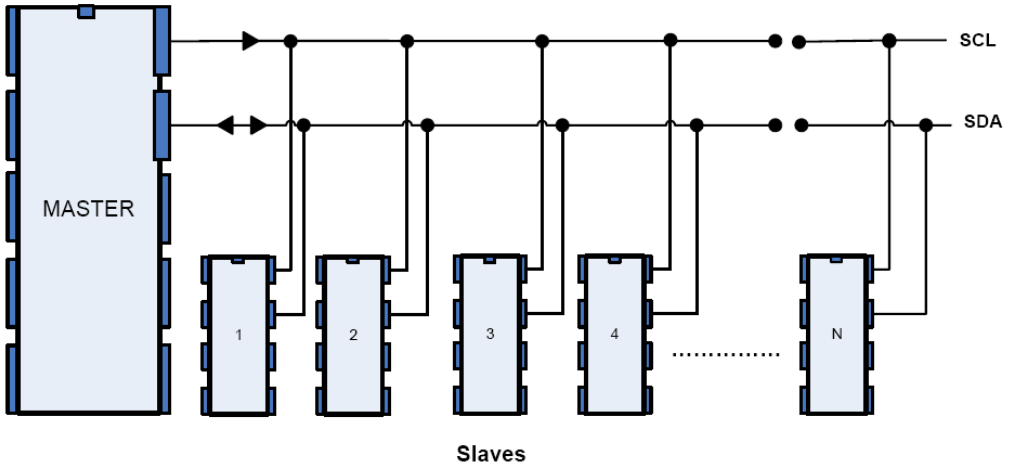


Figure 4.6: Connection between master and slave [10].

Properties of I^2C

Consist of serial data line (SDA) and serial clock line (SCL).This multi-master bus provides the feature of collision detection and reduced data corruption when two or more masters simultaneously transferring data. Each device defined by a unique address through software and maintains a master/slave relationships all times. Master is allowed to work as master transmitter and master receiver. It has the options to serial, 8-bit oriented, bi directional data transfer with 100kbits/s in the standard mode. Fast mode with 400kbit/s and high speed mode with 3.4Mbit/s. To maintain data integrity, chip filter (50ns) removes spikes on the bus line.With the maximum limit of capacitive loading of 400pF, numerous numbers of ICs can be connected to the same bus segment [9].

Merits of I^2C

Popular bus with world class standard over 20 years. Famous in telecom, networking, consumer and automotive industries. Various application features like cell phones, PDA's, DVD, set top boxes. Used in giant companies like HP, Compaq, IBM, Cisco, Intel, Nokia etc. Final schematic and functional block diagram resound with actual ICs.

Not necessary to design bus interfaces because of I^2C bus interface included with the chip. Software allocated integrated addressing and data transfer protocol flexibility. Possible to use same IC for various applications. Design period is short because of familiar functional block consist of I^2C bus compatible ICs. Indecency of adding or removing ICs from a system without harming anything. Easy to find fault and debugging. Reusable software flexibility reduces software development time [9].

SCL and SDA Signals

Bidirectional SDA and SCL with positive supply voltage through current source pull-up resistor. Both lines are HIGH when the bus is free. To execute wired AND function, the output stage of the devices connected to the bus with open drain or open collector. To perform wired AND function the output level of the bus must have an open drain or open collector connection. Standard mode is able to provide 100 kbit/s, up to 400 kbit/s in the fast mode, up to 1 Mbit/s in the fast mode plus and 3-4 Mbit/s in the high speed mode through I^2C bus. Number of interface connected to the nus limited by bus capacitances.

Following figure shows an example for sharing same bus with different supply.

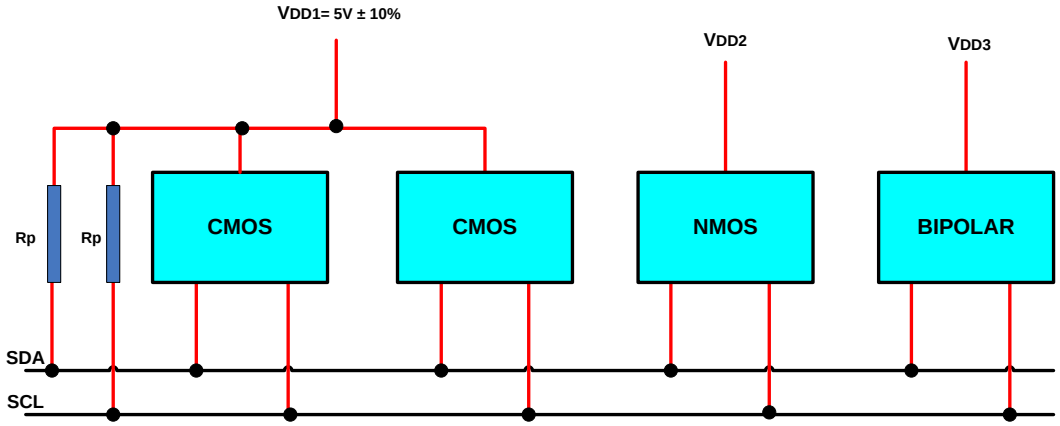


Figure 4.7: Devices with various supply voltages sharing the same bus [10].

V_{DD2} and V_{DD3} are depends on device like 12V.

START and STOP Conditions

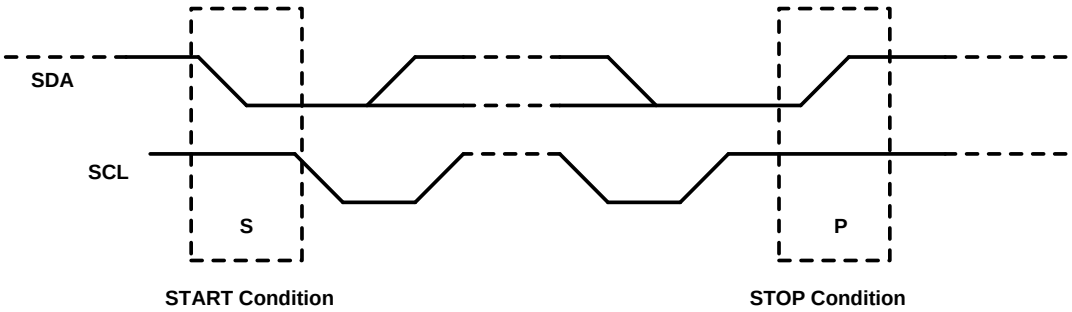


Figure 4.8: START and STOP Conditions [10].

START and STOP are responsible for beginning and stopping the transactions. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Master initiates the START and STOP conditions. Bus stays busy right after START condition and becomes free after STOP condition. Repeating START (Sr) condition causes bus busy. The START (S) and repeating START (Sr) condition are actually opposite.

Acknowledge (ACK) and Not Acknowledge (NACK)

After every byte acknowledgement event occurred. Its assured that receiver got the signal correctly and transmitter is allowed to send next signal. The ninth clock acknowledgement pulse generated by master. The acknowledgement session done by following way transmitter releases the SDA line between the clock pulses of acknowledgement after that receiver can set SDA line LOW and kept it LOW until the HIGH period of clock pulse. Set up and hold times should be counted [9].

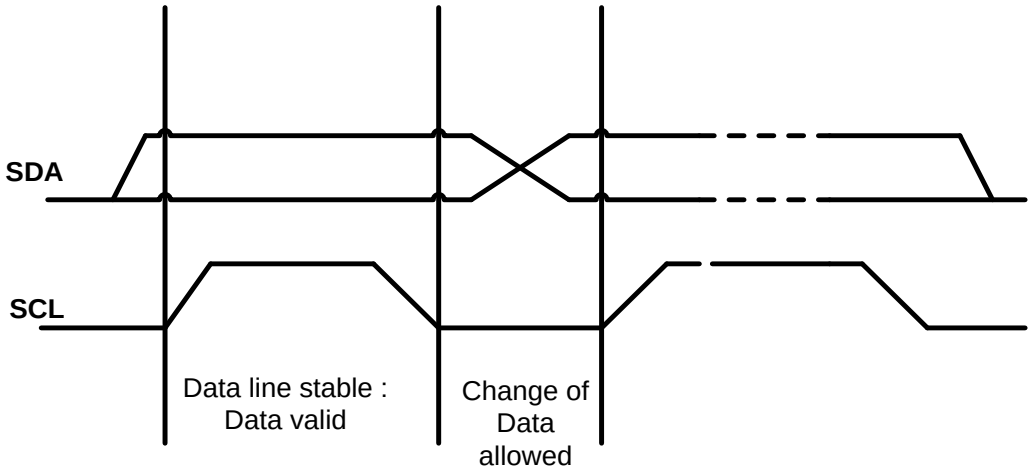


Figure 4.9: Bit Transfer of I2 C [10].

Not Acknowledgment signal is defined by the HIGH condition of SDA line during ninth clock pulse. To finish the transfer master can originates STOP condition or can continue START condition for new transfer. NACK conditions described by following five situations are Receiver will be absent with transmitted address furthermore no device is allowed to response with acknowledgement. Receiver is not available to communicate or receiving or transmitting data during busy with real time function. Problem with receiving data will notify during transfer. Receiver is only allowed to receive one data bytes at a time and Slave transmitter will get a notification signal after each transfer from master.

I^2C Physical Operation

Master block and slave block is the main pillar of physical interface of MAX11068. Master block is level shifted and referenced to the GND_U supply voltage. Coordinates of passing signals and data between the blocks organized by digital controller. Two standard I^2C interface pins for all ports. SCL for serial data clock and SDA for serial data line. For ground referenced $ALRM_L$ output and level shifted $ALRM_U$ input extra status pin is used. This pin provides information about the health of the bus by acting as SMBus laddered interrupt signal. I/O pins supported by level shifted VDD_U which is introduced by an internal charge pump up and referenced to GND_U.The level shifted bus communication signals raised by this generated supply voltage. Every bidirectional SDA pin controlled by internal pull-up drivers.

Address Byte Encoding

After receiving START or repeating START condition I^2C turn on all command with address bye. Every MAX11068 executes following steps after every START condition.

Broadcast Address, WRITEDEVICE command including the device address and HELLO command

Broadcast address is responsible for device respond. This address is used in ROLLCALL, WRITEALL and READALL command. Device address is unique for each part in the chain.

Table 4.1: I^2C Address Bit [10].

I^2C Address Bit	7	6	5	4	3	2	1	R/Wb
Broadcast Address	B7	B6	B5	B4	B3	B2	B	1/0
(Default value)	0	1	0	0	0	0	0	1/0
HELLOALL	1	1	A0	A1	A2	A3	A4	0
WRITEDEVICE	1	0	A0	A1	A2	A3	A4	0

4.3. Comparison between MAXIM and LTC Interface Board

From my system point of view MAXIM interface is not as compatible as LTC. One of the fundamental demerits of MAXIM board is, it has no virtual comport on the other hand LTC has the feature of built in SPI (Serial Peripheral Interface) ,so it can automatically make virtual comport when its connected to computer USB port. For my system we used MAX11068. But new product of MAX7830 has built in comport flexibility. For super cap MAX11068 interface is not appropriate choice due to isolated power supply problem, the input power supply pin is directly connect to the first capacitor cell of the pack. MAX11068 interface board needs minimum 6V power supply to turn it on. For in case of super capacitor during discharging the cell if the board get supplies from capacitor pack it could damage the capacitor due to the higher discharge rate. LTC-6304 has completely isolated power supply port and most importantly LTC-6304 is made for super capacitor. Furthermore, MAX11068 has some advantages as well as some disadvantages over the LTC6804. The voltage range for whole pack without any external power of MAX11068 is greater than the newest LTC6804. Moreover, max series cells of MAX11068 are greater than LTC6804. On the other hand, LTC6804 has more voltage measurement accuracy than MAX11068 and the data rate range of LTC6804 is greater than MAX11068. Therefore, the designers should select the right BMS EVKit based on their requirements.

To use MAX11068 with super capacitor we had to find a way to give extra 24V fully independent power supply for each board. For this situation we connect the power supply to DCIN pin and AGND pin. We took off the jumper JU131 and J132 to avoid the ground connection problem. Another point is we used java to configure the system

to read voltage and state of charge .it much easier to configure LTC systems than MAXIM. Even MAX11068 is no more available in the market. From all of the explanation we can clearly say LTC is much better than MAXIM to monitor capacitive power management unit.

5. SOFTWARE INFRASTRUCTURE

Purpose of designing our own GUI is to provide more flexibilities and options than MAXIM software. Measurement data record to excel, easy to use the software and SOC calculation .The main platform of software structure includes several sections and all these sections are finally express the total functionality of the Super cap power management unit. The prime findings of software structure are capacitor voltage, state of charge of capacitor, capacity status of the capacitor. Also voltage and state of charge statistic curve of the capacitor, total voltage and state of charge of the whole capacitors based on the voltage and stage of charge of the capacitor. We created excel data sheet where we record voltage and state of charge of the capacitor including number of measurements, date and time. The following figure illustrates the Graphical User Interface of 48volt Super capacitor PMU.

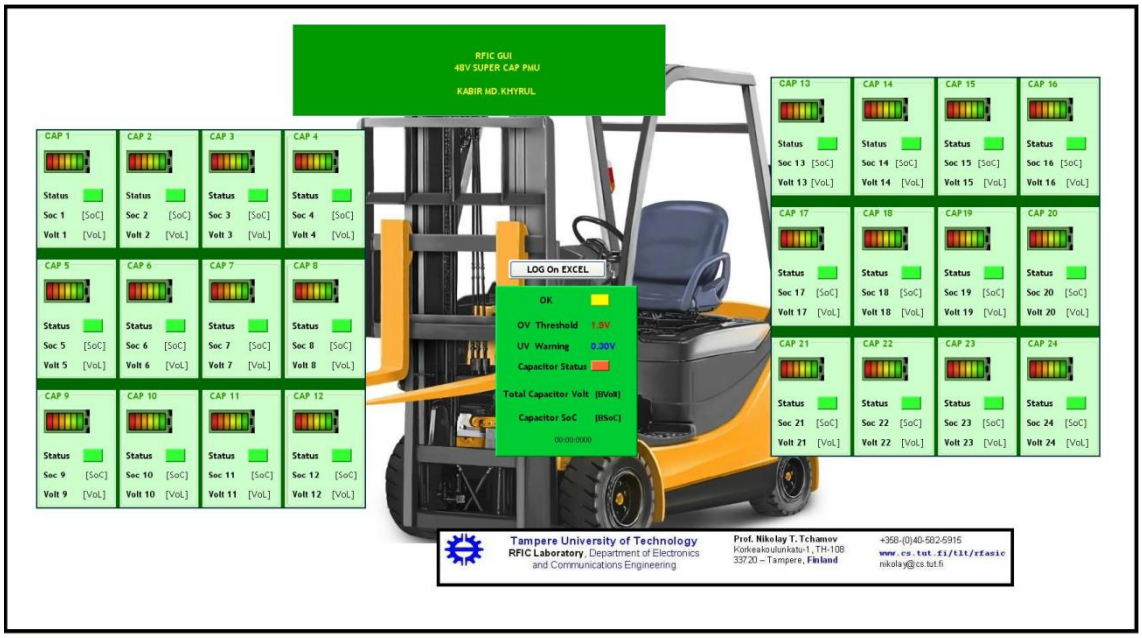


Figure 5.1: GUI of the 24 Cells Power Management System.

For 48 Volt power management units, we used 24 capacitors pack. Every cells showing status icon of the capacitor, status colour, state of charge of the capacitor, voltage of the capacitor. Additionally we used a jpanel to show the system is okay or not, also over and under threshold voltage. Status of the whole capacitor pack. Finally total voltage and state of charge of the pack. One jbutton we used to open the Excel file. After running the software when we will click on the Log on Excel button it will open the excel. We created a excel sheet to write the voltage, state of charge, number of measures, date and time. When we will run the software it will automatically write all these parameter on excel. To represent the statistical measurement of the capacitor, four graphs will create to express 24 capacitors voltage, state of the charge, total voltage and total SoC.

5.1. Software Demonstration Procedure

Java programming codes plays a fundamental role in our thesis to measure the voltage, SoC and to build the graphical user interface. Additionally we used Arduino microcontroller to overcome the I^2C communication problem. To make a reasonable communication between the CPMS and MAX11068 through Arduino .we had to write some additional command to start up Arduino and then turn on the CPMS. All the command we got from MAX11068 data sheet. Calculation of packet error checking (PEC) is necessary to improve the data accuracy. We have several classes to make the total GUI. USB communication to communicate with capacitor power management unit and computer, Excel sheet to record the data, creating GUI to show the update of the data, graphs are to express the characteristics of cell voltage and SoC and finally a main class to run the whole programme.

5.2. Assessment of Capacitor Voltage

Cell enabled (CELLEN) register address is 0x09 and ADC configuration (ADCCFG) register address 0x08. Cell voltage assessment is done in two steps, it starts with raw cell voltage acquisition where ADC scans all enabled cell input channel from highest cell. In the next stage correction phase of the channel scanning by utilizing a front end amplifier which is cut out the offsets and induced errors. In consequence we are getting high accuracy result. The channels are also converted in highest to lowest order as same in the input measurement. Because of I^2C command there is a communication delay from module to module. Through the double scan process ADC data is offset errorless, averaged and updated to cell data register. Full measurement is done in across each cell with the high speed 12-bits consecutive ADC. ADC is used to digitalize the cell voltage and maximum speed range is (0 – 0.5V). It's possible to measure 12 cells within 107μs. All the cell measurement command based on MAX11068 data sheet. Based on MAX11068 datasheet we can calculate the each cell voltage.

Maximum 12 data bits =4096

Capacitor Voltage$= \frac{ADC(Out)\times 5}{4095}$

Each cell voltage recorded in excels and also updated in GUI. Later on this voltage used to estimate SoC and for the characteristics curve.

5.3. Assessment of State of Charge (SoC)

States of the charge of the capacitors are divided into five steps. State of charge of the capacitor will change the icons according to different percentage of charge. Following

figure represent the icon when the capacitor 100% full. So it means the charge of the capacitor is good.

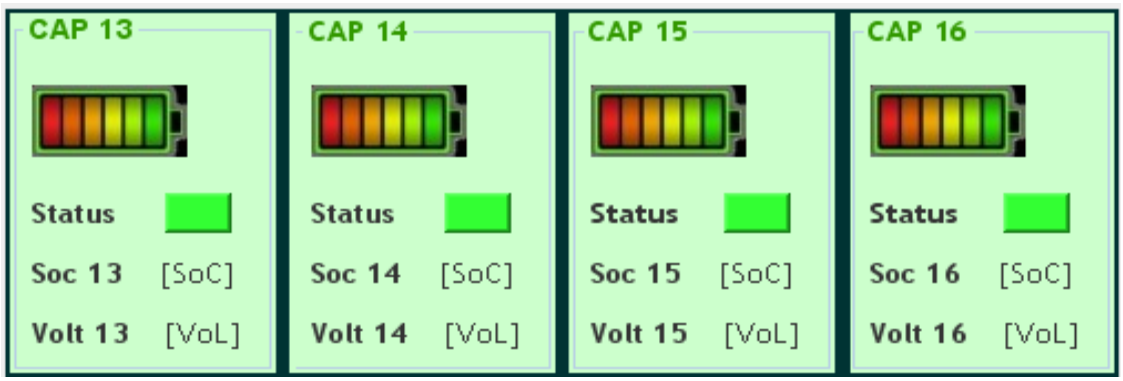


Figure 5.2: Icons when state of charge 80% to 100%.

At this stage when the charging will start to decrease and become below than 80% the following icon will show up and capacitor charge is not bad still good.

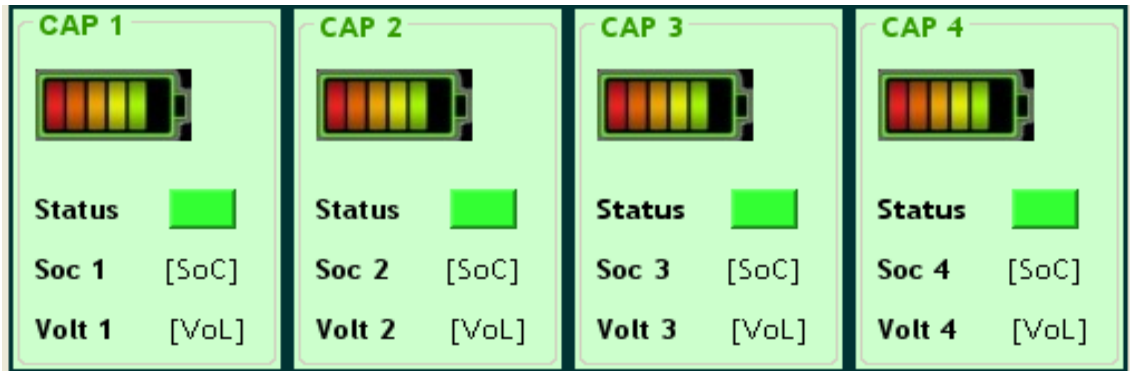


Figure 5.3: Icons when state of charge 50% to 79%.

Further decreasing of the charge will change the icon again when it's lower than 50% and icon will stay until 30% of the charge. This step is the first state of bad condition.

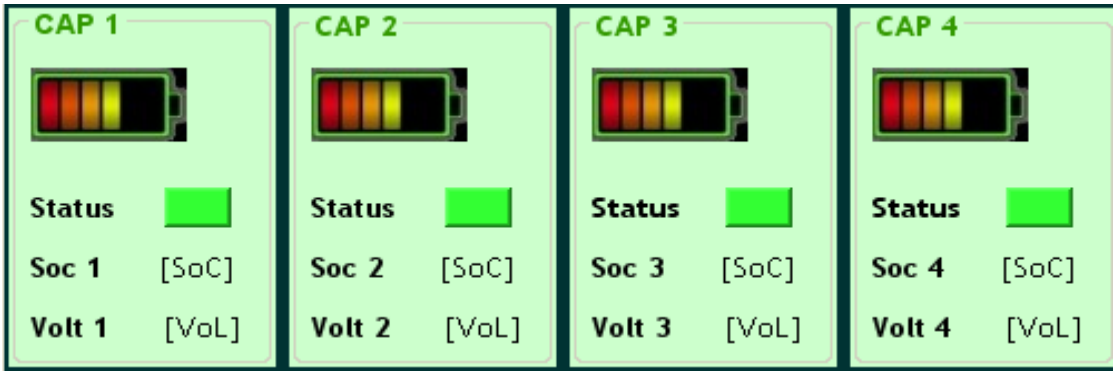


Figure 5.4: Icons when state of charge 30% to 49%.

Following icons are for charging state between 5% to 29Ä%. This state provides the icon state din below to charge the capacitor. It's the warning situation

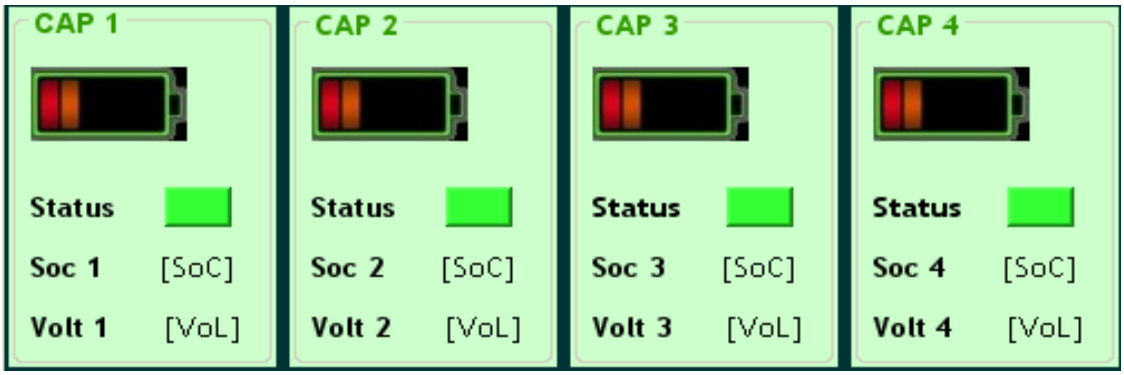


Figure 5.5: Icons when state of charge 5% to 29%.

When the charging stage of the capacitor is nearly zero the following icon will show up after this state capacitor will enter in dead zone.

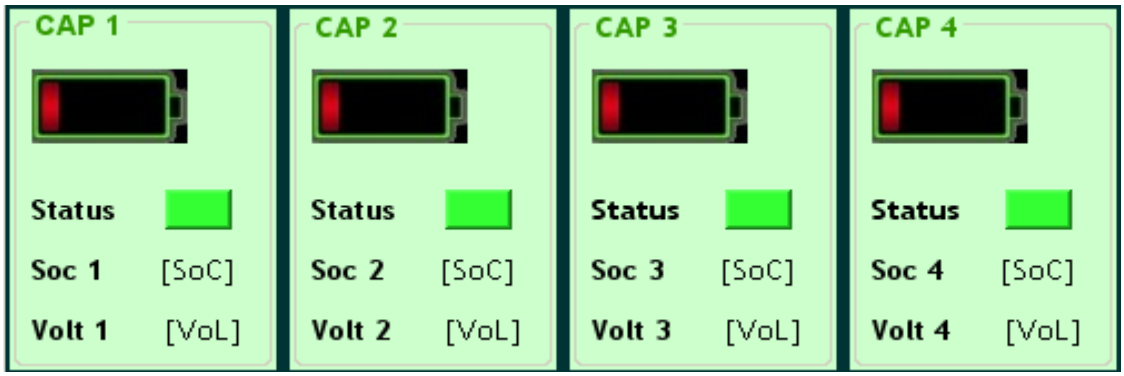


Figure 5.6: Icons when state of charge 5% to 29%.

The represented SoC calculations are just approximate value. To find the whole SoC of the capacitor pack, total SoC is divided my 24 (total number of capacitor). Individual SoC of each capacitor we calculate from capacitor voltage using java program. Initially 24 capacitor's value stored in 24 arrays after that SoC estimated from those 24 arrays. The icons of the cell change according to the following estimation.

Table 5.1: SoC Estimation Ranges.

Capacitor Voltage	SoC
1.9-2.0	95%
1.8-1.9	90%
1.7-1.8	85%
1.6-1.7	80%
1.5-1.6	75%
1.4-1.5	70%
1.3-1.4	65%
1.2-1.3	60%
1.1-1.2	55%
0.90-1.1	50%

0.80-0.90	45%
0.70-0.80	40%
0.60-0.70	35%
0.50-0.60	30%
0.40-0.50	25%
0.30-0.40	20%
0.20-0.30	15%
0.10-0.20	10%
0.05-0.10	5%

5.4. Measurement Data Updated on GUI

The graphical user interface (GUI) is representing the updated data during the measurement. In the programming the cell voltage and SoC are stored in arrays namely *CapacitorVoltage* and *StateOfCharge.* To represent the cell voltage and SoC we used individual jLabel. We used update function in the existing source code to update the data every time during the measurement.

Figure 5.7 :Updated GUI.

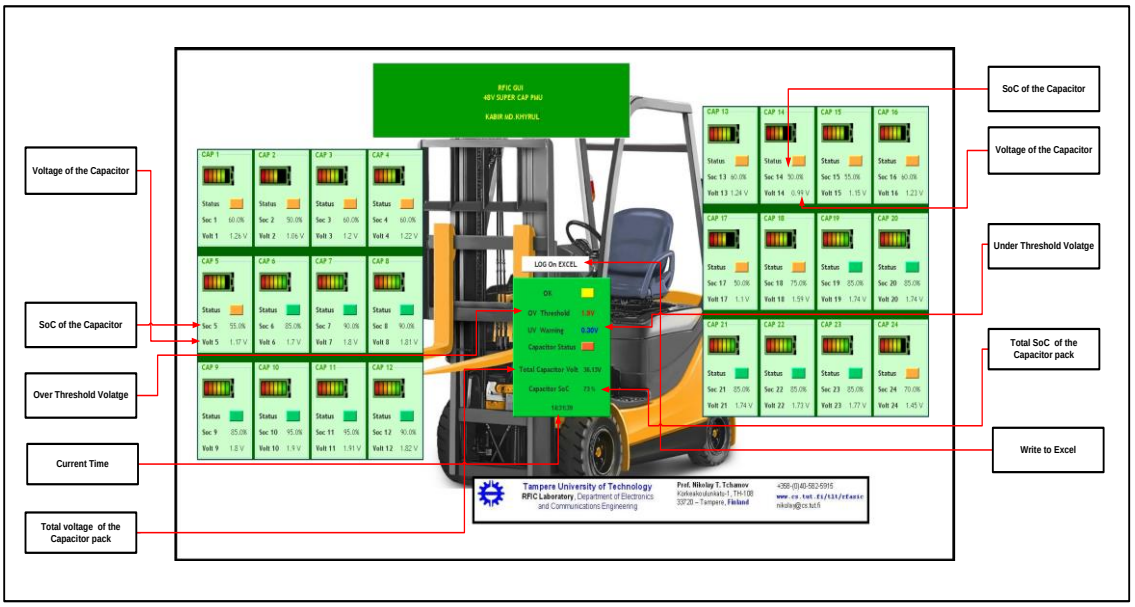
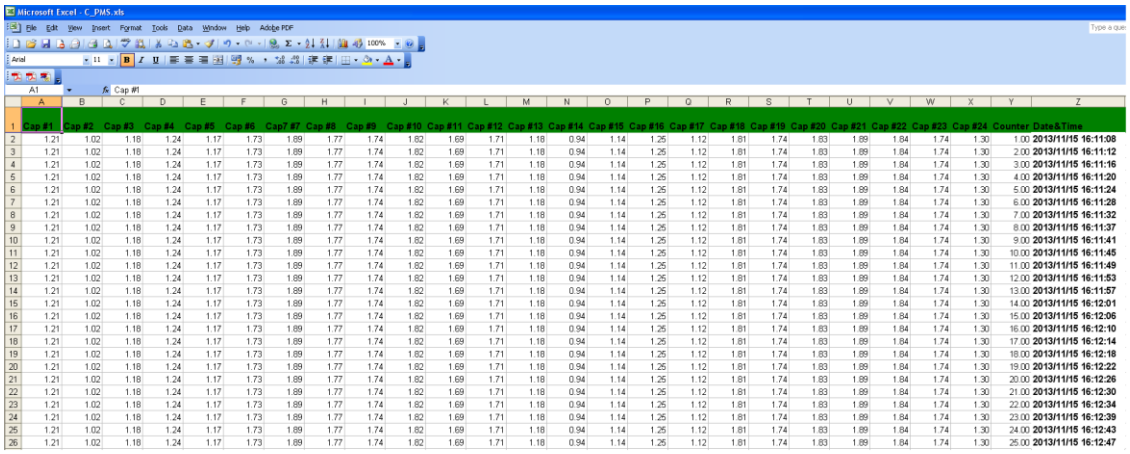


Figure 5.8 : Updated GUI with Indication.

From the presented pictures above we can easily notice that all measurement data including each capacitor cell voltage, state of charge, date, over threshold voltage. Under voltage warning and then total capacitor pack voltage and state of charge is updated. If we consider the capacitor number two voltages is 1.07V and state of charge according to state of charge estimation range is 55%. Then for capacitor number 14 the voltage is 0.99V and state of charge is 55%. Like this all capacitor voltage is updated. Finally total capacitor pack voltage is 36.13Volt and S0C is 73%.

5.5. Measurement Data Updated on Excel

Like GUI measurement data also recorded to Excel sheet. The following excel is for recording the individual capacitor voltage. Here 24 capacitor voltages with equal number of measurement counter. Each capacitor voltage stated with respected date and time slot.



Cap #1	Cap #2	Cap #3	Cap #4	Cap #5	Cap #6	Cap7 #7	Cap #8	Cap #9	Cap #10	Cap #11	Cap #12	Cap #13	Cap #14	Cap #15	Cap #16	Cap #17	Cap #18	Cap #19	Cap #20	Cap #21	Cap #22	Cap #23	Cap #24	Counter	Date&Time
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	1.00	2013/11/15 16:11:08
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	2.00	2013/11/15 16:11:12
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	3.00	2013/11/15 16:11:16
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	4.00	2013/11/15 16:11:20
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	5.00	2013/11/15 16:11:24
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	6.00	2013/11/15 16:11:28
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	7.00	2013/11/15 16:11:32
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	8.00	2013/11/15 16:11:37
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	9.00	2013/11/15 16:11:41
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	10.00	2013/11/15 16:11:45
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	11.00	2013/11/15 16:11:49
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	12.00	2013/11/15 16:11:53
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	13.00	2013/11/15 16:11:57
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	14.00	2013/11/15 16:12:01
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	15.00	2013/11/15 16:12:06
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	16.00	2013/11/15 16:12:10
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	17.00	2013/11/15 16:12:14
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	18.00	2013/11/15 16:12:18
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	19.00	2013/11/15 16:12:22
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	20.00	2013/11/15 16:12:26
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	21.00	2013/11/15 16:12:30
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	22.00	2013/11/15 16:12:34
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	23.00	2013/11/15 16:12:39
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	24.00	2013/11/15 16:12:43
1.21	1.02	1.18	1.24	1.17	1.73	1.89	1.77	1.74	1.82	1.69	1.71	1.18	0.94	1.14	1.25	1.12	1.81	1.74	1.83	1.89	1.84	1.74	1.30	25.00	2013/11/15 16:12:47

Figure 5.9 : Excel Sheet for Capacitor pack with Voltages, Date and Time

Here another Excel sheet for storing SoC of 24 capacitor.

AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	AL	AM	AN	AO	AP	AQ	AR	AS	AT	AU	AV	AW	AX
SoC #1	SoC #2	SoC #3	SoC #4	SoC #5	SoC #6	SoC #7	SoC #8	SoC #9	SoC #10	SoC #11	SoC #12	SoC #13	SoC #14	SoC #15	SoC #16	SoC #17	SoC #18	SoC #19	SoC #20	SoC #21	SoC #22	SoC #23	SoC #24
55.00	45.00	50.00	55.00	50.00	90.00	90.00	90.00	85.00	90.00	85.00	90.00	55.00	45.00	50.00	55.00	50.00	90.00	90.00	90.00	85.00	90.00	85.00	90.00
55.00	45.00	50.00	55.00	50.00	90.00	85.00	90.00	85.00	90.00	90.00	85.00	55.00	45.00	50.00	55.00	50.00	90.00	85.00	90.00	85.00	90.00	90.00	85.00
55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	85.00	90.00	90.00	80.00	55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	85.00	90.00	90.00	80.00
55.00	50.00	55.00	60.00	55.00	85.00	90.00	90.00	85.00	85.00	85.00	60.00	55.00	50.00	55.00	60.00	55.00	85.00	90.00	90.00	85.00	85.00	85.00	60.00
55.00	50.00	55.00	60.00	50.00	85.00	85.00	85.00	85.00	90.00	85.00	85.00	55.00	50.00	55.00	60.00	50.00	85.00	85.00	85.00	85.00	90.00	85.00	85.00
55.00	50.00	55.00	60.00	50.00	90.00	90.00	85.00	90.00	85.00	85.00	85.00	55.00	50.00	55.00	60.00	50.00	90.00	90.00	85.00	90.00	85.00	85.00	85.00
55.00	50.00	55.00	60.00	50.00	90.00	90.00	90.00	90.00	85.00	90.00	80.00	55.00	50.00	55.00	60.00	50.00	90.00	90.00	90.00	90.00	85.00	90.00	80.00
55.00	50.00	55.00	60.00	50.00	90.00	85.00	85.00	90.00	90.00	90.00	90.00	55.00	50.00	55.00	60.00	50.00	90.00	85.00	85.00	90.00	90.00	90.00	90.00
55.00	50.00	55.00	60.00	50.00	90.00	85.00	85.00	85.00	85.00	85.00	85.00	55.00	50.00	55.00	60.00	50.00	90.00	90.00	85.00	85.00	85.00	85.00	85.00
55.00	50.00	55.00	60.00	50.00	90.00	85.00	95.00	85.00	85.00	90.00	70.00	55.00	50.00	55.00	60.00	50.00	90.00	85.00	95.00	85.00	85.00	90.00	70.00
55.00	50.00	55.00	60.00	50.00	90.00	85.00	90.00	85.00	85.00	85.00	55.00	55.00	50.00	55.00	60.00	50.00	90.00	85.00	90.00	85.00	85.00	85.00	55.00
55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	90.00	90.00	90.00	90.00	55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	90.00	90.00	90.00	90.00
55.00	50.00	55.00	60.00	55.00	85.00	90.00	85.00	85.00	90.00	90.00	55.00	55.00	50.00	55.00	60.00	55.00	85.00	90.00	85.00	85.00	90.00	90.00	55.00
55.00	45.00	55.00	60.00	50.00	85.00	90.00	90.00	95.00	85.00	90.00	90.00	55.00	45.00	55.00	60.00	50.00	85.00	90.00	90.00	95.00	85.00	90.00	90.00
55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	90.00	90.00	85.00	90.00	55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	90.00	90.00	85.00	90.00
55.00	50.00	55.00	60.00	50.00	90.00	85.00	90.00	90.00	90.00	90.00	86.00	55.00	50.00	55.00	60.00	50.00	90.00	85.00	90.00	90.00	90.00	90.00	85.00
55.00	45.00	55.00	60.00	50.00	90.00	90.00	85.00	90.00	90.00	90.00	90.00	55.00	45.00	55.00	60.00	50.00	90.00	90.00	85.00	90.00	90.00	90.00	90.00
55.00	50.00	55.00	60.00	50.00	90.00	90.00	85.00	90.00	85.00	90.00	90.00	55.00	50.00	55.00	60.00	50.00	90.00	90.00	85.00	90.00	85.00	90.00	90.00
55.00	50.00	55.00	60.00	50.00	90.00	85.00	90.00	90.00	90.00	90.00	86.00	55.00	50.00	55.00	60.00	50.00	90.00	85.00	90.00	90.00	90.00	90.00	85.00
55.00	50.00	55.00	60.00	50.00	90.00	90.00	85.00	85.00	85.00	95.00	90.00	55.00	50.00	55.00	60.00	50.00	90.00	90.00	85.00	85.00	85.00	95.00	90.00
55.00	45.00	55.00	60.00	50.00	90.00	85.00	90.00	85.00	85.00	85.00	85.00	55.00	45.00	55.00	60.00	50.00	90.00	85.00	90.00	85.00	85.00	85.00	85.00
55.00	50.00	55.00	60.00	50.00	85.00	85.00	90.00	90.00	90.00	95.00	90.00	55.00	50.00	55.00	60.00	50.00	85.00	85.00	90.00	90.00	90.00	95.00	90.00
55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	90.00	90.00	85.00	85.00	55.00	50.00	55.00	60.00	50.00	85.00	90.00	85.00	90.00	90.00	85.00	85.00
55.00	50.00	55.00	60.00	50.00	85.00	85.00	90.00	90.00	85.00	85.00	85.00	55.00	50.00	55.00	60.00	50.00	85.00	85.00	90.00	90.00	85.00	85.00	85.00
55.00	50.00	55.00	60.00	55.00	90.00	85.00	90.00	90.00	90.00	85.00	60.00	55.00	50.00	55.00	60.00	55.00	90.00	85.00	90.00	90.00	90.00	85.00	60.00

Figure 5.10 : Excel Sheet for Capacitor pack with SoC

6. MEASURMENT SETUP AND RESULTS

System structure mainly composes of connections of MAX11068 with capacitor pack. Configuration main done with MAX11068 demo board and 24 series connected aluminium electrolytic capacitor to produce 48V voltage. Capacitor has the capacity up to 63V and capacitance 10000uF. So generally we can assume this capacitor's characteristics are almost as super capacitor.

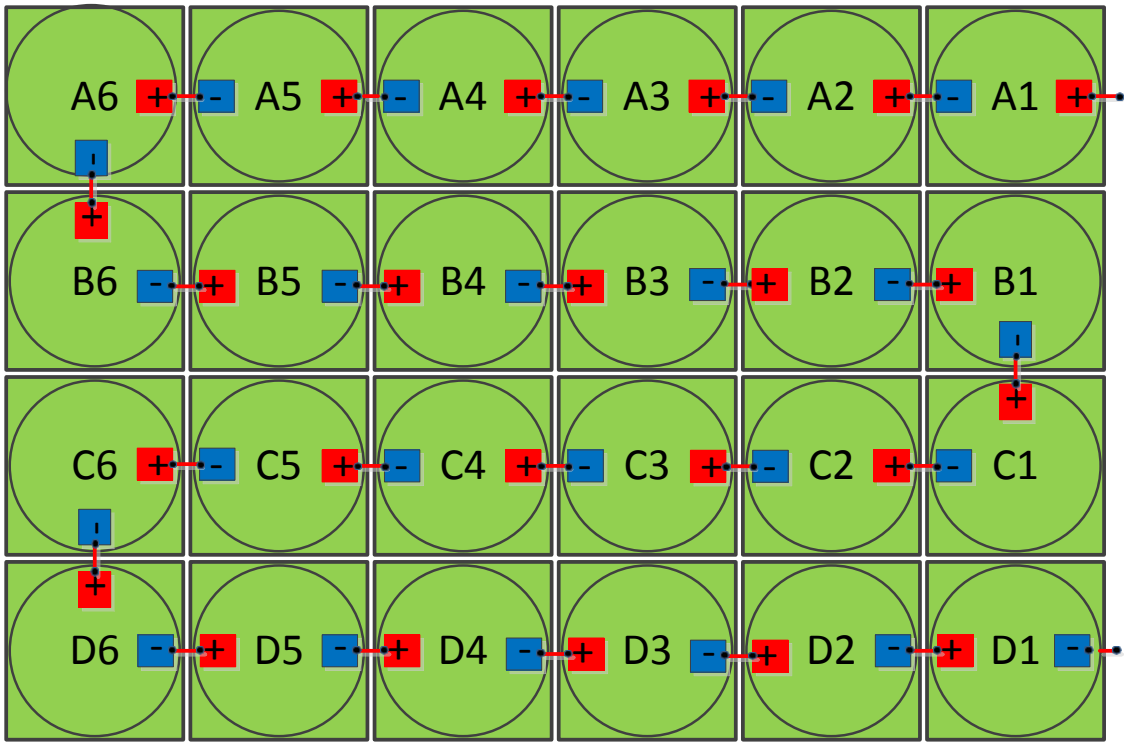


Figure 6.1: 24 Capacitor pack.

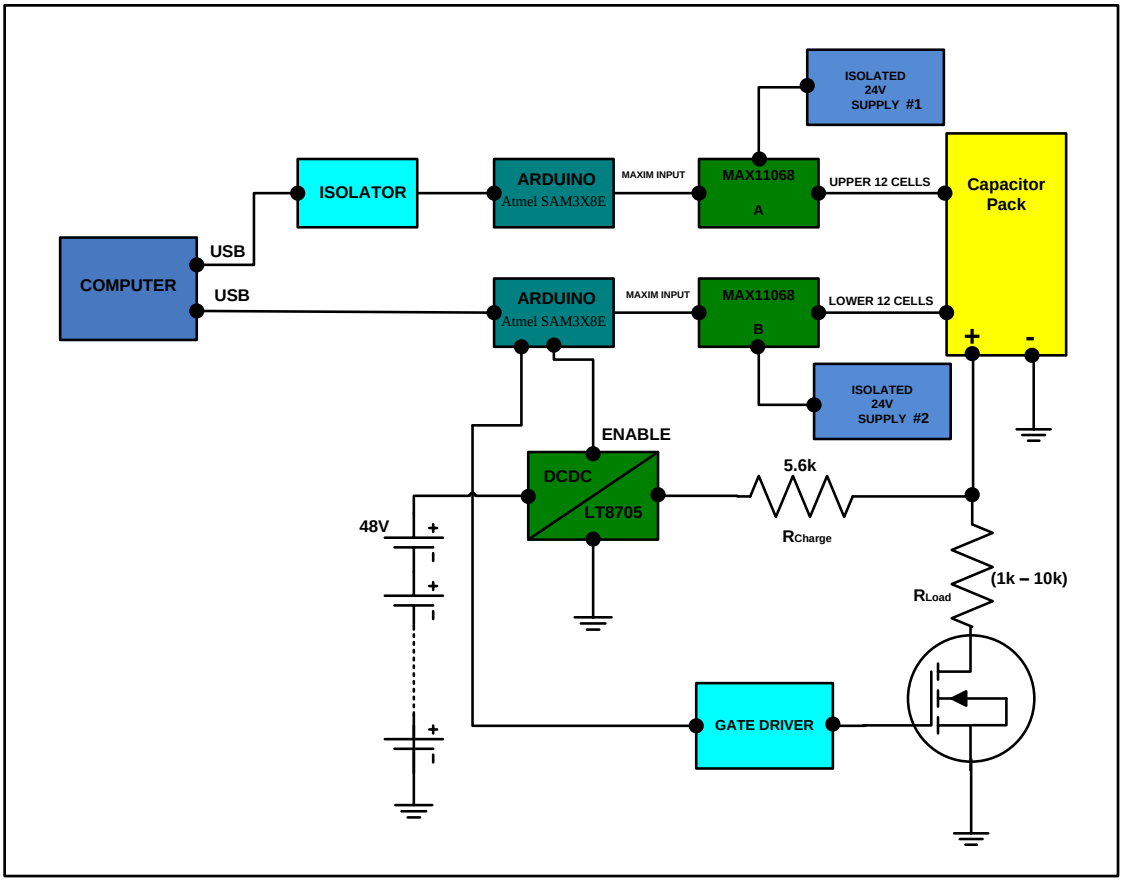


Figure 6.2: Whole PMU System Architecture.

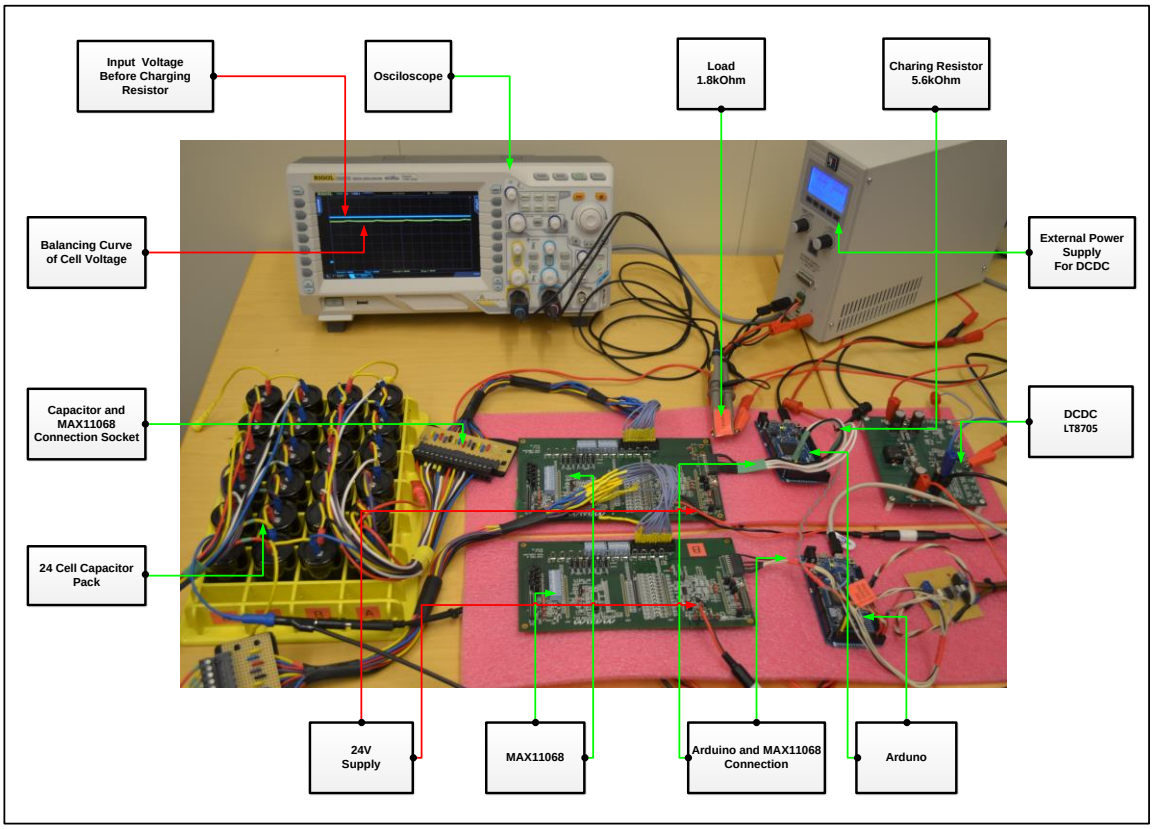


Figure 6.3: PMU System Set up

Connection socket between capacitor pack and MAX11068 is capable of 48V supply with .05A current to limit the supply to avoid any short circuit though it's not taking too much power. This supply is connected to the DCDC.

Nothing important but the low side gate driver can be used in 3.3V I/O pin can be replaced by a simple transistor or circuit to get 5V or something like that. The main purpose of the gate driver to get bit more gate voltage bigger than threshold (2V/3V) voltage to turn on the Arduino. Primary plan was to use this gate driver as high side gate driver but this driver based on bootstrap circuit like it takes the high voltage and when switching happens then pushes the capacitor voltage to gate voltage .5V is the gate or source voltage at this point but the capacitor voltage it lasts only 10ms after it drops so gate voltage also goes gets down. So this high side gate driver only works with PVM signal but we are not using PVM signal.

We used two individual microcontrollers to configure the MAX11068. In the following paragraph we described briefly the main features and functionality of Arduino Due (Atmel SAM3X8E).

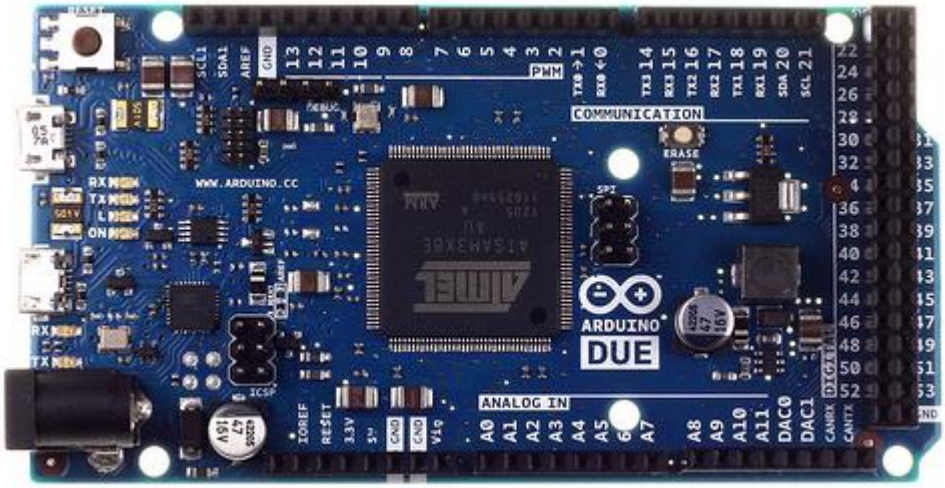


Figure 6.4 :Arduino Due Front View[16].

This microcontroller is a version of Atmel SAM3X8E ARM Cortex-M3 CPU. Its the primary 32-bit ARM core microcontroller. Consists of 54 digital input/output pin, 12 analog input, 4 UARTs,2 TWT, a power jack, an SPI header, an USB OTG capable connection, a 84MHz clock, a JTAG header, a reset button and erase button. Maximum operating voltage 3.3V. Simple connection can be established through USB cable and AC to DC adapter or battery.

ARM core has several advantages

- 32-bit core processor with 4 bytes wide data operation with single CPU clock.
- 84MHZ CPU Clock.
- SRAM with 96 Kbytes capabilities.
- Flash memory with 512 Kbytes code.
- Able to relieve CPU from memory intensive tasks because of DMA controller.
-

Table 6.1 : Features of Arduino Microcontroller [16].

Microcontroller	AT91SAM3X8E
Operating Voltage	3.3V
Input Voltage (Recommended)	7-12V
Input Voltage (limits)	6-16V
Digital I/O Pins	54 (of which 12 pins provide PWM output)
Analog Input Pins	12
Analog Output Pins	2 (DAC)
Total DC output current on all I/O lines	130mA
DC Current for 3.3V Pin	800mA
DC Current for 5V Pin	800mA
Flash Memory	512 KB all available for the user SRAM
SRAM	96 KB (two banks : 64 KB and 32 KB)
Clock Speed	84MHz

Power

Power connection established by USB with external power supply, will choose automatically. External power supply can be AD to DC adapter or battery. A 2,1mm centre positive plug into board's power jack is used to make the adapter connection. Through the headers of the power connector Gnd and Vin pin can be connected, operating voltage of the board is between 6V to 20V. Supply less than 7V board makes the board unstable, Supply more than 12V can damage the board. Recommended range is 7V to 12V.

Memory

512bKB flash memory storing code. Atmel has boot loader in pre burned factory. It has also dedicated ROM memory. Available 96KB SRAM memory. Direct accessible available memories (Flash, RAM and ROM). By pressing erase button flash memory can be deleted. This deletion will delete loaded sketch from the MCU.

Input and Output

- Digital I/O pins from 0 to 53

Each of the 54 pins possible to use as input or output by using the pinMode(), digitalWrite() and digitalREAD functions. Operating voltage is 3.3V. Capable to provide 3mA to 15mA source current, 6mA 0r 9mA receive current. Consist of 100k**Ω** pull up resistor.

- Serial: 0 (RX) and 1 (TX)
- Serial 1: 19 (RX) and 18 (TX)
- Serial 2: 17 (RX) and 16 (TX)
- Serial 3: 15 (RX) and 14 (TX)

This pin used to receive (RX) and transmit (TX) TTL serial data with 3.3V level. Pins 0 and 1 are tied up with corresponding pin of the ATmega16U2 USB to TTL serial chip.

- PWM : Pins 2 to 13

Able to provide 8-bit PWM output with analogWrite() function. analogWriteResolution() function is capable to change PWM function.

- SPI :

With SPI library this pins provides communication. Divided into central 6 pin header. Without programming this SAM3X ,SPI can be used to communicate with other SPI device.

- CAN : CANRX and CANTX

Supportive pin for CAN communication but not for Arduino APIs.

- "L" LED : 13

Built in LED attached to 13 no pin. LED is ON when the pin is HIGH and its OFF when the pin is LOW. With the PWM output LED can be made as dim.

- TWI 1: 20 (SDA) and 21 (SCL)
- TWI 2: SDA1 and SCL1

Using Wire library establish TWI communication

- Analog Inputs: pins from A0 to A11

Because of 12 analog pins it can provide 12 bits of resolution. 10 bit resolution defines by default setting to make compatible with other Arduino boards. More than 3.3V supply to this pin can damage the SAM3X chip because analog pin estimate from ground to a maximum value of 3.3V.

- DAC1 and DAC2

Deliver 12 bits resolution with true analog output and analogWrite() function. Using audio library can provide audio output.

- AREF

Reference voltage for the analog inputs with analogReference() function.

- Reset

Makes the line LOW to reset the microcontroller. Additional reset button to shields which block the one on the board.

Communication

Numerous numbers of functionalities to communicate with computers, another Arduino or other microcontroller and also phones, tablets and cameras. Its provide one hardware UART and three hardware USARTs for TTL (3.3V) serial communication. ATmega16U2 port connected to programming pin which is providing a virtual COM port to software on a connected computer. 16U2 also connected to the SAM3Xhardware UART. Serial on pins RXO and TXO provides serial to USB communication to ATmega16U2 microcontroller programming. Data can be sending and received from the board through serial monitor software. During the data transmitted TX and RX LEDs on the board will flash. Native USB provides the CDC communication over USB. This makes a serial connection to the serial monitor or other commuter applications. Native USB port can act as USB host for connecting mice, keyboards and smartphones.

Programming

Downloaded Arduino software typically used for programming. Re programming is necessary for different AVR microcontroller to erase the flash memory. Upload to the chip is organized by ROM on the SAM3X. Run with the empty flash memory.

Two Arduino used to configure the two of MAX11068 individually. In MAXIM there are so many ground levels (JU31, JU3, JU131 and JU132) and the timing difference between two board is problematic. The upper board IC (U1) is work as charge pump and it (lower board) will take the reference of the upper board for ground level and pum up to 3.4V. With one microcontroller the voltage was higher at that point so the reference was not working. So we had to use with two isolated 24 power supply source and two Arduino. For using the reference we had to disconnect the ground (JU31, JU3, JU131 and JU132) to avoid sparks. But with disconnecting ground there is no reference anymore for communication port. So we choose two Arduino to solve the reference problem. Though it’s complicated solutions for simple problem.

Here we used one 4-Switch buck boost DC/DC (LT-8705) Converter. This DC/DC converter is able to operate at below, above and equal to the input voltage. Useful with solar system, automotive, telecom and battery powered systems. Input range is 2.8V to 80V and wide output range is 1.3V to 80V. Consist of Quad N channel MOSFET Gate drivers and synchronization rectification is up to 98% efficiency. Also has input and output current monitor pins and 100kHZ to 400kHZ frequency range. Feedback loop including input current and voltage, output current and voltage [18].

DCDC Converter: to provide constant voltage source. Mainly used for automated system flexibility and many measurement. Easier to compare results. Enable (SWEN) pin is to turn on the DCDC converter (can work from 20V to 80V but we are using 48V). By manually and also by sending command to Arduino we can turn on the DCDC [18].
Charging resistor is preferred to 5.6k because of the small capacitor cell. Because if we choose much lower than this value the capacitor would charge up so fast so if we use this resister then capacitor will charged up moderately so we will have some time to make the test bench(take measurement). Load resistor 1.8k is because of fast discharge as charging resistor.

For Discharge current since we don't have any automated current sensor we have only option using mulitimeter or hand held calculation. We can estimate the rate of discharge of the cell (from voltage versus time graph) and then get capacitance of the capacitor and finally from the charging resistor we can indirectly calculate the discharging current.
For balancing we are using only internal MAX11068 circuit. Capacitor voltage can't go more than 1.9V. Problem is that we are using 24V external power supply and because of MAX11068 the accuracy is limited. Because of biasing of the MAXIM it can't go more than 1.9V.Because of the ground difference between Arduino and MAXIM we used isolator. Also the USB ground remains same. To avoid the sparks we had to isolate the ground from each other. Without the isolator the MAXIM chip might break.

6.1. Balancing of Capacitor Cell Voltages

The following flow chart is stating the three important performance characteristics of the capacitor pack. Those are cell charging, cell discharging and cell balancing. First of all start with charging of the cell which is controlled by the conditions of cell under voltage level and maximum threshold level. The under voltage is lowest level and threshold voltage is out of range then charging enabled. According to the MAX11068 configuration charger wait up 20ms to read the cell voltage is reach the Over voltage level then the charging system switch to cell balancing scheme or if cell voltage below than OV then return to wait 20ms to again read the OV. Cell balancing scheme is first

turn of the charger then check the cell voltage level, if the minimum voltage close to OV then its switch to cell discharging scheme. If lowest voltage not close OV then enabled the cell balancing resistor when cell voltage is not within a threshold from lowest voltage. Then its wait 20ms to read voltage if it's still out of threshold then switch to cell charging, if no then enabled the cell balancing resistor. When cell balancing switch to cell discharge section which also wait 20ms then read the voltage if it reach UV then turn on cell charging or if cell voltage more than UV then wait 20ms to read the voltage again.

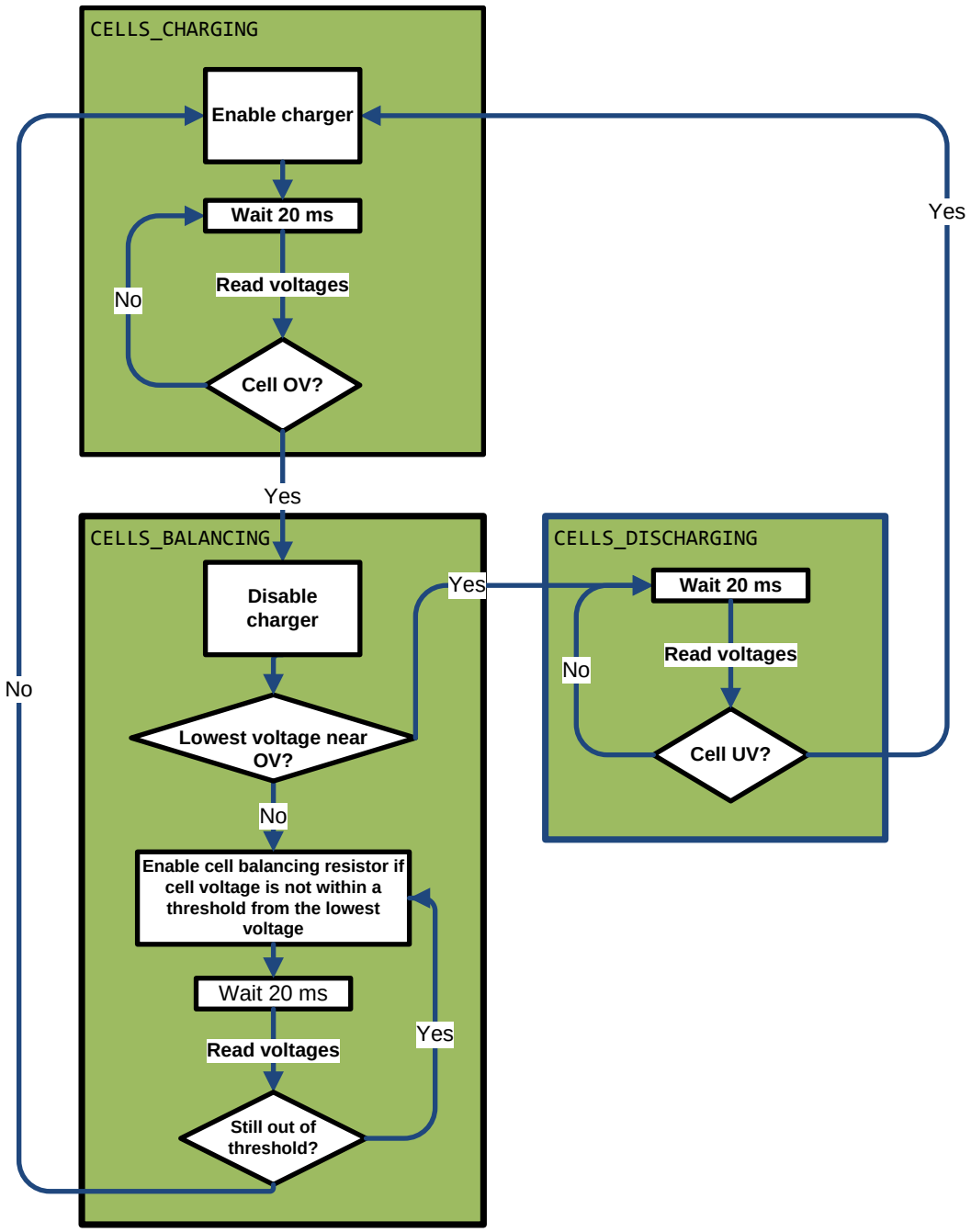


Figure 6.4 : Balancing Flow Chart [8].

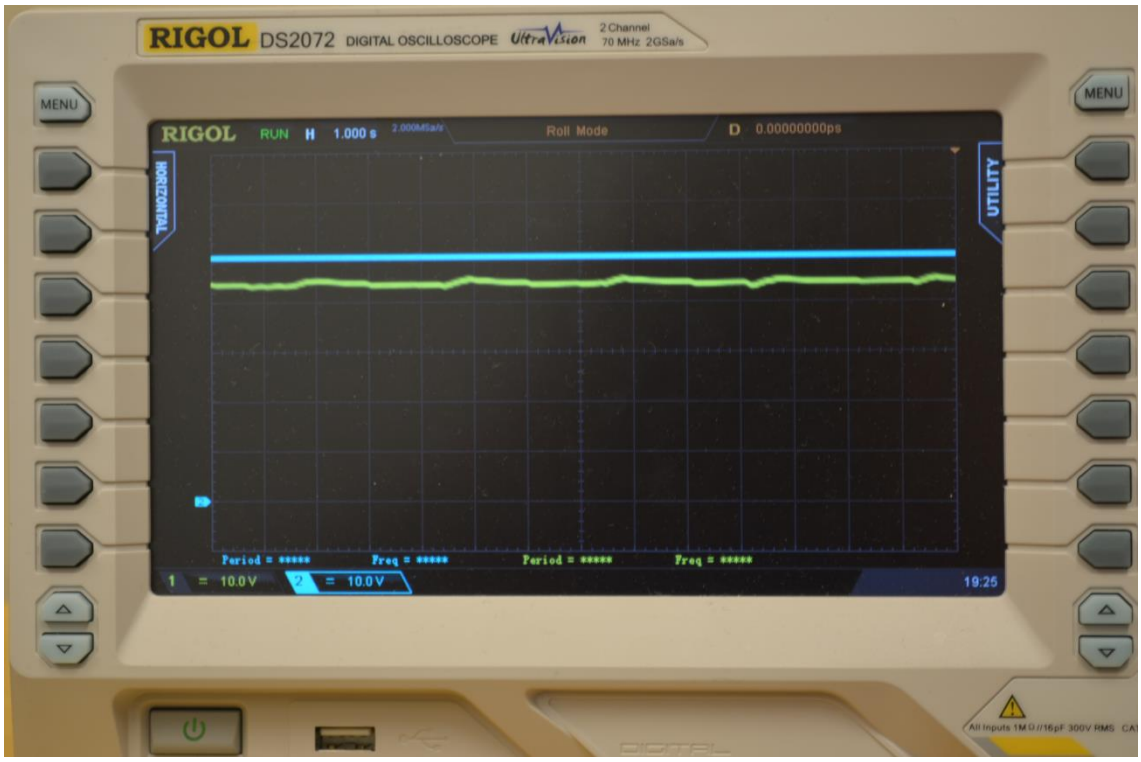


Figure 6.5 : Balancing Curve.

From the oscilloscope wave form we can easily distinguish the charging and balancing difference. First curve (blue) is the voltage going in the capacitor before charging resistor. Yellow curve is after balancing according to the MAX11068 balancing system after every 20ms it's balancing the cell voltage if there is any voltage is reach to OV between the all 24 cells.

6.2. System Configuration

According to the MAX11068 Evaluation System here are the entire jumpers and headers configuration

Table 6.2: Jumpers JU2-JU11 and JU102-JU111 Description [8].

No. of Cells	Shunt Position									
	JU2 JU102	JU3 JU103	JU4 JU104	JU5 JU105	JU6 JU106	JU7 JU107	JU8 JU108	JU9 JU109	JU10 JU110	JU11 JU111
2	On	On	On	On	On	On	On	On	On	On
3	Off	On	On	On	On	On	On	On	On	On
4	Off	Off	On	On	On	On	On	On	On	On
5	Off	Off	Off	On	On	On	On	On	On	On

6	Off	Off	Off	Off	On	On	On	On	On	On
7	Off	Off	Off	Off	Off	On	On	On	On	On
8	Off	Off	Off	Off	Off	Off	On	On	On	On
9	Off	Off	Off	Off	Off	Off	Off	On	On	On
10	Off	Off	Off	Off	Off	Off	Off	Off	On	On
11	Off	Off	Off	Off	Off	Off	Off	Off	Off	On
12	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off

*P103 has same cell connection as P3.

Table 6.2: Headers P3 and P103 Connections [8].*

CELL	+TERMINAL	-TERMINAL
1	P3-2	P3-4
2	P3-4	P3-6
3	P3-6	P3-8
4	P3-8	P3-10
5	P3-10	P3-12
6	P3-12	P3-14
7	P3-14	P3-16
8	P3-16	P3-18
9	P3-18	P3-20
10	P3-20	P3-22
11	P3-22	P3-24
12	P3-24	P3-26

6.3. Capacitor Voltage and SoC Curves

The following graph shows the voltages of the capacitors in different time slot .Due to the characteristics of the capacitor all the voltages are not equal. From the all measurement curves we can easily distinguish that it takes around 30s to produce stable the voltage level of the capacitors. Stable voltage levels are appeared after balancing the capacitor cells which is described in the previous section. If we notice capacitor number 1 indicating red colour with 1.8V. We can also observe the voltage level in different time slots. If we also consider capacitor number 19 it's consist of yellow colour with 1.6V. All the voltage is measured in real time. From the curve we can also physically identify which capacitor has which level of voltage.

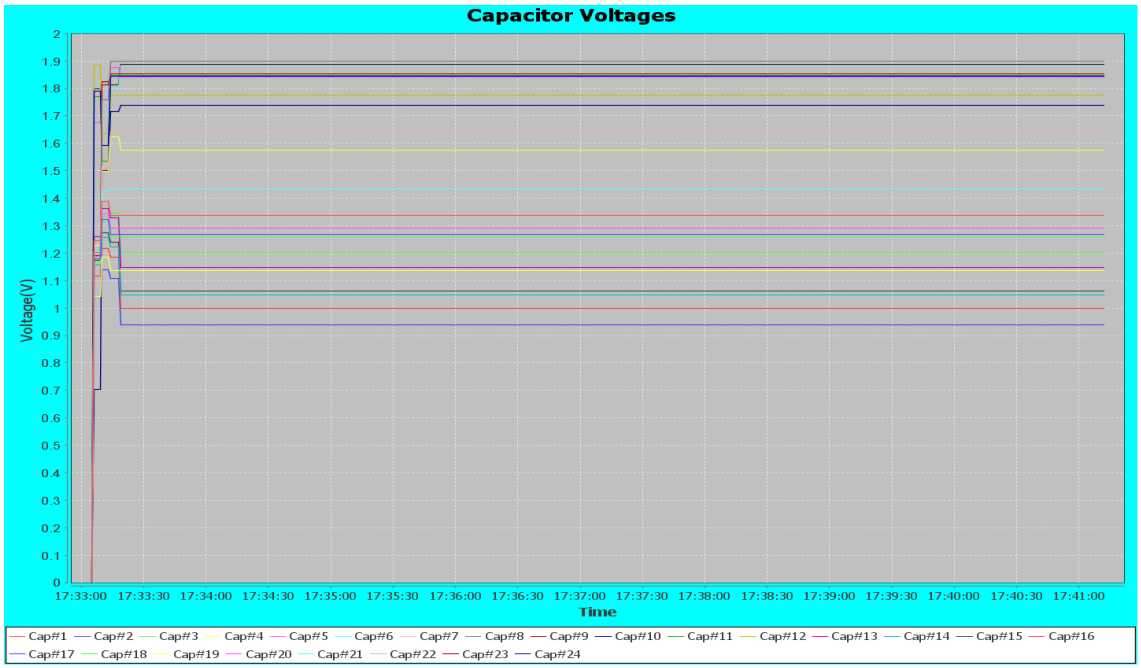


Figure 6.6 : Voltages of 24 Capacitor Cells.

The following graph shows the SoCs of the capacitors in different time slot. Different colours indicate different SoC level for different capacitors. To avoid complication of the curves we took SoC measurement for 12 capacitors. In the same way we could take SoC measurement for 24 capacitors. If we look at capacitor number 1 it's indicating red colour with SoC is 85%. Same as capacitor number 5 which showing yellow colour with 55% SoC.

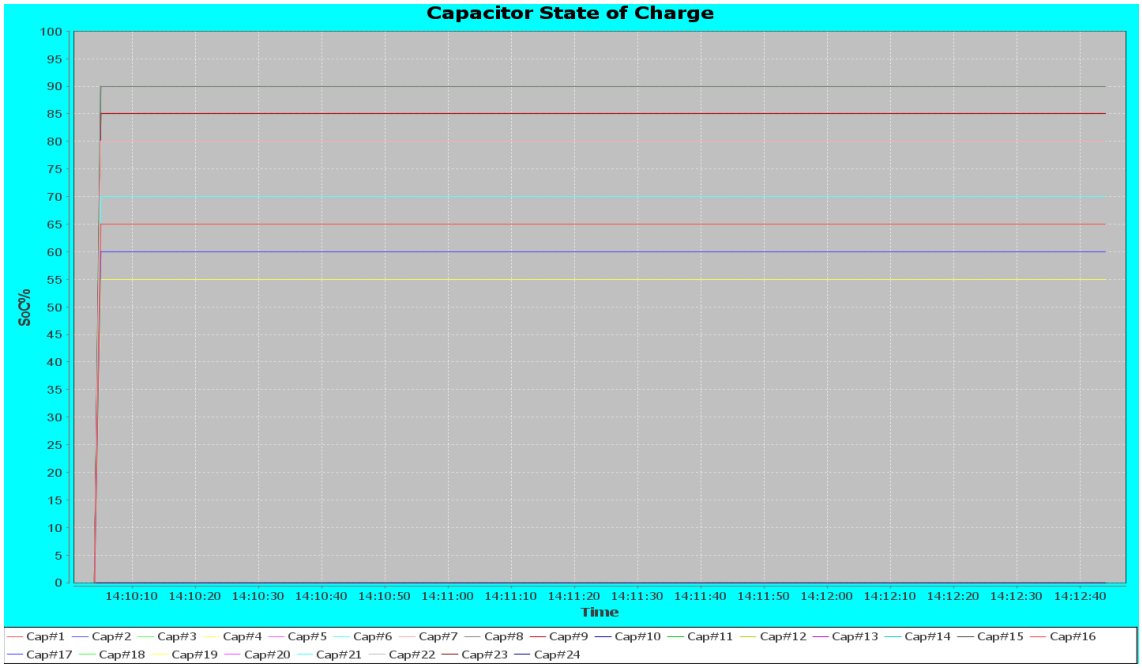


Figure 6.7 : State of Charges of 12 Capacitor Cells.

The following curve shows the total cell voltages of 24 capacitor pack in different time slot. From the figure we can see the total voltage levels of 24 capacitor cells. One line showing indicates whole pack voltage level. This voltage is sum of 24 capacitors pack which is around 32V. Due to the capacitor characteristics the voltage level is not fixed its changing every moment. we can estimate the SoC from the voltage level.

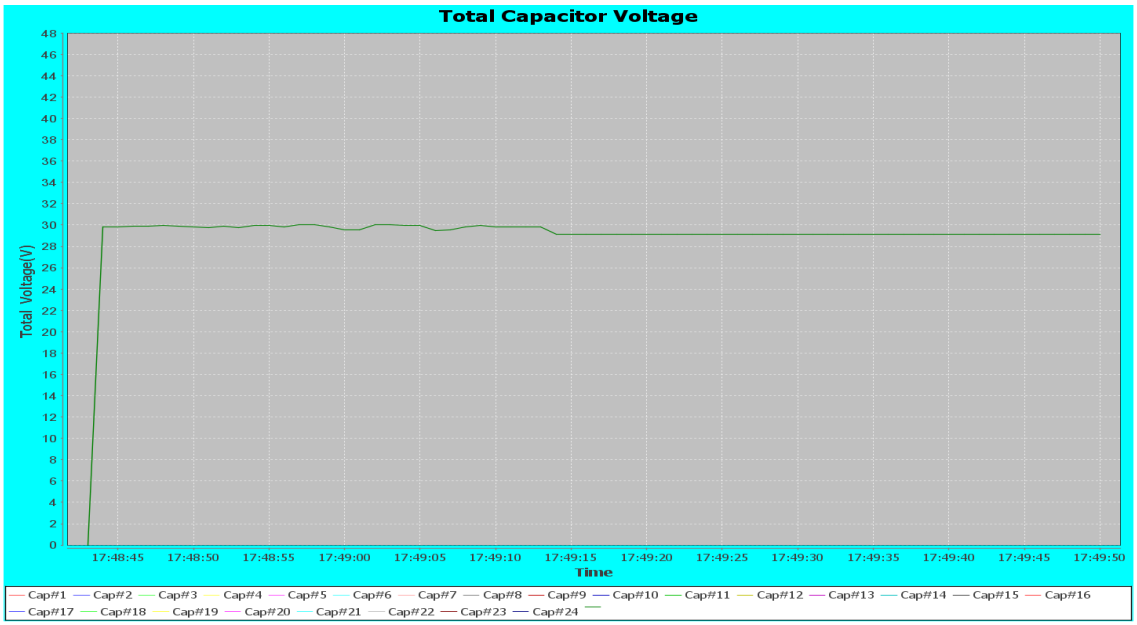


Figure 6.8 : Total Capacitor Voltage Curve.

The following curve shows the total SoC of 24 capacitor pack in different time period. From the figure we can see the total SoC levels of 24 capacitor cells. One line showing indicates whole pack voltage level. Here the SoC is around 20% because of characteristics of the capacitors. Total SoC level also varies time to time in accordance to voltage level.

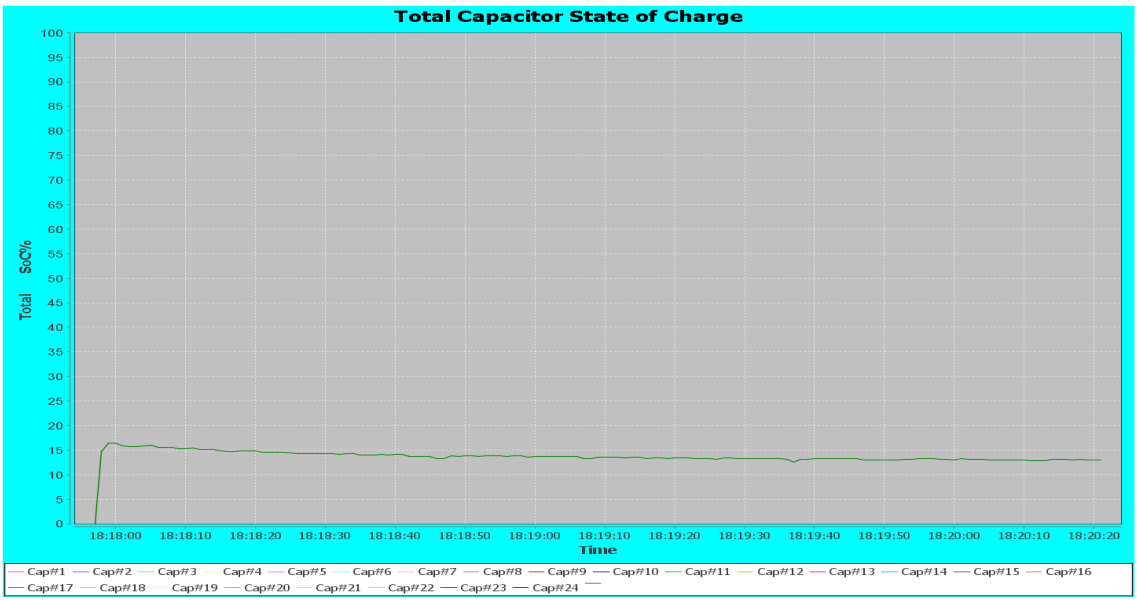


Figure 6.9 : Total Capacitor State of Charge

6.4. Result Comparison between Software and CEM DT-922 Multimeter

Capacitor voltage measurement can be tested and verified by comparing the result from software and manual measurement. From the MAX11068 data sheet we already know that the voltage measurement data of the capacitor is first stored to resister then converted by ADC and then final estimation done by voltage references. Calculated value express in decimal format. The PC then receives the calculated result to two digits after decimal point. Because of resolution and ADC error there is some differences exist between the two measurement methods. The following table shows the recorded data from GUI and CEM DT-922 multimeter at the same time [17].

Table 6.3: Real Time and Manually Measured Voltages Comparison.

Number of Capacitors	Result from GUI	Result from Multimeter
Cap1	1.26V	1.26V
Cap2	1.06V	1.05V
Cap3	1.2V	1.21V
Cap4	1.22V	1.22V
Cap5	1.17V	1.18V
Cap6	1.7V	1.71V
Cap7	1.8V	1.8V
Cap8	1.81V	1.81V
Cap9	1.8V	1.81v
Cap10	1.9V	1.9V
Cap11	1.91V	1.91V
Cap12	1.82V	1.82V
Cap13	1.24V	1.24V
Cap14	0.99V	1.0V
Cap15	1.52V	1.55V
Cap16	1.23V	1.23V
Cap17	1.10V	1.11V
Cap18	1.59V	1.60V
Cap19	1.74V	1.74V
Cap20	1.74V	1.73V
Cap21	1.74V	1.74V
Cap22	1.73V	1.73V
Cap23	1.77V	1.77V
Cap24	1.45V	1.45V

From the above result we can see that the difference between automated and manually measured result is 0.01V. Therefore, according to the analysis above, the cell voltage

measurement result of PMS can be trusted. Its measurement error compared with CEM DT-922 multimeter is in the range of 0.24% to 0.3%.

7. CONCLUSIONS

This thesis starts with characteristics and background explanation of Super capacitor. Detailed description about Aluminium electrolytic capacitor. Measurement setup including MAX11068 interface board, voltage and state of charge measurement of 24 capacitor pack .Main achievement is MAX11068 working for super capacitor cell with completely isolated power supply. Additional two Arduino microcontrollers to configure two MAX11068 boards.

This project can achieve up to 48V. Facilitate with Graphical user interface using Java programming. GUI is able to provide real time measurement of voltage & SoC of 24 capacitors, voltage and SoC chart of 24 capacitors and also total voltage and SoC chart of entire capacitor pack. Due to the unavailability of direct measurement of state of charge, we used characteristics of super capacitor to estimate SoC. Accuracy test has been done by GUI and manually, the error is 0.3%. So it proves the reliability of GUI.

During this thesis completion we have gone through many complications. One of the challenging problems was working with MAX11068 for super capacitor, since it has no isolated power supply port. Literally we had to find a way to put external power to the board. Then another difficult solution for simple problem is using two Arduino microcontrollers to configure two MAX11068, reference problem due to the presence of many ground. Another problem was MAX11068 was crushing so often, it was quite tricky to make reasonable measurement result. We had to restart Arduino microcontroller after every crush.

Finally the measurement setup is designed with two MAX11068 boards connected with 24 capacitor pack via 3.5mm cable screw terminal (PCB header) connector. Where series connected 12 capacitor is allocated for lower board and another 12 for upper board.

8. DISCUSSION

Complete battery management system is compose of monitoring, balancing, controlling and maintain the system. In the following block diagram my project was 48V super capacitor PMU. The following figure representing the whole BMS system.

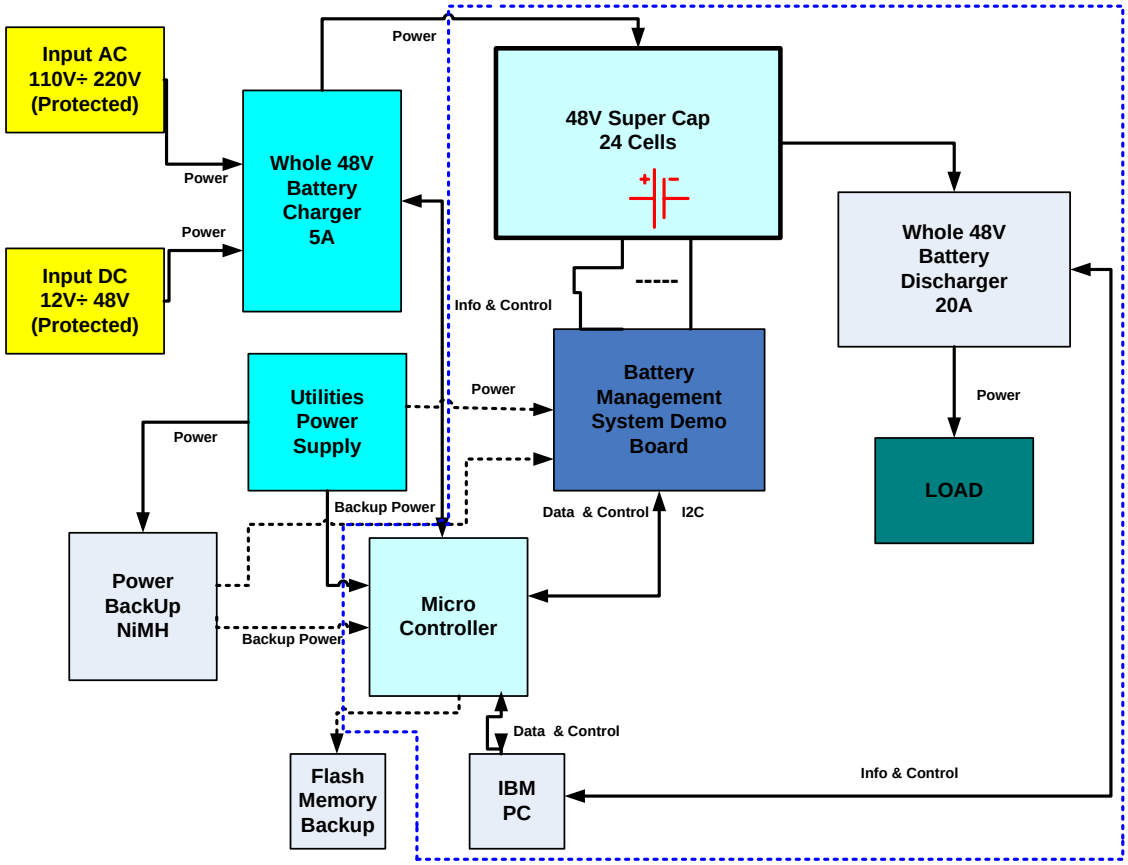


Figure 8.1: Block Diagram of Future BMS, blue line shows the part which is done in this thesis

In the future work there will be microcontroller for better control over the system. Constant current and constant voltage supply voltage (AC and DC), both of them controlled by current limiter and voltage limiter respectively. I^2C based communication exist between BMS demo board and microcontroller. Microcontroller process the command between PC and BMS system. BMS demo board is the fundamental key of the whole system. It's observed the battery conditions and performance, then control the whole system based on the received commends.

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APPENDIX 1: **Specifications of Aluminium Electrolytic Capacitor**

<table>
<tr><td>Temperature Range</td><td>Operating: -40°C +105°C
Storage : Preferably below +25°C, not exceeding +40°C</td></tr>
<tr><td>Rated Voltage Range (V_r)</td><td>16V to 450V DC</td></tr>
<tr><td>Surge Voltage (V_p)</td><td>$V_p = 1.15\ V_r$ ($V_r \leq 250$V DC)
$V_p = 1.10\ V_r$ ($V_r > 250$V DC)</td></tr>
<tr><td>Rated Capacitance Range</td><td>68 µF to 47,000 µF</td></tr>
<tr><td>Capacitance Tolerance</td><td>±20% at 100 Hz, 20°C [M class IEC-62]</td></tr>
<tr><td>Leakage Current (I_L) (mA, 5 min, 20°C)</td><td>max $I_L = 0.006\ C_r V_r + 4$ µA Kendeil product limit :
$I_L = 0.003\ C_r\ V_r$
At 85°C max $I_L = 0.02\ C_r V_r$ µA</td></tr>
<tr><td>Ripple current (I_r)</td><td>Refer to table at 105°C and 100Hz. For different temperature and frequency multiplier must be used as follows:
<table>
<tr><td>FREQUENCY</td><td colspan="2">50Hz</td><td>100Hz</td><td>500 Hz</td><td>1000Hz</td><td>>10k</td></tr>
<tr><td>MULTIPLIER (0-25V V_r DC)</td><td colspan="2">0.91</td><td>1.0</td><td>1.15</td><td>1.15</td><td>1.2</td></tr>
<tr><td>MULTIPLIER (40-100V V_r DC)</td><td colspan="2">0.88</td><td>1.0</td><td>1.35</td><td>1.40</td><td>1.45</td></tr>
<tr><td>MULTIPLIER (160-450V V_r DC)</td><td colspan="2">0.88</td><td>1.0</td><td>1.45</td><td>1.50</td><td>1.55</td></tr>
<tr><td>AMBIENT TEMP</td><td>35°C</td><td>45°C</td><td>55°C</td><td>65°C</td><td>75°C</td><td>85°C</td><td>95°C</td><td>105°C</td></tr>
<tr><td>MULTIPLIER</td><td>3.0</td><td>2.80</td><td>2.60</td><td>2.40</td><td>2.20</td><td>1.80</td><td>1.50</td><td>1.0</td></tr>
<tr><td colspan="3">Maximum internal temperature</td><td colspan="6">108°C</td></tr>
</table></td></tr>
<tr><td>Insulation Resistance</td><td>At 100V DC for 1 min is >100 MΩ across insulating sleeve and terminals.</td></tr>
<tr><td>Vibration Resistance</td><td>Frequency range: 10 Hz to 500 Hz, amplitude 0.75 mm max acceleration 10g for 3x2 h</td></tr>
<tr><td>Life test</td><td>After 2,000 hours application of rated voltage at 105°C capacitors meet characteristics aside</td><td>Cap change tan δ Leakage current (I_L)
Impedance (Z)</td><td>≤20%
≤200%
< initial limit
≤200%</td></tr>
<tr><td>Shelf life</td><td>After leaving capacitors under no load for 500 hours at 105°C, when restored at 20°C meet specifications aside</td><td>Cap change tan δ Leakage current (I_L)</td><td>≤±15%
≤150%
< initial limit</td></tr>
<tr><td>Useful life</td><td>250,000h at 40°C
15,000h at 85°C</td></tr>
</table>

	5,000h at 105°C
Failure percentage Failure rate	≤1% (during useful life) ≤Failure rate 30 fit (30 10^{-9}/h) ($V_r \leq 160$V DC) ≤40 fit (40 10^{-9}/h) ($V_r > 160$V DC)
Self-inductance	Approx. 20 nH
Reference standards	CECC 30.301 - IEC 60384-4 LONG LIFE GRADE