TAMPERE UNIVERSITY OF TECHNOLOGY

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LOW POWER SWITCHED CAPACITOR DC-DC CONVERTERS FOR LOW POWER TRANSCEIVER APPLICATIONS

Masters of Science Thesis

Examiners: Professor Nikolay T. Tchamov, Svetozar Broussev
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PREFACE

This work has been done at the RF-ASIC Laboratory of Institute of Communications Engineering, TUT. The atmosphere of interaction and innovation of all teams at this location has a major influence on this work and will be a guiding experience for my future. I sincerely acknowledge how much I owe to all my colleagues and friends for their support, friendly challenges and fruitful competition.

I would like to thank Professor Nikolay Tchamov for giving me the opportunity to work in his research group and develop this design. I would also like to thank Svetozar Broussev and other team members of RF-ASIC department for their helpful advices during the design process.

Last but not least, my parents and friends have been a great source of motivation for me during this whole time. I would like to thank them with kindest regards possible.

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ABSTRACT

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DC-DC converters, also known as switching voltage regulators, are one of the main components of a power management unit. Their main role is to provide a constant, smooth output voltage to power the electronic devices. Recent miniaturization trend of electronics circuitry has led to the need for smaller and high-efficient DC-DC converters in current and future applications.

This thesis presents a Switched Capacitor (SC) based DC-DC converter, which can directly operate at input voltage of 4.2V on 45nm CMOS process. Currently, most of the DC-DC converters on 45nm are not able to operate at such high voltages. Moreover, SC architecture has resulted in smaller size of converter compared with LC type DC-DC converters.

The design uses three SC topologies, which include two novel SC topologies of 2/5 and 2/7. Devices break down conditions have been overcome by implementing some of the MOS switches in cascoded structures. The converter structure uses eight phase interleaving approach to reduce output ripple to as low as 25mV level.

In addition to the main SC structure, a four-stage differential ring oscillator is designed for providing quadrature clock signals to the SC topologies. Clock generator can be enabled/disabled from outside the chip, through an enable (EN) pin. For instance, the EN pin can be used for regulating the output voltage in Pulse Frequency Modulation (PFM) feedback approach.

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Tasajännitemuuttaja, eli hakkuriteholähde, on keskeinen komponentti tehon hallinta yksikössä. Sen tehtävänä on tuottaa vakio käyttöjännite elektroniselle laitteelle. Elektroniikan miniatyrisoinnin johdosta nykyisiin ja tuleviin laitteisiin tarvitaan pienikokoisia ja korkean hyötysuhteen tasajännitemuuttajia.

Tässä diplomityössä esitellään kytketty kondensaattori (switched capacitor, SC) periaatteella toteutettu tasajännitemuuttaja, joka kestää 4.2V sisäänmeno-jännitteen 45nm CMOS prosessissa. Suurin osa nykyisistä 45nm prosessilla toteutetuista tasajännitemuuttajista eivät pysty toimimaan näin korkeilla sisäänmenojännitteillä. SC rakenteen ansiosta suunniteltu piiri on kooltaan pienempi kuin LC tyyppiset tasajännitemuuttajat.

Suunniteltu piiri muodostuu kolmesta SC topologiasta, mukaanlukien uudet 2/5 ja 2/7 topologiat. Transistorien rikkoutumisen estämiseksi osa MOS kytkimistä on toteutettu kaskodi raknteena. Muuntimessa on käytetty kahdeksaa lomitettua vaihetta, joilla ulostulojännitteen vaihojännite osan amplitudi saadaan tiputettua jopa 25 mV:iin.

SC piirien lisäksi suunniteltiin differentiaalinen rengasoskillaattori tuottamaan kvadratuuri kello signaalit eri SC topologioille. Kellogeneraattori voidaan kytkeä päälle tai pois piirin ulkopuolelta käyttäen enable (EN) pinniä. EN pinniä voidaan käyttää esimerkiksi säädettäessä ulostulojännitettä pulssitaajuusmodulaatio (pulse frequency modulation, PFM) menetelmällä.

CONTENTS

FIGURES

TERMS AND SYMBOLS

Symbols

SC	Switched Capacitor
DC-DC	Direct Current to Direct Current
DVS	Dynamic Voltage Scaling
IC	Integrated Circuit
EMI	Electromagnetic Interference
SMC	Switching Mode Converters
U-DVS	Ultra Dynamic Voltage Scaling
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
DCM	Digital Capacitance Modulation
MOS	Metal Oxide Semiconductor
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal

1 INTRODUCTION

Recent advances in the portable electronics industry have led to the development of more compact and higher performance electronic systems. Currently, these devices are powered through portable batteries, such as Li-Ion battery. One of the main performance drawbacks of these batteries is their variable output voltage. As most of the portable electronic devices operate at a fixed power supply voltage; using the output voltage of these batteries directly as a power supply can change the performance level of the electronic blocks. Therefore, there is an imperative need for a power management electronics circuit between the battery output and the electronics circuit's supply input, see Figure 1-1. The main purpose of the power management unit is to take widely varying voltage from the battery, and to convert it to a fixed output voltage, that is suitable for the operation of electronics circuits.

DC-DC converters, also known as switching voltage regulators, are one of the main components of the power management unit. Their main role is to provide a constant, smooth output voltage to power electronic devices. Recent advances in electronics have made it possible to integrate digital and analog electronics circuits into a single silicon chip, also known as mixed-signal Integrated Circuits (IC's). For example, consider the case of mixed-signal IC's in a mobile handset. The processor present in the IC normally operates on 1V while the analog circuitry may require higher voltages to operate, see Figure 1-1. In addition to these different voltage requirements, increased demand for speed and smaller portable electronic devices has made the design of a power management system even more challenging. This thesis deals with the importance and the technological requirements imposed on the design of DC-DC converters. Moreover, a design of state-of-the-art Switched Capacitor (SC) DC-DC converter has been presented with necessary performance results. Chapter 1 deals with the different types of DC-DC converters while Chapter 2 details Switched Capacitor (SC) converters, which in the integrated electronics domain, are one of the important type of DC-DC converters. The explanation continues in Chapter 3, where a design of state-of-the-art DC-DC converter is presented with necessary simulation results. Then, chapter 4 explains the necessary procedure for practical measurement of proposed DC-DC converter. At the end chapter 5 deals with the layout and chapter 6 concludes the topic with comparison of designed circuit with other published designs.

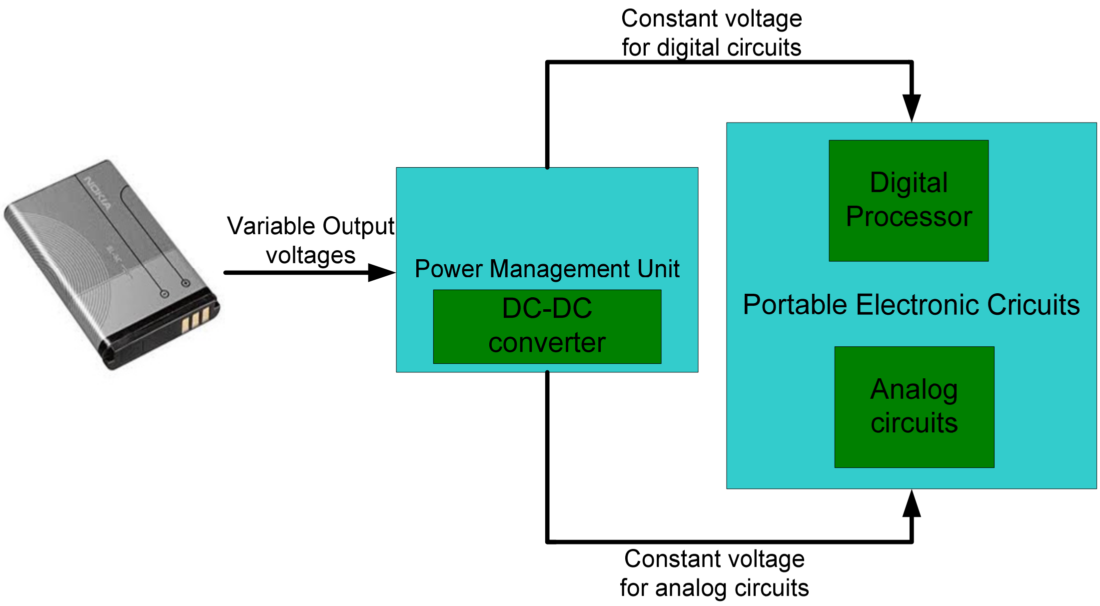

Figure 1-1. Use of DC-DC converters in portable electronic circuits

1.1 Background

Portable-electronic circuits today, ranging from cell phones, laptops, pagers, wireless sets etc, operate on batteries as their power source. One of the most commonly used batteries for portable-electronics circuits are Li-Ion. The nominal output voltage of a Li-ion battery is 3.6V. However, during operation, the output voltage of these batteries can vary widely from 4.2V to 2.6V [30],[1]. This varying output voltage makes the Li-Ion battery unsuitable for the current integrated circuits due to their requirement for a constant DC supply voltage at different power domains. Therefore, designing a DC-DC converter, which can provide regulated DC output voltage at varying battery input voltages, has become imperative. Furthermore, the constant increase in circuit complexity, their smaller size and higher speeds have given rise to greater challenges in DC-DC converter design. A state-of-the-art DC-DC converter for today's portable integrated applications should possess the following characteristics:

1. High power efficiency
2. Small size (~1mm^2 or smaller).
3. No off-chip components (or small amount).
4. Higher current delivering ability
5. Wider input voltage range (should be directly able to operate with current batteries such as Li-ion having input voltage range 4.2-2.6V)
6. Low output voltage ripple (10-50mV or smaller)

In order to reduce power consumption, the present trend in digital integrated circuits is the use of Dynamic Voltage Scaling (DVS). In DVS, supply voltage of a digital circuit is lowered to reduce the power consumption of the circuit. According to [1] supply voltage has got a quadratic relationship with power consumption. i.e.:.

$$P_{CONSUMED} \propto (V_{SUPPLY})^2 \tag{1.1}$$

However, decreasing the supply voltage comes at the cost of circuit operating speed. As digital circuits are not operating all the time at higher speeds, voltage scaling can be done in times of lower speed operations, thereby reducing the power consumption. Thus DC-DC converters should provide scalable output voltages for DVS.

These factors pose various design challenges on DC-DC converter design for portable electronics applications. Various design methods are adopted to meet the above performance parameters. These different design approaches have led to the division of DC-DC converters into two main types, i.e. Linear and Switching converters. The next section deals with these main classifications of DC-DC converters in detail.

1.2 Classification of DC-DC converters

Based on their circuit operation, DC-DC converters are divided into two main types: Linear and Switching DC-DC converters. Furthermore, switched DC-DC converters have a more general classification of Buck and Boost converters. Buck converters provide an output voltage lower than the input voltage, while in Boost converters output voltage is higher than their input voltage. Figure 1-2 shows the main divisions of DC-DC converters.

Following text explains briefly different types of DC-DC converters.

1.2.1 Linear Regulators

Due to their simple design and smaller size, linear regulators are employed in a large number of applications. Linear regulators regulate the output voltage by changing the resistance of the active transistor [2]. As the output current is taken entirely from the input source through a controlled transistor resistance, the maximum efficiency of the linear regulator is limited to the ratio of the output voltage to the input voltage (V_L/V_{BAT}). This efficiency limitation becomes quite critical when the difference between the battery and output voltage, also called the dropout voltage, is quite large. As a result, the use of linear regulators is only efficient for lower dropout voltages.

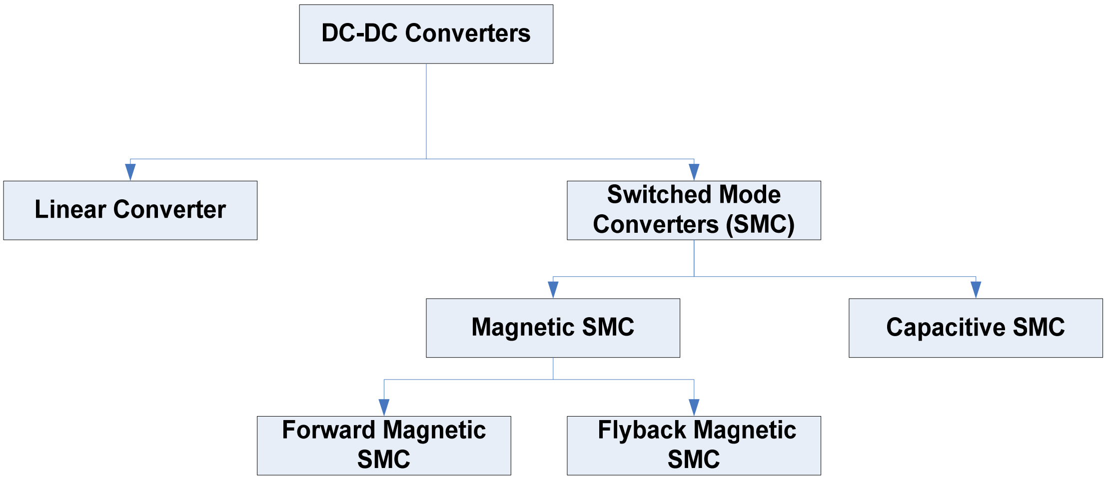

Figure 1-2. Classification of DC-DC converters [5]

1.2.2 Switching Regulators

The main transistor in switching regulators has either an 'on' or 'off' condition. This provides intermittent bursts of energy at the output. This working principle is different from that of the linear regulators, where the transistor operates in the active region all the time. As the transistors remain in saturation or cutoff region most of the time, switching regulators provide a much higher level of efficiency than linear regulators, which theoretically can go up to 100%. However, switching regulators are much more complex to design than linear regulators. They also generate Electromagnetic Interference (EMI) problems due to their switching action. On the basis of their main energy transfer components, switching regulators are further divided into Switched Capacitor (SC) converters and Magnetic switching mode converters.

Magnetic switching regulators consist of an inductor to smooth out the output ripples, which exist due to the switching operation of the regulator. Theoretically, these regulators are able to provide 100% efficiency, but the main problem with these regulators is their bigger size, which makes them unsuitable for integrated applications. Recent works [3],[4] have been able to design these regulators using monolithic inductors, but the space taken up by these regulators is still quite large. Magnetic regulators are further divided into Forward and Fly-back regulators. In Forward regulators, the energy goes from the input through the magnetic components and then to the load simultaneously. Fly-back regulators, on the other hand, first store energy from the input in the magnetic components and later release it to the load [5].

If the energy transfer component in switching converter is a capacitor rather than an inductor, resulting converters are categorized as Switched Capacitor (SC) DC-DC converters. More elaborated explanation of SC converters will be dealt in chapter 2. Here a brief summary for advantages/disadvantages of different DC-DC converter types is presented in Table 1.

Table 1 Advantages/disadvantages of different DC-DC converter types

Converter Types	Advantages	Disadvantages
Linear converters	• High Efficiency for low dropout voltages • Lower output ripples (practically no ripples) • Smaller size, ease of integration • Simple design • Less EMI	• Poor Efficiency for high dropout voltages • Can provide only output voltages lower than input voltage
Magnetic switching converters	• Very high efficiency	• More complex design • Not easily integrated • Bigger size • EMI problem
SC converters	• Ease of integration • Higher efficiency than linear regulators with large dropout voltage (same for LC) • Smaller size compared to magnetic switching regulators • Can provide higher or opposite polarity voltages (same for LC)	• Only discrete number of output voltages are possible at peak efficiency. Scalable output voltage generation is difficult to obtain. • Lower output current than Magnetic regulators • Less efficient than Magnetic switching regulators

1.3 State-of-the-art DC-DC converters

Due to increased demand of small-sized and highly-efficient portable electronic systems, design requirements for DC-DC converters are becoming more and more challenging. Up till now, magnetic switching converters have offered the best possible efficiency but the bigger size and electromagnetic interference (EMI) generated by these regulators make them unsuitable for future miniature electronic systems. Therefore, emphasize of converter design is shifting towards Switched Capacitor (SC) DC-DC converters for future miniature applications.

SC DC-DC converters not only provide smaller size than magnetic switching converters, but they are also comparable and even superior to magnetic converters in terms of efficiency at low power levels. In addition, SC technology can have less EMI if operated with a single switching frequency clock. These evident benefits have led to increased research in the field of SC DC-DC converters. However, like all other design approaches, SC converters have some design limitations. Few of these are listed below:

1. It is estimated that the current Li-Ion batteries will dominate the industry for at-least five to ten more years [30]. Output voltage of these Li-ion batteries vary from 4.2-2.6V [1]. This voltage poses a design problem in advanced silicon processes, as these voltages are much higher than voltage breakdown of the process. Because of this limitation, most of the current SC DC-DC converters operate at a lower input voltage generated by off-chip switching regulator.
2. SC converters have only discrete number of output voltages at peak efficiency i.e. scalable output voltage generation with equally high efficiency is difficult to obtain.
3. Integrated capacitors posses high value of bottom plate capacitance associated between bottom plate capacitor and substrate. If the capacitors are implemented with bottom plate connected to some other potential than ground a huge amount of power loss occurs during circuit operation due to charging and discharging of bottom plate capacitance.
4. Large currents require bigger capacitors in the design. This makes the size and losses associated with these capacitors quite big. Special silicon processes are required to produce high-density and linear integrated capacitors.

Recent works have tried to overcome these design limitations by introducing various novel techniques. References [7],[8] are examples of small size, fully integrated DC-DC converters in 45nm technology, while works [9],[10], provide scalable voltage conversion as well. For higher current designs, [11] is able to deliver 200mA of output current with an active area of only 0.37mm^2 in 32nm technology.

In the domain of magnetic switching converters, references [3],[4] are examples of designs with fully monolithic inductors. The sizes occupied by these converters are 3.76mm^2 and 1.592mm^2 respectively.

From the above discussion it is evident that state of the art monolithic SC DC-DC converter at the time of writing this thesis should possess the following properties:

1. Should directly operate from Li-ion battery.
2. Should provide a lower output voltage in range of 1-0.8V for near-future 32 and 28nm silicon processes.
3. Should provide scalable output voltage.
4. Should be fully integrated.
5. Should be as small as possible in size (~1mm^2 or smaller).
6. Should possess efficiency comparable to the magnetic converters.

1.4 Design targets

Based on above discussion, design targets for this thesis have been presented in the Table 2. Due to the increased circuit complexity, this thesis focuses on the analysis and design of the power stage of DC-DC converter only. More importantly, power stage is the most crucial converter element in determining efficiency and output ripple. Therefore, a proper design of power stage ensures that the circuit will work properly in closed loop operation. Full closed loop operation of DC-DC converter requires feedback circuitry as well, design of which however, is left for future research.

Table 2 SC DC-DC converter design specifications

Input Voltage	3.2-4.2V
Output Voltage	0.9-1V
Output Ripple	40mVp-p max
Output Current	0-100mA
Efficiency	60-80%

2 ON CHIP SWITCHED-CAPACITOR (SC) DC-DC CONVERTERS

2.1 Importance of SC converters

The ever-growing increase in the demand for smaller and battery-efficient integrated circuits, have resulted in the need for a power management unit. In this context, switched capacitor converters, which are one of the main components of a power management unit, offer high potential for integration and smaller size. Although SC circuits tend to be less efficient than contemporary inductor-based switching converters, recent advances have developed various methods to reduce the loss mechanisms associated with SC designs.

Judging by current trends in the integrated circuit industry, it is logical to assume that SC converters will become an essential part of power management units in integrated circuits. In the text to follow, basic operation of SC converter will be explained. Loss mechanisms associated with SC converters will be elaborated. The discussion will continue with the efficiency and load current analysis of common SC converter topologies and at the end various control schemes adopted in SC converters together with implementation issues will be addressed. This theoretical knowledge will form a basis for the design of state of the art dc-dc converter in Chapter 3.

2.2 Basic operation of SC converter

Consider the circuit shown in Figure 2-1, consisting of only switches and capacitors. The switches in the circuit are operated by two distinct non-overlapping clock signals, φ_1 and φ_2, so that the switches turn on when the clock signal is high.

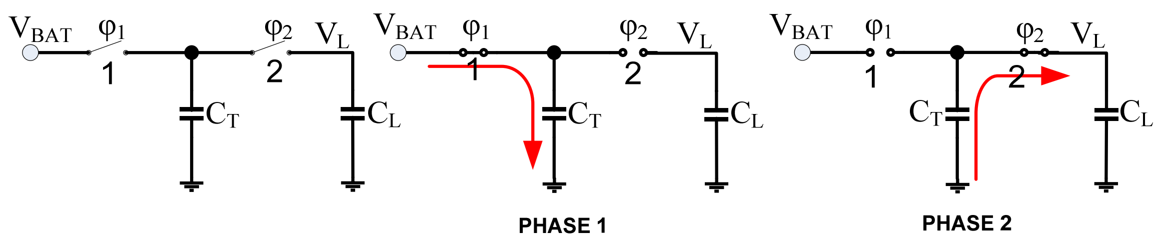

Figure 2-1. A 1:1 SC converter topology

During φ_1, the battery voltage starts charging the charge-transfer capacitor C_T through switch 1. The charging time depends on the on-resistance of the switch and a small amount of voltage is dropped across the switch-on resistance. Similarly, during φ_2 switch 1 turns off, switch 2 turns on, and C_T discharges into the load capacitor C_L through switch 2. If the switch on-resistance is assumed to be negligible, then the output voltage at no-load condition (V_{NL}) will be equal to the input battery voltage. Because of this, the SC converter topology shown in Figure 2-1 is called 1:1 SC topology.

In practice, SC converters always have some load attached with them. Moreover, switch on-resistance Ron is not negligible. Due to these load and switch on-resistances, output voltage V_L of the SC converter drops below the no-load output voltage V_{NL}. The difference between the V_{NL} and V_L is known as dropout voltage and is given by $\Delta V = V_{NL} - V_L$. It has been observed that V_L is mainly dependent on output current, switching frequency, and the charge transfer capacitor's value. The value of V_L is important in determining the linear efficiency related with the SC converter given by [1].

$$\eta_{LIN} = \frac{V_L}{V_{NL}} \tag{2.1}$$

Equation (2.1) implies that a smaller value for V_L will result in a loss in efficiency, and thus it is not possible to use a single SC converter topology in a power-efficient way, if multiple output voltages are desired.

The limitation imposed on the linear efficiency by SC converters demands the need for separate SC converter topologies whose output voltages are quite near to their no-load voltages. Recent developments of SC converter topologies are able to produce no-load voltages of 1, 1/2, 1/3, 2/3, 3/4, 1/4, 2/5 and 3/5 of battery voltages, etc [1], [6]. Other topologies can also be made by changing the configuration of the SC structure. Therefore, if scalable output voltages are required, various topologies need to be switched in the main circuit, so that the overall dropout voltage always remains low. Figure 2-2 shows some common topologies of SC converters.

2.3 Loss mechanisms in SC converters

Various loss mechanisms exist in SC converters due to which power efficiency of SC is greatly suffered. Most important of these loss mechanisms are explained below:

2.3.1 Linear Efficiency Loss

In all SC converter topologies, maximum power efficiency is limited by equation (2.1), where V_L is the output voltage of DC-DC converter, and V_{NL} is the output voltage at no load condition. This efficiency loss due to topology structure is known as linear efficiency loss. The reason for linear efficiency loss is due to charging and discharging of energy-transfer capacitors, where the charge-transfer currents cause power losses dissipated mainly in the capacitor series resistance (R_{ESR}) and the switch on resistance R_{ON} [15].

It has been observed that V_L is mainly dependent on output current, switching frequency and charge-transfer capacitors value. A lower value of V_L will result in lower efficiency, which is one of the major drawbacks of SC converters. As a result, in order to obtain similar efficiency for large range of output voltages, multiple topologies are required so that V_L is always quite close to V_{NL} [9].

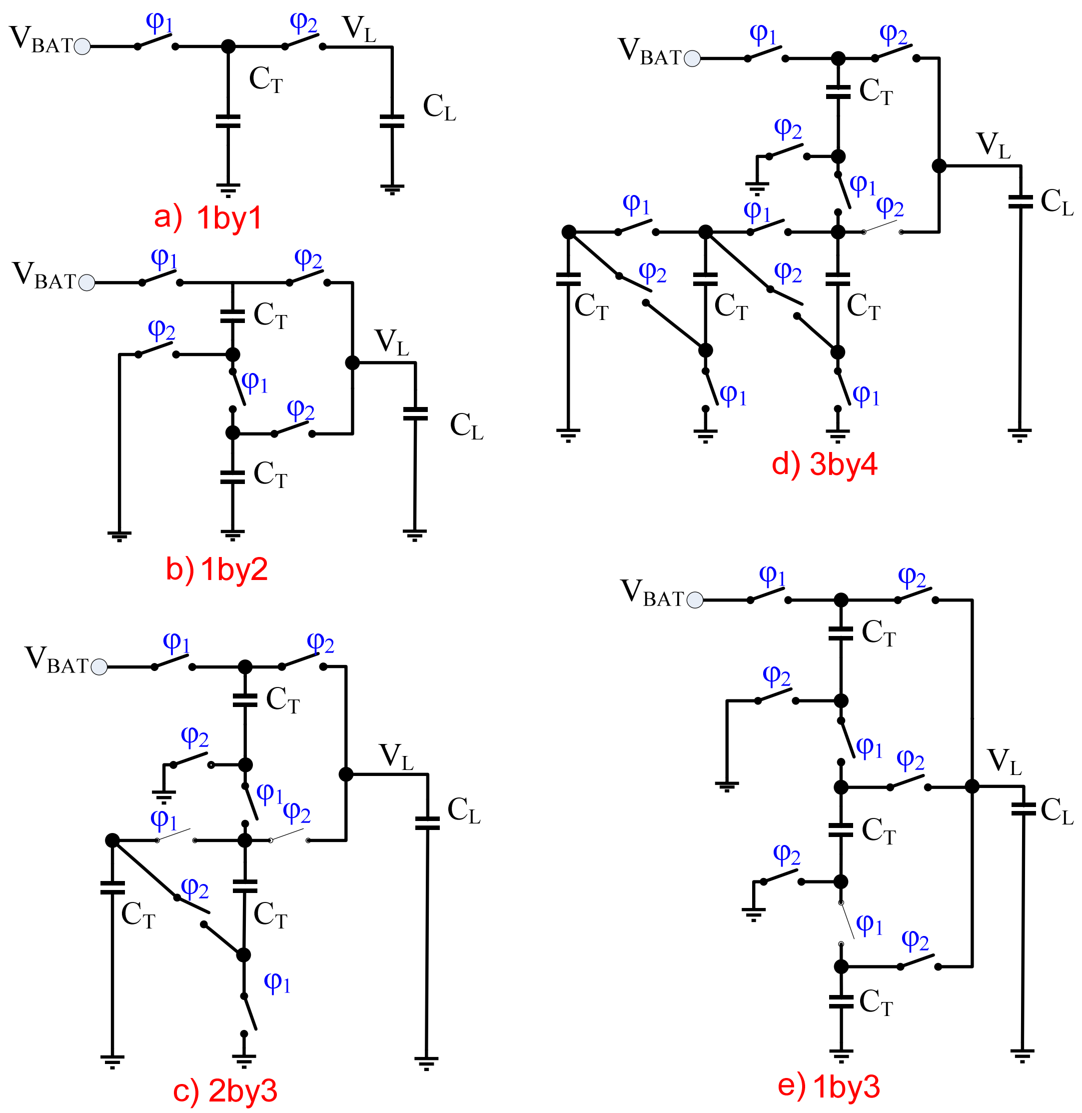

Figure 2-2. Some common SC converter topologies a) 1by1 b) 1by2 c) 2by3 d) 3by4 e)1by3 [1]

The above statement can also be expressed in terms of dropout voltage, which is given as $\Delta V = V_{NL} - V_L$. For the same switching frequency and charging capacitor values, smaller dropout voltage will result in higher efficiency but lesser output current. Thus, if a certain topology is unable to provide required output current at certain dropout voltage, a higher V_{NL} topology is used. Use of higher V_{NL} will result a drop in efficiency but load current requirements will be met [9].

As the maximum efficiency can be achieved only with minimum possible drop out voltage; switching frequency, charging capacitor size and switch conductance must be increased to reduce dropout voltage value.

2.3.2 Bottom Plate Capacitance Loss

In SC converters, parasitic capacitances exist from the bottom plate of the charge transfer capacitors to ground. The bottom plate capacitance can be up to 5-20% of the total charge-transfer capacitance and constitute a major role in SC circuits transfer functions [1]. In gate-oxide implementation of capacitors with N-well as a bottom plate, the parasitic arise due to reverse-biased diode capacitance of N-well, p-substrate junction [1]. If C_{BP} represent the bottom plate capacitance of the charge transfer capacitance C_T, then

$$C_{BP} = \alpha . C_T \tag{2.2}$$

Where α is a constant and can be from 5-20% for on-chip capacitors oxide capacitors [1].

The power loss associated with bottom plate capacitance is given as [28]:

$$P_{bp} = f_{sw} . \sum_i C_{bp,i} . V^2{}_{bp,i} \tag{2.3}$$

Where f_{sw} is switching frequency, C_{bp} is bottom plate capacitance and V_{bp} is the maximum voltage swing across bottom plate capacitance.

Consider a SC converter topology shown in Figure 2-3. The circuit operates in two distinct and non-overlapping phases φ_1 and φ_2. In phase 1, switches connected with φ_1 turn on, charging the two charge transfer capacitors C_T at half of battery voltage V_{BAT}.

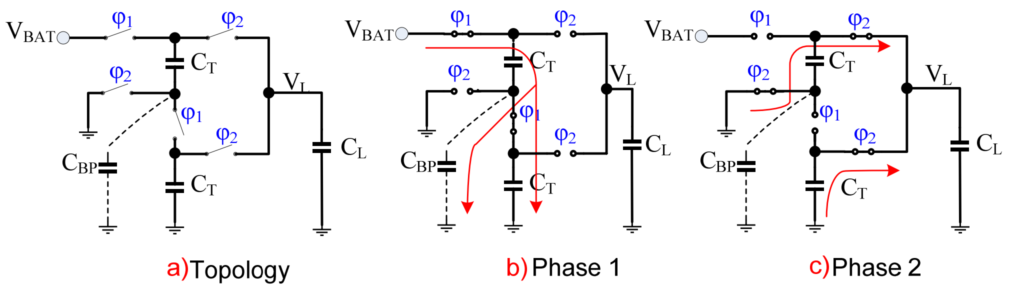

Figure 2-3. SC 1/2 topology with bottom plate capacitance [1]

In this phase the switches connected to φ_2 are open. Similarly, in phase 2 switches connected to φ_2 turn on, charging the output capacitor C_L through the charge-transfer capacitors C_T. The process repeats in next cycle.

Bottom plate capacitance associated with upper charge-transfer capacitor C_T also gets charged to $V_{BAT}/2$ during φ_1. During φ_2, this bottom plate capacitance gets connected to the ground terminal and useful energy stored in the C_{BP} capacitor is wasted. If the bottom plate capacitance is big enough, then this energy loss can result in notable efficiency degradation [1].

2.3.3 Gate Drive Loss

When a transistor is switched on in SC converters, parasitic capacitances associated with the transistor switches get abruptly discharged to zero [17]. Power consumed in this process is given by [27].

$$P_{sw} = f_{sw} . \sum_i C_{MOS,i} . V^2{}_i \tag{2.4}$$

Where C_{MOS} represents any of the MOS transistor capacitances e.g. C_{gs}, C_{gd}, C_{sb}, and C_{db} etc, while V_i represents the maximum voltage swing across these capacitors (see Figure 2-4). Overall switching loss P_{sw} will then be the sum of the power losses of all these capacitors C_{gs}, C_{gd}, C_{sb}, and C_{db}.

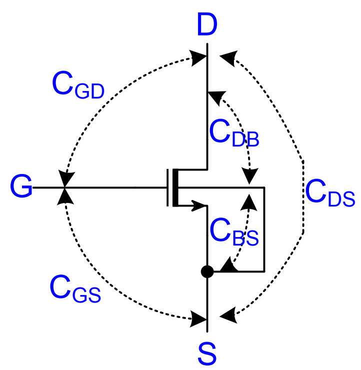

Figure 2-4. MOS transistor parasitic capacitances

Increasing the width of the transistor is associated with bigger transistor parasitic capacitances and will eventually increase the gate drive loss. On the other hand, bigger transistor width results in smaller $R_{ON,}$ which will decrease the conduction loss. Hence, there is an optimum width of the transistor at which efficiency is maximum.

Overall efficiency equation of the SC converter will then include all the above mentioned losses, and it is given by:

$$\eta = \frac{P_o}{P_o + P_{SW} + P_{bp} + P_{Cntrl}} \tag{2.5}$$

Here P_o is total output power, P_{sw} is switching power loss, P_{bp} is bottom plate capacitance power loss and P_{cntrl} is the control circuitry power loss.

2.4 Power delivery analysis

Consider SC converter 1/2 topology shown in Figure 2-3. For analysis purpose we will consider that the bottom plate capacitance is negligible. In phase 1, switches connected with φ_1 turn on, charging the two charge transfer capacitors C_T at half of battery voltage V_{BAT}. Energy extracted from the battery during φ_1 is given by [9]:

$$E_{BAT}=C_T.V_{BAT}.\Delta V \tag{2.6}$$

Where ΔV is given by $\Delta V = V_{NL} - V_{L.}$

During φ_2 charge transfer capacitors C_T get connected to the load and transfer a charge twice than the charge gained in φ_1. Hence the energy delivered to the load in is given by [9]:

$$E_L=2.C_T V_L \Delta V \tag{2.7}$$

Linear efficiency of the SC converter is given by:

$$\eta_{LIN} = \frac{E_L}{E_{BAT}} = \frac{2.C_T.V_L \Delta V}{C_T.V_{BAT}.\Delta V} = \frac{V_L}{V_{BAT}/2} \tag{2.8}$$

As $V_{BAT}/2=V_{NL}$ so

$$\eta_{LIN} = \frac{E_L}{E_{BAT}} = \frac{V_L}{V_{NL}} = \frac{V_{NL} - \Delta V}{V_{NL}} = \left(1 - \frac{\Delta V}{V_{NL}}\right) \tag{2.9}$$

The power delivered to the load is given by [9]:

$$P_o = \frac{E_L}{t_s} = E_L.f_s = 2.C_T.V_L.\Delta V.f_s = E_{BAT}.f_s.\eta_{LIN} \tag{2.10}$$

Where f_s is switching frequency of converter and t_s is the switching period.

It can be seen from Equation (2.10) that the power delivered to the load can be increased by increasing the switching frequency and/or the charge-transfer capacitor value. Moreover, increasing ΔV will cause increase in the amount of power delivered to the load, but it will result in decreased linear efficiency. Therefore, if a topology is unable to provide enough power at the output, a higher topology should be used having higher ΔV to meet the load requirements [9].

Reference [1] reports improvement in conventional SC converter topologies shown in Figure 2-2. The improved topologies possess higher current delivering ability. In conventional SC converter topologies, battery voltage has no direct connection with the load. During φ_1, charging capacitors get charged from the battery voltage with no connection to the load, while in φ_2 load capacitor is charged to V_L by the charging capacitors. This conventional process can be improved, for more output current, by providing a path from battery voltage to load during both charging phases φ_1 and φ_2. For clear understanding consider a conventional 1:1 SC converter topology shown in Figure 2-5 [1].

The topology can be improved for delivering more output current by connecting the ground terminal of bottom most charge transfer capacitor to the load. According to [1], "*If a particular gain setting in the previous version gave out a voltage ratio of p/q, then by connecting the ground terminal of the bottom-most charge-transfer capacitor during φ_1 to the load terminal, a gain setting with a voltage ratio of p/(p + q) can be obtained.*"

The improved topology shown in Figure 2-5, results in charging the load capacitor in both phases of converter. This results in higher output current. It has also been observed that the improved topologies provide lower bottom plate parasitic losses [1]. Figure 2-6 shows some common topologies for SC converters with output current enhancing improvement.

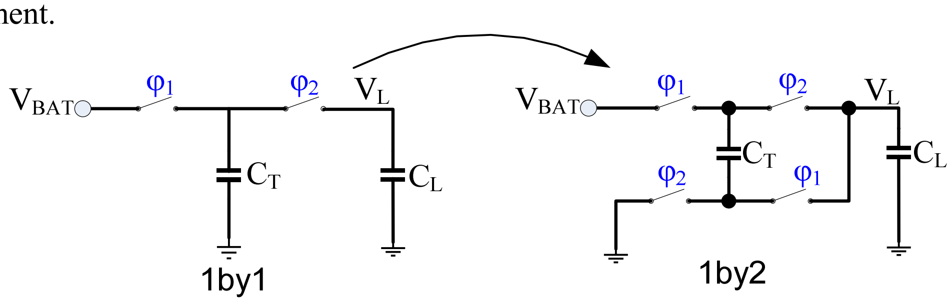

Figure 2-5. SC converter structure improvement for higher output current

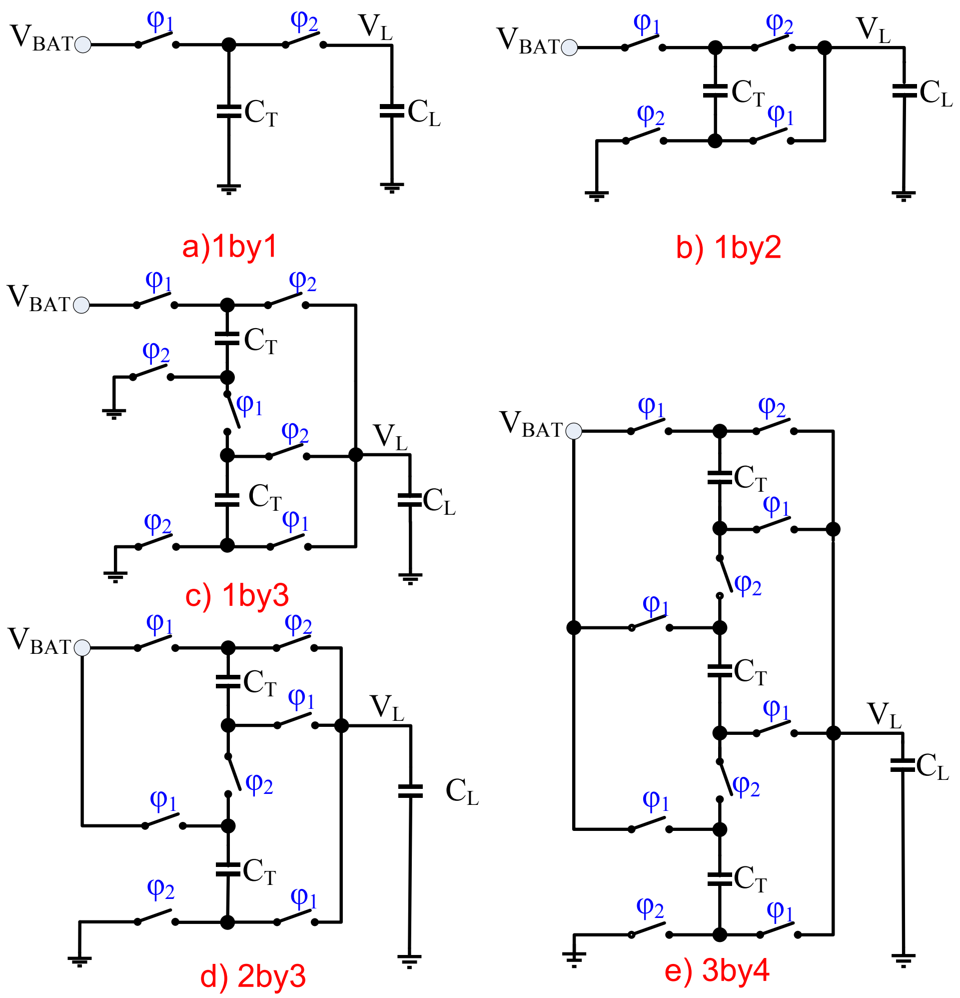

Figure 2-6. Improved gain setting of SC topologies a) 1by1 b) 1by2 c) 1by3 d) 2by3 e) 3by4 [1]

2.5 Output ripple

One of the major concerns in DC-DC converter design is the output voltage ripple, since many electronic circuits require extremely smooth output voltage. Therefore, the need for low ripple DC-DC converters becomes evident. It has been observed that the output ripple of SC DC-DC converter can be reduced by [21]:

1. Increasing the switching frequency.
2. Decreasing the load current.
3. Increasing the charge-transfer capacitor value.
4. Increasing the load capacitor value.
5. Reducing the R_{ESR} of the capacitors
6. Keeping the clock duty cycle far from 0 and 100%

Among all, the most influential parameters for output ripple in SC converters are load capacitance and duty cycle. An optimum value of duty cycle and bigger load capacitance value will result in smaller output ripple [24].

In designs where smooth output voltage is of main importance, various schemes have been implemented to reduce the output ripple voltage. One major approach is known as **Interleaving** [25]. The main idea of interleaving scheme is to give less time for discharge the output capacitor, so to lower the output ripple [26].

Figure 2-7 shows a basic 1/3 SC topology. The topology can be operated with or without interleaving as explained below.

In normal operation of the converter without interleaving, each capacitor gets charged to 1/3 of input voltage during φ_1. In φ_2, all the charge transfer capacitors are connected in parallel with each other and get discharged through C_L simultaneously. This results in the voltage curves shown in Figure 2-8 (a). If lower output ripple is desired, interleaving approach is implemented. The main idea is to discharge each charge transfer one by one into the load capacitor. This will result in lesser time to discharge the capacitors and hence the output ripple will be smaller. Voltage waveforms of SC converter with interleaving are shown in Figure 2-8(b).

2.6 Control schemes

Various schemes have been presented in the literature, which can regulate the output voltage of an SC DC-DC converter by changing some relevant parameters like switch ing frequency, pulse width, charging current and charge transfer capacitor value. Some of the most important schemes are presented below.

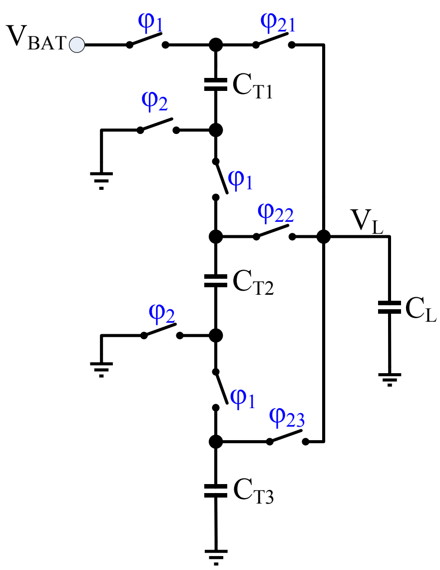

Figure 2-7. Basic 1/3 SC topology [25]

2.6.1 Pulse Frequency Modulation (PFM)

Pulse frequency modulation, or pulse skipping modulation, is one of the most common schemes employed in SC dc-dc converter designs [18]. Its main principle of operation is shown in Figure 2-9.

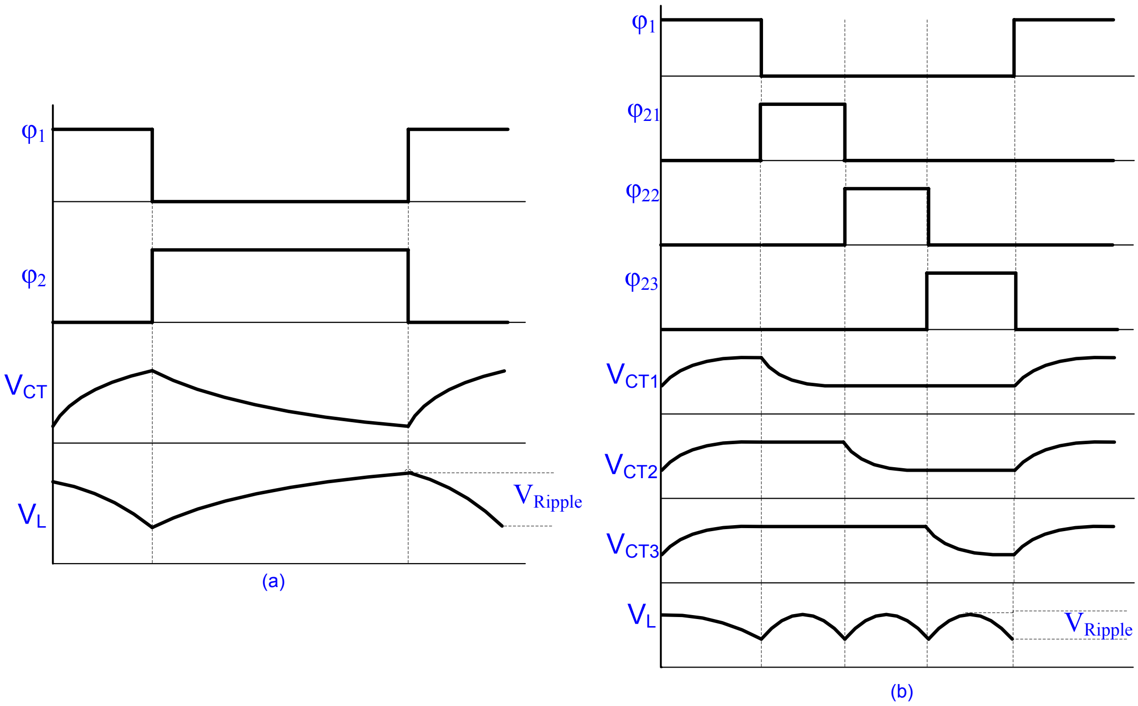

Figure 2-8. (a) Voltage Waveforms without interleaving (b) Voltage waveforms with interleaving [25]

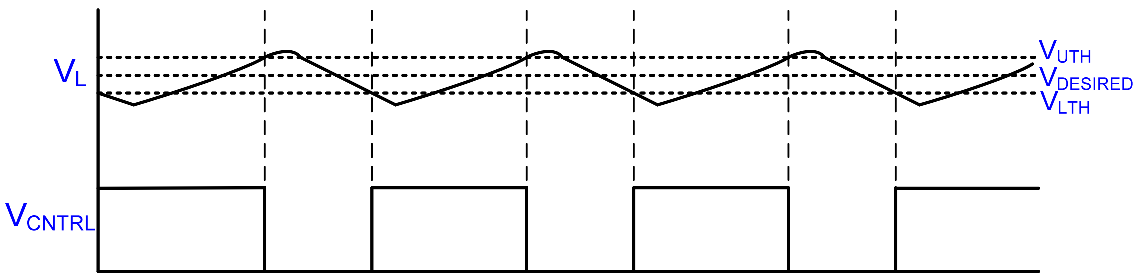

Figure 2-9. Pulse Frequency Modulation

When load voltage V_L falls below a certain defined lower threshold voltage V_{LTH}, the V_{CNTRL} signal goes to its high level. A high level V_{CNTRL} permits the clock signal to get connected to the SC stage, allowing the output capacitor to get charged through the charging capacitors. This will eventually raise the output voltage back to the $V_{DESIRED}$ value. In the same manner, when the load voltage goes above the defined threshold voltage V_{UTH}, the V_{CNTRL} signal goes low, disabling the clock connection from SC stage, thereby bringing the V_L back to $V_{DESIRED}$.

In some implementations of the pulse frequency modulation scheme, the clock frequency can also be changed to control the output voltage V_L. As higher switching frequency leads to more switching losses, the decrease in frequency at smaller loads results in higher efficiency for lighter loads [19].

2.6.2 Pulse Width Modulation (PWM)

By controlling the pulse width of the clock pulse in SC converters, the charging time of the capacitors can be controlled. This charging time eventually controls the amount of charge transferred to the load capacitor and, therefore, the output voltage. This form of feedback scheme, implementing changing pulse width to the clock signal, is known as pulse width modulation. It has been observed that the output ripples and efficiency of SC converter are dependent on the pulse width [20],[21]. A changing pulse width will result in varying output ripple voltage and efficiency. Pulse width modulation scheme, in this context, has the drawback of not achieving optimum efficiency and minimum output ripples.

2.6.3 Digital Capacitance Modulation (DCM)

In a digital capacitance modulation scheme, in order to control the output voltage, the amount of charge transfer capacitance involved in the SC converter is changed. For example, if a 4 bit DCM scheme is used, SC structure can be designed with 1x, 2x, 4x and 8x sized charging capacitors. In the beginning 1x topology is inserted into the main circuit and if the load current demands are not met, a 2x or higher topology can be inserted in the main circuit to meet to load current demand. [19]. One example of DCM algorithm can be seen in Figure 3-2.

For optimum efficiency, the switch resistance should be such that the charging capacitors settle down during phase 1 or phase 2. This means that the switch width is also changed in DCM when changing the charging capacitor value. This will help in reducing the bottom plate parasitic capacitance and/or switching losses [1].

A DCM control scheme has the advantage of having lower EMI interference compared to PFM, due to constant frequency operation. This property makes this scheme useful for the mixed signal IC designs where the noise generated can interfere with digital circuits [19]. Additionally, DCM bottom plate capacitance and switching losses scale down at lower load currents due to smaller transistor widths.

2.6.4 Quasi Switched-Capacitor (QSC) configuration

In a quasi switched-capacitor scheme, capacitor charging current is changed in order to control the output current. In this scheme, the MOS transistors are operated in the saturation region and the gate voltage of the MOS is used to control the output voltage. QSC scheme has got two main problems: 1) the conduction loss of the MOS transistors increase in the saturation region; 2) when the load current increases and comes to a limit, the switch will work from the saturation to the triode region, so it doesn't let the input current control achieve the fixed output voltage [22].

Using the QSC scheme makes the input current of the converter continuous. This reduces the EMI introduced by a pulsating current and the transistors do not need to be over-rated in order to cope with the short duration of instantaneous charging current stress. These converters are small, have low EMI and a lower output ripple. The design approach consists of two SC topologies in parallel working in anti-phase with each other. Because the linear charging process of the capacitors is dependent on the applied gate voltage, the output voltage is less affected by the supply voltage variations [23].

A brief summary for advantages/disadvantages of different feedback control schemes is presented in Table 3

Table 3. Advantages/disadvantages of different feedback control schemes in dc-dc converters

Control Schemes	**Advantages**	**Disadvantages**
Pulse Frequency Modulation	• Ease of implementation	• Generates EMI problem due to presence of harmonic component of changing clock frequency
Pulse Width Modulation	• Ease of implementation • Constant frequency scheme so less EMI generation problem	• Optimum efficiency is not achieved due to changing pulse width • Minimum output ripple is not possible due to changing pulse width. Output ripple is dependent on clock pulse width • Constant frequency makes the switching losses higher at smaller loads
Digital Capacitance Modulation	• Constant frequency scheme so less EMI problem • Bottom plate parasitic capacitance losses and/or switching losses reduce at smaller load currents.	• Requires more complicated structure of charge transfer capacitors

Quasi Switched Capacitor configuration	• Low EMI due to continuous input current • Smaller size • Lower output ripple • Less influence of supply voltage variations	• Conduction loss of MOS transistors is more • In limiting case of load current, MOS transistor goes from saturation to triode region Therefore, not allowing the input current to control the output voltage.

2.7 Implementation issues

Main circuit components in SC converters are capacitors and switches. These switches were implemented before by diodes but with the advent of MOS technology, MOS transistors are becoming increasingly popular due to their small dropout voltage in integrated circuits. Implementing MOS transistors as switches, pose a number of implementation issues. We will address these practical implantation details, one by one for MOS transistors and integrated capacitors in the topics to follow:

2.7.1 MOS transistor switch implementation

An ideal switch in SC converter has zero on-resistance and no parasitic capacitance associated with it. In practice, there is always a compromise between on-resistance and parasitic capacitance. Increasing the width 'W' of the MOS transistor will result in smaller on-resistance, but on the other hand it increases the parasitic capacitance of the switch. As discussed in Section 2.3.3, smaller switch-on resistance decreases the conduction loss and bigger parasitic capacitance increases the switching losses. A bigger gate parasitic capacitance will also require larger current to charge it up. This will result for a need of bigger input buffer. Therefore, there is optimum width W_{opt} of the transistor at which both losses are minimal and efficiency is at maximum.

MOS transistors need to be operated in triode region for minimum on-resistance. Gate voltages should also need to be close to the transistor rating to improve conduction. A higher gate voltage will be able to charge the gate parasitic capacitance faster and therefore conduction will be improved. However, higher gate drive voltages increase the gate drive loss. Some important concerns about MOS switch implementation are mentioned below:

1. Drive the transistors with the maximum drive level possible to improve conduction.
2. NMOS is preferred option over PMOS because of higher mobility and smaller size.

3. Use the transistors with the voltage rating close to the gate drive voltage to optimize their size.
4. Implement a dead time between different phases of converters, to eliminate possible short-circuit current.
5. Bulk terminal is normally biased with the highest voltage possible in PMOS and with lowest possible voltage in case of NMOS.
6. Instantaneous voltages appearing at the nodes of circuit after the switching from one phase to another are important and can damage the devices. Their affects should also be considered [27].

Due to the presence of different driving voltage requirements of transistors, in SC converters, required gate voltages of the MOS transistors in SC converter can be different. These driving voltage requirements pose a need to design level shifters for driving the transistors operating at different voltage levels.

2.7.2 Integrated capacitor implementation issues

Shrinking size of electronic devices with technology improvements has resulted in the need for smaller and more efficient integrated circuits. Therefore, technology is shifting now from off-chip implementation of capacitors to on-chip integrated capacitors. On-chip capacitor implementation poses a lot of problems: 1) the quality factor associated with integrated capacitors is very small compared to the off-chip capacitors; 2) the parasitic capacitance associated with the on-chip capacitors can be huge proportion of total capacitance. Moreover, it is very difficult to achieve bigger on-chip capacitance without compromising on the chip area.

Integrated capacitors can be implemented by different techniques e.g. Metal Insulator Metal (MIM) capacitors, Metal Oxide Metal (MOM) capacitors, Gate-oxide capacitors, Poly-metal capacitors, double poly capacitors, etc. Gate oxide capacitors offer the largest capacitance per area, but they are highly non-linear and, additionally, gate oxide capacitors have high bottom plate capacitance to the substrate (5-15%). Double poly capacitors can be the second efficient solution. They have lower capacitance per unit area than thin oxide, but have smaller stray capacitance (about 5%) [29]. Other integrated capacitors have low energy densities with lower parasitics e.g. MIM capacitors. Some specialized processes offer a high-metal layer high density capacitor with a reasonable energy density and low parasitics [28]. Table 4 summarizes the parasitic capacitance factor α and maximum efficiency η of common capacitor types. A 0.1 value of α will mean that the parasitic capacitance is 10% of original value.

Table 4 Practical capacitor type properties [29].

Capacitor type	α	η (max) %
Poly-metal	0.2-0.5	50-64
Thin oxide	0.05-0.15	68-80
Double-poly	0.05	80
External	0.002	95.6

3 INTEGRATED IMPLEMENTATION OF SC DC-DC CONVERTER

Chapter 2 provided a basic theoretical knowledge related with switched capacitor converters. Performance differences of SC technique were compared with other conventional approaches. Moreover, different loss mechanisms associated with SC converters were elaborated in details. This knowledge will now form basis for the design of state of the art DC-DC converter presented in this chapter. Based on the current design needs, as presented in 1.3, key specifications for the required dc-dc converter are given in Table 2

3.1 Proposed Design

The proposed design for SC DC-DC converter is presented in Figure 3-1. Apart from SC power stage, the circuit requires additional blocks for operating as a DC-DC converter. A short explanation of these blocks with their intended operation is provided below.

3.1.1 Feedback Control Unit

Function of feedback control unit is to change the necessary parameters in clock generator based on the comparison of output voltage with a reference voltage. For example, if the output demands more current, feedback control unit can ask the clock generator to increase the clock frequency. Similarly, if Digital Capacitance Modulation feedback is used, control unit can ask the clock generator to insert additional capacitance for heavier load current demand. This is done by providing clock signal path to additional capacitance stage. Feedback control unit will also ask the clock generator to change the SC power stage topologies, by blocking clock to some transistors, in case load current/voltage requirements are not met.

One example of Digital Capacitance Modulation feedback algorithm is presented in Figure 3-2. Operation starts with initial charge transfer capacitance of 1x. Feeback compares the output voltage with two threshold voltages Vref+ΔV and Vref-ΔV. If the output voltage is lower than Vref-ΔV, either charge transfer capacitance or switching frequency Fs is increased to meet load demand. On the other hand, for output voltages higher than Vref+ΔV, SC structure switches to lower charge transfer capacitance values and/or lower switching frequencies.

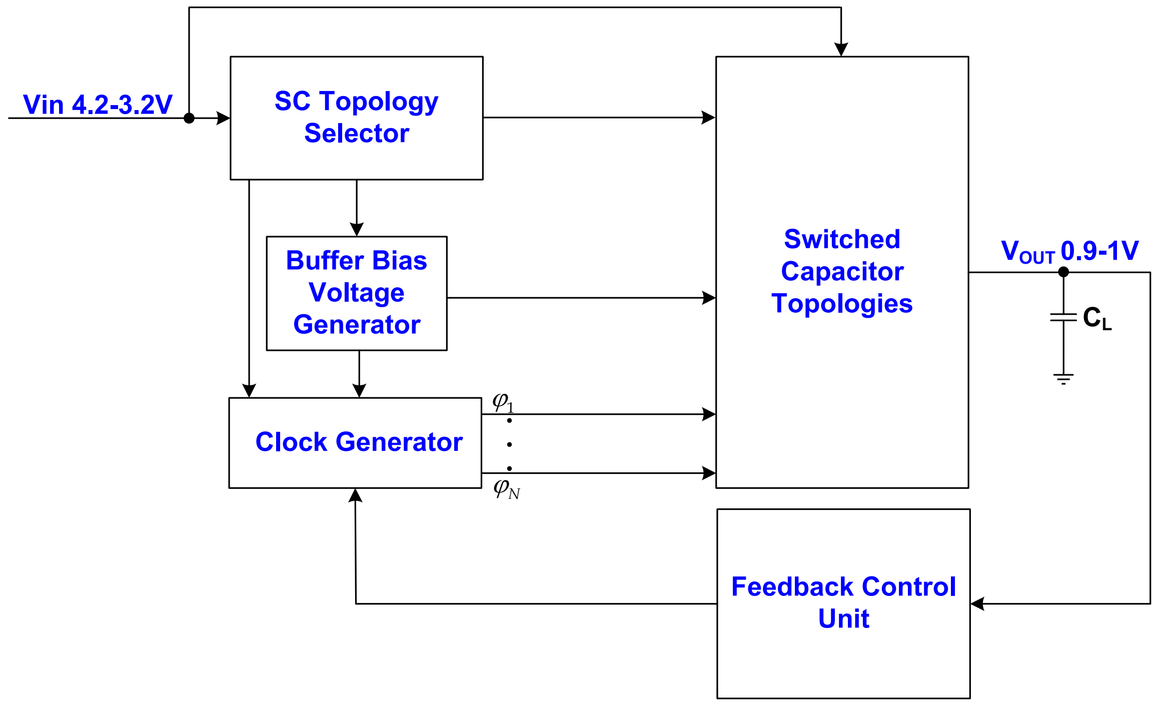

Figure 3-1. Proposed SC DC-DC converter block diagram

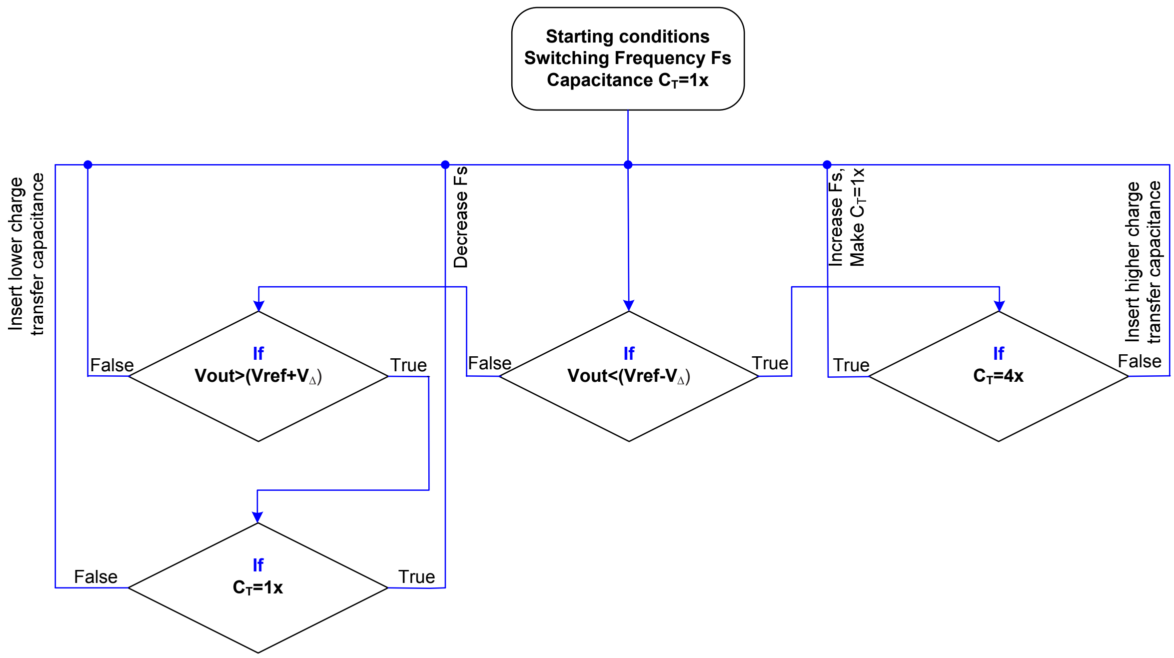

Figure 3-2. One example for DCM Feedback Algorithm

3.1.2 8-Phase Quadrature Clock Generator

The proposed SC topologies work with eight phase interleaving approach. Interleaving requires designing of eight phase quadrature clock generator. In addition to clock generation, the clock circuit should be able to block clock signals to some transistors in power stage. This is done in order to change the SC topologies.

A four stage differential ring oscillator was designed to implement the clock generator. Output of the clock generator is followed by level shifters in order to meet the requirements of some transistor clock voltages. Design of differential ring oscillator and level shifters in explained in detail in Section 3.7.

3.1.3 Topology Selector

SC topologies need to be switched based on the different input voltage requirements. This is required in order to preserve linear efficiency of converter. Topology selector

will compare input voltage with certain set of reference voltages and select certain topology which provides best possible efficiency for that range of input voltage.

3.1.4 Bias Voltage Generator

Additional bias voltages are required for buffer drivers attached with the power transistors. A separate internal bias voltage generator is required in order to generate these voltages. Design of bias voltage generator should take this fact into consideration that the bias voltages are in relation with input voltage. If the input voltage changes, some of the bias voltages in circuit should also change in same amount. For example a 1V increase/decrease in input voltage will require 1V increase/decrease in some of the bias voltages.

Next sections from 3.2 to 3.4 explain the design of SC power stage in more detail.

3.2 Topology Selection

Wide range of input voltage requirement poses a design challenge due to linear efficiency loss, given by equation (2.1). Different SC topologies need to be switched in the main circuit to preserve efficiency. For our design requirements three SC topologies 2/5, 1/3, and 2/7 were chosen for the varying input voltage requirements. Assuming 0.2-0.25 V ΔV is required to meet load current demands, calculations below show that the maximum theoretical efficiency will vary from 83.33 to 67.85%.

First Input Voltage Range: 3.2-3.5V
SC topology chosen: 2/5 V_L(required) = 0.95V

$V_{NL} @ 3.2 = (3.2).(2/5) = 1.28V$ $\eta = (1-(1.28-0.95)/1.28) = 74.21\%$

$V_{NL} @ 3.5 = (3.5).(2/5) = 1.4V$ $\eta = (1-(1.4-0.95)/1.4) = 67.85\%$

Second Input Voltage Range: 3.5- 4V

SC topology required: 1/3 V_L(required) = 0.95V

$V_{NL}@3.5 = (3.5).(1/3) = 1.16V$ $\eta = (1-(1.16-0.95)/1.16) = 81.89\%$

$V_{NL}@4 = (4).(1/3) = 1.33V$ $\eta = (1-(1.33-0.95)/1.33) = 71.42\%$

Third Input Voltage Range: 4-4.2 V

SC topology chosen: 2/7 V_L(required) = 0.95V

$V_{NL}@4 = (4).(2/7) = 1.14V$ $\eta = (1-(1.14-0.95)/1.14) = 83.33\%$

$V_{NL}@4.2 = (4.2).(2/7) = 1.2V$ $\eta = (1-(1.2-0.95)/1.2) = 79.16\%$

Figure 3-3 shows calculated theoretical linear efficiency for different input voltages

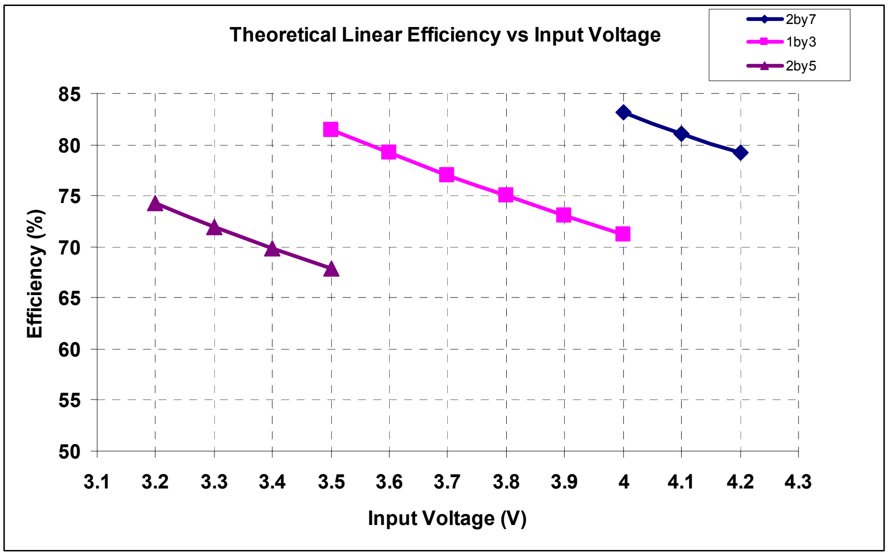

Figure 3-3. Theoretical linear efficiency versus Input voltage

The proposed 2/5, 1/3 and 2/7 topologies are presented in Figure 3-4. The combined topology was made by uniting all topologies together. During the operation of SC, these topologies will switch into the circuit depending upon the load and input voltage requirements. The operation of the above mentioned topologies is shown in Figure 3-5 to Figure 3-7.

During the φ_1, Load capacitor C_L is charged from battery voltage, through charge-transfer capacitors C_{T1} to C_{T4}. Charge transfer paths for each topology are shown by red arrows in respective figures. Similarly in φ_2, charge accumulated by charge transfer capacitors is transferred to load capacitor by connecting them together. Different capacitor arrangement in SC topologies results in the unique no-load voltages at the output.

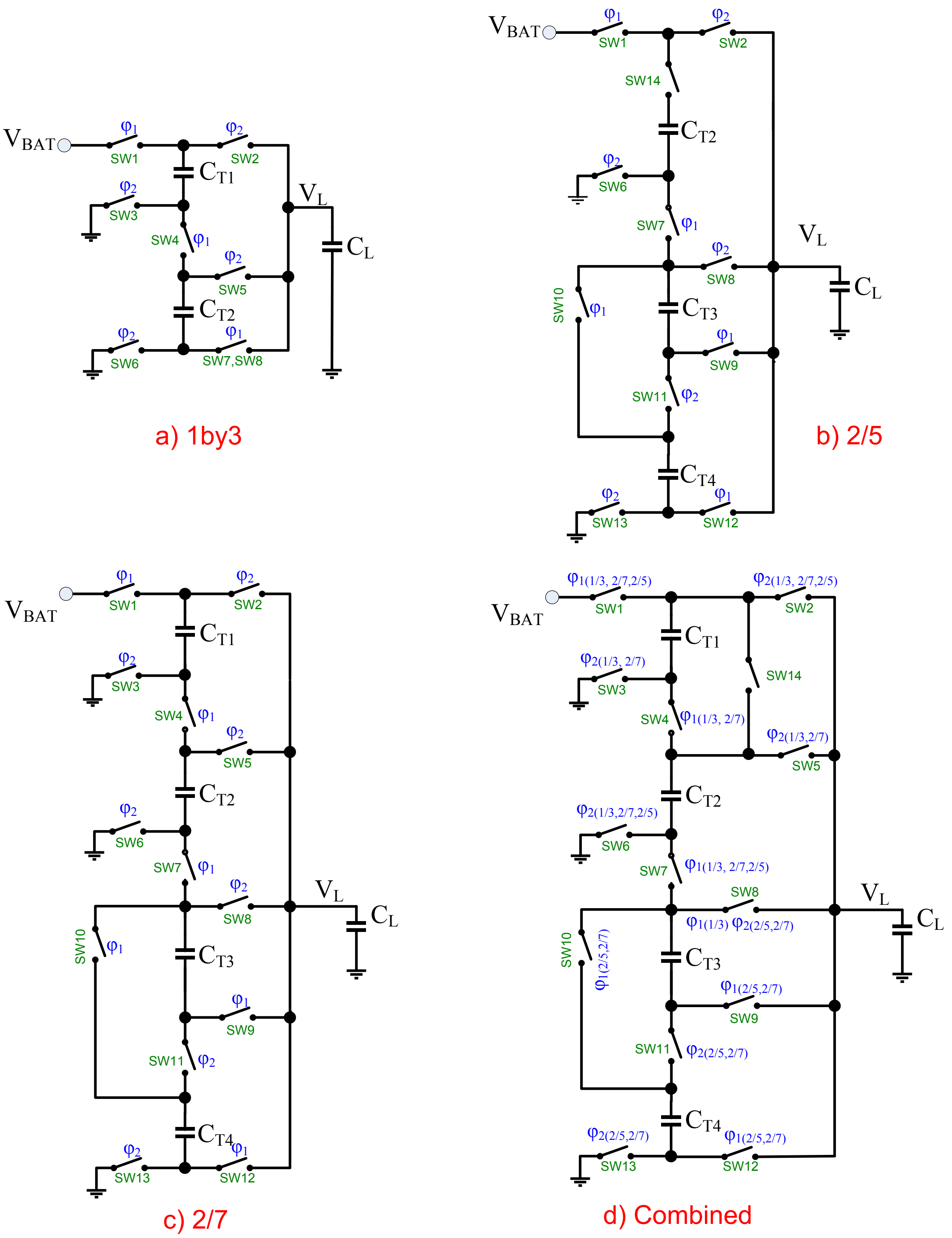

Figure 3-4. Proposed SC topologies for required design a) 1by3 b) 2/5 c) 2/7 d) Combined

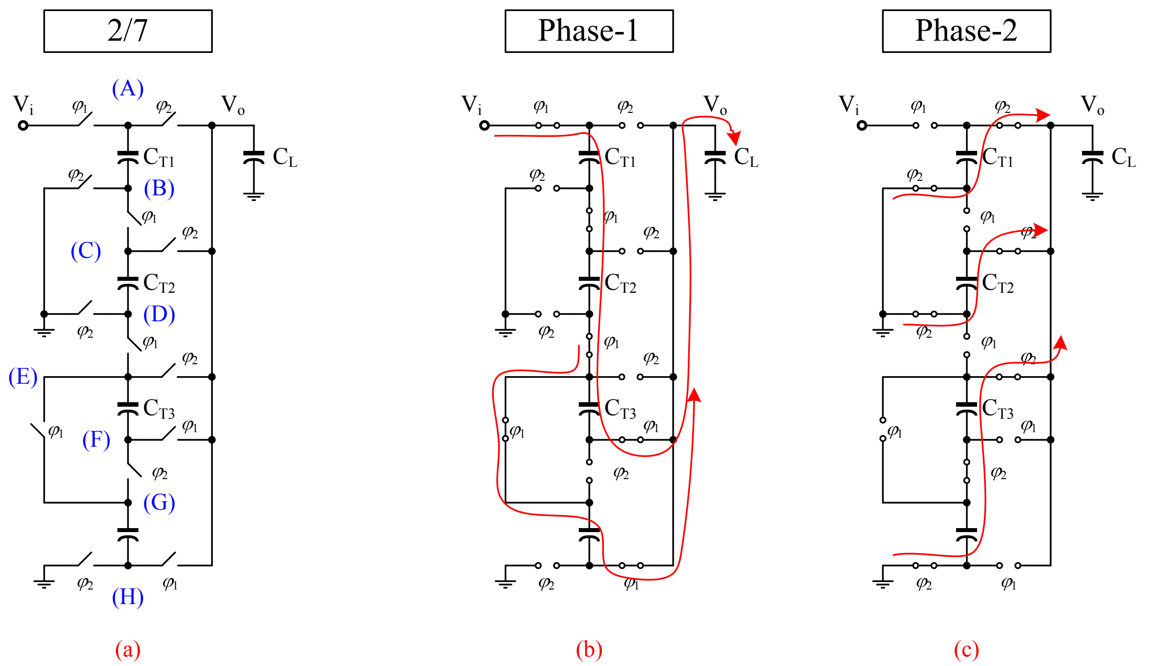

Figure 3-5. Working operation of 2/7 topology a) 2/7 topology b) phase 1 operation b) phase 2 operation

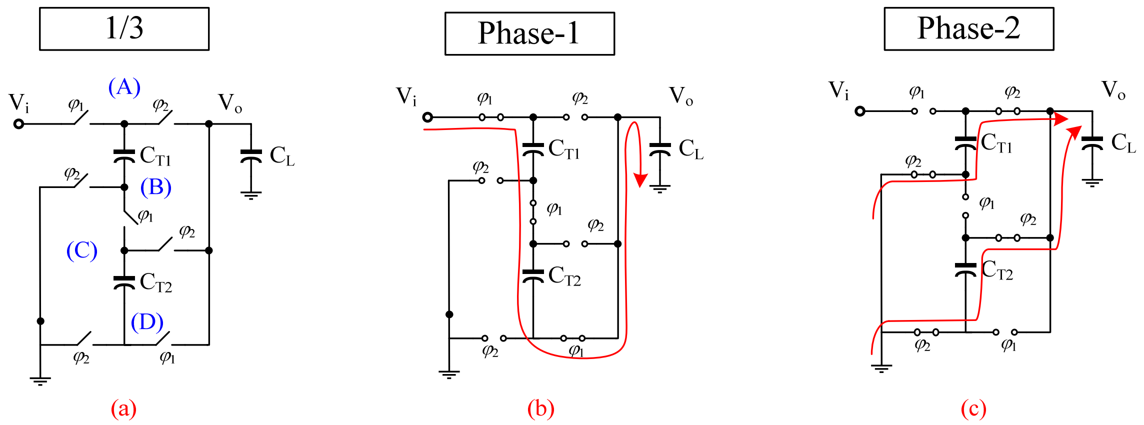

Figure 3-6. Working operation of 1/3 topology, a) 1/3 topology b) phase 1 operation b) phase 2 operation

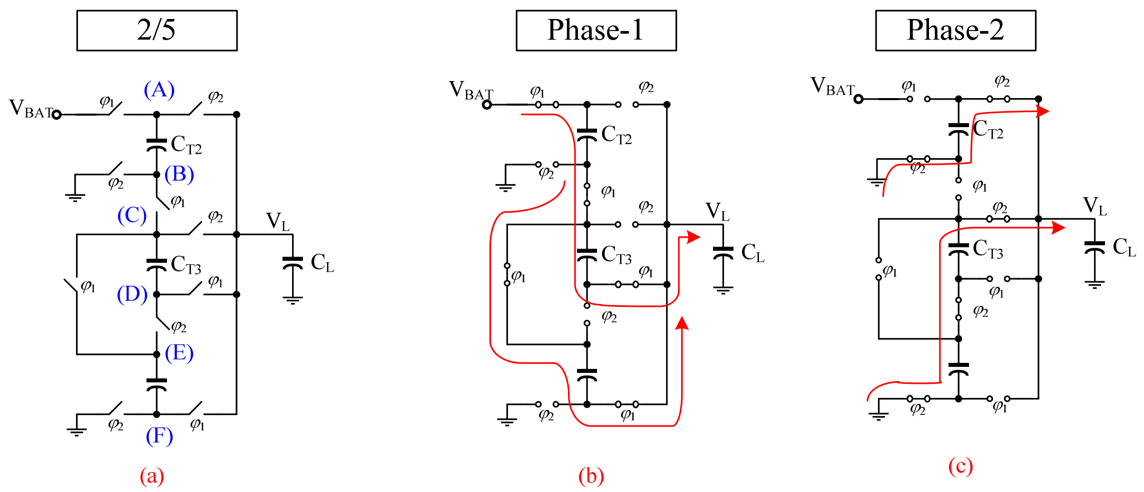

Figure 3-7. Working operation of 2/5 topology, a) 2/5 topology b) phase 1 operation b) phase 2 operation

During the closed loop operation of SC converter, above topologies will be configured in the main switching matrix based on the input voltage range and output voltage. If the output voltage falls below a certain value for a certain topology, a higher topology is needed to meet up the load current requirements.

The design of a closed-loop feedback circuit was not in the scope of this work. The selected topologies will be switched manually in simulations and measurements to check the performance for all voltage range.

3.3 Switch Implementation

Advanced CMOS processes with gate lengths of 45nm or lower possess a drawback of having break down voltages of 1.8V or lower. Currently many of the portable electronics devices are operated from Li-ion batteries whose voltages can go up to 4.2V. Therefore, design an integrated DC-DC converter operating at such higher input voltages becomes a challenge due to lower MOS breakdown voltages.

One solution of above problem is to use cascoded MOS structures. The idea is to connect the MOS transistors in cascoded configuration so that the overall voltage across the single MOS transistor does not go beyond 1.8V. As an example, consider 2/7 topology shown in Figure 3-8. During the circuit operation, maximum and minimum possible voltages appearing at different nodes are shown in blue color. These voltages are calculated with assumption of no-load condition and ideal switches. It can be seen that SW1, SW2 and SW3 have maximum voltage of 3V across them. Therefore, transistor implementation of these switches, need to be cascoded in order to eliminate breakdown conditions.

Some practical limitations still remain in cascoded implementation of transistors. Firstly, in order to provide the same on-resistance, transistor sizes in cascoded implementation will be approximately double than their normal size, which will result in bigger size of overall layout. Secondly, the clock signal requirements will become complex for the cascoded implementation.

The choice of using NMOS or PMOS depends on the specific location of MOS switch in the SC configuration. In normal cases, NMOS implementation is preferred over the PMOS because of higher mobility and smaller size for the same on-resistance. This choice is also dictated by the ease of gate drive voltage generation. In some cases of SC implementation, PMOS transistor was preferred over NMOS because the drive voltages were easier to generate from level shifters. 2/7 SC converter topology with MOS switch implementation is shown in Figure 3-9.

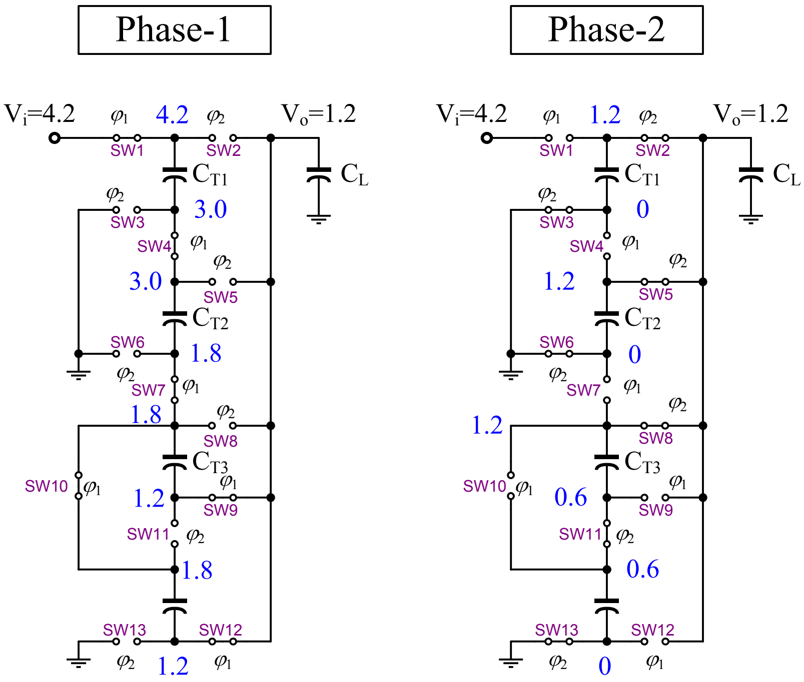

Figure 3-8. Maximum voltage conditions for 2/7 topology

SW1, SW2 and SW3 have been implemented using cascoded transistors SW1a, SW1b, SW2a, SW2b, SW3a, and SW3b respectively. This was decided by observing the drain to source voltage V_{DS}, gate to source voltage V_{GS}, and gate to drain voltages V_{GD}, across the MOS transistors, at highest input voltage of 4.2V. The voltage across SW1-3 in such condition is 3V at no load condition. Therefore, connecting two MOS transistors in cascode, each rated 1.8V, avoids breakdown conditions.

3.4 Capacitor Selection

As discussed in section 2.3.2, bottom plate capacitance can be a major loss component in SC topologies, where floating capacitors are used. Proposed design in this work is quite sensitive to bottom plate capacitance loss due to presence of floating capacitors. Moreover, high current at output demands the need for high density capacitor. These two requirements made the selection of the capacitors quite challenging.

Three types of integrated capacitors, namely Metal-Insulator-Metal (MIM), Metal-Oxide-Semiconductor (MOS) and Metal-Oxide-Metal (MOM), were analyzed for the proposed design. Table 5 shows the advantages and disadvantages of these capacitors for integrated implementation.

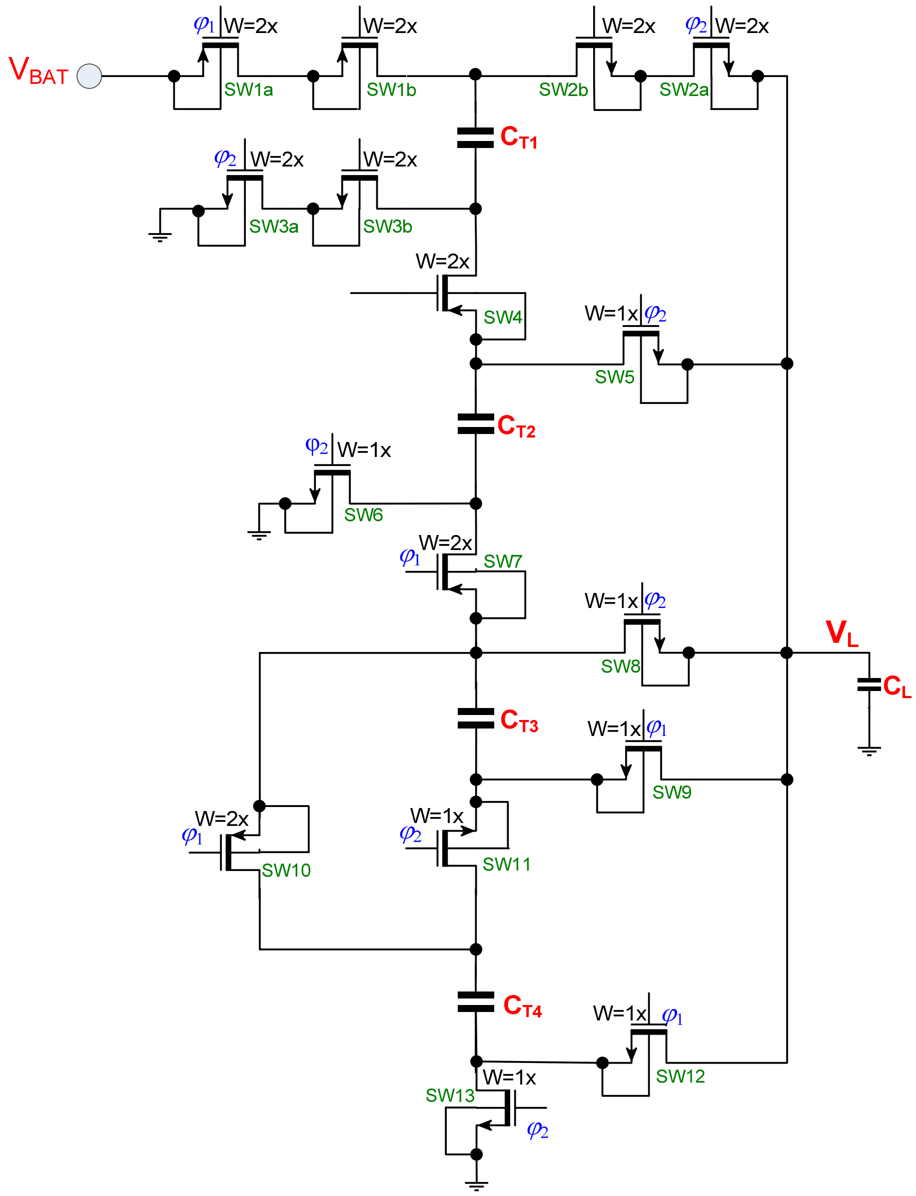

Figure 3-9. MOS implementation of 2/7 topology

Table 5 Integrated Capacitors advantages/disadvantages

Capacitor type	Pros	Cons
MOS capacitor	• High capacitance density 7-9 fF/um^2	• Higher bottom Plate capacitance 5-15% [29]. • Non-linear CV curve
MOM capacitor	• Higher capacitance density then MIM cap.~ 3.8-4.4fF/um^2 • Linear CV curve	• Higher Bottom plate capacitance then MIM capacitors
MIM Capacitor	• Low bottom plate capacitance • Linear CV curve	• Smaller capacitance density.~ 1-2 fF/um^2

In regard of smaller bottom plate capacitance, MIM capacitors offer the best choice. However, MIM capacitors are not suitable in higher current designs due to extremely bigger size. On the other hand, MOS capacitor, offer the best possible capacitance density, but it has high bottom-plate capacitance. Simulation results showed a drastic decrease in efficiency from 70% to 44% because of the MOS capacitor bottom plate capacitance. Therefore, a compromise was made to choose MOM capacitors which offer acceptable capacitance density and lower bottom plate capacitance at the same time.

MOM capacitor still consumes a huge portion of silicon chip. Standard eight phase Interleaving has been adopted to lower the output capacitor size for the required output ripple. In addition, output current specifications have been lowered from 100mA to 16mA in order to keep the chip size in practical limits.

Cadence design kit did not have a simulation model available for MOM capacitor so the value of capacitor was calculated using simple assumptions provided below. See Figure 3-10 for reference.

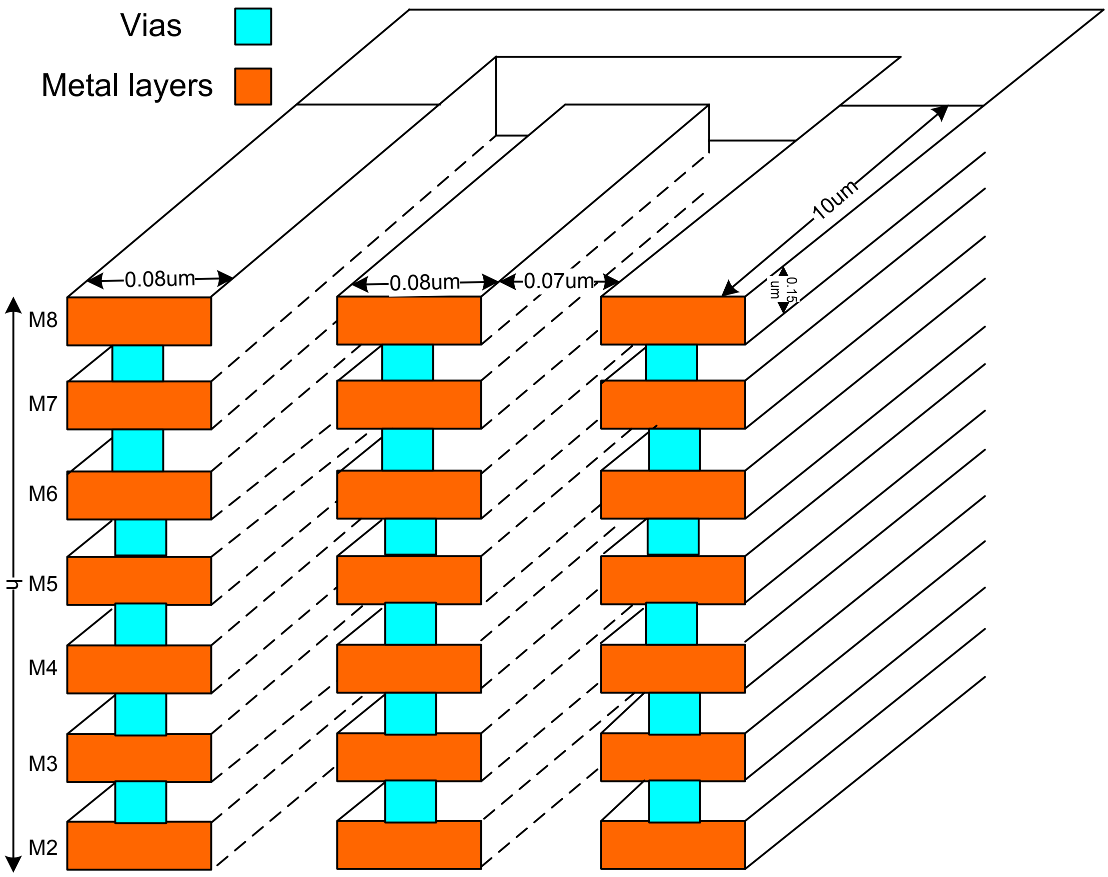

Figure 3-10. Metal Insulator Metal (MOM) capacitor physical structure

Metal Layer 2-8 thickness T_M= 0.15um [35]
Dielectric (between metal layers) thickness T_D = 0.30um [35]

Dielectric relative permittivity ε_r = 2.6 [35]
Metal Layer width W_M= 0.08um (minimum possible width) [33]
Metal Layer Length L_M= 10um (assumption)
Separation between adjacent Metal layers d =0.07um (minimum possible separation)

Assumption: Space covered by Vias is approximately half the area of metal layers. Therefore, the effective dielectric thickness becomes half of its original value i.e. 0.30um/2 = 0.15um

Overall height 'h' of M2-M8 MOM capacitor can be calculated as:

$$\text{Height h} = (0.15\mu m)(7) + \left(\frac{0.30\mu m}{2}\right)(6) = 1.95um \tag{3.1}$$

Overall area of one side of MOM cap plate 'A'

$$= h.L_M = (1.95\mu m)(10\mu m) = 19.5\mu m^2 \tag{3.2}$$

$$\text{Capacitance } C = \frac{A\varepsilon_o\varepsilon_r}{d} = \frac{(19.5\mu m^2)(8.85\times10^{-12} F/m)(2.6)}{0.07\mu m} = 6.41 fF \tag{3.3}$$

Effective area of single MOM structure

$$= (0.08\mu m + 0.07\mu m)(10\mu m) = 1.5\mu m^2 \tag{3.4}$$

$$\text{Capacitance density} = \frac{6.41 fF}{1.5\mu m^2} = 4.27 fF/\mu m^2 \tag{3.5}$$

$$\text{Parasitic capacitance area } A_{par} = 2.W_M.L_M = (2)(0.08\mu m)(10\mu m) = 1.6\mu m^2 \tag{3.6}$$

$$\text{Parasitic Capacitance } C_{par} = \frac{A_{par}\varepsilon_o\varepsilon_r}{d} = 81.8aF \tag{3.7}$$

$$\text{Percentage bottom plate Capacitance} = \frac{C_{par}}{C} = 1.28\% \tag{3.8}$$

Above calculations show that MOM capacitors are superior to MIM capacitors in terms of capacitance density. In addition, bottom plate capacitance is comparable to MIM capacitor values.

3.5 Driver Design

In integrated implementation of MOS switches, NMOS is preferred option over PMOS due to higher mobility and smaller on-resistance R_{on}. Initially all MOS switches in main SC configuration were implemented using NMOS except SW1. This resulted in six different drive voltages for gate clocks, mentioned below. Moreover, three additional bias voltages were required for SW1b, SW2b, and SW3b.

- Vin to Vss
- Vin to Vin-Vdrive
- V_L+ Vdrive to V_L
- Vdrive to Vss
- 2 Vdrive to Vss
- V_L+ Vdrive to Vss

Here Vin is the input voltage, Vss is ground potential and Vdrive is the optimum V_{GS} voltage.

Additional complex circuitry is required to generate above different voltage, clock signals. Therefore, in order to make the clocking requirement simple, some MOS transistors were replaced with PMOS transistors. Moreover, buffer driver design also reduced the number of different clock voltage requirements. In the final circuit, only three clock voltages and some constant bias voltages are required for proper operation. Final clock voltage requirements are mentioned below:

- Vin to Vin-Vdrive
- 2Vdrive to Vdrive
- Vdrive to Vss

Voltage levels of above clocks are presented in Table 11. Based on above clock requirements, three different buffers were designed to meet design needs. Among them, two buffer designs have no difference except the size of MOS transistors. Third buffer was designed as cascoded structure to operate at clock swings greater than breakdown voltage. Figure 3-12 and Figure 3-11 show the designed buffers for SC converter.

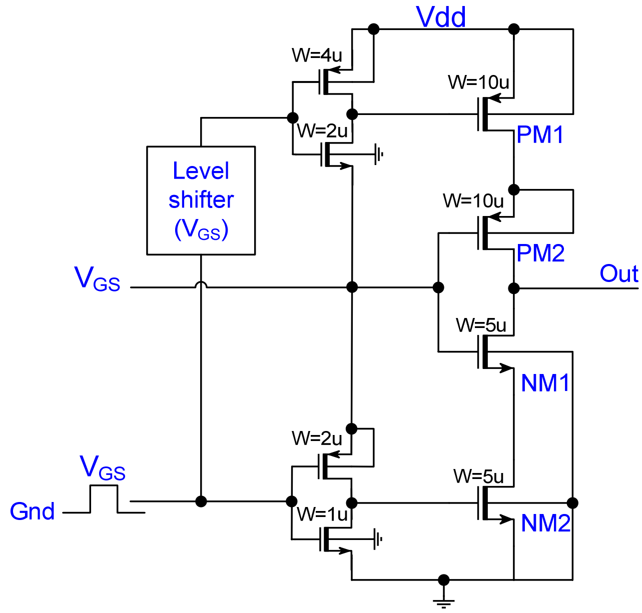

Figure 3-11. Cascoded buffer design for clock voltages above breakdown limit [32]

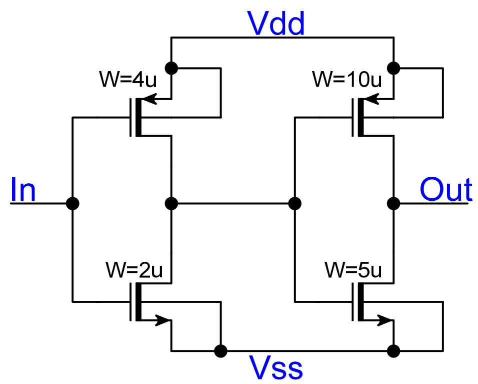

Figure 3-12. Buffer driver design

3.6 Ripple Reduction

Eight phase standard interleaving was used to reduce the output ripple within the required specifications. It also reduced the output capacitor value for required ripple hence reducing the overall layout size.

Each interleaved stage was optimized to provide 2mA output current so that the overall output current from all eight interleaved stages became 16mA. Clock signals to each interleaved stage was delayed T/8, where T is the time period of clocking signal.

3.7 Clock Generator Design

Proposed SC topologies operate in eight phase interleaving operation. Eight phase interleaving requires the need to design eight-phase quadrature clock generator. A four stage differential ring oscillator was implemented to meet the clock generation requirements [33]. Circuit diagram is shown in Figure 3-13.

Circuit works by connecting four differential inverters connected in closed loop with each other. Output frequency of oscillator can be controlled by changing the reference current of current source made by M7 and M8. Alternatively, frequency can also be adjusted by changing the load capacitances in ring oscillator. In circuit implementation only reference current was varied from outside the chip to tune the frequency.

Eight clock signals are taken from the output of ring oscillator namely POSa, POSb, POSc, POSd, NEGa, NEGb, NEGc and NEGd. Each successive clock signal is 90 degrees phase shifted from each other meeting the requirement of eight phase clock generator. Moreover, POS and NEG clocks are 180 degree phase shifted with each other meeting quadrature requirements. These signals are used to drive the two different phases of SC topologies.

Circuit diagram of single stage differential inverter is shown in Figure 3-14. Transistors M5 and M6 are auxiliary transistors used to make the POS and NEG signals 180 degrees phase shifted with each other. The size of M5 and M6 can be around 3-4 times smaller than main transistors in inverter stage.

Output of the Ring oscillator was supplied to an AND gate with enable (EN) pin. AND gate is designed for two reasons: 1) it provides buffering of the clock generator and produces clocks with sharper edges. 2) it provides additional control from outside for enabling/disabling clock generator. In some feedback approaches like Pulse Frequency modulation (PFM), EN pin can be used to regulate the output voltage of SC power stage at a fixed level. For example EN pin can be connected to output of comparator, which

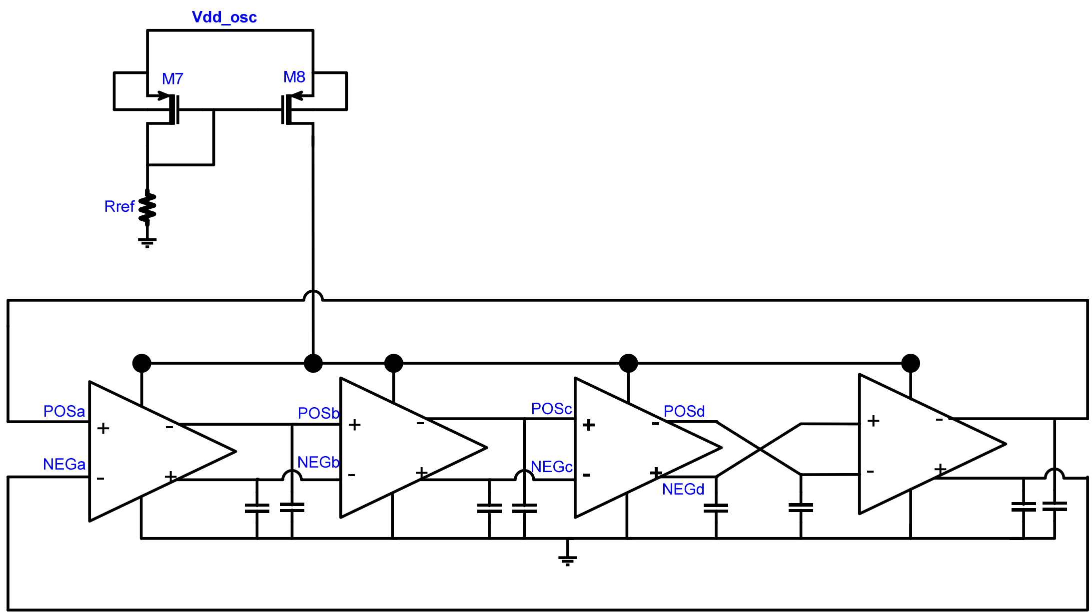

Figure 3-13. Four Stage Differential Ring Oscillator for Clock generation [33]

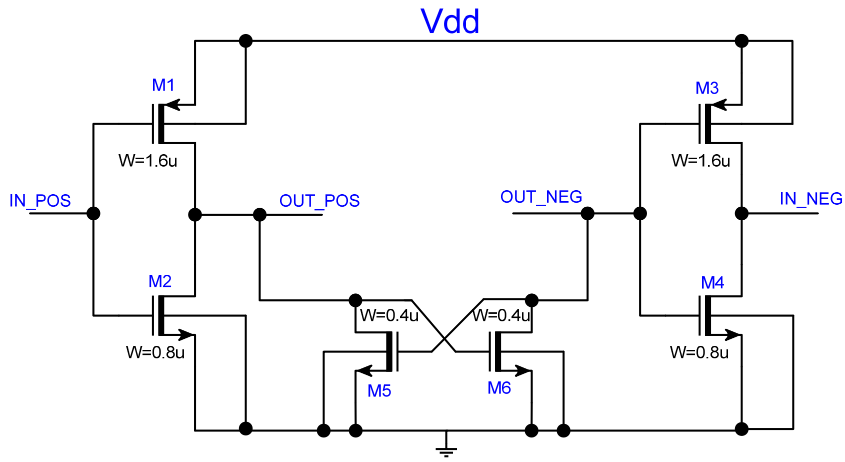

Figure 3-14. Single stage of differential ring oscillator

will disable the clock signal incase output voltage goes above a certain threshold. Circuit diagram of designed AND Gate is presented in Figure 3-15.

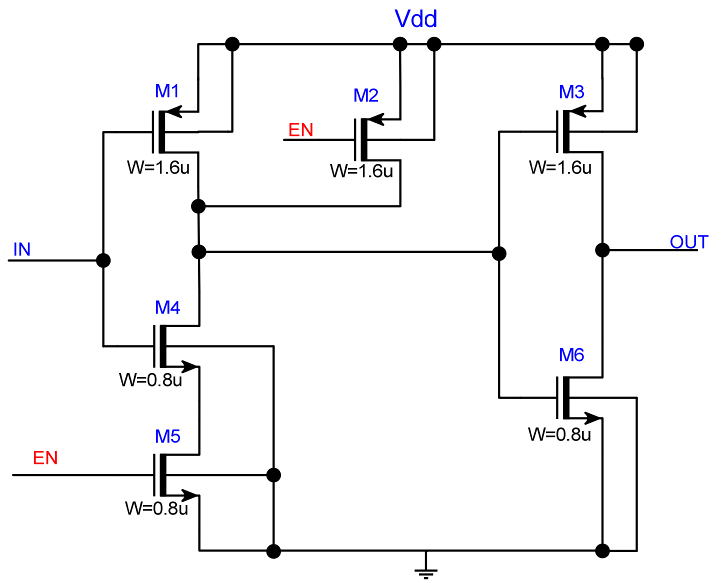

Figure 3-15. AND Gate implementation

3.8 Level Shifter Design

Some transistors in SC stage require different clock voltage requirements to operate. This poses the design requirement of level shifter which should switch the clock voltage of Vdrive to Gnd to following additional clock voltages:

Vdd to Vdd-Vdrive (Level shifter of Vdd Volts required)
Vdrive to 2Vdrive (Level shifter of Vdrive Volts required)

Here Vdrive is the optimum value of gate to source voltage V_{GS} at which the efficiency was maximum. Table 6 shows the drive requirements for different transistors in SC topologies.

Table 6 Drive voltage requirements for some transistors

Transistors	Drive voltage requirements
SW1a	Vdd to Vdd-Vdrive
SW1b	Constant dc voltage VbiasSW1b
SW2a	Vdrive to 2Vdrive
SW2b	Constant dc voltage VbiasSW2b
SW3a	Vdrive to Gnd
SW3b	Constant dc voltage VbiasSW3b
SW4	Constant dc voltage VbiasSW4b
SW5	Vdrive to 2Vdrive
SW6	Vdrive to Gnd
SW7	Vdrive to Gnd
SW8	Vdrive to 2Vdrive
SW9	Vdrive to Gnd and Constant dc voltage Vbias18
SW10	Vdrive to Gnd
SW11	Vdrive to Gnd
SW12	Vdrive to Gnd
SW13	Vdrive to Gnd
SW14	

Design of level shifter is taken from [34] and is shown in Figure 3-16. Capacitor C_{LS} AC couples the V_{drive}-GND clock signal while resistor R_{LS} biases the buffer driver at its trip point. More explanation for circuit functionality can be found from same reference [34].

Figure 3-17 shows the overall circuit consisting on SC power stage and clock generator. It also shows the IC signals which will be provided at outside pins.

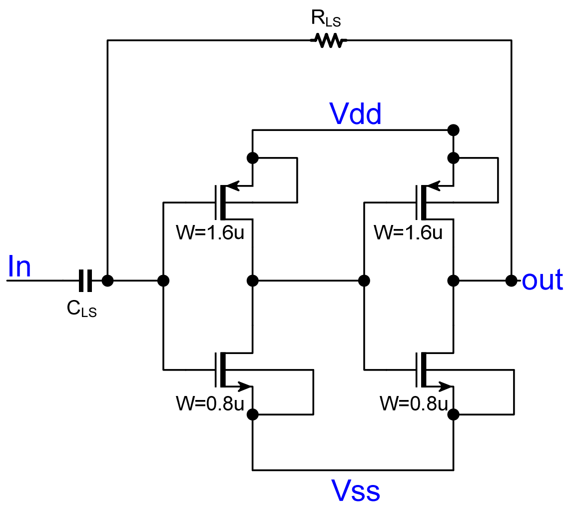

Figure 3-16. Level shifter design [34]

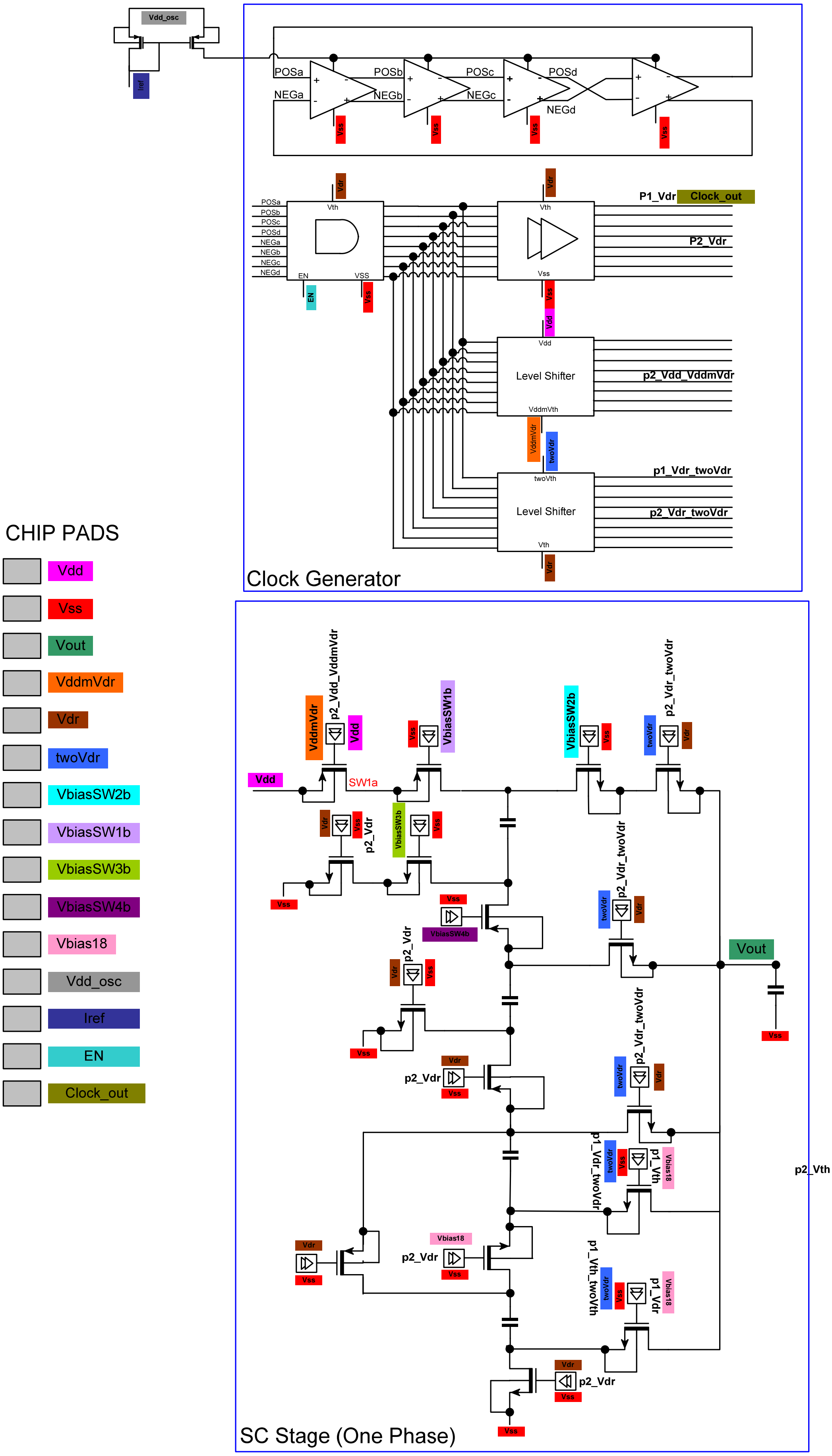

Figure 3-17. Overall circuit diagram

3.9 Simulation results

Initially, circuit was designed with ideal capacitors and 25mA output current. The idea was to use four phase interleaving where each stage provides 25mA output current. Later on, based on detailed simulation results, it was realized that four phase interleaving approach is not able to meet the ripple specification. Therefore, design shifted to eight phase interleaving, where each stage provided 12.5mA. Figure 3-21 shows interleaving results for SC converter. It should be noted down that interleaving simulations were carried out by keeping output current from all devices constant at a specified value. This was done to ensure proper comparison of interleaving results. Apart from output ripple, number of interleaved stages did not affect much on overall efficiency.

Frequency versus open loop efficiency and Power loss for one phase design is shown in Figure 3-18. Conditions: Transistor Width 500um, Output current 25mA and Input Voltage 4.2V.

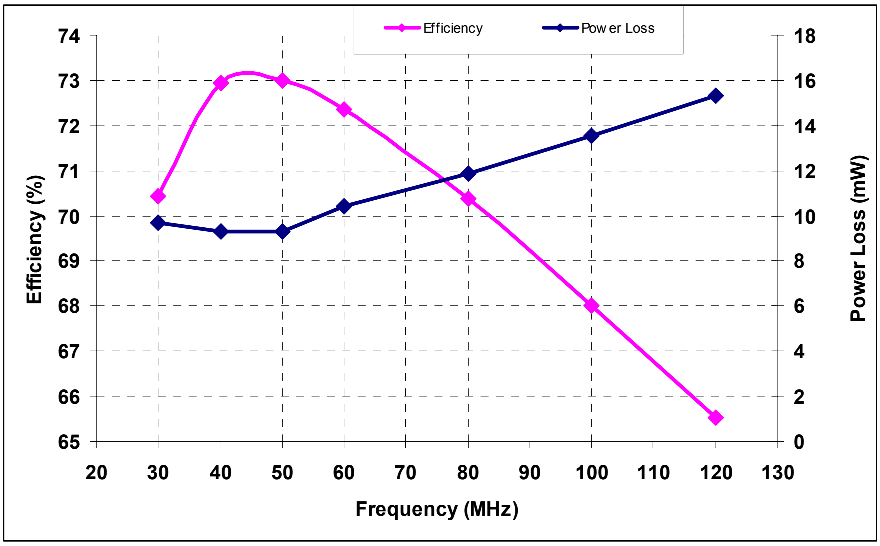

Figure 3-18. Frequency versus Efficieny and Power loss

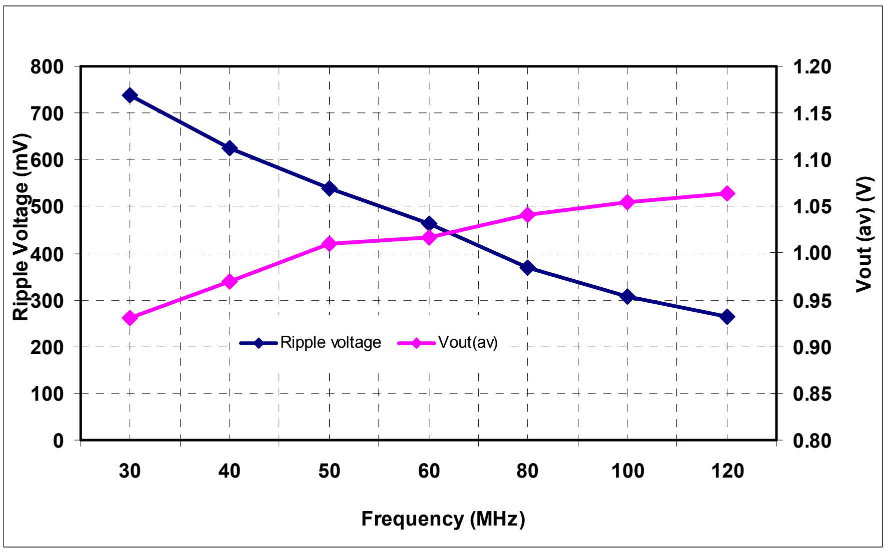

Figure 3-19. Frequency versus Ripple voltage and Vout (av)

Results presented in Fig. Figure 3-18 show that the maximum efficiency occurs between 40 to 50 MHz. However, ripple voltage reduces with increase in frequency, as shown in Figure 3-19. Switching frequency of 60MHz was chosen for desired operation as it gives a good compromise between efficiency and ripple specifications.

Transistor width was also optimized for best possible efficiency. Figure 3-20 shows the Transistor Width versus Efficiency and Average output voltage for Input voltage 4.2V and output current of 12.5mA. At 200um transistor width, efficiency is maximum and it starts decreasing after that. This is obvious from theoretical point of view, because after certain increase in width, parasitic capacitance losses will dominate the efficiency increase due to decreasing on-resistance R_{ON}. On the contrary, average output voltage keeps on increasing with increasing transistor width due to smaller transistor on-resistance at bigger transistor widths.

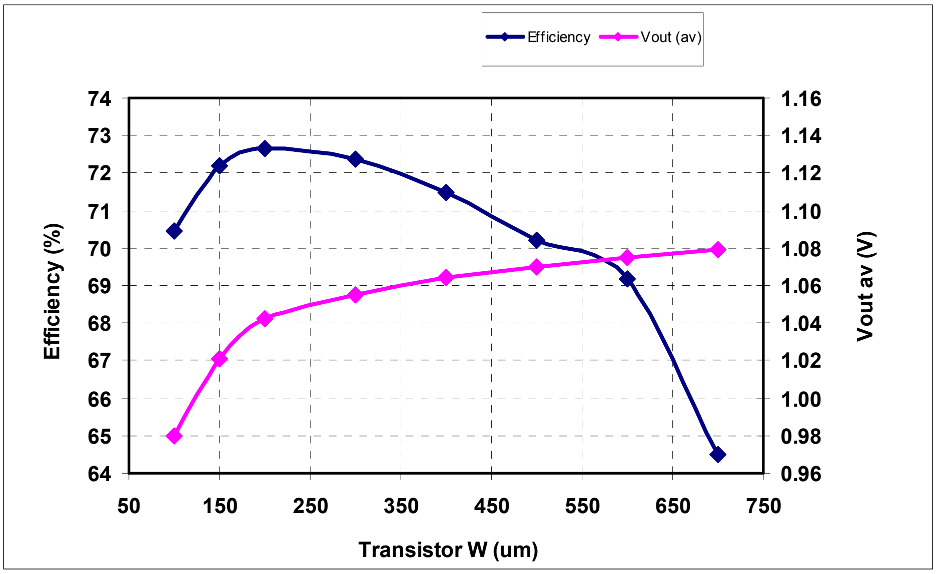

Figure 3-20. Transistor width versus. Efficiency and Average output voltage

Later on when the current specifications were changed from 100mA to 16mA due to size constraints of integrated capacitors, the optimum width of the transistors was scaled down linearly in the same proportion of current, to get the best possible efficiency. Final design has transistor width of 40um with each interleaved stage providing 2mA for eight phase structure.

Detailed analysis of power loss in the SC configuration showed SW4 and SW7 consumed more power than the rest of the transistors. Therefore, in order to reduce the on-resistance, SW4 and SW7 widths were made twice than the normal transistors. After this change, efficiency value, with ideal component simulation, increased from 71.3 % to 72.18% for input voltage of 4.2V.

Table 7 shows the power loss data for one phase SC topology, with simulation conditions of 60MHz clock frequency and load current of 25mA.

Figure 3-22 shows the effect of Vgs voltage on driver loss. Simulation was done at output current of 12.5mA per phase for eight phase interleaving and clock frequency of 60MHz. It can be seen that the driver loss has pronounced effect on the overall efficiency including driver loss. At Vgs voltage of 1.3 V, optimum efficiency is achieved.

Table 7 Simulation results for power loss in different transistors

Transistors	SW4, SW7 with normal widths	SW4, SW7 with twice bigger widths
SW1a	0.838	0.875
SW1b	1.148	1.067
SW2a	0.569	0.572
SW2b	0.987	0.982
SW3a	0.478	0.481
SW3b	0.788	0.78
SW4	0.896	0.606
SW5	0.623	0.614
SW6	0.513	0.503
SW7	0.816	0.525
SW8	0.148	0.147
SW9	0.361	0.431
SW10	0.111	0.126
SW11	0.132	0.138
SW12	0.243	0.27
SW13	0.161	0.161
SW14	0.267	0.281
Efficiency	71.3	72.2

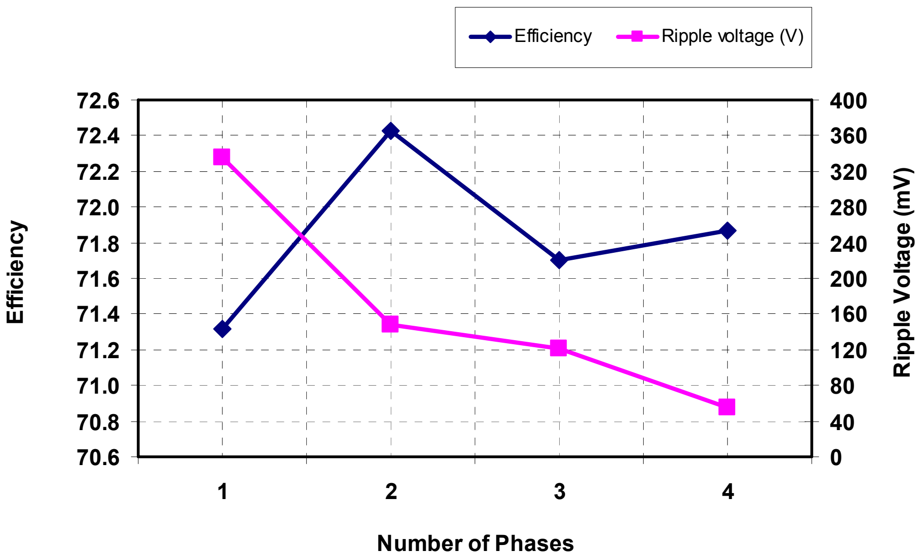

Figure 3-21. Interleaving effect on output ripple

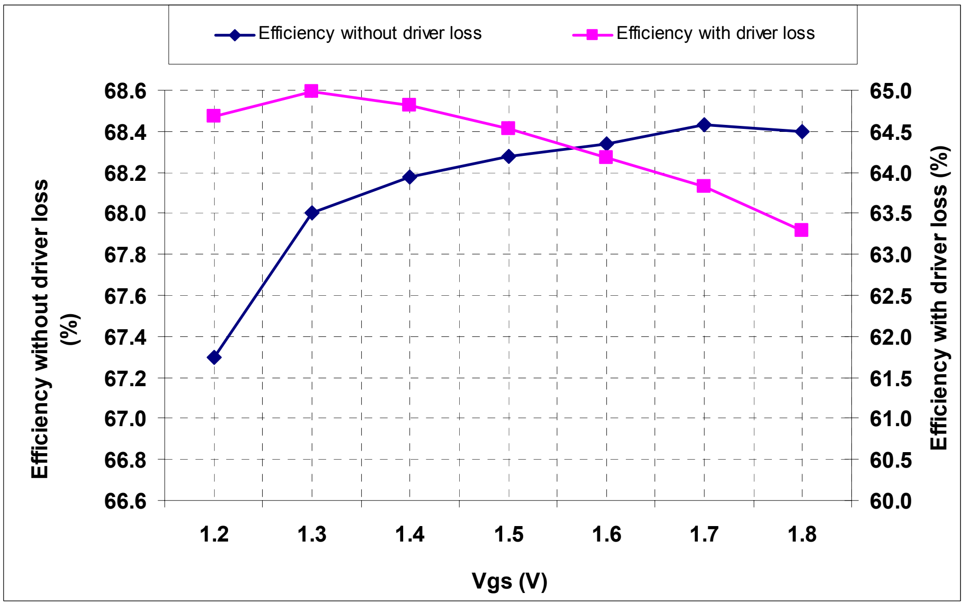

Figure 3-22. Driver loss versus Vgs voltage

Based on the Vgs voltage simulations in Figure 3-22, all gate drive voltages in the SC topologies were changed from 1.8V to 1.3V. This resulted in the increase of efficiency from 69.1 % to 70.12% in final design for 4.2V input.

Initial design simulations were carried out by ideal capacitor with 1% bottom plate capacitance. Figure 3-23 show the effect of bottom plate capacitance on efficiency.

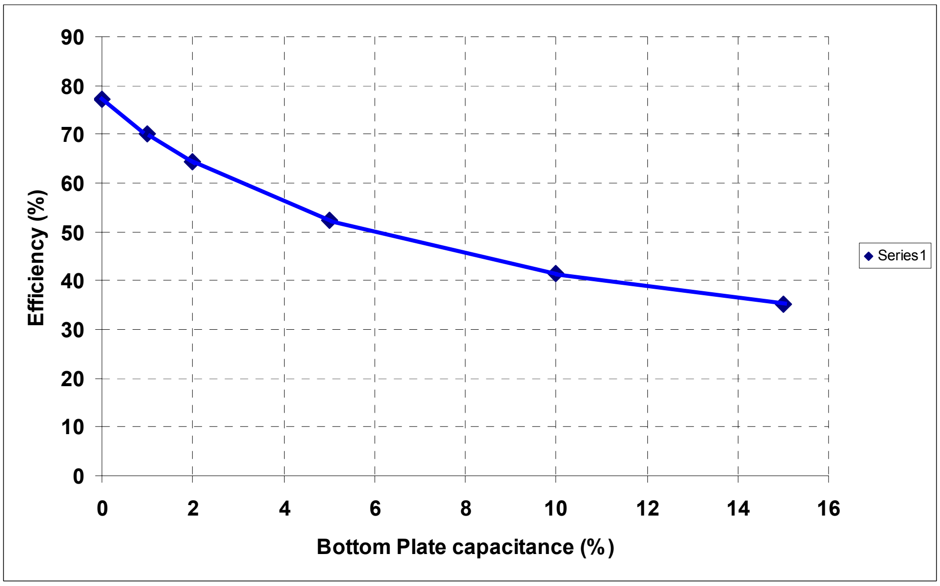

Figure 3-23. Bottom Plate capacitance effect on Efficiency

It can be easily observed that the SC topology is quite sensitive to bottom plate capacitance value. Therefore, using MOS capacitors for integrated implementation was out of consideration because of there high bottom plate capacitance value. On the other hand, MIM capacitor provides lower bottom plate capacitance value but one MIM charge transfer capacitor implementation for 100mA design consumed 0.195mm^2 area. In eight phase structure where we have 32 of such capacitors, MIM capacitor becomes inappropriate in terms of silicon space. A compromise was then made to reduce the size of SC configuration within specified limit. Firstly, MOM capacitors were implemented which offer smaller size and lesser bottom plate capacitance at the same time. Second, design specifications of 100mA were reduced from 100mA to 16mA to reduce the overall capacitance size.

Figure 3-24 show the open-loop efficiency versus Input voltage for the final design without including parasitic effects. Comparing the results in Figure 3-24 with Figure 3-3 shows that the simulated results do not match with the theoretical linear efficiency. The reason for this difference was due to the fact that in open-loop, output voltage does not remain constant with changing input voltage. For proper efficiency versus input voltage comparison, output voltage must remain constant.

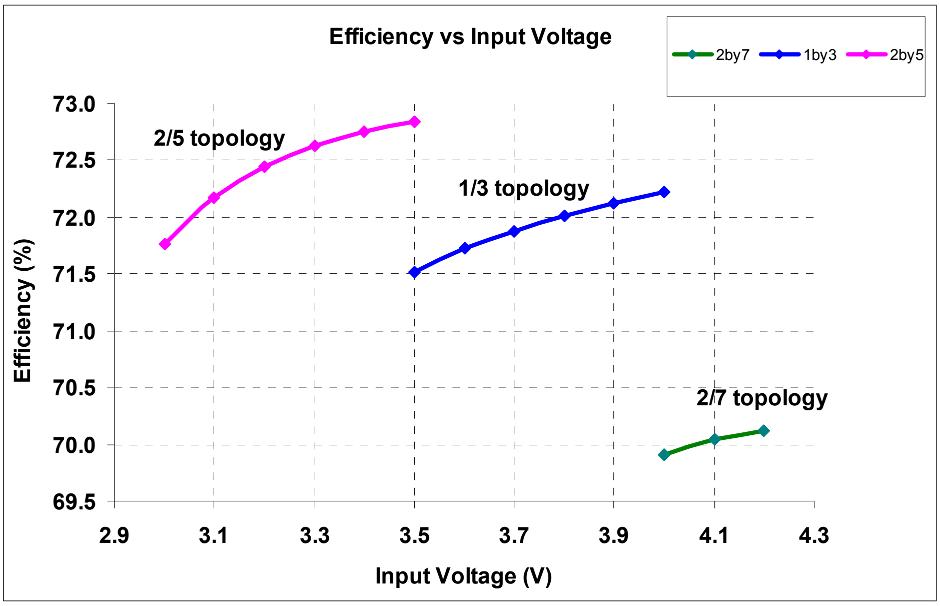

Figure 3-24. Simulated Efficiency versus Input Voltage

Therefore, for efficiency versus input voltage comparison, another set of simulations was carried out by keeping output voltage constant through clock frequency adjustment. The new set of results now follow the theoretical trend of linear efficiency and are shown in Figure 3-25. On the other hand, Figure 3-26 shows the power loss versus input voltage for SC topologies.

Figure 3-27 shows the simulated tuning curve for differential ring oscillator circuit.

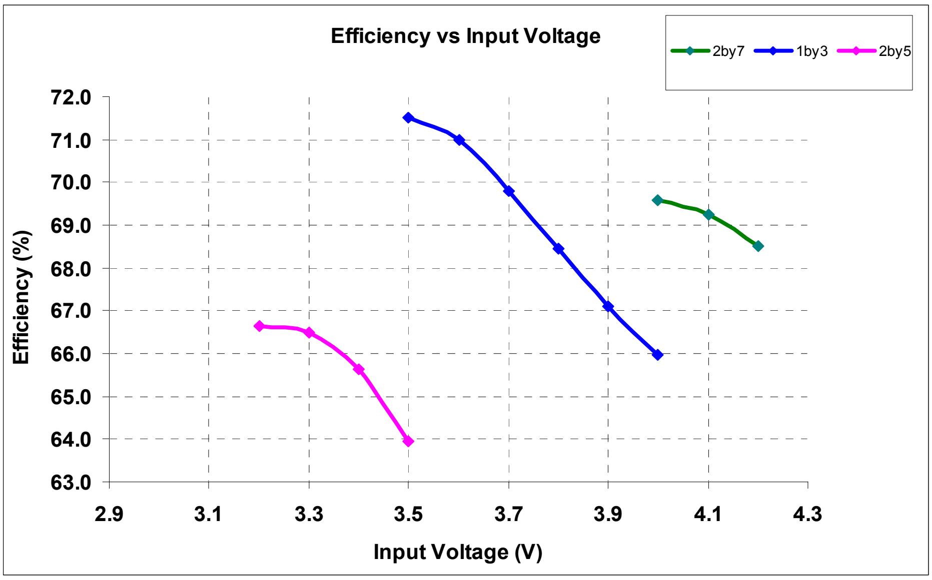

Figure 3-25. Efficiency versus Input Voltage while keeping output voltage constant

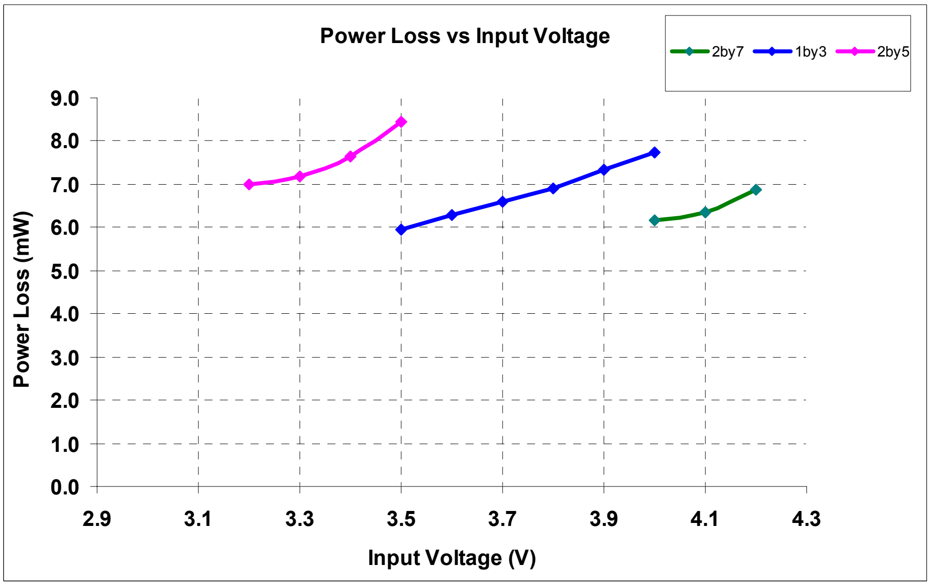

Figure 3-26. Power Loss versus Efficiency while keeping output voltage constant

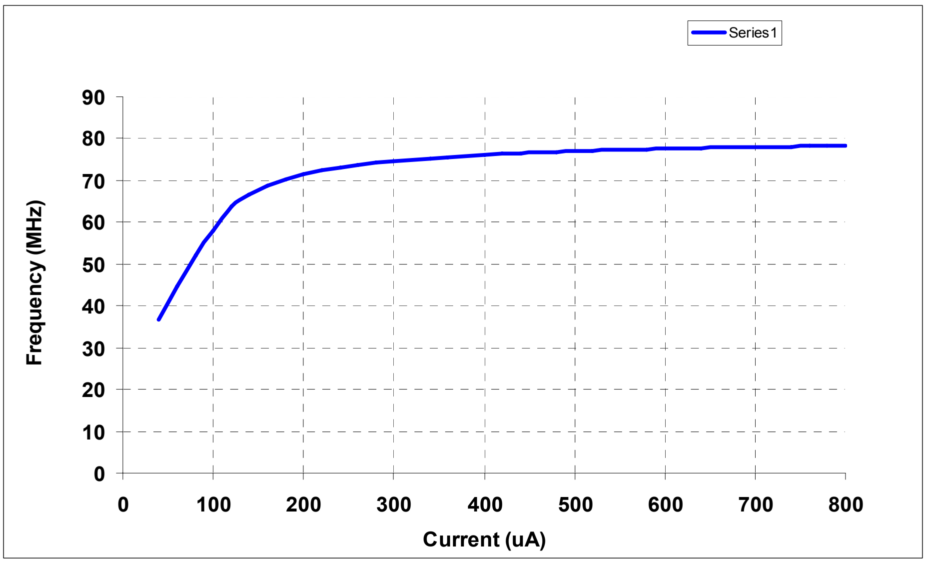

Figure 3-27. Ring oscillator tuning curve

Final design operates in eight phase interleaving with each stage optimized to 2mA output current. Some of the important parameters for final design are mentioned in Table 8 below:

Table 8 Final design circuit parameters

Parameter	**Value**
Clock Frequency	60MHz
Transistor Width	40um/80um
Transistor Gate Length	150nm
Charge-transfer capacitance per phase	140pF
Load Capacitance	190pF
Maximum output current	16mA
Output Ripple Voltage	25mV approx

Efficiency versus Input voltage for final design including internal and PCB parasitics is shown in Figure 3-28 while Figure 3-29 shows the efficiency versus load current for same circuit.

Figure 3-30 shows the output ripple voltage characteristics of final design for 16mA output current. Output waveform is not smooth because of addition of various internal and PCB parasitics, which effect the ripple performance of converter.

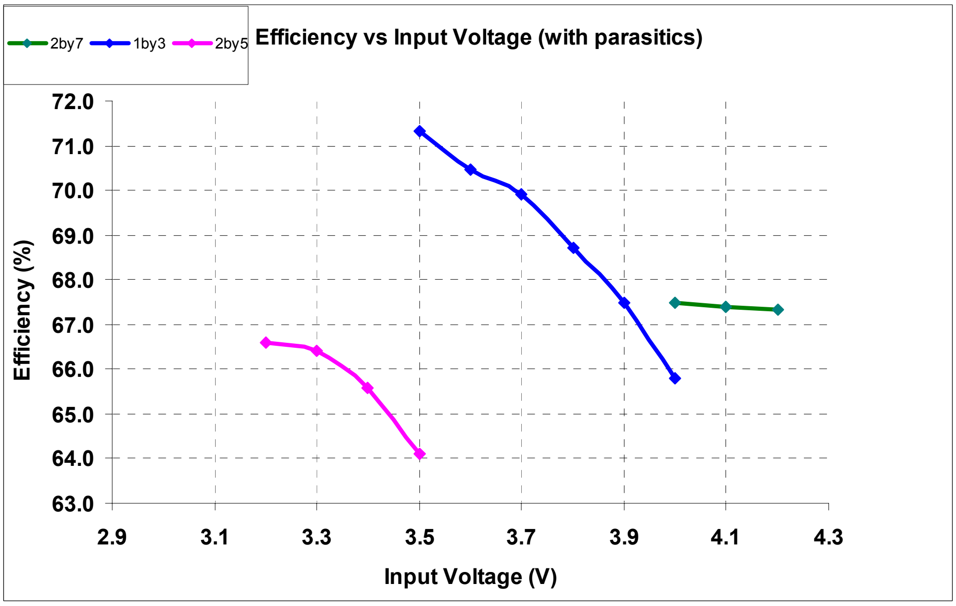

Figure 3-28. Efficiency versus Input Voltage for final circuit

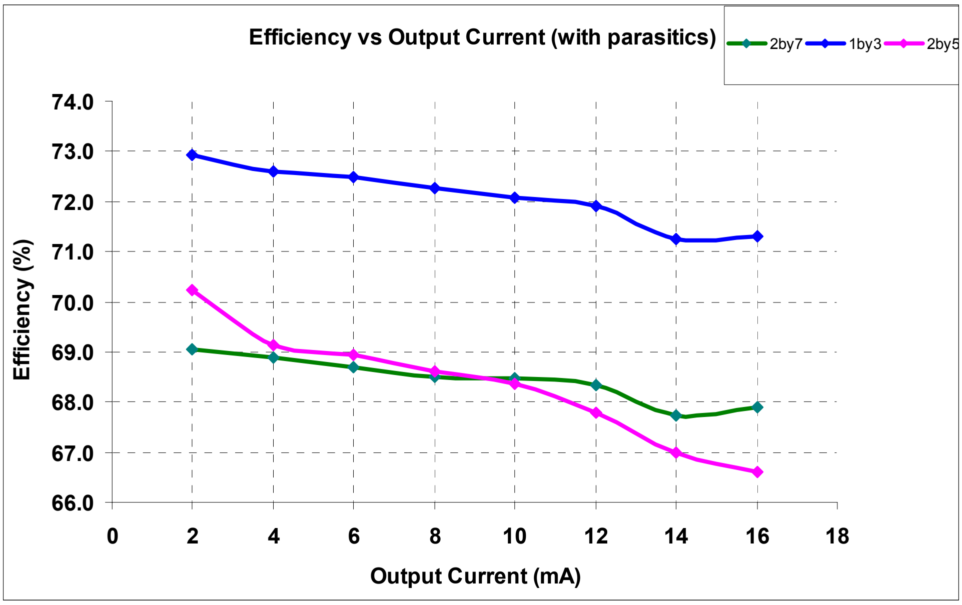

Figure 3-29. efficiency versus Load current for final design

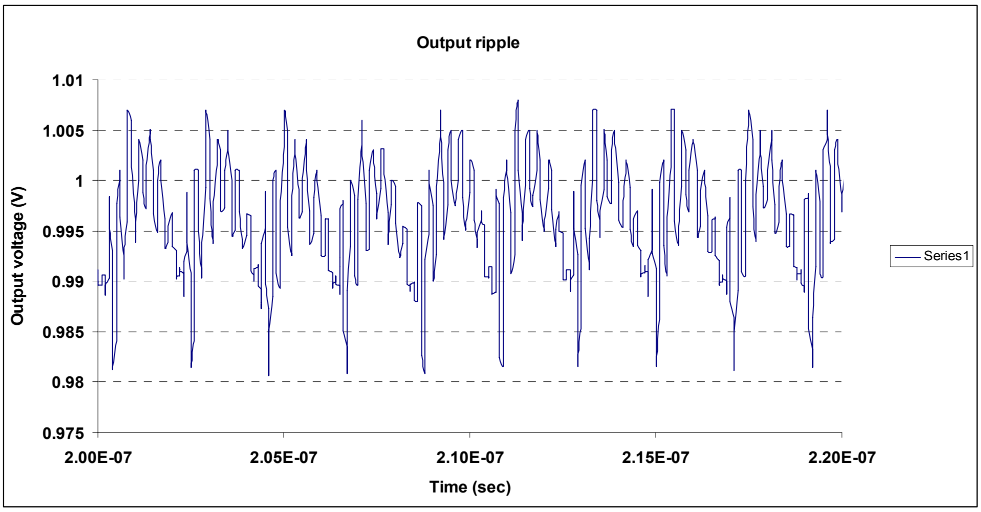

Figure 3-30. Output ripple characteristics of final design

4 MEASUREMENT SETUP

DC-DC converters are part of a bigger system and mounted on certain Printed Circuit Board (PCB). Metal traces on PCB possess parasitic capacitances, resistance and inductance. These effects must be added in the design process so that the manufactured chip performs quite closely to simulated results.

A measurement setup was proposed for the designed DC-DC converter including all critical PCB and instrument parasitics. Setup also provides detailed guide to measure circuit performance in real scenarios. Figure 4-5 shows the overall measurement setup with inclusion of critical parasitics.

Bias voltages for the IC are supplied externally from LM3851MR-ADJ adjustable voltage regulator. Output voltage of LM3851MR-ADJ can be adjusted by changing the variable resistor connected between OUT and ADJ PIN. Bypass capacitor of 3.3nF is added to all bias voltages outputs near the IC pins.

Detailed calculations for different components in measurement setup are presented below:

4.1 Load Resistor Calculations

Five resistors, 180, 270, 330, 390 and 470 Ω have been added in parallel at the output of SC converter as load, as shown in Figure 4-1. The idea is to select different load settings by different combinations of these load resistors. For the specified output voltage of 0.95V, following load combinations can be taken from these resistors:

Table 9 Load resistor combinations

Resistor Combination	Overall Resistance (Ω)	Equivalent Current (mA) @ V_L= 0.95V
180||270||330||390||470	58.9	16.13
180||270||330||390	67.3	14.11
180||270||330	81	11.67
180||270	108	8.7
180	180	5.2
220	220	4.3
330	330	2.9
390	390	2.4
470	470	2

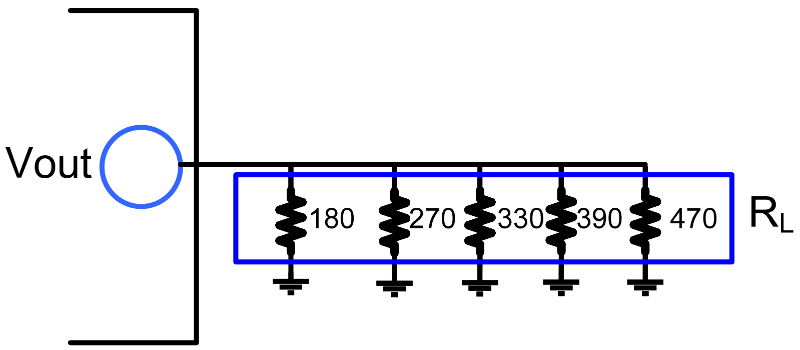

Figure 4-1. R_L resistor combination

4.2 LM38511 Resistor Calculations

LM3851 IC is used to generate five different supply voltages to bias the SC converter: 1.25V, 1.8V, 2.4V, 2.5V and 2.95V. Separate LM3851 ICs have been used to provide even the same voltages. This is done to ensure noise free and stable bias voltages. In addition, LM38511 provides current to Iref pin as current source. Resistor and capacitor values for LM38511 IC have been calculated based on IC datasheet. Calculations can be found below. Figure 4-2 can be used as reference.

$$V_{OUT} = V_{ADJ}.\ (1 + (R_1/R_2)) \text{ Where } V_{ADJ} = 0.5V$$

R_1 and R_2 should be selected such that $(R_1R_2)/(R_1+R_2) \leq 1k\Omega$

$$C_{FF} = 1/(2\pi R_1 F_z) \text{ Where } F_Z \text{ lies between 20-40KHz}$$

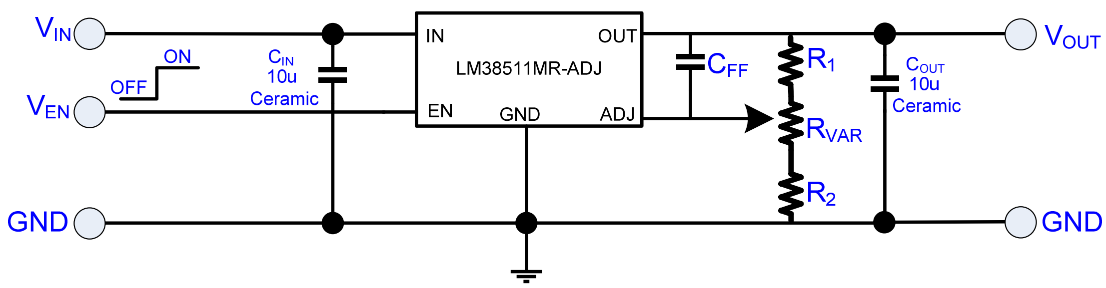

Figure 4-2. LP38511-ADJ circuit diagram [37]

Based on above formulae following values were selected for 1.25V output.

R_1= 1.5K R_2= 1K'

C_{FF} = 3300pF

A variable resistor of 1K was used in between R_1 and R_2 to provide tuning option for output voltage. For minimum and maximum values of R_{var}, following minimum and maximum values of Vout and Fz can be taken.

$Vout_{min}$=0.875V $Vout_{max}$= 1.75V
Fz_{min} = 19.29K Fz_{max} = 32.15K

Similarly for 1.8V, 2.4, 2.5 and 2.95, following component values are used.

1.8V Output

R_1= 2.7kΩ	R_2= 1.2 kΩ	C_{FF} = 1500pF
R_{VAR}= 1 kΩ	$Vout_{min}$=1.11V	$Vout_{max}$= 2.041V
Fz_{min} = 28.67kHz	Fz_{max} = 39.29 kHz	

2.4V Output

R_1= 1 kΩ	R_2= 270 Ω	C_{FF} = 4700pF
R_{VAR}= 1K	$Vout_{min}$=0.89V	$Vout_{max}$= 4.2V
Fz_{min} = 16.93K	Fz_{max} =33.86K	

2.5V Output

R_1= 1 kΩ	R_2= 270Ω	C_{FF} = 4700pF
R_{VAR}= 1K	$Vout_{min}$=0.89V	$Vout_{max}$= 4.2V
Fz_{min} = 16.93K	Fz_{max} =33.86K	

Iref Output

See Figure 4-3 for reference

$$I_{max}=\frac{V_{ADJ}}{R_{min}}=\frac{0.5}{100}=5mA$$

$$I_{min}=\frac{V_{ADJ}}{R_{min}}=\frac{0.5}{50.1K}=10\mu A$$

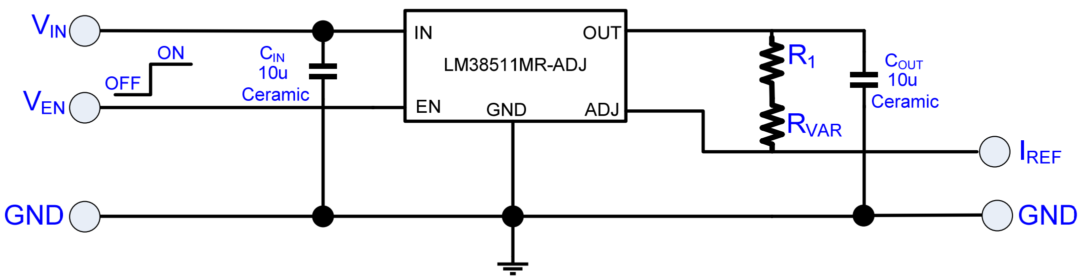

Figure 4-3. LM38511MR-ADJ as reference current source

4.3 PIN Description

Table 10 PIN description of SC converter

PIN	Description
Vin	Supply input voltage pin
Vout	Output voltage pin
Vss	Ground
VbiasSW1b	Internal bias voltage for SW1
VbiasSW2b	Internal bias voltage for SW2
VbiasSW3b	Internal bias voltage for SW3
VbiasSW4b	Internal bias voltage for SW4
twoVdr	Internal bias voltage
Vbias18	Internal bias voltage of 1.8V
Vdr	Internal bias voltage
VddmVdr	Internal bias voltage
Vdd_osc	Clock generator supply voltage pin
EN	Clock generator enable/disable pin. Pull High to enable clock signal
Iref	Reference current pin for clock generator frequency tuning
Clock_out	Output clock from clock generator

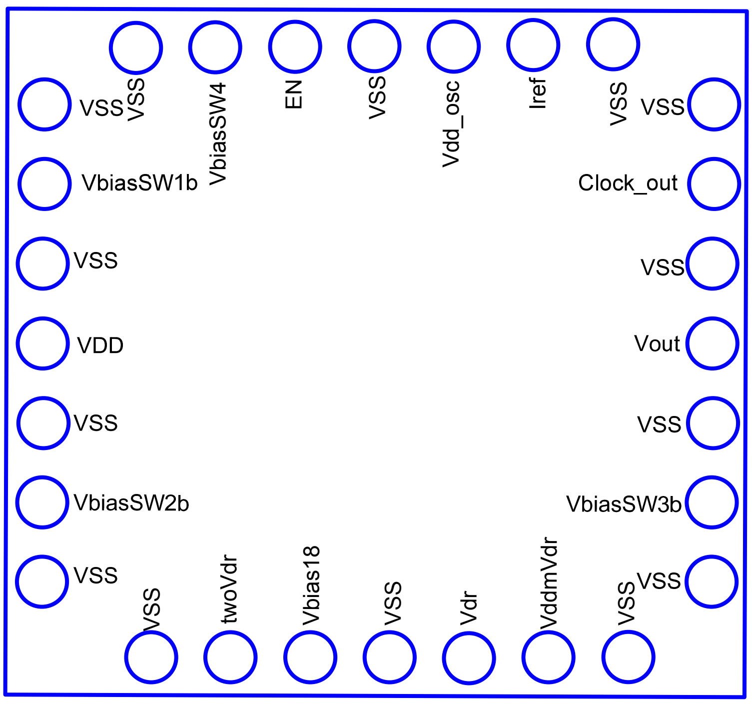

Figure 4-4. SC converter pin diagram

4.4 Electrical Characteristics

Table 11 Electrical characteristics of SC converter

Symbol	Parameter	Min	Typ	Max	Units
Vin	Input Voltage	3.2	4.2	4.2	V
VbiasSW1b	Switch1 drive voltage	Vin-1.8	Vin-Vdr	Vin-0.8	V
VbiasSW2b	Switch2 drive voltage a)2/7 topology b)1/3 topology c)2/5 topology	a) 2.4	a) 2.4 b) 2.2 c)2.4	a) 3.4	V
VbiasSW3b	Switch3 drive voltage	1.2	1.25	1.8	V
VbiasSW4b	Switch4 drive voltage a)2/7 topology b)1/3 topology c)2/5 topology	a) 1.2	a) 1.8 b) 1.25 c) 1.25	a)2.2	V
Vout	Output Voltage	0.9	0.95	1	V
Iout	Output current		16	16	mA
twoVdr	Internal bias voltage	1.8	2.5	2.75	V
Vbias18	Internal bias voltage	0.8	1.8	1.8	V
Vdr	Internal bias voltage (optimum drive voltage)	0.8	1.25	1.8	V
VddmVdr	Internal bias voltage	2.4	2.95	3.4	V
Vdd_osc	Clock generator supply voltage pin	1.6	1.8	1.8	V
ENon	Clock generator enable ON threshold voltage	0.8	1.25	1.8	V
ENoff	Clock generator enable OFF threshold voltage	0	0	0.4	V
Iref	Reference current pin for clock generator freq tuning	40	100	1000	uA
Clock_out	Output clock from clock generator	35	60	78	MHz

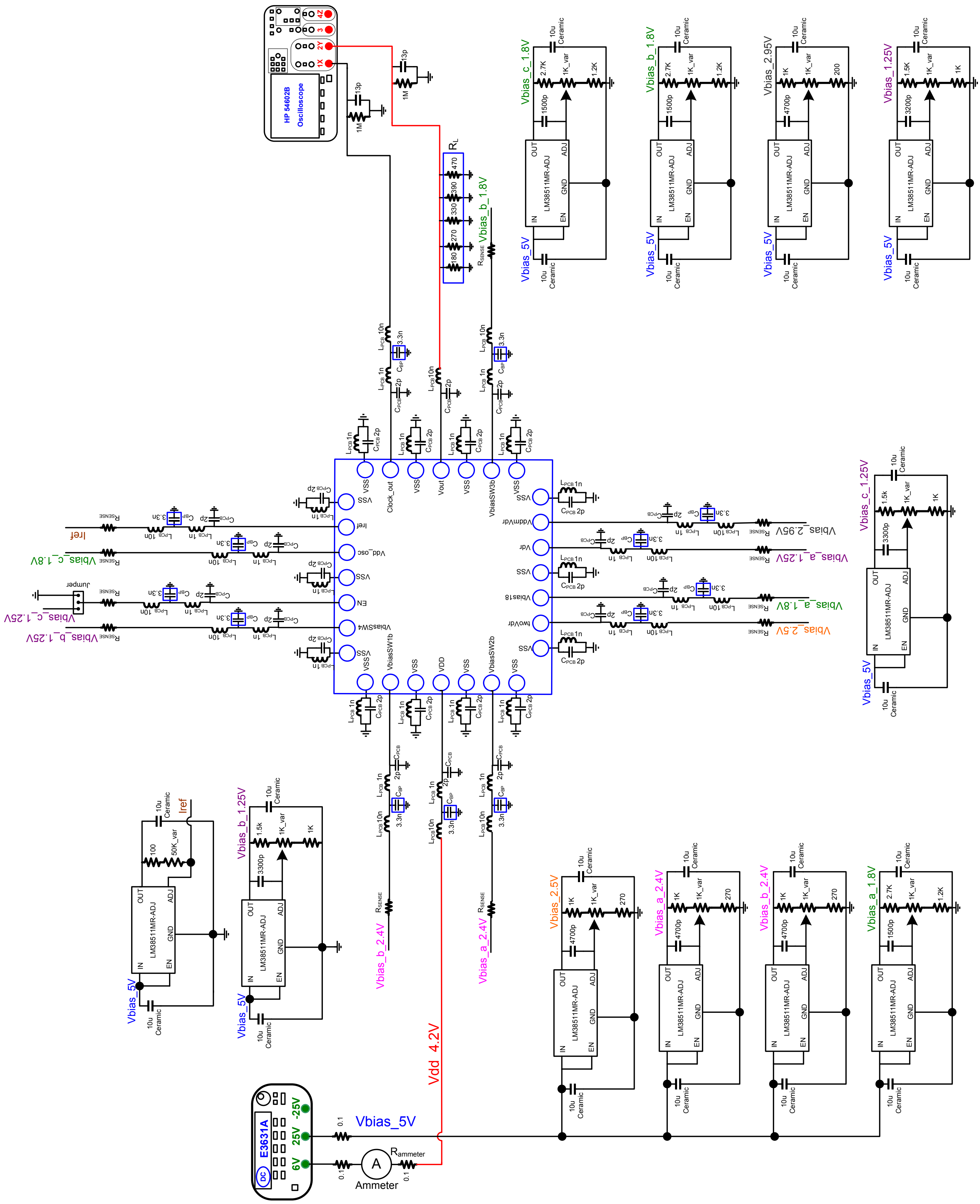

Figure 4-5. SC DC-DC converter measurement setup

5 LAYOUT DESIGN

Cadence generic design process was used to implement SC converter layout. While designing the floor-plan of layout, following points were taken into consideration.

- Make layout structure as symmetrical as possible.
- Make routing distance between Vin and Vout as small as possible.
- Make Vin, Vout and Ground paths as wide as possible to ensure lesser series resistance.
- Make Vout path with additional metal layers and add additional vias for connection between the layers. This will decrease the trace resistance and provide high parasitic capacitance to ground for output ripple suppression.
- Put bypass capacitors as big as possible at all DC supply pads.
- Make all Ground referenced capacitors from MOS structure with high capacitance density and smaller size.
- Add ESD protection circuitry to all IC pads.
- Make same distance of clock generator to all buffer drivers. This is done to ensure same clock delay through all clock routing lines.
- Use MOS transistors having 1.8V gate-oxide breakdown voltage.

Based on above points, an initial layout proposal was made, which helped in finalizing the final layout later. Figure 5-1 shows the proposed layout structure.

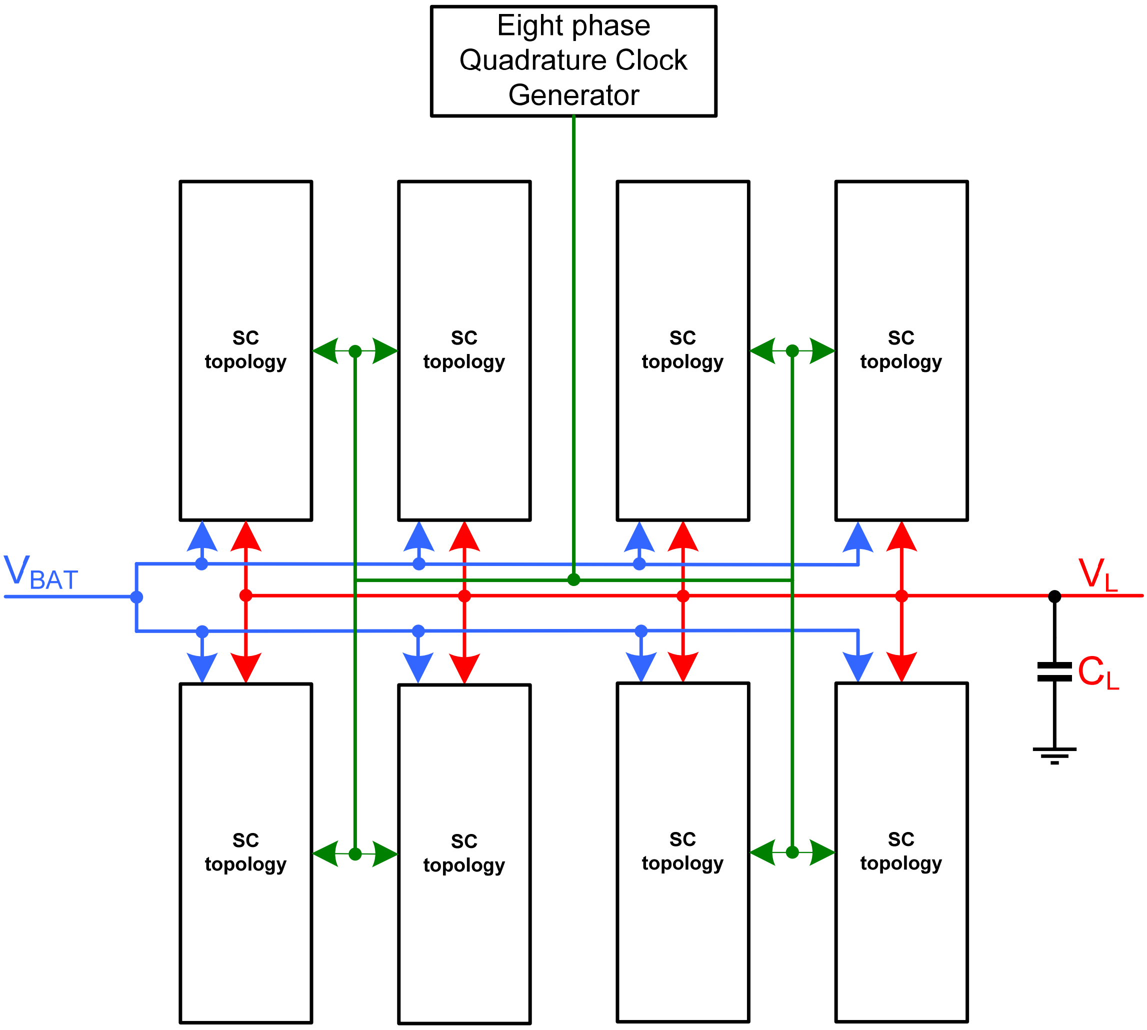

Figure 5-1. Initial Layout Proposal

First, the layout for single phase SC-converter was made, which was then copied to make an overall eight phase SC configuration. Figure 5-2 to Figure 5-5 show the designed layouts.

Figure 5-2 and Figure 5-3 show the final layouts of buffers. While making the layout the distance between Vin and Vout was made as small as possible. Moreover, metal layers were stacked on each other, in order to decrease the resistance of paths.

As the buffer circuit does not pass high current through it, metal widths of 0.5um have been used for main current paths. Direction of main current path is indicated by white arrows.

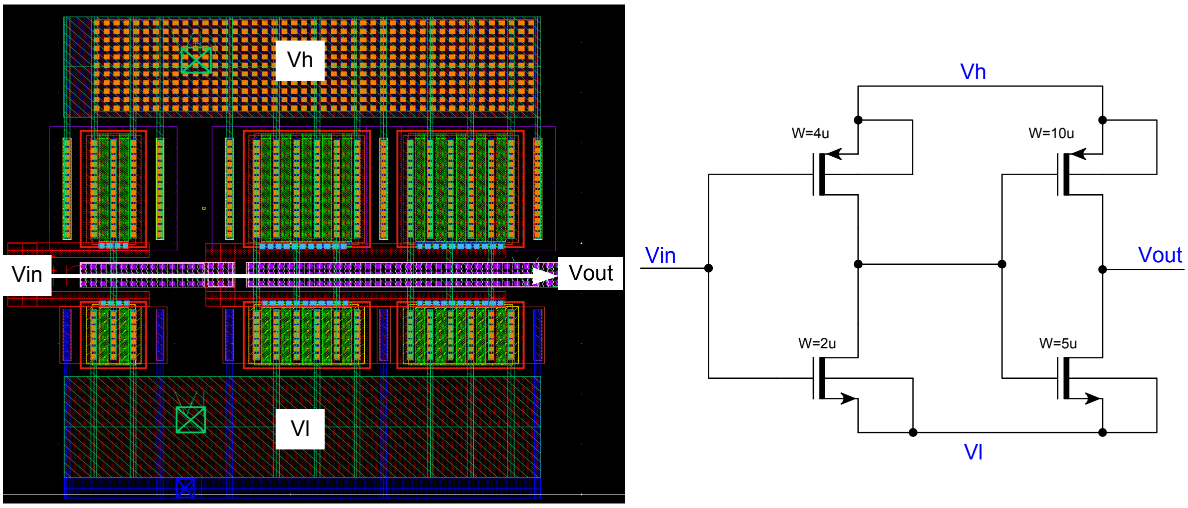

Figure 5-2. Buffer Layout

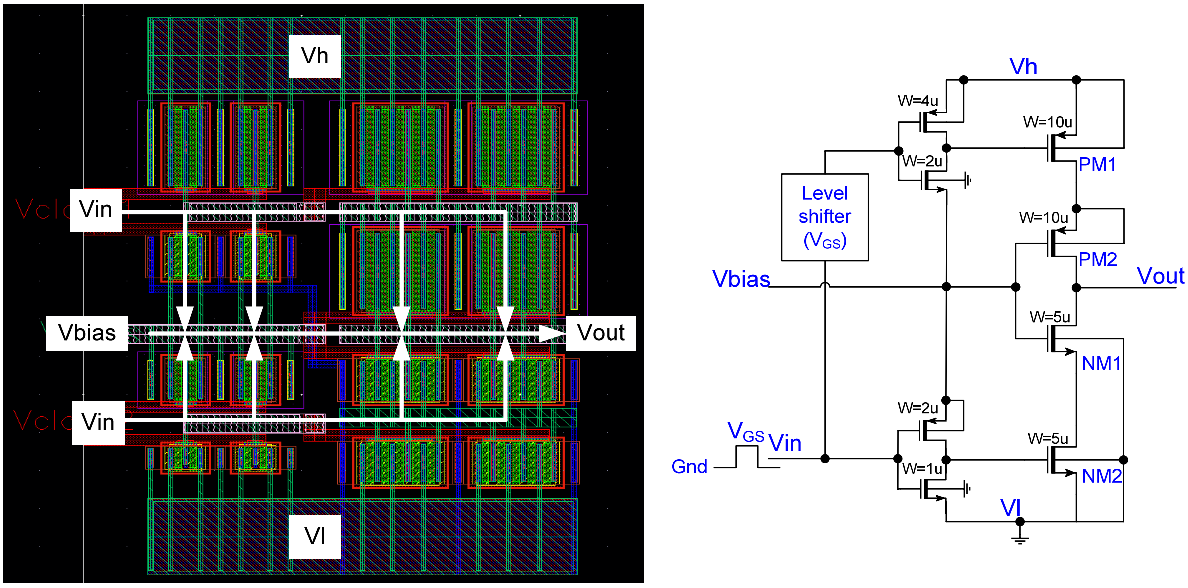

Figure 5-3. Cascoded buffer layout

Figure 5-4 shows the completed layout of one phase of SC topology. Similar to buffer layout design, layout components were organized in order to minimize the length of main current path. Ground path was routed to the left side of MOM capacitors while Vout path is towards the right side. Clock signals are distributed such that the overall clock delay remains same for all clocks. It can be seen that the biggest contributor in layout size are MOM capacitors. A single MOM capacitor covers an area of 89x89 um^2. This large size of MOM capacitor was one of the biggest problems because of which design specifications were changed from 100mA to 16mA. For 100mA output current, MOM capacitor size would have been really huge and thus impractical.

Stacked metal 3 and metal 4 layers have been used for output signal routing, each having width of 3um. Path resistance was calculated by following simple calculations:

Metal 3 and Metal 4 sheet resistance 0.17Ω

Approximate metal 3 & 4 path length 600um

$$\text{Path Resistance} = \frac{(\text{Total Lenght})}{(\text{Layer Width})} \cdot (\text{SheetResistance}) \tag{5.1}$$

$$\text{Path Resistance} = \frac{600\text{um}}{3\text{um}} \cdot 0.17\Omega = 34\Omega \tag{5.2}$$

As metal layer 3 and 4 are stacked together so the overall resistance is parallel combination of their resistances. Therefore, overall path resistance becomes 17Ω. Path resistances of other critical paths was also evaluated and later put into final simulations for more practical results.

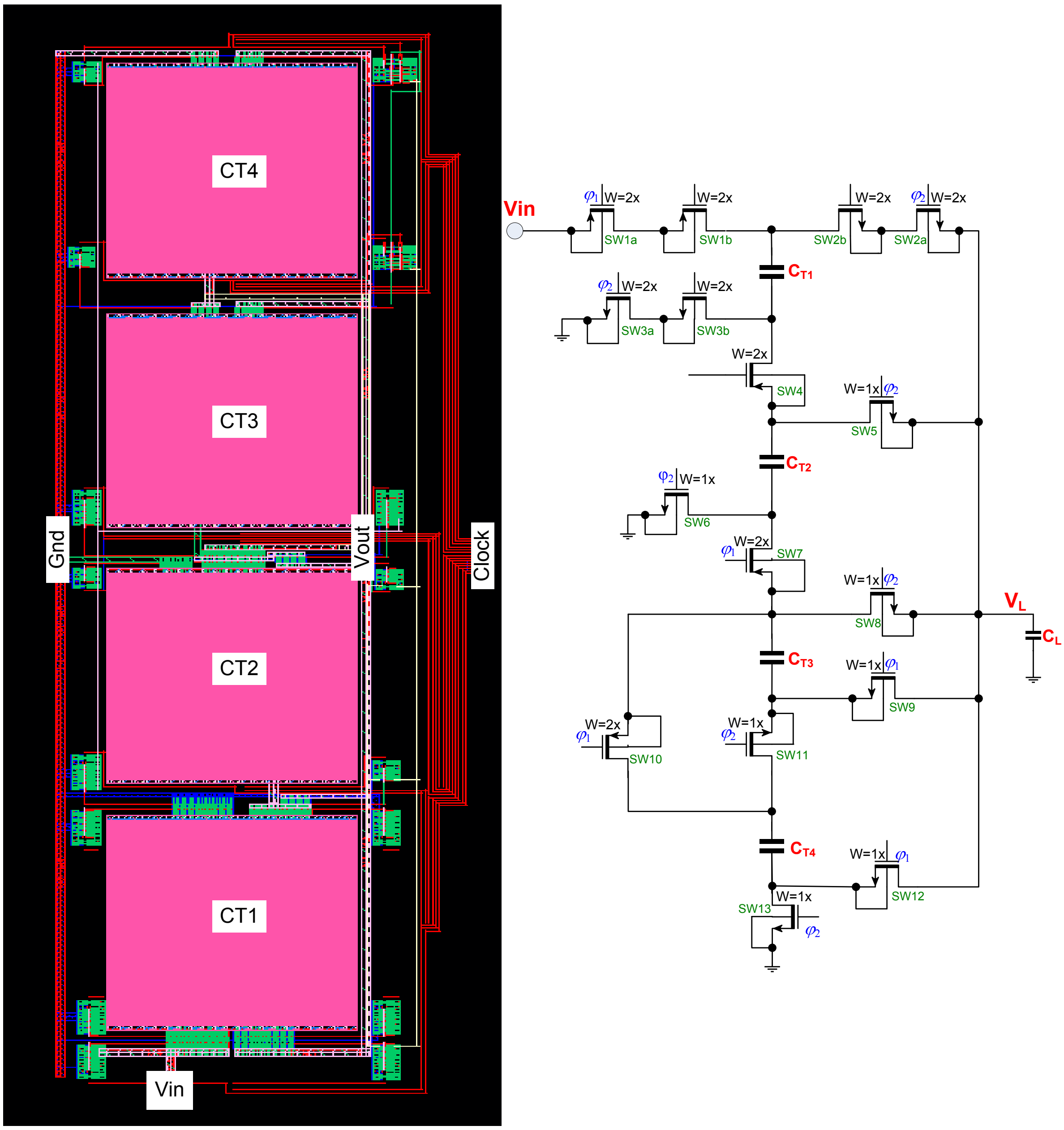

Figure 5-4. Layout of one phase of SC converter

Figure 5-5 shows the overall layout of designed SC topology. Layout occupies an active area of $1.3x1mm^2$ approximately. An overall charge transfer capacitance of 1120pF (MOM) was used while the load capacitor value is 190pF (MOS). All IC pads were connected with bypass capacitors of 30-90pF. This was done to ensure a low noise at the dc-bias input pins. Moreover, due to gate oxide device breakdown conditions at some input pads, some bypass capacitors have been implemented with MIM capacitors rather than MOS.

Main current path between Vin and Vout has been shown with a white arrow. The calculated sheet resistance from equation (5.1) for Vin and Vout paths was 0.34 Ω. This smaller value of sheet resistance was obtained by stacking metal layers 8-11 f or Vin and Vout Paths.

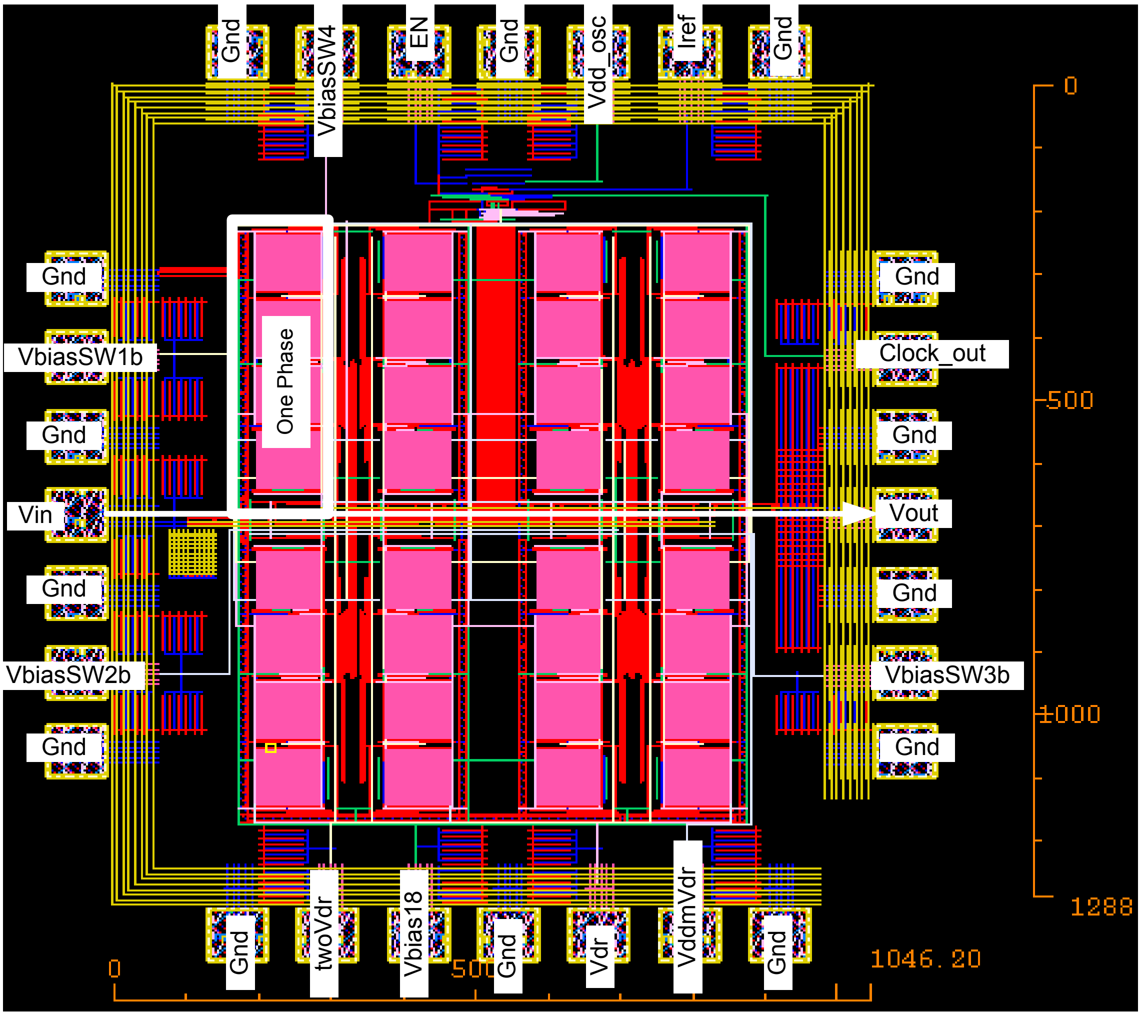

Figure 5-5. Overall Layout

6 CONCLUSION AND FUTURE WORK

A novel CMOS SC DC-DC converter utilizing MOM capacitors has been designed using Cadence generic 45nm design kit. Its design procedure, simulation results and preliminary measurement setup have been discussed above. Performance of the design meets most of the goals of this thesis.

The comparison of the main performance parameters with other published SC DC-DC converters is shown in Table 12. At the moment, this work is compared based on the simulated performance.

It is somewhat difficult to make one-to-one comparison with the other recently published SC converters, because many of them are fabricated in different CMOS technologies and different input voltages. Comparing with those designs would make the comparison not completely fair since design parameters are not matching 100%. On the contrary, comparison is still helpful to evaluate circuit performance, in relation with recent designs, specifically in certain domains.

Table 12 SC converter performance comparison

Reference	Input Supply Voltage (V)	Maximum Efficiency (%)	Output Ripple Voltage (mV)	Output capacitance (pF)	Charge Transfer Capacitance (pF)	Operating Frequency (MHz)	Output Voltage (V)	Max Output Current (mA)	Process
[7]	1.8	69		700	534	30	0.8-1	8	45nm
[8]	2	90				100	0.95	2.8	45nm SOI
[11]	2	79.76	-	-	-	80-220	0.5-1.2	200	32nm
This design	3.2-4.2	71.4	24	190	1120	60	0.9-1	16	45nm Candence generic

The comparison above indicates that the designed circuit possesses lower efficiency as compared to other recent designs. The lower efficiency is due to the presence of additional flying capacitors and cascoded structures in SC topology. Flying capacitors possess higher bottom plate capacitance which causes reduction in efficiency. Addition of additional flying capacitors and cascoded transistors is inevitable for circuit operation, as the input voltage is too high for 45nm process breakdown limits. It is still possible to achieve higher efficiency if the process allows creation of high density and low bottom plate parasitic capacitors.

Flexibility of the circuit to operate at higher input voltage makes it possible to directly use the converter with Li-ion batteries, without the use of external linear voltage regulators, thereby reducing space.

At the moment, circuit operates in open loop without a proper feedback to adjust its output voltage. With proper design of feedback structure, circuit will be able to operate well within desired specifications.

REFERENCES

[1] Y. K. Ramadass, “Energy processing circuits for low-power applications”, P.h.D. dissertation, Massachusetts Inst. of Technology, Cambridge, MA, Jun.2009.

[2] A. Pressman, K. Billing, T. Morey, *Switching power supply design*, 3rd ed. New York, McGraw Hill publications, April 2009.

[3] M. Wens, M. Steyaert, "An 800mW fully-integrated 130nm CMOS DC-DC step-down multi-phase converter, with on-chip spiral inductors and capacitors," *IEEE Energy Conversion Congr and Expo*., 2009, pp 3706-3709.

[4] S.S. Kudva, R. Harjani, "Fully integrated on-chip DC-DC converter with a 450x output range," *IEEE conf, Custom Integrated Circuits (CICC)*, 2010, pp1-4.

[5] Wikipedia.com. (2011, February 25). *DC-DC converters* [Online]. Available at: http://en.wikipedia.org/wiki/DC-to-DC_converter

[6] Technologyinterface.nmsu.edu (2011, February 25) *Applications of switched capacitor circuits in active filters and instrumentation amplifiers* [Online]. Available at: http://technologyinterface.nmsu.edu/3_3/3_3g.html

[7] Y. Ramadass, A. Fayed, B. Haroun, A. Chandrakasan, “A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter with Digital Capacitance Modulation in 45 nm CMOS,” *In IEEE J. Solid-State Circuits.*, vol.45, no.12, pp.2557-2565, Dec. 2010

[8] L. Chang, R. K. Montoye, B. L. Ji*, A. J. Weger, K. G. Stawiasz, and R. H. Dennard,"A Fully-Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3A/mm2", *IEEE Symp on VLSI Circuits/Technical Digest of Technical Papers, pp55-56, 2010.*

[9] R. Yogesh K, C. Anantha P, "Voltage Scalable switched dc-dc conveter for ultra low power on chip applications", *IEEE conf, Power Electron Specialist*, pp 2353-2359, 2009.

[10] I. Chowdhury, M. Dongsheng, "Design of Reconfigurable and Robust Integrated SC Power Converter for Self-Powered Energy-Efficient Devices", *IEEE trans. Ind. Electron*, pp 4018-4028, Sep 2009.

[11] Le. Hanh-Phuc, S. Micheal,S. Seth R, S. Visvesh, "Design techniques for fully integrated SC DC-DC converters", *IEEE J.* Solid-State Circuits, vol.46, no.9, pp.2120-2131, Dec. 2010

[12] P.G. Blanken, R. Karadi, H.J. Bergveld, "A 50MHz bandwidth multi-mode PA supply modulator for GSM, EDGE and UMTS application", *IEEE Symp. Radio frequency integrated circuits,* pp 401-404, 2008.

[13] D. Kang, D. Kim, J. Choi, J Kim,Y. Cho, B. Kim, "A Multimode/Multiband Power Amplifier With a Boosted Supply Modulator", *IEEE trans, Microw. Theory Tech.,* pp 2598-2608, 2010.

[14] R. Shrestha, R. van der Zee,A. de Graauw, B. Nauta, "A Wideband Supply Modulator for 20 MHz RF Bandwidth Polar PAs in 65 nm CMOS," *In IEEE J. Solid-State Circuits.*, vol.44, no.4, pp.1272-1280, Dec. 2010

[15] B. Arntzen, D. Maksimovic, "Switched Capacitor DC/DC converters with Resonant Gate Drive", *In IEEE trans, Power Electron.,* pp. 892-902, 1998.

[16] K. D. T. Ngo, R. Webster, "Steady state analysis and design of switched capacitor DC-DC converters," *IEEE conf, Power Electronics Specialist Conference*, pp. 378-385, 1992.

[17] Arntzen. B, Maksimovic. D, "Switched Capacitor DC/DC converters with Resonant Gate Drive," *In IEEE trans, Power Electron.,* pp. 892-902, 1998.

[18] Ma. Mengzhe,"Design of high efficiency step-down switched-capacitor DC-DC converter", M.S. Thesis, Oregon Sate University, 21 May 2003.

[19] Ramadass. Y, Fayed. A, Haroun. B, Chandrakasan. A, "A 0.16mm^2 Completely On-Chip Switched-Capacitor DC-DC Converter Using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS", In *IEEE conf, Solid-State Circuits,* pp.208-209, 2010.

[20] C. Yie-Tone, L. Kun-Jing, "The switched capacitor step-down DC-DC converter with improved voltage rating stability and load range," *IEEE conf, Industrial electronics,* pp. 1389-1393, 2010.

[21] K. D. T. Ngo, R. Webster, "Steady state analysis and design of switched capacitor DC-DC converters," *IEEE Power Electronics Specialist Conference*, 1pp. 378-385, 1992.

[22] Su. Feng, Ki. Wing-Hung, “Component-efficient multiphase switched-capacitor DC-DC converter with configurable conversion ratios for LCD driver applications,”*IEEE trans, Circuits. and Sys*, vol 55, no 8, pp. 753-757, August 2008.

[23] H. Chung, A. Ioinovoci, “Switched capacitor based DC-DC converter with improved input current waveform,” *In IEEE Int. Symp., Circuits and Sys.,* Atlanta, USA, pp.541-544, 1996.

[24] Andrabadu K P Viraj and G A J Amaratunga, “Analysis of switched capacitor dc-dc step down converter,” *IEEE Int. Symp., Circuits and Sys.*, vol 5, pp. 836-839,May 2004.

[25] H. Jifeng, J. Annette Von, T. Gabor C, ”Design and IC implementation of ultra-low ripple switched capacitor based buck dc-dc converter,” *IEEE conf, Appl. Power Electron.*, vol 3, pp. 1447-1452, 2005.

[26] Mingliang Liu, *Demystifying switched capacitor circuits*, Burlington MA, Newnes Elsevier Inc, 2006.

[27] Ma. Mengzhe,”Design of high efficiency step-down switched-capacitor DC-DC converter,” M.S. Thesis, Oregon State university, 21 May 2003.

[28] M. D. Seeman, “Analytical and practical analysis of switched capacitor DC-DC convertes,” M.S. thesis, University of California, 2008.

[29] F. Pierre, D. Philippe, D. Michel, “A high efficiency CMOS voltage doubler,” *IEEE J. Solid State Circ.*, vol 33, no 3, pp. 410-416. March 1998.

[30] B. Peter.(2011, June 06). *Actual and future battery technology trends* [Online]. Available at: http://www.electricmotion.cz/download/prezentace_Birke.pdf.

[31] S. Jinglin, K. Kai, X. Yong, Z. Brinkhoff et al.,“Millimeter-Waver Passives in 45nm Digital CMOS,” *IEEE Electronic device letter*, vol 31, no 10, October 2010.

[32] G. Schrom, P. Hazucha, “Feasibility of Monolothic and 3D stacked DC-DC converters for microprocessors in 90nm technology generation”, *IEEE Symp. Low Power Electronics and Design*, pp. 263-268, 2004.

[33] B. Razavi, “*Design of Analog CMOS integrated circuits,*” McGraw Hills publications, 2001.

[34] Hanh-Phuc, Seth R, Sanders, Elad Alon, “Design technique for fully integrated switched capacitor dc-dc converters”, *IEEE J. Solid State circuits*, vol 46, no 9, pp. 2120-2131, 2011.

[35] PCD File, Cadence Generic Design Kit, version 6.1.3

[36] DRC manual, Cadence Generic Design Kit, version 6.1.3

[37] National Semiconductors, “LM38511MR-ADJ datasheet”