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Reverse-offset printed flexible chips assembled on thermoplastic polyurethane: studies on mechanical tolerance

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Abstract—Reverse-offset printing (ROP) is a high-resolution printing method that can deliver µm-level linewidths. ROP could be used to fabricate flexible high-performance devices and integrated circuits (ICs) to replace, in the future, some of the conventional Si ICs e.g. in wearable electronics applications, potentially improving their form-factor and sustainability. Here, we fabricated test chips with Cu conductors on thin, flexible polyimide substrate using two ROP-based processes: i) ROP of Cu nanoparticles, and ii) ROP of polymer resist and lift-off of vacuum deposited Cu. Both types of samples were attached onto screen-printed Ag conductors on stretchable thermoplastic polyurethane (TPU) substrates using conductive adhesives and mechanically supported either by edge adhesive or glop-top encapsulation. The electromechanical behavior of the assembled test chips was examined by performing compression and expansion bending tests for five test chip samples of each fabrication variation, showing good mechanical tolerance of the ROP-based Cu and the interconnections. Although the expansion bending tests reveal weaknesses in the Ag structure on the TPU, the compression bending tests indicate encouraging robustness. The conductor at the edge of the more rigid adhesive is found to be the weakest point and preliminary tests using a more flexible underfill support material suggest potential mitigation pathways.

Keywords—high-resolution printing; reverse offset printing; flexible chip; component assembly; reliability

I. Introduction

Printing methods are utilized for the sustainable fabrication of flexible and wearable electronics, energy harvesting and storage devices, and point-of-care diagnostics. Conventional printing methods, such as screen, flexography and inkjet, are well-suited for large-area or large-volume manufacturing via roll-to-roll (R2R) process. However, these lack the accuracy needed for the fabrication of electronic circuits with reasonable device size and lead to considerable material volume on the final substrate. Flexible hybrid electronics (FHE) is a fabrication paradigm for e.g. wearable electronic systems that combines the high-performance of conventional Si integrated circuits (ICs) and scalability of printing, where Si chips are assembled onto printed circuit boards manufactured using conventional printing methods [1]. Reverse-offset printing (ROP) is a high-resolution printing method that has many beneficial features over conventional printing methods: i) single µm-level printing resolution allowing both miniaturization and low material volume, ii) potential for high overlay accuracy at few µm-level, iii) equivalence of nominal and printed feature size, iii) low line edge roughness, iv) uniform layer thickness, and v) sharp, nearly vertical sidewalls of the printed structures. The last feature allows the use of ROP in resist printing in lift-off (LO) or etching process, thus allowing combinations of printing and vacuum deposition methods (e.g. evaporation and atomic layer deposition). The unique features of ROP arise from the patterning of inks in a semi-dry state on top of polydimethylsiloxane (PDMS) blanket using a high-resolution relief plate. ROP can be used in R2R process for large-area single layer applications (e.g. touch panels, electrodes, and antennas) or in roll-to-sheet process for multilayer devices (e.g. thin-film transistors, sensors, and circuits) [2]. ROP could be further developed to fabricate flexible ICs or sensors to replace some of the Si ICs e.g. in wearable electronics. To demonstrate the feasibility of the approach, similarly to the assembly processes utilized in FHE, a robust assembly process of ROP-based flexible circuits on stretchable carrier substrates (flex-on-stretch) would need to be developed.

In this paper, we fabricated flexible test chips on 38 µm thick polyimide (PI) substrate using ROP and study their assembly using isotropic conductive adhesive (ICA) to screen-printed Ag electrodes on stretchable thermoplastic polyurethane (TPU), a typical substrate in wearable electronics. The conductive structures on the PI have been fabricated with two methods: i) ROP of Cu nanoparticle (NP) ink and intense pulsed light (IPL) sintering (~120 nm thick) and ii) ROP of polymer resist and lift-off (LO) of vacuum evaporated Cu (~40 nm thick). We study the electromechanical behavior of the assembled test chips considering the bending-induced stress when i) glued at edges or ii) glob-top encapsulated. The results indicate good mechanical tolerance of the ROP chip wiring and TPU to ROP chip interconnection. However, the tests reveal that the durability of the Ag electrode at the meeting point of the non-elastic support adhesive and the stretchable TPU needs optimization. Preliminary stretching tests suggest that stress at the critical location can be lowered by using a flexible underfill material as the support.

II. EXPERIMENTAL

A. *Sample fabrication*

A sheet fed ROP system (Jemflex/Nihon Denshi Seiki) was used to fabricate the Cu NP and Cu LO flexible test chip samples on 38 µm thick PI substrate (Xenomax, Nagase). The Cu NP ink (CUNI-AC-01, Ishihara Chemical) was IPL sintered using a broad band spectrum xenon lamp system (Xenon Sinteron S-2100, Xenon Corp.). The poly-4-vinylphenol (PVPh) based polymer resist ink for the Cu LO patterned samples was prepared by dissolving PVPh into ethyl lactate and ethyl acetate solvents at 3.5 wt-% solids loading [3]. 40 nm of Cu was deposited via e-beam evaporation (MinilabET080A, Moorfield Nano-technology) on the negative ROP-patterned polymer resist layer followed by removal of the underlying resist layer in a lift-off process using ethanol/DIW in a megasonic bath (Sonosys), resulting in the positive Cu pattern remaining on the substrate. Fig. 1 shows the achieved patterning quality of nominal 4 µm line-space patterns for both processes. The complete sample fabrication process is detailed in [4].

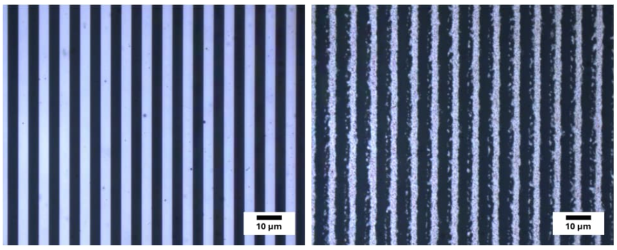

Fig. 1. High resolution ROP patterned Cu. Left: Cu LO, Right: Cu NP 4 µm line-space pattern.

The 10 cm x 10 cm printed samples were diced into 5 mm x 5 mm chips and placed onto a component carrier tape for flexible component assembly using a pick and place machine (Fuji NXT3). Each printed sample contained 400 pieces of 5 mm x 5 mm sized chips, demonstrating the good scalability of the roll-to-sheet ROP process. Isotropic conductive silver adhesive (ICA) (EPO-TEK H20E-PFC) was dispensed onto a screen-printed Ag electrode pattern (LS411-AW, Asahi) on a stretchable 100 µm thick TPU substrate (Platilon U073, Covestro) attached to a 75 µm thick polyethylene carrier film. The flexible IC test chip was then aligned face down to the Ag electrodes followed by drying at 120 °C for 15 minutes. To ensure the mechanical robustness of the chip to TPU interconnection, a UV-curable adhesive (Loctite AA 3525, Henkel) was dispensed (i) at the chip edge and (ii) as a glob-top encapsulation. Fig. 2 (left) shows a PI chip with ROP Cu patterning assembled on stretchable TPU substrate with edge adhesive and Fig. 2 (right) shows the ROP chip and screen-printed Ag electrode pattern with glob-top (right). Preliminary tests were also done using a flexible, low viscous adhesive (Panacol Vitralit 5140) as underfill material. Wires (~50 cm in length) were attached to the screen-printed contact pads using conductive silver paint to measure the resistance during the bending stress. The connection was secured mechanically by depositing a UV-curable adhesive (Loctite 3494) over the interconnection area (Fig. 2, right).

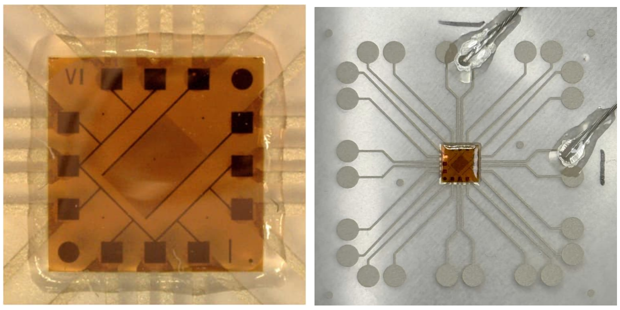

Fig. 2. Left: 5 mm x 5 mm PI chip with ROP Cu patterning assembled on stretchable TPU substrate and adhesive dispensed at edge for mechanical robustness. Right: Cu NP glob-top test sample with attached wires.

B. *Electromechanical testing*

The electromechanical behavior of the assembled test chips was examined with the Mark10 bending machine (setup shown in Fig. 3). Compression bending tests were performed for five samples of each fabrication variation: Cu NP glob-top and edge adhesive, Cu LO glob-top and edge adhesive.

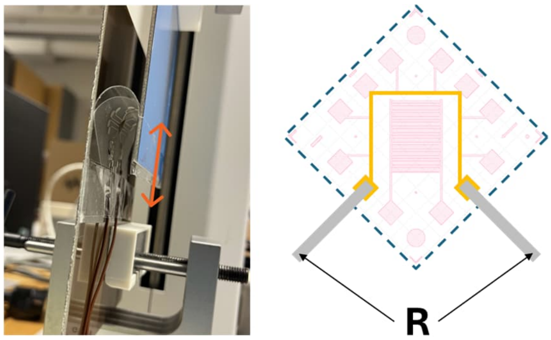

Fig. 3. Left: Test sample in bending test apparatus with arrow indicating movement of plates. Right: Schematic of the resistance measurement with yellow color indicating ROP Cu wiring on PI chip and gray color indicating screen-printed Ag electrode on TPU.

Fig. 3 shows the initial positioning of the test sample when the chip is facing the left-hand side plate. The backside of the test sample was attached to a PET film with a two-sided 3M adhesive to ensure a consistent bending radius. The left-hand side plate of the bending machine is fixed while the right-hand side plate was programmed to move down 33 mm after which it moved up back to the starting position with a speed of 500 mm / min, thereby bending the chip attached to the TPU. The distance between the plates was set to 15 mm corresponding to a bending radius of 7.5 mm. 500 bending cycles were performed for each test chip sample.

The length of the measured 50 µm wide ROP copper wiring on the PI chip was ~7.4 mm. Fig. 5 (right) shows a schematic of the 2-wire resistance measurement, with the measured conducting path highlighted in yellow (Cu) and gray (Ag). The samples were attached to the plates such that the bending

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curvature was aligned vertically with respect to the schematic. A National Instruments (NI) USB-6003 device with program written in LabVIEW was used for data acquisition. One of the channels in NI measured the supply voltage (5 V ± 3%) and one channel measured the voltage across the printed copper line. The measurement was done in real time every 500 ms. The voltage values were converted to corresponding resistance using

$$R_{Cu} = \frac{V_{AI}R_{ref}}{V_{supply}-V_{AI}}, \quad (1)$$

where V_{AI}, V_{supply} and R_{ref} are measured voltage, supply voltage and reference resistance respectively. For these measurements the reference resistor was selected to be 1.2 $k\Omega$ so that the reference resistor could handle even the increased resistance in bending. The inaccuracies caused by the selected reference resistor and the 2-wire measurement were considered to be acceptable as the main interest in the measurements was in the change of resistance rather than the absolute resistance value.

After the bending tests of the samples supported by glob-top and edge adhesive, failure analysis was performed using optical microscope and X-ray microscopy (XRM) (SKYSCAN 1273, Bruker). After the failure analysis, samples with glop-top and underfill were also subjected to stretching tests using similar Mark 10 machine to evaluate the potential of the softer underfill material in improving the mechanical robustness.

III. RESULTS

Fig. 4 shows optical microscope images of the PI chip edge of Cu NP glob-top (left) and Cu NP edge adhesive (right). In both cases, the adhesive penetrates under the chip as indicated by the blue dashed lines, providing mechanical support for the flexible chip in the interconnect region. Optical microscopy from the reverse side through the TPU confirmed the support adhesives filling the area between the interconnects at the edge.

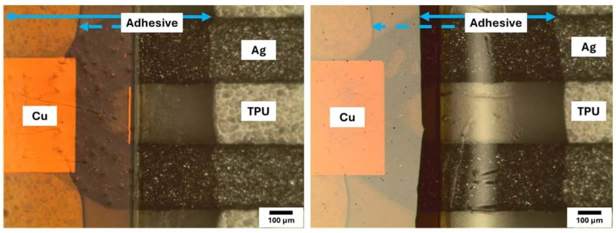

Fig. 4. Left: Cu NP glop-top, Right: Cu NP edge adhesive.

The resistance of the printed copper wire varies depending on the state of the bending. The resistance is higher when the chip and Ag conductors are under bending stress and thus, they experience more intense strain. The average normalized resistances of successful measurements without an open circuit (out of total 5) of each fabrication variation as a function of bending cycles are depicted in Fig. 5-6. The inset figures show the maximum normalized resistances for each sample from 250 to 500 cycles. The minimum normalized resistance as a function of bending cycles remained relatively stable for each test chip sample (1.16 times at the highest) suggesting that when the chip and the conductors do not experience high strain the resistance returns near to the initial value.

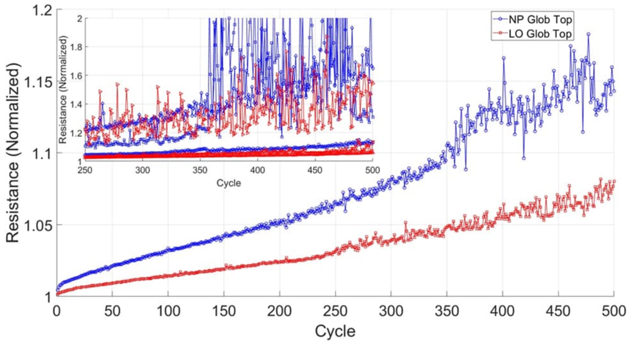

Fig. 5. Average normalized resistance values of Cu NP glob-top (blue) and Cu LO glob-top (red) as a function of bending cycles. Inset: normalized maximum resistance for all samples without an open circuit.

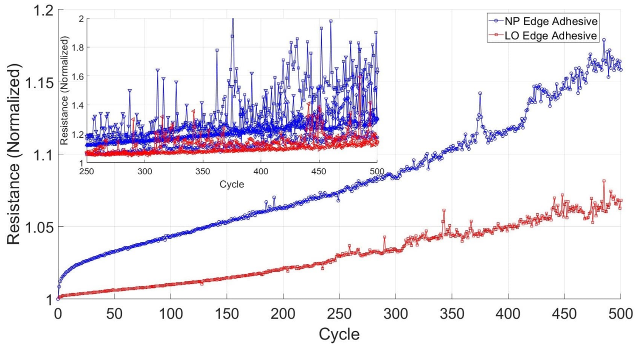

Fig. 6. Average normalized resistance values of Cu NP edge adhesive (blue) and Cu LO edge adhesive (red) as a function of bending cycles. Inset: normalized maximum resistance for all samples without an open circuit.

The resistance follows a rather stable increasing trend for all samples until approximately 350 cycles. As the insets in Fig. 5-6 indicate, the maximum resistance at > 350 cycles varies greatly between the test samples and between the fabrication variables. In general, Cu LO seems to result in a smaller increase in resistance than Cu NP. Two Cu LO glob-top samples and one Cu LO edge adhesive sample survive 500 cycles without a >20% increase in the maximum resistance whereas the corresponding numbers for Cu NP are one and zero, respectively. When comparing glob-top and edge adhesive, three glob-top samples survive 500 cycles without a >20% increase in maximum resistance, but only one edge adhesive sample does. Overall, four test chip samples out of 20 survived 500 compression bending cycles without a >20% increase in maximum resistance. Expansion bending tests, where the samples were attached to the reverse side of the PET film, were also conducted. However, an open circuit was observed for all sample parameter variations at maximum bending stress from the first bending cycle. The resistance returned near to the initial value after each bending cycle suggesting a reversible failure mechanism.

When examining the test chip samples with an optical microscope, fractures in the silver conductors on the TPU near the adhesive edge are observed as shown in Fig. 7, explaining the increase in the resistance values. The fractures are mainly in the conductors that are parallel to the bending curvature, which are likely subject to the largest stresses in the bending test, but they are also observed in the conductors through which the resistance is measured. Fractures in the chip to TPU interconnection and Cu wiring on the chip were not observed by optical microscopy. Closer inspection of the Cu/ICA/Ag interconnection from a sample that has been bent over a similar radius of curvature as used in the bending tests, using 3D XRM, suggests that the interconnection has remained intact even though the low imaging resolution is not able to reveal µm-level discontinuities. The XRM image (Fig. 8) reveals the fractures of the Ag electrode close to the edge of the support adhesive.

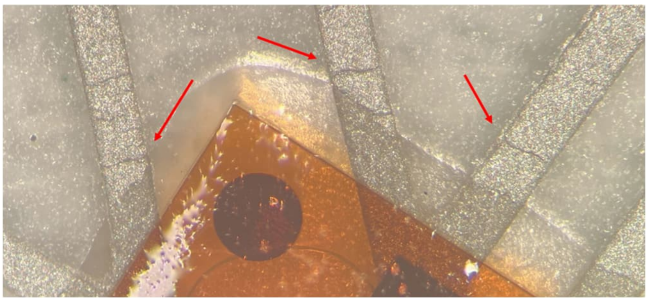

Fig. 7. Fractures in silver conductors after the compression bending test.

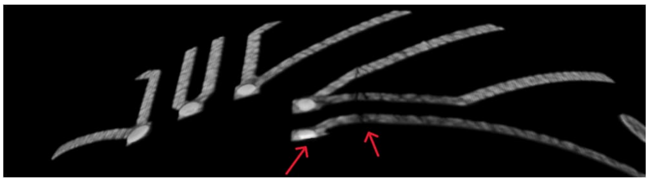

Fig. 8. 3D X-ray microscope image showing Ag electrodes and ICA at interconnection locations (left red arrow) and the fractured Ag electrode at location to where the support adhesive extends at edge of chip (right red arrow).

The location of the fractures can be explained by a change in material stack, which increases the local stiffness and its behavior under the bending. This change in stiffness forms the highest strain-stress concentration near to the adhesive region. This is previously studied in the case of stretchable electronics applications [5-7]. In the compression bending tests, the Ag electrodes were subject to compressive stress and the fractures induced by the compression bending did not consistently result in completely open circuits during the bending cycle. In these tests, the ROP Cu wiring was subject to an expansion stress, since the PI chips were assembled face down on the TPU. Thus, the results indicate a promising robustness of the flexible ROP wiring towards bending stress, but revealed a weak point at the edge of the more rigid adhesive.

Based on the bending test results, a flexible underfill material was tested to decrease the stress on the Ag electrode where it meets the adhesive edge. Stretching tests were conducted to compare the resistance change between the samples supported by the flexible underfill adhesive and the rigid glob-top during cycling. Preliminary tests indicate that the flexible underfill adhesive material decreases the stress on the conductive path from the Ag electrodes through the chip interconnections. All tested samples with the underfill adhesive withstood 100 stretching cycles, with the final maximum resistance remaining within ~2 to 20% of the initial maximum resistance. For the glob-top supported samples, 3/4 samples showed an increase of several times the normalized resistance at 10% maximum strain in the beginning of the cycling. This suggests a similar defect mechanism of the Ag electrode fracturing as in the bending tests. The encouraging results suggest incorporating the flexible underfill material in further mechanical testing of ROP chips integrated on stretchable and flexible substrates.

IV. Conclusion

ROP flexible IC test chips have been successfully integrated on stretchable TPU substrate. Electromechanical tests indicate a promising robustness of the ROP chip and interconnection towards bending induced stress. The results reveal a critical weakness of the conductor on the TPU close to the edge of the rigid adhesive that provides mechanical support to the chip interconnection. Preliminary results show that the bending induced stresses could be distributed more evenly using a more flexible underfill adhesive, thus improving the overall mechanical robustness of the flex-on-stretch device. More detailed failure analysis of the chip interconnection and Cu wiring on the ROP chip is left for further work. The results indicate possible pathways towards a robust assembly process for flex-on-stretch integration, which would enable replacing some of the conventional Si IC's in e.g. wearable electronics applications using ROP-based flexible chips in the future.

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References

[1] C. S. Buga and J. C. Viana, “A Review on Materials and Technologies for Organic Large-Area Electronics,” *Adv Mater Technol*, vol. 6, no. 6, Jun. 2021, doi: 10.1002/admt.202001016.

[2] Y. Kusaka, N. Fukuda, and H. Ushijima, “Recent advances in reverse offset printing: An emerging process for high-resolution printed electronics,” *Jpn J Appl Phys*, vol. 59, no. SG, Apr. 2020, doi: 10.7567/1347-4065/ab6462.

[3] A. Sneck, H. Ailas, F. Gao, and J. Leppäniemi, “Reverse-Offset Printing of Polymer Resist Ink for Micrometer-Level Patterning of Metal and Metal-Oxide Layers,” *ACS Appl Mater Interfaces*, p. acsami.1c08126, Aug. 2021, doi: 10.1021/acsami.1c08126.

[4] K. Eiroma, A. Sneck, O. Halonen, T. Happonen, H. Sandberg, and J. Leppäniemi, “Miniaturized Micrometer-Level Copper Wiring and Electrodes Based on Reverse-Offset Printing for Flexible Circuits,” *ACS Appl. Electron. Mater.*, vol. 7, no. 8, pp. 3511–3520, Apr. 2025, doi: 10.1021/acsaelm.5c00230.

[5] D. Di Vito, M. Mosallaei, B. Khorramdel, M. Kanerva, and M. Mäntysalo, “Mechanically driven strategies to improve electromechanical behaviour of printed stretchable electronic systems,” *Sci Rep*, vol. 10, no. 1, Dec. 2020, doi: 10.1038/s41598-020-68871-w.

[6] M. H. Behfar *et al.*, “Fully Integrated Wireless Elastic Wearable Systems for Health Monitoring Applications,” *IEEE Trans Compon Packaging Manuf Technol*, vol. 11, no. 6, pp. 1022–1027, Jun. 2021, doi: 10.1109/TCPMT.2021.3082647.

[7] T. Happonen, P. Järvinen, M. Paakkolanvaara, and T. Alajoki, “Reliability Assessment of Temperature Sensors Integrated on Elastic Substrate,” in *2024 IEEE 10th Electronics System-Integration Technology Conference, ESTC 2024 - Proceedings*, Institute of Electrical and Electronics Engineers Inc., 2024. doi: 10.1109/ESTC60143.2024.10712123.