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SINGLE-EVENT EFFECTS AND RADIATION HARDENING IN DIGITAL CIRCUITS

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ABSTRACT

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Single-event effects (SEEs) are a group of phenomena manifesting for the most part, in integrated circuits (ICs). SEEs are disruptions in the operation of circuits, that are caused by ionizing radiation. The kind of ionizing radiation most commonly associated with SEEs is high energy particle radiation, such as very fast-moving alpha particles and other heavier ions. The highest particle fluxes in nature are encountered in space and high in the atmosphere. This is a cause of major concern for the reliability of modern systems operating in these conditions. Bit flips and data corruption are the most concerning outcomes of SEEs along with total system failures and damaged circuitry. There exists, however, a multitude of radiation hardening methods for ICs designed to combat SEEs and their consequences.

This thesis presents a literary overview of SEEs and physics related to them as well as a look at common radiation hardening methods, all from the point of view of digital systems. Firstly, background physics and radiation environments relevant to this thesis are laid out. In the third chapter, common relevant SEE types are discussed: single-event upset (SEU), single-event functional interruption (SEFI), single-event transient (SET) and single-event latchup (SEL). Finally, relevant radiation hardening methods are presented. These are split into radiation hardening by process (RHBP) and radiation hardening by design (RHBD).

It is concluded in this thesis that there are many ways to combat SEEs in ICs with different circuit designs and manufacturing processes. Other radiation hardening methods are more relevant than others and RHBD has become the preferred method to RHBP due to modifications to manufacturing processes being a costly endeavor. Space exploration has been a growing area of interest over recent years so more knowledge over the challenges of digital systems in this environment has become paramount.

Keywords: Single-event effects, Single-event upset, Radiation hardening by process, Radiation hardening by design

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TIIVISTELMÄ

Joonas Kelavuori: Yksittäistapahtumat ja säteilykovetus digitaalisissa piireissä
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Yksittäistapahtumat ovat tapahtumien joukko, jotka ilmenevät suurimmaksi osaksi sulautetuissa piireissä. Yksittäistapahtumat ovat monien järjestelmien vikatilojen syypäitä ja ne johtuvat ionisoivasta säteilystä. Säteilyn tyyppi, joka yleisesti liitetään yksittäistapahtumiin, on korkeaenergistä hiukkassäteilyä, kuten suurinopeuksiset alfahiukkaset ja suuremmat ionit. Intensiivisimmät hiukkasvuot luonnossa sijaitsevat avaruudessa ja korkealla ilmakehässä. Tämä on suuri huolenaihe modernien järjestelmien luotettavuudelle näissä olosuhteissa. Yksittäistapahtumien huolestuttavimmat vaikutukset ovat bittien vaihdokset, datan korruptoituminen, järjestelmien kaatumiset ja vaurioituneet piirit. On kumminkin olemassa useita säteilykovetusmenetelmiä sulautetuille piireille, jotka ovat tarkoitettu ennaltaehkäisemään yksittäistapahtumia ja niiden vaikutuksia.

Tämä työ on kirjallisuuskatsaus yksittäistapahtumista ja niiden ymmärtämisen kannalta tärkeistä fysiikan ilmiöistä, sekä myös säteilykovetustavoista. Tämä kaikki tehdään digitaalisen elektroniikan näkökulmasta. Ensin työssä käsitellään työn kannalta tärkeät taustalla olevat fysiikan ilmiöt ja säteily-ympäristöt. Kolmannessa luvussa tarkastellaan työn kannalta tärkeitä yksittäistapahtumia: yksittäisvaihdos, yksittäistoiminnanpysäytys, yksittäistransientti ja yksittäislukitautuminen. Viimeiseksi tarkastellaan säteilykovetusmenetelmiä, jotka on jaettu säteilykovetukseen prosessilla ja säteilykovetukseen suunnittelulla.

Tässä työssä käy ilmi, että on useita tapoja suojautua sulautettujen piirien yksittäistapahtumilta erilaisilla piirisuunnittelutavoilla ja valmistustavoilla. Toiset säteilykovetusmenetelmät ovat ajankohtaisempia, kuin toiset, ja säteilykovetus suunnittelulla on suositumpaa, kuin säteilykovetus prosessilla, sillä valmistusprosessin muuttaminen on huomattavasti kalliimpaa. Kiinnostus avaruuden tutkimiseen on noussut jyrkästi viime vuosina, joten tarve digitaalisten järjestelmien haasteiden ymmärtämiseen tässä ympäristössä on myös noussut.

Avainsanat: Yksittäistapahtumat, Yksittäisvaihdos, Säteilykovetus prosessilla, Säteilykovetus suunnittelulla

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LIST OF SYMBOLS AND ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
BJT	Bipolar Junction Transistor
BOX	Buried Silicon Oxide
BPSG	Borophosphosilicate Glass
CMOS	Complementary Metal-Oxide-Semiconductor
CR	Cosmic Ray
DICE	Dual Interlocked Storage Cell
FDSOI	Fully Depleted Silicon on Oxide
FPGA	Field-Programmable Gate Array
GCR	Galactic Cosmic Ray
IC	Integrated Circuit
IP	Intellectual Property
LEAP	Layout Design Through Error-Aware Transistor Positioning
LET	Linear Energy Transfer
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-Type Metal-Oxide-Semiconductor
PDSOI	Partially Depleted Silicon on Insulator
PMOS	P-Channel Metal-Oxide-Semiconductor
RHBD	Radiation Hardening by Design
RHBP	Radiation Hardening by Process
SEE	Single-Event Effect
SEFI	Single-Event Functional Interruption
SEL	Single-Event Latchup
SEP	Solar Energetic Particle
SET	Single-Event Transient
SEU	Single-Event Upset
SOI	Silicon on Insulator
STI	Shallow Trench Isolation
TMR	Triple-Modular Redundancy

1. INTRODUCTION

As silicon-based transistors in integrated circuits are developing ever closer to their natural physical limits, their natural susceptibility to ionizing radiation has also risen considerably over the years. Nowadays, radiation damage and single-event effects (SEEs) in electronics are a serious issue especially in space- and high-altitude atmospheric environments. Many unique design considerations need to be taken to mitigate device susceptibility to SEEs and their secondary effects such as complete mission failures and loss of human life. [1, p. 29]

Single-event effects are a class of phenomena caused by an interaction between a semiconductor device and a single high-energy particle. These particles include very fast-moving heavy ions, alpha particles and protons along with other smaller particles I will be discussing in this thesis. High-energy particles can ionize silicon, creating unwanted charge carriers potentially leading to a non-destructive SEE or a soft-error such as a single-event upset (SEU) where a bit is flipped from a 1 to a 0 or vice versa. [1, p. 31] An SEE can also lead to a destructive hard error such as a single-event latchup (SEL) where parasitic transistor structures get activated leading to high currents and possibly a burn-out of the struck complementary metal-oxide-semiconductor (CMOS) device. [2, p. 40]

Radiation hardening is the study of hardening devices against radiation effects, such as single-event effects. Radiation hardening can be achieved by modifying the fabrication process, layout of transistors, or the circuit topology of an integrated circuit (IC). [1, p. 63] These methods can be combined to create robust designs capable of enduring the harshest radiation environments.

The purpose of this thesis is to shed light on the nature of SEEs and to discuss the relevant radiation hardening methods aimed at mitigating them through literary overview. I will first be discussing the relevant physics and environments, after which I will move on to discussing SEEs. After shedding light on SEEs, I will discuss the relevant radiation hardening methods.

2. BACKGROUND

To understand single-event effects, and furthermore, radiation hardening – it is important to first look at the environment in which we exist in together with electronics from the perspective of ionizing radiation and physics relevant to this thesis. This chapter covers these topics.

2.1 Ionizing radiation

Ionizing radiation is defined as electromagnetic or subatomic radiation that possesses sufficient energy to detach electrons from atoms or molecules. This creates a free electron, and a positively charged particle called an ion. A single ionizing particle can ionize a considerable amount of atoms. This can create an accumulation of charges in electronics, which is one of the main focus-points of this thesis. [1, p. 16]

Ionizing electromagnetic radiation includes everything from upper ultraviolet part of the electromagnetic spectrum and up in photon energy. This range naturally includes X-rays and gamma rays as seen in figure 1.

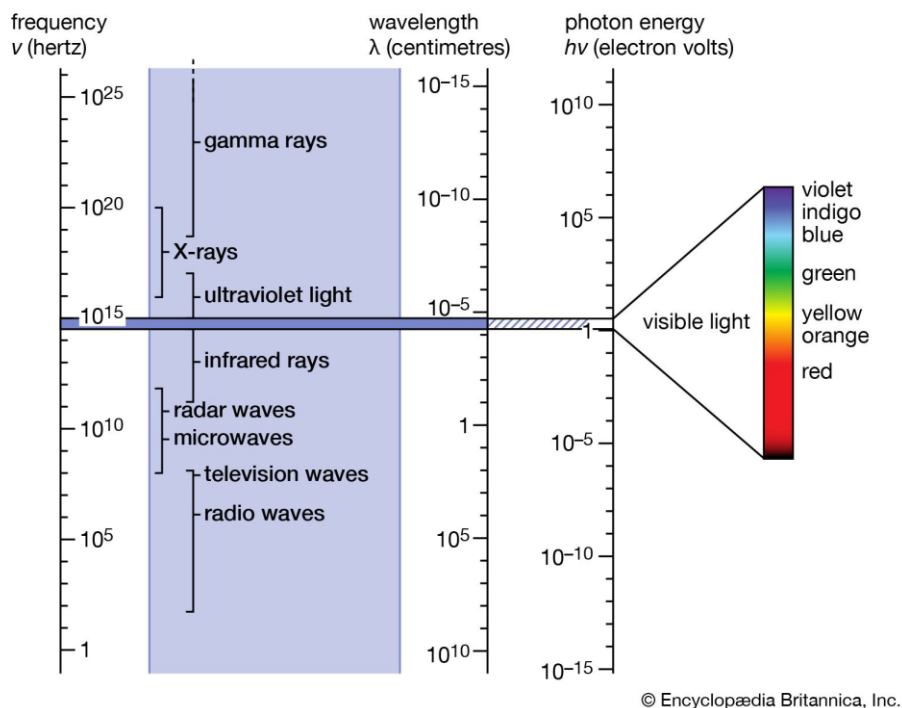


Figure 1. Electromagnetic spectrum [3].

While ionizing electromagnetic radiation can indeed ionize matter, in the case of single-event effects, a single photon's effect is negligible. A single gamma ray for instance can

lead to ionization of a handful of atoms at most. For all intents and purposes, high energy electromagnetic radiation doesn't cause single-event effects in electronics. High radiation intensity can lead to cumulative radiation damage that has similar outcomes to SEEs but are not considered as such as they need to be induced by a single particle to be considered as SEEs. [1, p. 13]

Particle radiation is the main culprit when it comes to SEE occurrences. [1, p. 15] High speed particles can deposit an order of magnitude more energy into matter than photons and thus can ionize enough atoms to cause SEEs. This includes high speed ions like protons (hydrogen nuclei), alpha particles (helium nuclei) and heavier ions as well as neutrons, electrons, positrons and muons. [1, p. 7] Electrons and muons are known to rarely cause SEEs so they are not considered when looking at SEE mechanisms in this thesis. Positrons are the anti-particles of electrons, so they annihilate quickly creating two photons and thus are not very relevant to SEEs.

2.2 Cosmic rays and solar energetic particles

Galactic cosmic rays (GCRs) are a special form of particle radiation. They originate from outside our solar system and are believed to be formed in supernovae explosions. [4, p. 15] Protons and heavier nuclei are the primary form of cosmic rays. GCRs encompass the most energetic particles encountered and are a constant source of radiation in space. The flux of GCRs is more intense outside our solar system since the sun radiates a vast bubble of charged particles that shield the solar system from GCRs to an extent. [1, p. 4]

One other major source of radiation in our solar system is solar particle radiation consisting of solar energetic particles (SEPs). As with GCRs, SEPs primarily consist of high energy protons and heavier nuclei emitted by our sun during enhanced periods of solar activity. The highest energy SEPs aren't nearly as energetic as highest energy GCRs since supernovae where GCRs originate are one of the most violent events in the universe and release gargantuan bursts of energy.

GCRs and SEPs are often put under a general category of cosmic rays (CRs). This is helpful since GCRs and SEPs are very similar by nature and streamlines the discussion around them.

2.3 Indirect ionization

Ions and protons can directly ionize the target material unlike charge-neutral neutrons. However, all three of them can participate in nuclear reactions in the material they hit.

These nuclear reactions can create ionizing nuclear radiation that further ionizes the material. This process is called indirect ionization. [5, p. 119] The relevant ionizing products of these nuclear reactions are, again, heavy ions, protons and neutrons as can be seen from figure 2.

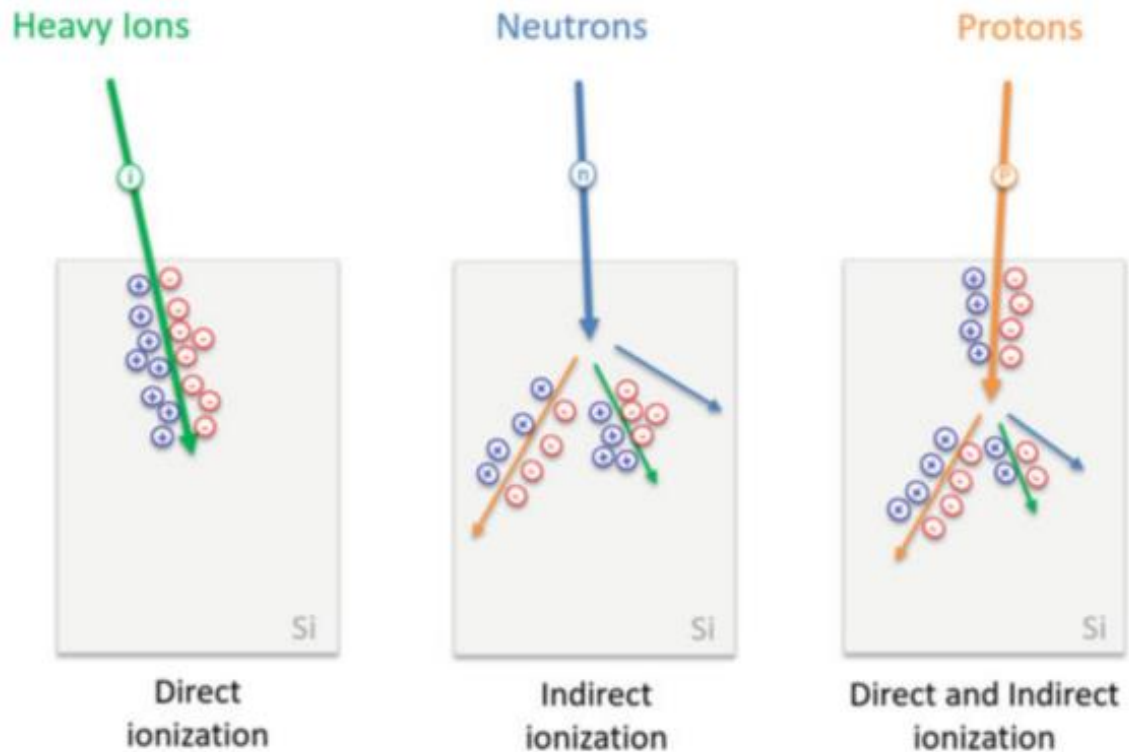


Figure 2. Direct and indirect ionization in silicon [1, p. 16].

While nuclear reactions caused by heavy ions occur, they are an insignificant cause of ionizations in target material compared to their potent direct ionization. Meanwhile protons have relatively high indirect ionization potential compared to their direct ionization potential.

Neutrons are chargeless and thus cannot directly ionize material. However, neutrons can more easily penetrate cores of atoms and consequently cause nuclear reactions and furthermore indirect ionizations thanks to their neutral charge. [1, p. 13] Electron clouds of atoms repel negative charges and protons in atomic nuclei repel positive charges, so incoming neutrons are not affected.

2.4 Radiation environments

Different radiation environments have different particle fluxes that are composed of different kinds of particles with different energies. This creates unique requirements for different kinds of electronic systems for different radiation environments and missions.

Radiation environments are not limited to space and atmospheric environments. For example, nuclear plants [6, p. 123] and particle accelerator environments [1, p. 9] often require some precautions relating to radiation on electronics.

2.4.1 Space environment

The kind of ionizing radiation in space, that can induce single-event effects in electronics is mainly composed of GCRs and SEPs. However, in near-Earth space there exists a type of radiation zone called the Van Allen Belts which can be seen in figure 3. This is a product of the Earth's magnetosphere trapping charged particles into radiation zones around the Earth. Van Allen Belts can be divided into inner and outer belts. The inner belt consists mainly of high-energy protons while the outer belt has a mix of protons and electrons. The Van Allen Belts are highly dynamic by nature since Earth's magnetosphere is in constant flux and highly dependent on solar activity. While subjected to intense solar winds, Earth's magnetosphere is squeezed and thus the Van Allen Belts shift to lower orbits. [1, p. 2]

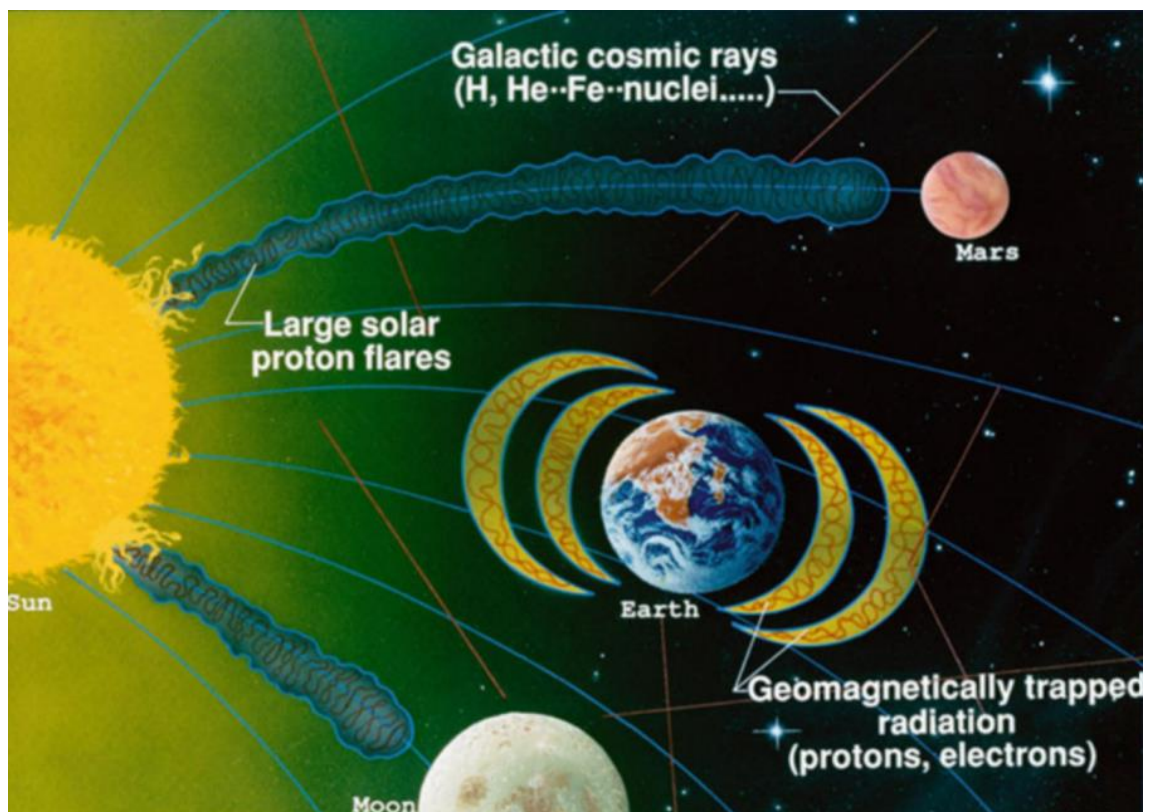


Figure 3. Radiation sources in near-Earth space [1, p. 2].

Geomagnetically trapped radiation belts are not unique to Earth. Other planets with notable magnetic fields can also trap charged particles into radiation belts. For example, Jupiter has a much harsher radiation belt compared to Earth's. [6, p. 1]

2.4.2 Atmospheric environment

A major source of particle radiation on Earth and in the atmosphere are cosmic ray air showers. Figure 4 illustrates the process of cosmic ray showers. When cosmic rays enter the atmosphere, they collide with atmospheric particles, mainly nitrogen and oxygen molecules, creating a cascade effect of secondary particles. These cascades continue until the secondary particles no longer have sufficient energy to create more particles in collisions. The secondary particles include protons, neutrons, electrons, positrons, neutrinos, pions, kaons and muons. In many collisions, photons are also created. [1, p. 7]

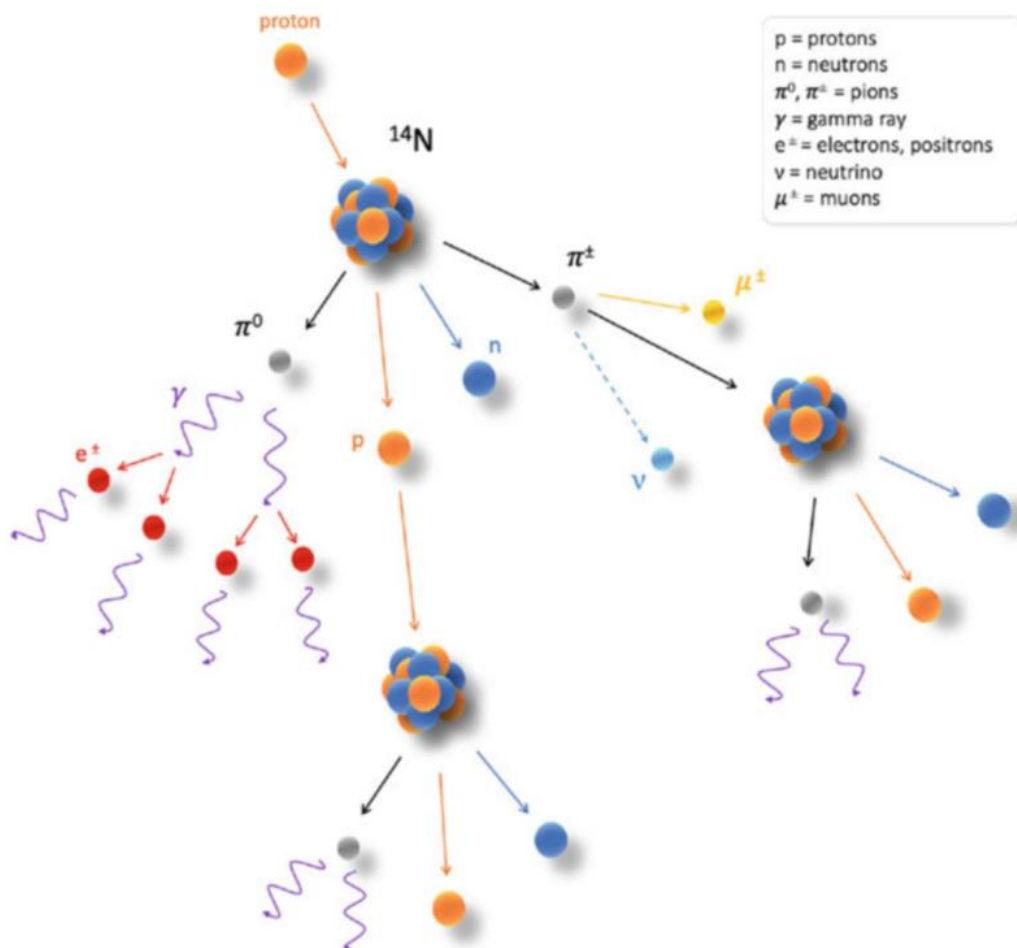


Figure 4. Cosmic ray air shower [1, p. 7].

Out of these secondary particles, a particularly noteworthy one in the context of SEEs together with protons, neutrons and electrons, is the muon. It is a subatomic particle that

has the same negative electric charge as an electron but much higher mass, giving it a greater penetrating potential. It has an average lifetime of 2.2 microseconds [4, p. 43], during which it has enough time to travel several kilometers in the atmosphere or a couple of centimeters in materials like silicon [1, p. 8] potentially ionizing it to cause an SEE.

Needless to say – cosmic ray air showers are very complex processes with a multitude of variables and the main culprit of SEEs particularly in aviation. SEE probability increases with flights taken higher in the atmosphere due to cosmic ray air showers having to traverse through less atmosphere.

2.5 Ionization in semiconductors

When a particle ionizes a reverse biased p-n junction in a semiconductor, as can be seen in figure 5, the resulting charge carriers begin to drift to their respective sides of the junction based on the present electric field. As they do, they create a drift current, which when great enough, can cause a change in state of the device in question.

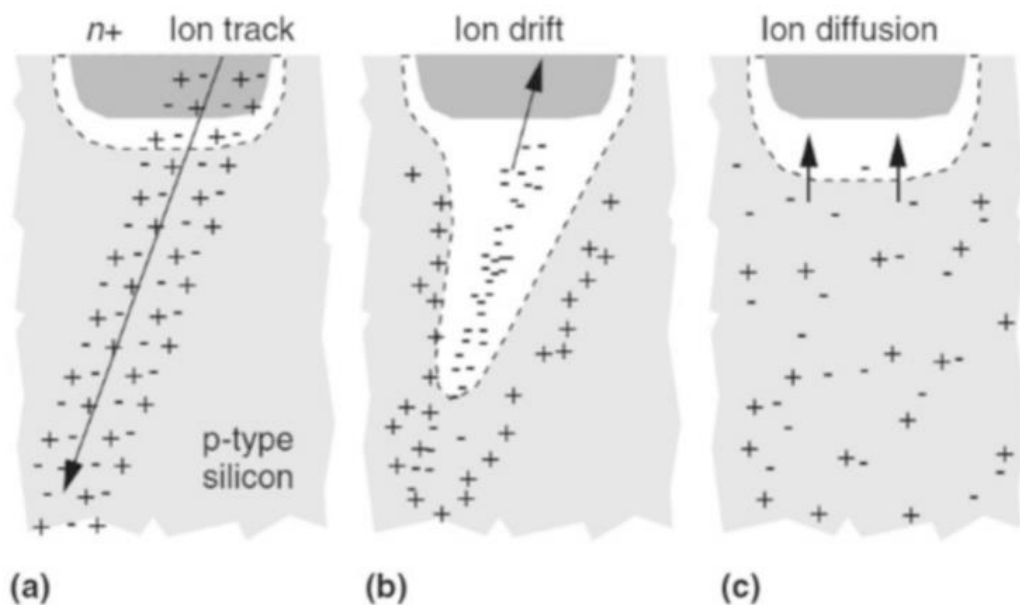


Figure 5. Charge collection mechanism after ion-strike in p-n junction [1, p. 21].

As particle strikes occur in semiconductor materials, the induced charges can distort the electric field of the device enlarging the depletion region in p-n junctions. [7, p. 1] This is known as the funneling effect and is a crucial part of understanding single-event effects. The ionization happens because the particle deposits its energy into the material, ionizing it. This is called the linear energy transfer (LET), and it describes how much of the particle's energy gets transferred to the material. Linear energy transfer is a very often used term when discussing SEEs.

3. SINGLE-EVENT EFFECTS

As highly energetic particles penetrate sensitive areas of a device and create charge carriers, they have the potential to create single-event effects. SEEs can be categorized into soft and hard errors. [5, p. 195] Soft errors are nondestructive to electronics, as no permanent physical damage is done. Hard errors on the other hand are permanently damaging to the device and might require replacement or repair.

3.1 Single-event upset (SEU)

A single-event effect is considered as a single-event upset when a single particle interaction in a memory unit of a digital circuit causes the logic state of said memory unit to change. [5, p. 195] A single particle can induce multiple-bit upsets where the particle or its daughter particles cause an SEU in multiple bit storage cells. [1, p. 34]

Bit storage in modern digital devices is largely implemented by flip-flops, which in turn are implemented via latches made with cross-coupled inverter pairs as seen in figures 6 and 7.

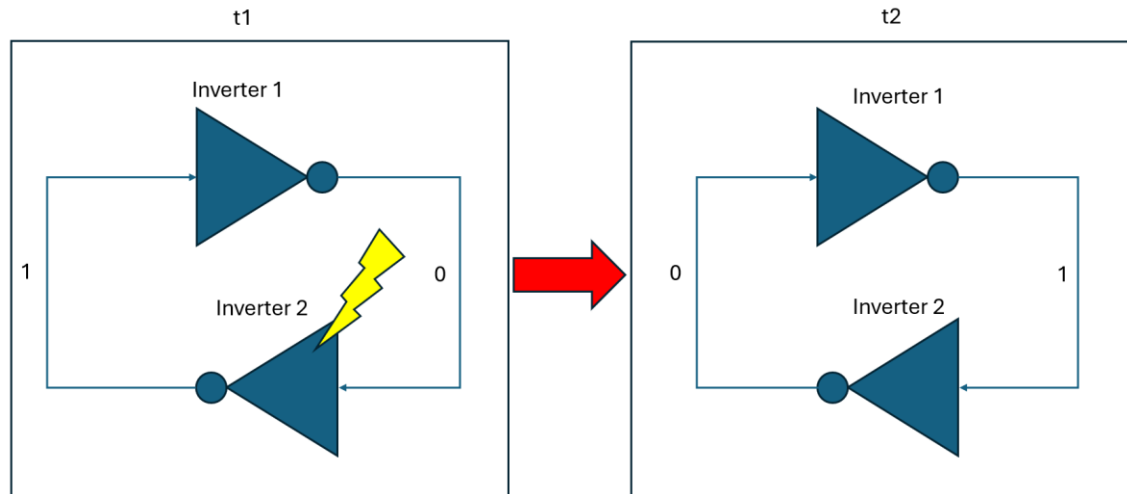


Figure 6. Cross coupled inverter pair SEU (gate level) based on source [1, p. 32].

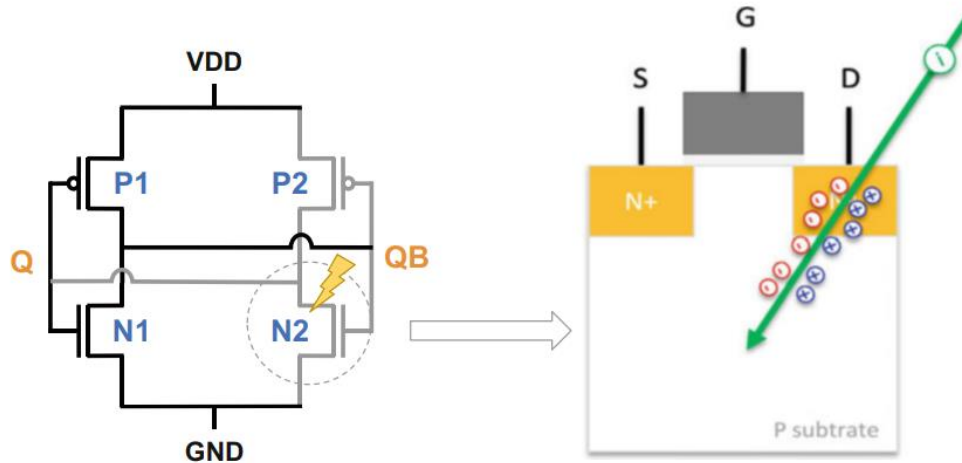


Figure 7. Inverter SEU (transistor level) [1, s. 32].

As a particle strikes an off-state transistor in the inverter pair, given high enough ionization, the bit under storage can be subject to change. The minimum required charge collected to change the output signal of the circuit is known as the critical charge. [1, p. 33] This is linearly dependent on the nodal capacitance of the transistor and varies with the materials and geometry of the transistor.

3.2 Single-event functional interruption (SEFI)

When an SEU corrupts data so that the corrupted data path leads to a loss of operation, the event is called a single-event functional interruption (SEFI). These usually manifest in larger, more complex ICs such as Field-programmable gate arrays (FPGAs), processors, Application specific integrated circuits (ASICs) and modern memories. [5, p. 196] This stems from the fact that they often rely on very accurate logic states to maintain function and any disruption in control signals could indeed impact the function of said circuit.

Soft errors can be, however, intercepted by the system's own error detection and can be corrected with a system reset for example. SEFIs are very detectable since the system often ceases correct function. A "blue screen of death" for instance on a Windows computer could very well be caused by an SEFI in some of the cases.

3.3 Single-event transient (SET)

A typical SEU happens with a direct particle strike in a memory element. In digital logic, memory elements such as d-flip-flops are almost always connected via combinational logic consisting of gates and connections. A sufficiently violent particle interaction in a

combinational logic gate may cause a high enough voltage transient which can propagate to a memory element and cause a bit flip. [1, p. 37] This event is called a single-event transient (SET). Before the propagating voltage spike can cause a SET, it must pass through three basic masking effects of combinational circuitry. [8, p. 13]

As the voltage spike needs to propagate through various elements in the circuitry, the signal loses magnitude and/or amplitude during its' travel due to electrical losses. The transient can also be tightened or broadened when traveling through logic gates. Alternatively, the transient can also be not propagated at all if its' duration is shorter than the gate delay. These effects are all parts of the electrical masking effect and act as a major roadblock in the formation of SETs. [9, p. 1] [1, p. 38]

If a big enough transient occurs in combinational logic and it manages to appear in the input of a logic gate as a false bit, it may manifest in the output of said logic gate. That is if the false bit in the input has any impact on the output. If the gate is for example a two input AND gate, and the other non-corrupted input is a logical 0, the other input that has the temporary corrupted bit has no impact on the output of the AND gate. This phenomenon is known as the logical masking effect. [10, p. 2] Combinational logic sections of digital circuitry are often multi layered, meaning that signals from register to register need to travel through several logic gates. This naturally amplifies the chance for logical masking effect to occur.

During SET propagation, if the transient manages to reach the input of a register, it has the potential to corrupt the bit. That is if the electrical masking effect hasn't diminished the signal enough and the transient reached the register in the clock transition time window where the register is to capture the input bit. The latching-window masking effect occurs when the big enough transient reaches the register input, but not when the latch captures the input bit. [11, p. 3] As one might imagine, the potential for latching-window masking effect to occur diminishes with higher frequency clock signals.

3.4 Single-event latchup (SEL)

Current lithography processes print transistors to a single piece of silicon in high density. Adjacent transistors are therefore electrically connected to an extent. Due to this, there exists parasitic structures within the substrate. In normal circuit operation, these structures seen in figure 8 are in a high-impedance state or in other words in a high-voltage/low-current state. The structures are made of parasitic bipolar junction transistors (BJTs) and are formed between a p-channel metal-oxide-semiconductor field-effect transistor (MOSFET) device and an n-channel MOSFET device.

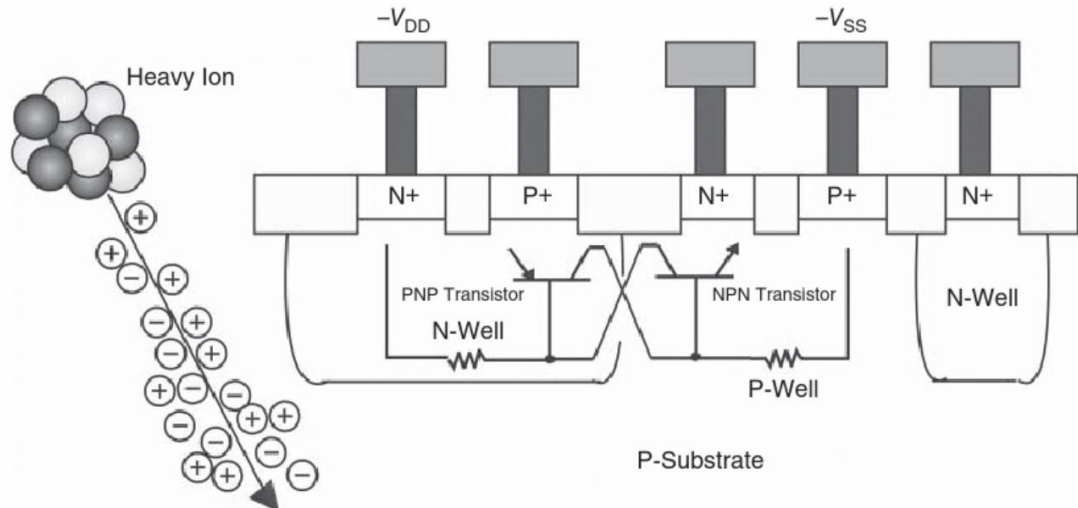


Figure 8. Single-event latchup [6, p. 147].

When a particle strike occurs, given high enough charge deposition, the parasitic BJTs can activate and create a low-impedance path between operating voltage rail and ground. This is also called a low-voltage/high-current state. When this state is reached, it is considered a single-event latchup (SEL). [5, p. 205]

When a SEL occurs, the current jumps to a high level. This can break the CMOS device due to high power. The high power causes the device heat up and can break the device in under a second. This can be prevented via a power reset during SEL. [1, p. 41]

4. RADIATION HARDENING

Launching equipment into low earth orbit is rather costly, although prices have come down over the 21st century. Traditional radiation shielding has usually been achieved by encasing electronics into heavy shielding materials. This might not be the wisest method in space and aviation since added weight has a price. When it comes to sending equipment deeper into space from low earth orbit, the extra weight causes the need for longer burn times when wanting to exit earth's gravitational field or to change orbit. This in turn needs more fuel, so it is best to keep weight as low as possible.

Radiation hardened electronics are designed to tolerate radiation with little to no actual physical shielding around them. This makes them essential for space travel and other harsh radiation environments. There are two main high abstraction methods for radiation hardening as can be seen in figure 9: radiation hardening by process (RHBP) and radiation hardening by design (RHBD).

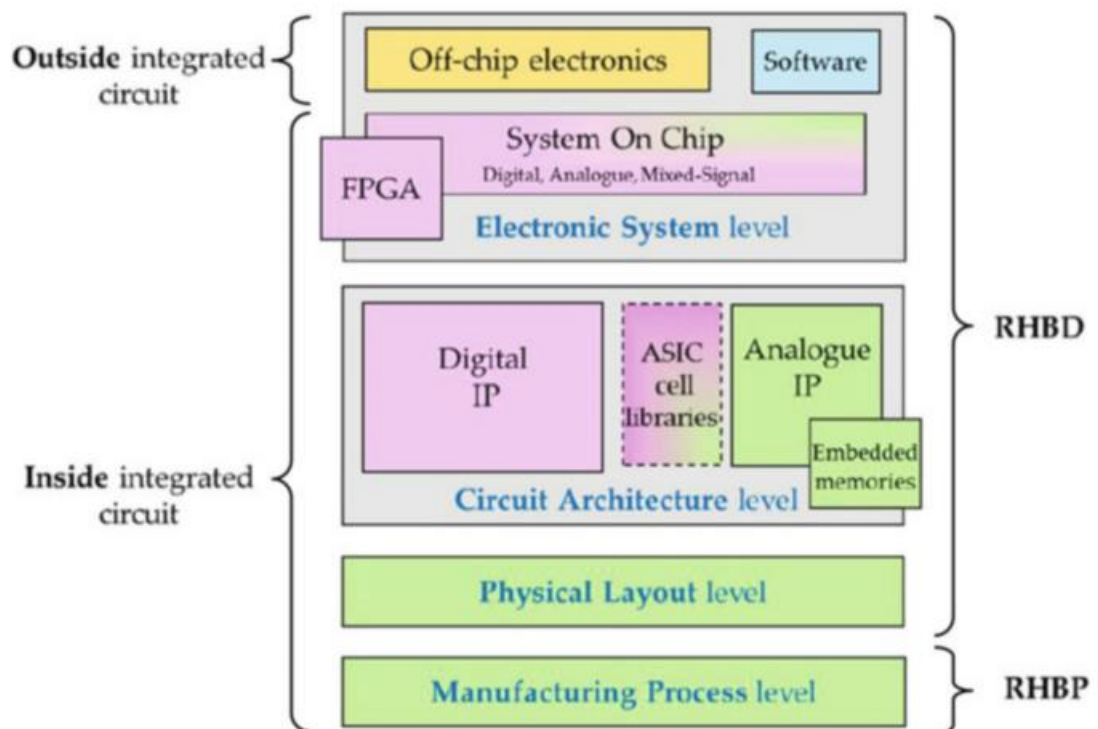


Figure 9. Radiation hardening abstraction levels [1, p. 64].

In RHBP, radiation hardening is achieved by modifying the manufacturing process of the device in question. For ICs, this includes modifying the doping profile and substrate as well as the use of different materials. In RHBD, radiation hardening is achieved by physical layout- and system level choices. The physical layout choices aim to reduce charge

collection while system level design aims to mask errors and prevent system failures caused by radiation. Today, RHBD is the preferred method since chips made with RHBP are several generations behind modern ICs in performance. Modifying the manufacturing process of ICs is also very costly.

4.1 Radiation hardening by process (RHBP)

Radiation resilience of components intended for space use was initially achieved mainly by radiation hardening by process. Radiation hardening by process focuses on the use of unorthodox materials and doping profiles in the fabrication process. Modifications to fabrication processes are often, in the case of commercial products, proprietary, so it is difficult to access industry-specific information. There exists, however, a multitude of different studies focused on techniques for radiation hardening by process.

When borophosphosilicate glass (BPSG) was used for planarization between metallic layers in semiconductor devices, the boron-10 isotope present would pose an increased SEE rate. Boron-10 has a high chance of neutron capture when hit by cosmic neutrons. When neutron capture occurs, the boron atom undergoes fission, producing an alpha particle, a lithium-7 isotope, and a gamma photon. Extra alpha- and gamma radiation inside a chip of course increases SEE-rates. [12, p. 2]

It has been demonstrated that removing BPSG layers reduces SEE-rates. If using BPSG is mandatory, boron-11 isotope is a much better choice, since it has a much lower chance of neutron capture. A purification process is necessary to isolate boron-11 for use in BPSG. Another trick to prevent neutron capture in critical places is to use boron shields. Chips can be covered with a B_4Si_3 -layer or the chip packaging can be doped with boron to facilitate neutron capture far away from critical components. [13, p. 3] Alpha particles generated in boron shields do not reach critical nodes of the device since alpha particles have a very low penetrating potential when generated through fission.

Nowadays BPSG is no longer generally used in standard fabrication processes more advanced than 130 nm scale. Boron is still present in critical nodes of semiconductor devices as a doping material in many mainstream technologies and can facilitate SEEs. [14, p. 1] Use of boron-11 as doping material instead of boron-10 is advised if better radiation hardness is needed.

Another widely used radiation hardening method is the use of silicon-on-insulator (SOI) technology. SOI adds a buried silicon oxide (BOX) layer seen in figure 10, that acts as an insulator, into the transistor substrate. SOI wasn't developed specifically to combat

radiation effects, but to also increase, among other characteristics, the performance and power efficiency of certain digital circuits. [15]

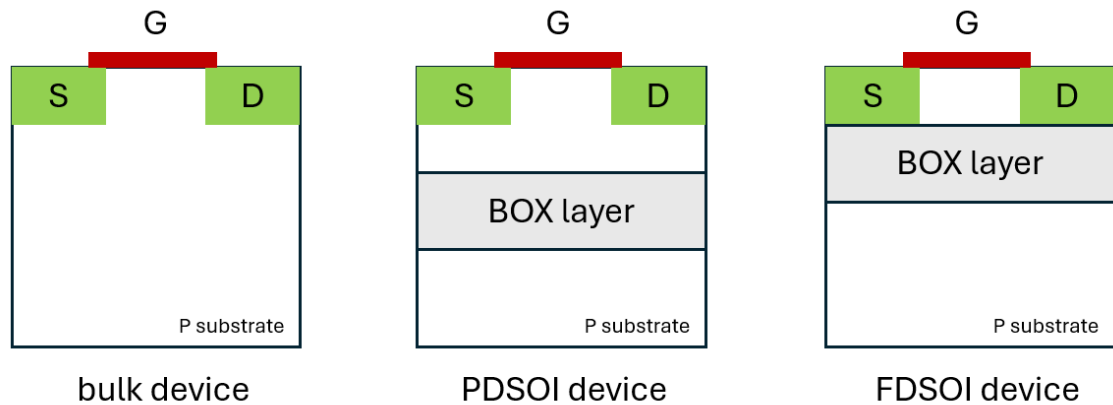


Figure 10. Traditional bulk technology and SOI technology compared, based on source [15].

There generally exists two types of SOI: partially depleted SOI (PDSOI), and fully depleted SOI (FDSOI). FDSOI has a minimal silicon thickness on top of BOX layer while PDSOI has a thicker one. Both are used in slightly different applications, but FDSOI is the preferred one for radiation hardening. In the context of radiation hardening, major benefits of SOI are the decreased silicon volume in which charges generated by radiation can manifest, SEL immunity, funneling effect immunity. [16, p. 1] The decrease in silicon volume comes from the BOX layer limiting the sensitive silicon on top of BOX layer. The BOX layer breaks up the parasitic transistor structures that would be otherwise present in the formation of SEL, so that SEL cannot form.

4.2 Radiation hardening by design (RHBD)

It is possible to reduce SEE: s without modifying the fabrication process by using radiation hardening by design. Many of the upsides of current state-of-the-art CMOS technology can thus be retained even in radiation hardened chips. Layout based techniques aim to achieve radiation hardening by creative ways of component positioning on silicon as well as modifying component geometry. Circuit based techniques aim for radiation hardening by circuit topologies.

4.2.1 Layout-based techniques

A common way to reduce leakage currents induced by radiation is the use of edgeless transistors. In a typical transistor layout, the source and drain nodes of a transistor can

be weakly connected through the shallow trench isolation (STI) oxide present around the transistor. If this oxide is ionized sufficiently due to radiation, a conducting path may be created between the source and drain and leakage current follows. In edgeless transistor layout, the geometry of the transistor is such that the source and drain do not have a straight path to each other through the STI as can be seen from figure 11.

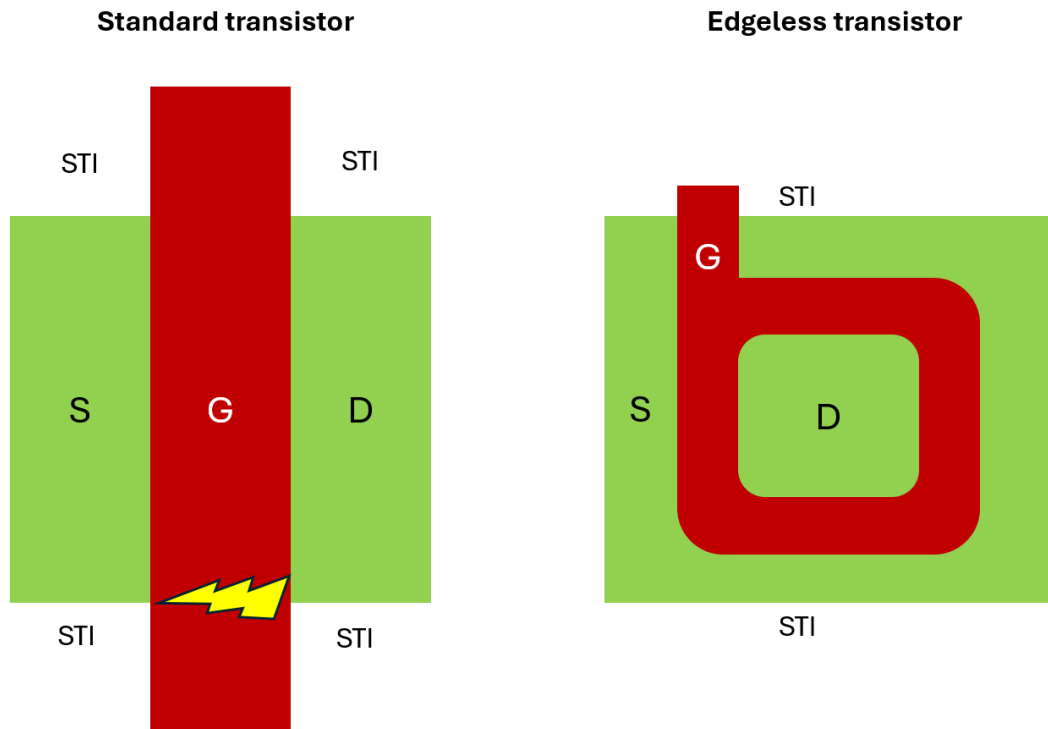


Figure 11. Comparison of standard transistor layout with parasitic leakage path and edgeless transistor layout based on source [17].

The drain is placed in the middle of the layout with source covering the edges of the layout. Gate node is placed between the two. The main drawback with using edgeless transistors is their area needs and dimensions.

STI regions exist to isolate transistors from each other on the die. Transistors are fabricated very densely on the die to achieve high performance in modern chips. The same kind of parasitic leakage current can occur between transistors through STI regions as between a single transistor's source and drain. Edgeless transistors are only useful in preventing leakage currents inside the transistor. For cross-device leakage current protection, so called p+ guard rings are often used alongside edgeless NMOS transistors, while n+ guard rings are used for CMOS transistors. The guard rings are fabricated around the transistor as illustrated in figure 12. The p+ guard rings are grounded and catch any intra device leakage currents while the n+ rings are connected to an operating voltage. [1, p. 69]

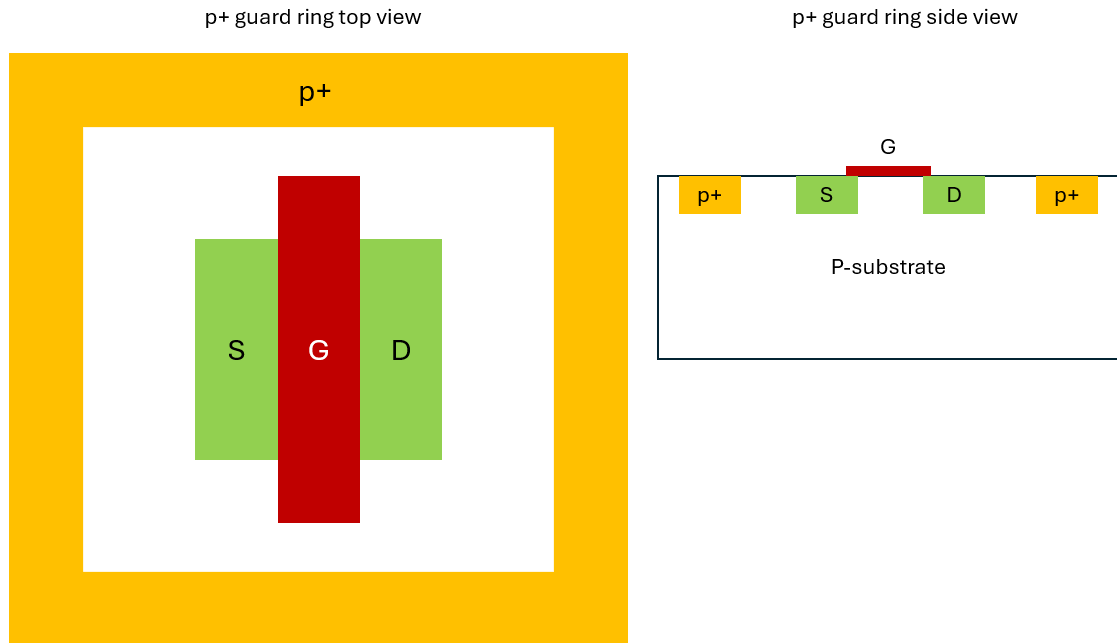


Figure 12. Common p^+ guard ring layout based on source [1, p. 70].

A major downside with guard rings is the increased area requirements. Dual guard rings have also been tested where both PMOS and NMOS transistors have guard rings, but this doesn't improve SEL immunity in a major way. Thus, often single guard ring configurations are preferred.

Transistor positioning has also been studied as an RHBD strategy. It has been shown that in inverter design, placing the NMOS device close to the N-well region can significantly decrease the SET pulse width. This naturally decreases the latching window for a single-event upset. The decreased pulse width can be attributed to the reverse-biased diode that is formed by the N-well and substrate interface that collects the additional carriers created a particle strike in the NMOS device. [18, p. 3] This doesn't come without a cost, however. Studies have also shown that this closer proximity of the PMOS and NMOS devices decreases the LET threshold and increases the saturation SEL cross-section. [19, p. 1] This effect can be offset by substrate and well tap placement for instance as these have a stronger impact on SEL susceptibility.

Layout design through error-aware transistor positioning (LEAP) is another SEE robustness improving transistor layout strategy. The main idea behind LEAP is to position the NMOS and PMOS transistors horizontally so that if a particle pierces the drain nodes of both NMOS and PMOS at the same time, the charge collection of the transistors cancels each other out, shortening the resulting transient pulse as illustrated in figure 13.

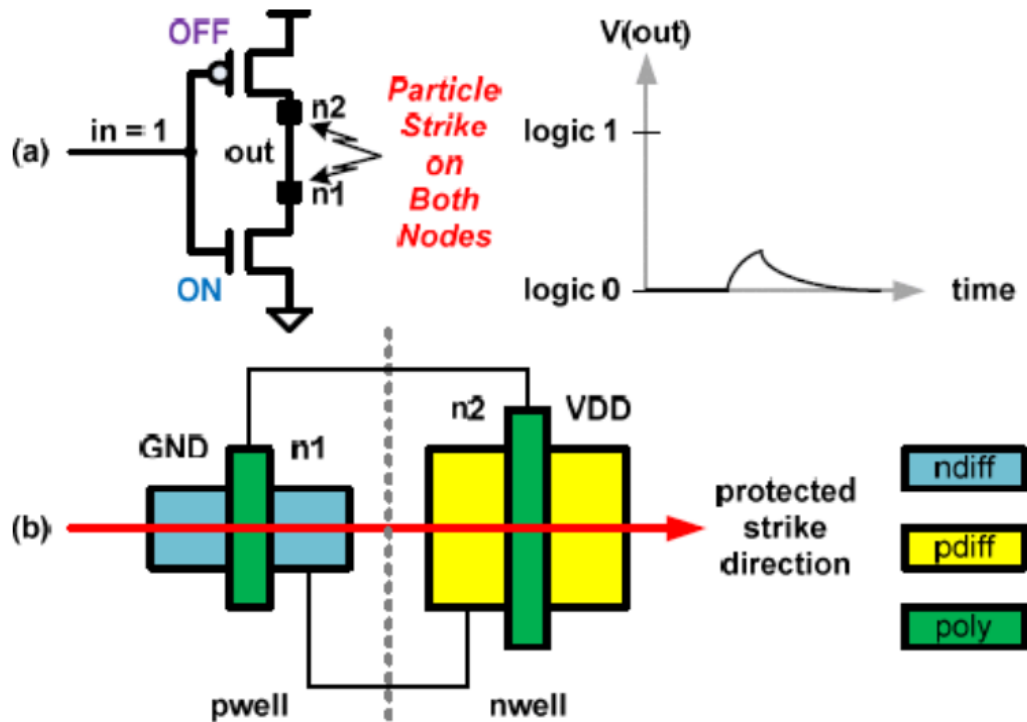


Figure 13. Leap principle for an inverter [20].

The absolute value of transient pulse peak voltage is much higher if the particle strike occurs in only one of the nodes. Depending on the state of the inverter and if the particle strike occurs in the NMOS or the PMOS, the transient pulse can be negative or positive in both logical 1 and 0 states. If the strike occurs in PMOS, the pulse is positive, while a strike in NMOS gives a negative pulse. Sufficiently high pulse can result in a latching of a new logic state. [18]

4.2.2 Circuit-based techniques

While layout-based techniques focus on the prevention of SEE formation in circuits, it is possible to also design systems that tolerate SEEs. Circuit based radiation hardening techniques attempt to achieve just that. Many modern systems rely on circuit-based techniques to mask SEEs, often along with layout-based techniques. As ICs have become more and more complex over the years, they have also become more prone to radiation effects, which calls for a level of fault tolerance. SEEs will always manifest despite layout-based radiation hardening and radiation hardening by process, so it is of paramount importance for a chip to tolerate SEEs. Circuit-based techniques essentially focus on fault tolerance that can be roughly split into four categories: hardware-, software-, information- and time redundancy. [21, p. 8] In the context of this thesis, the most relevant form of fault tolerance is hardware redundancy since it very directly ties into circuit topology.

In hardware redundancy, the most widely used method is the replication of hardware. Replicated components serve the same function as each other and could work a sole component itself as part of a system. Replication only aims to harden the circuit against errors. As system critical components are replicated on-chip, an error in one replicated component becomes meaningless in theory.

A common utilization of hardware replication is triple-modular redundancy (TMR) [1, p. 73]. In TMR, critical intellectual property (IP) components are tripled, and their outputs are connected to a majority voter as illustrated in figure 14.

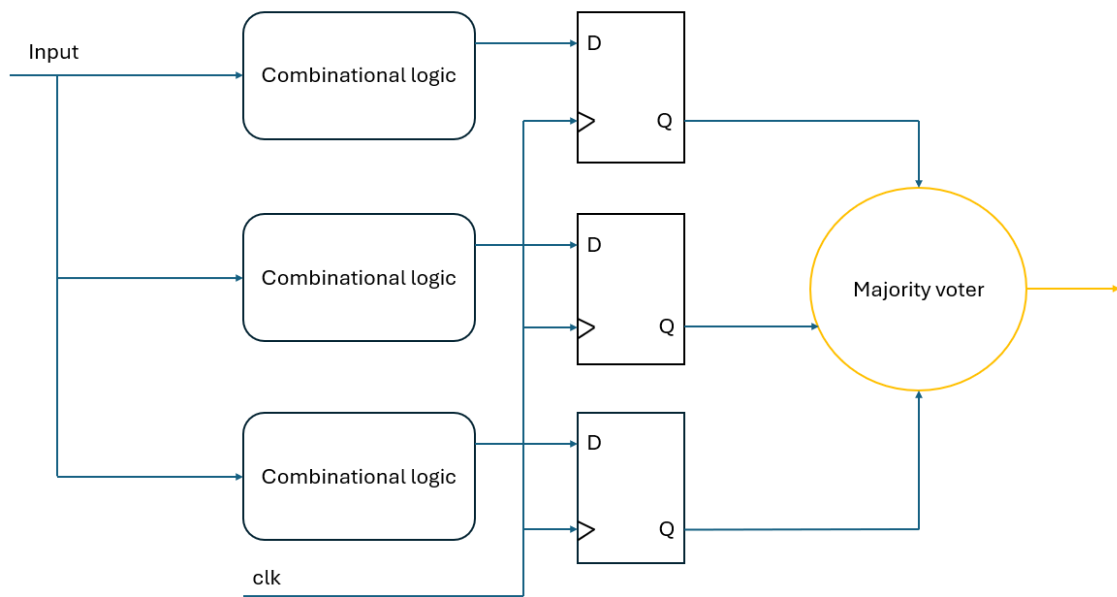


Figure 14. Triple modular redundancy with a majority voter, based on source [22].

The majority voter propagates the input it sees as the most common. If one of the IP components experiences an SEE or other fault that changes its output, the output of that component is ignored. Of course, if two of the IP components experience the same fault at the same time, the faulty output is propagated. As one might imagine, this is very unlikely to happen in common radiation environments unless, in the case of SEEs, the particle flux is extremely intense.

Even the voters aren't perfect. In some critical aerospace applications for example, the majority voters are triplicated also. All data paths are now triplicated where possible. A decision must be reached at some point, however. This is usually done by a highly reliable voting actuator. [20, p. 10]

Triplification of components and signal wires leads to a significant impact on area overhead and power consumption. These are major concerns for battery powered applica-

tions such as autonomous Mars-rovers and other space missions. Temporal TMR attempts to alleviate these concerns by only tripling the output registers. Only one instance of a specific IP component is used to feed the inputs off all three registers as seen in figure 15.

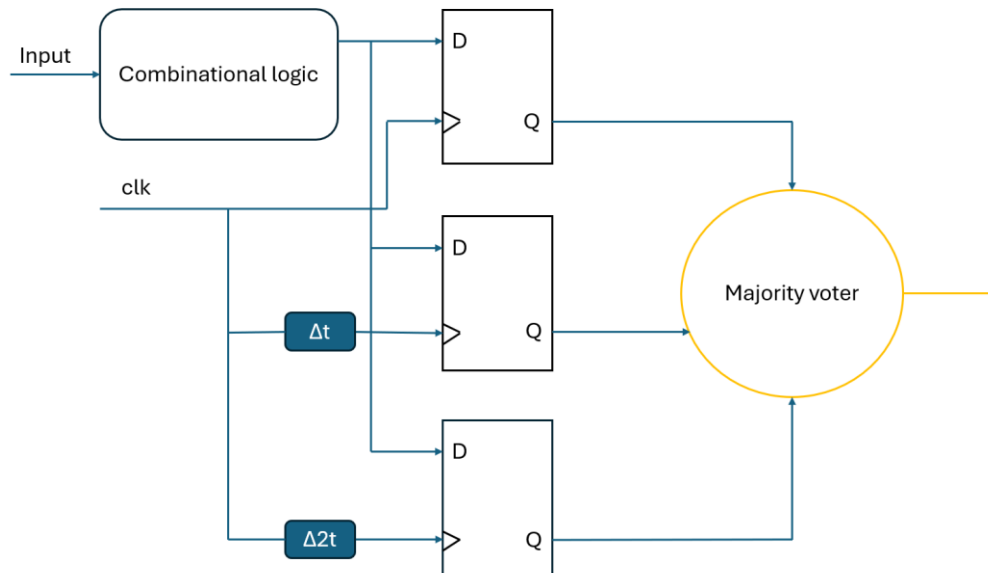


Figure 15. Example of temporal triple modular redundancy, based on source [21].

The ability to filter SET pulses comes from the delayed clock signals. The three registers present are out of sync with each other because of the intentional clock delay. This way, a SET pulse has very little chance to latch to more than one of the registers. If the SET pulse latches to only one of the registers, the majority voter filters it out, naturally. Temporal TMR has a large area advantage to TMR, but it also has a negative impact on the performance of the circuit, due to the clock delays. [1, p. 73]

As corruption of data stored in memory cells is one of the core problems of SEEs in digital circuits, it might make sense to harden memory cells with circuit design. One good way is to use redundant reinforced feedback architectures. Of these, two noteworthy designs are “Quatro-10T” and dual interlocked storage cell (DICE) circuits seen in figure 16. These designs are applied to implement radiation resistant 1-bit Static Random Access Memory (SRAM) cells. The stored bit is defined by multiple interlocking feedback structures that provide a robust level of resistance against charge collection caused by SEEs.

The DICE circuit topology has been the most cited radiation hardened memory design, since it has been extensively validated throughout the years by simulations and experiments. DICE is made up of 12 transistors that are interlocked so that they together make

up four internal nodes that correct each other if charge gets collected by one. [23, p. 3] The logic state of each of the four nodes is controlled by two adjacent nodes that can correct a wrongly charged node.

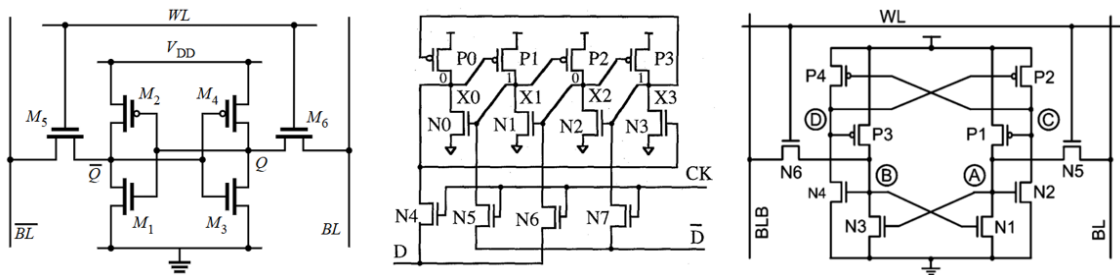


Figure 16. Conventional SRAM, DICE cell, and Quatro-10T topologies from left to right [22][23].

The aim of Quatro cell design is to improve the area overhead and data stability compared to DICE cell. Quatro-10T cell as the name implies, is made of 10 transistors instead of the 12 needed for a DICE cell. Quatro-10T has four storage nodes like DICE, but the nodes are made of two cross coupled inverter pairs [24, p. 2]. Conventional Quatro-10T is an improvement over DICE in area overhead, operating speed, power consumption and simplicity.

Quatro-10T tends to be less radiation resistant compared to DICE, but the truth is much more nuanced. DICE is often the chosen design when extreme radiation robustness is required. Some literature, however, points to Quatro-10T being the better choice. In these deeply scaled technologies, many factors, such as the charge sharing phenomena affect the performance of micro scale circuits. Circuit- and layout-based techniques can be used in tandem to optimize performance. To address the issue of charge sharing in DICE circuits, it has been shown that combining DICE with LEAP can reduce SEU rates by two orders of magnitude. [25, p. 3] There exists a variety of other technique mixing methods that, for example, can focus on nodal spacing optimization to reduce the effects of charge sharing. [26, p. 1]

5. CONCLUSIONS

In this thesis a literary overview of common SEEs, the relevant physics behind them and hardening methods against them were provided. SEEs are a source of data corruption, broken transistors and circuits, and potential mission failures in radiation environments. They pose a huge challenge for modern digital ICs and need to be accounted for with radiation hardening or physical shielding.

Firstly, the relevant background physics was explained together with the most relevant radiation environments in which SEEs are the biggest problem. Ionizing radiation is the source of SEEs. The most dangerous kind of radiation for ICs is high energy particle radiation such as high energy alpha particles, which are often cosmic rays generated from our sun or from outside our solar system. This radiation, when penetrating the right junctions in semiconductors, can generate charge carriers by ionizing the semiconductor material.

In Chapter 3, different types of SEEs were discussed. The most relevant and most well-known of SEEs is SEU. In SEU, a stored bit is flipped due to a particle strike resulting in possible data corruption or faulty control signal. A multiple bit upset is the same fundamental process but with one particle strike inducing multiple bit flips. SET is a process in which a stored bit is flipped indirectly by a transient pulse originating from a component other than the bit storage unit. Masking effects were also discussed that hinder SET pulses. SEFI is the loss of bigger operations due to SEU. These can manifest in bigger systems such as ASICs. Lastly, SEL was discussed. SEL is the activation of parasitic transistor structures induced by a particle strike in CMOS technology. During SEL, large currents are often observed and can result in the burnout of said CMOS device.

Lastly, I looked at common radiation hardening methods aimed at combatting SEEs and other radiation effects. Radiation hardening can be split into two main categories: radiation hardening by process (RHBP) and radiation hardening by design (RHBD). RHBP aims to harden ICs by modifying the fabrication process, while RHBD aims to harden chips by designing clever transistor geometries and circuit topologies.

Understanding SEEs and radiation hardening is crucial for the reliability of equipment in radiation environments, particularly space. With the advent of commercial space travel and humanity's renewed interest in space exploration, the need for reliable radiation hardened chips has never been higher.

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