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## RESEARCH ARTICLE

# True-Time-Delay Receiver IC With Reconfigurable Analog and Digital Beamforming

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**ABSTRACT** Spatial diversity advantages such as improved signal-to-noise ratio and in-band blocker filtering can be achieved through beamforming in the digital and/or analog domain. Digital beamforming benefits from the precision and efficient parallelization of digital signal processing. On the other hand, analog beamforming allows the filtering of in-band but out-of-beam blockers before the ADC which can improve the dynamic range performance of the receiver. A delay method based on resampling has recently emerged as a viable solution for enabling true-time-delay analog beamforming receivers, which overcome the fractional bandwidth limitation of phase-shift beamforming due to beam squint. This paper presents a 22-nm CMOS receiver prototype that enables reconfiguration between true-time-delay analog and digital beamforming to allow choosing the more suitable operation mode in different signal environments. The reconfigurability is achieved by exploiting the time-interleaved nature of both the resampling delay setup and high speed ADCs. In addition to the beamforming mode reconfigurability, the receiver achieves state-of-the-art 2 GHz instantaneous beamformed bandwidth in the analog mode. The receiver reaches a 100% fractional bandwidth at the low end of the 1–6 GHz frequency range.

**INDEX TERMS** Analog beamforming, beam squint, CMOS, digital beamforming, integrated circuit, phased array, radio receiver, spatial filtering, true-time-delay.

## I. INTRODUCTION

Beamforming allows advantages from spatial diversity such as multiple-input multiple-output communications, improved signal-to-noise ratio [1] and filtering of both out-of-band and in-band signals based on their direction of arrival [2]. The weighted signal combining required for beamforming can be performed either in the analog [3], [4] or digital [5], [6], [7] domain, or partially in both using hybrid [8], [9] structures. Digital beamforming benefits from the precision and spatial flexibility [10] of digital signal processing (DSP). However for receivers, doing the spatial filtering in DSP does not allow for in-band but out-of-beam blockers to be spatially filtered before digitization, leading to higher

dynamic range requirements for the analog-to-digital converter (ADC). In comparison, analog beamforming, where the spatial filtering is performed before the ADC, can protect the ADC from large blockers. Analog beamforming can therefore lead to better dynamic range performance for the whole receiver [8]. On the other hand, analog beamforming loses the spatial flexibility of digital beamforming. Hence, analog and digital beamforming are optimal choices in different scenarios.

Another trend in receivers, in addition to beamforming, are wider bandwidths. Several true-time-delay (TTD) beamformers, which overcome the fractional bandwidth limitation due to beam squint [11], [12], have been proposed recently [13], [14], [15], [16]. These share a TTD solution based on resampling, which is efficient in terms of power consumption, area and delay range in modern CMOS. The efficiency

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comes from the utilization of only switches, capacitors and clock tuning for creating the delays. The maximum delay in the resampling TTD is limited to the sample period, whereas large sampling frequencies (short sample period) are needed for high bandwidth analog beamforming. This delay range–bandwidth trade-off is overcome with parallel time-interleaved lower-sample-rate TTD branches.

In receivers targeting wide bandwidths, the ADC following the beamforming RF front-end is typically time-interleaved. In this work we present a receiver prototype in 22-nm CMOS where the time-interleaving in both the beamformer and the ADC are utilized to allow on-the-fly reconfiguration between analog and digital beamforming modes. In the analog beamforming mode the time-interleaved ADC cores are used together as a single fast converter providing a single beamformed output data stream. In the digital mode, each of the ADC cores receive a signal from a different antenna, enabling spatially flexible signal combining in DSP. The reconfigurability allows the receiver to choose the more suitable operating mode based on the signal environment. The reconfigurability between the modes is achieved by controlling the clocking of sampling in the RF front-end and does not require additional hardware on the signal path. The paper extends our work on TTD beamforming receivers [14], [17], [18] by introducing the digital beamforming mode reconfigurability.

In addition to demonstrating the beamforming mode reconfigurability, the proposed receiver integrates baseband TTD beamforming similar to [13] and [16] with a down-conversion mixer. This integrates the additional RF phase shifting required [13], [16] in baseband TTD beamforming to a single beamforming delay control circuit. The ADC sampling is also integrated to the delay setup. The ADC sampling clocks are re-used as the align-and-combine clocks of the TTD beamforming.

The analog beamforming mode’s RF frequency range is 1–6 GHz which is the highest published for a TTD beamformer that is implemented without area-consuming passive delay lines. In addition, the 2 GHz instantaneous beamformed bandwidth achieving 100% fractional BW at 2 GHz center frequency is the widest published.

The paper is organized as follows. Section II describes how the reconfigurable beamforming modes are implemented by disabling clocks in some of the signal branches. Section III describes the operation of the fabricated prototype receiver. Section IV presents measured results and compares the proposed solution to the state-of-the art. Finally, Section V concludes the paper.

## II. RECONFIGURABLE BEAMFORMING MODES WITH RESAMPLING TRUE-TIME-DELAYS

Fig. 1 (a) and (b) show block diagrams for generic true-time-delay analog and digital beamforming receivers, respectively. Analog TTD beamforming requires an analog domain delay element in each antenna path, as well as analog signal combining between the paths, which in this case are placed after

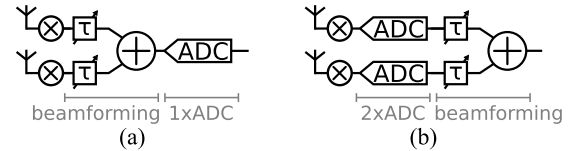


FIGURE 1. Illustrations of generic analog (a) and digital (b) beamforming for receivers with two antennas.

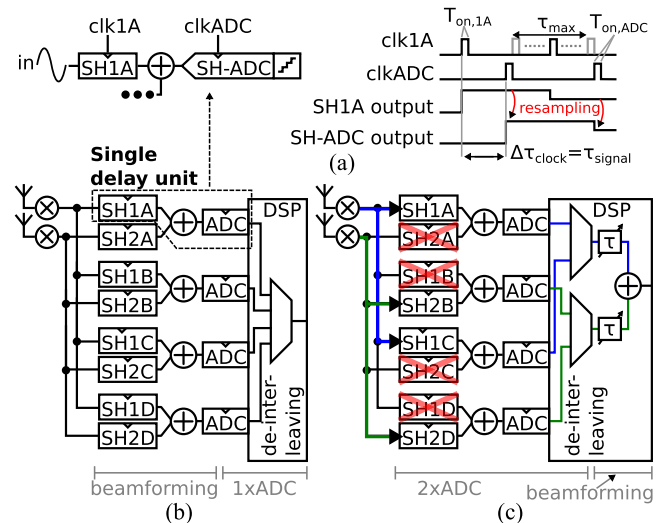


FIGURE 2. Illustration of the resampling delay concept and the related clock waveforms for a single path (a), and the reconfigurability of the proposed receiver between true-time-delay analog (b) and digital (c) beamforming modes.

the down-converting mixers. The beamforming section is followed by a single ADC. In digital beamforming, each antenna requires its own ADC, and the delays and the summing are implemented in DSP. In both cases the reception angle  $\theta$  is chosen with delays that cancel the antenna array propagation delays and result in constructive interference for signals from  $\theta$ . The required delay for antenna index  $i$  of a general size linear array is

$$\tau_i = \frac{(i - 1)d}{c} \sin(\theta), \quad (1)$$

where  $d$  is the antenna spacing and  $c$  is the speed of light [11].

The proposed receiver’s ability to reconfigure between true-time-delay analog and digital beamforming modes is illustrated in Fig. 2. The proposed analog beamforming mode shown in Fig. 2 (b) implements the generic true-time-delay beamforming of Fig. 1 (a), and the equivalence is highlighted by denoting the beamforming and digitization sections in both figures. Similarly, the proposed digital beamforming shown in Fig. 2 (c) implements the generic digital beamforming of Fig. 1 (b). The reconfigurability between the beamforming modes is enabled by having time-interleaving in both the true-time-delay beamforming setup and the ADC.

### A. RESAMPLING TRUE-TIME-DELAYS

The analog beamforming of the proposed receiver is built with resampling true-time-delay units which are based on

two consecutive samplers shown in Fig. 2 (a). The addition of the sampler SH1A in front of the ADC's input sampler SH-ADC allows delaying the input signal by controlling the two samplers' clocks relative to each other. The waveforms on the right side of Fig. 2 (a) show the outputs of the samplers SH1A and SH-ADC and their sampling clock signals,  $\text{clk1A}$  and  $\text{clkADC}$  respectively. The resampling, carried out with the second sampler SH-ADC and shown with the red arrows, results in the waveform 'SH-ADC output' which is a delayed but identical version of the waveform 'SH1A output'. The delay is controlled by the adjustable delay  $\Delta\tau_{\text{clock}}$  between  $\text{clk1A}$  and  $\text{clkADC}$ . The consecutive samplers thus map an easily implementable tunable delay  $\Delta\tau_{\text{clock}}$  between their clock signals to a delay  $\tau_{\text{signal}}$  for the analog input signal. The signal summing between different antennas is performed before SH-ADC which allows sharing the resampling between the antennas. The summation point is shown in Fig. 2 (a). In the proposed receiver the ADC is integrated into the delay setup by using its sampler for the resampling. Further details of the resampling delay can be found for example from [17].

The block diagram of the analog beamforming of the proposed receiver, shown in Fig. 2 (b), includes four time-interleaved delay units of Fig. 2 (a). The time-interleaving is applied because the maximum delay with a single delay unit is limited to

$$\tau_{\text{max}} = 1/F_{s,\text{unit}} - T_{\text{on,ADC}} - T_{\text{on,SH1A}}, \quad (2)$$

where  $F_{s,\text{unit}}$  is the sample rate in a single branch's delay unit and  $T_{\text{on,ADC}}$  and  $T_{\text{on,SH1A}}$  are the lengths of the sampling clocks of SH-ADC and SH1A, respectively. The beamforming delay tuning range, which is limited to  $\tau_{\text{max}}$ , is illustrated in Fig. 2 (a) on top of the waveform  $\text{clk1A}$  with the grey clock pulses showing the extremes to where  $\text{clk1A}$  can be tuned without overlapping with  $\text{clkADC}$ .

Dividing the delayed sampling to four lower- $F_{s,\text{unit}}$  time-interleaved branches increases the beamforming delay tuning range in each branch without reducing the combined  $F_s$  and therefore bandwidth. The branches A to D in Fig. 2 (b) operate at one quarter of the system sample rate  $F_s = 2$  GHz, and they are sampled with increasing time-interleaving delay-offsets of  $1/F_s$ . With the four-way time-interleaving the prototype achieves a maximum delay of of 1.375s. With an antenna spacing of half of the center frequency wavelength, this maximum delay is long enough for a linear antenna array of seven elements at the lowest operating center frequency of 2 GHz. At higher center frequencies larger arrays are possible as the antenna spacing and therefore the required delays decrease in proportion to the frequency. This prototype implements two antenna inputs for demonstrating the reconfigurability between analog and digital beamforming modes.

The analog true-time-delay beamforming is achieved in each branch A to D by sampling the mixer output signals of the two antenna paths with delays according to (1). The time-interleaved delay branches are connected to different ADC cores of the full time-interleaved ADC as shown in Fig. 2 (b).

The samples from the different antennas are summed and then re-sampled with the ADC cores to complete the true-time-delay beamforming. After quantization each core, their outputs are de-interleaved, resulting in a single data stream. The clock waveforms for the complete receiver are illustrated and explained in Section III-A.

## B. RECONFIGURABLE BEAMFORMING MODES

Instead of using the analog true-time-delay beamforming mode of Fig. 2 (b), the receiver can be re-configured to a digital beamforming mode presented in Fig. 2 (c). To implement the digital beamforming of Fig. 1 (b) the ADC cores are divided between the antennas such that each antenna has its own ADC. The reconfiguration is implemented by selectively disabling signal paths inside the time-interleaved branches, as shown in Fig. 2 (c) with the red crosses. The remaining signal paths from the two different antennas to the two separately digitized data streams are illustrated in with blue and green. The two data streams allow beamforming in the digital domain with the added spatial flexibility [10]. The number of antenna inputs for digital beamforming  $k$  is limited by  $k_{\text{max}} = \min(\text{TTD TI factor}, \text{ADC TI factor})$ . The digital beamforming mode operates with  $1/k$  of the bandwidth of the analog mode, due to splitting the time-interleaved ADC. The mode re-configurability does not require anything in the signal path as the required signal paths are disabled by only re-configuring the clocking scheme.

## III. PROTOTYPE RECEIVER

The proposed beamforming mode reconfigurability was verified with a prototype receiver. In addition to the reconfigurability, the prototype combines the baseband resampling TTD functionality with an RF phase shift. The RF phase shift is required [13], [16] for correct beamforming when implementing TTDs in baseband. The RF phase shift is implemented by delaying local oscillator (LO) signal. The LO delay is controlled with the same circuit as the true-time-delay control, simplifying the synchronization of the baseband TTD and the RF phase shift. Further integration is achieved by implementing the resampling function of the TTD beamforming with the ADC sampling capacitor.

### A. CIRCUIT OVERVIEW

Fig. 3 shows the block diagram of the receiver. The receiver includes two antenna paths with time-interleaved samplers for implementing the true-time-delay beamforming, a baseband summing amplifier and an eight-way time-interleaved ADC. In both of the two antenna paths the signal is first amplified by a resistive feed-back low gain amplifiers, which were selected to allow demonstration of the wideband beamforming. After the amplifier, the signal is down-converted by a passive IQ sampling mixers with a capacitive output load. The figure only shows the receiver I branch but the Q branch is identical from the mixer onwards. The mixer output signal is sampled with the time-interleaved TTD switches  $iA$  to  $iD$ , where  $i$  is the antenna index. This sampling is carried out

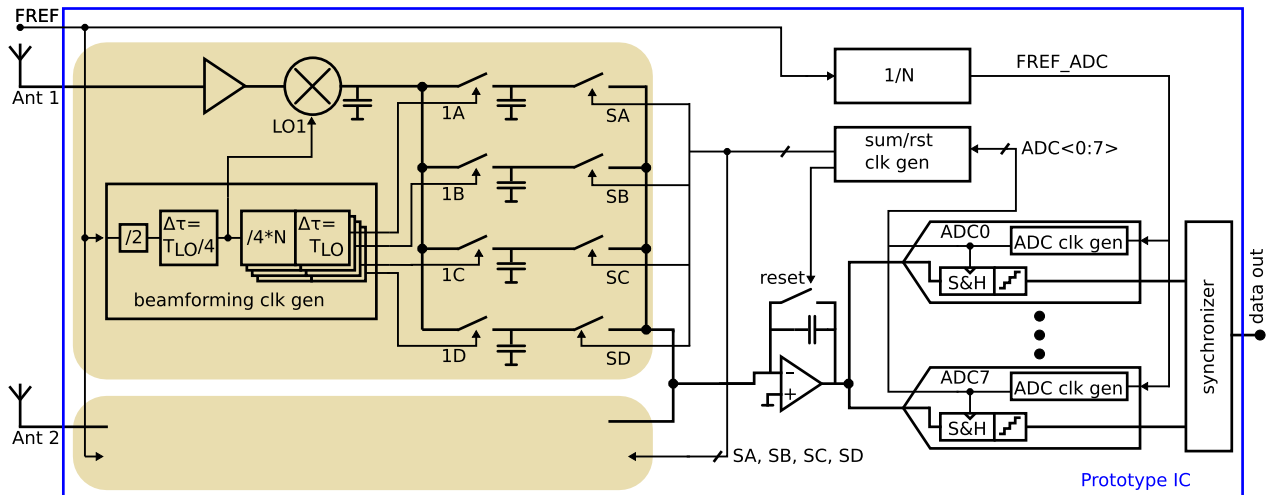


FIGURE 3. Block diagram of the proposed beamforming receiver (single-ended simplification, Q branch not shown).

while the mixer switches are in the OFF state and with a delay according to (1). The mixer and the switches  $iA$  to  $iD$  are both controlled by beamforming clock signal generators in each antenna path.

The signals from the beamforming sampling are transferred to the ADC cores through a capacitive feed-back amplifier that is time-shared between the branches. The samples are propagated consecutively from each branch to the ADC cores designated for the branches using the switches SA to SD. The clocks SA to SD are simultaneous with the sampling clocks of the ADC cores, and the samples are propagated to the ADC sampling capacitors directly during these pulses. Since the beamforming front-end is four times time-interleaved and the ADC eight times, each of the beamforming branches is connected to two ADC cores.

### B. ANALOG MODE

In the analog beamforming mode all time-interleaved sampling branches A to D are active in both antenna paths. The analog mode sampling clocks are shown in Fig. 4 (a). Each antenna has four sampling clocks  $iA$  to  $iD$ , one for each branch. The clocks control the corresponding switches shown of Fig. 3. The four clocks of each antenna are offset from each other by the period of the combined sample rate  $T_s = 1/F_s$  to achieve the time-interleaving. Antenna 1 is selected as the delay reference for beamforming, and the sets-of-four sampling clocks for the other antenna are delayed by  $\tau_i$  according to (1). To achieve the RF phase shift needed for baseband TTD operation, the LO signals are delayed as well. A correct phase shift is achieved with the same delays of (1). However, since the LO is periodic about  $T_{LO}$ , it is sufficient to delay it by only  $\tau_{wrap} = \text{mod}(\tau, T_{LO})$ .

To complete the TTD operation, samples from each antenna path are synchronized and summed with the clocks SA..SD shown in Fig. 4 (c). These clocks control the corresponding switches in Fig. 3. The summing at the input of

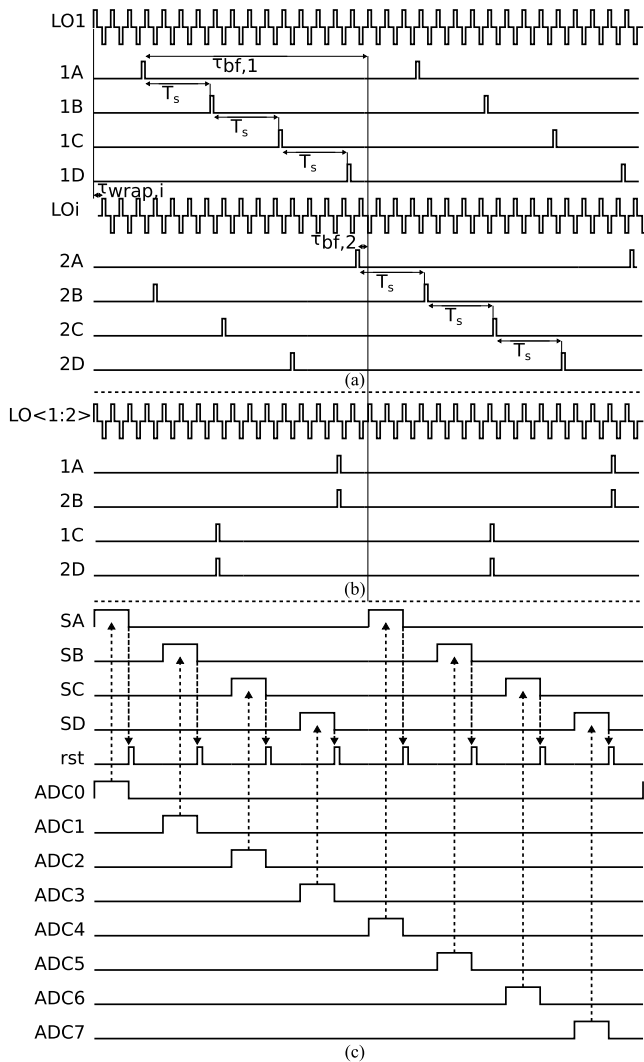
the first baseband amplifier achieves full signal combining in the analog domain. The summation clocks SA..SD are created with OR gates from the ADC sampling clocks ADC0 to ADC7 such that SA is ADC0 OR ADC4, SB is ADC1 OR ADC5 and so on. During the sum clocks, the voltages from corresponding sampling capacitors are summed at the input of the first baseband amplifier and transferred to the input capacitor of one ADC core. After each sample is transferred to an ADC, the baseband amplifiers are reset, and the eight ADC cores form a single time-interleaved ADC. These reset clocks (rst) are generated from the falling edges of the summation clocks, as shown in Fig. 4 (c), with a flip flop and a delay line.

### C. DIGITAL MODE

Digital beamforming is achieved by separating the ADC cores such that each antenna its exclusive cores. With eight ADC cores, each of the two antennas is assigned four ADC cores. Two of the four time-interleaved TTD sampling branches is active for each antenna: branches A and C for antenna 1, and B and D for antenna 2. Fig. 4 (b) shows the sampling clocks for the digital mode. The delay control is used such that all antennas are initially sampled at the same time to avoid having to delay-align the received signals in DSP. The simultaneous sampling is achieved with sampling delays of  $\tau_i = (i - 1)/F_s$ , which make 1A and 2B as well as 1C and 2D simultaneous. The inactive branches for each antenna have their respective sum clocks disabled, and the LO signals in each antenna path have identical timing. Now, the signals received by each antenna are propagated only to its assigned ADC cores. After A/D conversion the weighted signal combining for digital beamforming is performed in post-processing.

### D. BEAMFORMING CLOCK GENERATOR

The beamforming is controlled with a separate clock generator in each antenna path. The generator, shown in Fig. 5,



**FIGURE 4.** Receiver LO and clock waveforms: Analog (a) and digital (b) beamforming modes, and the summation, and ADC clocks used in both modes (c). Inactive clocks for the digital mode not shown.

creates the delayed LO and time-interleaved sampling clocks of Fig. 4 from a frequency reference (FREF) at twice the LO frequency. As shown in Fig. 3, FREF is also used in the ADC, which keeps the beamforming sampling and the ADC clocks that control the resampling synchronized.

The frequency reference is first used to clock the LO divider to create four-quadrant non-overlapping 25 percent duty-cycle LO clocks for I/Q down-conversion. Delay tuning in steps of  $0.25 T_{LO}$  is implemented by changing the order of the LO divider outputs with four MUXes. This delay controls the LO delay as well as the sampling clocks by  $\tau_{wrap}$ , thus keeping the baseband TTD beamforming delay and the RF phase shift synced to the selected reception angle. More precise delay fine-tuning is not included in this prototype, but could be implemented by adding a delay line in front of the LO divider, as was demonstrated in [14].

One of the four LO phases is selected to clock a chain of 16 D flip-flops (DFF). Predetermined nodes of the DFF

chain output four equally spaced pulses at  $f = f_{LO}/N$  for the time-interleaved sampling clocks  $iA..iD$  of Fig. 4 (a). This prototype supports division ratios  $N=1,2$  or 4 between  $F_{LO}$  and the baseband sampling rate  $F_s$ . Different  $N$  are handled by setting every  $4N$ th node of the DFF chain high during initialization. Additionally, the output nodes used change such that the pulses are taken from every  $4/N$ th node. With these two settings one of the selected output nodes is high every  $N$ th LO cycle. Delay steps of  $T_{LO}$  are implemented by moving the position of the nodes set high during initialization along the DFF chain. The  $T_{LO}$  delay steps together with  $\tau_{wrap}$  cover the full beamforming delay tuning range of 1.375 ns.

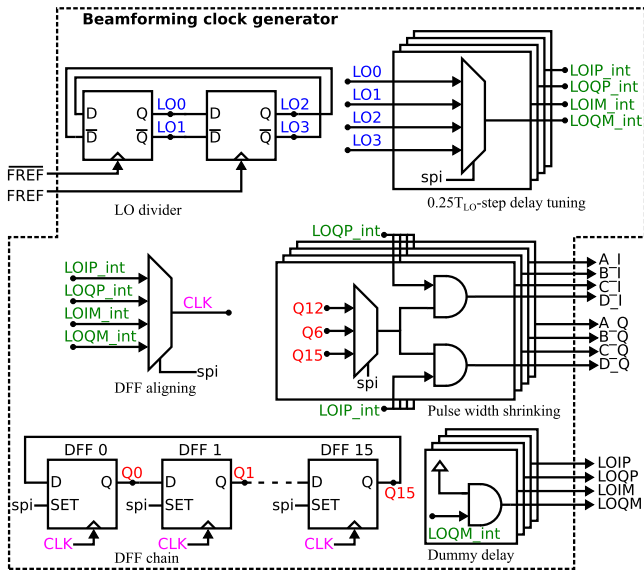
The pulses at the DFF chain output nodes have a pulse width equal to the period of the flip-flops' clock, i.e.  $T_{LO}$ . To make the sampling clocks non-overlapping with the LO driving the mixer, as shown in Fig. 6 (a), the sampling clock's pulse width must also be  $0.25 T_{LO}$ . Pulse width shrinking for creating the  $0.25 T_{LO}$  sampling clocks is achieved with an AND operation. The sampling clocks for the I branch are created by ANDing with a Q branch LO phase, as shown in Fig. 6 (b), and vice versa. The selection of which LO phase clocks the DFF chain depends on frequency of FREF and is completed with the DFF aligning MUX. The selection is performed to align the DFF chain outputs with the LO phase for the AND operation such that they overlap fully and create single sampling pulse. The LO phases are passed through a dummy AND gate before the mixer to align them with the sampling clocks.

The clock generator is suited for modern CMOS processes. In this prototype chip the generator excluding the LO divider was constructed with standard cells, which simplifies re-design effort. The functions of delay tuning for LO and sampling clocks, and, creation of the 4 time-interleaved sampling clocks for both I and Q branches take up only  $15.5 \mu\text{m} \times 25 \mu\text{m}$  of area. The area includes also a clock tree, buffering and decoupling capacitance.

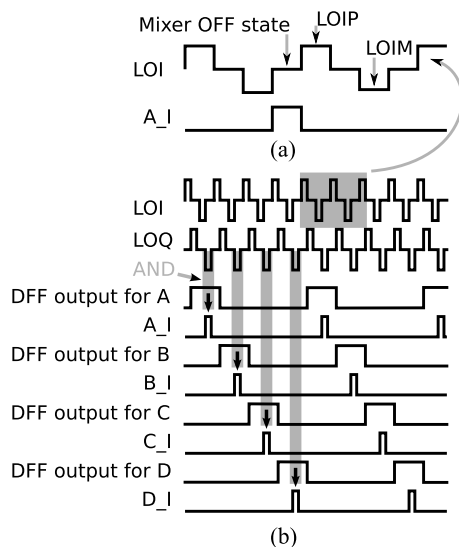
### E. ANALOG-TO-DIGITAL CONVERTER

The prototype receiver contains a successive approximation register (SAR) ADC that digitizes the received signal. The samples taken from different antennas are passed to the ADC by the summing amplifier as shown in Fig. 3. In the analog beamforming mode, the samples are first combined to form a beam and then fed to an 8-way time-interleaved ADC. In the digital beamforming mode, the samples from the two antennas are digitized separately by two 4-way time-interleaved ADCs resulting in two separate data streams for beamforming. The ADC is followed by parallel RAM memory blocks where the data can be written and subsequently read from at a lower speed to perform digital beamforming with postprocessing.

Fig. 7 shows the block diagram of the implemented 9-bit SAR ADC. The ADC consists of eight cores, each being used at up to 50 MS/s sample rate, thus giving a maximum time-interleaved sample rate of 400 MS/s. One ADC core consists of a split-array [19] capacitive digital-to-analog converter

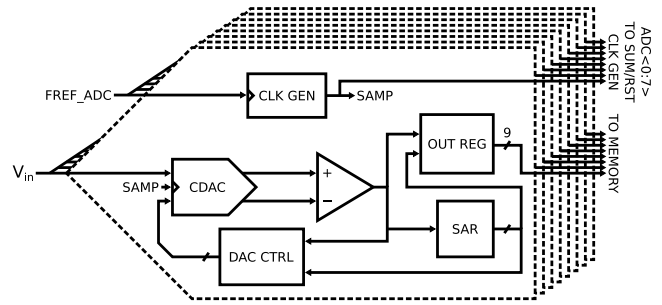


**FIGURE 5.** Beamforming clock generator for creating and delay controlling the four LO phases and the time-interleaved sampling clocks. Connected nodes are color matched for clarity.



**FIGURE 6.** Non-overlapping LO phases and sampling clock (a) and the creation of the narrow sampling clocks by ANDing the flip-flop chain outputs with an LO phase of the Q branch (b).

(CDAC), a StrongARM comparator [20] and synthesized SAR, clock generator and control logic. The CDAC takes a sample from the front-end’s summing amplifier and stores it in a capacitor array inside the CDAC. During the conversion stage, following the sampling, the CDAC consecutively outputs 9 values for the comparator for resolving the quantization result bits. The CDAC output value is controlled by logic that determines the capacitor array connections for each bit. The CDAC control logic has inputs from both the comparator and the SAR due to utilization of overlapping conversion steps for increasing the sample rate [21]. After all nine bits are converted, the result is saved to an output register. The output



**FIGURE 7.** Block diagram of the included 8-way time-interleaved SAR ADC.

register output stays constant during the next conversion allowing output data of all 8 ADC cores to be synchronized to a single 50 MHz clock before writing to memory.

The ADC is controlled by a clock generator in each ADC core, shown in Fig. 8. The clock generator takes in a clock FREF\_ADC, which is derived from the common reference clock of the chip as shown in Fig. 3. FREF\_ADC clocks a synchronous 4-bit counter that is initialized to a specified 4-bit value for creating timing offsets between the time-interleaved ADC cores. To get the timing as shown in Fig. 4 (c) the initial values are set two apart, i.e. 14 for ADC0, 12 for ADC1, 10 for ADC2 and so on using the VALUE nodes. The sampling clock is generated by checking if the counter value is zero with the logic shown on the upper right side of Fig. 8. This will produce a clock signal whose duty cycle is 1/16 and frequency one 16th of FREF\_ADC. The resulting signal is buffered with a DFF to avoid glitches and get more accurate timing for the sampling clock. The sampling clock is given to the CDAC to control the ADC sampling, as well as to the front-end, along with sampling clocks of the other cores, to generate the summing clocks SA to SD of Fig. 4 (c). In addition to the sampling clock, the counter phases are used to derive a clock for the comparator and control the SAR. The schematic shown in Fig. 8 is a simplified version of the synthesized clock generator. While the ADC core digitization operates at 50 MS/s, the clock generation can be run at a higher frequency which allows the analog RF front-end beamforming to operate at a total of 2 GHz sample rate.

**IV. MEASUREMENT RESULTS**

The proposed receiver was fabricated in 22-nm FD-SOI CMOS. Dimensions of the chip are 1.25 mm × 2.5 mm. The chip micrograph is shown in Fig. 9 with relevant parts of the circuit highlighted. The IC is directly bonded to a PCB. The automated measurement environment controls various sources and an FPGA controlling the digital interfaces.

The true-time-delay analog domain beamforming is demonstrated in Fig. 10. Due to the lower bandwidth of the ADC, the analog domain beamforming measurements were executed through a test output before the ADC input. The result shows squint-free beamforming towards a target angle of 30 degrees. The reception center frequency is 2 GHz and

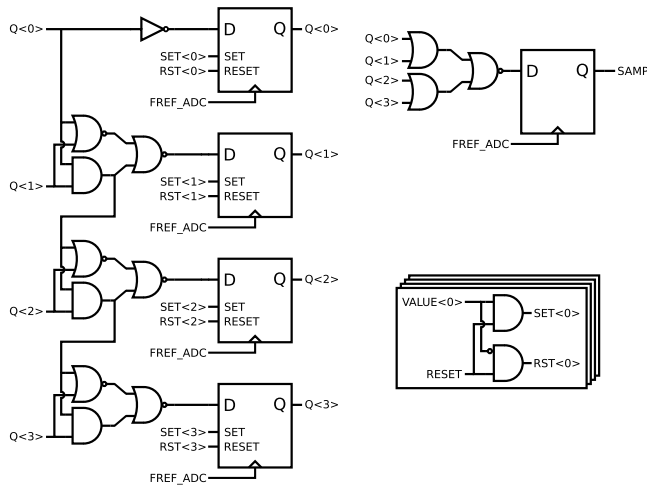


FIGURE 8. Single ADC sampling clock generation.

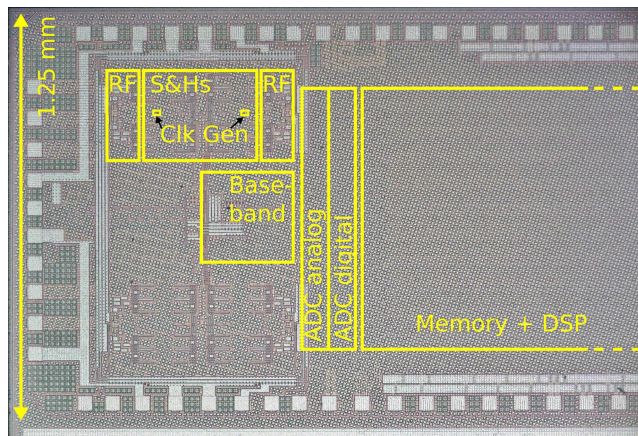


FIGURE 9. Chip micrograph.

the instantaneous bandwidth is 2 GHz as well resulting in a 100% fractional bandwidth. The solid lines show the measured array factor at different frequencies inside the instantaneous bandwidth. Comparison to the dashed lines showing ideal simulated array factors show a good match between measurements and simulations.

The parallel time-interleaved TTD sampling branches are used to enable delays exceeding period of the total system sample rate  $1/F_s = 1/2 \text{ GHz} = 0.5 \text{ ns}$ . This delay extension is demonstrated in Fig. 11. To demonstrate long delays with only two antennas, the antenna inputs are chosen to represent the outermost elements in an 8-antenna linear array, with an element spacing of half wavelength at a center frequency of 4 GHz. This antenna setup together with the chosen target angle of 59 degrees results in 0.75 ns of required delay. The directivity is towards the target angle across the instantaneous bandwidth of 2 GHz and matches the ideal simulated results shown with the dashed lines. Fig. 12 shows the gain variation for a single antenna when the beamforming delay is swept between 0 and 1.375 ns. The gain variation is within 3.8 dB

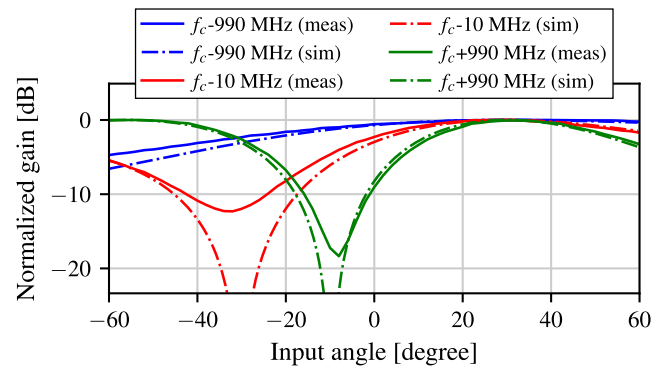


FIGURE 10. Analog true-time-delay beamforming with 2 GHz center frequency: squint free directivity towards 30 degrees across a 100% fractional bandwidth. The curves show parts of the instantaneous bandwidth at different offsets from the center frequency. Measurements compared to ideal simulations.

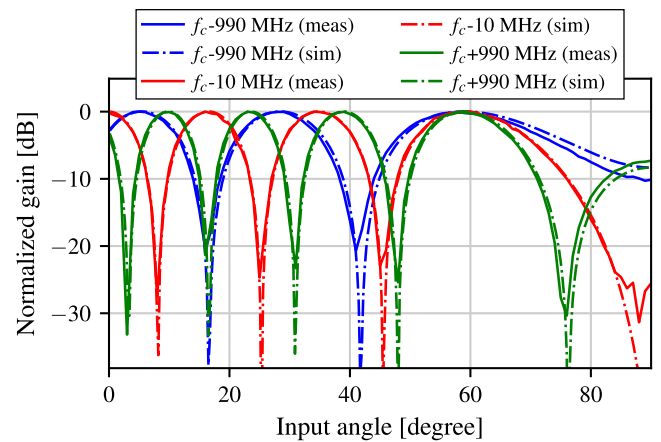


FIGURE 11. Demonstration of analog TTD beamforming with delays exceeding the period of the system sample rate. The target direction is 59 degrees, and the curves show parts of the instantaneous bandwidth at different offsets from the center frequency. Measurements compared to ideal simulations. The grating lobes are a result of the large element spacing chosen to demonstrate a beamforming delay of 0.75 ns.

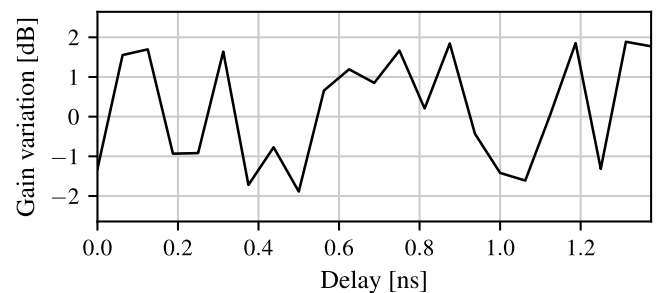


FIGURE 12. Measured gain variation over the beamforming delay range.

without calibration. These results verify the delay-extending function of the time-interleaved sampling paths.

The digital beamforming functionality is demonstrated in Fig. 13. It shows three spatial beam patterns created from a single set of measured data at 1.6 GHz reception frequency. The beams are formed in post-processing by applying different weights, for each of the three target angles,

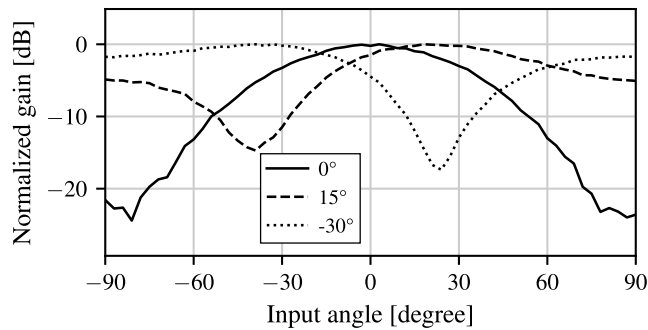


FIGURE 13. Measured digital beamforming: three simultaneous beam patterns with different target directions formed in post-processing from the same set of data streams.

TABLE 1. Comparison to state-of-the-art analog TTD Beamformers.

	TCAS-I 2019 [13]	SSC-L 2020 [14]	ISSCC 2020 [24]	JSSC 2022 [16]	This work
Delay domain	BB	RF	BB	BB	BB <sup>1</sup>
# of elements	4	2	4	4	2
Supports digital beamforming	No	No	No	No	Yes
Delay range (ns)	15	0.750–5	1	3.8	1.38
Frequency range (GHz)	N/A	0.6–4	N/A	N/A <sup>2</sup>	1–6
BW (MHz)	100	800	500	800	2000
Power (mW)	52	70	40	29	146
Area (mm <sup>2</sup> )	0.57	0.13	0.31	1.98 (chip)	0.41
Technology (nm)	65	28	65	65	22

<sup>1</sup> Required RF phase shift is delay-synced to the baseband TTD.

<sup>2</sup> Emulated off-chip down-conversion from 28 GHz.

to the measured data. In addition to the angle dependent weights, there are also gain and phase offset calibration weights for each ADC’s data. The calibration weights are static and not changed for the three demonstrated beams. Due to layout related issues in the reset switch of Fig. 3, the resetting between samples from separate antennas was performed externally in the digital beamforming mode. The result proves the functionality of switching between the analog and digital beamforming modes by only changing the clocking, as explained in Section III.

Table 1 compares the analog beamforming mode of the prototype receiver to the state-of-the-art analog domain TTD beamforming solutions for receivers. The proposed receiver is the only one supporting both analog and digital beamforming. The receiver reaches the highest frequency range of 1–6 GHz in this comparison which omits TTDs based on passive delay lines, such as [22] and [23], due to their more than an order of magnitude worse delay range/area. Gain variation of the receiver over the frequency range, measured with a constant offset from the LO, is shown in Fig. 14. The instantaneous beamformed bandwidth is 2 GHz achieving a 100% fractional bandwidth at the low end of the frequency range as demonstrated in Fig. 10. In summary, the ability

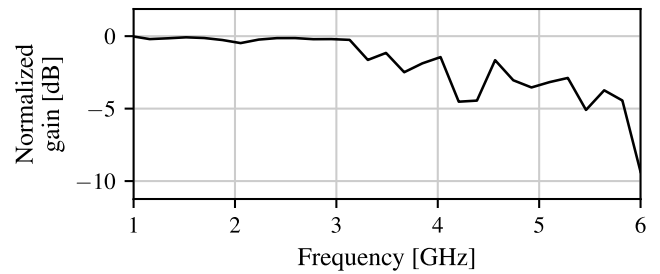


FIGURE 14. Single RF channel gain variation over the frequency range.

to support the digital beamforming mode does not limit the analog beamforming capability.

### V. CONCLUSION

This paper presents a receiver prototype that enables reconfiguration between analog and digital beamforming modes to better deal with different operating scenarios. The analog beamforming is implemented with resampling based true-time-delays that avoid the beam squint problem and thus allow wide bandwidths. Measurements with the prototype demonstrate beamforming with a state-of-the-art 2 GHz instantaneous bandwidth reaching up to 100% fractional bandwidth. The frequency range of the receiver is 1–6 GHz. The reconfigurability between analog and digital beamforming modes is demonstrated with measurements.

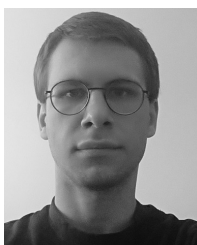
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