

# Circuit Configuration of a Sensoreless Multilevel Inverter with Voltage Multiplying Ability

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**Abstract**— This paper proposes a novel circuit configuration for multilevel inverters based on the switched-capacitor concept. This topology is suitable for integrating renewable energy sources into the utility grid due to its versatile voltage boosting capability. Simple Nearest Level Modulation (NLM) technique is used to control the newly proposed inverter topology. Requiring a single DC source and a reduced number of semiconductor devices are the main advantages of the proposed circuit structure. Furthermore, inherent voltage balancing of the capacitors and simple control process with neither a need for any external controllers nor sensors are other operational benefits of the presented topology. The performance of the 9-Level inverter is validated through a simulation model and experimental setup.

**Keywords**— Multi-Level Inverter, switched-capacitor, Nearest Level Modulation, Single Source Converter, Boost

## I. INTRODUCTION

Power electronics converters play an important role to promote the integration of intermittent and unregulated DC voltage renewable energy resources such as wind and photovoltaic systems to AC grid [1]. Although simple two-level and three-level topologies have been preferred converter structure, the deployment of Multi-Level Inverters (MLIs) in residential and industrial applications is significantly increased, during recent years [2]. MLIs have several advantages over classic two and three-level structures [3], [4]. They can produce the desired output waveform by synthesizing the DC sources' voltages to form each intended level through proper arrangement of semiconductor switches [5]. Accordingly, the researchers aim to reach a high number of output voltage levels with regard to reducing the number of components. As the number of levels increases, the resolution of the output voltage waveform increases. Hence, the harmonic content of the output voltage can effectively be decreased [6], [7]. Whereas, in classic MLIs, raising the number of voltage levels would cause a rise in the number of circuit devices, increasing the power loss and jeopardizing the reliability of the converter. Classic MLIs include circuits based on Neutral Point Clamped (NPC), Cascaded H-Bridge (CHB), Flying Capacitors (FC), and any hybrid combination of them [8].

To overcome these step-up inverting limitations, Switched-Capacitor MLI (SC-MLI) topologies were introduced. Unlike classic NPC MLIs suffering from

capacitors' voltages imbalance issue, SC-MLIs take advantage from capacitors' self-voltage-balancing capability. Besides, different from Classic CHB MLI topologies which need several DC sources in their topology, SC-MLIs can boost the input voltage by using a single DC source. They employ capacitors to produce different output voltage levels which are charged either by the input DC source or by a combination of other capacitors in every cycles (capacitors charge and discharge through each other) [3], [9].

So far, the majority of articles in this literature concentrated on vanguard topology design. Particularly, to reduce the circuit components accompanied by more output levels and simple control [10], [11]. In this context, [5], [6] and [9] have introduced nine-level inverters with fewer elements, supplied by a single DC source. Similarly, the authors in [12] and [13] proposed topologies fed by two separate DC sources. Moreover, [14] and [15] have designed converters by paying attention to the arrangement of semiconductors concerning their blocking voltages.

This research paper aims to propose a novel single-source nine-level SC-MLI suitable for medium power and voltage application. Generating negative voltage levels without any auxiliary circuit along with the pioneer configuration design reduces the blocking voltages of the power switches sufficiently. Simple control strategy eases the implementation and operation of the proposed topology which is its other privilege.

To present the characteristics of the proposed single source SC-MLI, this manuscript is organized as follows: section II is devoted to the suggested converter and its operating principles. Then, the design procedure as well as theoretical analyses are brought in section III. Also, different operational factors of the proposed topology are compared with similar single-source ones in this section. Afterwards, the performance of the proposed 9L-SCMLI is assessed via both simulation and experimentation in Section IV. Finally, the paper is concluded in section V.

## II. TOPOLOGY DESCRIPTION

The overview of the proposed nine level Switched-Capacitor inverter (9L-SCI) is illustrated in Fig. 1. This structure comprises of 11 uni-directional power switches, 2 bi-directional ones, and 13 gate driver circuits. It is also utilizing a single DC source and four capacitors to generate output voltage levels. This converter boosts the input voltage four times and generates a bipolar output voltage without using an

H-Bridge module. This factor helps the switches not to withstand the whole output voltage and reduces their blocking voltage as well. Therefore, the 9L-SCI demanding in application with low input voltage would increase. To reach this goal, the selected switching states of 9L-SCI are brought in Table I. Also, corresponding paths of the mentioned switching states as well as the charging (C) and discharging (D) paths of the capacitors are then depicted in Fig. 2.

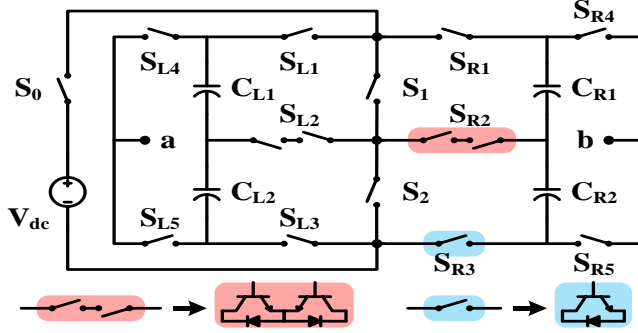


Fig. 1. The proposed 9L-SCI

TABLE I. SELECTED SWITCHING STATES OF 9L-SCI

Level	Active Switches	C <sub>L1</sub>	C <sub>L2</sub>	C <sub>R1</sub>	C <sub>R2</sub>
0	S <sub>L4</sub> , S <sub>L2</sub> , S <sub>L1</sub> , S <sub>0</sub> , S <sub>2</sub> , S <sub>R1</sub> , S <sub>R2</sub> , S <sub>R4</sub>	C	-	C	-
	S <sub>L5</sub> , S <sub>L3</sub> , S <sub>L2</sub> , S <sub>0</sub> , S <sub>1</sub> , S <sub>R2</sub> , S <sub>R3</sub> , S <sub>R5</sub>	-	C	-	C
+1 V <sub>dc</sub>	S <sub>L4</sub> , S <sub>L2</sub> , S <sub>L1</sub> , S <sub>0</sub> , S <sub>2</sub> , S <sub>R3</sub> , S <sub>R5</sub>	C	-	-	-
	S <sub>L4</sub> , S <sub>L1</sub> , S <sub>0</sub> , S <sub>1</sub> , S <sub>R2</sub> , S <sub>R3</sub> , S <sub>R5</sub>	-	-	-	C
+2 V <sub>dc</sub>	S <sub>L4</sub> , S <sub>L3</sub> , S <sub>L2</sub> , S <sub>0</sub> , S <sub>1</sub> , S <sub>R2</sub> , S <sub>R3</sub> , S <sub>R5</sub>	D	C	-	C
	S <sub>L4</sub> , S <sub>L2</sub> , S <sub>L1</sub> , S <sub>0</sub> , S <sub>2</sub> , S <sub>R1</sub> , S <sub>R2</sub> , S <sub>R5</sub>	C	-	C	D
+3 V <sub>dc</sub>	S <sub>L4</sub> , S <sub>L3</sub> , S <sub>0</sub> , S <sub>2</sub> , S <sub>1</sub> , S <sub>R2</sub> , S <sub>R5</sub>	D	D	C	D
+4 V <sub>dc</sub>	S <sub>L4</sub> , S <sub>L3</sub> , S <sub>1</sub> , S <sub>2</sub> , S <sub>R1</sub> , S <sub>R5</sub>	D	D	D	D
-4 V <sub>dc</sub>	S <sub>L5</sub> , S <sub>L1</sub> , S <sub>1</sub> , S <sub>2</sub> , S <sub>R3</sub> , S <sub>R4</sub>	D	D	D	D
-3 V <sub>dc</sub>	S <sub>L5</sub> , S <sub>L2</sub> , S <sub>L1</sub> , S <sub>0</sub> , S <sub>2</sub> , S <sub>R3</sub> , S <sub>R4</sub>	C	D	D	D
-2 V <sub>dc</sub>	S <sub>L5</sub> , S <sub>L3</sub> , S <sub>L2</sub> , S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub> , S <sub>R3</sub> , S <sub>R4</sub>	-	C	D	C
	S <sub>L5</sub> , S <sub>L2</sub> , S <sub>L1</sub> , S <sub>0</sub> , S <sub>2</sub> , S <sub>1</sub> , S <sub>R2</sub> , S <sub>R4</sub>	C	D	C	-
-1 V <sub>dc</sub>	S <sub>L5</sub> , S <sub>L3</sub> , S <sub>L2</sub> , S <sub>0</sub> , S <sub>1</sub> , S <sub>R1</sub> , S <sub>R4</sub>	-	C	-	-
	S <sub>L5</sub> , S <sub>L3</sub> , S <sub>0</sub> , S <sub>2</sub> , S <sub>R1</sub> , S <sub>R2</sub> , S <sub>R4</sub>	-	-	C	-

The Nearest Level Modulation Technique (NLM) is used to control the operation of the 9L-SCI. This modulation makes the appropriate nearest voltage ( $V_{nl}$ ) levels to follow the reference ( $V_{ref}$ ) in an offline mode. Initially,  $V_{nl}$  is calculated by equation (1) and then the related time intervals and appropriate switching angle  $T_i$  ( $i = 1, 2, 3, 4$ ) for each level are determined. The process of NLM utilization in 9L-SCI is illustrated in Fig. 3.

$$V_{nl} = \frac{1}{V_{dc}} \text{round}(V_{ref}) \quad (1)$$

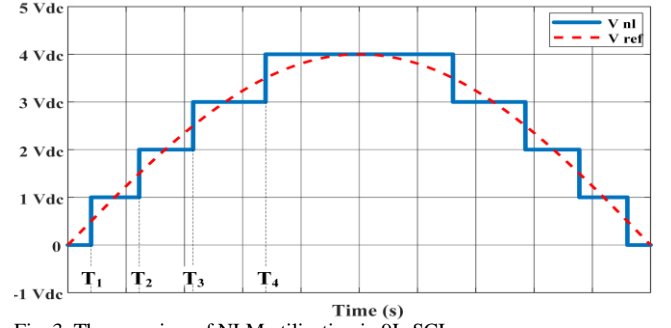


Fig. 3. The overview of NLM utilization in 9L-SCI.

### III. DESIGN CONSIDERATIONS AND MATHEMATICAL ANALYSES

The process of designing an SC-MLI including calculation of required circuit capacitances, power loss studies, and efficiency analysis are discussed in this section. Moreover, the literature of the single source 9L-SCI is reviewed and a thorough comparative study with the proposed one is included as well.

#### A. Circuit Capacitance Determination

The output voltage in SC-MLIs is generated by the help of the voltages of the capacitors. To shape the desired output voltage, the voltages of the capacitors has to be maintained in a certain acceptable range, as their voltages drop due to frequent charging and discharging [3]. By proper control over the voltage drop during charging and discharging procedures, the self-voltage-balancing ability of the circuit capacitors is ensured. The voltage drop mainly depends on the capacitance ( $C$ ), load current ( $I_{out}$ ), output frequency ( $f_{ref}$ ), and the length of the discharging time interval ( $t_s, t_f$ ). Accordingly, it is vital to specify the exact range of required capacitances. The first step is to specify the maximum charge drawn from the circuit capacitors ( $\Delta Q_{max}$ ) which is calculated by (2).

$$\Delta Q_{max} = \int_{t_s}^{t_f} I_{out} \sin(2\pi f_{ref} t) dt \quad (2)$$

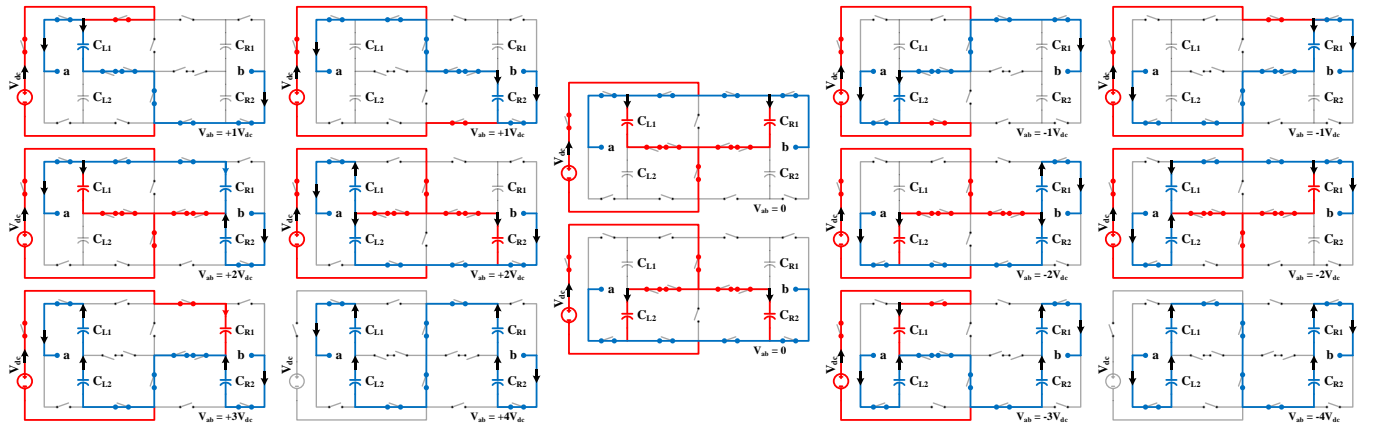


Fig. 2. The capacitors' charging and discharging current paths of the proposed 9L-SCI to produce each voltage level.

As the capacitors feed the load in series and regarding their similar capacitances, the equivalent capacitance ( $C_{eq}$ ) is a quarter of each one. Also, the charge variation determined by (2) occurs to all of the circuit capacitors identically. Considering the worst case scenario of supplying a pure resistive load with maximum  $K$  % voltage drop, and the sum of all capacitors' voltages as  $V_{eq}$ , the equivalent capacitance can be derived from:

$$C_{eq} \geq \frac{\Delta Q_{max}}{K \cdot V_{eq}} \quad (3)$$

Accordingly, the changes in load and the tolerance of voltage drop would result in variation of the required circuit capacitances to maintain the desired criteria. Fig. 4 shows the capacitance curve with regard to the load changes and different applicable values of  $K$  in the range of (5,10,15) %.

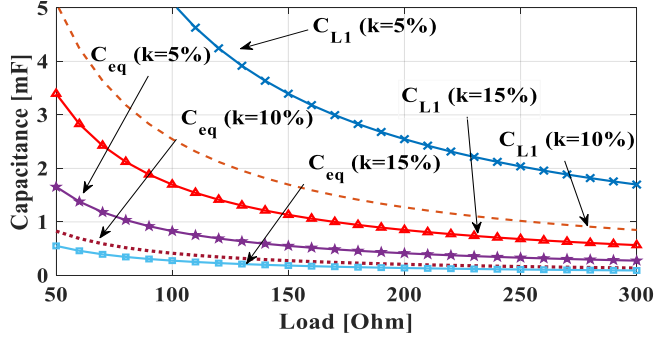


Fig. 4. The capacitance variations versus load changes

To prove the self-voltage balancing properties of the capacitors, the energy received from and delivered to each capacitor should be equal. To investigate this issue, initially, the energy flowing through the circuit ( $U$ ) should be calculated. Hence, by considering  $V_C$  as the capacitor's voltage, and  $Q$  as its charge, it yields:

$$dU = V_C \cdot dQ = V_C \cdot I_{out} \cdot dt \Rightarrow U = \int V_C \cdot I_{out} \cdot dt \quad (4)$$

Then, for the positive half cycle, the energy received by capacitor  $C$  can be achieved by:

$$\begin{aligned} U_C^+ &= \int_0^\pi V_m I_m \sin(\theta) d\theta \\ &= \int_0^{\alpha_{T1}} 0V_{dc} I_m \sin(\theta) d\theta + \int_{\alpha_{T1}}^{\alpha_{T2}} 1V_{dc} I_m \sin(\theta) d\theta \quad (5) \\ &+ \dots + \int_{\pi-\alpha_{T2}}^{\pi-\alpha_{T1}} 1V_{dc} I_m \sin(\theta) d\theta + \int_{\pi-\alpha_{T1}}^{\pi} 0V_{dc} I_m \sin(\theta) d\theta \end{aligned}$$

Identically, for the negative half cycle, with regard to the symmetrical switching times, the received energy is calculated by:

$$\begin{aligned} U_C^- &= \int_\pi^{2\pi} V_m I_m \sin(\theta) d\theta \\ &= \int_\pi^{\pi+\alpha_{T1}} 0V_{dc} I_m \sin(\theta) d\theta + \int_{\pi+\alpha_{T1}}^{\pi+\alpha_{T2}} -1V_{dc} I_m \sin(\theta) d\theta \quad (6) \\ &+ \dots + \int_{2\pi-\alpha_{T2}}^{2\pi-\alpha_{T1}} -1V_{dc} I_m \sin(\theta) d\theta + \int_{2\pi-\alpha_{T1}}^{2\pi} 0V_{dc} I_m \sin(\theta) d\theta \end{aligned}$$

Accordingly, by comparing the relations (5) and (6), it is concluded that:

$$U_C^+ = -U_C^- \quad (7)$$

Which means that the energy received from and delivered to each capacitor are equal during each operating cycle. Therefore, the voltages of capacitors inherently stay balanced without using any sensors and/or auxiliary circuits.

### B. Loss and efficiency calculations

The power loss in SC-MLI circuit is mainly comprised of three major factors of conduction, switching, and capacitor voltage ripple losses [3]. Due to the fact that the output voltage includes only nine levels operating with the NLM technique, circuit switches can be turned on and off up to 16 times. Therefore, the switching frequency of all the circuit switches is very low (below 1 kHz), and their related switching loss is negligible [7]. Generally, the total circuit conduction losses ( $P_{conduction}$ ) can be calculated by the sum of the conduction loss of each voltage level ( $P_{con-L}$ ) [16], [17].

$$P_{conduction} = \sum_{L=4}^4 P_{con-L} \quad (8)$$

$$P_{con-L} = P_{con-L}^{sw} + P_{con-L}^D \quad (9)$$

Where  $P_{con-L}^{sw}$  and  $P_{con-L}^D$  represent the conduction losses of the power switches and diodes per each level, respectively. The conduction loss mainly depends on the number of semiconductor devices, the average ( $i_{av-L}$ ) and root mean square ( $i_{rms-L}$ ) values of the current flowing in each level which can be calculated by means of (10) and (11).

$$P_{con-L}^{sw} = N_{sw} (V_{on}^{sw} i_{av-L} + R_{on}^{sw} i_{rms-L}^2) \quad (10)$$

$$P_{con-L}^D = N_D (V_{on}^D i_{av-L} + R_{on}^D i_{rms-L}^2) \quad (11)$$

Note that,  $V_{on}^{sw}$ ,  $V_{on}^D$  are the on-state voltages of circuit switches and diodes, respectively. Similarly,  $R_{on}^{sw}$ ,  $R_{on}^D$  are their on-state resistance. In addition, the number of power switches ( $N_{sw}$ ) and diodes ( $N_D$ ) involved in forming each voltage level are specified in table II.

TABLE II. SIMPLIFIED OVERVIEW OF THE 9L-SCI

Level	Active Switches ( $N_{sw}$ )	Diodes ( $N_D$ )
0	2	2
$\pm 1$ Vdc	3	3
$\pm 2$ Vdc	3	1
$\pm 3$ Vdc	5	1
$\pm 4$ Vdc	6	0

Furthermore, power losses caused by the voltage ripple of the capacitors ( $P_{ripple}$ ) can be calculated by [3]:

$$P_{ripple} = \sum_{m=1}^4 P_{ripple,Cm} \quad (12)$$

$$P_{ripple,Cm} = \frac{f_{ref}}{2} (C_m \cdot \Delta V_{ripple,Cm}^2) \quad (13)$$

Where,  $C_m$  represents the capacitance of each capacitor and  $f_{ref}$  is the output frequency. Also, the voltage ripple of each capacitor ( $\Delta V_{ripple,Cm}$ ) can be obtained by:

$$\Delta V_{ripple,Cm} = \frac{1}{C_m} \int_{t_c}^{t_d} i_{Cm}(t) dt \quad (14)$$

Therefore, total power loss of the converter can be achieved by collecting all the power losses together as described in (15). Eventually, the efficiency ( $\eta$ ) of the whole circuit can be determined by (16).

$$P_{Loss} = P_{conduction} + P_{ripple} \quad (15)$$

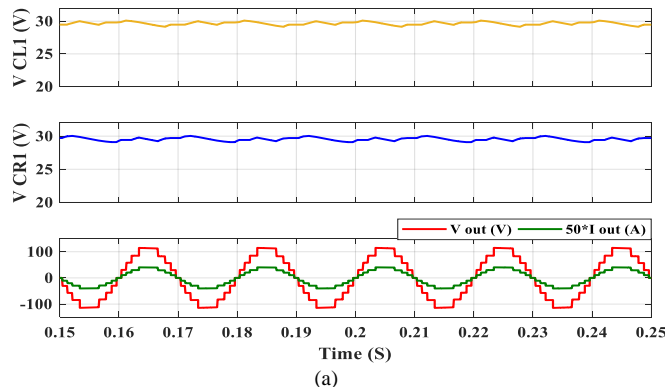
$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \quad (16)$$

### C. Comparative Study

In order to thoroughly survey the structures in this context, several single-phase nine-level SC-MLIs are reviewed in this section. Then, a comparison with these topologies is conducted and the results of this study are brought in Table III. The comparison involves several operational factors consisting the number of voltage levels ( $N_L$ ), semiconductor device count ( $N_{SC}$ ), gate driver circuit ( $N_{dr}$ ), Number of capacitors ( $N_C$ ) and required DC sources ( $N_S$ ). Since, the maximum voltage that each switch should withstand is an important factor for MLIs, Peak Blocking Voltage (PBV) and Total Blocking Voltage (TBV) are taken into consideration for this study.

TABLE III. COMPARISON OF THE 9L-SCI WITH OTHER TOPOLOGIES

Ref.	$N_L$	$N_{sc}$	$N_{dr}$	$N_C$	$N_S$	PBV (*Vdc)	TBV (*Vdc)	Boost ratio
9L-SCI	9	15	13	4	1	2	21	4x
[6]	9	13	13	3	1	4	25	4x
[9]	9	14	9	3	1	4	32	4x
[10]	9	20	8	4	1	4	16	4x
[11]	9	22	19	3	1	1	22	4x
[12]	9	14	12	2	2	2	40	4x
[13]	9	14	10	2	2	4	40	4x
[14]	9	11	8	2	1	2	12	2x
[15]	9	11	10	3	1	1	10	2x



According to this table, the blocking voltage over the switches in [6], [9] are more than the proposed converter. Besides, the structures introduced in [10] and [11] utilize more semiconductors to generate the same output voltage compared to the proposed 9L-SCI. Moreover, the topologies introduced in [12] and [13] require more DC sources. Also, their TBV is significantly higher than the other structures. Although, the structure of [14] and [15] need lower number of semiconductors and blocking voltage, to generate the same output voltage level, their boosting ratio is half of the other topologies.

### IV. PERFORMANCE EVALUATION

The proposed 9L-SCI is simulated in MATLAB SIMULINK environment to ensure the sufficient behavior of the inverter facing various operating conditions. Then, to validate the theoretical and simulation results, experimental ones are conducted by the use of a laboratory prototype. To reach this goal, both of simulations and experimentations are accomplished with similar parameters, as presented in Table IV. The operation of the 9L-SCI prototype is controlled by help of NLM modulation technique, as well. Accordingly, the operation of the proposed converter supplying a resistive ( $L_1$ ) and resistive-inductive ( $L_2$ ) loads are presented in figs. 5 and 6, respectively. In these figures, the output voltage and current waveforms accompanied by the capacitors voltages for both simulation and experimental results are depicted. To investigate the performance of the circuit capacitors,  $C_{L1}$  and  $C_{R1}$  are selected as a sample from each side of the converter. It can be seen that their voltages ( $V_{CL1}$ ,  $V_{CR1}$ ) stay in their pre-defined boundaries without the necessity to use any kinds of external controller to balance their voltage.

TABLE IV. SPECIFICATION OF THE 9L-SCI

Factor	Description
<b>Input voltage (<math>V_{dc}</math>)</b>	32 V
<b>Boost Ratio (n)</b>	4
<b>Output Frequency (<math>f_o</math>)</b>	50 HZ
<b>Circuit Capacitances</b>	2200 $\mu$ F
<b>Switch</b>	MOSFET- IRFP460
<b>Opto-coupler Driver</b>	HCPL-3120
<b>Controller Chipset</b>	AVR- ATMEGA 16
<b>Load</b>	$L_1 = 140 \Omega$
	$L_2 = 50 \Omega + 300 \text{ mH}$
	$L_3 = 280 \Omega$

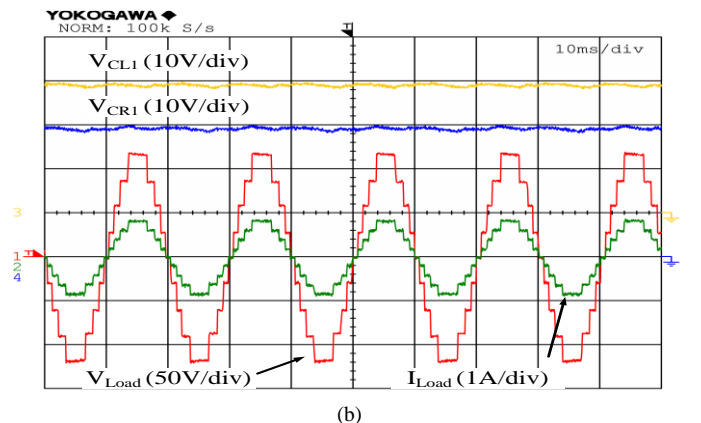


Fig. 5. The output voltage and current waveforms supplying a resistive load (a) simulation, and (b) experimentation

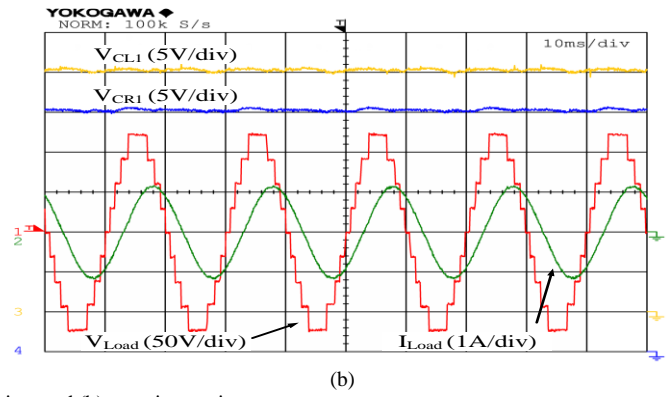
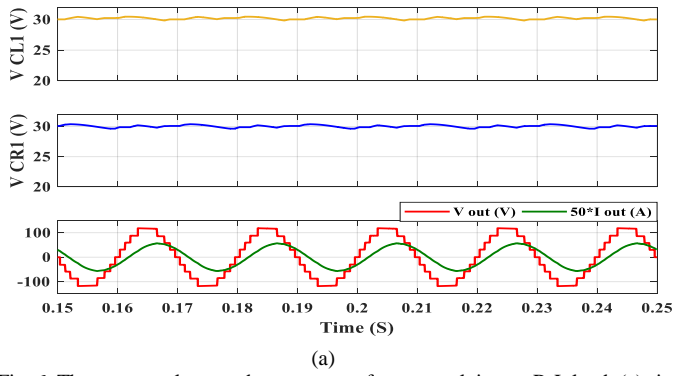


Fig. 6. The output voltage and current waveforms supplying an R-L load: (a) simulation, and (b) experimentation

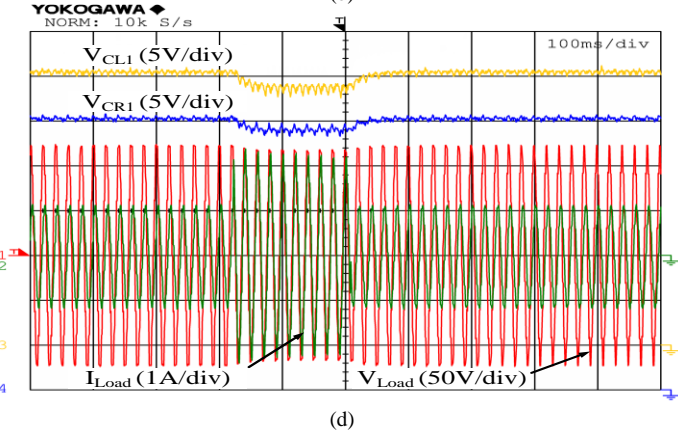
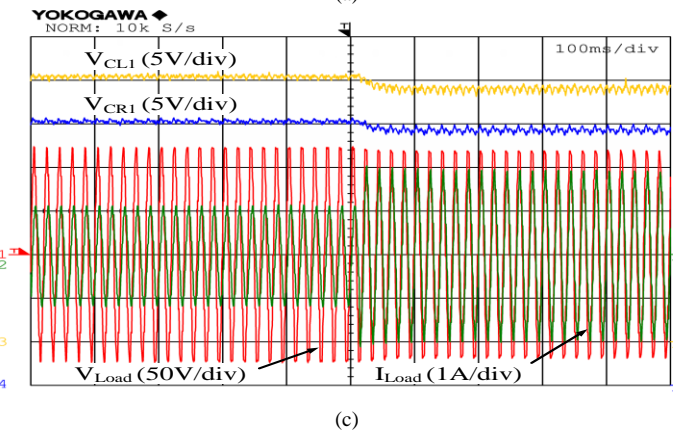
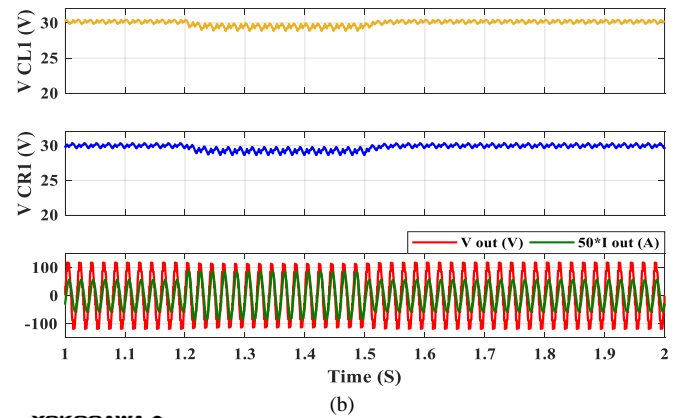
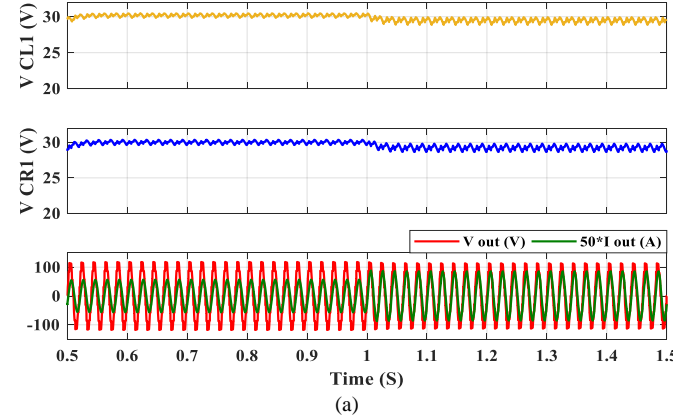


Fig. 7. The output voltage and current waveforms facing sudden change load: (a), (b) simulation, (c) and (d) experimentation

Moreover, the performance of the converter when another load ( $L_2$ ) suddenly connects to the existing load ( $L_1$ ) in parallel is also assessed. The results of such instantaneous load variation are depicted in Fig. 7. The results show that the behavior of the 9L-SCI converter ensures the capacitors properly follow their intended reference voltage and their voltages remain well balanced. The amplitude of the load voltage will in turn remain almost unaffected. By comparing the simulation results with the experimentation ones, the proper operation of the proposed inverter is validated.

Furthermore, Fig.8 (a) provides the harmonic spectrum of the load voltage for a pure resistive load with a Total Harmonic Distortion (THD) of 9.59 %. It also implies that the amplitude of all unwanted harmonics are kept below 4 % of the fundamental signal without using any filters. However, in

case of requiring an output voltage with higher quality, an output filter is applied for the same load condition lowering the THD down to 3.47 % with each individual harmonic coefficient less than 3 %. The harmonic content in presence of the filter is demonstrated in Fig. 8 (b).

To further investigate the performance of the inverter in various loading conditions, the THD of the load voltage and the efficiency of the converter with the variation of input voltage ( $V_{dc}$ ), are calculated. Then, the results are summarized in Fig. 9. As the figure shows, the THD is not reliant on the changes of the input voltage and it is just affected by the load alterations. However, the efficiency of the converter varies align with the variations of the input voltage. The rise in the input voltage leads to an increase in the efficiency.

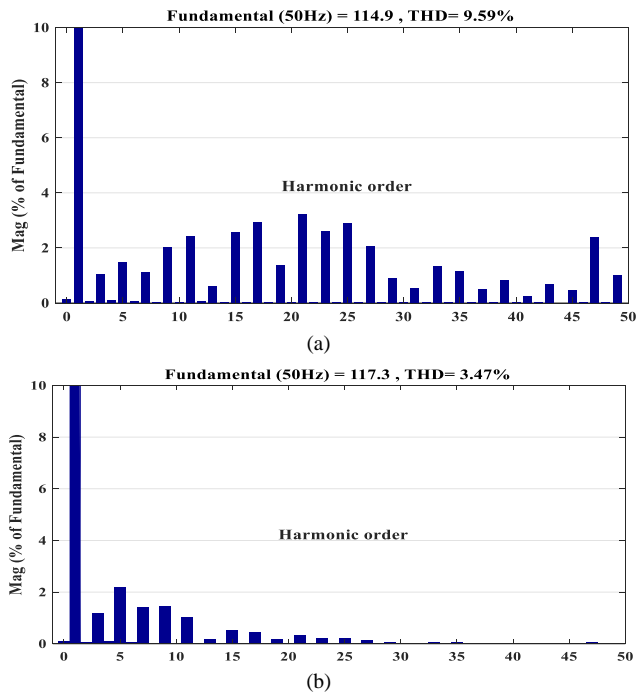


Fig. 8. The harmonic content of the output voltage waveform (a) THD spectra without using output filter, (b) THD spectra with employing an output filter

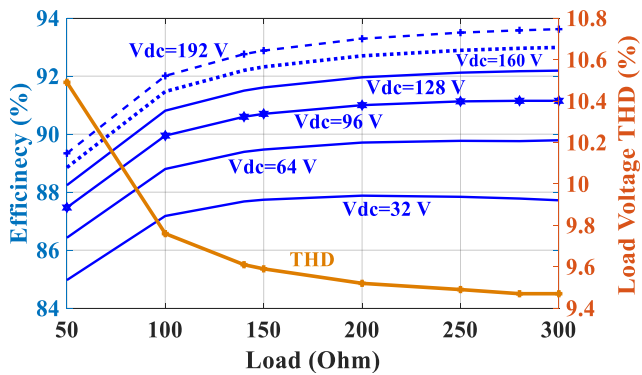


Fig. 9. Efficiency and output voltage THD variation versus load variation at different input voltage levels

## V. CONCLUSION

In this paper, a new multilevel inverter structure with the ability to boost the input voltage four times is introduced. The operation of this switched-capacitor converter is controlled by the help of the NLM technique which significantly eases its implementation. The proposed single source inverter benefits from the reduced number of semiconductor devices, less PBV and TBV for generating the 9-Level output compared to the similar topologies. Precise mathematical analyses ensure the self-voltage balancing ability of the circuit capacitors eliminating any need for sensors and external complex balancing circuits. The performance of inverter is validated through both simulation model and implementation of a nine-level laboratory prototype. The results show a THD of 9.59 % for the output voltage with an efficiency above 87.32 % depending on the input voltage which approve the proper operation of the proposed circuit structure for different loading conditions.

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