Design of State-Feedback Controller for a Single-Phase Grid-Connected Siwakoti-H Inverter with LCL filter

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Abstract

Grid-tied transformerless inverters for photovoltaic (PV) systems have attained a prominent share in the distributed power generation applications on both the domestic and utility scale. This arises the need of a transformerless inverter with less hardware components and complexity. This paper presents a state-feedback current controller (SFCC) for a flying-capacitor based transformerless inverter (Siwakoti-H topology). Compared to the conventional proportional-integral (PI) based control, the state-feedback current control provides a better dynamic performance for a single-phase grid-tied converter equipped with an LCL filter. The controller is designed using pole placement to set the dominant behavior of the converter, which actively damps the resonant frequency of the LCL filter. The controller is extended using *dc* voltage feedforward compensation (DVFC) to maintain the voltage ripple of the flying capacitor within the limits, and an integral state for improved disturbance rejection. Simulation results illustrate the steady-state and dynamic performance of the controller as well as the inherent damping of the LCL filter resonance. Experimental results are presented to verify the steady-state operation of the system.

1 Introduction

The increase in the global consumption of renewable energy necessitates the integration of renewable resources to the grid, which requires an interfacing converter. Power electronic converters are considered as the backbone for energy conversion. In recent years, grid-tied inverters for PV systems have seen an exponential growth for both the utility-scale and distributed generation applications owing to government incentives, declining prices of PV panels and advancement in power electronics technology [1, 2]. Due to the massive development of grid-connected PV systems, there has been an increasing trend to avoid the use of interfacing transformers and replace them with transformerless inverter topologies. Although, transformerless topologies offer better efficiency, less weight/volume and hence lower costs, removing the transformer gives rise to common-mode currents, due to the presence of a parasitic capacitance between the PV panel and its frame [1]. Hence, additional measures have to be undertaken to eliminate the leakage currents and prevent any safety hazard [2].

Various research works have proposed different techniques to mitigate the common-mode currents, e.g., decoupling the *dc* from *ac* side and/or clamping the common-mode voltage (CMV) during the freewheeling period, or using common ground configurations [1]. Among these, the common-ground-type PV inverter has attracted a lot of interest from both industry and academia as it can effectively reduce the leakage current of the PV system. Many common-ground transformerless inverters have been proposed, e.g. in [3–6], but they either use more switches, or more passive components. In [7], a new common-ground-type transformerless inverter was proposed, which works on the principle of a flying capacitor and consists of only four switches. In order to eliminate the leakage currents, the new inverter allows direct connection between the grid-neutral and negative-pole of the PV system.

The use of grid-connected converters allows independent control of active and reactive power exchanged with the grid. However, grid-connected converters generate harmonics which might be harmful for other devices connected to the same grid. In order to meet the grid-code requirement of injecting a current with less total harmonic distortion (THD), it is crucial to use a filter (L or LCL filter) between the converter and the grid [8]. Compared to the L filter, the LCL filter provides much higher attenuation of switching harmonics, and uses smaller components that reduce the volume and weight, while increasing the power density [9]. However, control of the LCL

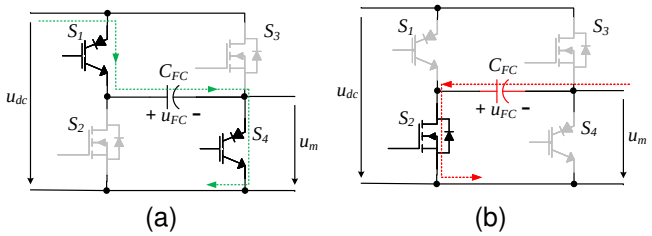


Fig. 1: (a) Charging cycle of the flying capacitor, (b) discharging cycle of the flying capacitor where it acts as a virtual *dc*-link.

filters is complicated due to the presence of a resonant peak in its response. The resonant behavior of the LCL filter amplifies any harmonic components in its vicinity, thereby deteriorating the performance of the converter [10]. This behavior can either be damped by using passive methods which cause additional power losses, or by using active damping methods [11].

Conventionally, the control of grid-connected inverters is carried out by employing voltage oriented control (VOC) [12]. Among other approaches, a proportional-resonant (PR) controller [13], state-feedback controller [14–16] and a predictive controller [17] have been proposed in literature. In [14–16] a pole-placement based control strategy has been proposed that has inherent resonance damping and does not require any additional damping solutions.

In this paper, a discrete-time state-feedback current controller is designed for the recently proposed Siwakoti-H flying capacitor inverter (sFCI) [1, 7] connected to the grid with an LCL filter. Owing to the novel nature of the topology, its various features and working principle are discussed before the design of the control algorithm. The main contributions of this paper are: 1) description and analysis of the operating states; 2) description of the additional non-linear behavior of this topology; 3) system modeling and design of a state-feedback controller for single phase sFCI.

2 Novel flying capacitor topology

2.1 Description and principle of operation

The sFCI is based on the topology proposed in [1, 7]. It is a common-ground-type transformerless inverter that works on the principle of a flying capacitor and has only four active switching elements, see Fig. 1. The uniqueness of this topology is that the negative voltage bus, required for the negative cycle, is fulfilled by using a single input *dc* supply. This is achieved by the cyclic charging and discharging of the flying capacitor thus creating a virtual negative *dc*-link, illustrated in Fig. 1. Since the neutral of the grid can be directly connected to the negative pole of the *dc*-link, any leakage current is automatically eliminated [7]. The phase leg of the three-level sFCI consists of four power switches and one capacitor, as depicted in Fig. 2. Among the four

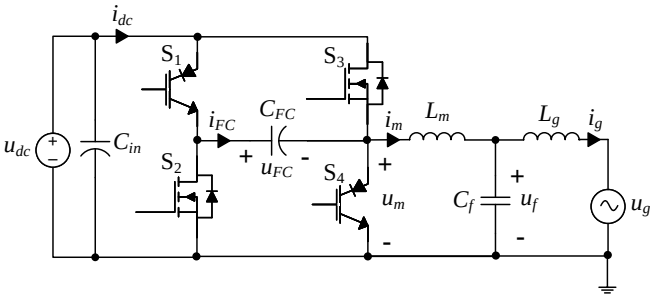
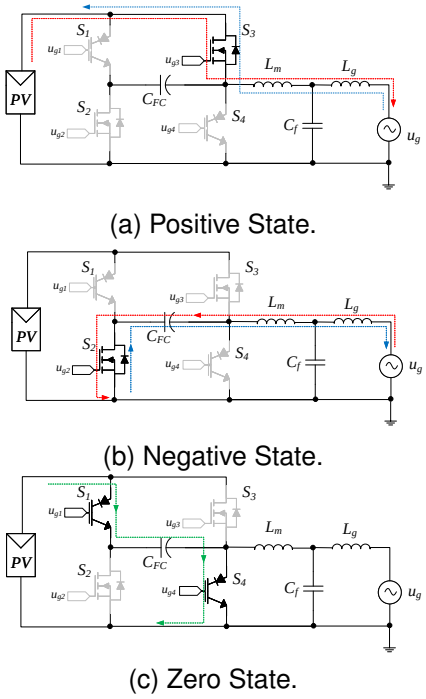


Fig. 2: Single-phase grid-connected sFCI with LCL filter and various measurements.



(a) Positive State.

(b) Negative State.

(c) Zero State.

Fig. 3: Schematic overview of the three operation states and with respective paths for the current flows (red: active current path, blue: reactive current path, green: C_{FC} charging current path).

switches, S_1 and S_4 are devices with bipolar voltage blocking capability, whereas switches S_2 and S_3 are unipolar voltage devices [1]. Therefore, the switches S_2 and S_3 are realized using a MOSFET while S_1 and S_4 are realized using a reverse blocking IGBT (RB-IGBT). As described in [7], this topology has three modes of operation, i.e., positive active (P), negative active (N) and zero state (O), shown in Fig. 3. During the positive and negative states switches S_3 and S_2 are turned on, respectively. During the zero state, which follows the active states P/N, the switches S_1 and S_4 are turned on to allow the flow of charging current.

2.2 Additional non-linear behavior of the Siwakoti-H topology

Although power electronic converters are inherently non-linear due to the presence of switching elements, the sFCI was observed to have additional non-linearities.

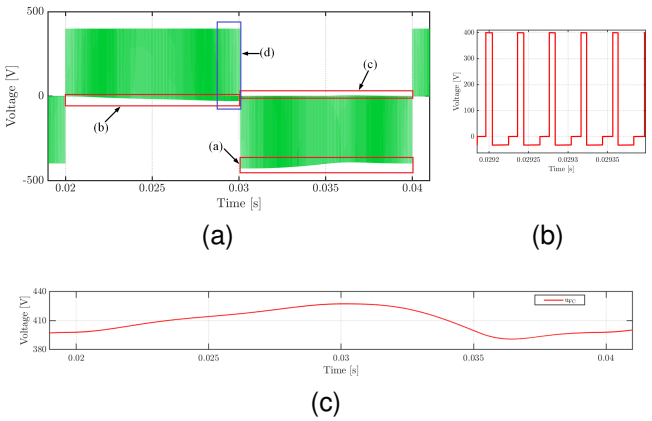


Fig. 4: (a) Bridge output voltage with distortion regions marked with red/blue. (b) Open-loop converter bridge voltage: three-step behavior. (c) Flying capacitor voltage.

This is primarily due to the flying capacitor C_{FC}, which is designed to sustain a ripple voltage $\Delta u_{FC} = (\max(u_{FC}) - \min(u_{FC}))$, see Fig. 4(c). The effect is visible at the voltage output of the converter bridge as shown in Fig. 4. Fig. 4(a) shows the bridge voltage output of the sFCI with distorted regions marked in red/blue boxes. A brief explanation is as follows:

(a) The peak of the bridge voltage, during the negative cycle, follows the slow decrease in the voltage u_{FC}. As can be seen, the peak output voltage u_m varies between $-430\,\text{V}$ and $-390\,\text{V}$ due to the voltage ripple of the flying capacitor (Δu_{FC}).

(b) During the zero state of positive half cycle, the bridge voltage u_m of the sFCI is non-zero. The main reason for this is that the voltage u_{FC} is higher than the input *dc*-link and hence a negative voltage drop appears across the switch S_4, i.e., $u_{S_4} = (u_{dc} - u_{FC}) < 0$.

(c) During the zero state of negative half cycle, the bridge voltage u_m is again non-zero. This voltage is primarily due to the voltage drop across the switch S_4 as both the main current and charging current flow through it.

(d) From the zoomed-in view of the region (d) [see Fig. 4(b)] it is observed that the Siwakoti-H inverter generates three different voltage values in a single switching period unlike the conventional topology like the NPC converter. This behavior is primarily due to the ripple of the main inductor current. At the transition from positive to negative cycle, the main inductor current i_m goes negative due to its ripple. In this situation, series diode of the switch S_4 becomes forward biased due to high di/dt and hence S_4 conducts for a part of the switching period. Whenever S_4 conducts, the output voltage changes from a negative value (u_{S_4}) to a voltage ≈ 0. Hence, instead of a normal two-level voltage behavior, three stepped voltages are observed in the sFCI.

3 System modeling

A grid connected sFCI with an LCL filter is shown in Fig. 2. The converter employs a common capacitor C_{in} for the input *dc*-link with a constant voltage u_{dc}, and a separate flying capacitor (C_{FC}) for each phase. The LCL-filter consists of a main inductor L_m and a grid-side inductor L_g, with internal resistances R_m and R_g, respectively, and the filter capacitance C_f with parasitic resistance R. The LCL filter offers attenuation to the harmonics generated by the converter, before it is connected to the grid. It is assumed that the amplitude and phase of the grid voltage remains constant for the model and the direction of the current flow is from the converter to the grid.

In the following, the continuous- and discrete-time models of the system are introduced and will be utilized for the design of the controller. Since the resistances of the filter components provide extra damping, a loss-less LCL filter is considered, representing a worst-case situation for the LCL filter resonance. Such a simplification, however, reduces the complexity of the discrete-time model and the controller.

For the modeling of the system, we introduce the following assumptions :

Assumption (A.1) *The grid voltage $u_g(t)$ is considered as a disturbance input. It has a positive magnitude, and a constant angular frequency $\omega_g > 0$.*

Assumption (A.2) *The switching behavior of the converter bridge is neglected, i.e. the non-linear behavior of the flying capacitor due to its interaction with the switches is not considered in the modeling stage.*

Assumption (A.3) *The bridge voltage $u_m(t)$ is assumed to be constant during $kT_s < t < (k+1)T_s$,* where T_s is the sampling interval [15].

3.1 Continuous-time model

As per assumption (A.2) the dynamics of the flying capacitor are neglected, and hence the system to be controlled reduces to the LCL-filter/grid. The state vector is defined as $\boldsymbol{x} = [i_m \;\; u_f \;\; i_g]^\top$, where i_m is the main inductor current, u_f is the voltage across the filter capacitor C_f, and i_g is the grid current. Invoking assumptions (A.1), (A.2), Kirchhoff's current and voltage laws, the system dynamics in continuous time can be written as

$$\frac{d\boldsymbol{x}}{dt} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_m} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ 0 & \frac{1}{L_g} & 0 \end{bmatrix}}_{\mathbf{F}} \boldsymbol{x} + \underbrace{\begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{G}} u_m + \underbrace{\begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g} \end{bmatrix}}_{\mathbf{T}} u_g$$
$$y = \underbrace{\begin{bmatrix} 0 & 0 & 1 \end{bmatrix}}_{\mathbf{C}} \boldsymbol{x} \tag{1}$$

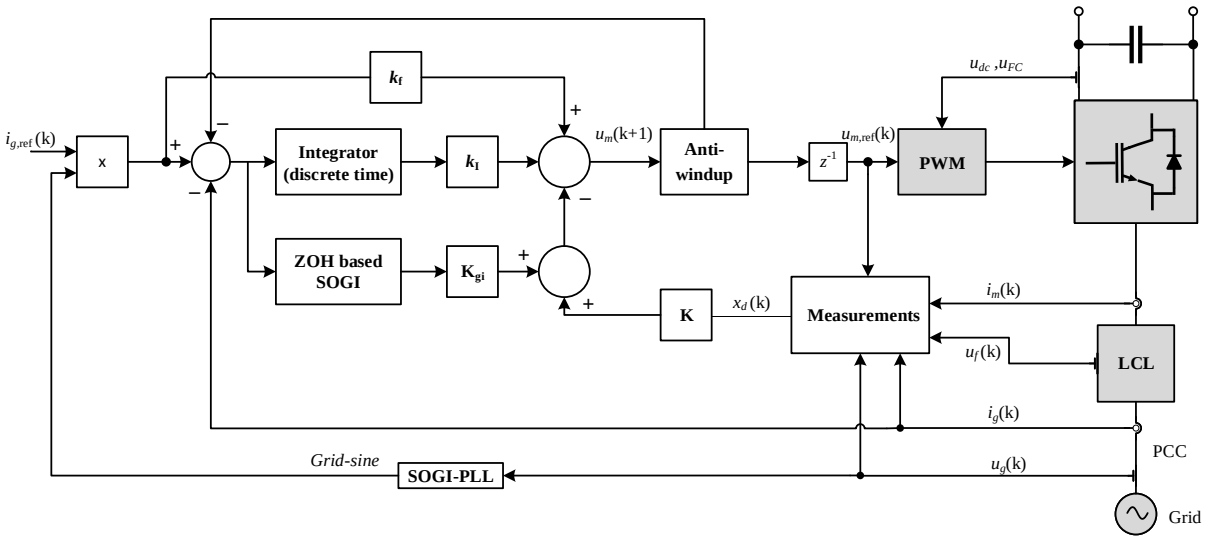


Fig. 5: Closed loop control structure for the single-phase sFCI.

where u_m is the converter bridge voltage, u_g is the grid voltage and y is the output, i.e., the grid current i_g of the system.

3.2 Discrete-time model

For the discrete-time controller design, a zero-order-hold (ZOH) discrete-time model is used. Under the assumptions (A.1), (A.3) and considering that the bridge voltage is averaged over the switching-cycle, the discrete time model of (1) becomes

$$\boldsymbol{x}(k+1) = \mathbf{A}\boldsymbol{x}(k) + \mathbf{B}u_m(k) + \mathbf{E}u_g(k) \quad (2a)$$
$$y(k) = \mathbf{C}\boldsymbol{x}(k) \quad (2b)$$

where the discretized system matrices are

$$\mathbf{A} = e^{\mathbf{F}T_s}, \mathbf{B} = \left(\int_0^{T_s} e^{\mathbf{F}\tau} d\tau\right)\mathbf{G}, \mathbf{E} = \left(\int_0^{T_s} e^{\mathbf{F}\tau} d\tau\right)\mathbf{T}. \quad (3)$$

Due to the finite computation time, there exists a computational delay between the calculation of the desired voltage $u_{m,\text{ref}}$ and its application to the pulse-width-modulation (PWM) block [18]. This delay is modeled as $u_m(k) = u_{m,\text{ref}}(k-1)$ [15]. Taking the computational delay into account, the discrete-time model is written as

$$\begin{aligned}\boldsymbol{x}_d(k+1) &= \mathbf{A}_\text{d}\boldsymbol{x}_d(k) + \mathbf{B}_\text{d}u_{m,\text{ref}}(k) + \mathbf{E}_\text{d}u_g(k)\\ \boldsymbol{y}(k) &= \mathbf{C}_\text{d}\boldsymbol{x}_d(k)\end{aligned} \quad (4)$$

where the modified state vector is $\boldsymbol{x}_d = [\boldsymbol{x}^\top \;\; u_m]^\top$, and

$$\mathbf{A}_\text{d} = \begin{bmatrix}\mathbf{A} & \mathbf{B}\\ \mathbf{0}_{1\text{x}3} & 0\end{bmatrix}, \mathbf{B}_\text{d} = \begin{bmatrix}\mathbf{0}_{3\text{x}1}\\ 1\end{bmatrix}, \mathbf{E}_\text{d} = \begin{bmatrix}\mathbf{E}\\ 0\end{bmatrix}, \mathbf{C}_\text{d} = \begin{bmatrix}\mathbf{C}^\top\\ 0\end{bmatrix}^\top.$$

4 State-feedback control design

The scheme of the current controller based on state feedback is shown in Fig. 5. The objective of the controller is the grid current reference ($i_{g,\text{ref}}$) tracking, while maintaining the voltage ripple of the flying capacitor within prescribed limits. For improved disturbance rejection, the controller is extended using an integral-state by introducing an integrator into the control loop. The integral state is defined as

$$x_I(k+1) = x_I(k) + i_{g,\text{ref}}(k) - i_g(k) \quad (5)$$

where $i_{g,\text{ref}}$ is the grid current reference. The state-space control law becomes

$$u_{m,\text{ref}}(k) = k_I x_I(k) + k_f\, i_{g,\text{ref}}(k) - \mathbf{K}\boldsymbol{x}_d(k) \quad (6)$$

where k_I is the gain of the integral state, k_f is the feedforward gain, $\mathbf{K} = [k_1 \;\; k_2 \;\; k_3 \;\; k_4]$ is the state-feedback gain, and $\boldsymbol{x}_d = [\boldsymbol{x}^\top \;\; u_m]^\top$ is the state matrix augmented with the delayed voltage reference. The state-feedback controller, with the integral action included, can be designed to have good damping of the LCL filter resonance and disturbance rejection [15].

4.1 Second order generalized integrator (SOGI)

SOGIs are used for obtaining zero steady-state error when using stationary reference frames in grid-connected inverters, rectifiers, and active filters. These integrators have also been used in algorithms for grid synchronization, detection of sequences and harmonic compensation [19]. In state-feedback based control approaches, SOGIs can be employed to enable grid phase detection and subsequently minimize or eliminate the generated phase delay [20]. Since the implementation of these algorithms is done using

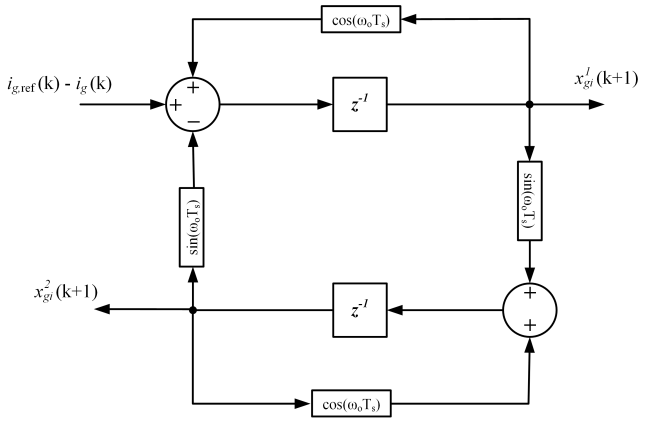


Fig. 6: SOGI based on ZOH method.

microcontrollers, design in discrete time is a necessity. In [19], it has been shown that for a discrete time SOGI, better results are obtained using ZOH technique. Fig. 6 depicts the structure of the SOGI where the sine and cosine gains are related to the tuning frequency of the SOGI, i.e., 50Hz.

The (discrete-time) difference equations for the SOGI can be written as

$$\begin{aligned} x_{gi_1}(k+1) =& \cos(\omega_g T_s) x_{gi_1}(k) - \sin(\omega_g T_s) x_{gi_2}(k) \\ & - i_g(k) + i_{g,\text{ref}}(k) \\ x_{gi_2}(k+1) =& \sin(\omega_g T_s) x_{gi_1}(k) + \cos(\omega_g T_s) x_{gi_2}(k) \end{aligned} \tag{7}$$

Hence the generalized integrator model becomes

$$\boldsymbol{x}_{gi}(k+1) = \boldsymbol{\Gamma}_{\text{gi}} \boldsymbol{x}_{gi}(k) - [(i_g(k) + i_{g,\text{ref}}(k)) \;\; 0]^\top \tag{8}$$

where

$$\boldsymbol{\Gamma}_{\text{gi}} = \begin{bmatrix} \cos(\omega_g T_s) & -\sin(\omega_g T_s) \\ \sin(\omega_g T_s) & \cos(\omega_g T_s) \end{bmatrix}, \boldsymbol{x}_{gi}(k) = \begin{bmatrix} x_{gi_1}(k) \\ x_{gi_2}(k) \end{bmatrix}$$

4.2 Augmented system for pole placement

For pole placement, the system model of (4) is augmented with the integral state (5) and the generalized integrator (8), resulting in

$$\begin{aligned} \boldsymbol{x}_a(k+1) =& \mathbf{A}_{\text{a}} \boldsymbol{x}_a(k) + \mathbf{B}_{\text{a}} u_{m,\text{ref}}(k) \\ & + \mathbf{E}_{\text{a}} u_g(k) + \mathbf{P}_{\text{a}} i_{g,\text{ref}}(k) \end{aligned} \tag{9}$$

where $\boldsymbol{x}_a = [\boldsymbol{x}_d^\top \;\; x_I \;\; \boldsymbol{x}_{gi}^\top]^\top$ is the augmented state vector, and

$$\mathbf{A}_{\text{a}} = \begin{bmatrix} \mathbf{A}_{\text{d}} & \mathbf{0}_{4\text{x}1} & \mathbf{0}_{4\text{x}2} \\ -\mathbf{C}_{\text{d}} & 1 & \mathbf{0}_{1\text{x}2} \\ -\boldsymbol{\Gamma}_{\text{a}} & \mathbf{0}_{2\text{x}1} & \boldsymbol{\Gamma}_{\text{gi}} \end{bmatrix}, \mathbf{B}_{\text{a}} = \begin{bmatrix} \mathbf{B}_{\text{d}} \\ 0 \\ \mathbf{0}_{2\text{x}1} \end{bmatrix}, \mathbf{E}_{\text{a}} = \begin{bmatrix} \mathbf{E}_{\text{d}} \\ 0 \\ \mathbf{0}_{2\text{x}1} \end{bmatrix},$$

$$\boldsymbol{\Gamma}_{\text{a}} = \begin{bmatrix} \mathbf{C}_{\text{d}} & 0 \\ \mathbf{0}_{1\text{x}4} & 0 \end{bmatrix}, \mathbf{C}_{\text{d}} = \begin{bmatrix} \mathbf{C} & 0 \end{bmatrix}, \mathbf{P}_{\text{a}} = \begin{bmatrix} \mathbf{0}_{1\text{x}4} & 1 & 1 & 0 \end{bmatrix}^\top. \tag{10}$$

Parameter	Value
ζ_1	0.8
ω_1	2π·1950 rad/s
ζ_2	0.204
ω_2	$\approx \omega_r$ rad/s
ζ_d	0.1

Tab. 1: Tuning Parameters.

are the augmented system matrices. The state-feedback gain vector is $\mathbf{K}_{\text{a}} = [\mathbf{K} \;\; -k_I \;\; k_6 \;\; k_7]$ where the gains k_6, k_7 are related to the SOGI. Also the output matrix $\mathbf{C}_{\text{a}} = [0 \;\; 0 \;\; 1 \;\; 0 \;\; 0 \;\; 0 \;\; 0]$. The transfer function from the reference current $i_{g,\text{ref}}(z)$ to the grid side current $i_g(z)$ is written as

$$\boldsymbol{H}(z) = \mathbf{C}_{\text{a}}(z\mathbf{I} - \mathbf{A}_{\text{a}} + \mathbf{B}_{\text{a}}\mathbf{K}_{\text{a}})^{-1}(\mathbf{B}_{\text{a}} k_f + \mathbf{P}_{\text{a}}). \tag{11}$$

The denominator polynomial (i.e. the characteristic polynomial) written as

$$\boldsymbol{d}(z) = \det(z\mathbf{I} - \mathbf{A}_{\text{a}} + \mathbf{B}_{\text{a}}\mathbf{K}_{\text{a}}) \tag{12}$$

has seven poles, where one pole is originating from the ZOH property of the system, four poles depend on the dynamics of the LCL filter and the remaining two poles depend on the SOGI.

4.3 Pole Placement

A fully controllable system can be controlled by designing the feedback gain matrix using direct pole placement. Selection of the pole locations depends on a compromise between robustness and dynamic response [15, 16]. Let the desired characteristic polynomial be

$$\boldsymbol{d}^*(z) = z(z-\boldsymbol{\alpha}_1)(z-\boldsymbol{\alpha}_2)(z-\boldsymbol{\alpha}_3)(z-\boldsymbol{\alpha}_4)(z-\boldsymbol{\alpha}_5)(z-\boldsymbol{\alpha}_6). \tag{13}$$

In the desired characteristic polynomial (13), the two complex poles $\boldsymbol{\alpha}_{1,2}$ are placed to determine the dominant behavior (i.e., bandwidth of the controller) and two poles $\boldsymbol{\alpha}_{3,4}$ are placed to determine the resonant behavior (i.e., the resonance damping). These poles are placed such that the controller has sufficient bandwidth and the closed loop offers sufficient damping of the LCL filter resonance. To simplify the procedure, poles are specified in the continuous-time domain and then mapped to the discrete-time domain [15]. The dominant and the resonant behavior can be specified by two second order polynomials as

$$\underbrace{(s^2 + 2\zeta_1\omega_1 s + \omega_1^2)}_{\text{Dominant behavior}} \underbrace{(s^2 + 2\zeta_2\omega_2 s + \omega_2^2)}_{\text{Resonant behavior}} \tag{14}$$

Tab. 1 gives an overview of the tuning parameters chosen for pole placement. ω_1 specifies the desired bandwidth, selected as $1/20^{th}$ of the switching frequency. The damping ratio ζ_1 is set to a large value to prevent large overshoots. For damping of the resonant behavior frequency ω_2 is kept near the natural frequency of the

Parameter	Symbol	Value
Nominal power	P_n	1.67 kW
Converter-side inductance	L_m	400 µH
Converter-side resistance	R_m	50 mΩ
Grid-side inductance	L_g	56 µH
Grid-side resistance	R_g	30 mΩ
Filter Capacitance	C_f	5 µF
ESR of filter capacitor	R	7.4 mΩ
Flying Capacitor	C_{FC}	680 µF
DC-link voltage	u_{dc}	400 V
Switching frequency	f_{sw}	40 kHz
Sampling time	T_s	25 µs
Dead time	T_d	300 ns
Nominal grid voltage	u_g	230 V(rms)
Grid Inductance	L_{grid}	0.01 mH
Grid Resistance	R_{grid}	0.1 Ω

Tab. 2: System parameters for simulations and hardware test-bench.

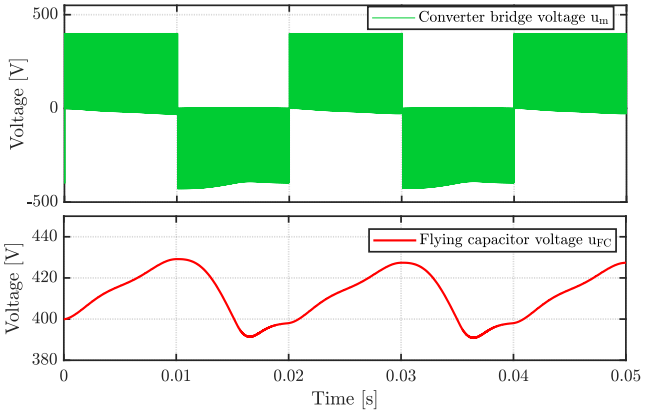
LCL filter ω_r, whereas the damping ratio ζ_2 is chosen to be small, in order to keep the damping effort of the controller low [21].

Furthermore, the pole at the origin due to the ZOH discretization, is not moved. The SOGI introduces a complex-conjugate pair of poles corresponding to its tuning frequency $\omega_g = 2\pi \cdot 50$ rad/s. Since the main aim of using an SOGI is to eliminate the phase-shift, it is sufficient to provide a slight damping to its poles (ζ_d), in order to keep them in the vicinity of the open loop poles and avoid aggressive control inputs which might compromise the loop stability.

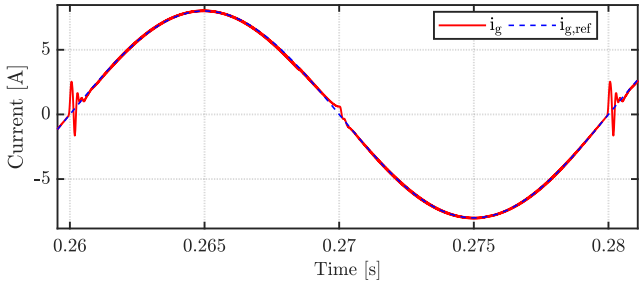
4.4 DC voltage feedforward compensation (DVFC)

The input supply of the three-level sFCI is composed of two separate capacitors, i.e., the input *dc*-link capacitor C_{in} and the flying capacitor C_{FC}, that are responsible for supplying power in the positive and negative cycles, respectively. Although the input capacitor C_{in} has a constant voltage across it, the flying capacitor has a voltage ripple equal to Δu_{FC} across it, see Fig. 7(a). This variation in the supply voltage has a prominent effect on the output of the converter bridge. In order to account for this abrupt variation of supply voltage a feedforward approach is proposed.

As a general practice, the output of the state-feedback controller $u_{m,\text{ref}}(k)$, which is fed to the PWM block, is normalized with the input *dc*-link voltage measurement. However, in the present scenario, the normalization should be carried out separately for the positive and negative cycles using the voltage measurements across C_{in} and C_{FC}, respectively. In this way the effect of the voltage ripple Δu_{FC} and the variation in the supply voltage can be incorporated into the control structure. This approach is termed as *dc* voltage feedforward compensation (DVFC).



(a) Converter Bridge voltage and C_{FC} voltage.



(b) Comparison of the reference and the grid currents.

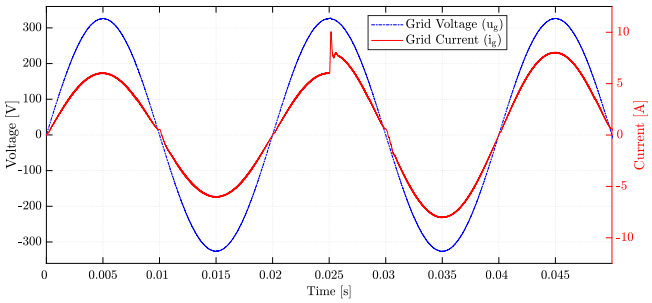
Fig. 7: Steady-state performance of the closed loop system with dead-time = 300 ns.

5 Simulation Results

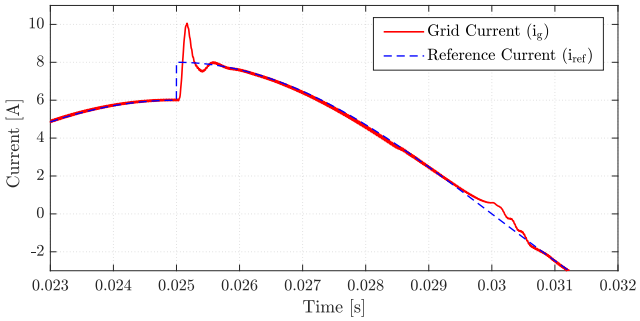
The performance of the proposed control scheme is verified using Matlab/Simulink and PLECS simulations. The configuration of the control scheme is shown in Fig. 5. Tab. 2 summarizes the system parameters used for the simulations. The system under consideration is a single-phase sFCI rated for 1.67 kW. Since the resonant frequency of the LCL filter is 10.155 kHz, the switching frequency is set to 40 kHz to avoid any excitation of the filter modes and provide sufficient bandwidth to the control loop.

5.1 Steady-state performance

Figs. 7(a) and (b) show the steady-state response of the grid-connected converter for a current reference of 6 A. Fig. 7(a) shows the voltage output u_m of the converter, and the voltage u_{FC} across the flying capacitor, which exhibits a voltage ripple $\Delta u_{FC} \approx 40$ V. From Fig. 7(b) it can be concluded that the proposed SFCC achieves reference tracking, with slight deviation at the zero crossings. The deviation at the first zero crossing (positive going) is due to the converter dead time, while at the second crossing it is due to the abrupt change in the supply source, i.e. from the input capacitor to the flying capacitor.



(a) Comparison of grid voltage and grid current.



(b) Comparison of reference and grid currents.

Fig. 8: Dynamic performance of the closed loop system with no dead-time.

5.2 Dynamic performance

Figs. 8(a) and (b) show the dynamic response of the closed-loop system for an initial current reference of 6 A with a step at 0.025 s to 8 A. Fig. 8(a) shows a comparison between the grid voltage and the grid current. Since the reactive power demand is set to zero, the grid current follows the grid voltage, i.e., it is in-phase with the grid, implying that the controller achieves grid synchronization. The dynamic response of the SFCC is apparent from Fig. 8(b) which shows a zoomed-in view of the comparison between the reference current and the grid current. At 0.025 s the current reference is increased from 6 A to 8 A and it is observed that the current settles within 1 ms after a small overshoot. Moreover, the deviation at zero crossing, which is inherent to this topology, is clearly visible.

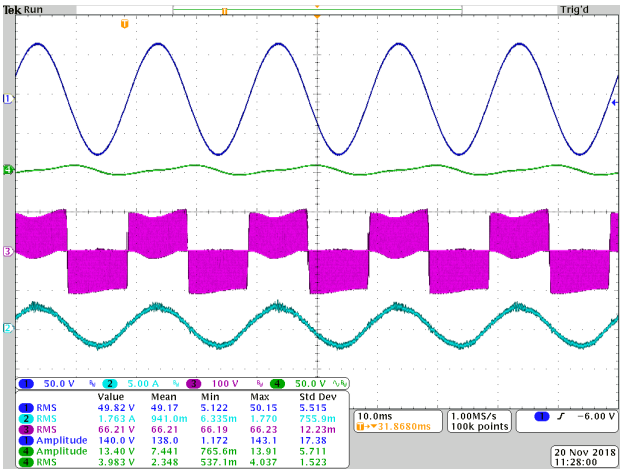
The THD of the grid current is 2.02% for zero dead-time and 3.7% for a dead-time of 300 ns.

6 Experimental Results

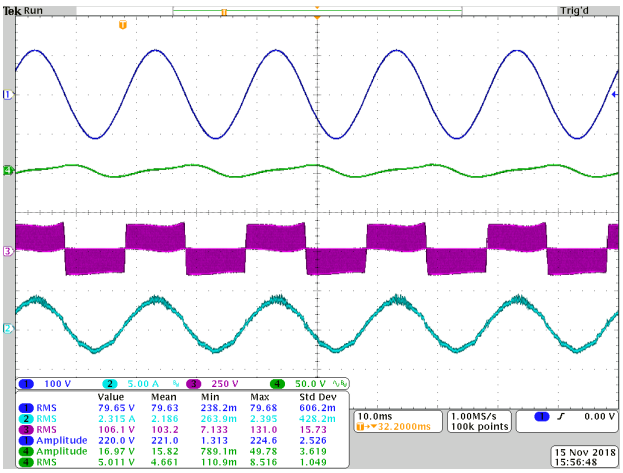
In this section preliminary results obtained at low power are presented to prove the working of the designed controller for the sFCI topology. The implementation was carried out using the controller TMS320F28379D from the C-2000 microcontroller family of Texas Instruments. The hardware design of the inverter was carried out previously in [22]. For details see [22, Fig. 9].

Figs. 9(a) and (b) show the closed-loop measurements when grid voltages of 50 V(rms) and 80 V(rms) are used, respectively. From Figs. 9(a) and (b) it can be seen that the grid current is in-phase with the grid voltage. Additionally, it is observed that the deviation from sinusoidal behavior is present at the transition from positive to negative cycle.

The experimental measurements could not be carried out at higher voltages as the case temperature of RB-IGBTs (particularly S_4) approached the maximum allowed limit of 110 °C, for a *dc*-link voltage of 190 V and were mostly destroyed due to thermal runaway.



(a) Closed-loop measurements with a grid voltage of 50 V (rms) and a reference current of 2 A.



(b) Closed-loop measurements with a grid voltage of 80 V (rms) and a reference current of 3.3 A.

Fig. 9: Experimental measurements for implementation of the state-feedback control on the single-phase sFCI. The oscilloscope measurements represent: grid voltage(dark blue), flying capacitor voltage(green), converter output voltage(pink), and grid current(cyan).

7 Conclusion

In this paper the single-phase Siwakoti-H inverter has been investigated and the design of a discrete-time state-feedback controller has been presented. The Siwakoti-H inverter has the potential of becoming an

attractive alternative to conventional topologies as it can be realized using lesser and smaller components.
The behavior of this new topology has been discussed and a model of the converter with an LCL filter was derived. The operation of the state-feedback controller was validated using simulation and experimental results. The results prove that this newly proposed topology, in spite of the additional non-linear behavior, can be controlled using a linear controller. The results also show the dynamic and steady state performance of the designed controller. Moreover, the resonance behavior of the LCL filter is well damped without employing any separate damping methods.

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