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NORCHIP and International Symposium of System-on-Chip (SoC)

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2018 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)

Welcome to NORCAS 2018

On behalf of the Organizing Committee, we would like to welcome all of you to Tallinn and to the Fourth IEEE Nordic Circuits and Systems Conference (NorCAS 2018). The conference is a merge of the well-established conferences NORCHIP and the International Symposium on System-on-Chip (SoC).

We have a high-quality program with keynotes and papers to be presented as well as a pre-conference tutorial. Research covering a wide range of topics within circuits and systems in the digital, analog and mixed domains will be presented.

From in total 85 papers submitted, 41 papers were selected for oral presentations and an additional 12 papers for poster presentations. There will be four invited speakers who will share their view on emerging key technologies in the circuits and systems field. In the opening session Dr. Dag T. Wisland, the CTO of Novelda AS, Norway will present innovative wireless sensor solutions based on Ultra-Wideband (UWB) technology. Later in the afternoon Prof. Leonel Sousa from Instituto Superior Técnico, Portugal, will give insights to modular srithmetic based circuits and systems for emerging technologies and applications, in particular the timely deep neural networks and cryptography. In the second morning, Dr. Christoph Hagleitner of IBM Research Zürich, Switzerland, will present transprecision computing circuits and how they can be exploited for energy efficiency. The final talk is given by Dr. Mikkel Høyerby, Merus Audio, Denmark, introducing solutions for cooler, smaller, lighter and better sounding audio products. The day before the official opening of the conference there will also be an exciting tutorial on “Combined Effects of Ionizing Radiation and Electromagnetic Interference on Integrated Circuits and Systems” by Fabian Vargas, PUCRS, Brazil.

The electronics industry in Estonia is not a big one but represented are both international and local companies. The best known from international ones are ABB and Ericsson but there are more. The local companies are not big ones but are known also at international level – Artec Design, Stoneridge Electronics, Testonica – to name only very few of them. In Tallinn, many startups have been gathered into science parks – Tehnopol at Mustamäe, next to the Tallinn University of Technology, and Technopolis at Ülemiste.

Furthermore, we would also like to put forward our great thanks to IEEE Circuits and Systems Society (CAS) for financial co-sponsoring of the conference. We are also thankful to all the Program Committee members and reviewers who have put time and effort into reviewing the submitted papers. Moreover, we are grateful to the NorCAS steering committee for helpful advice and their contribution in the paper selection process. Finally, sincere thanks to Ivan Ring Nielsen from Technoconsult for the technical organization of the event. Starting with NORCHIPin 1985, he has after 33 years, decided to cease his conference organization.

We hope that you will enjoy your time in Tallinn. Although Tallinn is not a big city with population of 450,000, it is known for its famous Old Town – one of the best preserved medievial cities in Europe and listed as a UNESCO World Heritage Site. Tallinn was first mentioned in 1219 and received city rights in 1248 but the earliest settlements date back 5000 years. Today, Tallinn is a mixture of old and new – you can walk between medieval buildings, churches and towers, visit bastions from few centuries old, and shop in different boutiqes, supermarkets, etc. Thanks to the compactness of Tallinn, very many points of interests are in the city center and reachable by just walking. In addition to the Old Town, in the western part of Tallinn is Rocca al Mare – the open-air museum where buildings and farmhouses preserve aspects of Estonian rural culture

We wish you an inspiring conference where your knowledge is increased and friendships are both established and strengthened.

Jari Nurmi	Peeter Ellervee	Technical program committee chairs
General Chair	Conference Chair	Analog: Juri Mihhailov
		Digital: Maksim Jenihhin
		SoC: Kalle Tammemäe

Programme 30 October 2018

09.00 **Opening and welcome**

Jari Nurmi, Tampere University of Technology, FI

Peeter Ellervee, Tallinn University of Technology, EE

1. Plenary session

Chair: Tor S. Lande, University of Oslo, NO

09.15 **Invited talk: UWB Radar Sensor**

Dag T. Wisland, Novelda AS, NO

10.00 A RF Pulse-Width and Pulse-Position Modulator IC in 28 nm FDSOI CMOS

Markus Grözing1, Johannes Digel1, Thomas Veigel1, Robert Bieg1, Jianxiong Zhang1, Simon Brandl1, Martin Schmidt1, Christoph Haslach2, Daniel Markert2, Wolfgang Templ2

1 University of Stuttgart, DE; 2Nokia Bell Labs, DE

10.20 A 0.0186 mm2, 0.65 V Supply, 9.53 ps RMS Jitter All-Digital PLL for Medical Implants

Arjun Ramaswami Palaniappan1,2, Liter Siek1, 1 School of Electrical and Electronic Engineering, VIRTUS, Nanyang Technological University, SG;2 NXP Semiconductors, SG

10.40 Unleashing the full power of feed-forward opamps: a 200MHz, fully differential, conditionally stable, 36dB gain PGA, using a four-stage multi-path 2.5V amplifier with double feed-forward compensation.

Vahur Kampus1, Martin Trojer1, Robert Teschner2, 1 Intel Austria;2 IMST, AT

11.00 **Coffee break**

2.1 Power/Amplifiers

Chair: Kari Halonen, Aalto University, FI

11.30 A 24 GHz, 18 dBm, Broadband, Three Stacked Power Amplifier in 28nm FDSOI

Imad ud Din1, Stefan Andersson1, Therese Forsberg2, Henrik Sjöland1,2, 1 Ericsson AB, SE;2 Lunds Tekniska Högskola, SE

2.2 Network-on-Chip

Chair: Peeter Ellervee, Tallinn University of Technology, EE

Multi-Swarm based NoC Configuration and Synthesis

Muhammad Obaidullah, Gul Nawaz Khan, Fei Yuan, Ryerson University, CA

11.50 A Design Approach for SiGe Low-Noise Amplifiers Using Wideband Input Matching

Zhe Chen, Hao Gao, Peter Baltus, Eindhoven University of Technology, NL

12.10 Design of Stacked-MOS Transistor mm-Wave Class C Amplifiers for Doherty Power Amplifiers

Mohammad Hassan Montaseri, University of Oulu, FI

Fault-Tolerant and Energy-Efficient Communication in Mixed-Criticality Networks-on-Chips

Adele Maleki, Hamidreza Ahmadian, Roman Obermaisser, University of Siegen, Germany

A Distributed DoS Detection Scheme for NoC-based MPSoCs

Cesar G. Chaves1, Siavoosh Payandeh Azad2, Thomas Hollstein1,2, Johanna Sepúlveda3, 1 Frankfurt University of Applied Sciences, DE;2 Tallinn University of Technology, EE;3 Technical University of Munich, DE

12.30 **Lunch**

3.1 Data Converters

Chair: Kari Halonen, Aalto University, FI

13.40 Flying-Capacitor Bottom-Plate Sampling Scheme for Low-Power High-Resolution SAR ADCs

Dmitry Osipov, Steffen Paul, ITEM, DE

14.00 A Configurable Hysteresis Comparator for Asynchronous Sigma-Delta Modulators

Olaitan Olabode, Vishnu Unnikrishnan, Ilia Kempi, Andreas Hammer, Marko Kosunen, Jussi Ryynanen, Aalto University, FI

14.20 A Row-Column Accessed Dynamic Element Matching DAC Architecture for SAR ADCs

Mustafa Kilic, Selman Ergunay, Yusuf Leblebici, EPFL, CH

3.2 Test and Fault Tolerance

Chair: Gert Jervan, Tallinn University of Technology, EE

Mitigating Multi-bit Soft Errors in ASIC Registers Using ECC-aware Register Clustering

Keisuke Inoue, International College of Technology, Kanazawa, JP

On Designing PUF-Based TRNGs with Known Answer Tests

Yang Yu, Elena Dubrova, Mats Näslund, Sha Tao, KTH Royal Institute of Technology, SE

Semiconductor Component Fault Assessment and Probability Impact Estimation on Application Level

Jonas Stricker1, Clemens Kain2, Jerome Kirscher2, Andi Buzo2, Linus Maurer1, Georg Pelz2, 1 Bundeswehr Universität München, DE;2 Infineon Technologies AG, DE

4. Poster session I

Coffee break

14.40 A Comparison of Polar and Quadrature RF-PWM
Muhammad Fahim Ul Haque1, Muhammad Touqir Pasha2, Tahir Malik1, Ted Johansson2, 1 NED University of Engineering and Technology, PK;2 Linkoping University, SE

A Radiation Hardened 16 GS/s Arbitrary Waveform Generator IC for a Submillimeter Wave Chirp-Transform Spectrometer
Philip Ostrovskyy1, Oliver Schrape1, Klaus Tittelbach-Helmrich1, Frank Herzel1, Gunter Fischer1, Peter Boerner3, Alexander Loose3, David Hellmann3, Paul Hartogh3, Dietmar Kissinger1,2, 1 IHP, DE;2 TU Berlin, DE;3 Max Planck Institut for Solar System Research, DE

Insertion-Loss Optimization of Transformer-based Matching Networks for mm-Wave Applications
David Bierbüsse, Renato Negra, RWTH Aachen, DE

FPGA Based Hybrid Computing Platform for ESS Linac Simulator
Arun Jeevaraj1, Emmanuel Laface2, Maurizio Donna2, Fredrik Edman1, Liang Liu1, 1 Lund University, SE;2 ESS, SE

Analysis of Synchronous-Asynchronous NoC for the Dark Silicon Era
Reem Walid Etman1, Salma Hesham1, Diana Goehringer2, Mohamed AbdElGhany1, Klaus Hofmann3, 1 GUC, EG;2 TU-Dresden, DE;3 IES TU-Darmstadt, DE

Master-Clone Placement with Individual Clock Tree Implementation – a Case on Physical Chip Design
Oliver Schrape1, Alexey Balashov1, Aleksandar Simevski1, Carlos Benito2, Milos Krstic1,3, 1 IHP, DE;2 Arquimea Deutschland GmbH, DE;3 University of Potsdam, DE

15.30 **Invited talk: Modular Arithmetic based Circuits and Systems for Emerging Technologies and Applications: Deep Neural Networks and Cryptography**

Leonel Sousa, Instituto Superior Técnico, PT

5.1 High Frequency

Chair: Juri Mihhailov, Tallinn University of Technology, EE

16.15 A 15-50GHz Multiplexer Circuit in 130nm SiGe BiCMOS Technology for Ultra-Wide Frequency Ramps in FMCW Radar

5.2 SoC Applications

Chair: Jari Nurmi, Tampere University of Technology, FI

Three-Dimensional Dynamic Programming Accelerator for Multiple Sequence Alignment

Ruei-Ting Chien1, Yi-Lun Liao1, Chien-An Wang2, Yu-Cheng Li2, Yi-Chang Lu1,2, 1

	Frank Herzel1, Arzu Ergintav1, Johannes Borngräber1, Dietmar Kissinger1,2, 1IHP, DE;2Technische Universität Berlin, DE	*National Taiwan University, TW;2 Graduate Institute of Electronics Engineering, National Taiwan University, TW*
16.35	Building lumped models for measured passive mm-wave components *Eero Sankila, Veeti Kiuru, Janne P. Aikio, Timo Rahkonen, University of Oulu, FI*	Design and Implementation of 2D IDCT/IDST-Specific Accelerator on Heterogeneous Multicore Architecture *Mohammad Ali Pourabed, Sajjad Nouri, Jari Nurmi, Tampere University of Technology, FI*
16.55	A 4.3-mW mm-Wave Divide-by-Two Circuit with 30% Locking Range in 28-nm FD-SOI CMOS *Therese Forsberg, Johan Wernehag, Henrik Sjöland, Markus Törmänen, Lund University, SE*	Embedded Programmable Processor for Compressive Sensing Applications *Mehdi Safarpour, Ilkka Hautala, Olli Silven* *University of Oulu, FI*
17.15	Break	
19.00	**Dinner**	

Programme 31 October 2018

09.00 **Invited talk: Transprecision Computing Circuits for Energy Efficiency**

Christoph Hagleitner, IBM Research, CH

6. Poster session II

Coffee break

09.45 Time-gated CMOS SPAD and a Quantum Well Laser Diode with a CMOS driver for Time-Resolved Diffuse Optics Imaging
Jan Nissinen, Ilkka Nissinen, Sahba Jahromi, Tuomo Talala, Juha Kostamovaara, University of Oulu, FI

Analysis and Design of ESD Protection for Robust Low-Power Pierce Crystal Oscillator Startup
Kim B. Östman1, Erlend Strandvik2, Phil Corbishley2, Tor Ø. Vedal2, Mika Salmi1, 1 Nordic Semiconductor Finland Oy, FI;2 Nordic Semiconductor ASA, NO

An 87% Peak Efficiency, 37W, Class H Audio Amplifier with GaN Output Stage
Nardi Utomo1, Liter Siek1, Heng Goh Yap1, Don Disney2, Lawrence Selvaraj2, Lulu Peng2, 1 Nanyang Technological University, SG;2 GlobalFoundries Inc

Comparison of Ultra Low Power Full Adder Cells in 22 nm FDSOI Technology
Somayeh Hossein Zadeh, Trond Ytterdal, Snorre Aunet, NTNU, NO

Dynamically Reconfigurable Gearbox Switched-Capacitor DC-DC Converter
Dennis Øland Larsen1,2, Martin Vinter2, Ivan Jørgensen1, 1 Technical University of Denmark, DK;2 GN Hearing A/S, DK

Characterization and Considerations for Upset in FPGA
Christian Johansson, Torbjörn Månefjord, Saab AB, SE

6. Plenary session

Chair: Atila Alvandpour, Linköping University, SE

10.30 Design and Implementation of Multi-Purpose DCT/DST-Specific Accelerator on Heterogeneous Multicore Architecture

Sajjad Nouri1, Ramin Ghaznavi-Youvalari2, Jari Nurmi1, 1 Tampere University of Technology, FI; 2 Nokia Technologies, FI

10.50 VELS: VHDL E-Learning System for Automatic Generation and Evaluation of Per-Student Randomized Assignments

Martin Mosbeck, Daniel Hauer, Axel Jantsch, TU Wien, AT

7.1 Data Converters

Chair: Timo Rahkonen, Oulu University, FI

11.10 A 10b SAR ADC with Widely Scalable Sampling Rate and AGC Amplifier Front-End

Ayca Akkaya1, Firat Celik1, Armin Tajalli2, Yusuf Leblebici1, 1 EPFL, CH;2 The University of Utah, US

11.30 Design Considerations and Evaluation of a High-Speed SAR ADC

Victor Åberg, Christian Fager, Lars Svensson, Chalmers University of Technology, SE

11.50 On the Noise Considerations of the Pulse-Shaping Based TIA Channel Designed for a Pulsed TOF Laser Radar Receiver

Aram Baharmast, Juha Kostamovaara, University of Oulu, Oulu, FI

7.2 Extra Functional Design Aspects

Chair: Maksim Jenihhin, Tallinn University of Technology, EE

Energy-Delay Trade-offs in Instruction Register File Design

Joonas Iisakki Multanen, Heikki Olavi Kultala, Pekka Olavi Jääskeläinen, Tampere University of Technology, FI

Towards Multidimensional Verification: Where Functional Meets Non-Functional

Maksim Jenihhin, Xinhui Lai, Tara Ghasempouri, Jaan Raik, Tallinn University of Technology, EE

Power Intent from Initial ESL Prototypes: Extracting Power Management Parameters

David Lemma1, Mehran Goli1, Daniel Große1,2, Rolf Drechsler1,2, 1 University of Bremen, DE;2 DFKI GmbH, DE

12.10 **Lunch**

13.15 **Invited talk: Solutions for cooler, smaller, lighter and better sounding audio products**

Mikkel Høyerby, Merus Audio, DK

14.00 **NorCAS 2019 announcement and Best Paper Award**

8.1 Power Amplifiers

Chair: Tor S. Lande, University of Oslo, NO

14.15 Low-Power Regulator for Micro Energy Harvesting Applications

Tapani Antero Nevalainen1, Esteban Ferro2, Víctor Manuel Brea2, Paula López2, Ari Paasio1, 1 University of Turku, FI, 2 Universidade de Santiago de Compostela, ES

8.2 Application-Specific Design Optimizations

Chair: Peeter Ellervee, Tallinn University of Technology, EE

GPU-enhanced Multimodal Dense Matching

Nicolai Behmann, Max Mehltretter, Sebastian P. Kleinschmidt, Bernardo Wagner, Christian Heipke, Holger Blume, Leibniz University Hannover, DE

14.35 Application Specific Integrated Gate-Drive Circuit for Driving Self-Oscillating Gallium Nitride & Logic-Level Power Transistors

Jacob Elias Fæster Overgaard, Jens Christian Hertel, Jens Pejtersen, Arnold Knott, Technical Univ. of Denmark, DK

A Low-Power Hardware Stack for Continuous Data Streaming from Telemetry Implants

Ilia Kempi, Nouman Ahmed, Andreas Hammer, Olaitan Olabode, Vishnu Unnikrishnan, Marko Kosunen, Jussi Ryynanen, Aalto University, FI

14.55 Design of Multi-Stacked CMOS mm-Wave Power Amplifiers for Phased Array Applications Using Triple-Well Process

Mohammad Hassan Montaseri, University of Oulu, FI

Implementation of an Area Efficient Crypto Processor for a NB-IoT SoC Platform

Luis Cavo, Sebastien Fuhrmann, Liang Liu, Lund University, SE

15.15 **Coffee**

9.1 Biomedical Systems

Chair: Dag T. Wisland, University of Oslo, NO

9.2 Data Processing Systems

Chair: Jari Nurmi, Tampere University of Technology, FI

15.40 Current Readout Circuit for Point-of-Care Infectious Disease Diagnostics in Animal Health

Kathy Hanley1, Aidan Murphy1, Niamh Creedon2, Alan O' Riordan2, Daniel O' Hare1, Ivan O' Connell1, 1 (MCCI), Tyndall National Institute, IE;2 (NTG), Tyndall National Institute, IE

Low-latency Packet Parsing in Software Defined Networks

Hesam Zolfaghari1, Davide Rossi2, Jari Nurmi1, 1 Tampere University of Technology, FI;2 University of Bologna, IT

16.00 High-speed Sampling System in CMOS

E. Ulvestad, K. G. Kjelgård, T. Moradi *Khanshan, D. T. Wisland, T. S. Lande. University of Oslo, NO*

Time-predictable Distributed Shared Memory for Multi-core Processors

Simon Thye Andersen, Morten Borup Petersen, Anthon Vincent Riber, Martin Schoeberl, DTU, Denmark

16.20 CMOS LIDAR for Biosensing

Tohid Moradi Khanshan, Kristian Gjertsen Kjelgård, Emil Ulvestad, Dag T Wisland, Tor Sverre Lande, University of Oslo, NO

Goal Formulation: Abstracting Dynamic Objectives for Efficient On-chip Resource Allocation

Elham Shamsa1, Anil Kanduri1, Amir M. Rahmani2,3, Pasi Liljeberg1, Axel Jantsch3, Nikil Dutt2, 1 University of Turku, Turku, FI;2 University of California, Irvine, US;3 TU Wien, AT

16.40 **Finish**