# Optimized Pulse Patterns with Bounded Semiconductor Losses

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***Abstract*—This paper proposes the computation of three-level optimized pulse patterns (OPPs) that achieve not only low harmonic load current distortions (*load-friendly* operation) but also low semiconductor losses (*converter-friendly* operation). To this end, the conduction and switching losses are modeled as a function of the OPP switching angles and the amplitude and phase of the converter current. By minimizing the current harmonics subject to an inequality constraint on the semiconductor losses, OPPs are derived that achieve minimal current distortions with a guaranteed upper bound on the semiconductor losses, thus ensuring the safe operation of the semiconductor switches within their thermal limits. Detailed numerical results for a medium-voltage system consisting of a neutral-point-clamped converter and an inductive load verify the benefits of this approach.**

***Index Terms*—Optimized pulse patterns, semiconductor losses, three-level converters, Pareto optimal solutions**

## I. Introduction

Optimized pulse patterns (OPPs) are a specific pulse width modulation (PWM) method in which the switching signal is computed offline and stored in a look-up table. Unlike selective harmonic elimination [1], [2], OPPs require formulating and solving a mathematical optimization problem [3]. Traditionally, for a given number of switching angles, the current distortions have been minimized [4]; this, in turn, ensures minimal harmonic losses in the load and achieves load-friendly operation. The influence of the commutated current on the semiconductor switching losses, however, is ignored. Therefore, the semiconductor losses are limited only indirectly by operating at a fixed switching frequency.

To solve the optimization problem underlying OPPs, a gradient-based optimization method is typically used, see [4] when applied to two-level converters. For mulilevel converters, a multitude of switching sequences arises and optimization problems are solved for each one [5], [6]. In doing so, OPPs can be computed for converters with any number of output voltage levels, including two, three, five and general $n$ levels [7].

This paper proposes the computation of OPPs that achieve not only load-friendly but also converter-friendly operation by explicitly limiting the semiconductor losses. To do so, for a given amplitude and phase of the converter current, we derive the commutated current at the switching events. We also determine the current during the time intervals in which a semiconductor switch conducts current. This enables the computation of the associated switching energy losses as well as the conduction losses as a function of the to-be-computed switching angles. The sum of the switching and conduction losses is added as an inequality constraint to the optimization problem. This allows us to compute OPPs with a guaranteed upper bound on the semiconductor losses, thus ensuring converter-friendly operation.

Two types of constraints can be added. By limiting the sum of the semiconductor losses, the converter efficiency is improved. By limiting the losses of each individual semiconductor switch, the worst-case losses are reduced and, as a consequence, the worst-case junction temperature tends to be reduced as well.

The influence of the modulation method on the semiconductor losses is well understood for continuous and discontinuous carrier-based PWM; see [8], [9] for two-level converters and [10] for three-level converters. By varying the switching frequency of carrier-based PWM within a fundamental period the switching losses can be minimized while bounding the harmonic distortions [11]. However, the literature on OPPs with minimal or bounded semiconductor losses is scarce. Single-phase OPPs are proposed in [12] that minimize (the distribution of) the semiconductor losses in a three-level active neutral-point-clamped (NPC) converter with the help of a genetic algorithm and Matlab/Simulink simulations to determine the losses. Hence, this paper aims to present the first analytical way to compute OPPs that achieve the best possible trade-off between current distortions and switching losses, thus ensuring both load- and converter-friendly operation.

The paper is organized as follows. Section II introduces and reviews conventional OPPs. The switching and conduction losses are translated into constraints in Section III, based on which Section IV formulates and solves loss-bounded optimization problems. A conclusion is provided in Section V.

## II. Conventional OPPs

Hereafter we will focus on three-level switching signals for NPC medium-voltage converters with integrated-gate-commutated thyristors. This topology is shown in Fig. 1. We refer to the active semiconductor switches as gate-commutated thyristors (GCTs). Freewheeling diodes and clamping diodes are required as passive semiconductor switches.

The work of P. Karamanakos was supported by the Research Council of Finland. The work of I. Koukoula was supported by ABB Oy Drives.

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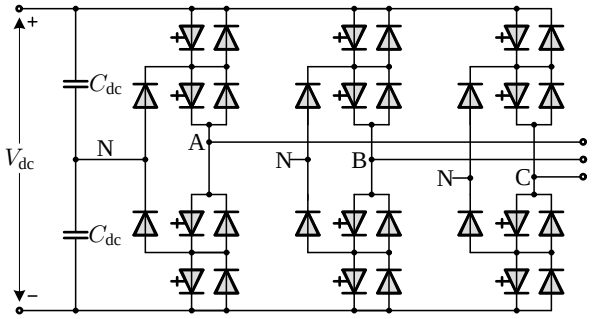



Fig. 1: Three-level neutral-point-clamped converter

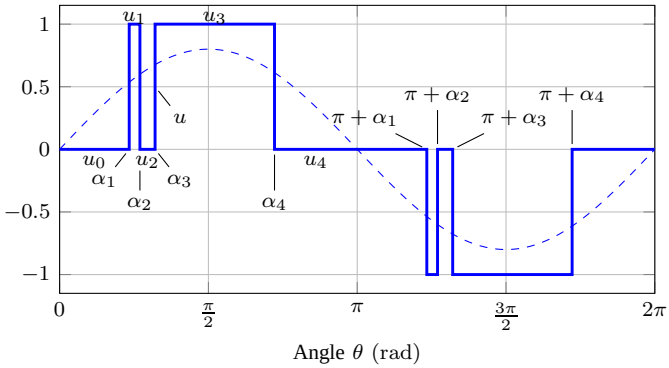



Fig. 2: Single-phase switching signal $u(\theta)$ with half-wave symmetry, modulation index $m = 0.8$ and pulse number $d = 2$

The switching frequency of the semiconductor switches is given by

$$f_{\text{sw}} = df_1\,, \tag{1}$$

where $d$ is the pulse number and $f_1$ is the fundamental frequency of the switching signal.

Two assumptions are universally made when computing OPPs. The switching signal is $2\pi$-periodic and three-phase symmetric. This implies that the pulse number $d$ is an integer. In particular, OPPs are a *synchronous* modulation method.

### A. Switching Signal

The two assumptions made above imply that three-phase OPPs are fully characterized by the single-phase switching signal $u(\theta)$ with the (integer) switch position $u \in \{-1, 0, 1\}$ and the angle $\theta \in [0, 2\pi]$ as argument. Half-wave symmetry (HWS) is imposed on the switching signal, i.e.,

$$u(\theta) = -u(\pi + \theta)\,.$$

An exemplary switching signal with HWS and pulse number $d = 2$ is shown in Fig. 2.

The single-phase switching signal $u(\theta)$ is fully defined by the switching angles $\alpha_i$ with $i \in \{1, 2, \ldots, 2d\}$ and the switch positions $u_i$ with $i \in \{0, 1, \ldots, 2d\}$. It is common practice to consider only non-negative switching signals in the positive half-wave of the fundamental period, i.e., $u(\theta) \geq 0$ for $\theta \in [0, \pi]$. This implies that the polarity of the $2d$ switch positions is non-negative as well, i.e., $u_i \in \{0, 1\}$ with $i \in \{0, 1, \ldots, 2d\}$.

The switching transition

$$\Delta u_i = u_i - u_{i-1}$$

is defined as the change in switch position at the switching angle $\alpha_i$, where $i \in \{1, 2, \ldots, 2d\}$. Because only non-negative switch positions are considered, the initial switch position $u_0$ is zero and the switching transitions are given by

$$\Delta u_i = (-1)^{i+1} \tag{2}$$

with $i \in \{1, 2, \ldots, 2d\}$.

### B. Harmonic Analysis

Owing to the $2\pi$-periodicity of the single-phase switching signal, it can be represented by the Fourier series

$$u(\theta) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left(a_n \cos(n\theta) + b_n \sin(n\theta)\right)$$

with the Fourier coefficients $a_n$ and $b_n$. The harmonic spectrum of the single-phase switching signal can be computed analytically as shown, e.g., in [13] and [14].

For HWS switching signals the Fourier coefficients

$$a_n = \begin{cases} -\dfrac{2}{n\pi} \displaystyle\sum_{i=1}^{2d} \Delta u_i \sin(n\alpha_i), & n = 1, 3, 5 \ldots \\ 0, & n = 0, 2, 4, \ldots \end{cases} \tag{3a}$$

$$b_n = \begin{cases} \dfrac{2}{n\pi} \displaystyle\sum_{i=1}^{2d} \Delta u_i \cos(n\alpha_i), & n = 1, 3, 5 \ldots \\ 0, & n = 2, 4, 6, \ldots \end{cases} \tag{3b}$$

result [13]. All harmonics of even order and the dc-offset are zero.

Often, quarter-wave symmetry

$$u(\pi - \theta) = u(\theta)$$

is imposed on the switching signal in addition to HWS. We refer to this as quarter- and half-wave symmetry (QaHWS), which leads to the Fourier coefficients [14]

$$a_n = 0, \qquad n = 0, 1, 2, \ldots \tag{4a}$$

$$b_n = \begin{cases} \dfrac{4}{n\pi} \displaystyle\sum_{i=1}^{d} \Delta u_i \cos(n\alpha_i), & n = 1, 3, 5 \ldots \\ 0, & n = 2, 4, 6, \ldots\,. \end{cases} \tag{4b}$$

QaHWS implies that the switching signal is fully defined by $d$ switching angles over $\pi/2$.

Regardless of the imposed symmetry, the amplitude $\hat{u}_n$ of the $n$th harmonic of the single-phase switching signal $u$ is given by

$$\hat{u}_n = \sqrt{a_n^2 + b_n^2}\,. \tag{5}$$

Note that the amplitude of the fundamental component $\hat{u}_1$ is equal to the *modulation index* $m$, with $m \in [0, 4/\pi]$.

### C. Voltage and Current Harmonics

The amplitude of the $n$th voltage harmonic is

$$\hat{v}_n = \frac{V_{\mathrm{dc}}}{2}\hat{u}_n\,, \tag{6}$$

where $V_{\mathrm{dc}}$ is the dc-link voltage. Assume that the converter is connected to a purely inductive load with inductance $L$ and a sinusoidal (three-phase) voltage source, such as an electrical machine with a sinusoidal back electromotive force (EMF) for which the stator resistance is neglected. For induction machines $L$ is the total leakage inductance, whereas for an (externally excited) synchronous machine $L$ refers to the subtransient inductance. Alternatively, the converter may be connected to an idealized grid; $L$ then includes the sum of the transformer and grid inductances with any resistive or capacitive components neglected.

The amplitude of the $n$th current harmonic, with $n \neq 1$, directly follows as

$$\hat{i}_n = \frac{\hat{v}_n}{n\omega_1 L}\,, \tag{7}$$

where $\omega_1 = 2\pi f_1$ is the angular fundamental frequency.[1]

### D. Objective Function

OPPs are typically computed with the aim to minimize the harmonic distortions in the load current. To this end, the total demand distortion (TDD) of the current

$$I_{\mathrm{TDD}} = \frac{1}{\sqrt{2}I_R}\sqrt{\sum_{n\neq 1}\left(\hat{i}_n\right)^2} \tag{8}$$

is considered, which is the square root of the sum of the squared current harmonic amplitudes $\hat{i}_n$ of order $n$. The current harmonic amplitudes are normalized with respect to the amplitude of the rated load current, with $I_R$ being the rms value of the rated load current.

Inserting (6) and (7) into (8) leads to

$$I_{\mathrm{TDD}} = \frac{1}{\sqrt{2}I_R\omega_1 L}\frac{V_{\mathrm{dc}}}{2}\sqrt{\sum_{n\neq 1}\left(\frac{\hat{u}_n}{n}\right)^2}\,. \tag{9}$$

We interpret (9) as $I_{\mathrm{TDD}} = c\sqrt{J}$. The constant $c$ depends on the converter and load parameters, whereas the term

$$J = \sum_{n\neq 1}\left(\frac{\hat{u}_n}{n}\right)^2 \tag{10}$$

is a function of the amplitudes of the switching signal harmonics. Minimizing the current TDD is thus equivalent to minimizing $J$, which is typically chosen as the objective function of the OPP optimization problem.

In a three-phase system, the phases $b$ and $c$ are phase-shifted by $-\frac{2\pi}{3}$ and $-\frac{4\pi}{3}$ with respect to phase $a$. Harmonics of order $n = 3, 6, 9, \ldots$, are thus in phase. These *common-mode* voltage harmonics do not drive harmonic currents in a three-phase load with a floating star point. It is therefore common practice to consider only (odd) non-triplen *differential-mode* harmonics in the objective function and to simplify (10) to

$$J = \sum_{n=5,7,11,\ldots}\left(\frac{\hat{u}_n}{n}\right)^2\,. \tag{11}$$

### E. Conventional Optimization Problem

Traditionally, OPPs have been computed such that they meet the following requirements:

- The harmonic current distortions are minimized with the assumption of a purely inductive load (with an optional voltage source).
- The amplitude of the fundamental component of the switching signal, $\hat{u}_1$, is equal to the desired modulation index $m$.
- The fundamental component has zero phase.
- The switching angles are in an ascending order; in combination with (2) this ensures that the switch positions are limited to $u_i \in \{-1, 0, 1\}$ for $i \in \{0, 1, \ldots, 4d\}$, i.e., for the whole fundamental period.

For OPPs with QaHWS this leads to the optimization problem

$$\underset{\alpha_i}{\text{minimize}} \quad \frac{16}{\pi^2}\sum_{n=5,7,11,\ldots}\frac{1}{n^4}\left(\sum_{i=1}^{d}\Delta u_i\cos(n\alpha_i)\right)^2 \tag{12a}$$

$$\text{subject to} \quad \frac{4}{\pi}\sum_{i=1}^{d}\Delta u_i\cos(\alpha_i) = m \tag{12b}$$

$$0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_d \leq \frac{\pi}{2}\,, \tag{12c}$$

where we have inserted (4) into (5) and (11) to derive the objective function (12a). The constant term $16/\pi^2$ is typically neglected and removed from (12a).

For OPPs with HWS the optimization problem is

$$\underset{\alpha_i}{\text{minimize}} \quad \frac{4}{\pi^2}\sum_{n=5,7,11,\ldots}\frac{1}{n^4}\left(\sum_{i=1}^{2d}\Delta u_i\sin(n\alpha_i)\right)^2 + \\ + \frac{1}{n^4}\left(\sum_{i=1}^{2d}\Delta u_i\cos(n\alpha_i)\right)^2 \tag{13a}$$

$$\text{subject to} \quad \frac{2}{\pi}\sum_{i=1}^{2d}\Delta u_i\cos(\alpha_i) = m \tag{13b}$$

$$-\frac{2}{\pi}\sum_{i=1}^{2d}\Delta u_i\sin(\alpha_i) = 0 \tag{13c}$$

$$0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_{2d} \leq \pi\,. \tag{13d}$$

As before the constant term $4/\pi^2$ is typically ignored in (13a). The constraint (13c) ensures that the phase of the fundamental component is zero.

[1] Note that the amplitude of the fundamental current component, $\hat{i}_1$, is given by the load and the operating point, not by (7). In case of a non-inductive load, such as a transformer with an $LC$ filter, the term $n\omega_1 L$ in (7) is to be replaced by an appropriate transfer function.

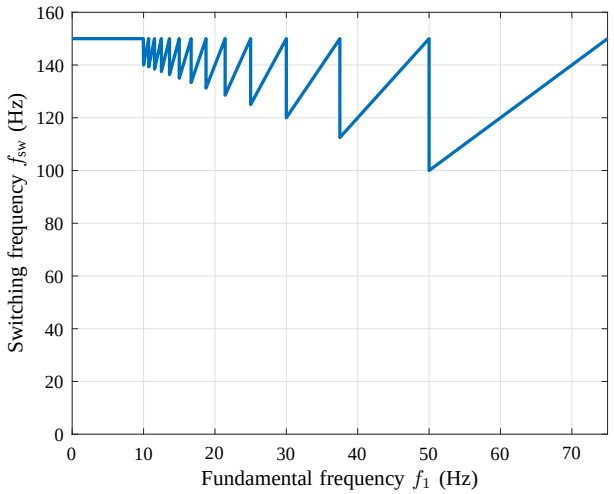



Fig. 3: Exemplary (device) switching frequency as a function of the fundamental frequency $f_1$. Above $f_1 = 10\,\text{Hz}$ OPPs with pulse numbers $d = 14$ down to $d = 2$ are used, whereas below $f_1 = 10\,\text{Hz}$ asynchronous carrier-based PWM is used. The upper bound on the switching frequency is $f_{\text{sw,max}} = 150\text{Hz}$.

### F. Limitations

Switching and conduction losses cause thermal losses in the semiconductor switches that are transferred by its housing and heatsink to the water-cooling circuitry. The heat removal capability of the latter is limited and strongly depends on the thermal resistance of the heatsink, the cooling water temperature and its flow rate. The switching losses are proportional to the commutated current, the blocking voltage and the switching frequency. The conduction losses depend on the phase current and the forward voltage. During the converter operation the semiconductor losses must be limited to avoid too high a junction temperature and a premature failure of the semiconductor switch.

The classic approach to ensure that an upper bound on the semiconductor losses is met is to limit the switching frequency below the maximum switching frequency $f_{\text{sw,max}}$. For a given fundamental frequency $f_1$, the pulse number $d$ is chosen as the largest integer so that the switching frequency is equal to or below its allowed maximum, i.e.,

$$d = \text{floor}(f_{\text{sw,max}}/f_1)\,. \tag{14}$$

OPPs being a synchronous modulation scheme, see also (1), give rise to the well-known *gear shifts* in the switching frequency. A typical switching frequency profile is provided in Fig. 3. Particularly at low pulse numbers, the switching frequency is often significantly lower than its maximum value, resulting in a poor utilization of the thermal capability of the semiconductor switches. Owing to the sinusoidal variation of the phase current and the switching losses within a fundamental period it is also apparent that the switching frequency only mildly correlates with the overall switching losses.

Clearly, the classic approach fails to fully utilize the capability of the semiconductor switches and to achieve high output currents close to the physical limits of the converter. To address this issue we propose to analytically model the semiconductor losses and to add them as an inequality constraint to the optimization problems when computing OPPs.

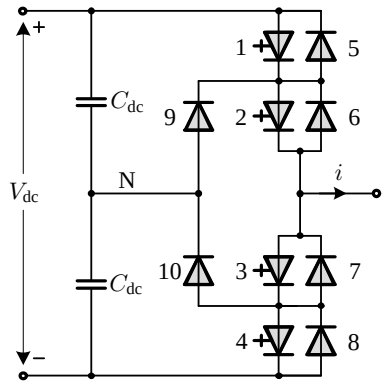



Fig. 4: Definition of the semiconductor index variable $j \in \{1, 2, \ldots, 10\}$ in a phase leg of an NPC converter

## III. Limiting the Semiconductor Power Losses

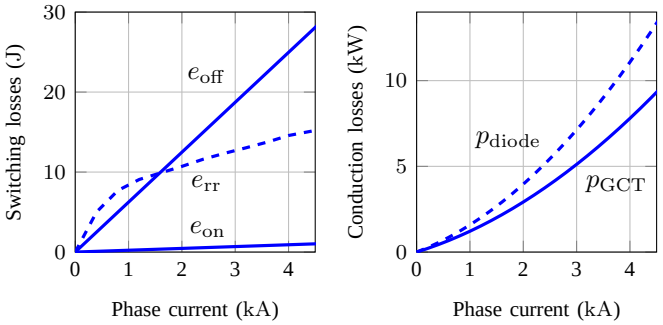
Two types of losses arise in semiconductor switches. The *switching* losses are due to the turn-on and turn-off switching transitions, whereas the *conduction* losses result from the on-state voltage of the semiconductor switches. To distinguish between the semiconductor switches, we introduce the index variable $j \in \{1, 2, \ldots, 10\}$. The indices one to four refer to the GCTs, which are the active switches, the indices five to eight correspond to the freewheeling diodes, and the indices nine and ten represent the clamping diodes, see Fig. 4.

### A. Switching Energy Losses

For the GCTs, the turn-on and turn-off losses linearly depend on the anode-cathode voltage and the anode current. In an NPC converter, the former is the half dc-link voltage, which is approximately equal to $0.5V_{\text{dc}}$ when the neutral-point potential is close to zero, and the latter is equal to the phase current $i$. With the device specific coefficients $c_{\text{on}}$ and $c_{\text{off}}$, it follows that

$$e_{\text{on}} = c_{\text{on}} 0.5 V_{\text{dc}} i \tag{15}$$

$$e_{\text{off}} = c_{\text{off}} 0.5 V_{\text{dc}} i\,. \tag{16}$$




(a) Switching energy losses (b) Conduction power losses

Fig. 5: Switching and conduction losses of the considered GCTs and diodes

| Polarity of the phase current $i$ | Switching transition | Switching energy losses |
|---|---|---|
| $> 0$ | $0 \to 1$ | $e_{1,\text{on}} + e_{9,\text{rr}}$ |
| | $1 \to 0$ | $e_{1,\text{off}}$ |
| | $0 \to -1$ | $e_{2,\text{off}}$ |
| | $-1 \to 0$ | $e_{2,\text{on}} + e_{8,\text{rr}}$ |
| $< 0$ | $0 \to 1$ | $e_{3\text{off}}$ |
| | $1 \to 0$ | $e_{3,\text{on}} + e_{5,\text{rr}}$ |
| | $0 \to -1$ | $e_{4,\text{on}} + e_{10,\text{rr}}$ |
| | $-1 \to 0$ | $e_{4,\text{off}}$ |

TABLE I: Switching energy losses in a phase leg of an NPC converter. The indices are defined in Fig. 4.

For GCTs, $c_{\text{on}}$ is typically much smaller than $c_{\text{off}}$, see Fig. 5(a).

The turn-on losses of the power diode are effectively zero, and only the turn-off losses, the *reverse-recovery* losses, are to be considered. The reverse-recovery losses

$$e_{\text{rr}} = c_{\text{rr}} 0.5 V_{\text{dc}} f_{\text{rr}}(i) \tag{17}$$

are linear in the voltage but nonlinear in the current. The coefficient $c_{\text{rr}}$ is typically bounded by $c_{\text{on}}$ and $c_{\text{off}}$. The nonlinear function $f_{\text{rr}}$ is concave and bounded by 0 and 1, see Fig. 5(a).

Consider the single-phase switching signal $u(\theta)$ with the argument $\theta = 2\pi f_1 t$, the fundamental frequency $f_1$, the time $t \in [0, T]$, and the fundamental period $T = 1/f_1$. Consider the phase current

$$i = \sqrt{2} I_R \sin(2\pi f_1 t - \phi)\,,$$

where $I_R$ is the rated rms current and $\phi$ is the displacement angle (between the fundamental voltage and the fundamental current component); a positive $\phi$ implies a lagging current.

The polarity of the phase current and the switching transition determine the current paths during the switching events and the semiconductor switches that commutate the current. This leads to eight different commutation paths in a phase leg, for which the switching energy losses can be deduced as summarized in Table I. Note that the switching energy losses $e_{j,\text{sw}}$ of the $j$th semiconductor switch, with $j \in \{1, 2, \ldots, 10\}$ as defined in Fig. 4, are either turn-on, turn-off or reverse-recovery losses.

The switching energy losses for each switching angle $\alpha_i$ then directly follow from Table I. As an example, consider $\alpha_1$ that corresponds to a switching transition from 0 to 1, and assume that it occurs when the phase current is positive. The switching energy losses are then given by $e_{1,\text{sw}}(\alpha_1) = e_{1,\text{on}}$, $e_{2,\text{sw}}(\alpha_1) = 0$, and so on.

### B. Switching Power Losses

The switching energy losses of the $j$th semiconductor switch are summed up over the $4d$ switching transitions within the fundamental period and divided by its length to obtain the *average* switching *power* losses

$$\bar{p}_{j,\text{sw}} = \frac{1}{T} \sum_{i=1}^{4d} e_{j,\text{sw}}(\alpha_i)\,. \tag{18}$$

| Polarity of the phase current $i$ | Switch position | Conduction power losses |
|---|---|---|
| $> 0$ | 1 | $p_{1,\text{con}} + p_{2,\text{con}}$ |
| | 0 | $p_{2,\text{con}} + p_{9,\text{con}}$ |
| | $-1$ | $p_{7,\text{con}} + p_{8,\text{con}}$ |
| $< 0$ | 1 | $p_{5,\text{con}} + p_{6,\text{con}}$ |
| | 0 | $p_{3,\text{con}} + p_{10,\text{con}}$ |
| | $-1$ | $p_{3,\text{con}} + p_{4,\text{con}}$ |

TABLE II: Conduction power losses in a phase leg of an NPC converter. The indices are defined in Fig. 4.

Note that a full fundamental period is required to capture the losses in the upper as well as in the lower part of the phase leg. We write $\bar{p}$ to highlight the fact that (18) refers to the average, not the instantaneous, power losses.

The sum of the switching power losses of all semiconductor switches in a phase leg is

$$\bar{p}_{\text{sw}} = \sum_{j=1}^{10} \bar{p}_{j,\text{sw}}\,. \tag{19}$$

### C. Conduction Losses

The conduction power losses of the GCTs and diodes

$$p_{\text{con}} = v_T(i) i \tag{20}$$

are a function of the on-state voltage

$$v_T = a + bi$$

with the semiconductor-specific parameters $a$ and $b$, see Table IV in the appendix, and the phase (or anode) current $i$. The conduction losses of the GCTs and the diodes are shown in Fig. 5(b) as a function of the phase current.

The conduction losses of each semiconductor switch depend on the polarity of the current and the switch position, as summarized in Table II. Two semiconductor switches always conduct current, with the inner GCTs (with indices two and three) typically burdened with the highest conduction losses.

The average conduction losses of the $j$th semiconductor switch over a fundamental period are given by

$$\bar{p}_{j,\text{con}} = \frac{1}{T} \int_0^T p_{j,\text{con}}(t)\ \mathrm{d}t = \frac{1}{2\pi} \int_0^{2\pi} p_{j,\text{con}}(\theta)\ \mathrm{d}\theta\,. \tag{21}$$

To solve (21), we split the integral into several subintegrals so that the switch position and the polarity of the phase current are constant within each subintergral. This implies that the limits of the subintegrals are given by the switching angles and the zero-crossing angles of the phase current. Only subintegrals are considered for which the specific semiconductor switch is in conduction mode.

Using Simpson's rule, an exemplary integral is given by

$$\int_{\alpha_i}^{\alpha_{i+1}} p_{j,\text{con}}(\theta)\ \mathrm{d}\theta = \frac{\alpha_{i+1} - \alpha_i}{6} \Bigg( p_{j,\text{con}}(\alpha_i) + \\ + 4 p_{j,\text{con}} \left( \frac{\alpha_i + \alpha_{i+1}}{2} \right) + p_{j,\text{con}}(\alpha_{i+1}) \Bigg),$$

where we implicitly assumed that the phase current does not change its polarity between the switching angles $\alpha_i$ and $\alpha_{i+1}$. Simpson's rule provides considerably more accurate results than the trapezoidal rule but it requires the computation of the losses at three angles instead of two, i.e., at the limits of the integral and at their mean value.

### D. Constraint

We propose to add upper bounds on the permissible semiconductor losses as inequality constraints to the OPP optimization problem.[2] This is a straightforward way to calculate OPPs with a guaranteed upper bound on the semiconductor losses. The objective function, which captures the (squared) harmonic distortions of the current remains unchanged, see (11).

By adding the constraint

$$\sum_{j=1}^{10} \left( \bar{p}_{j,\mathrm{sw}} + \bar{p}_{j,\mathrm{con}} \right) \leq p_{\max} \tag{22}$$

to the optimization problem (12) or (13) we limit the sum of the semiconductor losses by $p_{\max}$, which is the upper limit on the permissible total semiconductor losses in one phase leg. Alternatively, we may limit the semiconductor losses of each device using 10 constraints of the form

$$\bar{p}_{j,\mathrm{sw}} + \bar{p}_{j,\mathrm{cond}} \leq p_{j,\max}, \quad \forall j \in \{1, 2, \ldots, 10\}, \tag{23}$$

where $p_{j,\max}$ is the upper limit on the permissible semiconductor losses of the $j$th semiconductor switch. In both cases, the *average* losses in one phase leg over one fundamental period are constrained. Because the switching signals and phase currents of the three phases are symmetrical to each other, it suffices to consider only one phase leg.

By limiting the sum of the semiconductor losses, see (22), the converter efficiency is improved. By limiting the losses of each individual semiconductor switch, see (23), the worst-case losses are reduced and, as a consequence, the worst-case junction temperature tends to be reduced as well.

Adding these limits as inequality constraints to the OPP problems (12) and (13) reduces the search space of the permissible switching angles. In general, it is to be expected that the current distortions tend to (slightly) increase when imposing limits on the semiconductor losses. Because minimal semiconductor losses and minimal current distortion are conflicting objectives, a trade-off between the two emerges, which will be discussed in the next section.

## IV. Pareto Optimal Solutions

### A. Loss-Bounded Optimization Problems

To visualize the trade-off between semiconductor losses and current distortions we constrain the maximum semiconductor (power) losses of each device while minimizing the current TDD. To compute OPPs with bounded losses, we add the constraints (23) to the optimization problem. More specifically, for OPPs with QaHWS, we add (23) to (12), which leads to the revised optimization problem

$$\underset{\alpha_i}{\text{minimize}} \quad \frac{16}{\pi^2} \sum_{n=5,7,11,\ldots} \frac{1}{n^4} \left( \sum_{i=1}^{d} \Delta u_i \cos(n\alpha_i) \right)^2 \tag{24a}$$

$$\text{subject to} \quad \frac{4}{\pi} \sum_{i=1}^{d} \Delta u_i \cos(\alpha_i) = m \tag{24b}$$

$$0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_d \leq \frac{\pi}{2} \tag{24c}$$

$$\bar{p}_{j,\mathrm{sw}} + \bar{p}_{j,\mathrm{cond}} \leq p_{j,\max}, \forall j \in \{1, 2, \ldots, 10\}. \tag{24d}$$

Accordingly, for OPPs with HWS, we add (23) to (13) and formulate the loss-bounded optimization problem

$$\underset{\alpha_i}{\text{minimize}} \quad \frac{4}{\pi^2} \sum_{n=5,7,11,\ldots} \frac{1}{n^4} \left( \sum_{i=1}^{2d} \Delta u_i \sin(n\alpha_i) \right)^2 + \\ + \frac{1}{n^4} \left( \sum_{i=1}^{2d} \Delta u_i \cos(n\alpha_i) \right)^2 \tag{25a}$$

$$\text{subject to} \quad \frac{2}{\pi} \sum_{i=1}^{2d} \Delta u_i \cos(\alpha_i) = m \tag{25b}$$

$$-\frac{2}{\pi} \sum_{i=1}^{2d} \Delta u_i \sin(\alpha_i) = 0 \tag{25c}$$

$$0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_{2d} \leq \pi \tag{25d}$$

$$\bar{p}_{j,\mathrm{sw}} + \bar{p}_{j,\mathrm{cond}} \leq p_{j,\max}, \forall j \in \{1, 2, \ldots, 10\}. \tag{25e}$$

The average switching losses in (24d) and (25e) are computed using the exact loss models, i.e., Table I and (18). Similarly, for the average conduction losses, the exact loss models in Table II and (21) are used.

### B. Algorithm

To compute Pareto optimal solutions for a given modulation index $m$, displacement angle $\phi$, and pulse number $d$, we propose an algorithm with the following main steps:

1) We set the maximum power losses $p_{j,\max}$ in (24d) and (25e) for all 10 semiconductor switches to the same value, even though different upper bounds could be applied to the GCTs and diodes. We start with a sufficiently high value of the maximum power losses so that the constraint is not active, say 5000 W, and decrease it in small steps, e.g., by 50 W.
2) For each maximum power loss $p_{j,\max}$ the optimization problem (24) or (25) is solved to derive the optimal switching angles $\alpha_i$. To ensure that the optimal solution is found, several instances of the optimization problem are solved using random initial values for the switching angles. The result with the lowest harmonic distortions is adopted as the optimal solution.

[2] Alternatively, one could augment the objective function with a second term that captures the semiconductor losses. A weighting factor would be required to decide on the trade-off between current distortions and losses. Choosing this weighting factor proves to be cumbersome, and bounds on losses can only be achieved through trial-and-error.

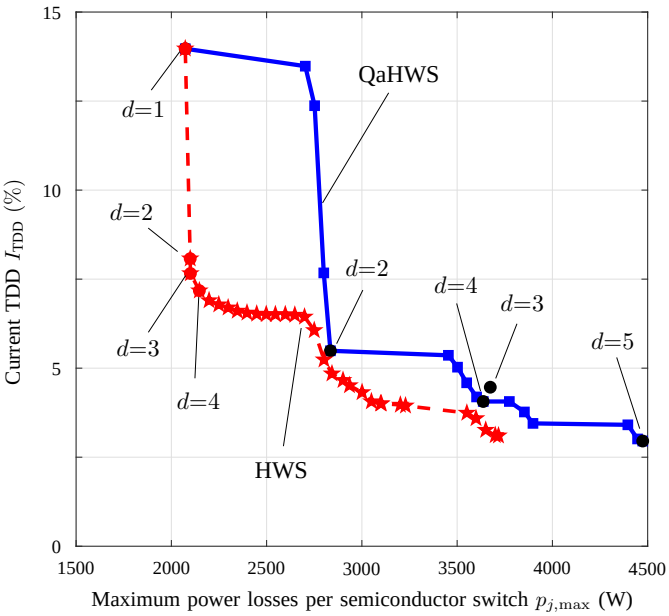



Fig. 6: Current TDD versus maximum power losses per semiconductor switch at $m = 1.15$ and $\phi = 35°$. Conventional OPPs with QaHWS and pulse numbers 1 to 5 are shown as (black) dots. Loss-bounded OPPs with QaHWS are shown as (blue) squares and loss-bounded OPPs with HWS are depicted as (red) stars. The loss-bounded OPPs use pulse number $d = 5$ and apply pulse dropping as indicated for the HWS case.

3) During the optimization process pairs of switching angles that violate a minimum pulse width requirement, e.g., of 25 µs, are removed. This leads to the dropping of pulses and a reduction of the pulse number—this characteristic will be further discussed in Section IV-E. The overall (power) losses per phase leg, the current TDD, and the modulation index are computed after a possible pulse dropping while solving the optimization problem. As a result, even when dropping pulses, the correct modulation index is preserved.

All optimization problems in this paper are nonlinear programs, for which several solvers are available. We chose the Matlab solver `fmincon` for its ease of use.

### C. Case Study

As a case study consider a medium-voltage NPC converter with the parameters summarized in the appendix. The converter could be connected to the grid or to an electrical machine. The rated converter voltage of 3.52 kV for a dc-link voltage of 5 kV implies that rated operation corresponds to the modulation index $m = 1.15$, which is considered throughout this section unless otherwise mentioned. As a typical displacement angle we assume $\phi = 35°$. The fundamental frequency is 50 Hz and the pulse number is limited to $d = 5$. This leads to a maximum switching frequency of 250 Hz, which is commonly used in medium-voltage converters.

### D. Pareto Optimal Solutions for Displacement Angle $\phi = 35°$

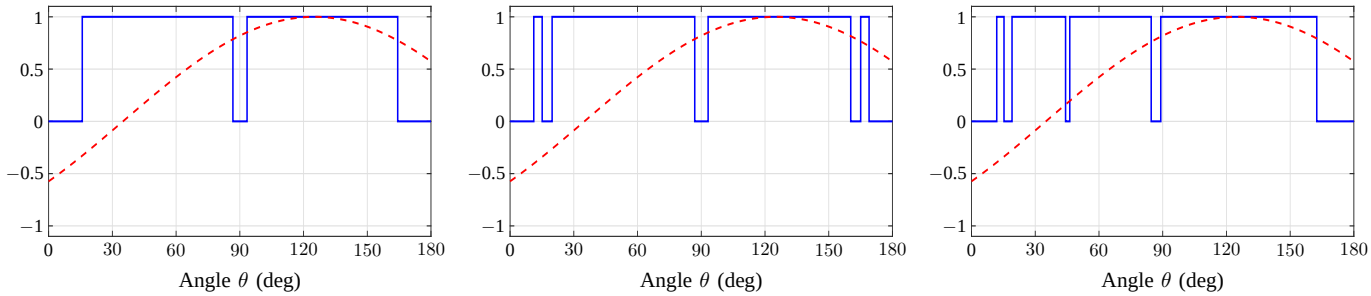
We start by solving the conventional optimization problem (12) for pulse numbers $d \in \{1, 2, \ldots, 5\}$. The current TDDs and power losses of the resulting OPPs are shown as (black) dots in Fig. 6. Assume that power losses of up to $p_{j,\max} = 3000$ W per switch were acceptable. Conventional OPPs would require us to choose the OPP with pulse number $d = 2$, which incurs losses of up to $p_{j,\max} = 2840$ W per switch and a current TDD of 5.49%. The switching waveform and phase current over 180° are shown in Fig. 7(a). Conventional OPPs with pulse numbers 3 and 4 result in losses in excess of 3640 W and are, thus, not suitable choices in our example, see Fig. 7(b). Note that pulse number $d = 4$ results in slightly lower losses as well as a lower current TDD than pulse number 3, hence the OPP with pulse number 4 is shown in Fig. 7(b).

Next, we use the algorithm of Section IV-B to solve the loss-bounded optimization problem (24) with QaHWS. This leads to the solid (blue) Pareto curve in Fig. 6, which provides a wide range of suitable combinations of current distortions and power losses. The conventional OPPs are embedded in the Pareto front. However, the loss-bounded OPPs with QaHWS do not provide a better solution than the conventional OPPs in the discussed example.

To improve the Pareto front, quarter-wave symmetry is relaxed and the algorithm is applied to the loss-bounded optimization problem (25) with HWS. The resulting Pareto optimal solutions, which are shown with the dashed (red) curve in Fig. 6, clearly outperform the OPPs with QaHWS. In particular, an OPP with $p_{j,\max} = 3000$ W and a much reduced current TDD of 4.32% is available. Even though pulse number $d = 5$ is used, the switching transitions are placed such that the switching losses are low, see Fig. 7(c).

To further highlight the benefits of loss-constrained OPPs with HWS, when compared to conventional OPPs with QaHWS, consider two cases. For the same current TDD of 4.06%, the loss-constrained OPP reduces the maximum power losses per semiconductor switch by 16% from 3630 W to 3050 W. Alternatively, for the same maximum power losses of 3630 W, the loss-constrained OPP reduces the current TDD by 20% from 4.06% to 3.26%, see Fig. 6.

Fig. 8 provides further insight into the loss-bounding methodology by comparing the semiconductor losses of a conventional OPP with that of a loss-bounded OPP. The 10 individual semiconductor switching and conduction losses are shown for one phase leg. As is commonly the case when operating at low displacement angles and at high modulation indices, the outer GCTs incur the highest switching losses, see Fig. 8(a). The three switching transitions between 150° and 180°, see Fig. 7(b), significantly contribute to these losses, as can be read out from Table I. Bounding the losses of the semiconductor switches moves, in effect, these switching transitions close to where the phase current is zero, see Fig. 7(c). As a result, the loss-bounded OPP reduces the switching losses of the outer GCTs from 2410 W to 1770 W, see Fig. 8(a). Consequently, the total losses are reduced from 3640 W to 3000 W as the conduction losses remain effectively the same, see Fig. 8(b). This, however, occurs at the expense of a slight increase in the current TDD from 4.06% to 4.32%. The losses of the inner GCTs and freewheeling diodes (indices 5

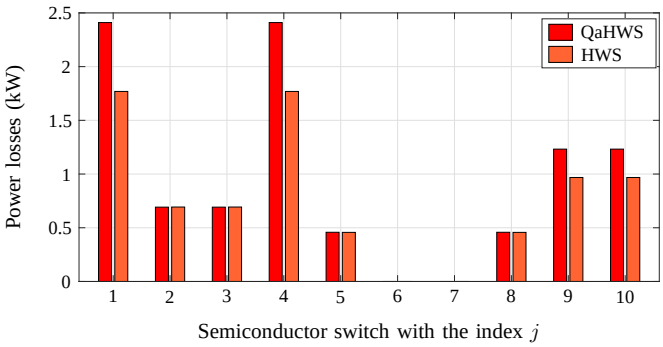



(a) Conventional OPP with QaHWS and $d = 2$: $I_{\text{TDD}} = 5.49\%$ and $p_{j,\max} = 2840\,\text{W}$

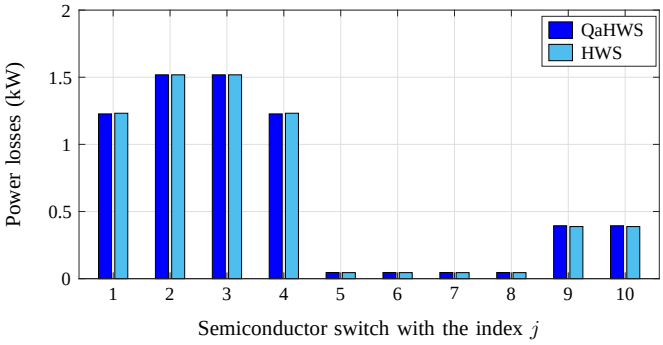
(b) Conventional OPP with QaHWS and $d = 4$: $I_{\text{TDD}} = 4.06\%$ and $p_{j,\max} = 3640\,\text{W}$

(c) Loss-bounded OPP with HWS and $d = 5$: $I_{\text{TDD}} = 4.32\%$ and $p_{j,\max} = 3000\,\text{W}$

Fig. 7: Switching waveforms and phase currents of three exemplary OPPs at $m = 1.15$ and $\phi = 35°$




(a) Switching losses




(b) Conduction losses

Fig. 8: Switching and conduction losses per semiconductor switch at $m = 1.15$ and $\phi = 35°$. The indices 1 to 10 refer to the GCTs, freewheeling diodes and clamping diodes as defined in Fig. 4. Conventional (unconstrained) OPPs with QaHWS and $d = 4$ ($I_{\text{TDD}} = 4.06\%$ and $p_{j,\max} = 3640\,\text{W}$), see Fig. 7(b), are considered alongside loss-bounded OPPs with HWS and $d = 5$ ($I_{\text{TDD}} = 4.32\%$ and $p_{j,\max} = 3000\,\text{W}$), see Fig. 7(c).

to 8) are unaffected, whereas the losses of the clamping diodes (indices 9 and 10) are also reduced.

### *E. Pulse Dropping*

For the loss-bounding algorithm in Section IV-B to be effective, a relatively high pulse number is required so as to provide the optimizer with a sufficient degree of freedom to achieve low current distortions despite bounded losses. This

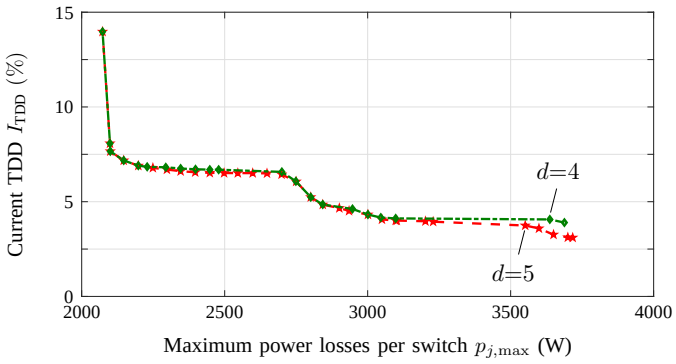


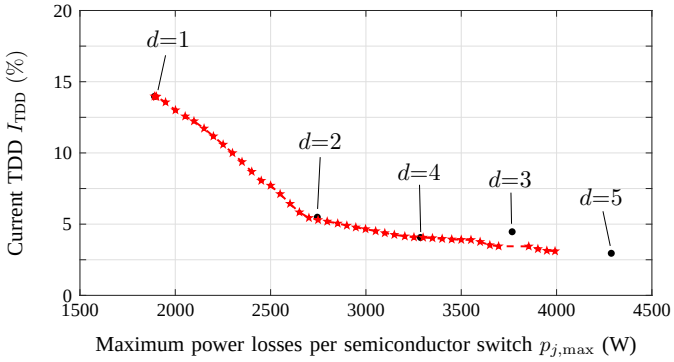

Fig. 9: Current TDD versus maximum power losses per semiconductor switch at $m = 1.15$, $\phi = 35°$ for HWS OPPs with $d = 4$ and $d = 5$. Loss-bounded OPPs with HWS for $d = 4$ are depicted as (green) rhombi and for $d = 5$ as (red) stars.

can be seen in Fig. 9 for OPPs with HWS. The higher degree of freedom that pulse number 5 offers improves the Pareto solutions when fairly high semiconductor losses are tolerated, here above 3500 W. For lower losses, however, the tighter constraints limit the search space and fewer degrees of freedom suffice to establish the Pareto optimal solutions.

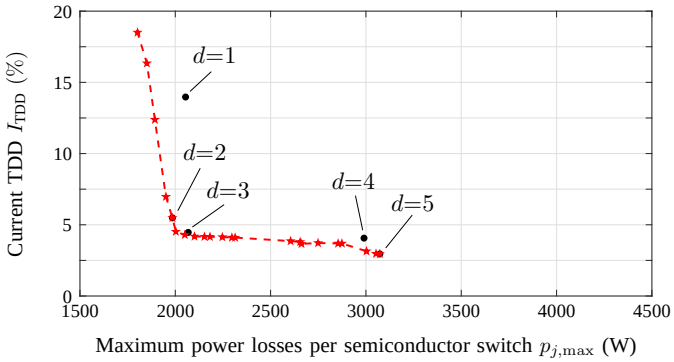
Pairs of switching angles that would result in suboptimal or infeasible solutions are placed by the optimizer in the vicinity of the displacement angle, where the switching losses are effectively zero. Pulses of close-to-zero width, e.g., of less than 25 µs width, do not reduce the current distortions but increase the switching losses, hence they are removed in the optimization procedure by imposing a minimum pulse width requirement. This, in effect, achieves the dropping of pulses when the power loss constraints are active. Pulse dropping is exemplified in Fig. 6 for the Pareto optimal solutions with HWS that were computed with pulse number $d = 5$; when the power loss constraint is tightened below 2200 W, the effective pulse number drops step by step from 4 down to 1, as shown in the figure.

### *F. Pareto Optimal Solutions for a Range of Displacement Angles and Modulation Indices*

The Pareto optimal solutions discussed in the previous sections were limited to modulation index $m = 1.15$ and




(a) $\phi = 0°$




(b) $\phi = 90°$

Fig. 10: Current TDD versus maximum power losses per semiconductor switch at $m = 1.15$ for displacement angles $\phi = 0°$ and $\phi = 90°$. Conventional OPPs with QaHWS are shown as (black) dots, and loss-bounded OPPs with HWS are depicted as (red) stars for pulse numbers up to $d = 5$.

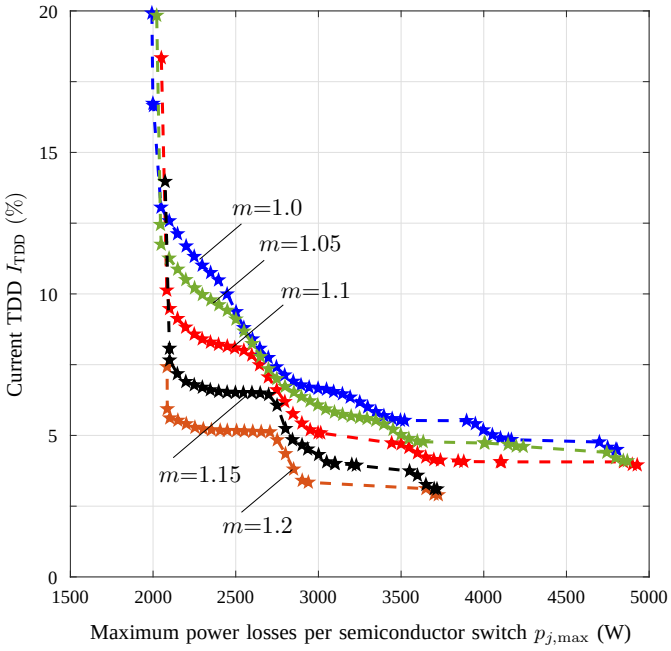



Fig. 11: Current TDD versus maximum power losses per semiconductor switch at modulation indices $m \in \{1.0, 1.05, 1.1, 1.15, 1.2\}$ for $\phi = 35°$ and HWS OPPs with $d = 5$.

displacement angle $\phi = 35°$. To widen the analysis, additional modulation indices and displacement angles are investigated in this section.

We start by considering the displacement angles $\phi = 0°$ and $\phi = 90°$ for the (previously used) modulation index $m = 1.15$. More specifically, conventional OPPs with QaHWS are compared with loss-bounded HWS OPPs in Fig. 10. The loss-bounded HWS OPPs provide solutions for a wide range of maximum power losses, whereas conventional OPPs offer only a few solutions at discrete pulse numbers. Pulse number $d = 1$ of the conventional OPP is a particularly poor choice at the displacement angle $\phi = 90°$ due to its combination of high current TDD and high switching losses. The latter result from the fact that the single switching transition occurs when the phase current is at its peak (for $\phi = 90°$). In contrast, loss-bounded HWS OPPs mitigate this issue by offering additional switching transitions placed at low phase currents, thus lowering the switching losses as well as the current TDD.

Next, we vary the modulation index between 1 and 1.2 in steps of 0.05. The Pareto optimal solutions are shown in Fig. 11 for loss-bounded OPPs with HWS and the displacement angle $\phi = 35°$. When increasing the modulation index from $m = 1.0$ to $m = 1.2$ the current distortions are reduced for a given maximum power loss, say 3000 W. Similar observations can be made when considering the current distortion for a given pulse number, see, e.g., Figs. 6 and 10 in [13]. As such, operation at $m = 1.2$ is particularly attractive; beyond $m = 1.22$, however, the current TDD quickly increases when approaching the modulation index of $4/\pi$.

## V. Conclusion

This paper pioneered the computation of loss-bounded OPPs by modeling and constraining the switching and conduction losses of each semiconductor switch in the optimization problem. As shown and analyzed in depth, by adopting the proposed systematic approach, OPPs that improve the trade-off between load current harmonic distortions and power losses can be computed. As a result, OPPs with bounded semiconductor losses are not only load-friendly (by minimizing the current distortions) but they also achieve converter-friendly operation by limiting the thermal stress on the semiconductor switches. To maximize the efficiency of the inverter, a constraint on the sum of the semiconductor losses can also be imposed, see (22). A detailed analysis of the benefits of doing so shall be presented in a follow-up publication.

## Appendix

The parameters of the considered NPC converter system are provided in Table III. We define a per unit system using the base current $I_B = \sqrt{2} I_R$, the base voltage $V_B = \sqrt{\frac{2}{3}} V_R$ and the base angular frequency $\omega_B = \omega_R$. In this per unit system the load inductance is 0.255 per unit.

As semiconductor switches we consider the 5SHY 4045L0004 GCT [15], which is produced by Hitachi Energy,

| Parameter | Symbol | SI value |
|---|---|---|
| Rated converter (line-to-line) output voltage | $V_R$ | $3520\,\mathrm{V}$ |
| Rated converter phase current | $I_R$ | $2200\,\mathrm{A}$ |
| Angular fundamental frequency | $\omega_R$ | $2\pi 50\,\mathrm{rad/s}$ |
| Dc-link voltage | $V_{\mathrm{dc}}$ | $5\,\mathrm{kV}$ |
| Load inductance | $L$ | $0.750\,\mathrm{mH}$ |

TABLE III: Parameters of the converter and its load

| GCT 5SHY 4045L0004 | Diode D1961 SH45TS02 |
|---|---|
| $e_{\mathrm{on}} = 1.029\,\mathrm{J}$ | |
| $e_{\mathrm{off}} = 28.08\,\mathrm{J}$ | $e_{\mathrm{rr}} = 15.2\,\mathrm{J}$ |
| $a_{\mathrm{GCT}} = 0.97\,\mathrm{V}$ | $a_{\mathrm{diode}} = 1.19\,\mathrm{V}$ |
| $b_{\mathrm{GCT}} = 0.245\,\mathrm{mV/A}$ | $b_{\mathrm{diode}} = 0.395\,\mathrm{mV/A}$ |

TABLE IV: Semiconductor parameters for the loss calculations

and the Infineon D1961 SH45TS02 diode [16]. These semiconductor switches are optimized towards low conduction losses (but incur high switching losses) and are therefore a suitable choice when operating at high currents and low switching frequencies. Their parameters are provided in Table IV; the typical on-state voltage and the maximum switching losses are considered at the maximum rated values of $v_T = 2.4\,\mathrm{kV}$ and $i_T = 4.5\,\mathrm{kA}$. Operation at the maximum junction temperature is assumed, which is $125\,^{\circ}\mathrm{C}$ for the GCTs and $135\,^{\circ}\mathrm{C}$ for the diodes.

The loss coefficients $c_{\mathrm{on}}$, $c_{\mathrm{off}}$ and $c_{\mathrm{rr}}$ in (15)–(17) can be easily computed from Table IV; the turn-off loss coefficient, for example, is given by

$$c_{\mathrm{off}} = \frac{e_{\mathrm{off}}}{v_T i_T} = 2.6\,\frac{\mu\mathrm{J}}{\mathrm{V\,A}}.$$

The switching energy losses and the conduction power losses for the chosen semiconductor switches are shown in Fig. 5 as a function of the phase current.

## ACKNOWLEDGMENTS

The authors would like to thank and acknowledge Annika Birth and Hendrik du Toit Mouton for their initial Matlab implementation and results towards achieving loss-bounded OPPs.

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