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POWER CONVERTER TOPOLOGIES FOR ENERGY STORAGE INTEGRATION

Master of Science Thesis
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ABSTRACT

Vilma Hanhela: Power Converter Topologies for Energy Storage Integration
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Renewable energy production is being installed faster than ever. This creates problems in the transmission grid since the generated power is fluctuating due to the intermittent nature of renewable energy sources. As a solution, an energy storage system could store the excess energy when it is being produced and supply it back to the grid when momentary demand exceeds the production. This thesis addresses this problem by proposing an energy storage system. In this system, a supercapacitor works as an energy storage element and is integrated into a submodule of a modular multilevel converter (MMC) through a dc-dc converter. This bidirectional energy storage system can supply and absorb active and reactive power.

An MMC consists of several submodules connected in series. In this thesis, a configuration is examined where a string of supercapacitors is connected to each submodule. The supercapacitor is proposed as an energy storage element due to its numerous advantages, such as high power density, high efficiency, and longer lifetime than batteries. These make it suitable for high-power applications such as the proposed bidirectional energy storage system.

A bidirectional buck-boost dc-dc converter drastically improves the operation of the energy storage system connected to the MMC submodule. It has the capability of manipulating the power flow and the supercapacitor state of charge. This is achieved by increasing and decreasing voltage levels depending on whether the supercapacitor is charging or discharging.

To ensure the supercapacitor is able to absorb and supply the desired amount of energy of 1 MJ, the supercapacitor string and the dc-dc converter as well as the control system are designed. In this thesis, the number of supercapacitor modules required to produce at least 1 MJ of energy is calculated. Design objectives also included relatively low switching frequency and the aim to keep the cost down by using the smallest possible number of supercapacitors. The effective operation of the proposed design was verified with simulations.

Keywords: M.Sc. thesis, dc-dc converter, supercapacitor, modular multilevel converter, energy storage system.

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TIIVISTELMÄ

Vilma Hanhela: Tehonmuunnintopologiat energian varastoinnissa
Diplomityö
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Sähkötekniikan DI-tutkinto-ohjelma
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Uusiutuvaa energiaa tuotetaan ja asennetaan enemmän kuin ikinä. Tästä seuraa ongelmia sähköverkkoon, sillä energian tuotanto ei ole jatkuvaa ja tasaista, vaan tehoa saadaan vain, kun aurinko paistaa tai tuulee. Energia varastointijärjestelmä kykenisi varastoimaan tuotettua energiaa, kun sitä on saatavilla ja syöttämään sitä takaisin verkkoon, kun tarve on suurin. Tässä diplomityössä on pyritty vastaamaan tähän ongelmaan ehdotamalla ratkaisusksi energianvarastiontijärjestelmää. Energiavarastona toimiva superkondensaattori kytketään dc-dc-muuntimen avulla modulaariseen monitasomuuntimeen, (engl. modular multilevel converter, MMC). Tämän kahteen suuntaan toimivan energianvarastointijärjestelmän avulla on mahdollista syöttää ja purkaa pätö- ja loistehoa.

MMC koostuu useasta sarjaan kytketystä submoduulista. Tässä diplomityössä tutkitaan konfiguraatiota, jossa useampi superkondensaattorimoduuli on kytketty sarjaan ja tämä superkondensaattorirypäs on liitetty MMC:n submoduuliin. Superkondensaattori on valittu energianvarastointijärjestelmäksi sen lukuisten hyötyjen takia. Suuren tehotiheytensä sekä hyvän hyötysuhteensa ansiosta superkondensaattori soveltuu hyvin korkeatehoisiin systeemeihin, kuten ehdotettuun kaksisuuntaiseen energianvarastointijärjestelmään.

Energianvarastointijärjestelmän toiminnan parantamiseksi superkondensaattori on kytketty dc-dc muuntimen avulla MMC:n submoduuliin. Dc-dc-muunnin parantaa järjestelmän toimintaa huomattavasti ja se pystyy nostamaan tai laskemaan jännitettä riippuen ladataanko vai puretaanko energiavarastoa. Dc-dc-muuntimen toimintaa analysoidaan yksityiskohtaisesti simulaatioiden avulla.

Tässä työssä energianvarastointijärjestelmän toiminnan varmistamiseksi on suunniteltu dc-dc-muunnin ja ohjausjärjestelmä. Näin pystytään varmistamaan, että superkondensaattori kykenee varastoimaan ja purkamaan 1 MJ energiaa. Tavittavien superkondensaattorimoduuleiden määrä on laskettu. Suhteellisen pienet taajuudet sekä kustannukset on varmistettu laskemalla pienin tarvittava superkondensaattorimoduulien määrä. Järjestelmlän tehokas toiminta on todennettu simuloimalla.

Avainsanat: diplomityö, dc-dc-muunnin, superkondensaattori, modulaarinen monitasomuunnin, energianvarastointijärjestelmä.

PREFACE

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LIST OF SYMBOLS AND ABBREVIATIONS

Acronyms

ac	alternating current
CCM	continuous conduction mode
DAB	dual-active bridge
dc	direct current
DSBC	double-star bridge cell
EDLC	electric double layer capacitor
emf	electromotive force
ESE	energy storage element
ESR	equivalent series resistance
ESS	energy storage system
FB	full bridge
FWD	anti-parallel freewheeling diode
HB	half bridge
IGBT	insulated-gate bipolar transistor
Li-ion	Lithium-ion
MMC	modular multilevel converter
MPC	model predictive control
PCC	point of common coupling
PI	proportional-integral
PWM	pulse width modulation
SC	supercapacitor
SDBC	single-delta bridge cell
SM	submodule
SOC	state of charge
SSBC	single-star bridge cell
STATCOM	static synchronous compensator
TIM	thermal interface material
VSC	voltage source converter
ZN	Ziegler–Nichols method

Symbols

c_{off}	IGBT turn-off coefficient
c_{on}	IGBT turn-on coefficient
c_{rr}	diode reverse recovery coefficient
C_{sc}	supercapacitor capacitance
e_{off}	turn-off energy losses
e_{on}	turn-on energy losses
e_{rr}	reverse recovery energy losses
E_{sc}	supercapacitor energy
d	duty cycle
D_1	upper IGBT freewheeling diode
D_2	lower IGBT freewheeling diode
Δi_{L}	peak-to-peak inductor current
f_{sw}	switching frequency
f_{rr}	nonlinear reverse recovery frequency function
I_{L}	inductor current
$I_{\text{peak,max}}$	supercapacitor maximum peak current
I_{ref}	supercapacitor current reference
I_{sc}	supercapacitor current
I_{T}	anode current
K_{i}	integral gain
K_{p}	proportional gain
K_{u}	ZN ultimate gain
L_{arm}	arm inductance
N_{P}	number of supercapacitor modules in parallel
N_{S}	number of supercapacitor modules in series
$P_{\text{converter}}$	bidirectional dc-dc converter power
P_{ref}	converter power reference
P_{sc}	supercapacitor power
$R_{\text{self,dis}}$	self-discharge resistance
$S_{1,2,..,\text{n}}$	submodule switch or dc-dc converter switch
$T_{\text{j,max}}$	maximum junction temperature
$T_{\text{j,min}}$	minimum junction temperature
t_{on}	switch on-time
t_{off}	switch off-time
t_{sw}	switching period
t_{u}	time period of ZN oscillations
V_{dc}	dc link voltage
$V_{\text{sc,ini}}$	initial supercapacitor voltage
$V_{\text{sc,max}}$	maximum supercapacitor voltage
$V_{\text{sc,min}}$	supercapacitor minimum voltage
v_{T}	anode-cathode voltage

1 INTRODUCTION

An increase in renewable energy generation means fewer synchronous rotating machines and increasingly fluctuating power generation in the transmission grid. Traditional synchronous generators, found for example in coal-fired power plants are replaced with power electronics-based generators, such as photovoltaic and wind power. Fluctuating power generation leads to voltage fluctuations, and the reduction of synchronous generators leads to reduced frequency stability due to the reduction of inertia. Voltage and frequency stability are mandatory for the grid to maximize active power transfer and to ensure that the grid can withstand transient faults and switching operations without becoming unstable. Instability would lead to voltage collapse and large blackouts. Improvement of the power transmission network is required [2].

Energy storage systems (ESSs) can provide support to the transmission grid. Traditionally, ESSs have been operated at low dc voltages. Energy storage elements (ESEs) have been connected to the transmission grid through 2- or 3-level converters [3]. ESEs are usually connected in series into a dc link of the converter, leading to a significant risk of failure if one ESE fails. In addition, traditional systems, such as 2-level converters need large passive components like filters. Maintaining high powers with such systems requires multiple ESEs to be connected in parallel, which increases complexity [3]. Modular multilevel converter (MMC) provides an alternative solution that can replace traditional ESS.

The MMC consists of branches, each of which has several submodules (SMs) connected together with an inductor. Series connection of SMs ensures high voltage output, as seen in Fig 1.2. One branch is made up of tens to hundreds of SMs, and hence the achievable magnitude of the output voltage is proportional to the number of SMs. Modular design allows high efficiency (99 %), modularity, and high power to be transferred to the grid. The modularity allows the output to be scaled at the desired voltage level. A step-up transformer is used when MMC is connected to a high-voltage transmission network to reduce the number of required SMs when GVA-level power output is not required. [2]

This thesis presents and analyzes power converter topologies for energy storage integration. ESEs can be integrated into the MMC SM through a dc-dc converter along with a suitable control scheme. In addition, a suitable bidirectional dc-dc converter is presented and the schematics and buck and boost operation for the proposed con-

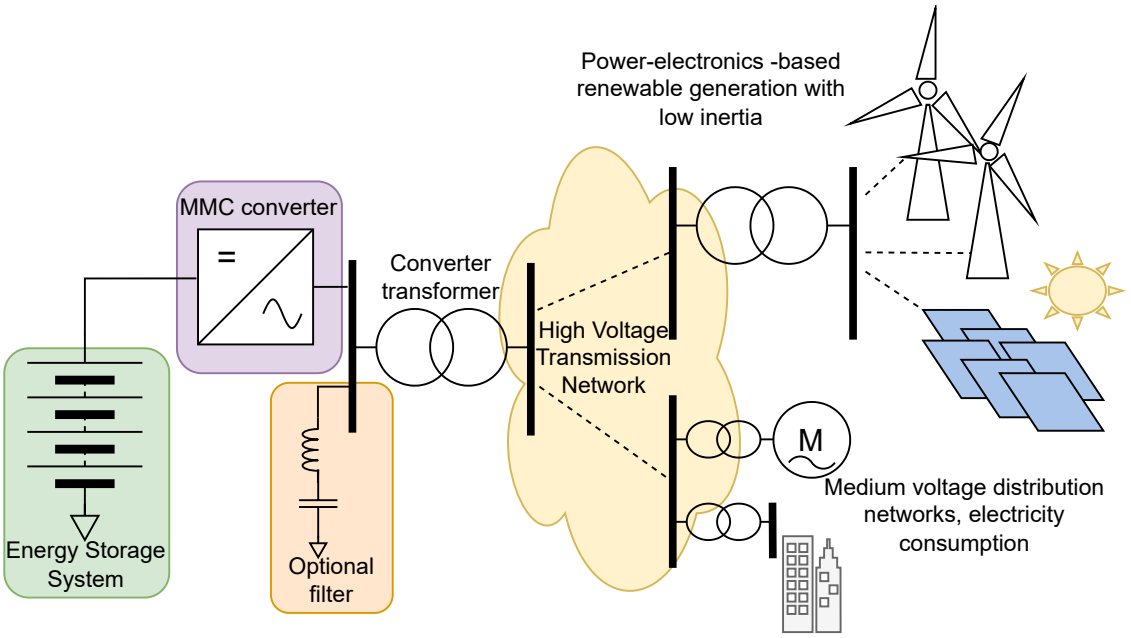

Figure 1.1 *ESS integrated into a weak high voltage transmission network, susceptible to collapse due to significant amounts of power-electronics-based renewable generation and long transmission lines.*

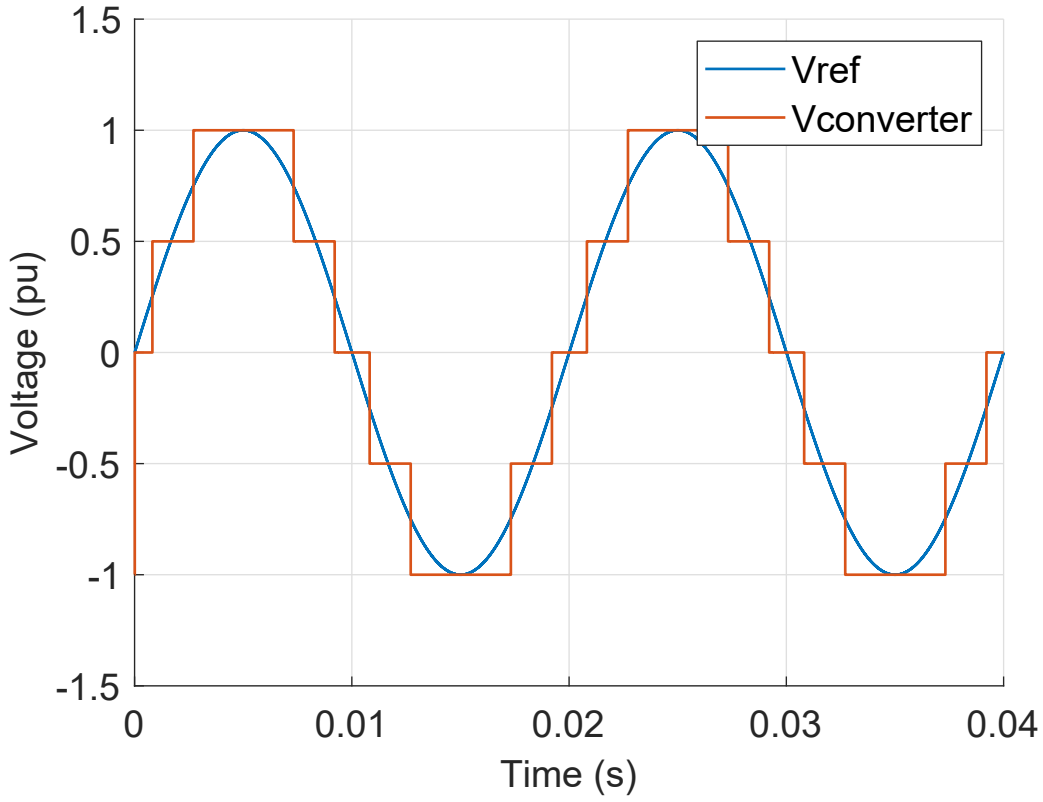

Figure 1.2 *Output voltage waveform of a modular multilevel converter compared to the reference voltage.*

verter are analyzed. A visual concept of ESS integration to the transmission grid is presented in Fig. 1.1.

This thesis is structured as follows. Chapter 2 covers the basics of power converter topologies for energy storage integration. Such as common MMC topologies. The benefits and disadvantages of distributed and centralized energy storage systems are analyzed. In addition, different kinds of potential technical solutions for energy storage elements are compared. In Chapter 3 the operation principle of a supercapacitor is discussed, and different supercapacitor modules are analyzed. Dc-dc converter and control are discussed in detail in Chapter 4. Chapter 5 discusses the thermal parameters and losses of insulated-gated bipolar transistors (IGBTs), which is a switching component widely used in high-power converters. Chapter 6 presents and analyzes the simulation results and Chapter 7 draws the conclusions of this thesis and discusses future research.

2 MMC TOPOLOGIES

2.1 Modular Multilevel Converter

The MMC is a multilevel voltage source converter used in medium to high-voltage applications. Nowadays, the MMC is considered to be the most advanced configuration for such applications. MMCs can transfer high powers i.e., hundreds of MVA to the power grid with high redundancy which contributes to high fault tolerance. The MMC has benefits over traditional multilevel converters, such as the ability to add voltage levels without increasing the complexity significantly. Modularity reduces the voltage stress of the switches and the switching frequency is also reduced. In addition, multiple voltage levels reduce the voltage harmonics and the current harmonics. This means that the line (harmonic) filter can be reduced, or totally removed, while it is easier to meet the grid standards at the point of common coupling. [2]

Four MMC configurations are considered for further investigation in this overview. The MMC can be in a star (single-star bridge cell SSBC) configuration or in a delta (single-delta bridge cell SDBC). Another MMC configuration is the double-star, which can be divided into a chopper cell converter (double-star chopper cell DSCC) and full-bridge cells (double-star bridge cell DSBC). All aforementioned MMC variants are very attractive configurations. Their operations for energy storage integration are investigated more closely in the sections below.

2.2 MMC Topologies

When the performance of all four aforementioned MMC configurations is based on theoretical limits of volume and efficiency of the power conversion, the power losses can be considered comparable. SSBC and SDBC MMCs have the lowest power losses since they need smaller capacitor volumes [1]. Two split arms in double-star MMCs introduce a dc offset in the voltage. In practice, arms in the double-star configurations are exposed to larger power fluctuations than the arms in the SSBC and SDBC MMC configurations [1]. However, a centralized string of ESEs cannot be connected to SDBC, due to the delta configuration. A comparison between the three MMC topologies is seen in Table 2.1.

The SSBC MMC consists of full-bridge type SMs as positive and negative voltages are required for the operation [3]. However, also SSBC configuration has the disadvantage that connecting a centralized string of ESEs is not feasible. It might

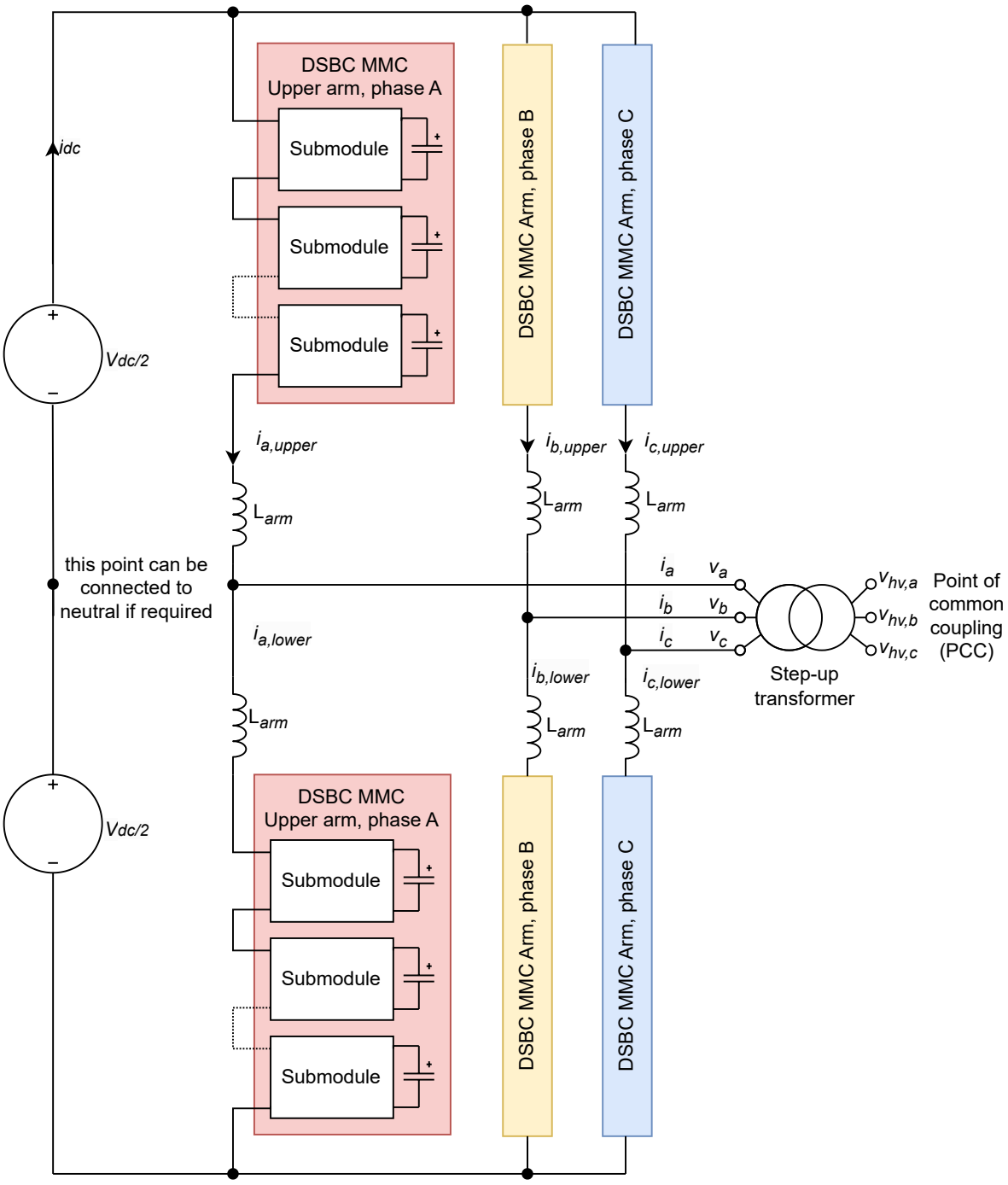

Figure 2.1 *Double-star MMC.*

be envisioned, that it could be connected between the start-point of the SSBC configuration and the transformer (star-connected) secondary ground. In practice, this is not possible since this would lead to the ESE dc current flowing through the transformer windings, which would saturate the current.

Double-star MMC configurations, see Fig. 2.1 consist of branches that have an

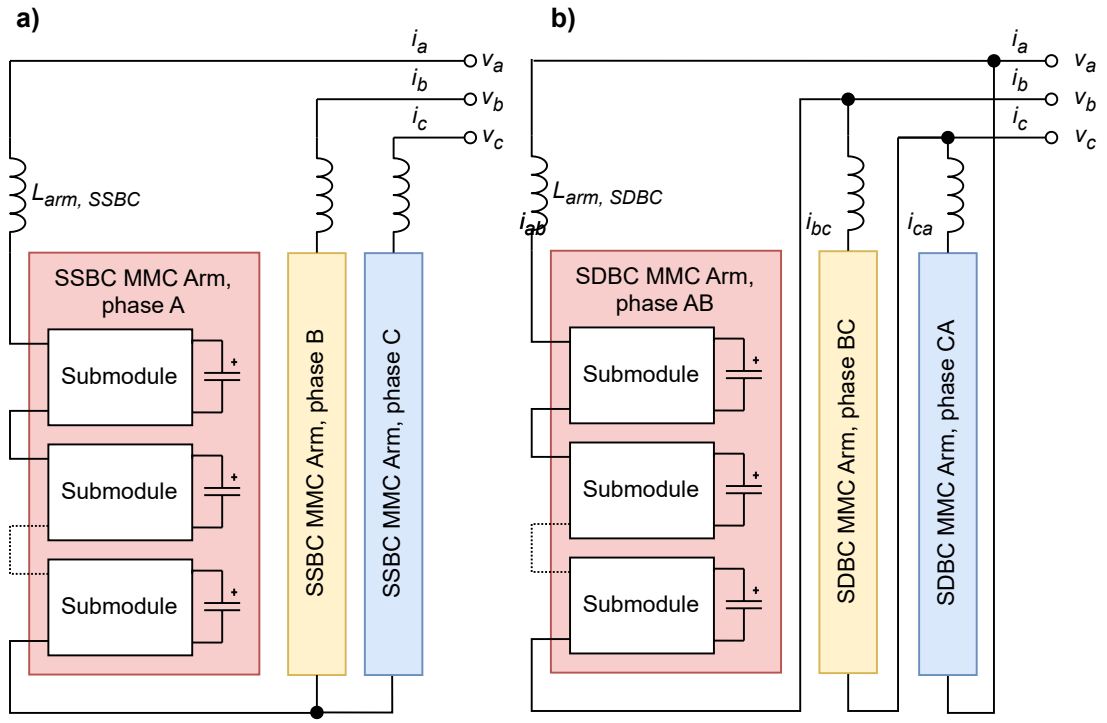

Figure 2.2 *Single-star a) and single-delta b) MMCs. Adapted from [1]*

upper and lower arm that consist of series connected identical SMs and an arm inductor L_{arm}, which reduces harmonics in the circulating currents [4]. Correspondingly, DSCC and DSBC configurations have an arm inductor, which is capable of limiting possible fault currents. DSCC and DSBC have six branches divided into two arms whereas SSBS and SDBC configurations have three branches, as seen in Fig. 2.2. Single-star and single-delta configurations have one arm only. The power output of double-star MMC can be controlled independently from the power fed to the grid and the power fed to ESEs [1].

2.3 Comparison of Full- and Half-Bridge Submodules

The SM in MMC can be achieved by using full-bridge (FB) SMs (also known as H-bridge) or half-bridge (HB) SMs, as seen Fig. 2.3. Both types have a small capacitor and both SMs can be supplied by a dc-voltage source. Positive voltage in HB is achieved by turning on the upper switch S_1 and zero voltage is achieved by tuning on the lower switch S_2. In FB-SMs, positive and negative voltage levels can be achieved by charging the capacitor in both directions. This can be done by turning on switches S_1 and S_4 or S_2 and S_3. Zero voltage is achieved when the capacitor is bypassed by turning on upper switches at the same time or lower switches at the same time. In both SM types, connecting several SMs in series increases the converter output voltage.

Table 2.1 *Comparison of MMC topologies. The benefits of each technology are shown in green and the downsides in red. Items, where ranking cannot be done between competing technologies are shown in orange font.*

DSCC	DSBC	SSBC	SDBC
Centralized dc link where ESEs can be added.	Centralized dc link where ESEs can be added	No dc link for additional ESEs.	No dc link for additional ESEs.
ESEs can be both distributed on the SM level or centralized in the dc link.	ESEs can be both distributed on the SM level or centralized in the dc link.	Distributed ESEs result in large oscillating components.	Distributed ESEs result in large oscillating components.
Large cost and volume for capacitors, since arms are exposed to larger power fluctuation. (When the performance of all four MMC configurations is comparable based on theoretical volume limits.)	Largest cost and volume for capacitors. (When the performance of all four MMC configurations is comparable based on theoretical volume limits.)	Small capacitor volumes and costs. (When the performance of all four MMC configurations is comparable based on theoretical volume limits.)	Small volume and cost for capacitors. (When the performance of all four MMC configurations is comparable based on theoretical volume limits.)
Potentially only one dc-dc converter.	Potentially only one dc-dc converter.	Requires dc-dc converter between each SM and ESE.	Requires dc-dc converter between each SM and ESE.
High initial costs and large footprint with comparable system efficiency.	High initial costs and large footprint with comparable system efficiency.	Low initial costs and small footprint with comparable system efficiency.	Low initial costs and small footprint with comparable system efficiency.

Using FB-SMs in double-star configuration results in a considerable decrease in the required number of SMs if the same power flow is required from HB-SMs and FB-SMs [5]. HB allows each SM to generate only two voltage levels instead of three in FB-SMs, but the number of semiconductor devices is halved. This leads to lower losses per SM and thus HB-SM is the most efficient of the two SM types [6]. However, if the number of SMs is decreased so that HB-MMC and FB-MMC produce the same output power, FB-MMC has lower switching losses with lower volume. FB-MMC requires much fewer SMs and this can potentially lower the costs. In addition, the capacitor voltage ripples are reduced. Thus FB-MMC is a good option, especially in such applications as the STATCOM [7].

Table 2.2 *Comparison of full- and half-bridge submodules. The benefits of each technology are shown in green and downsides in red.*

Half-bridge	Full-bridge
Number of SM semiconductor devices is halved.	Double the number of SM semiconductor devices.
Lower SM power losses.	Larger SM power losses.
Higher MMC power losses.	Lower MMC power losses.
Two voltage levels.	Three voltage levels.
No negative voltage levels.	Negative and positive voltage levels.

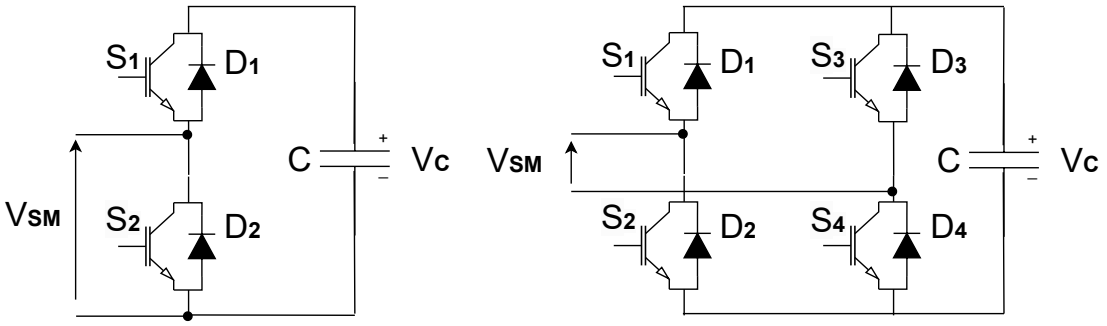

Figure 2.3 *Half-bridge (left) and full-bridge (right) submodules.*

Providing energy does not necessarily require high efficiency from one SM, especially if the need for energy is infrequent. The ability of HB-SM to generate power that has the correct polarity depends on the arm-current polarity. FB-SMs can generate correct polarity despite the current polarity and they have a boosting capability in the inversion operation [8]. As a result, HB-SM requires a significantly higher voltage rating and capability from the SM compared to FB-SM. HB-SM can only be considered an option if negative voltage levels are not required [5]. Half- or full-bridge SM are seen in Fig. 2.3.

2.4 Energy Storage Elements

Energy storage elements, such as batteries and supercapacitors are capable of fast, millisecond range, response time, and thus they fit well for inertial response and primary frequency response services [3].

Batteries store energy through electrochemical processes, where energy is converted into chemical energy, which can be used later. Battery types, such as lithium-ion

(li-ion), sodium-sulfur, nickel–metal hydride, and lead-acid batteries, have low maintenance costs and high energy density allowing them to store a lot of energy. The li-ion battery has the highest energy density of all battery types and is among the fastest-growing battery technologies. Supercapacitors can be used to compensate for fast power variations since they have a high power density [9]. Supercapacitors have much faster response time and shorter time frame storage capability than li-ion batteries or other battery types. Nowadays, supercapacitors are supported technology and they are modular and can be connected in series or parallel to increase the storage capability. Supercapacitors have considerably longer lifetimes and they can be recharged significantly more times compared to li-ion batteries. In addition, supercapacitors have higher discharge efficiency compared to batteries. One downside of supercapacitors compared to batteries is the high self-discharge rate. Energy densities and power densities for energy storage elements can be seen in Fig. 2.4.

Comparison between supercapacitors li-ion batteries and lead acid batteries can be seen in Table 2.3. In a comparison done for very short-time applications (millisec-

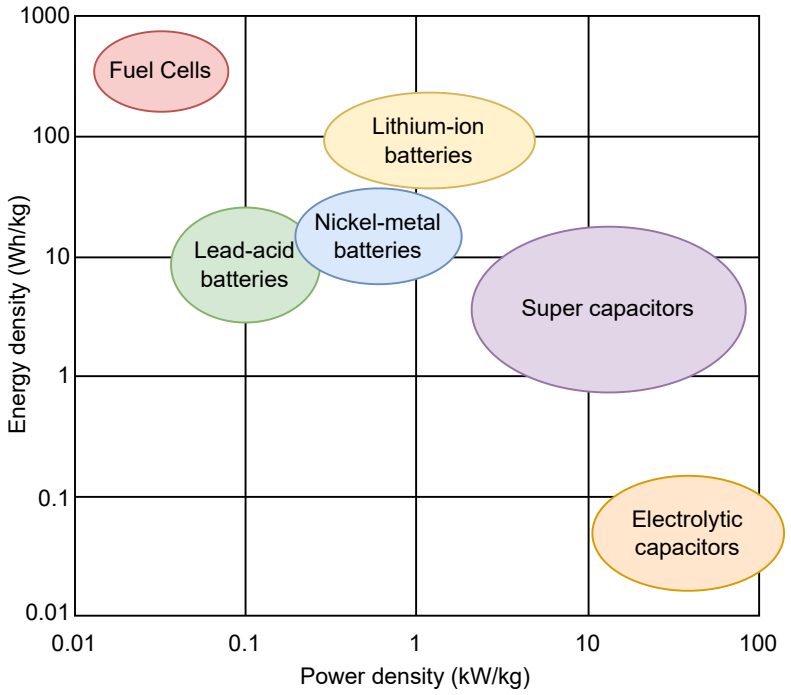

Figure 2.4 *Energy and power densities of different energy storage technologies. Supercapacitors excel in power density compared to electrochemical technologies but still lack energy density.*

onds to seconds), a 50 MW system footprint and initial costs for a supercapacitor were significantly lower compared to li-ion battery storage [2]. In conclusion, supercapacitors have technical and economic advantages over Li-Ion batteries and other

Table 2.3 *Comparison between supercapacitor and common battery types [10].*

Characteristic	**Supercapacitor**	**Lead-acid**	**Lithium-ion**
Operating temperature	-40 – +70 °C	-20 – +40 °C	-20 – +45 °C
Life cycles	1 000 000	300	10 000
Life in years	5 - 20 yr	0.5 – 5 yr	3 – 10 yr
Energy density	1 – 10 Wh/l	100 – 290 Wh/l	250 – 650 Wh/l
Power density	1000 – 10 000 W/l	100 - 1000 W/l	850 – 3000 W/l
Efficiency	>98 %	70 %	80 – 90 %
Discharge time	Seconds	Hours	Hours

battery types. A supercapacitor is selected as an energy storage element in the following chapters.

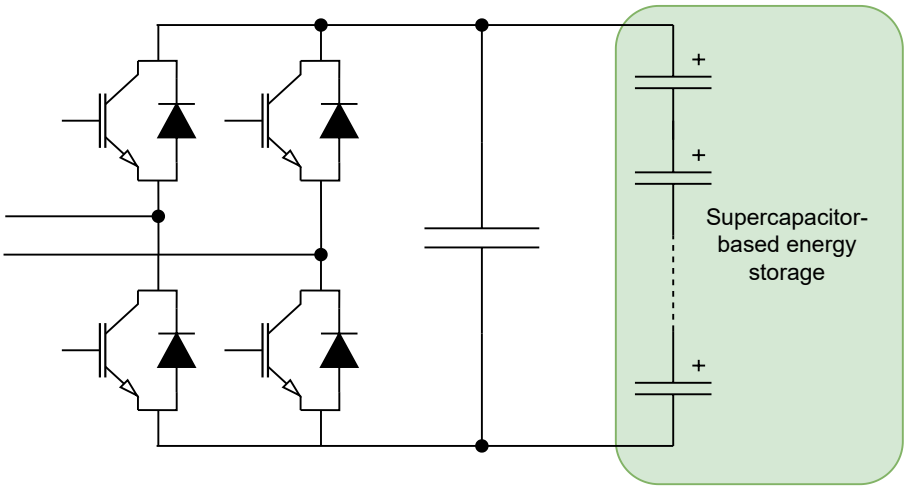

Figure 2.5 *Direct passive interface (full-bridge submodule)*

2.5 Distributed and Centralized Energy Storage Systems

The difference between the supercapacitor voltage and the MMC voltage can be large. A dc-dc converter can be added between the supercapacitor and each MMC SM or between the supercapacitor module string and the MMC dc link. Direct passive interface without a dc-dc converter is seen in Fig. 2.5. Energy storage elements, such as supercapacitors, can be distributed at the SM level or centralized at the high-voltage dc link. The centralized energy storage elements are placed in parallel with the dc link. Distributing energy storage system means that each energy storage element is connected in parallel with each submodule. Only DSCC- and DSBC-based configurations can have a centralized dc link. SSBC and SDBC configurations have distributed ESEs but no dc link.

From an operations point of view, a centralized solution allows easier scaling and maintenance of the energy storage solution. A centralized supercapacitor string can be isolated from the MMC and de-energized for maintenance when the MMC is operating. This is not possible if energy storage elements are distributed to the SM level.

Distributing ESEs results in large oscillating components in the ESE current, especially at low frequencies, which is harmful to ESE performance. A dc-dc converter can be added between ESE and the SM to reduce the oscillations. This arrangement allows a wider variety of ESEs to be connected and provides a fixed dc-output. Furthermore, with a great number of dc-dc converters, the switching power of the whole system is higher, and the efficiency is lower. [8]. However, the dc-dc converter decouples ESEs from the SMs and can therefore extend the ESE lifetime. A dc-dc converter significantly reduces the voltage variation in ESEs. More dc-dc converters

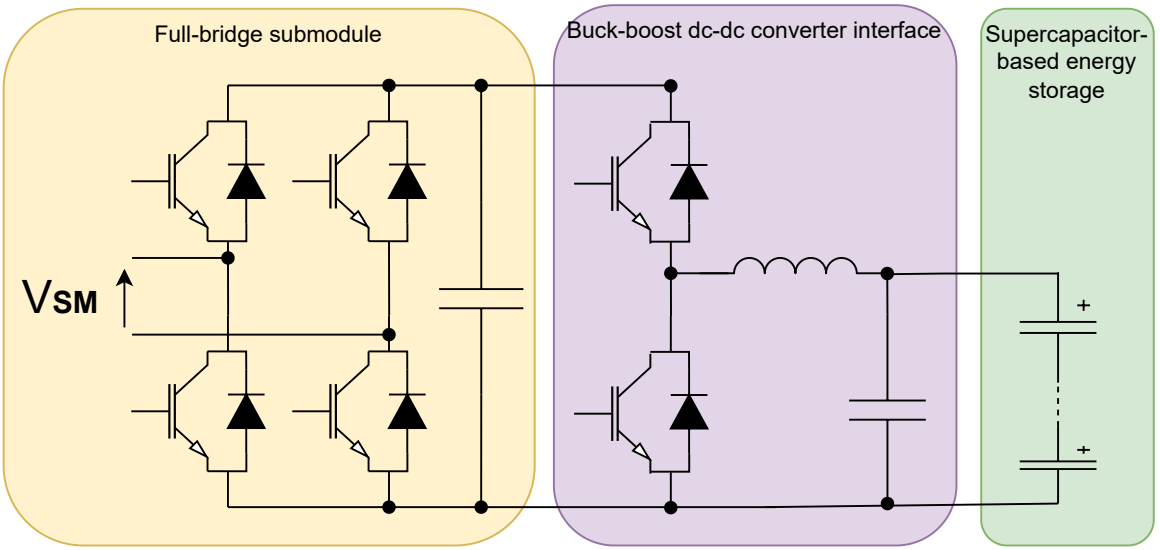

Figure 2.6 *Buck-boost dc-dc converter interface (full-bridge submodule).*

in distributed systems increase costs. However, the component sizes of the dc-dc converters are decreased compared to the centralized system. Another downside is that a power management system needs to be implemented with the MMC control loops. Maintaining proper power management in a high-power system during the charging and discharging is challenging. In addition, the power management system needs to work alongside the supercapacitor thermal management system [11, 8]. On the other hand, one benefit of this arrangement is that it combines the modularity of the supercapacitor energy storage and the high modularity of MMC. In addition, low ESE voltage and high dc link voltage can be achieved at the same time. However, the distributed energy storage system is inconvenient to build and maintain and the control and management systems become complex.

Partially-rated ESEs are one potential option for connecting ESEs at the SM level. When distributing ESEs, the ac voltage can be increased or decreased by inserting or removing ESEs. When ESE is connected to the SM, energy is transferred between ESE and SM. In double-star configurations, if only some SMs are connected to energy storage elements, circulating currents cause high losses and optimization of the circulating currents is required. Connecting ESEs to only some SMs might require nonidentical capacitor sizing due to energy deviations between the SMs. However, reducing the number of SMs that are connected to ESEs provides benefits, such as a reduced number of interface converters. Partially rated ESEs are applicable, especially in delta MMCs. [12, 5, 3]

One interface converter is called a buck-boost converter, as seen in Fig. 2.6. It is a common interface due to its simplicity [3]. High gain converters, such as dual-

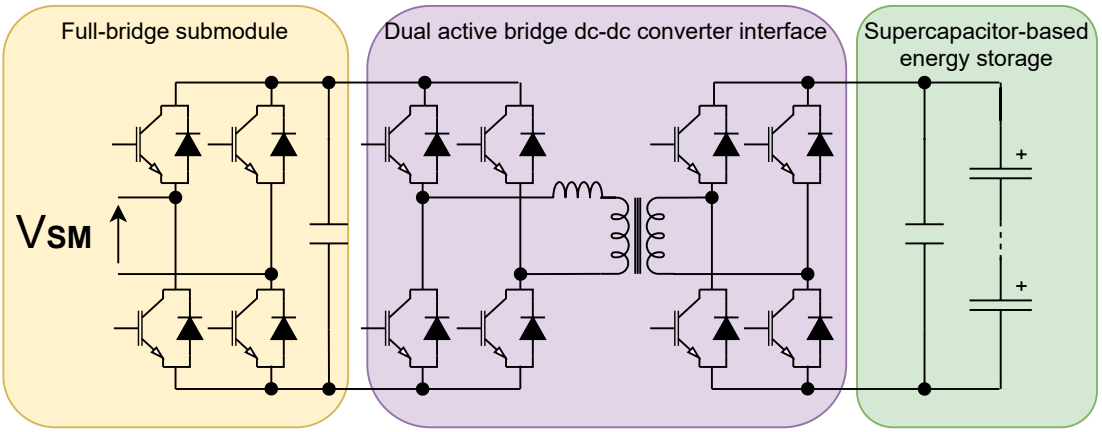

Figure 2.7 *Dual active bridge dc-dc converter interface and a full-bridge submodule.*

active bridge converters (DABs), seen in Fig. 2.7, are commonly used for their high boosting capability [13]. DAB is a converter that is electrically isolated with a transformer. It can handle higher powers than the buck-boost converter since the size of the inductor does not become a limiting factor. Comparing the two aforementioned common converters, the buck-boost converter has fewer components than DAB. In addition, buck-boost is cheaper and the footprint is lower. However, several converters, such as current-fed push-pull converters and interleaved 4-level flying capacitors can be used as bidirectional dc-dc converters [6].

The bidirectional dc-dc converter that is connected between the MMC SM and ESE is studied in the following chapters. This means that from this chapter on the ESEs are assumed to be connected to SMs in a distributed manner.

3 SUPERCAPACITOR AS AN ENERGY STORAGE ELEMENT

Supercapacitors (also known as ultracapacitors) are electric double-layer capacitors (EDLCs) that are nowadays widely used in different kinds of applications, such as ESEs due to their capability to provide high output powers. Supercapacitors function like typical capacitors, storing electrostatic energy, which makes them inherently different from batteries. Batteries are based on electrochemical energy storage. However, compared to traditional types of capacitors such as film/foil, ceramic and electrolytic, their capacitance value is several orders of magnitude larger. Hence, supercapacitors are well suited to function as energy storage elements due to their capacity to store electrical potential energy.

The energy storage system presented in this thesis is bidirectional, and thus energy can be stored in the supercapacitor and the stored energy can be used when the supercapacitor is discharging. Accumulated charge of the supercapacitor Q is the integral of the current i_{sc} flowing into the supercapacitor module:

$$Q = \int i_{\mathrm{sc}}(t)\, dt \tag{3.1}$$

If the charge Q moves through the voltage V_{sc}, the change in potential energy of the supercapacitor E_{sc} is:

$$E_{sc} = \frac{1}{2} Q V_{sc} \tag{3.2}$$

The voltage across the supercapacitor module is the accumulated charge divided by the capacitance C_{sc}:

$$V_{sc} = \frac{Q}{C_{sc}} \tag{3.3}$$

At constant power P_{sc}, the energy transferred to or from the supercapacitor over time t can be derived from (3.2) and (3.3) above:

$$E_{sc} = \frac{1}{2} C_{sc} V_{sc}^2 = P_{sc} t \tag{3.4}$$

The supercapacitor energy formula (3.4) can be used for the whole supercapacitor energy storage, where supercapacitor cells or modules are connected in series or parallel, or both. Energy in (3.4) can also be calculated for one single cell or module. Supercapacitors have lower energy density compared to other energy storages and batteries, which means that their ability to store large amounts of energy per unit is

lower. Connecting supercapacitor modules in series increases the amount of energy that can be stored.

3.1 Series and Parallel Connection of Supercapacitor

As mentioned in the previous section, one supercapacitor cell or module is capable of providing a certain, limited amount of energy. When large powers or energies are required, single supercapacitor modules can be connected in series to provide more power. Connecting supercapacitors in series increases the voltage across the whole supercapacitor energy storage. This voltage is the sum of the number n of individual cell voltages:

$$V_{\mathrm{sc,tot}} = V_{\mathrm{sc,1}} + V_{\mathrm{sc,2}} \cdots + V_{\mathrm{sc,n}} \tag{3.5}$$

Connecting supercapacitors in series decreases the capacitance:

$$C_{\mathrm{sc,tot}} = \frac{1}{\frac{1}{C_{\mathrm{sc,1}}} + \frac{1}{C_{\mathrm{sc,2}}} \cdots \frac{1}{C_{\mathrm{sc,n}}}} \tag{3.6}$$

If the capacitance is equal in each supercapacitor module, the total capacitance of the supercapacitor can be formulated as:

$$C_{\mathrm{sc,tot}} = \frac{C_{\mathrm{sc}}}{n} \tag{3.7}$$

All capacitors have internal resistance. The equivalent series resistance (ESR) is the heat dissipation of energy when electricity flows through the supercapacitor. ESR has the single strongest impact on supercapacitor efficiency and temperature and the peak power capability of a supercapacitor is largely dependent on ESR. ESR increases as the supercapacitor modules are connected in series:

$$ESR_{\mathrm{sc,tot}} = ESR_{\mathrm{sc,1}} + ESR_{\mathrm{sc,2}} \cdots + ESR_{\mathrm{sc,n}} \tag{3.8}$$

In addition, supercapacitor modules can be connected in parallel to increase the capacitance of the whole supercapacitor energy storage. The voltage across the supercapacitor storage is the same across each parallel branch:

$$V_{\mathrm{sc,tot}} = V_{\mathrm{sc,1}} = V_{\mathrm{sc,2}} \cdots = V_{\mathrm{sc,n}} \tag{3.9}$$

Capacitance increases as the branches are connected in parallel:

$$C_{\mathrm{sc,tot}} = C_{\mathrm{sc,1}} + C_{\mathrm{sc,2}} \cdots + C_{\mathrm{sc,n}} \tag{3.10}$$

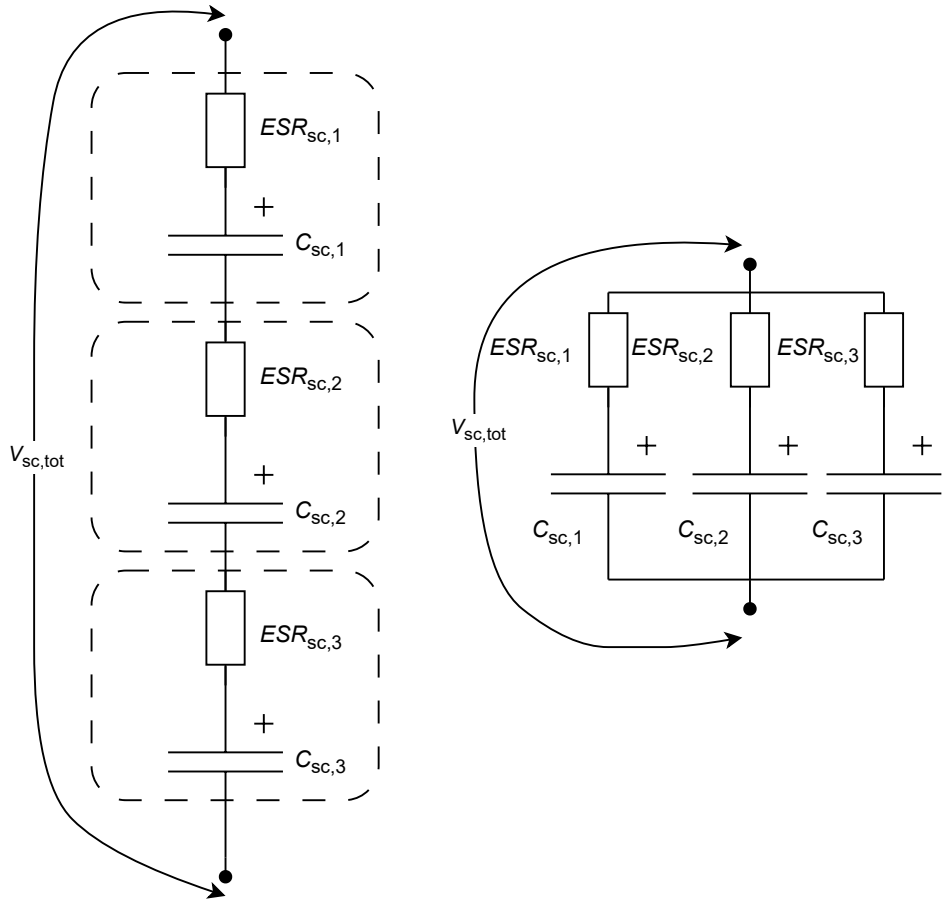

Figure 3.1 *Series (left) and parallel (right) connected supercapacitors.*

Connecting the supercapacitor in parallel decreases the ESR:

$$ESR_{\mathrm{sc,tot}} = \frac{1}{\frac{1}{ESR_{\mathrm{sc,1}}} + \frac{1}{ESR_{\mathrm{sc,2}}} \cdots \frac{1}{ESR_{\mathrm{sc,n}}}} \tag{3.11}$$

When the ESR is the same in each supercapacitor module, the total ESR of the supercapacitor is:

$$ESR_{\mathrm{sc,tot}} = \frac{ESR_{\mathrm{sc}}}{n} \tag{3.12}$$

An example of series and parallel connection of supercapacitors is shown in Fig. 3.1. Despite the modules being similar, the capacitances and insulated resistances might have variations between the modules.

3.2 Different Supercapacitor Modules

The supercapacitor modules in series produce higher voltages compared to one supercapacitor module. When supercapacitors are not in parallel, the number of needed modules and costs are reduced. The total voltage, capacitance, and ESR can be calculated from the equations presented in the previous section. Skeleton superca-

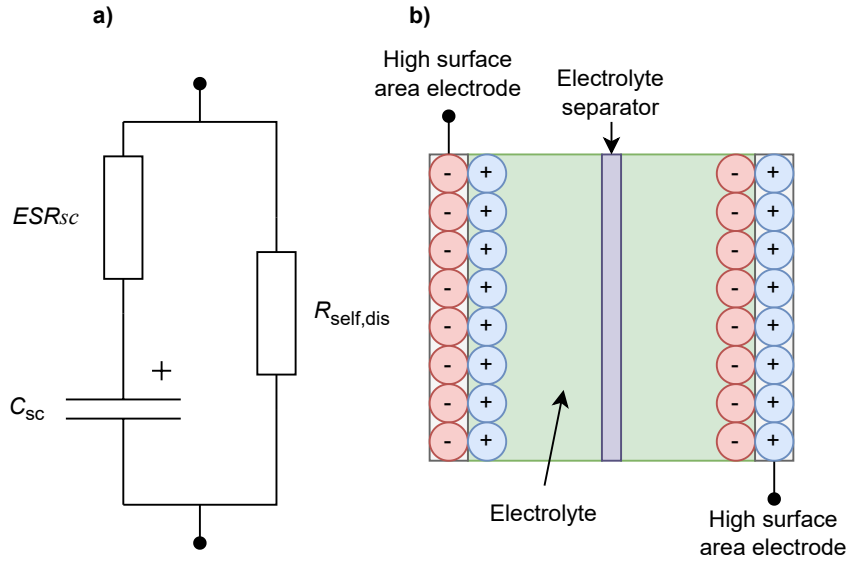

Figure 3.2 *a) The electrical equivalent circuit of a supercapacitor includes a parallel resistor simulating self-discharge. b) Conceptual drawing of an EDLC supercapacitor shows the electric double layer, where the negligible separation between opposing charges yields a large capacitance.*

pacitors provide high voltages with low ESR. Preliminary sizing calculation is done with Eaton XLM-69R0137B-T, Eaton XLM-62R1137A-R, Skeleton SkelMod 102V 88F and Skeleton SkelMod 162V 92F supercapacitors. ESE should work with different types of supercapacitors. However, one supercapacitor, Eaton XLM-69R0137B-T, is chosen as an energy storage element in the simulations, due to the suitable capacitance and voltage value that can provide the desired amount of energy. The parameters of the supercapacitor modules can be seen in Table 3.1 [14].

When the supercapacitor is not charged, it starts losing its charge. This characteristic is called self-discharge. Self-discharge is a phenomenon where the supercapacitor experiences a voltage drop after energy is stored in it. This means that less energy and power is available. The supercapacitor datasheet has information about self-discharge resistance. Self-discharge rates are higher in supercapacitors than in batteries, and a high self-discharge rate might result in a notable and rapid voltage drop. In addition, 75 % of stored energy in supercapacitors is supplied when the supercapacitor voltage is reduced to half [15]. This means that the self-discharge rate is taken into consideration in the simulation model. It is modeled by placing the supercapacitor parallel with a self-discharge resistance. The equivalent circuit of a supercapacitor is shown in Fig. 3.2. The whole bidirectional buck-boost converter is represented in Chapter 4 and it includes the supercapacitor in parallel with the self-discharge resistance.

Table 3.1 *Parameters for the supercapacitor modules.*

Paramater	**Value**	**Eaton XLM-69R0137B-T**	**Eaton XLM-62R1137A-R**	**Skeleton SkelMod 102V 88F**	**Skeleton SkelMod 162V 92F**
Maximum initial ESR	ESR	6.7 mΩ	6.7 mΩ	7.6 mΩ	12.2 mΩ
Rated voltage per module	V_{sc}	69 V	62.1 V	102 V	162 V
Maximum peak current	$I_{\text{peak,max}}$	2440 A	2157 A	2690 A	3152 A
Rated capacitance	C_{sc}	130 F	130 F	88 F	92 F
Operating temperature	T	-40 –+65 C°	-40 –+65 C	-20–+60 C°	-20–+60 C°

3.2.1 Required Number of Supercapacitor Modules

An algorithm estimates how many supercapacitors could supply and absorb 1 MW of power for at least 1 s. However, many factors can potentially vary in such an algorithm. ESR affects the supercapacitor current and voltage making the equations vastly more complex. The supercapacitor capacitance increases with the applied voltage. Furthermore, ESR increases as the temperature decreases but stays constant on the upper end of the temperature maximum. ESR will increase as the supercapacitor ages. In addition, the voltage does not behave linearly when the supercapacitor is charging and discharging. An instantaneous voltage drop in the SC voltage occurs due to ESR.

The grid where the energy storage system is integrated requires the power supply and demand to be equal at any given time. In addition, the voltage and frequency stability has to be ensured. The energy storage system is designed to provide 1 MW of energy for 1 s if needed, but if there is more supply than demand in the grid, the excess power can be stored in the supercapacitor. The supercapacitor needs to be capable of absorbing the fluctuating power and hence smoothing the power injected into the grid. In conclusion, the supercapacitor is not charged to the maximum voltage but the initial voltage is 80 % of the maximum voltage. This ensures the capacity to absorb 1 MJ of excessive energy when the supercapacitor is charged to its initial voltage. The minimum voltage can be calculated by using the relationship for electric power, as the maximum peak current $I_{\text{peak,max}}$ of the supercapacitor module is 2440 A, and the power is 1 MW. N_{P} is the number of modules in parallel:

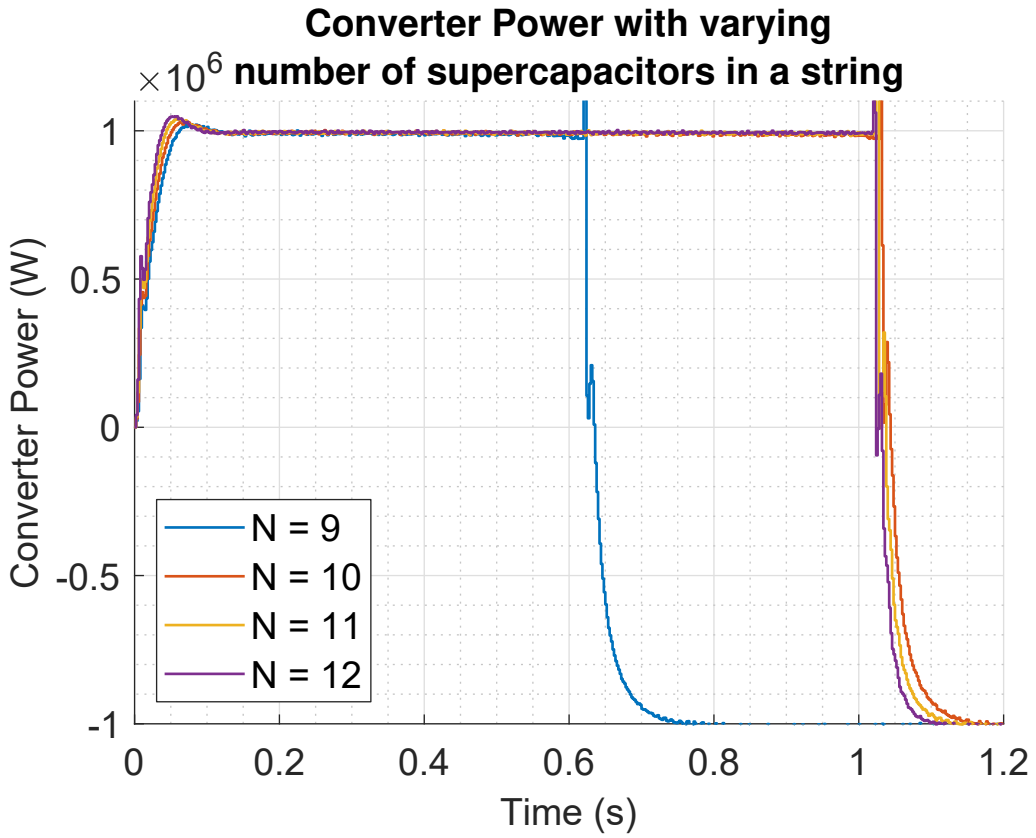

Figure 3.3 *Converter power as the number of supercapacitor modules changes.*

$$V_{\mathrm{sc,min}} = \frac{P_{\mathrm{sc}}}{N_{\mathrm{P}} I_{\mathrm{max,peak}}} \tag{3.13}$$

A simpler way of estimating the number of modules required to supply and absorb 1 MW during 1 s can be done based on (3.4). An initial guess of the number of modules in series N_{S} and the number of modules in parallel N_{P} is needed to calculate the capacitance and the voltage over the whole supercapacitor, as they depend on the number of modules, as seen in (3.9), and (3.7), respectively.

Too small number of modules may not provide enough energy, but on the other hand, a higher number of modules will increase the costs. The usable energy of the supercapacitor is calculated based on the initial supercapacitor voltage $V_{\mathrm{SC,ini}}$ and minimum supercapacitor voltage $V_{\mathrm{SC,min}}$ calculated in (3.13):

$$E_{\mathrm{sc}} = \frac{1}{2} C_{\mathrm{sc}} \frac{N_{\mathrm{P}}}{N_{\mathrm{S}}} ((0.8 \times N_{\mathrm{S}} V_{\mathrm{sc}})^2 - V_{\mathrm{sc,min}}^2) \tag{3.14}$$

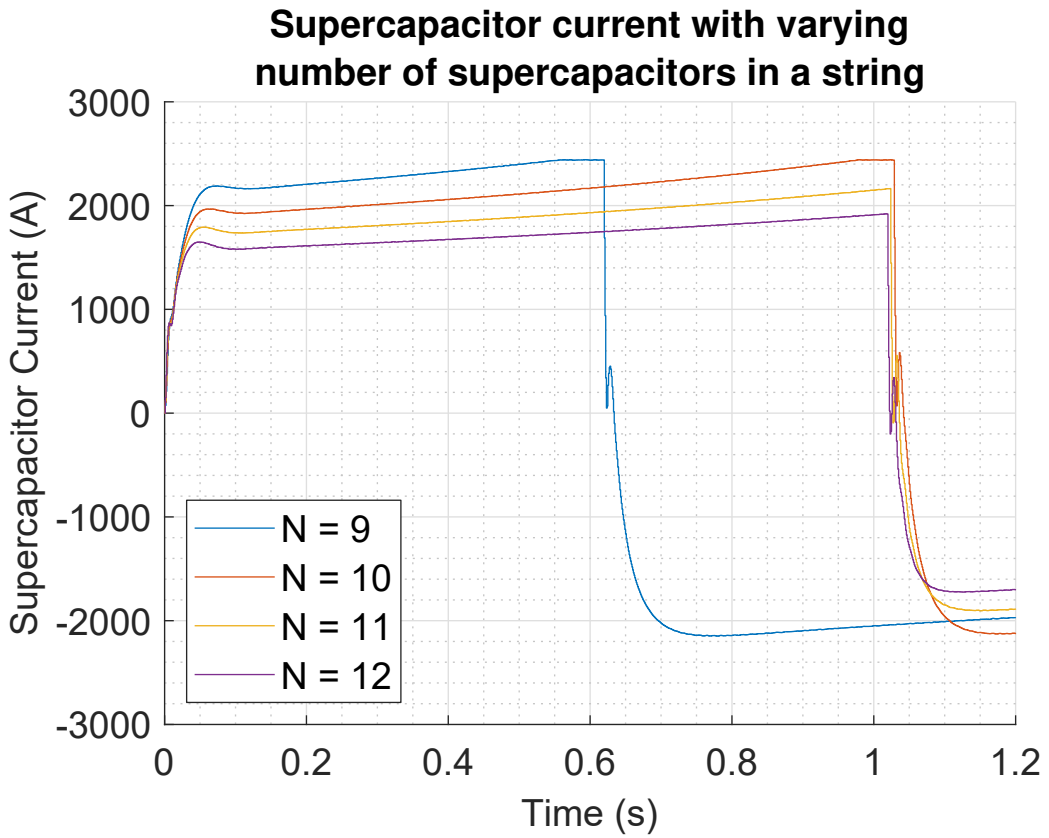

Figure 3.4 *Supercapacitor current as the number of supercapacitor modules changes.*

Energy provided with initial guess of 10 modules with Eaton XLM-69R0137B-T module:

$$E_{\text{sc}} = \frac{1}{2} \times \frac{130\,F}{10}((0.8 \times 10 \times 69\,V)^2 - (409.84\,V)^2) = 0.889\,MJ \approx 0.9MJ \quad (3.15)$$

The energy with 10 modules is too small and thus the number of modules is increased. Energy provided with 11 Eaton XLM-69R0137B-T modules:

$$E_{\text{sc}} = \frac{1}{2} \times \frac{130\,F}{11}((0.8 \times 11 \times 69\,V)^2 - (409.84\,V)^2) = 1.186\,MJ \approx 1.2MJ \quad (3.16)$$

11 modules in series can provide more than 1 MJ of energy, and thus it is cosidered as a feasible option. The supply time t with 11 modules can be calculated based on (3.4):

$$t = \frac{E_{\text{sc}}}{P_{\text{sc}}} \approx 1.2\,s \quad (3.17)$$

As the supercapacitor voltage drop is nonlinear due to ESR, the results are verified by simulating the supercapacitor currents and the converter output power with

Table 3.2 *Parameters for the whole Eaton XLM-69R0137B-T supercapacitor energy storage (11 modules).*

Paramater	**Unit**	**Value**
Number of modules in series	N_{S}	11
Number of modules in parallel	N_{P}	1
Maximum peak current	$I_{\mathrm{peak,max}}$	2440 A
Maximum supercapacitor voltage	$V_{\mathrm{sc,max}}$	759 V
Initial supercapacitor voltage	$V_{\mathrm{sc,ini}}$	607.2 V
Minimimum supercapacitor voltage	$V_{\mathrm{sc,min}}$	409.84 V
Capacitance	C_{sc}	11.82 F
ESR	ESR	73.7 mΩ
Power	P_{sc}	1 MW

varying numbers of supercapacitors, as seen in Fig. 3.3, and Fig. 3.4, respectively. The output power can clearly not provide 1 MJ of energy if the number of supercapacitor modules is 9. With 9 modules, the supercapacitor voltage drops below the minimum $V_{\mathrm{sc,min}}$ and the converter power collapses after $t = 0.6\,\mathrm{s}$. With 10 modules, the supercapacitor current saturates at the maximum at time $t \approx 0.95\,\mathrm{s}$, after which the converter power begins to fall, which makes 11 modules in series the minimum required number of supercapacitors. The parameters for this supercapacitor consisting of 11 modules can seen in Table 3.2.

4 DC-DC CONVERTER

The operation of a bidirectional buck-boost converter is studied in this thesis. The schematic circuit of the converter is shown in Fig. 4.1. This type of converter works in buck mode when a supercapacitor integrated into it is charging. The schematic circuits of the buck operation can be seen in Fig. 4.2 and Fig. 4.3. The same converter works in a boost mode when the supercapacitor is discharging, as seen in Fig. 4.4 and Fig. 4.5. The dc-dc converter consists of two IGBT switches, an inductor, and a capacitor. IGBTs are used as switching devices for the ability to handle high currents, in the range of a few kA, and their capability to withstand very high voltages, over 1 kV, and thus high power. A supercapacitor is connected to one end of the dc-dc converter and the other end is the SM of an MMC.

The objective of the converter is to transfer energy from the supercapacitor to the dc link and vice versa. This allows secure connection of different kinds of supercapacitor configurations to different voltage levels. The supercapacitor and the dc link form two voltage sources that can both supply and absorb voltage. An inductor is connected in series with a supercapacitor to filter current ripple. The aim is to keep the output power at 1 MW for at least 1 s when the supercapacitor voltage decreases from initial voltage to voltage minimum as the supercapacitor is discharging. Furthermore, the output power should be kept at -1 MW for at least 1 s when the supercapacitor voltage charges back to its initial value. In addition, the converter-supercapacitor system is designed to absorb 1 MW power from the dc link despite the state of charge of the supercapacitor. The initial voltage needs to be scaled smaller than the rated supercapacitor voltage to be able to absorb 1 MW when the initial voltage is at its maximum.

Real-world components are not ideal and contain parasitic resistance, capacitance, inductance, or can dissipate power. Practical inductors exhibit copper losses, originating in the resistance of the wire, and core losses, due to hysteresis and eddy current losses in the magnetic core. The dc-dc converter circuit includes parasitic resistance of the inductor, capacitor ESR and IGBT resistance.

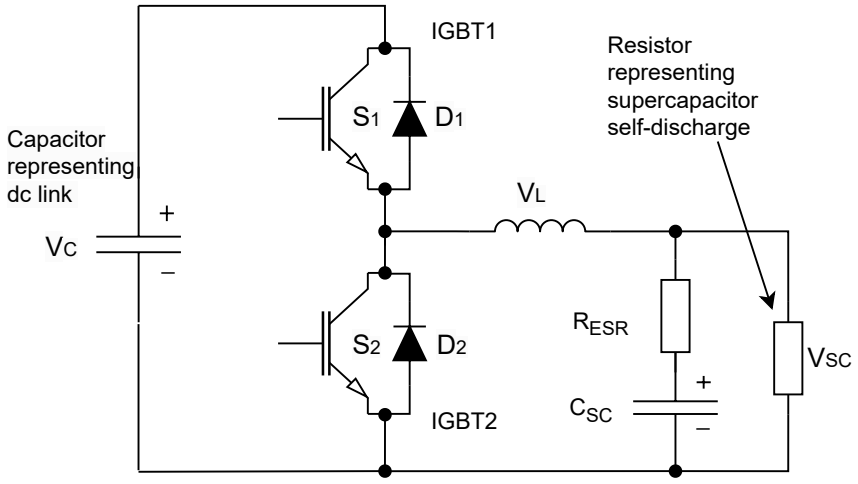

Figure 4.1 *Schematic circuit diagram of bidirectional buck-boost converter*

4.1 Bidirectional dc-dc Converter Schematics

The bidirectional dc-dc converter studied in this thesis works in continuous conduction mode (CCM), which means that the inductor current never goes to zero. When the dc-dc converters operate in CCM, the peak-to-peak inductor current Δi_{L}. The converter in Fig. 4.1 can step up and step down the voltage. These types of converters have been used in various applications, such as electric vehicles and energy storage systems. The direction of the power flow is indicated by an arrow above the schematic circuit in Fig. 4.2, Fig. 4.3, Fig. 4.4 and Fig. 4.5.

During the buck operation, the voltage level of the dc link is stepped down to the lower voltage level of the supercapacitor. The SC is charging and the power and current flow from the dc link to the SC. When the converter starts to work in the buck mode, the upper controllable switch S_1 is on and the lower controllable switch S_2 is off and both of the diodes D_1 and D_2 are off. The upper and lower diodes and the upper and lower switches can be seen in Fig. 4.1. The current flowing to the inductor is charging the inductor. This situation can be seen in Fig. 4.2. In the next step, seen in Fig. 4.3 diode D_2 acts as an anti-parallel freewheeling diode (FWD), and both of the controllable switches and the diode D_1 are not conducting.

The direction of the current and thus power is reversed in the boost mode. In the boost mode, as the supercapacitor is discharging and the power and current flow from the supercapacitor to the dc link, the lower switch S_2 is first on and the upper switch S_1 is off. This allows the inductor to be charged by the current flowing

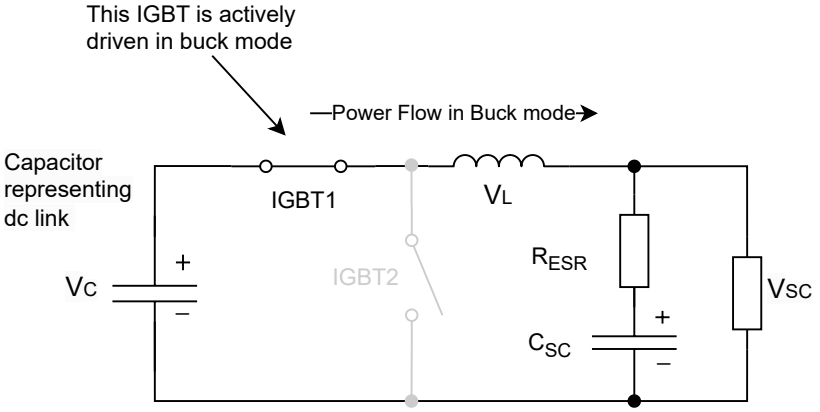

Figure 4.2 *Converter working in buck-mode when the upper IGBT is on.*

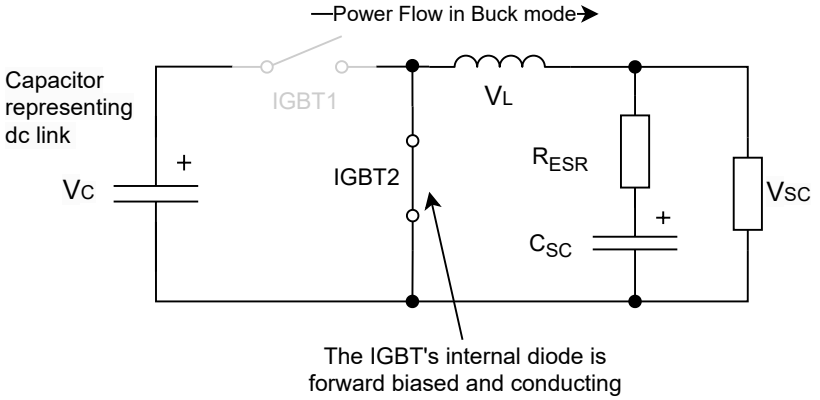

Figure 4.3 *Converter working in buck-mode when lower IGBT is on. Its internal diode is conducting.*

from the supercapacitor. The upper and lower controllable switches and the diodes can be seen in Fig. 4.1 and the state where the lower switch S_2 is on is shown in Fig. 4.4. During the next state, the inductor current is decreasing as current is flowing through diode D_1 connected to the switch. This state is seen in Fig. 4.5.

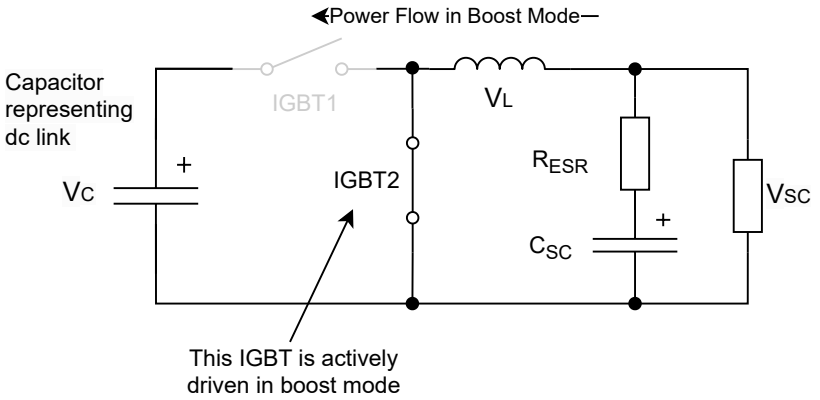

Figure 4.4 *Converter working in boost-mode when lower IGBT is on.*

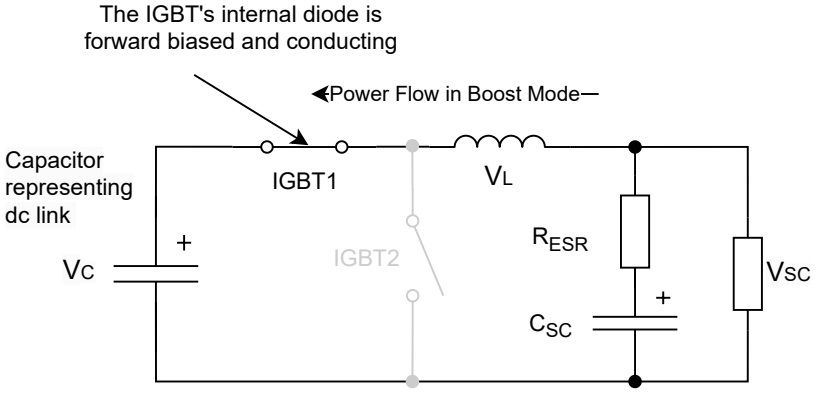

Figure 4.5 *Converter working in boost-mode when upper IGBT is on.*

In this state, only diode D_1 is conducting while switch S_1 and switch S_2 and diode D_2 are not conducting. The inductor current I_{L} will decrease linearly until the next buck mode when the switch S_1 is opened again. The turning on of the switch S_1 happens after a short time, called dead time, during which both upper and lower controllable switches are off. It is also notable that the polarity of the inductor current does not change immediately. Dead time is the time interval during which both the IGBTs are off after each switching event when the system is not capable of starting a new switching event. Dead time should be as short as possible without causing shoot-through and shorting the dc link and leading to excessive current [16].

4.1.1 Duty Cycle

The time the pulse is on t_{on} is the pulse width. The duty cycle d is defined as the ratio of pulse width to the switching period t_{sw}:

$$d = \frac{t_{\mathrm{on}}}{t_{\mathrm{on}} + t_{\mathrm{off}}} = \frac{t_{\mathrm{on}}}{t_{\mathrm{sw}}} \tag{4.1}$$

In addition, the duty cycle defines the relationship between the input voltage and the output voltage or the relationship between the dc link and the SC voltage.

Volt-second balance states that for steady-state operation, the net inductor voltage during one switching period must be equal to zero. After the switching time t_{sw} has passed, the inductor current i_L, is back to its initial value. Otherwise, the inductor current would increase continuously destroying the dc-dc converter. The duty cycle can be calculated in buck operation assuming that the inductor voltage at the end of the switching period t_{sw} is equal to the inductor voltage at the beginning of the cycle. The peak-to-peak inductor current Δi_{L} unlike the average inductor current I_{L} is independent of the output power.

The inductor current is rising as the upper IGBT is turned on, as the current flow is towards the inductor, as seen in Fig. 4.2. The inductor current is decreasing as the upper IGBT is turned off, as seen in Fig. 4.3. The relationship between inductor voltage and inductor current can be stated as:

$$\int_0^{t_{\mathrm{sw}}} V_{\mathrm{L}}\, dt = \int_0^{t_{\mathrm{sw}}} L\frac{di_{\mathrm{L}}}{dt}\, dt \tag{4.2}$$

Integral over one switching period when the net charge over the period is zero:

$$i_{\mathrm{L}}(t_{\mathrm{sw}}) - i_{\mathrm{L}}(0) = \frac{1}{L}\int_0^{t_{\mathrm{sw}}} V_{\mathrm{L}}\, dt = \langle V_{\mathrm{L}} \rangle = 0 \tag{4.3}$$

Two sub-circuits are created based on the on- and off-times of the converter. Using Kirchhoff's law and the on-time circuit, seen in Fig. 4.2, the inductor voltage during the on-time becomes:

$$V_{\mathrm{L}} = V_{\mathrm{dc}} - V_{\mathrm{sc}} \tag{4.4}$$

Using Kirchhoff's voltage law and the off-time circuit, seen in Fig. 4.3, the inductor voltage during the off-time becomes:

$$V_{\mathrm{L}} = -V_{\mathrm{sc}} \tag{4.5}$$

The duty cyle of the buck mode can be calculated using(4.1),(4.3), (4.4) and (4.5):

$$\begin{cases} \langle V_{\mathrm{L}} \rangle = \frac{V_{\mathrm{dc}} - V_{\mathrm{sc}}}{L} t_{\mathrm{on}} = dt_{\mathrm{sw}} \frac{V_{\mathrm{dc}} - V_{\mathrm{sc}}}{L} \\ \langle V_{\mathrm{L}} \rangle = \frac{-V_{\mathrm{sc}}}{L} t_{\mathrm{off}} = (1-d) t_{\mathrm{sw}} \frac{-V_{\mathrm{sc}}}{L} \end{cases} \tag{4.6}$$

The two equations are equal since the net inductor voltage during one switching period $\langle V_L \rangle$ goes back to its initial value, and the inductances L and the switching time t_{sw} are the same in both equations:

$$d(V_{\mathrm{dc}} - V_{\mathrm{sc}}) = (1-d)V_{\mathrm{sc}} \tag{4.7}$$

The duty cycle can be solved:

$$d = \frac{V_{\mathrm{sc}}}{V_{\mathrm{dc}}} \tag{4.8}$$

In the boost operation the duty cycle is:

$$d = 1 - \frac{V_{\mathrm{sc}}}{V_{\mathrm{dc}}} \tag{4.9}$$

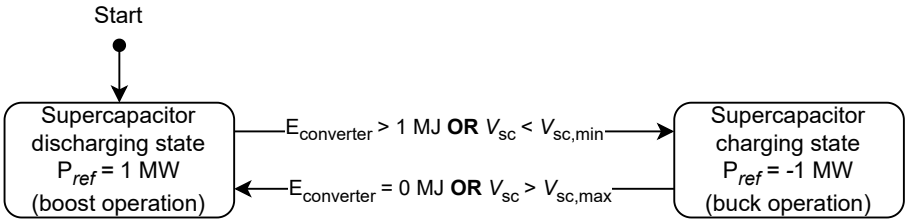

Figure 4.6 *Hysteresis controller.*

In the boost mode, the IGBT pulses switch in a complementary manner with respect to the buck mode.

4.2 Automated Charging and Discharging of the Supercapacitor

The controller can be made to work in a buck or boost mode. In boost mode, positive power discharges the supercapacitor; in buck mode, negative power charges the supercapacitor. The buck and boost modes can be changed by converting the IGBT pulses into opposite pulses. Furthermore, the direction of the power needs to be changed to operate in the desired mode.

A hysteresis controller shown in Fig. 4.6 is implemented to automatically and repeatedly discharge and charge the supercapacitor. The hysteresis controller has upper and lower band limits for both the supercapacitor voltage and the energy transferred to or from the dc link. Supercapacitor voltage has a minimum and a maximum value, which indicates when the charging mode changes. Buck or boost mode change is carried out in the hysteresis controller as the supercapacitor voltage minimum and maximum is reached or 1 MJ of energy has been transferred to either direction. This hysteresis controller switches between charging and discharging when the set amount of energy has been transferred through the dc-dc converter, or if the supercapacitor voltage exceeds the minimum and maximum bounds. In theory, this type of converter would also operate without the outer loop PI controller. In this case, the hysteresis controller outputs the converter power, and instantaneous current reference I_{ref} is calculated by dividing the power request by the converter voltage. Power reference P_{ref} toggles between charging and discharging modes based on the energy exchanged between the dc link and the supercapacitor, and the supercapacitor voltage. However, preliminary simulations done during this thesis work revealed that this type of control may easily suffer from excessive overshooting, especially when switching between buck and boost modes. Hence, a decision was made

to add the outer loop PI controller to reduce and produce a smoother transition between the operating modes.

4.3 Controller

A closed loop cascaded control system is implemented to regulate the supercapacitor current and dc-dc converter power, as shown in Fig. 4.7. It is based on a PWM modulator with two cascaded traditional proportional-integral (PI) controllers. The output of the hysteresis controller is the power reference. The outer loop is the slower loop of the cascade and it regulates the dc-dc converter power. The input of the outer loop is the power error signal calculated from the given power reference and the measured converter power. The output of the outer loop is the current reference.

The faster inner loop regulates the supercapacitor current. An error signal is the difference between the current reference and the measured supercapacitor current. This current error is fed to the input of the inner PI controller to adjust the duty cycle.

The controller contains a PWM generator which acts as the modulator. The duty cycle is the input to the PWM generator and the output is a pulse signal, which is used to form two opposite pulses as the commands to the IGBT switches. The other switch is on when the other is off, and vice versa [17]. A double-update PWM method and an up-down counter form a triangular carrier and a PWM signal to the IGBTs. Current sampling is carried out at the peaks and valleys of the triangular carrier with the first sampling point being the start of the switching period. This allows the average current to be sampled instead of the ripple current. Similarly, the output pulses of the PWM generator are inverted, when the converter is operating in buck mode.

However, it should be noted, that the current control of this type of bidirectional non-isolated dc-dc converter is inherently complicated to implement with a single PI current controller, since the transfer function of the dc-dc converter is different in buck and boost mode, as has been analyzed in for example [18]. Before implementing the converter in hardware, additional work should be spent on optimizing the control strategy to ensure optimal current and power regulation.

4.4 Component Selection for the dc-dc Converter

The dc-dc converter consists of two power switches, an inductor, and a storage supercapacitor. These components are selected so that the operation of the energy storage

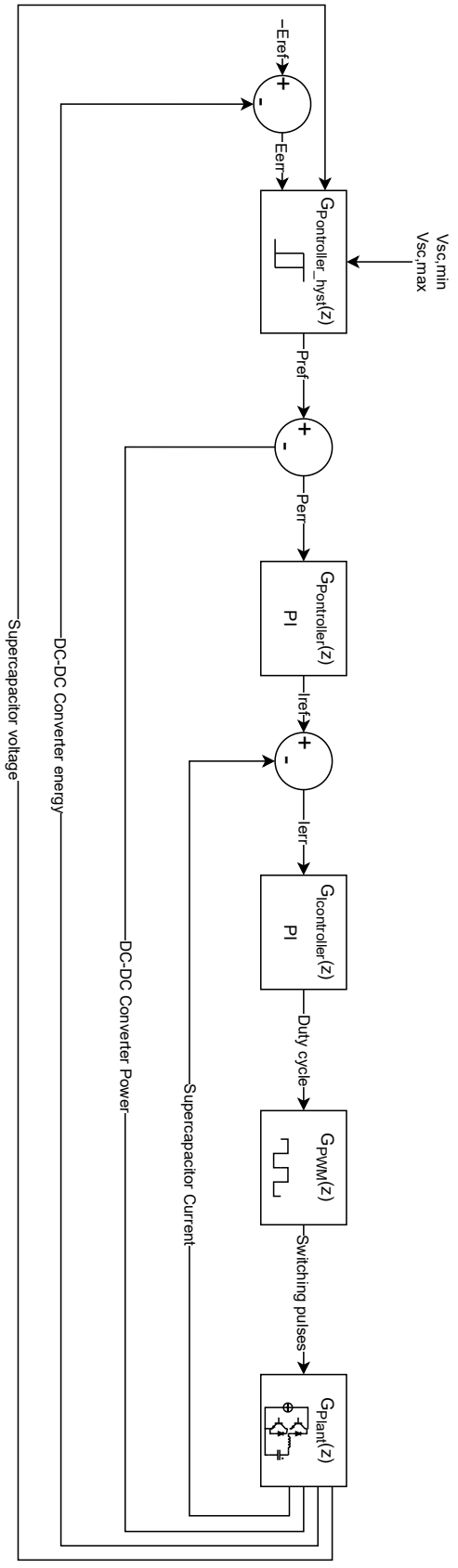

Figure 4.7 *Dc-dc converter control strategy.*

Table 4.1 *Parameters in buck mode for inductor sizing*

Parameter	Unit	Value
Supercapacitor minimum voltage	$V_{\text{sc,min}}$	409.83 V
Supercapacitor maximum voltage	$V_{\text{sc,max}}$	607.2 V
Dc link voltage	V_{dc}	2 kV
Ripple current	Δi	244 A
Switching frequency	f_{sw}	1 kHz
Diode forward voltage drop	V_{d}	2.35 V
Voltage drop across IGBT	V_{sw}	2.7 V

system can be simulated without excessive disturbances. Decreasing the losses of the aforementioned components increase the overall efficiency of the converter.

4.4.1 Inductor

Inductor has a critical role in providing stable current to the supercapacitor or to the dc link. Inductor stores energy in a magnetic field when current is flowing through it. The current flow induces a time-varying magnetic field and the alternating magnetic field creates an electromotive force (emf) to obstruct current fluctuations. Lenz's law states that the induced electric current flows in a direction where the current opposes the change that induced it, thus indicating the direction of the current. As the current flows through the inductor the energy stored in the magnetic field of the inductor is:

$$E = \frac{1}{2}LI^2 \tag{4.10}$$

Inductance L is the capacity of the inductor to oppose a change in the current flowing through it. Choosing the correct inductance value is critical to obtain an acceptable rate of change of the current passing through the inductor. The current changes during the switching cycle are known as current ripple:

$$V = L\frac{di}{dt} \tag{4.11}$$

$$\rightarrow \frac{di}{dt} = \frac{V}{L} \tag{4.12}$$

The voltage drop across an inductor is directly proportional to the current ripple. The inductor in the dc-dc converters needs to carry high currents, up to 2440 A. Inductor sizing is done by selecting the correct ripple current maximum of 10 % of the average inductor current.

Values needed for sizing the inductor can be seen in Table 4.1. The maximum voltage across the inductor can be calculated by using Kirchhoff's voltage law.

The required inductance value for a given current ripple in buck and boost operation mode can be calculated by using formulas commonly found in the engineering literature. Considering the power flow in buck mode is from the dc-link to the supercapacitor, in the equation shown in (4.13), V_{sw} is the voltage drop across the IGBT switch, V_{d} is the forward voltage drop across the diode, r is the ratio between the ac and dc components in the inductor current, f_{sw} is the switching frequency and I_{o} is the converter output current. Diode and IGBT forward voltage drop are taken from the component datasheet. For the inductor sizing point of view, their effect is small due to the high the voltages involved.

$$L = \frac{(V_{\mathrm{dc}} - V_{\mathrm{sw}} - V_{\mathrm{sc}}) \times (V_{\mathrm{sc}} + V_{\mathrm{d}})}{(V_{\mathrm{dc}} - V_{\mathrm{sw}} + V_{\mathrm{d}}) \times r \times f_{\mathrm{sw}} \times I_{\mathrm{o}}} \tag{4.13}$$

Since the control system maintains the converter power at a fixed value, the converter output voltage and current vary with the supercapacitor state of charge. Hence, the required inductance was calculated in one hundred operating points between the extremes: at the end of the charge cycle, with maximum voltage $V_{\mathrm{sc}} = 0.8 \times V_{\mathrm{sc,max}}$ and minimum current, and at the beginning of the charge cycle, with minimum voltage with the maximum current. The switching frequency 1 kHz is selected. The ripple is 10 %, or $r = 0.1$. With these parameters, the minimum inductor value is 2.6 mH, which was used in the simulations. However, it should be noted, that as in (4.14), the required inductance increases with decreasing output current. Hence, if the converter is designed to allow charging up to 100 % capacity $V_{\mathrm{sc}} = 1.0 \times V_{\mathrm{sc,max}}$ with 10 % ripple, an inductor of 3.6 mH would be required.

In boost operation mode the power flow is from the supercapacitor to the dc-link, and hence the input voltage is the decreasing supercapacitor voltage, and the output voltage is the fixed dc-link voltage. Hence, the parameters are the same as used in (4.13), but input and output voltages are reversed. The inductor current ripple used in the calculation is 10 % ($\Delta I_{\mathrm{L}} = 0.1 \times I_{\mathrm{L}}$).

$$L = \frac{V_{\mathrm{sc}} \times (V_{\mathrm{dc}} + V_{\mathrm{d}} - V_{\mathrm{sc}})}{\Delta I_{\mathrm{L}} \times f_{\mathrm{sw}} \times (V_{\mathrm{dc}} + V_{\mathrm{d}})} \tag{4.14}$$

Similarly to the calculation of the required inductance in buck mode, the inductance is calculated for one hundred operating points between the extremes, the beginning and end of the discharge cycle. These correspond to the operating points with maximum voltage and minimum current and vice versa. The calculation yielded the same

minimum value for the inductor, 2.6 mH, or 3.6 mH if charging to full capacity of the supercapacitor with 10 % current ripple is required.

To validate the inductor selection, the converter operation is simulated with the calculated inductance of 2.6 mH, and with 20 % lower and higher inductances of 2.08 and 3.12 mH. The simulation results are shown in Fig. 4.8. It should be noted that since the supercapacitor is connected in series with the inductor, $I_{\mathrm{sc}} = I_{\mathrm{L}}$. With $L = 2.08\,\mathrm{mH}$, the ripple in the current is 11.3 %, and decreases to 9.0 % with $L = 2.6\,\mathrm{mH}$ and further down to 7.5 % with $L = 3.12\,\mathrm{mH}$. From these results, it can be concluded that the inductor calculations are correct, and that the inductor selection is appropriate. The ripple at $L = 2.6\,\mathrm{mH}$ is less than the design criterion of 10 %. At least one predicted reason for this is that due to the outer loop power controller, it will take approximately 100 ms for $P_{\mathrm{converter}}$ to reach the power of 1 MW. During this time, the supercapacitor voltage increases, and the converter has already moved away from the worst-case operating point.

Furthermore, it can be seen from Fig. 4.8 that the current measurement and sampling are operating properly. The sampled current used by the closed loop controls, shown in blue, is free from switching ripple. In addition, proper operation of the PWM with a switching frequency of 1 kHz is verified.

The inductance can potentially be reduced from the calculated value since $I_{\mathrm{peak,max}}$ only applies in the worst-case scenario and during a very short time interval. Switching losses are present repeatedly in real devices each time the switch opens and closes, and thus the higher the switching frequency the more losses the converter has.

4.4.2 IGBT

An insulated-gate bipolar transistor (IGBT) is a power device used in high-power switching. Due to the bidirectional dc-dc converter used in the energy storage system, a diode is used in an anti-parallel manner with the IGBT to conduct current in the opposite direction. The path of the current can be analyzed from Fig. 4.1. The IGBT current in the converter is the same as the current flowing through supercapacitor.

IGBT is the chosen switching device because it can handle high voltage and current ratings. Nowadays, the power of a typical commercial IGBT module can be up to ten thousand watts and in the future, the power ratings of IGBT modules are expected to grow. There are commercial IGBT modules from i.e. Fuji Electric, Mitsubishi Electric, and Infineon Technologies, that have an even higher power output [19].

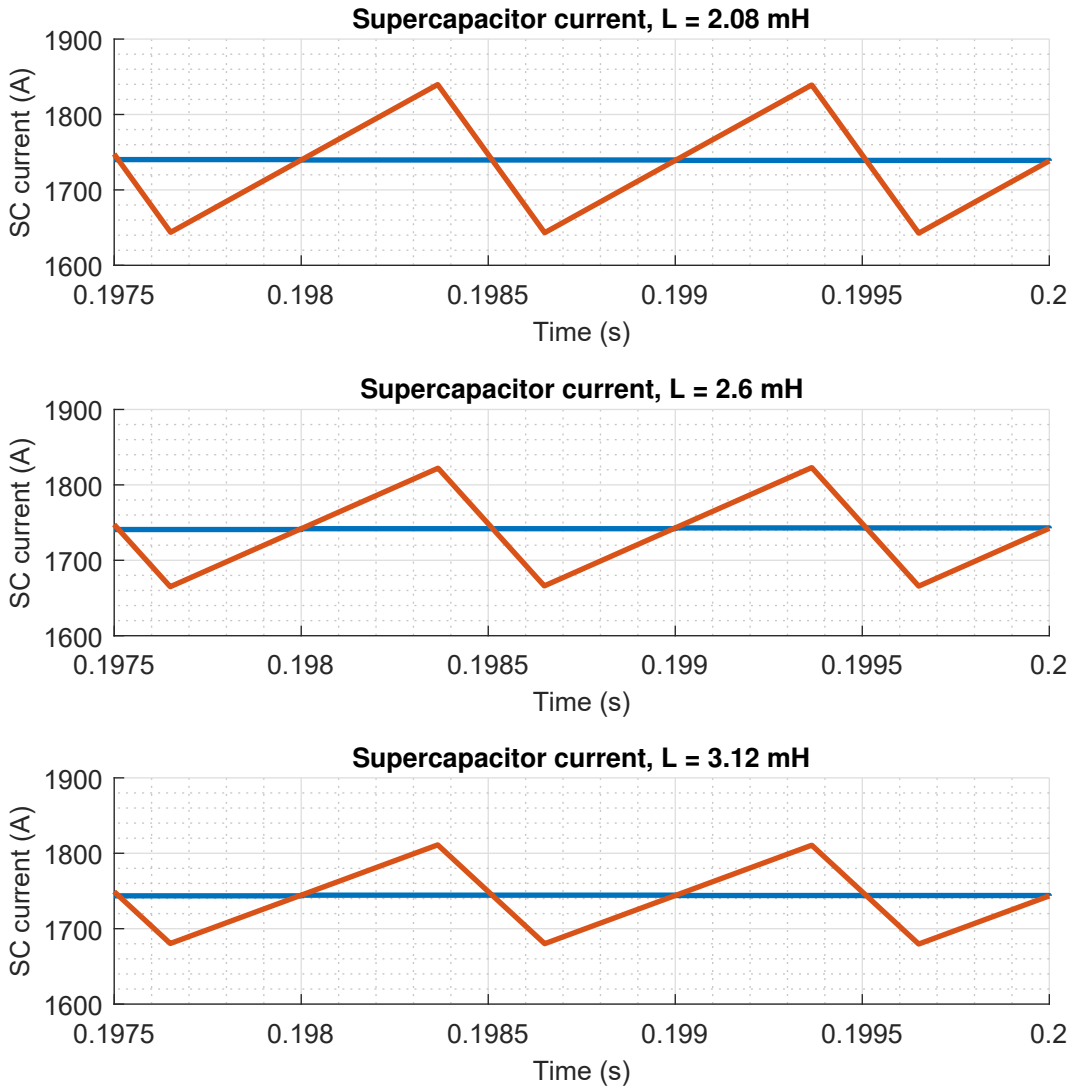

Figure 4.8 *Supercapacitor current in buck mode with varying inductance, taken after* $P_{converter}$ *is stabilized at 1 MW. The ripple decreases as the inductance is increased. The same trend would be observed in boost mode as well. Instantaneous current is shown in orange, and the sampled current used by the closed loop current controller is shown in blue.*

Regular IGBT is a unidirectional device and thus the current can only conduct in a forward direction. A reverse-conducting IGBT is used, which integrates an IGBT and FWD on a single chip to conduct the current in both directions. The direction and path of the current depend on the switching of the IGBT modules during on- and off-times and whether the buck or boost mode is used.

In the boost operation, the inductor current is flowing through the upper diode

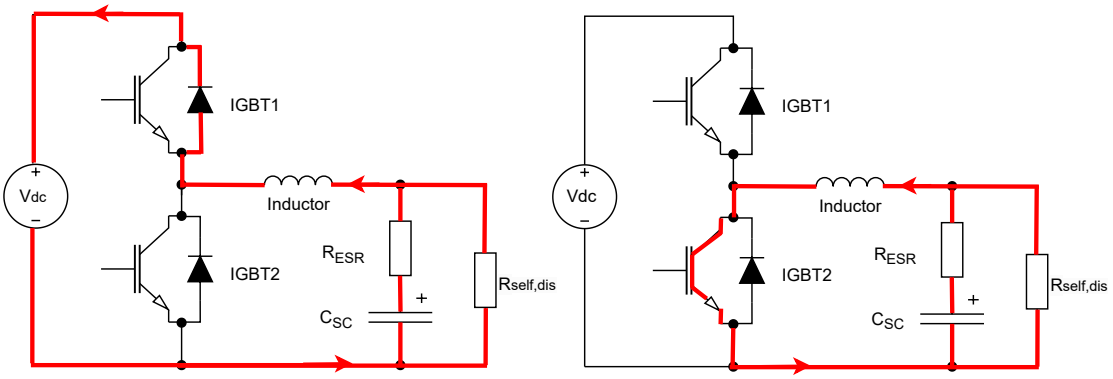

Figure 4.9 *Current paths through IGBT and diode in boost mode.*

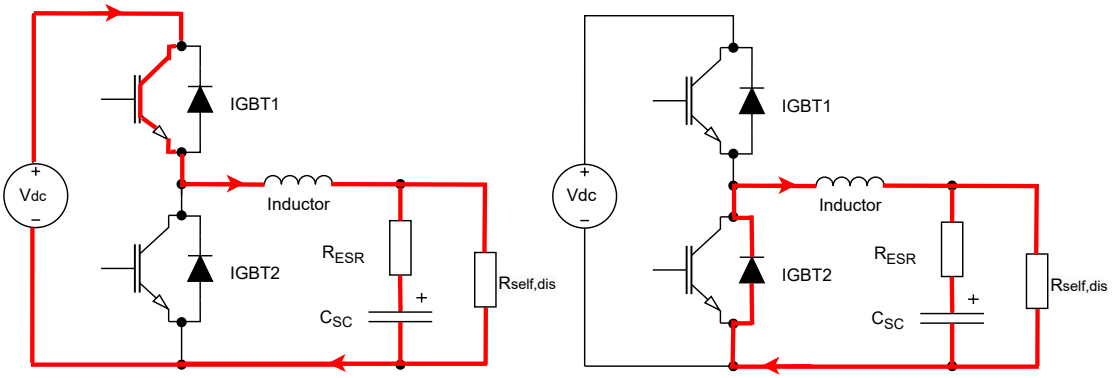

Figure 4.10 *Current paths trough IGBT and diode in buck mode.*

toward the supercapacitor or through the lower controllable switch. This indicates that the currents are inductor/supercapacitor currents. IGBT modules should be rated to the dc link voltage. During the buck operation, the direction of the IGBT and diode current is opposite compared to the boost operation but the path is the same. The path of the current in both buck and boost mode can be seen in Fig. 4.9 and in Fig. 4.10.

Due to the high current and voltage ratings required in the dc-dc converter, the Infineon FZ2000R33HE4 IHM-B IGBT module is chosen as a switching device for the converter. Infineon IGBT modules have the highest current rating of the manufacturers, which is the most important criterion. Other important factors are collector-emitter voltage, maximum junction temperature, efficiency, and cost. FZ2000R33HE4 IHM-B module is rated for 3300 V collector-emitter saturation voltage, 2000 A continuous nominal dc current, and 4000 A repetitive peak current [20].

5 IGBT THERMAL PARAMETERS AND LOSSES

IGBT power modules may dissipate remarkable amounts of thermal energy in energy conversion applications. If this heat, generated due to the switching and conduction losses, is not conducted away, the IGBT module will be damaged due to overheating. Thus, it is imperative to develop effective cooling components for IGBT. Furthermore, to validate the cooling system design, a thermal analysis of the dc-dc converter is essential. IGBTs are the most critical components of the dc-dc converter and high temperatures can easily lead to failures in the solder layers or elsewhere. The IGBT junction temperature is relevant for the operation of the device and must be considered as the practical design limit value. The maximum junction temperature listed in the component datasheet cannot be exceeded. The conduction and switching losses and the thermal impedance, among other parameters, can be found in the IGBT datasheet. Optimizing the cooling system is an effective way to improve the reliability of the whole system.

A heat sink is a passive component that transfers the heat of a higher temperature IGBT to lower temperature air or to a liquid coolant where the heat dissipates. The thermal resistance of the heat sinks and the thermal interface material (TIM) between the IGBT and the heat sink must be included in the thermal calculations. Thermal resistance, measured in Kelvins per Watt, is the ability of a component to resist heat flow, similarly as electrical resistance is the capability to resist the flow of electric current. Thermal resistances inside the IGBT and associated components are used to determine the heat dissipation from the IGBT to avoid overheating [21].

An appropriately designed heat sink and TIM can improve the performance of the converter by increasing the power density or efficiency and decreasing the size of the IGBT module. Depending on the mechanical design and component layout, the IGBT modules can be installed either on a common heat sink, or it may be beneficial for them to have separate heat sinks. The heat sink can be a separate component, either custom-made or ordered from a supplier, and it may be part of a larger mechanical support structure. While the heat sink is a passive component, in high-power applications is almost always augmented with liquid or forced air cooling, instead of relying solely on gravity and convection. The cooling system is assumed to be properly designed to maintain the coolant temperature at 50 °C, as seen in Table 5.1. The thermal conductivity of the TIM should be as low as achievable in

Table 5.1 *Thermal model parameters for the Infineon FZ2000R33HE4 IHM-B IGBT.*

Parameter	**Value**
Liquid coolant temperature	50 °C
Thermal conductivity	1e-3 W/mK
Heat sink resistance	0.009 % °C or K/W
Heat sink time constant	0.1 % s
TIM time constant	1e-3 s

the case of power electronic converters that use IGBT modules. The thickness of the thermal grease affects the IGBT temperature. The thermal conductivity of a typical thermal grease is approximately 1 W / (m · K) [22]. Power modules are typically mounted on heat sinks using TIM to make an even, high-quality contact with low thermal resistance. Smooth contact surfaces are beneficial as they can inhibit the formation of hot spots. [23]

Compared with other cooling techniques, air cooling is the simplest approach with often competitive costs. Liquid cooling is also often suitable for high-power IGBT modules because air cooling has limited thermal performance. Liquid-cooled heat sinks are significantly smaller and lighter, and they typically have lower thermal resistance. Liquid cooling also enables the heat to be transferred far away from the converter, far away from its delicate electronics. For example, with liquid cooling, the heat can be transferred outside of the converter or outside of the building where the converter is operating and dissipated there. With air cooling, the heat is spread in the vicinity of the converter. Hence, its components may suffer higher thermal stresses, and the space where the converter is operating, may need more powerful air condition systems. However, liquid cooling comes with the disadvantage of requiring a complicated coolant circulation system with valves, piles, chillers, pressure tanks, etc. [24]

Cauer or Foster thermal networks can be used to analyze the thermal characteristics of a system. Both models consist of thermal resistances R and capacitances C. A thermal model of the whole converter is challenging to create due to the dependency on the thermal grease and heat sink. The Cauer network includes capacitances from ground to node and thermal resistances, as seen in Fig. 5.1. The Cauer network represents a model based on the physical and thermal structure of the real system. However, creating an accurate Cauer model is challenging because it requires knowledge of the internal structure and knowledge of the used materials.

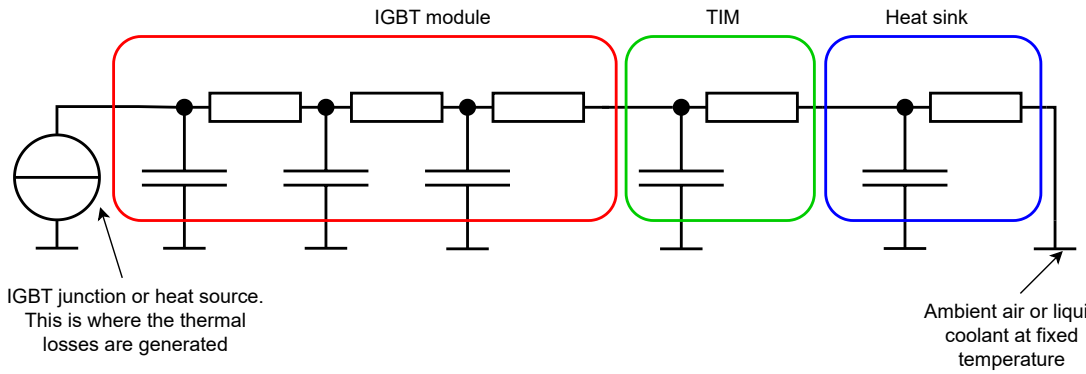

Figure 5.1 *An example Cauer thermal network, whose parameters are based on underlying physical properties, can be used to model a complete converter. The model can be branched and additional components and TIMs can be easily added.*

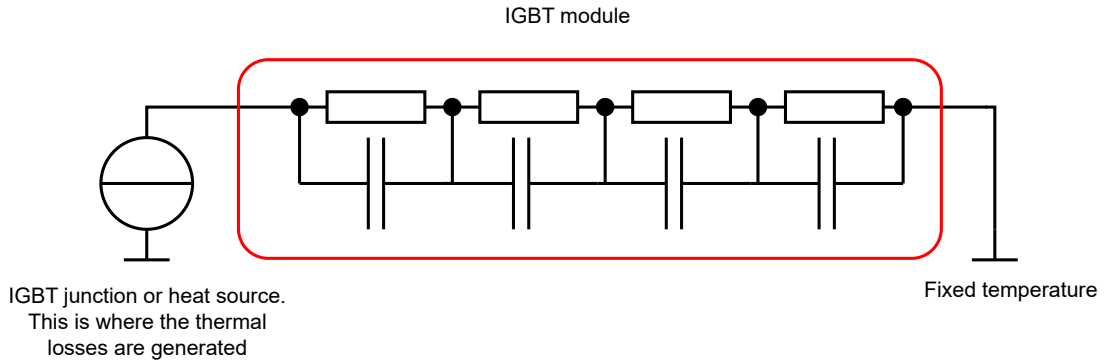

Figure 5.2 *An example Foster thermal network. Foster model parameters are based on curve fitting with no relationship with physical properties.*

Another way to model heat transfer through a semiconductor is the Foster thermal model. The Foster model is purely based on curve fitting. Hence, in the Foster model, seen in Fig. 5.2, resistances R and capacitances C do not represent any actual physical structures. When the Foster model of IGBT is connected in series with the models of a TIM and heat sink, the simulation results show unrealistic temperatures. Hence, a Foster model cannot be used directly to simulate the thermal behavior of a whole converter. [24, 25]

Datasheet provides thermal data of a Foster model. To model realistic heat sink thermal mass and convection to the environment, the Foster thermal data must be converted to a Cauer equivalent, which can then be used.

All sorts of factors, such as electric load, power cycles, and temperature variations affect the reliability of the IGBT module [26]. Thermal responses can be simulated to discover the thermal behavior of the IGBT module. Junction temperatures T_j and power losses for the IGBT are simulated as a reliability requirement for the

Table 5.2 *Worst-case parameters at T = 150 °C for Infineon FZ2000R33HE4 IHM-B IGBT module.*

Parameter	Value
Threshold voltage	6.4 V
Forward voltage	3.25 V
On-state resistance	0.095e-3 Ω
Switch-on loss	3900 mJ
Switch-off loss	4950 mJ
Off-state voltage	1800 V
On-state current	2400 A
Maximum junction temperature	150 °C

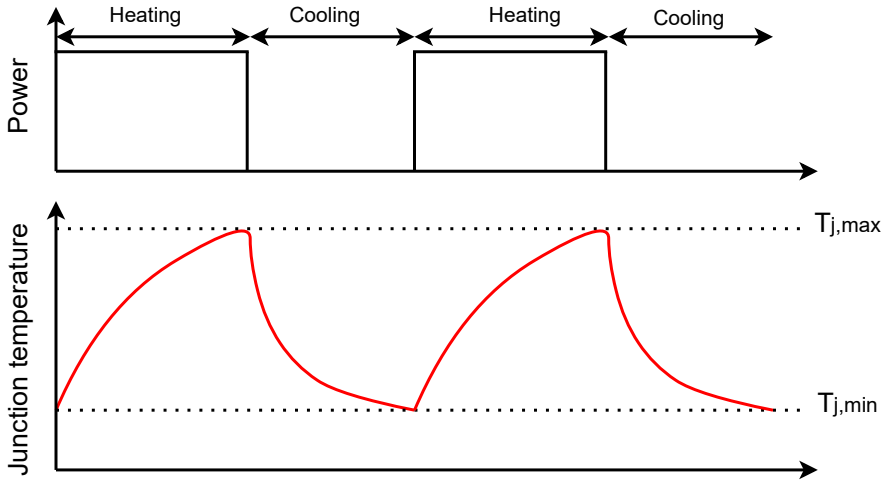

Figure 5.3 *Injected power affects the junction temperature.*

dc-dc converter. The junction temperature varies between the maximum $T_{\mathrm{j,max}}$ and minimum junction temperature $T_{\mathrm{j,min}}$ during the power cycles. The junction temperature profile of the IGBT can be seen in Fig. 5.3. A power cycling test is often performed to estimate the lifetime of the IGBT, requiring multiple cycles of injected power and cooling time between the power injections. High temperatures can be applied to reduce the number of cycles needed for simulating the thermal response of the IGBT [27].

The power losses of the IGBT module comprise switching and conduction losses, as seen in Table 5.2. The power losses of the IGBT module can be simulated with respect to thermal performance. Switching losses are caused by the collector-emitter current i_{T} and voltage v_{T} not changing in a step-wise manner. Instead, they have rising and falling slopes. The IGBT datasheet provides information about switching losses: The turn-on and turn-off energy losses in a specific test condition e_{on} and e_{off} are tabulated for different temperatures. Furthermore, a graph of the typical

switching losses as a function of collector current is provided. For the selected IGBT, turn-off losses are greater than turn-on losses. Conduction losses happen due to the nonideal behavior during the conduction period, which manifests as on-state resistance and a non-zero forward voltage drop (collector-emitter voltage). This voltage drop results in losses that depend on the collector current. Turn-off and turn-on coefficients ($c_{\text{off}} >> c_{\text{on}}$) can be used to calculate the switching losses:

Switching energy losses are turn-on losses:

$$e_{\text{on}} = c_{\text{on}} v_{\text{T}} i_{\text{T}} \tag{5.1}$$

And turn-off losses:

$$e_{\text{off}} = c_{\text{off}} v_{\text{T}} i_{\text{T}} \tag{5.2}$$

Switching power losses (over time T):

$$p_{\text{IGBT,sw}} = \frac{1}{T}(\sum_{\text{i}} e_{\text{off,i}} + e_{\text{on,i}}) \tag{5.3}$$

Conduction losses:

$$p_{\text{IGBT,con}} = v_{\text{T}}(i_{\text{T}}) i_{\text{T}} \tag{5.4}$$

The anti-parallel diode has reverse recovery energy losses e_{rr} that depend on the current i_{T}, voltage v_{T}, and frequency [19]. Switching energy losses, or reverse recovery losses for the diode can be calculated with a coefficient c_{rr} and a nonlinear function f_{rr}:

$$e_{\text{rr}} = c_{\text{rr}} v_{\text{T}} f_{\text{rr}}(i_{\text{T}}) \tag{5.5}$$

Diode switching power losses (over time T):

$$p_{\text{diode,sw}} = \frac{1}{T} \sum_{\text{i}} e_{\text{rr,i}} \tag{5.6}$$

Diode conduction losses:

$$p_{\text{diode,con}} = v_{\text{T}}(i_{\text{T}}) i_{\text{T}} \tag{5.7}$$

Simulations can provide data at three different temperatures including the maximum temperature. To calculate or simulate the conduction power losses of the IGBT, it is necessary to evaluate the temperature dependency.

6 SIMULATION RESULTS AND THERMAL ANALYSIS

A test cycle maintains $P_{\text{converter}}$ at 1 MW. First, a total of 1 MJ of energy is supplied from the supercapacitor to the dc link. Then, the direction of the power flow is reversed, and the supercapacitor absorbs 1 MJ. Then, the cycle is repeated indefinitely. The simulation results are discussed in this chapter. Simulations are done in MATLAB/Simulink software using the Simscape toolbox.

6.1 Controller Tuning

The supercapacitor current controller and the converter power controller gains were chosen using a modified Ziegler-Nichols (ZN) tuning rule, by setting the integral gain K_{i} to zero and increasing the proportional gain K_{p} until persistent oscillations appear [28]. This K_{p} is marked down as the ultimate gain K_{u}, and the time period of the oscillations is recorded as t_{u}. Then, the K_{p} and K_{i} were calculated using the "no overshoot" tuning rule from [28]: $K_{\text{p}} = 0.2 \times K_{\text{u}}$ and $t_{\text{i}} = 0.5 \times t_{\text{u}}$, and $K_{\text{i}} = \frac{1}{t_{\text{i}}}$. However, as already highlighted in [28], such rule-based tuning results in sub-optimal control performance, and indeed much manual tweaking of the controller gains are required to prevent the supercapacitor current from overshooting during the start, or when switching between buck and boost modes. Overall, finding adequate tuning parameters proved to be challenging. This is likely due to the extremely low damping of the RLC load due to low R. That is, compared to the typical textbook example of a converter supplying power to an LR circuit simulating an induction motor.

More ideal control could be achieved if buck and boost modes had different tuning parameters, or with sophisticated control algorithms such as model predictive control. The main challenge is two goals: to reverse the inductor current as soon as possible and to prevent high overshoot. If the inductor current is reversed rapidly, there is a high overshoot. If the inductor current is changed slowly, there is less overshoot, but then the converter charges and discharges the supercapacitor too much. Also, the transition is highly nonlinear with a fast current reversal.

6.2 Time-Domain Results

The supercapacitor current and voltage during the test cycle are plotted in Fig. 6.1 and Fig. 6.2 respectively. The supercapacitor and converter powers are plotted in Fig. 6.3 Fig. 6.4. The figures are analyzed to discover whether the theory discussed

in Chapter 4 is adequate.

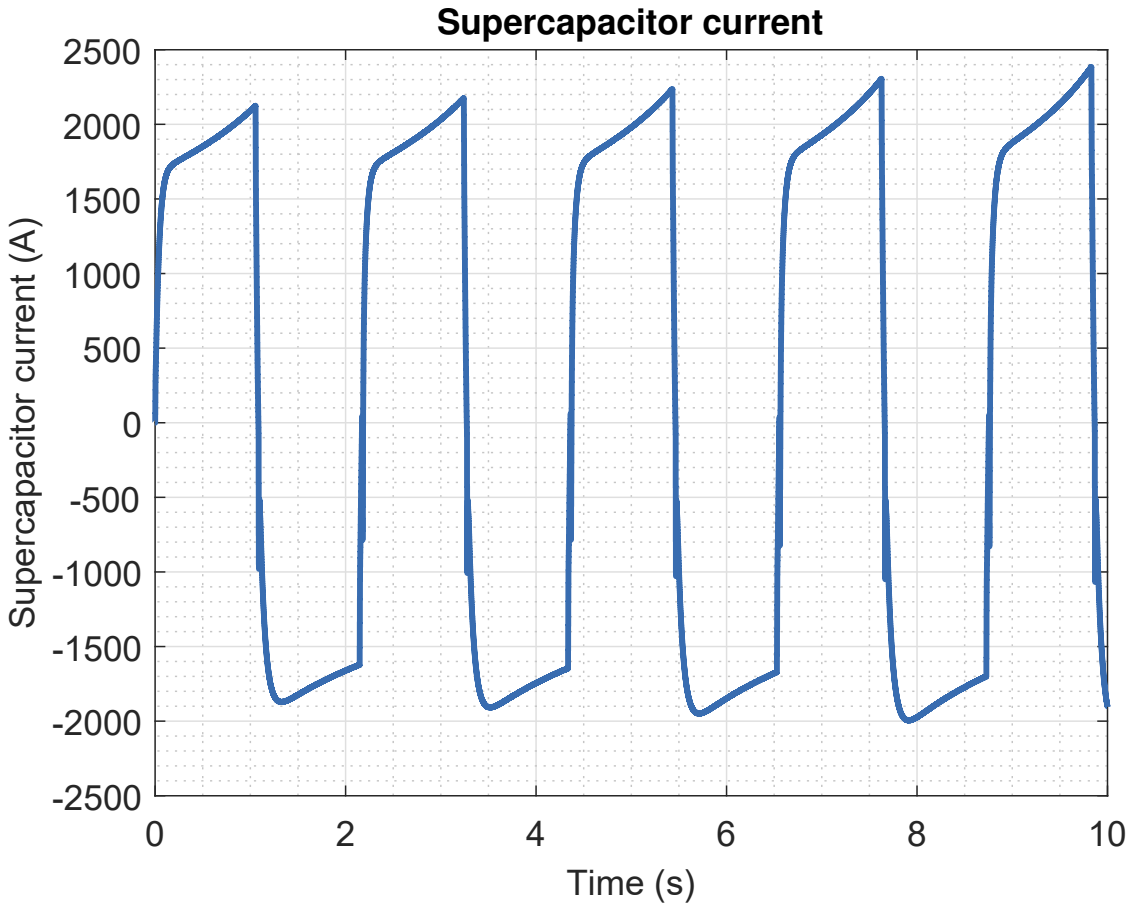

Figure 6.1 *Supercapacitor current.*

The supercapacitor current (Fig. 6.1) is controlled by a PI controller. (Note that the inductor current ripple is not displayed to facilitate the subsequent analysis.) When the simulation is started, the hysteresis controller sets the converter power reference to 1 MW. As a result, the cascaded control system will rapidly ramp up the supercapacitor current to approximately 1750 A, to ramp the converter power up to desired power reference, as seen in Fig. 6.1. When the converter is operating in boost mode, the supercapacitor voltage decreases. This means that at the same time, a steady increase is seen in the supercapacitor current, due to the regulating action of the outer loop power controller. The decrease in the supercapacitor voltage is demonstrated in Fig. 6.2. It can also be observed, that the supercapacitor current never increases above $I_{\text{peak,max}}$ value indicated in the supercapacitor datasheet (2440 A). It can be observed from Fig. 6.1 that during the first cycles, the supercapacitor current increases to 2133 A.

After approximately one second, when the total energy of 1 MJ has been transferred

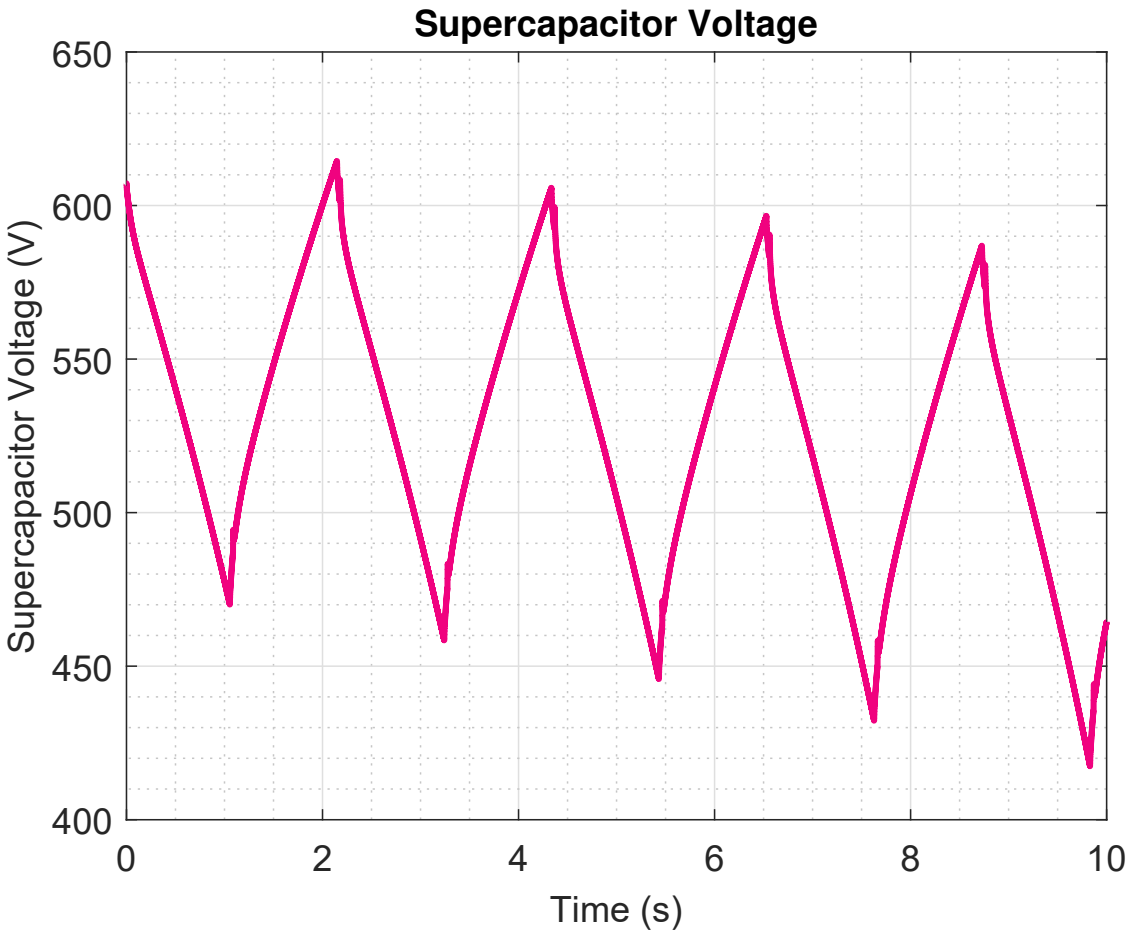

Figure 6.2 *Supercapacitor voltage when the supercapacitor is discharging and charging.*

from the supercapacitor to the dc link, the hysteresis controller sets the power reference to -1 MW. This will then switch the bidirectional converter from boost to buck mode, and the direction of the flow of the energy is reversed. This is done by reversing the polarity of the current, which is seen the first time in Fig. 6.1 after 1 s. It can be seen that it will take approximately 200 ms for the cascaded control system to reverse the direction of power, and regulate the converter power to its desired value.

It should be noted, that during these simulations, it is assumed that the dc link voltage remains at a constant value. In practice, this is not true, and in a real MMC converter, the dc link has a voltage ripple [29, 30]. The peak-to-peak value of the voltage ripple predominantly depends on the capacitance of the MMC. That is, because the SM is part of the MMC converter, and it will be switching to create the sine wave MMC output. To further refine the simulation model, the dc link should have a voltage ripple. Furthermore, it is expected, that the operation of the bidirectional dc-dc converter will also affect the dc link voltage. However, in this thesis, it is assumed that a controller will keep the voltage of the SM capacitor

constant. It would be interesting to study if coordination between the higher-level SM controller is required because the SM dc link voltage must always remain within a specific range. If the voltage decreases too low, the MMC cannot produce anymore the sine wave output, and if it increases too high, equipment damage will occur.

The discharging and charging voltage cycles of the supercapacitor can be seen in Fig. 6.2. In the simulation, the supercapacitor is first discharged and the voltage decreases until 1 MJ of energy has been transferred from the supercapacitor to the dc link. Nearly linear voltage drop and voltage gain due to ESR are visible at the beginning and end of each cycle. After that the supercapacitor voltage increases as the supercapacitor is charging. Discharging from initial supercapacitor voltage $V_{\mathrm{sc,ini}}$ to the minimum supercapacitor voltage $V_{\mathrm{sc,min}}$ is not required to provide 1 MJ of energy. This reduces the maximum current, which is beneficial to the operation of the whole system. After the discharging and charging the cycle starts from the beginning. One notable thing is that the maximum voltage peak after the first discharging-charging cycle has increased, due to losses affecting the operation. This increase is small (1 % of the $V_{\mathrm{sc,ini}}$) and it is taken into account. In reality, the supercapacitor is scaled so that slightly more than 1 MJ of energy can be stored in the supercapacitor at each point of the cycle. After the first cycle, the minimum supercapacitor voltage starts decreasing and the increased voltage peak is no longer reached. That is because the hysteresis control is based on converter energy exchange. Hence, the losses are not compensated for. When the minimum supercapacitor voltage drops to $V_{\mathrm{sc,min}}$, the hysteresis controller follows the supercapacitor voltage limit instead of the limit created by the transferred energy.

The supercapacitor power stays approximately at -1 MW when the supercapacitor is discharging and 1 MW when the supercapacitor is charging as seen in Fig. 6.3 The dc-dc converter power is regulated with a PI controller. It can be seen that the ESS can maintain the converter power request, as seen in Fig. 6.4. The different dynamics in buck and boost mode are seen from the overshoot: when changing from boost to buck mode, the overshoot is present, while for the reverse transition, there is no overshoot. The overshoot occurs due to inductor polarity change as energy is stored in the inductor.

A spike is seen in the converter power shown in Fig. 6.4. The converter power surges momentarily up to 200 % when switching from buck to boost, and 120 % when switching from boost to buck. It is assumed that this surge is due to the rapid reversal of the inductor current, and due to the high nonlinearity associated with this phenomenon. It is expected that a PI controller without complicated tun-

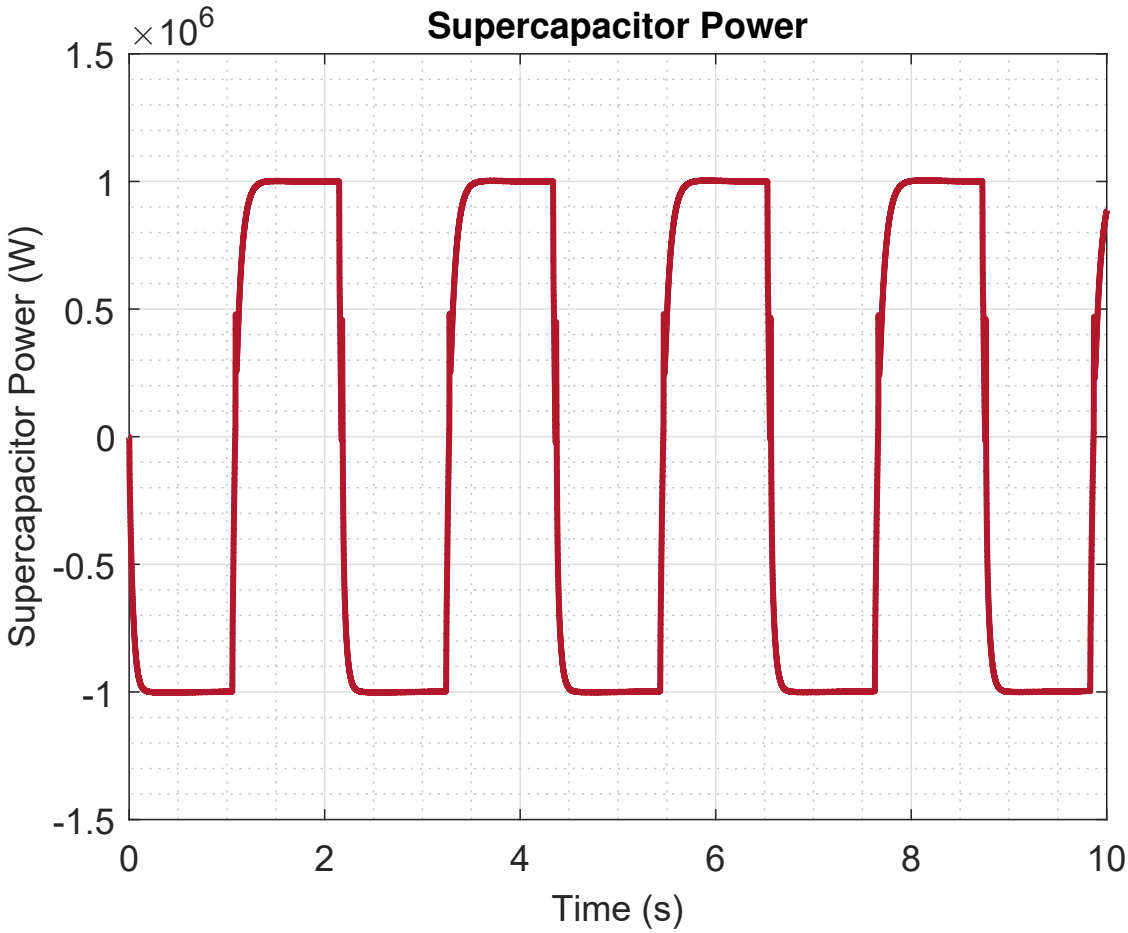

Figure 6.3 *Supercapacitor power when the supercapacitor is discharging and charging.*

ing and anti-windup mechanisms cannot maintain regulation during it. During this thesis, it is evaluated if making the outer loop power controller slower reduces the overshoot. It is found that as expected, when the outer loop controller is slower, the overshoot is smaller. Further reduction of the overshoot could be achieved by limiting the duty cycles of the inner loop current controller, with separate limits for buck and boost operation.

However, making the outer loop power controller slower is problematic in another way, since making it slower results in the supercapacitor being charged and discharged too much. Making the power loop slower makes it respond slower to changes in the power references. The direction of the converter power is not changed immediately when the sign of the power reference changes. Hence, it is shown that there are two contradictory control objectives. One is to reduce the overshoot in the converter power, and the other is to realize an ideal cycle as described at the beginning of this chapter, where converter power is maintained at fixed $\pm$ 1 MW. As a compromise solution a modified version of the hysteresis controller shown in

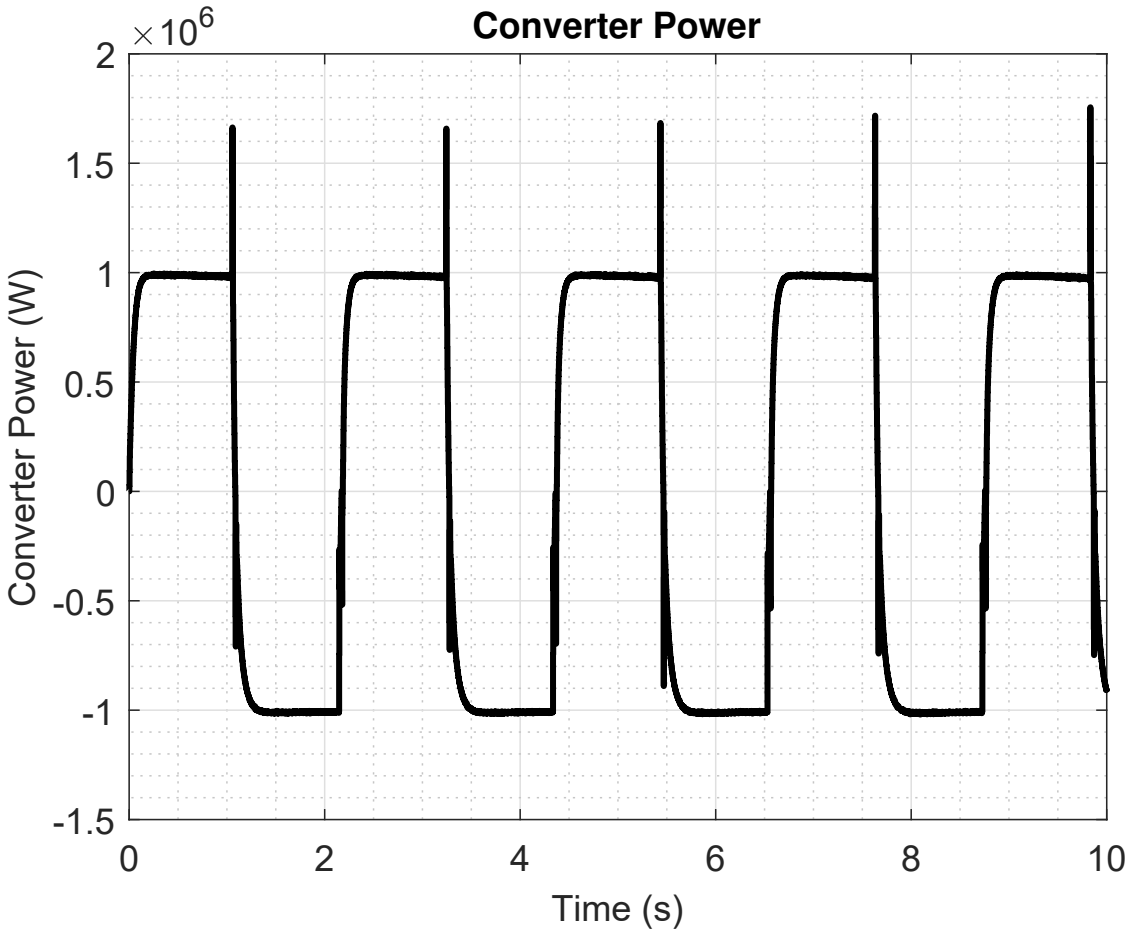

Figure 6.4 *Converter power when the supercapacitor is discharging and charging.*

Section 4.3 could be implemented. As a part of future research, this could ramp the converter power down to zero, before switching operation from buck to boost or vice versa.

The duty cycle for the buck and boost mode is calculated in (4.8) and (4.9). At the beginning of the operation, the supercapacitor voltage decreases as the dc link voltage remains constant at 2 kV. The dynamic response of the dc-dc converter depends on its operating point, which is time-variant and changes periodically. The closed-loop system response must be satisfactory during all anticipated conditions. The duty cycle can be seen in Fig. 6.5. Since the duty cycle also changes as the supercapacitor voltage changes, the duty cycle at each operating point can be calculated by using the initial value of the supercapacitor voltage. For example, initial SC voltage $V_{\mathrm{sc,ini}}$ gives the minimum theoretical duty cycle in the boost mode:

$$d_{\mathrm{min,boost}} = 1 - \frac{607.2\,V}{2000\,V} = 0.696 \approx 0.7 \tag{6.1}$$

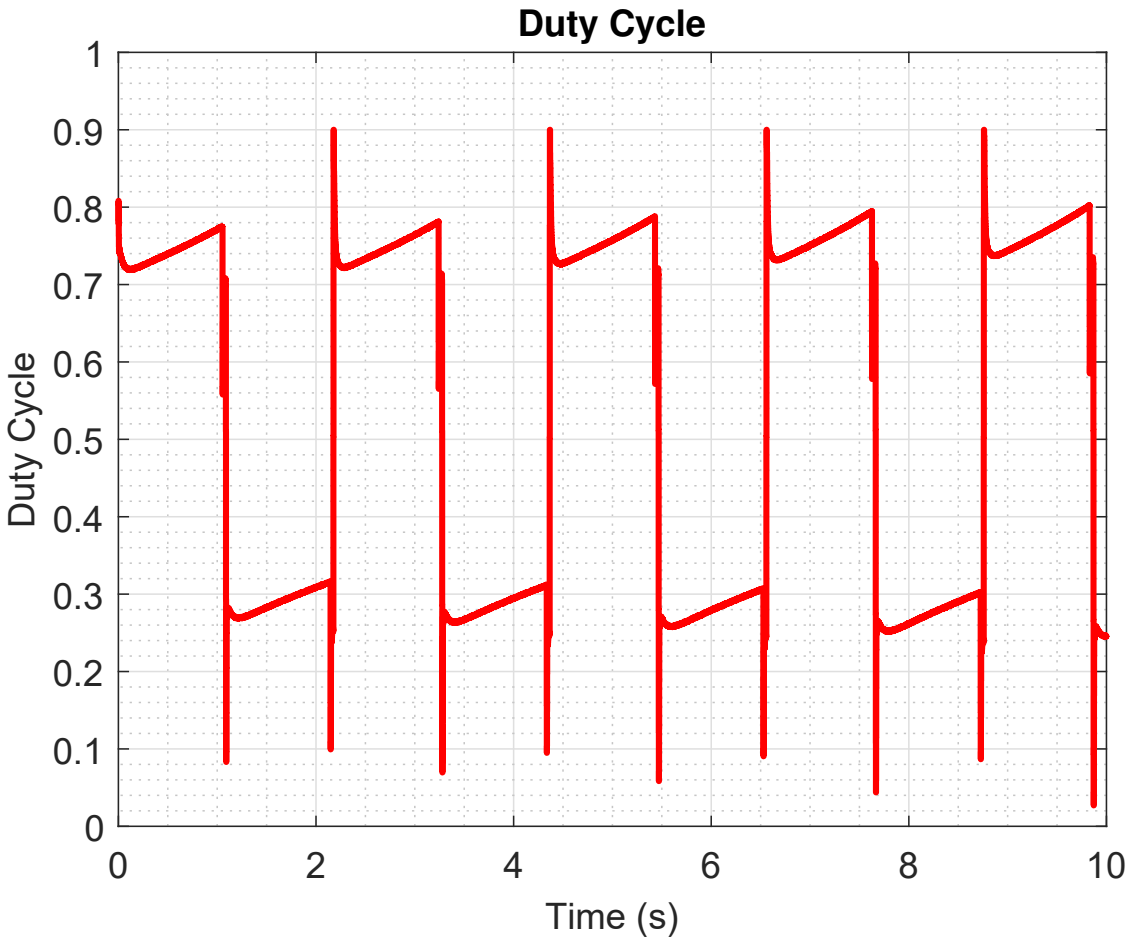

Figure 6.5 *Duty cycle of the converter changes in the buck and boost mode and is time variant.*

The minimum value of the duty cycle in boost mode in Fig. 6.5 is approximately 0.7 (A bit more since the converter power has not stabilized at this point.) Minimum supercapacitor voltage $V_{\mathrm{SC,min}}$ gives maximum duty cycle in boost mode:

$$d_{\mathrm{max,boost}} = 1 - \frac{409.84\,V}{2000\,V} = 0.795 \approx 0.8 \tag{6.2}$$

The duty cycle is saturated to 0.95 to avoid violation of the physical limit that it has to be in, as seen in Fig. 6.5. The minimum duty cycle limit is zero. The $I_{\mathrm{peak,max}}$ is never reached. This means that the minimum voltage, where the supercapacitor is discharged is larger than the minimum supercapacitor voltage calculated with the $I_{\mathrm{peak,max}}$. This reduces the maximum boost mode duty cycle (if the spikes are not considered) to approximately 0.77. This can be confirmed by calculating the duty cycle with a simulated minimum voltage of 468.8 V, which can be seen Fig.

6.2. The actual maximum duty cycle in boost mode:

$$d_{\text{max,act,boost}} = 1 - \frac{468.8\,V}{2000\,V} = 0.765 \approx 0.77 \tag{6.3}$$

The same calculations can be done for minimum and maximum duty cycles in buck mode. Minimum supercapacitor voltage gives the actual minimum duty cycle in buck mode:

$$d_{\text{min,act,buck}} = \frac{468.8\,V}{2000\,V} = 0.234 \approx 0.23 \tag{6.4}$$

However, the duty cycle exhibits some overshoot that reach zero at the beginning of the buck mode, as the operation mode changes. In addition, the minimum duty cycle in the beginning of the buck operation is slightly more in reality. (The converter power has not stalibized at this point.)

In theory, the supercapacitor should be charged back to its initial value $V_{\text{sc,ini}}$. However, the simulations indicate that the supercapacitor value at the end of the buck mode is 614 V, as seen in Fig. 6.2. This gives the maximum duty cycle value in the buck mode before the mode change:

$$d_{\text{max,act,boost}} = \frac{614.5\,V}{2000\,V} = 0.307 \approx 0.31 \tag{6.5}$$

These calculations show that the simulated duty cycle corresponds to the theoretically estimated duty cycle.

6.3 Thermal Analysis

It is important to analyze the thermal behavior of the semiconductor device to get information on how to build, operate, and maintain the system. It is critical to calculate the temperatures accurately and analyze the temperature of the system. Especially IGBT modules are heated up while exposed to repeated charging and discharging cycles. During the test cycle, the power losses of each IGBT and FWD are simulated and calculated. The power losses are calculated during one power cycle, which includes a boost mode and a buck mode. The power losses are roughly the same over each cycle. Thermal simulations determine whether the maximum junction temperature $T_{\text{j,max}}$ stays below the maximum temperature in the datasheet (150 °C), seen in Table 5.2.

As seen from the junction temperatures shown in Figure 6.6, the junction temperature of lower controllable switch S_2 and upper diode D_1 increase in boost operation. In buck operation, the temperature of the upper controllable switch S_1 and lower diode D_2 increases instead. This is in line with the current paths shown in Chapter

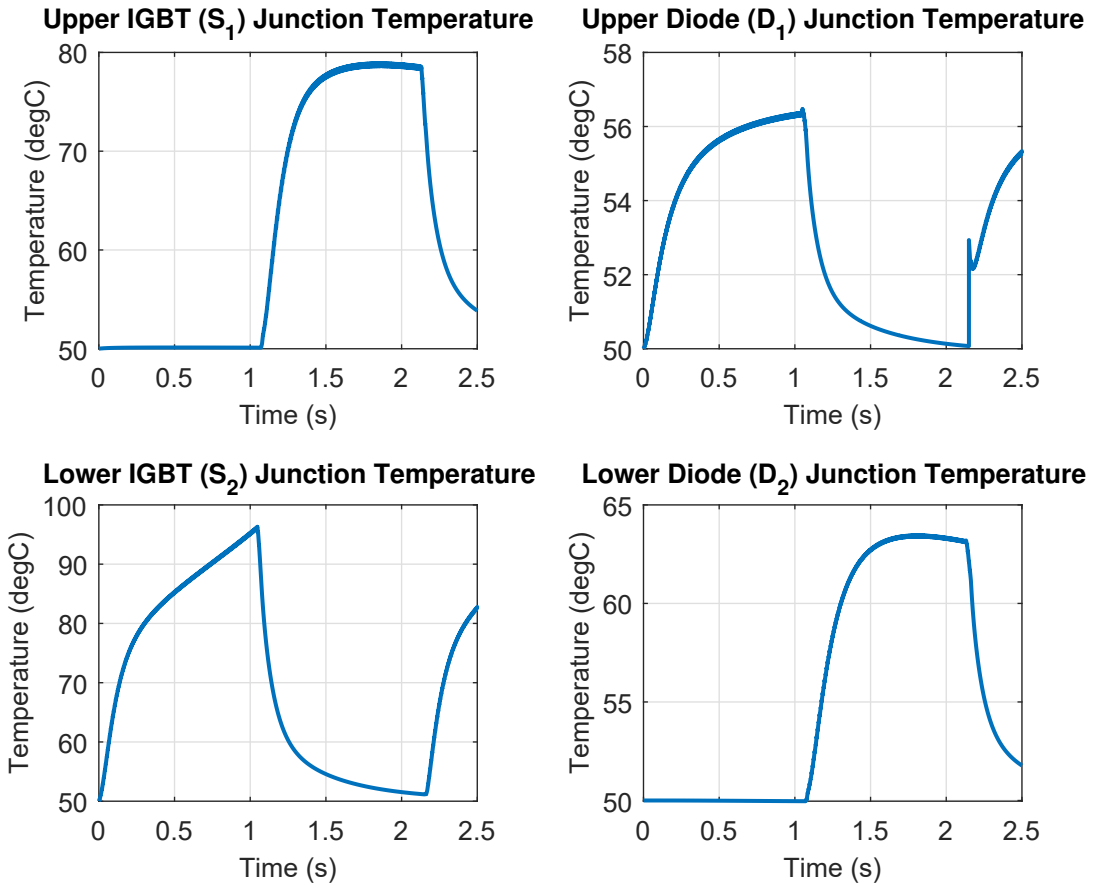

Figure 6.6 *IGBT and junction temperatures during buck and boost operation.*

4 Figures 4.9 and 4.10. In boost operation, the current and thus the power flows through the lower IGBT and the upper diode. The path depends on the on- and off-times. Due to the high frequency both the lower IGBT and the upper diode heat up during boost operation. In buck operation, the power flows through the upper IGBT or the lower diode heating up the device. These temperature variations resemble the power cycle test where the IGBT temperature profile is created based on injected power [27], as seen in Fig. 5.3. These simulations indicate that the temperatures of the IGBT junctions remain below the maximum value of 150 °C. The different current incurs different losses and this results in different junction temperatures. The rapid increase in the upper diode D_1 temperature seen in Fig. 6.6 is likely caused by a power surge, caused by the reversal of the inductor current.

From the power losses shown in Figure 6.7, it is seen that both the peak and the average (mean) power dissipated when the lower controllable switch S_2 and upper diode D_1 are conducting increases with time in boost operation. That is because of the increase in the supercapacitor current. Similarly, the losses decrease in buck operation, which is because of the decrease of the supercapacitor current. It is also

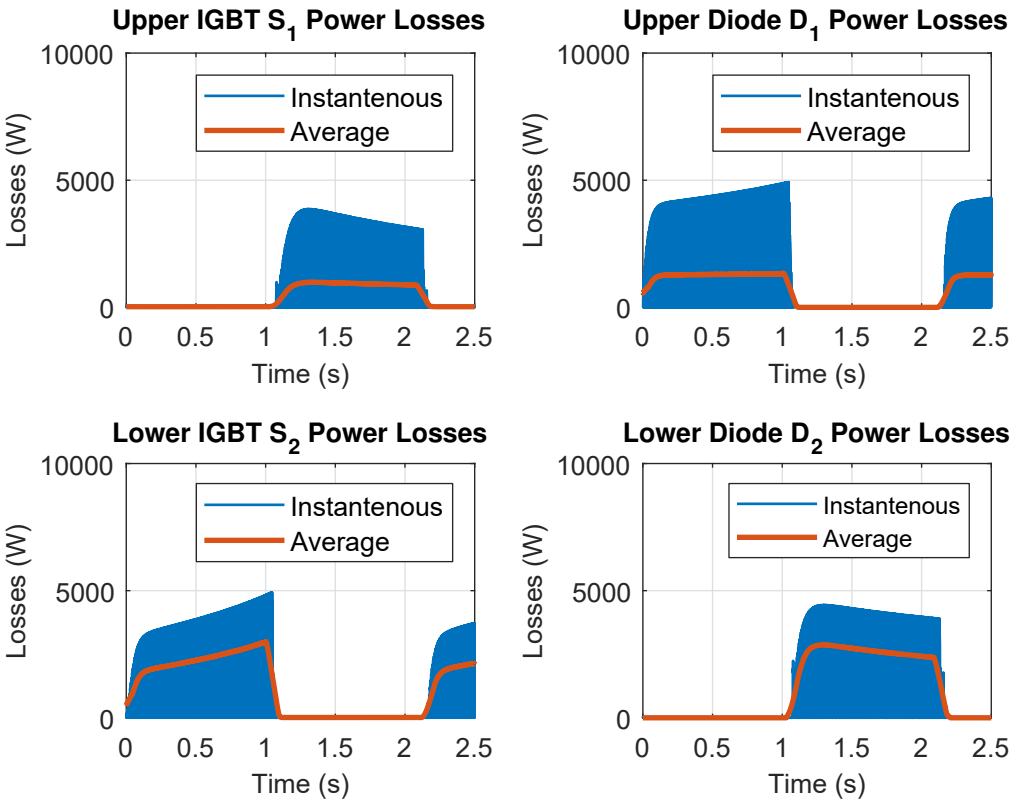

Figure 6.7 *IGBT and diode power losses during buck and boost operation.*

seen, that the average (mean) losses are significantly less than the instantaneous losses. It should be noted that the losses shown in Fig. 6.7 include both conduction and switching losses, as they are calculated by MATLAB Simscape. However, in thesis the conduction and switching losses are not differentiated.

7 CONCLUSIONS

This thesis focuses on integrating an energy storage element into a modular multilevel converter (MMC). MMCs are reliable and efficient voltage source converters that have high modularity. Energy storage can supply or absorb power, and the amount of power depends on the energy storage element and the design. A supercapacitor is used as an energy storage element due to its high power density, charge and discharge speed, and other properties appropriate for the application. An optimal number of supercapacitor modules is connected in series to form the supercapacitor energy storage element. In this thesis, the energy storage elements distributed to the MMC submodules were studied.

This thesis presents the operation of a dc-dc converter connected in the interface of the MMC and the supercapacitor. The converter works as a bidirectional buck-boost converter, with the target of 1 MW power flowing in both directions. Two IGBT modules are chosen for the converter based on the maximum peak current of the supercapacitor and the current ratings of the IGBT module. An inductor is chosen based on the allowed current ripple, frequency, and output and input voltages.

The converter is simulated using MATLAB Simulink software. The number of supercapacitor modules that provide the desired amount of energy of at least 1 MJ in both directions can be calculated. The optimal number of supercapacitor modules can be confirmed by simulating the converter power and the supercapacitor current. Based on simulation results, the bidirectional dc-dc converter steps up the supercapacitor voltage from initial supercapacitor voltage $v_{\mathrm{sc,ini}}$ to dc link voltage V_{dc} and steps down the dc link voltage to charge the supercapacitor again. This cycle can be repeated multiple times without major power losses. The duty cycle and the power and current waveforms behave according to the theoretical analysis discussed before the simulations. Thus the performance of the energy storage system is as expected. The thermal behavior and power losses of the system are simulated and the results are analyzed. The power losses are calculated over one power cycle where the supercapacitor discharges and charges.

7.1 Future Research

To achieve higher power output, a dual-active bridge (DAB) converter can be used instead of the bidirectional buck-boost converter. Component sizing calculation and simulation study could be performed for such a converter.

In this thesis, the dc link voltage is modeled as an ideal voltage source. But in reality, the dc link could rather be a weak voltage source, meaning that the voltage at the converter terminals varies based on the converter output. This can be modeled by adding an impedance between the ideal voltage source and the converter. Furthermore, the voltage ripple can be 40 % of the dc link voltage. It would be interesting to simulate the converter operation and verify the component selection with these improvements to the simulation model.

The dc-dc converter presented in this thesis uses a PI controller, with the same controller gains in buck and boost operation. Two different PI controllers or two different set of parameters for buck and boost modes would allow better control and operation of the converter. The PI controllers could be tuned using more sophisticated methods than ZN tuning. Furthermore, it would be interesting to implement a model predictive controller (MPC) for the converter to improve its performance.

Bibliography

[1] A. Hillers, M. Stojadinovic, and J. Biela, "Systematic comparison of modular multilevel converter topologies for battery energy storage systems based on split batteries," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1–9, Sept. 2015.

[2] E. Spahic, C. P. Susai Sakkanna Reddy, M. Pieschel, and R. Alvarez, "Multilevel STATCOM with power intensive energy storage for dynamic grid stability - frequency and voltage support," in *2015 IEEE Electrical Power and Energy Conference (EPEC)*, pp. 73–80, Oct. 2015.

[3] S. G. Mian, P. D. Judge, A. Junyent-Ferŕ, and T. C. Green, "A Delta-Connected Modular Multilevel STATCOM With Partially-Rated Energy Storage for Provision of Ancillary Services," *IEEE Transactions on Power Delivery*, vol. 36, pp. 2893–2903, Oct. 2021.

[4] R. O. d. Sousa, D. d. C. Mendonça, W. C. S. Amorim, A. F. Cupertino, H. A. Pereira, and R. Teodorescu, "Comparison of double star topologies of modular multilevel converters in statcom application," in *2018 13th IEEE International Conference on Industry Applications (INDUSCON)*, pp. 622–629, 2018.

[5] P. D. Judge and T. C. Green, "Modular Multilevel Converter With Partially Rated Integrated Energy Storage Suitable for Frequency Support and Ancillary Service Provision," *IEEE Transactions on Power Delivery*, vol. 34, pp. 208–219, Feb. 2019.

[6] A. Abdelhakim, F. Blaabjerg, and H.-P. Nee, "Single-Stage Boost Modular Multilevel Converter (BMMC) for Energy Storage Interface," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, pp. P.1–P.10, Sept. 2020.

[7] J. Yin, J. I. Leon, L. G. Franquelo, S. Vazquez, and A. Marquez, "Cost-effective design of modular multilevel converter employing full-bridge submodules," in *2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, pp. 1–6, 2019.

[8] J. H. D. G. Pinto, W. C. S. Amorim, A. F. Cupertino, H. A. Pereira, S. I. S. Junior, and R. Teodorescu, "Optimum Design of MMC-Based ES-STATCOM Systems: The Role of the Submodule Reference Voltage," *IEEE Transactions on Industry Applications*, vol. 57, pp. 3064–3076, May 2021.

[9] F. Hahn, L. Camurca, and M. Liserre, "Investigation of Modular Multilevel Converters for E-STATCOM Applications," in *2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*, pp. 1028–1032, June 2020.

[10] E. E. Division, "The major differences between supercapacitors and batteries," in *Eaton battery vs supercapacitor whitepaper*, 2022.

[11] L. Baruschka and A. Mertens, "Comparison of Cascaded H-Bridge and Modular Multilevel Converters for BESS application," in *2011 IEEE Energy Conversion Congress and Exposition*, pp. 909–916, Sept. 2011.

[12] F. Errigo, L. Chédot, P. Venet, A. Sari, P. Dworakowski, and F. Morel, "Assessment of the Impact of Split Storage within Modular Multilevel Converter," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, pp. 4785–4792, Oct. 2019.

[13] S. P. Ahmed Abdelhakim, Paolo Mattavelli and G. Spiazzi, "Bidirectional dc-dc converter topologies for low-voltage battery interface: Comparative assessments," *IEEE 4th International Forum on Research and Technology for Society and Industry (RTSI)s*, 11 2018.

[14] Eaton, *XLM Supercapacitor 62 V and 69 V, 130 F Module*, 7 2021.

[15] S. Dinglasan-Fenol, F. S. Caluyo, and W. Sugimoto, "Effect of charging methods on self-discharge and leakage current of supercapacitors," in *2016 4th International Conference on Control Engineering and Information Technology (CEIT)*, pp. 1–5, 2016.

[16] G. Si, Z. Shen, Z. Zhang, and R. Kennel, "Investigation of the limiting factors of the dead time minimization in a h-bridge igbt inverter," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, pp. 1–6, 2016.

[17] R. D. Bhagiya and R. M. Patel, "Pwm based double loop pi control of a bidirectional dc-dc converter in a standalone pv/battery dc power system," in *2019 IEEE 16th India Council International Conference (INDICON)*, pp. 1–4, 2019.

[18] J. M. Blanes, R. Gutiérrez, A. Garrigós, J. L. Lizán, and J. M. Cuadrado, "Electric vehicle battery life extension using ultracapacitors and an fpga controlled interleaved buck–boost converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5940–5948, 2013.

[19] C. Qian, A. M. Gheitaghy, J. Fan, H. Tang, B. Sun, H. Ye, and G. Zhang, "Thermal management on igbt power electronic devices and modules," *IEEE Access*, vol. 6, pp. 12868–12884, 2018.

[20] Infineon FZ2000R33HE4 Datasheet, *IHM-B module*, 11 2022. Rev 1.10.

[21] W. Wu, M. Held, P. Jacob, P. Scacco, and A. Birolini, "Investigation on the long term reliability of power igbt modules," in *Proceedings of International Symposium on Power Semiconductor Devices and IC's: ISPSD '95*, pp. 443–448, 1995.

[22] P. Khatri and J. Ziemski, ""dry-to-the-touch" thermal grease," in *Proceedings International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces (IEEE Cat. No.01TH8562)*, pp. 236–239, 2001.

[23] X. Li, Y. Wang, G. Chang, X. Huang, W. Gong, Y. Chen, Z. Wang, M. Packwood, H. Luo, and G. Liu, "Thermal imbalance among paralleling chips in power modules and the impact from traction inverter system view," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 3, pp. 2231–2240, 2023.

[24] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7183–7193, 2016.

[25] Z. Zhou, P. Holland, and P. Igic, "Compact thermal model of a three-phase igbt inverter power module," in *2008 26th International Conference on Microelectronics*, pp. 167–170, 2008.

[26] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of igbt modules in traction application," in *Proceedings of Second International Conference on Power Electronics and Drive Systems*, vol. 1, pp. 425–430 vol.1, 1997.

[27] U.-M. Choi, F. Blaabjerg, and S. Jørgensen, "Power cycling test methods for reliability assessment of power device modules in respect to temperature stress," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, 2018.

[28] A. McCormack and K. Godfrey, "Rule-based autotuning based on frequency domain identification," *IEEE Transactions on Control Systems Technology*, vol. 6, no. 1, pp. 43–61, 1998.

[29] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631–1656, 2017.

[30] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3702–3713, 2013.