Tampere University

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Flexible, Low-Voltage, Metal Oxide Thin Film Transistors (TFT) and Circuits for Wearables and Internet of Things (IoT)

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ACADEMIC DISSERTATION
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ABSTRACT

Multifunctional flexible electronics are booming in many ways. Flexible electronics have opened up a world of possibilities for their widespread use in smart electronics such as artificial electronic-skin (e-skin), flexible displays, consumer electronics, implantable devices. Flexible devices and sensors are paramount in order to realize the true potential of flexible electronics, wearable eco-systems, biomedical and anticipated pervasive Internet of Things (IoT). With special properties like enhanced flexibility, light weight and conformability, flexible technology allows a seamless system integration. Although today's modern electronics are capable of performing everyday needs in existing applications, flexible electronics can provide potential solutions for many as yet unseen applications which requires lower processing capacity, low cost as well as thin, lightweight and environmentally friendly products. To fulfill the needs of a diverse range of applications, next-generation flexible electronics should be engineered with added flexibility and mechanical deformability, by exploring new materials and tactics to overcome the limits of traditional methods.

At the moment, enhanced device performance, greater integration density, fabrication cost and advanced functionality are propelling the traditional silicon semiconductor technology and electronics industry forward, servicing traditional macro-electronic sectors (e.g., mobile phones, laptops, routers, automotive). This unquenchable need for higher performing electronic devices necessitates new technological advances and keeps costs high. The overall performance of modern silicon-based devices and technologies are reaching new levels. With the ballooning consumer electronics needs; the global semiconductor industry is expected to remain growing robustly. But rather than competing with well-developed rigid silicon devices, the goal for flexible electronics is to improve the efficiency of current state-of-the-art thin film transistors (TFTs), required for low energy flexible wearables and Internet of Things (IoT), and mature these designs for low-cost, printable manufacturing.

Thin film transistors (TFTs) are among the most important thin film devices and can form the foundation of any electronic system and application. In this regard,

metal oxide semiconductors are viewed as a potential candidate for flexible electronics, due to a broad range of properties, such as a large band gap, high optical transparency, high mobility, and solution processable deposition at low temperatures compared to CMOS processes. However, despite a dedicated effort by the research community and industry, metal oxide thin film transistors still face great challenges being used in flexible electronics, wearables, and Internet of Things (IoT), such as operating voltage, switching speed, on-off ratio, process temperature and gate dielectric deposition compatible for flexible substrates.

The present thesis investigates solution-processed metal-oxide thin film transistors (TFTs) and inverter circuits for flexible electronics. The low-voltage (< 3 V) thin film transistors using indium oxide (In_2O_3), gallium oxide (Ga_2O_3) and indium gallium zinc oxide (IGZO) as the active channel semiconductor were fabricated on solid (glass) and flexible (polyimide) substrates. The low-voltage operating thin film transistors were accomplished by following low temperature solution processing and room-temperature anodization routes for metal oxide semiconductor and gate oxide dielectric deposition, respectively. The incorporation of anodized high-κ aluminum oxide (Al_2O_3) for gate dielectric into the TFT fabrication process has significantly helped to reduce operating and threshold voltages while also improving carrier mobility. On the other hand, solution processing allows low-temperature, large-area deposition while lowering fabrication costs.

The solution-processed metal-oxide TFTs show excellent electrical performance, at a low gate voltage (V_g), which could enable novel applications in flexible electronics. Along with electrical characterization, bending performance and SPICE simulation results are also presented. Furthermore, thorough thin film characterization and interface analysis between oxide semiconductor and gate dielectric were performed, using various characterization techniques, such as C-V (Capacitance-voltage) profiling, AFM (atomic force microscopy), TEM (transmission electron microscopy) and TLM (transfer length measurement). Additionally, a low-voltage flexible inverter circuit using solution-processed metal-oxide thin film transistors was fabricated and characterized. The results indicate that flexible, low voltage operating devices and circuits enable a viable alternative to silicon dominated semiconductor devices, and hence a path forward, for wearables and Internet of Things (IoT).

CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

TFTs	Thin Film Transistors
IoT	Internet of Things
MO	Metal oxide
In_2O_3	Indium oxide
Ga_2O_3	Gallium oxide
IGZO	Indium gallium zinc oxide
Al_2O_3	Aluminum oxide
AFM	Atomic force microscopy
TEM	Transmission electron microscopy
TLM	Transfer length measurement
MOS	Metal oxide semiconductor
V_G	Gate voltage
V_D	Drain voltage
I_D	Drain current
V_{th}	Threshold voltage
μ	Mobility
D_{it}	Trap state densities
PI	Polyimide
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
a-Si	Amorphous silicon
LTPS	Low temperature polysilicon
R&D	Research and development
RFID	Radio-frequency identification
IV	Current voltage
CV	Capacitance voltage
FETs	Field effect transistors
AMLCD	active-matrix liquid-crystal display
ICs	Integrated circuits
Si	Silicon

CPM	Conduction band minimum
VBM	Valence band maximum
EHD	Electrohydrodynamic
HfO_2	Hafnium oxide
ZrO_2	Zirconium oxide
SiO_2	Silicon oxide
MOSFET	Metal oxide semiconductor field effect transistors
CMOS	Complementary metal oxide semiconductors
W	Channel width
L	Channel length
C_{ox}	Oxide capacitance
V_{BD}	Breakdown voltage
I_{ON}/I_{OFF}	Current ratio
SS	Subthreshold swing
g_m	Transconductance
g_p	Peak conductance
f	Frequency
q	Electronic charge
R_c	Contact resistance
BGTC	Bottom gate – top contact
BGBC	Bottom gate – bottom contact
TGTC	Top gate – top Contact
TGBC	Top gate – bottom Contact
Al	Aluminum
Au	Gold
Ti	Titanium
IPA	Isopropanol
DI	Deionized

LIST OF PUBLICATIONS

Publication I Sagar R. Bhalerao, Donald Lupo, Amirali Zangiabadi, Ioannis Kymissis, Jaakko Leppaniemi, Ari Alastalo and Paul R. Berger, "0.6V Threshold Voltage Thin Film Transistors with Solution Processable Indium Oxide (In_2O_3) Channel and anodized high-κ Al_2O_3 Dielectric", IEEE Electron Device Letters, May 2019.
DOI: 10.1109/LED.2019.2918492

Publication II Sagar R. Bhalerao, Donald Lupo and Paul R. Berger, "2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton", IEEE Xplore, IEEE International Flexible Electronics Technology Conference (IFETC), Aug. 2019.
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Publication V Sagar R. Bhalerao, Donald Lupo and Paul R. Berger, "Flexible Thin Film Transistor (TFT) and Circuits for Internet of Things (IoT) based on Solution processed Indium Gallium Zinc Oxide (IGZO)", IEEE International Flexible Electronics Technology Conference (IFETC), Aug. 2021.
DOI: 10.1109/IFETC49530.2021.9580506

1 INTRODUCTION

1.1 Motivation

One would wonder why anyone would want to look beyond the well-established and highly popular amorphous silicon (a-Si) technology and the availability of low temperature polysilicon (LTPS) when higher performance TFTs are needed. Despite this fact, TFT research and development (R&D) has expanded greatly in recent years in a quest to surpass a-Si. There are some strong driving forces for the continuous R&D effort, the first of which is fabrication cost reduction [1, 2]. Since the demand for much bigger display is rising in popularity, the materials cost is not as big an issue as it is with equipment and processing complexity, which accounts for more than half of the manufacturing cost. As a result, the primary goal is to reduce the number of manufacturing steps, while also simplifying the machinery. Therefore, simple solution deposition and printing methods may be used instead of vacuum deposition and photolithography [3, 4].

The second driving force is flexible electronics. The most popular substrate for TFT processing is glass or silicon, but its rigidity makes it easily breakable. Thus, lightweight, rugged displays with the added flexibility of being rollable, bendable, or foldable, and requiring no more maintenance than a paper document, are highly desirable. Mobile phones with roll-up display, e-books and electronic paper, and electronic smart cards are just a few of these applications [5]. Along with flexible displays, new functionality and applications such as radio-frequency identification (RFID) tags, transparent electronics, medical patches that can be applied to the skin to administer medications or track vital signs, disposable food quality monitor labels, novelty gadgets, Internet of Things (IoT), wearables and more are all possibilities [6, 7]. Therefore, with an eye on all upcoming future applications, flexible thin film transistors must be developed to meet modern needs rather than trying to replace established silicon [8-10].

1.2 Structure of the Thesis

The present thesis consists of total six chapters and five peer-reviewed publications, of which four are already published and one is accepted. The first chapter gives a broad overview of the subject, lays out the thesis' structure, and describes the author's contributions to publications. General insights of thin film transistors, materials and flexible electronics are presented in Chapter 2. Chapter 3 provides an overview of TFTs along with fabrication techniques and electrical parameters. The different materials, substrates and tools used for device fabrication are described in Chapter 4. In Chapter 5, device architecture along with comprehensive flexible TFTs and circuit fabrication, along with electrical performance and device characterization, is presented. The major findings are summarized in Chapter 6, and the publications are included at the end of the thesis.

1.3 Aim and Scope of the Dissertation

Despite the focused effort and research on metal oxide semiconductors for thin film transistors (TFTs), the operating voltage, switching speed, on-off ratio, reproducibility, high temperature and vacuum processing are impeding them from being used in flexible electronics, wearables and Internet of Things (IoT). The majority of today's state-of-the-art metal oxide TFTs employ ALD (Atomic layer deposition), PLD (pulsed laser deposition), HVPE (halide vapor phase epitaxy), MBE (molecular beam epitaxy), MOVPE (metalorganic vapor phase epitaxy), and other expensive, high temperature and/or high vacuum deposition techniques, spatially for the gate dielectric and/or channel semiconductor deposition and processing. As a result of sophisticated equipment and complex processing, the cost of the manufacturing increases significantly. This makes them too expensive to scale to the trillions of IoT devices envisioned. Additionally, glass or silicon are the most common widely used substrates for TFT fabrication, however their hardness makes them readily breakable. They are also unsuitable for flexible wearable applications due to their rigidity, which may produce discomfort to the wearer.

The solution processing is believed to be one of the key routes to ultra-low-cost, light weight, easy processability, high-mechanical flexibility, which could be well exploited in scalable fabrication techniques for achieving a long standing goal of economic and high performance circuit fabrication. Low voltage operation, high

performance circuitry is, together with energy autonomy, a key requirement for the anticipated "Wearables and Internet of Things (IoT)" to become reality. Therefore, the development of flexible thin film transistors (TFTs) and circuits based on solution-processed metal oxide semiconductors would open up an entirely new realm of possibilities in flexible wearable electronics.

The main objectives of the thesis are –

- To reduce the number of fabrication steps while also utilizing simpler equipment instead of vacuum deposition and photolithography.
- To investigate solution processing routes for active semiconductor (metal oxide) deposition at low temperature.
- To explore low temperature gate dielectric deposition methods compatible for flexible substrates.
- The fabrication of the low voltage (< 3 V) thin film transistors with a reliable device performance at relatively low temperature.
- Fabrication and characterization of low voltage flexible TFTs and circuits for low energy flexible wearables and Internet of Things (IoT).

The scope of this thesis is to investigate the use of different metal oxide semiconductors for the fabrication of flexible thin film transistors and circuits for wearables and the Internet of Things (IoT) by combining solution processing with a room temperature deposited anodized high-κ dielectric. In addition to electrical characterization, device performance under bending, interface analysis, and materials characterization are all covered in detail. Initially, TFTs were fabricated on glass substrates to create a device fabrication prototype, which was then used as a reference before the same architectures and processes were moved to flexible substrates. Henceforth, the flexible TFTs and inverter circuit were fabricated on flexible polyimide (Kapton) substrates following the same processes. The device performance analysis includes electrical characterization through current-voltage (IV) and capacitance-voltage (CV) measurements, contact resistance with the help of the transfer length measurement (TLM) method and interface studies using trap states density (D_{it}). Furthermore, thin film and material characterization were performed via cross sectional transmission electron microscopy (TEM) and atomic force microscopy (AFM).

1.4 The Author's Contribution

Publication I. The author was responsible for the majority of the work, including indium oxide (In_2O_3) TFT fabrication and measurements along with manuscript writing. Amirali Zangiabadi performed the cross sectional TEM measurements. Prof. Donald Lupo and Prof. Paul R. Berger have assisted in the design of experiments and data interpretation as well as revising and improving the manuscript. Other co-authors also revised and improved the manuscript.

Publication II. The author was the main contributor and written the manuscript. The author fabricated the flexible TFTs and performed data analysis. The manuscript was revised and improved with the assistance of Prof. Donald Lupo and Prof. Paul R. Berger.

Publication III. The author was the main contributor. Flexible TFT and inverter circuit fabrication, electrical characterization and bending performance were carried by the author. The author analyzed the results and was responsible for the manuscript writing. With manuscript revision and improvement, Prof. Donald Lupo and Prof. Paul R. Berger have closely monitored the TFT modeling and bending performance.

Publication IV. The author was the main contributor. The author designed, fabricated, and characterized the gallium oxide (Ga_2O_3) based flexible TFTs, performed data analysis and drafted the manuscript. With the help of Prof. Donald Lupo and Prof. Paul R. Berger, the manuscript was revised and improved.

Publication V. The author made the main contribution. The flexible TFTs based on indium gallium zinc oxide (IGZO) were fabricated and characterized by the author. He also wrote the manuscript. The manuscript was rephrased and updated with the help of Prof. Donald Lupo and Prof. Paul R. Berger.

2 BACKGROUND

The chapter aims to provide a brief outline of the basic concepts of the device and processes utilized in the thesis. The thin film transistor (TFT) is discussed first, followed by metal oxide semiconductors. The solution processing and high-κ gate dielectric are explored in the subsequent sections. A discussion of flexible electronics concludes the chapter.

2.1 Thin Film Transistors (TFTs)

Realization of a transistor is a milestone in the context of the development of modern microelectronics since the control (i.e., gate) electrode empowers the implementation of functions, such as logic circuits, memory, amplification, processing and conditioning of electronic signal, which play a pivotal role in today's advanced technology [11-13]. Over the decades, transistors have been the foremost building blocks for electronics and continue to form the basis of today's modern devices and technological gadgets. There are many other types of transistors, but field effect transistors (FET) are the most often utilized, namely the metal-oxide-semiconductor field-effect-transistor (MOSFET). They have attracted a lot of attention as an electronic device for a variety of applications, including active-matrix liquid-crystal displays (LCDs), radio frequency identification (RFID) tags, opto-electronics, bio-medical devices, and more recently, flexible devices, printed RFID, and wearable devices [14, 15].

TFTs have similar origins as silicon MOSFET (Metal oxide semiconductor filed effect transistors) and integrated circuits (ICs), but each of these technologies has its own set of applications. With the advancements in fabrication techniques, for the silicon ICs, size is not an unsurmountable limitation, hence silicon ICs have become increasingly dense, and as the feature size is reduced, the cost goes down and performance increase [16, 17]. However, the availability of CMOS chips to populate ever increasing IoT demands could become a limitation as the number of IoT devices reaches the trillions, as is predicted [18]. TFTs, on the other hand, are driven

by large substrate size rather than system density [19]. TFTs have a lower cost per unit area than silicon ICs due to different fabrication processes, but the cost per FET is much higher [20-22].

2.2 Metal Oxide Semiconductors

Metal oxide semiconductors form a distinct class of materials owing to their electrical charge transfer properties, as opposed to traditional covalent semiconductors such as silicon (Si) [23]. Metal oxide semiconductors have received a lot of attention and growth in recent years, due to a broad range of properties that set them apart from traditional silicon, such as a large band gap, high optical transparency, high mobility, and solution processable deposition at low temperatures. Metal oxide semiconductors are high-ionic-bonding valence compounds that contain at least one of the metal cations Zn, In, Ga, Sn, and Cd. The metal (M) ns orbital and oxygen (O) 2p orbitals dominate their conduction band minimum (CBM) and valence band maximum (VBM), respectively [24, 25].

Furthermore, in metal oxides, the charge carrier transport is slightly different due to the interaction between the metal and oxide orbitals. Even though electronic band structures in metal oxide semiconductors allow electron or hole transport, intrinsically achieving a good n-type or p-type conductivity is difficult [26]. Intrinsic point defects act as donors or acceptors in metal oxide semiconductors. However, in general, band gaps are often too large and defect levels too deep to have high concentration carriers. Hence, to achieve moderate or high conductivity, extrinsic doping is required [27, 28]. Nonetheless, despite some shortcomings, metal oxides are regarded as a crucial next generation semiconductor with significant promise, thanks to their outstanding advantages in terms of cost-effective fabrication, simple manufacturing process, environmentally safe production, fast composition changes, and high throughput [29, 30]. Therefore, metal oxide semiconductors have been extensively studied for thin film transistors [31, 32].

2.3 Solution Processing

Solution processing is thought to be one of the main routes to ultra-low cost, light weight, fast processability, high-mechanical flexibility, which could be well suited in

scalable fabrication techniques for achieving a long-standing target of cost-effective and high-performance electronic circuits [33]. Low-voltage operation and high-performance circuitry, as well as energy autonomy, are essential for the "Wearables and Internet of Things (IoT)" to become a reality [34, 35]. Generally, there are two types of solution deposition processes: entire/whole area deposition and selective area deposition. For entire area deposition, spin-coating, dip-coating, and chemical bath deposition are often used, while for selective area deposition, printing methods are used. Amongst all, the most popular methods for depositing oxide films are spin-coating, spray-coating, and printing process such as inkjet, gravure, flexography, aerosol jet, electrohydrodynamic (EHD) jet [36, 37].

Spin coating is the commonly used method for the entire area deposition since the resulting devices outperform their printed counterparts in terms of efficiency and durability. However, in recent years, as printing methods have become more popular, selective area deposition has become extremely significant because of lesser material wastage, cost effectiveness, environmentally sustainable processing, and improved device performance [38-42].

2.4 High-κ Gate Dielectrics

The gate dielectric layer has a significant impact on the reliability and overall efficiency of a TFT. A gate dielectric layer contributes to the accumulation of electrons in the active layer by polarization induced by the gate electrode [43-45]. Therefore, numerous studies on gate dielectric have been focused on high-κ oxides such as HfO_2, Al_2O_3, ZrO_2, etc. Since they have a much higher dielectric constant than standard silicon oxide (SiO_2), they empower reduced leakage current while retaining a high capacitance [46-49]. Furthermore, high-κ gate dielectrics also significantly reduce the device operating voltage (10 V or less) compared to silicon oxide devices (~30 V), As a result, TFTs with high-κ gate dielectric can be used in power thrifty devices such as wearables and Internet of Things (IoT) applications. However, to deposit a good quality, high-κ gate dielectric to minimize the gate leakage current and film densification, a high annealing temperature (>1000 °C) is needed [50, 51]. This high processing temperature has prevented high-κ gate dielectrics and metal oxide TFTs from being used in flexible and printed electronics. Therefore, low, or room temperature processing of gate dielectrics is also needed to

achieve a fully flexible TFT, similar to the low temperature method used for the active layer [53-54].

2.5 Flexible Electronics

Modern electronic devices are undergoing a transformative evolution, moving away from being rigid and bulky to being thin, soft, and flexible [55, 56]. The key impetus is to integrate electrical sensors and circuitry into everyday items in order to increase the performance of wearable devices, such as for sports or healthcare applications. Moreover, electronic integration is leading the way for new technologies such as smart tags, artificial robotics, and prosthetic devices along with sophisticated surgical instruments [57-59]. The technology of flexible electronics is now at a stage where device architecture and process integration can propel it. To transform the well-being of mankind through upcoming advanced technologies, electronic devices must be flexible, stretchable, lightweight, and environmentally friendly [60, 61]. In general, thin film transistors (TFTs) are essential components for any flexible electronic system and hence flexible thin-film transistors must fulfill specific requirements, such as reproducibility, reliability, high mobility, low threshold voltage, low temperature processing [62-64], etc. Thus, to envision the full potential of flexible electronics, it is possible that device performance, material efficiency, system integration and circuit design will be pushed to their limits [65, 66]. Figure 1 shows an array of electronic pattern on flexible substrate (for illustrative purpose).

Figure 1. The array of electronic pattern on flexible substrate (for illustrative purpose).

3 OVERVIEW OF THIN FILM TRANSISTORS (TFTs)

This chapter presents a detailed understanding of the basic concept and operating principle of the thin film transistor (TFT), as well as the key parameters. The first section provides an overview of the device's structure, while the subsequent section explores essential device parameters.

3.1 Working Principle

Thin field transistors (TFTs) are field effect devices with 3-terminals, namely - gate, source and drain. In terms of functionality and comprising layers, thin film transistors can be thought of as analogous to field effect devices, such as well-known metal oxide semiconductor field effect transistors in general (MOSFETs) [67]. However, there are significant differences amongst them, some of which may be understood by looking at their conventional architectures shown in Figure 2. Foremost, unlike TFTs, which are fabricated on an insulating substrate, usually glass, MOSFETs have a silicon wafer that serves as both the substrate and the semiconductor. As a result, MOSFETs offer better performance than polycrystalline or amorphous semiconductors since electrons flow in a single crystalline semiconductor with reduced scattering than polycrystalline or amorphous materials.

Furthermore, the temperatures used to fabricate both devices are significantly different, whereas processing temperatures above 1000 °C are typical for MOSFETs, for example to form the dielectric layer, TFTs are restricted by factors like the glass transition of substrate, which for most common glass substrates does not surpass 600 – 650 °C. MOSFETs also possess p-n junctions at the source-drain regions, which aren't present in TFTs. This associates with yet another significant difference in the way the device works, i.e., although both TFTs and MOSFETs depend on the field effect to modulate the conductance of the semiconductor near to its interface with the dielectric, in case of TFTs, an accumulation layer does this, but in MOSFETs, an inversion zone must be created near to the interface; in other words, in a p-type silicon substrate, an n-type conductive layer is formed.

TFTs can be fabricated using solution processing, low temperature and/or low vacuum deposition with amorphous or polycrystalline materials [68, 69]. Similar to the MOSFET, the gate dielectric plays a crucial role in device operation by separating the gate electrode from the active semiconductor material, which is in contact with source-drain electrodes [70]. The dielectric layer was deposited between the semiconductor and a gate contact. The modulation of current that flows through a semiconductor located between the source and drain electrodes is the primary basis of operation for TFT. The electric current flow modulation is generated in the semiconductor channel by capacitive injection and subsequent aggregation of carriers at the semiconductor-dielectric interface, characterized as field effect [71]. Figure 2 shows the general schematic structure comparing the TFTs and MOSFETs.

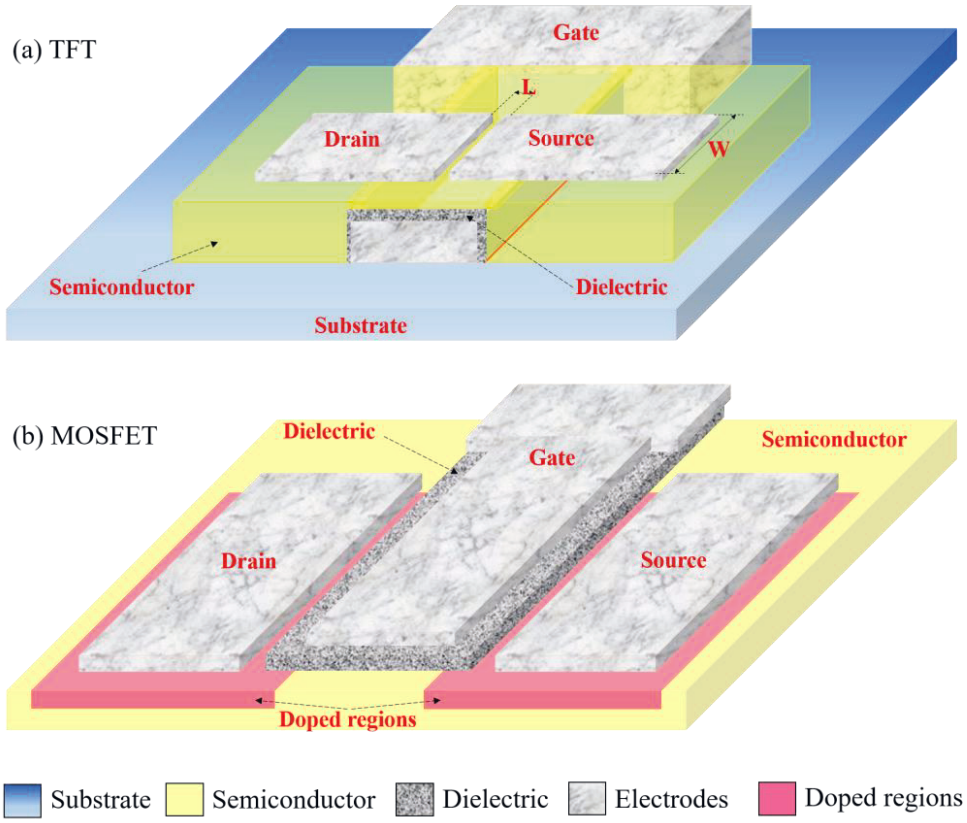

Figure 2. The general schematic structure showing comparison between the TFTs and MOSFETs.

The majority of TFT static parameters are derived from current-voltage (I-V) characteristics i.e., output and transfer characteristics, in two different operating

regimes: linear and saturation. Usually, the values of the drain current (I_d) in the linear and saturation regimes are approximated by equations (1) and (2), respectively [72-78].

$$I_{D,lin} = \frac{W\mu C_{ox}}{L}(V_G - V_{TH})V_D \quad for \quad V_D \leq V_G - V_{TH} \qquad \ldots\ldots\ldots (1)$$

$$I_{D,sat} = \frac{W\mu C_{ox}}{2L}(V_G - V_{TH})^2 \quad for \quad V_D \geq V_G - V_{TH} \qquad \ldots\ldots\ldots (2)$$

Where W is the channel width, μ is the charge carrier mobility, C_{ox} is the specific capacitance of the gate dielectric per unit area, L is the channel length (Figure 2), V_{TH} is the threshold voltage, V_G is the gate voltage and V_D is the drain voltage.

3.2 Parameters of Interest

To understand and analyze the electronic device, a set of electrical parameters needs to be used as a figure of merits. Some of the key parameters used in this dissertation are -threshold voltage (V_{TH}), field effect mobility (μ), current ratio I_{ON}/I_{OFF}, MOS capacitance, breakdown voltage (V_{BD}), transconductance (g_m), Subthreshold swing (SS), contact resistance (R_c) and trap states density (D_{it}).

3.2.1 Current Voltage (IV) Characteristics

The current-voltage (I-V) characteristics, or plots, are the most important parameters to understand the behavior of the device. There are usually two kinds of current-voltage (I-V) characteristics in TFTs. The first is the transfer characteristic (I_D vs. V_G), which is a plot of drain current (I_D) vs. gate voltage (V_G) over a finite number of drain voltages (V_D). And the second is the output characteristic (I_D vs. V_D), which is a plot of drain current (I_D) vs. drain voltage (V_D) over a finite number of gate

voltages (V_G) [78-80]. The general behavior of transfer and output characteristics are represented Figure 3 (a) and (b), respectively.

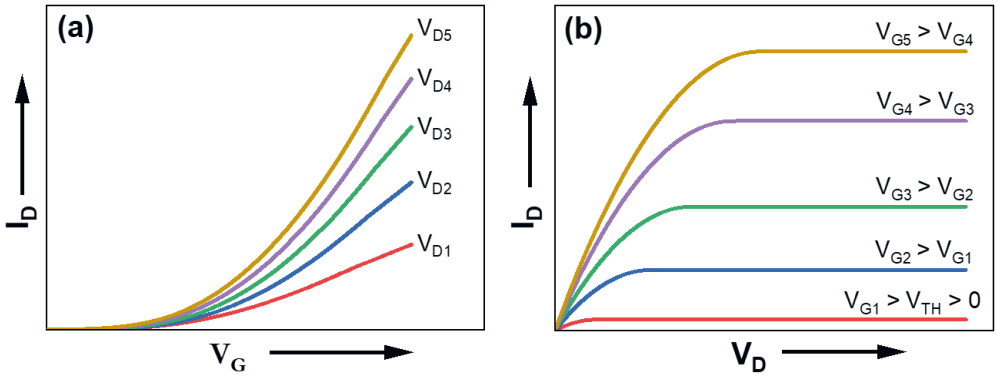

Figure 3. The general behavior of (a) transfer and (b) output characteristics of the TFT.

3.2.2 Threshold Voltage (V_{TH})

In general, the threshold voltage (V_{TH}) is basically the point at which current begins to flow through the device, specifically, in the accumulation regime for TFTs [81, 82]. However, as there is no inversion charge occurs in TFTs since they are generally accumulation devices, thus in practice threshold voltage needs to be redefined. A linear extrapolation of the square root of drain current (I_D) vs. gate voltage (V_G) plot at a given drain voltage (V_D) is often used to obtain the threshold voltage. On the square root I_D vs. gate voltage (V_G) plot, a straight line is drawn from the point of maximum transconductance till zero. The intersection of this extrapolated line with the x-axis defines the threshold voltage. The threshold voltage may be calculated in the linear region, when V_D is fixed and I_D is not constant, as follows:

$$V_{TH,lin} = V_{TH,Extrapolated} - \frac{V_{DS}}{2} \qquad \text{..... (3)}$$

However, as with mobility in the linear domain, inadequate charge injection might put the credibility of the linear extrapolation into doubt. So, if the saturation current $I_{D,SAT}$ is constant and the fixed V_D is being used in the saturation region, then the values for V_{TH} are as follows:

$$V_{TH,sat} = V_{TH,Extrapolated} \quad \text{..... (4)}$$

TFTs can exhibit non-saturating characteristics, making linear extrapolation challenging. Additionally, the sluggish subthreshold turn-on within the TFTs ends up in substantial drain current before V_G approaches the projected threshold voltage. As a result, the actual value of the projected threshold voltage becomes more ambiguous. Therefore, A quasi-static capacitance-voltage (QSCV) measurement can be used as an alternative way to obtain V_{TH}. In this case, by shorted drain/source electrodes, the TFT transitions from the depletion to the accumulation region upon a gate voltage (V_G) sweep. In the C-V measurements, the inclusion of the oxide (channel) capacitance in conjunction with the gate-source overlap and gate-drain overlap capacitances (geometrical capacitances) can be observed. The gate voltage (V_G) at which the charge accumulation and its corresponding channel capacitance may be detected is designated as the threshold voltage (V_{TH}).

3.2.3 Carrier Mobility (μ)

Another important parameter is the carrier mobility (μ), which relates to the efficiency of charge carrier transport in a material, where the transport is restricted to a small area at the gate dielectric to semiconductor channel interface [83, 86]. It can also have a direct influence on the device's maximum drain current and operating frequency. The carrier mobility is defined by the following equation,

$$\mu_{(sat)} = \frac{\left(\frac{\partial(\sqrt{I_D})}{\partial V_G}\right)^2}{\frac{1}{2} C_{ox} \frac{W}{L}} \quad \text{..... (5)}$$

where I_D is the drain current, V_G is the gate voltage, C_{ox} the specific capacitance of the gate dielectric per unit area, and W/L is the ratio of width to length (Figure 2) of the TFT channel.

3.2.4 ON/OFF Ratio (I_{ON}/I_{OFF})

The ratio of the maximum on-state current (I_{ON}) to the minimum off-state (I_{OFF}) current is termed as ON/OFF ratio or current ratio. The off-state current (minimum) is usually determined by the measuring equipment's noise level or the gate leakage current (I_G), whereas the on-state current (maximum) is determined by the active channel (semiconductor material) and the strength of capacitive injection due to the field effect. The current ratio is a key important figure of merit because it shows how effectively the gate controls the channel and the leakage currents [87-89]. It is normally extracted from the transfer characteristics (I_D vs. V_G), which demonstrates the ability of the device to differentiate between on and off states.

3.2.5 Metal Oxide Semiconductor (MOS) capacitance

The metal-oxide-semiconductor (MOS) capacitor is the core of the TFT. It plays a vital role in dictating the charge carrier density in the channel and the drain current in an active semiconductor channel between drain and source [87-89]. It is basically a two-terminal one-dimensional structure made up of three layers, which includes a metal gate contact, an oxide dielectric, and the semiconductor in question. Under bias (positive or negative), the MOS capacitor may be found in either of three states: accumulation, depletion, and inversion [90-95].

3.2.6 Breakdown voltage (V_{BD})

In order to fabricate durable and stable TFTs, understanding the maximum drain voltage (V_D) allowed before dielectric breakdown is crucial [96]. This can be done by measuring the output characteristic of the TFT, with every measurement increasing in full drain voltage (V_D), until the TFT breaks permanently [97]. The value of the breakdown voltage (V_{BD}) is determined by the measurement done before breakdown. Furthermore, the persistent quest for high-performance devices has been driven by aggressive device scaling. With the device scaling, the thickness of the gate oxide must be reduced. In case of the thin dielectrics, the dielectric breakdown voltage (V_G) due to the gate bias plays a significant role in the device operation, which is basically an applied gate voltage which causes a significant increment in the leakage current resulting in dielectric breakdown.

3.2.7 Transconductance (g_m)

Transconductance (g_m) is the change in the drain current as a function of a small change in the gate voltage under the constant drain voltage, essentially the DC gain. The electrical property that connects the current flowing across a device's output to the voltage through its input is known as transconductance (g_m) [98-100]. Transconductance is a measure of a TFT's performance, i.e., under steady state; the higher the transconductance, the larger the gain device can deliver [101]. It is the derivative of drain current (I_D) with respect to gate voltage (V_G) and it is represented by the equation (6)

$$g_m = \frac{\partial I_D}{\partial V_G} \quad \text{..... (6)}$$

3.2.8 Subthreshold swing (S)

The subthreshold swing (S) is a measure of how quickly a transistor changes its state, i.e., off to on and vice versa [102]. It can be determined using the reciprocal steepest slope (subthreshold slope) in the log of drain current (I_D) to gate voltage (V_G) curve calculated below threshold. A steeper subthreshold slope also implies reduced biasing voltages needed to switch a TFT, thus lowering power requirements. Subthreshold swing is expressed in millivolts per decade, which signifies the voltage required to raise the drain current by an order of magnitude [103]. The subthreshold swing (S) is given as,

$$SS = \frac{dV_G}{d\log(I_D)} \quad \text{..... (7)}$$

3.2.9 Contact Resistance (R_c)

The contacts are an important part of any electronic device where the semiconductor transitions to the connecting wires, at which this interface can lead to parasitic resistance losses that should be minimized. It is important to quantify the contact resistance in order to aid in better understanding how to minimize its deleterious

effects. [103, 104]. There are various ways and methods to measure the contact resistance. Amongst all, transfer length measurement (TLM) is the simplest and commonly used techniques for larger commonplace resistance values [105-107]. As shown in Figure 4, a standard TLM test pattern consists of an array of rectangular metal contacts separated by different lengths. The TLM plot can be constructed by comparing resistance between two sets of contacts, by which the contact resistance can be calculated.

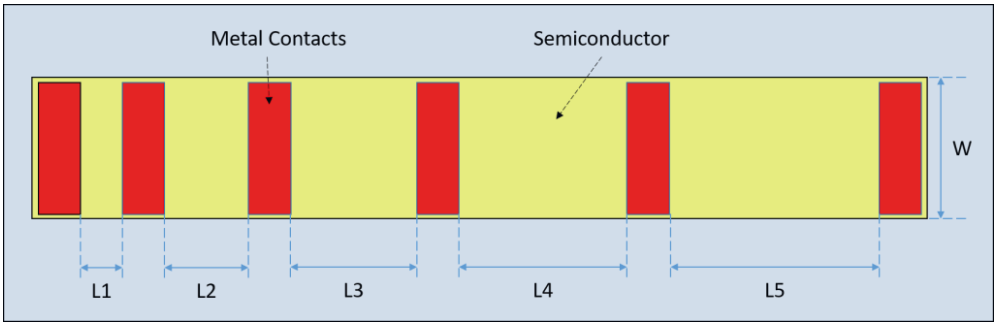

Figure 4. The standard TLM test pattern consists of an array of rectangular metal contacts separated by different lengths.

3.2.10 Trap State Densities (D_{it})

In amorphous semiconductors, the localized states caused due to structural defects, induces discrete states in the semiconductor's bandgap, which act as charge carrier traps that slows and reduces TFT response. The electrical performance of TFTs fabricated based on disordered semiconductors are hugely impacted by the density and energetic distribution of these localized states [108, 109]. Therefore, in a semiconductor device, under a low applied gate voltage and hence gate-induced carrier density, the bulk of the charges are trapped deep within the energy gap [110-112]. However, trap states near the transport stage are gradually filled as the gate voltage rises. As a result, the density of trap states (D_{it}) influences the TFT's subthreshold slope, i.e., the slope of the transfer characteristics in the exponential area below the threshold voltage. It is observed that, in addition to subthreshold slope, interface trap density (D_{it}) can also influence carrier mobility and bias stress effect as well as the semiconductor to drain-source contact interface [113].

4 MATERIALS AND FABRICATION TOOLS

Metal oxide semiconductors and their ink formation are discussed in this chapter. The next section discusses the types of substrates (rigid and flexible) utilized for the device fabrication. The chapter also provides an aspect of the design and geometry of the shadow mask used for the thin film transistor and inverter circuit. The deposition techniques for the metal contacts/electrodes (gate, drain-source), as well as gate dielectric and metal oxide semiconductor deposition are also presented in detail.

4.1 Metal Oxide Semiconductors

Any future flexible electronic devices must be adaptable and processable at low temperatures. In this regard, metal oxide semiconductors have attracted a lot of interest for thin film transistors (TFT), due to their exceptional electrical, chemical and mechanical properties [114, 115], along with wide band gap, wide optical transparency, high mobility and low temperature solution processable deposition [116]. The metal-oxide semiconductors, indium oxide (In_2O_3), Gallium Oxide (Ga_2O_3), and Indium Gallium Zinc Oxide (IGZO) with bandgap 3.6 eV, 4.8 eV and 3.5 eV [116-119], respectively, are exclusively studied in this dissertation for flexible thin film transistors and circuit. Like solids, electronic characteristics of metal oxides can be best explained by their band structures; however, the interaction of the metal and oxygen orbits can result in much more complex electronic phenomena as well as a considerable disparity in carrier transport. The high degree of ionicity within chemical bonding of metal oxide semiconductors provides an electronic structure that differs from covalent semiconductors. In metal oxide semiconductors, the formation of Conduction band minimum (CBM) and valence band maximum (VBM) is facilitated by metal (M) ns and oxygen (O) 2p orbitals, respectively [120], resulting in a widely dispersed CBM and confined VBM. This results in reduced effective masses for electrons, enables greater electron transport than hole, hence, most metal oxide semiconductors display n-type behavior. While most metal oxides' electronic band structures technically facilitate charge transfer, the wide band gaps

hinder thermal carrier formation, resulting in low intrinsic carrier densities. Hence, the novel approaches are required to understand their conductivity mechanism. In general, non-stoichiometry of metal oxides are commonly attributed to electrical conduction. For example, n-type metal oxide semiconductor conductivity may be altered by deposition in oxygen-deficient or metal-rich environment. The oxygen vacancies as well as metal interstitial constitute viable electron donors [121].

4.1.1 Ink Formation

The solution processable inks of the respective metal oxide semiconductors were prepared by dissolving the corresponding precursors in the solvents as follows –

A. Indium Oxide (In_2O_3) Ink – To form the In_2O_3 ink, indium (III) nitrate hydrate $In(NO_3)_3 \cdot xH_2O$ was dissolved in 2-methoxyethanol anhydrous 99.8% in 0.2 M concentration [Publication I-III]. The resulting ink was stirred for 12 hours at 75 °C.

B. Gallium Oxide (Ga_2O_3) Ink – Ga_2O_3 ink was prepared by dissolving Gallium (III) nitrate hydrate $Ga(NO_3)_3 \cdot xH_2O$ in deionized water (DI) with 0.1 M concentration [Publication IV]. The resulting ink was stirred for 12 hours at 75 °C.

C. Indium gallium zinc oxide (IGZO) ink – IGZO ink was formed by dissolving, indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$), gallium nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$), and zinc nitrate hydrate ($Zn(NO_3)_3 \cdot xH_2O$) in a proportion of 0.085 : 0.0125 : 0.0275 M respectively [Publication V]. The resulting ink was stirred for 12 hours at 75 °C.

4.2 Substrates – Glass and Kapton Polyimide (PI)

In the TFT fabrication process, thin films are deposited onto insulating substrates [128]. The TFT can be fabricated on a rigid or flexible substrate, each of which has a set of advantages and disadvantages. The rigid substrates include glass and silicon wafers, having an advantage of being easy to fabricate, handle, clean and higher temperature processability [129]. On the other hand, the flexible substrates such as Kapton polyimide (PI), polyethylene terephthalate (PET), polyethylene naphthalate

(PEN), Polyurethane, fabric or paper, are gaining popularity for the wearables, lightweight, flexible and printed electronics [130]. Furthermore, despite the good mechanical stability, most of the flexible substrates have a limited thermal range, e.g., in case of polyurethane it is limited to 120°C, making them incompatible with high-temperature processing [131, 132]. Therefore, whether they are rigid or flexible, the substrates must be mechanically, chemically, and thermally stable during the fabrication, measurements and application [133].

Two type of substrates are used in this dissertation for the fabrication of TFTs and circuits: glass and Kapton polyimide (PI). Glass substrates are 25 mm by 25 mm square size with 1 mm thickness and Kapton polyimide are cut from the roll into 25 mm by 25 mm square size having a thickness of 200 μm. In addition, multiple test samples were fabricated on glass substrates to aid in the optimization of the device fabrication process.

4.3 Metal Shadow Masks

The shadow mask is a collection of a sophisticated designs created by laser cutting or chemical etching on a thin metal sheet, usually stainless steel, and used to selectively deposit materials on substrates using a line-of-sight point-source process, like electron beam or thermal evaporation. They are commonly used to deposit materials onto the desired region of the substrate during vacuum evaporation and sometimes less directional sputtering processes. A number of metal shadow masks were used during the thin film transistors and circuit fabrication and optimization process to delineate gate metal pads and source/drain metal pads. All the metal shadow masks were conceptualized and designed in-house and fabricated from an outside vendor. The minimum dimensions (drain-source gap) were limited to 60 μm only due to the vendor's manufacturing fidelity.

4.3.1 Gate and Drain-Source

Two shadow masks, namely gate mask and drain-source mask as shown in Figure 5 (a) and (b), respectively, were used during the thin film transistor fabrication process to form a gate and drain-source electrodes. Figure 5 (c) represents the top view showing overlapping of the gate and drain-source along with dimensions. To reduce

or eliminate mismatch alignment between the layers, the size of this mask is kept the same as the substrate size.

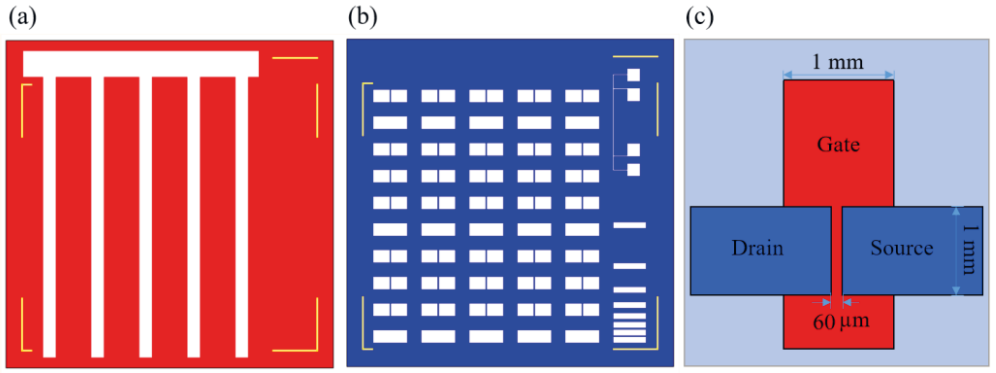

Figure 5. TFT Masks (a) gate (b) Drain-source and (c) Top view of the drain-source overlapping with gate.

4.3.2 Inverter Circuit

In a similar fashion to the TFT, for the fabrication of the inverter circuit two different shadow masks are used. First is the inverter gate mask and second is the inverter drain-source mask, as shown in Figure 6 (a) and (b), respectively. Figure 6 (c) represents the top view showing dimensions.

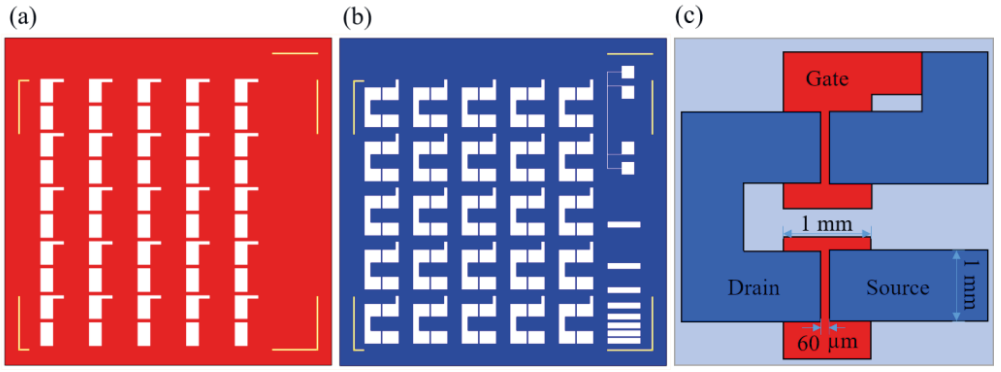

Figure 6. Inverter circuit masks (a) gate, (b) Drain-source mask and (c) Top view.

4.4 Deposition Techniques

4.4.1 Metal Electrodes - E-Beam Evaporator

To form (deposit) various metal contacts (Aluminum, Gold, Titanium) and inter layers (gate, drain-source, TLM and inverter) via metal shadow mask, an e-beam evaporator (which also includes a thermal/resistive source) as shown in Figure 7, provided by MBraun as an integrated part of a glovebox system was used. The use of metal shadow mask empowers the direct deposition and patterning of metal, eliminating the need of lithography techniques that expose samples to chemical developing and etching. The e-beam metal evaporation was always performed under a high vacuum below 2×10^{-6} Torr, which reduces oxidation of the evaporated metal.

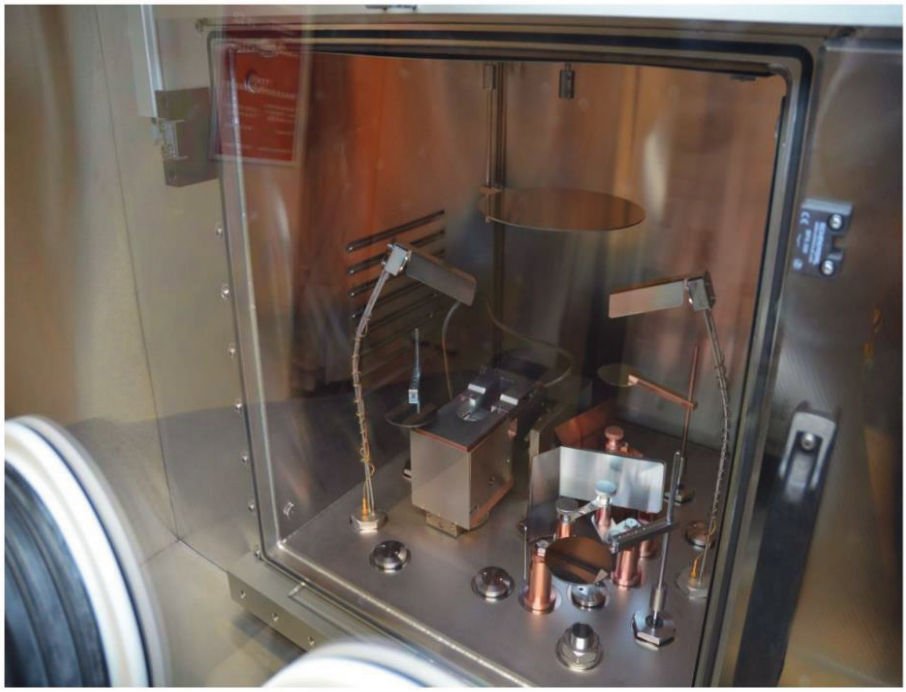

Figure 7. Photograph of the MBraun e-beam evaporator.

4.4.2 Metal Oxide Semiconductor - Spin Coating

During the device fabrication process to deposit the solution processed metal oxide, the most versatile printing process, namely the spin coating technique was utilized. Although it wastes some ink, spin coating is a facile way for rapid prototyping. Technology transfer to other printing modalities can be leveraged once device optimization is well underway. Regardless of the substrates used, spin coating has many advantages, including ease of use, uniformity, reproducibility, and compatibility [134, 135]. The general mechanism of spin coating is the equilibrium condition between the centrifugal force generated by the rotating base and the viscous force produced by the viscosity of the solution is the theory of this operation. As soon as the desired solution is poured on the substrate, the spinning base containing the substrate is accelerated at higher angular speed, permitting excess solution to be removed from the surface by centrifugal force. The film is then dried and annealed at a specific temperature. The thickness of the resulting films depends on the speed and acceleration profile of the spin coating process as well as the viscosity and the molar concentration of the solution [136, 137]. Figure 8 shows the general mechanism of the spin coating process.

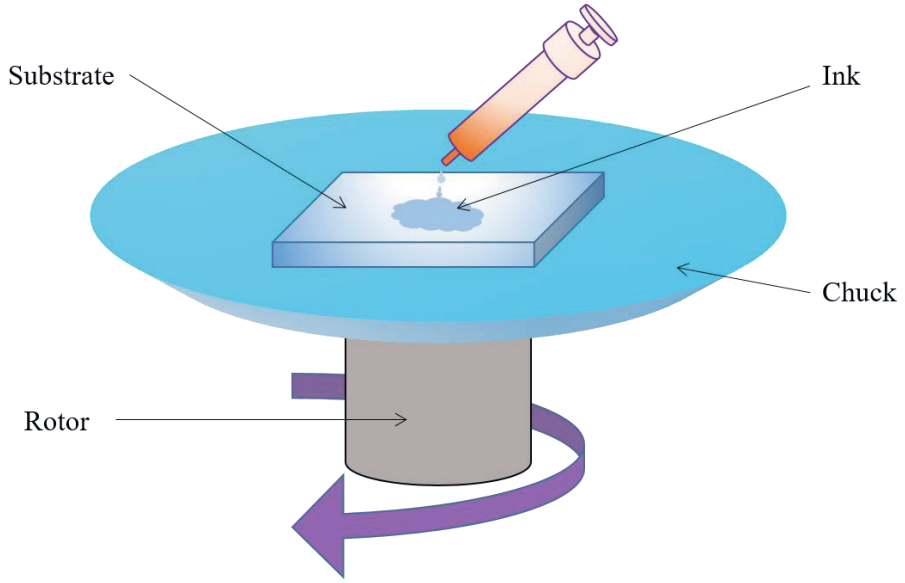

Figure 8. The schematic representation of the spin coating mechanism.

4.4.3 High-κ Gate Dielectric - Anodization

For the high-κ gate dielectric, aluminium oxide (Al_2O_3) was used for the thin film transistor and circuit fabrication process in the dissertation. The high-κ gate dielectric was deposited using the anodization pathway empowering for low voltage device operation, i.e., < 3V, and the procedure was carried out in accordance with previous studies [138, 139]. The room temperature anodization allows high-κ gate dielectric deposition on a flexible substrate, eliminating the need of high temperature [140], high vacuum processes [141-144], with additional benefits such as low cost, nanoscale deposition, denser and high-quality films [138-139]. The general representation of the anodization process is shown in Figure 9.

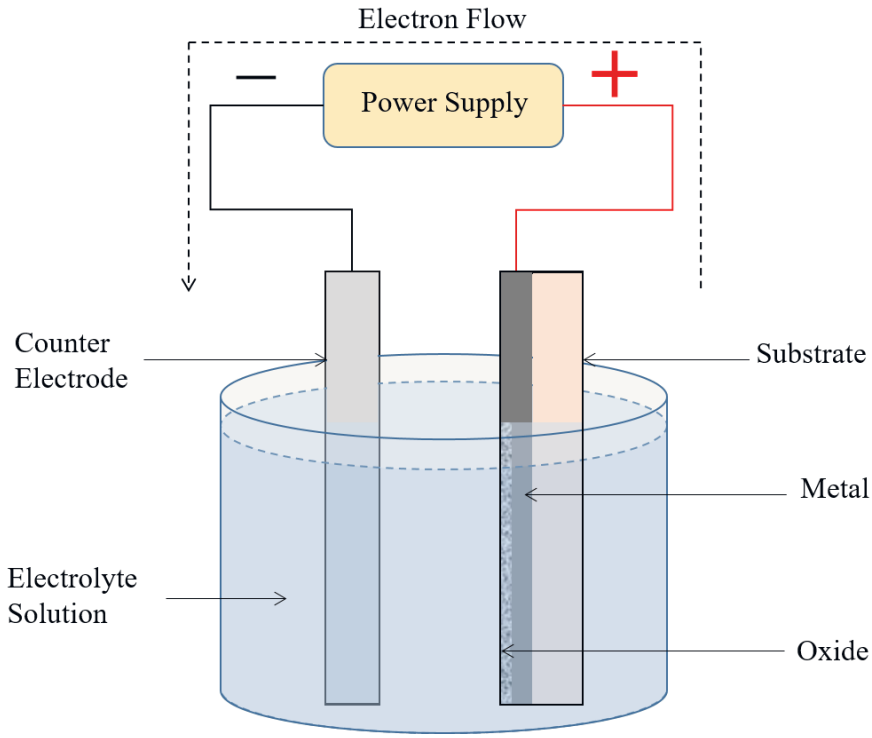

Figure 9. The schematic representation of the anodization process.

The 0.01M electrolyte solution was prepared by dissolving the citric acid monohydrate ($C_6H_8O_7 \cdot H_2O$) in ultrapure deionized (DI) water. To achieve the desired oxide thickness, potentiostatic anodization was used. The working electrode (anode) was formed by immersing the evaporated gate (aluminum) electrode into the

electrolyte solution, with a platinum foil serving as the counter electrode (cathode). A Keithley source meter was utilized to provide the constant voltage (DC) source. For several minutes (30 min.), the anodization potential (5.0 V) was applied until the current dropped below 1 μA. An approximately 9 nm aluminum oxide was produced with an oxide formation factor of 1.8 nm V^{-1}. This resulted in a total oxide thickness of ~12 nm, included ~2 nm native oxide due to air exposure to deposited aluminum. The overall oxide thickness was confirmed by electron microscopy (TEM). Thereafter, the samples were rinsed with distilled water and dried under nitrogen flow.

5 FABRICATION PROCESS AND CHARACTERIZATION

The metal oxide (MO) thin film transistors were fabricated and characterized using the materials, process and equipment described in Chapter 4. The thin films and materials deposited were also investigated using transmission electron microscopy (TEM) and atomic force microscopy (AFM).

5.1 Device structure and Architecture

TFTs are comprised of five parts: substrate, gate, drain-source, semiconductor and gate dielectric.

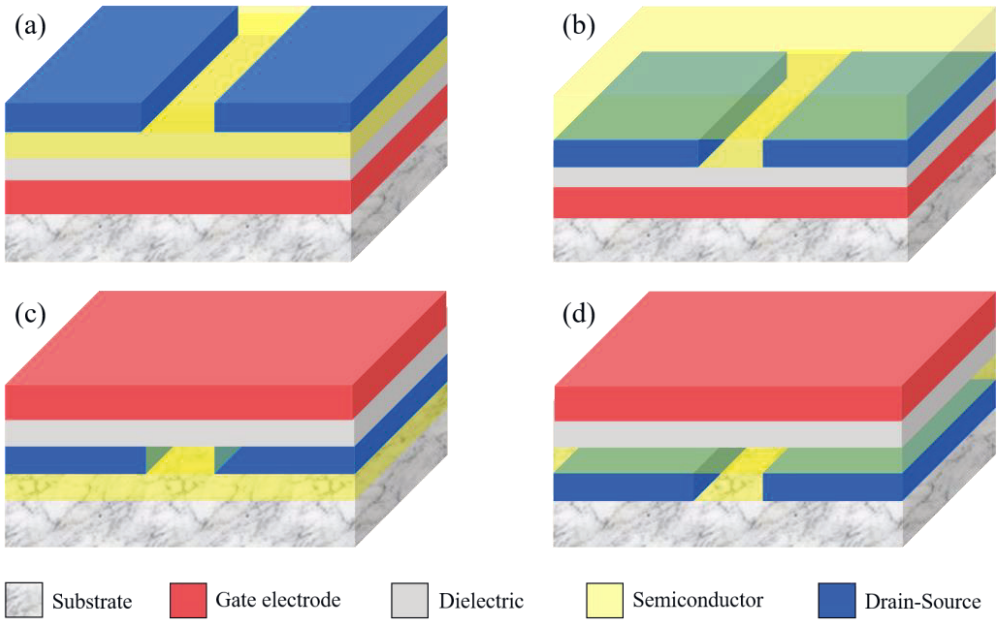

Figure 10. The Schematic representations of TFT architectures. (a) bottom gate – top contact (BGTC), (b) bottom gate – bottom contact (BGBC), (c) top gate – top Contact (TGTC) and (d) top gate – bottom contact (TGBC).

Depending on the gate and drain-source electrode configurations in the semiconductor, there are four types of TFT architectures, bottom gate – top contact (BGTC), bottom gate – bottom contact (BGBC), top gate – top Contact (TGTC) and top gate – bottom contact (TGBC) [28]. The general schematic representations of these types are shown on Figure 10.

5.2 Thin Film Transistors (TFTs) Fabrication

The three different metal oxide (MO) semiconductors, i.e., indium oxide (In_2O_3), gallium oxide (Ga_2O_3), and indium gallium zinc oxide (IGZO) were used to fabricate the thin film transistors on the two different substrates: glass and flexible Kapton. The initial TFT prototype was developed on a glass substrate with a channel length (L) 60 μm and width (W) 700 μm, with multiple iterations of the device fabrication. Subsequently, by following the same device prototype flexible TFTs were also fabricated on a flexible Kapton (polyimide) foil. Owing to the added advantage in ease of fabrication process, the bottom gate, top contact (BGTC) topology, as shown in Figure 11, was used here for the TFT fabrication. More details can be found in the attached publications I-V.

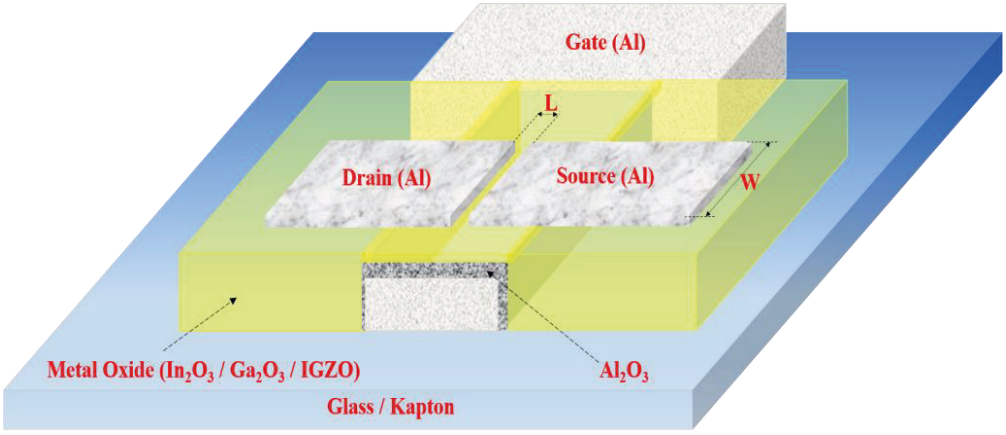

Figure 11. Schematic representation of metal oxide TFT with Al_2O_3 gate dielectric.

The thin film transistors were separately fabricated on the 25 × 25 mm glass and flexible Kapton substates. The glass and Kapton substrates were ultrasonically cleaned with acetone, IPA (isopropanol), and DI (deionized water) for 30 minutes each prior to device fabrication.

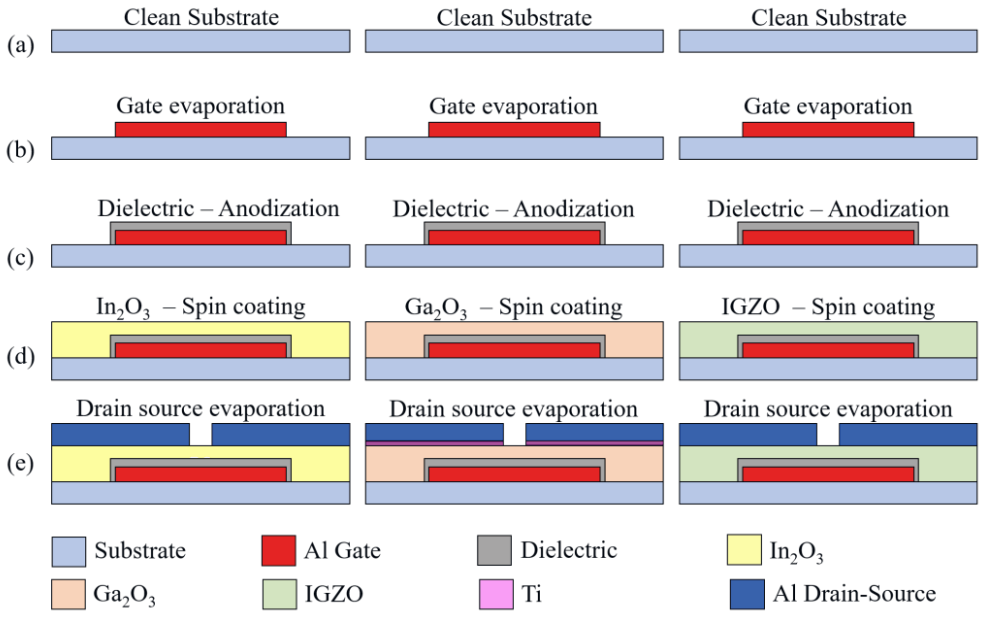

Figure 12. Solution processed metal oxide TFT fabrication process flow with Al_2O_3 gate dielectric.

Initially, a gate electrode was formed by depositing 100 nm of aluminum (Al) metal onto the substrate using an e-beam evaporator and a patterned metal shadow mask. The substrates were then anodized to transform the evaporated aluminum gate electrode's upper surface (12 nm) into aluminum oxide (Al_2O_3) forming a high-κ gate dielectric. Subsequently, the substrates were carefully cleaned many times using DI water and dried. Afterwards, using the spin coating method, the precursor solution of the respective metal oxide (In_2O_3, Ga_2O_3 and IGZO) semiconductors was deposited followed by annealing at 90 °C for 15 min and 300 °C for 30 min in air. The film was then dried by annealing in air for 15 minutes at 90 °C and 30 minutes at 300 °C. Finally, a drain-source electrode was generated by depositing 100 nm of aluminum (Al) metal on glass and Kapton substrates using an e-beam evaporator and a patterned metal shadow mask. In the case of gallium oxide, a drain-source electrode was formed by depositing 10 nm of titanium (Ti) followed by 100 nm aluminum (Al). The length (L) and width (W) of the channel were 70 μm and 700 μm, respectively. The e-beam evaporations of all the metal electrodes were performed under a high vacuum 10^{-6} Torr. Furthermore, MOS test structures made of $Al/Al_2O_3/MO/Al$ were constructed on the same substrates as the TFTs under the same conditions. More details in the attached publications I-V. The TFT

fabrication process flow is shown in Figure 12, and top view of the fabrication process flow is shown in Figure 13.

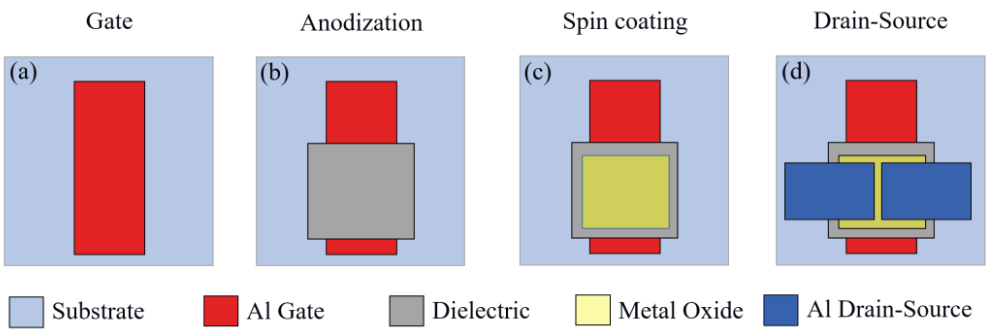

Figure 13. Top view of the fabrication process flow.

The summarized TFT fabrication process parameters are shown Table 1. More details in the attached publications I-V.

Table 1. Summarized TFT fabrication process parameters

Sr. no.	Metal Oxide Semiconductor	Deposition method	Gate Electrode		Gate Dielectric
			Gate	Drain-Source	
1.	Indium oxide (In_2O_3) (Publications I-III)	Spin coating	Aluminum (Al) 100 nm	Aluminum (Al) 100 nm	Anodized Al_2O_3 12 nm
2.	Gallium oxide (Ga_2O_3) (Publications IV)	Spin coating	Aluminum (Al) 100 nm	Titanium (Ti) 10 nm + Aluminum (Al) 100 nm	Anodized Al_2O_3 12 nm
3.	Indium gallium zinc oxide (IGZO) (Publications V)	Spin coating	Aluminum (Al) 100 nm	Aluminum (Al) 100 nm	Anodized Al_2O_3 12 nm

The photograph and optical micrograph of the finally completed metal oxide TFTs are represented in Figure 14.

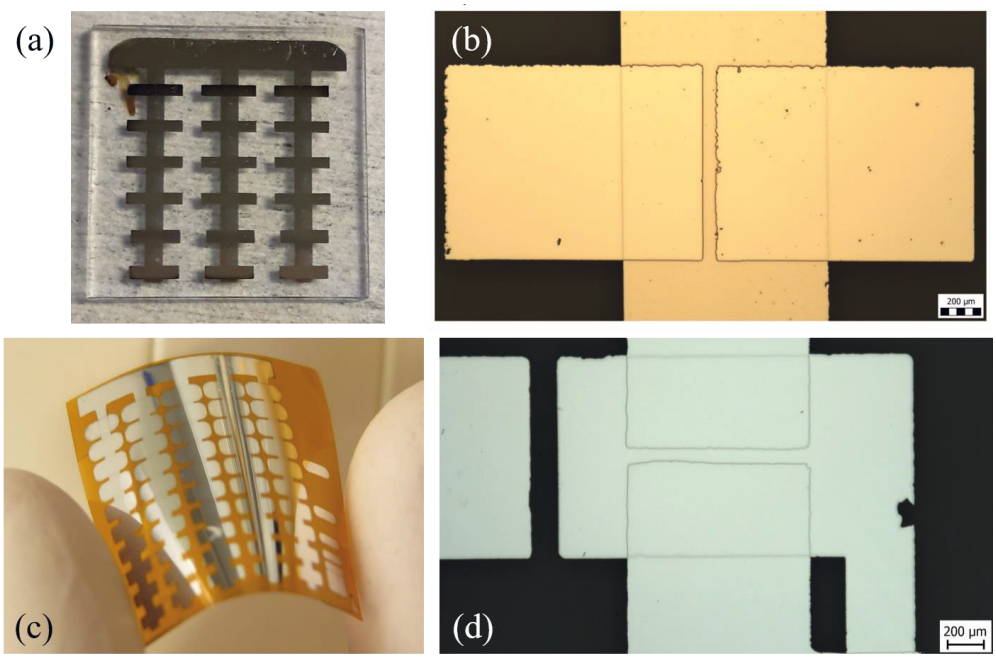

Figure 14. (a) A photograph and (b) optical micrograph of the TFTs fabricated on a glass substrate, (c) A photograph and (d) optical micrograph of the TFTs fabricated on a flexible Kapton. © [2019], IEEE.

5.3 Flexible Inverter Circuits Fabrication

A prototype flexible inverter circuit was fabricated by following the architectures and processes used for TFT fabrication. Figure 15 represents the schematic of the proposed two TFT based inverter circuit. More details are provided in the attached publication III-V. The inverter circuit fabrication process flow is shown in Figure 16. A 100 nm of aluminum gate electrode evaporated on a clean substrate Figure 16 (a). Then a small piece of adhesive Kapton tape was added to part of the gate electrode area, shown as violet colored in Figure 16 (b), to protect the part of the gate electrode area from the anodization and spin coating, which was at the end used for the overlapping between gate and drain of the TFT towards the formation of the inverter circuit. The inverter circuit fabrication then concluded by following the process flow shown in Figure 16. More details in the attached publications III-V.

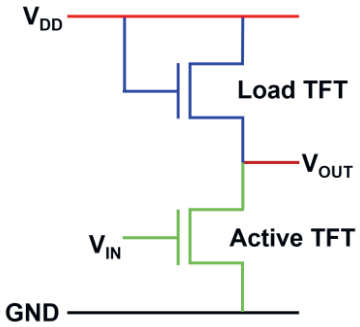

Figure 15. Proposed two TFT based inverter circuit processed metal oxide inverter circuit fabrication process flow with Al_2O_3 gate dielectric. (Publication III-V).

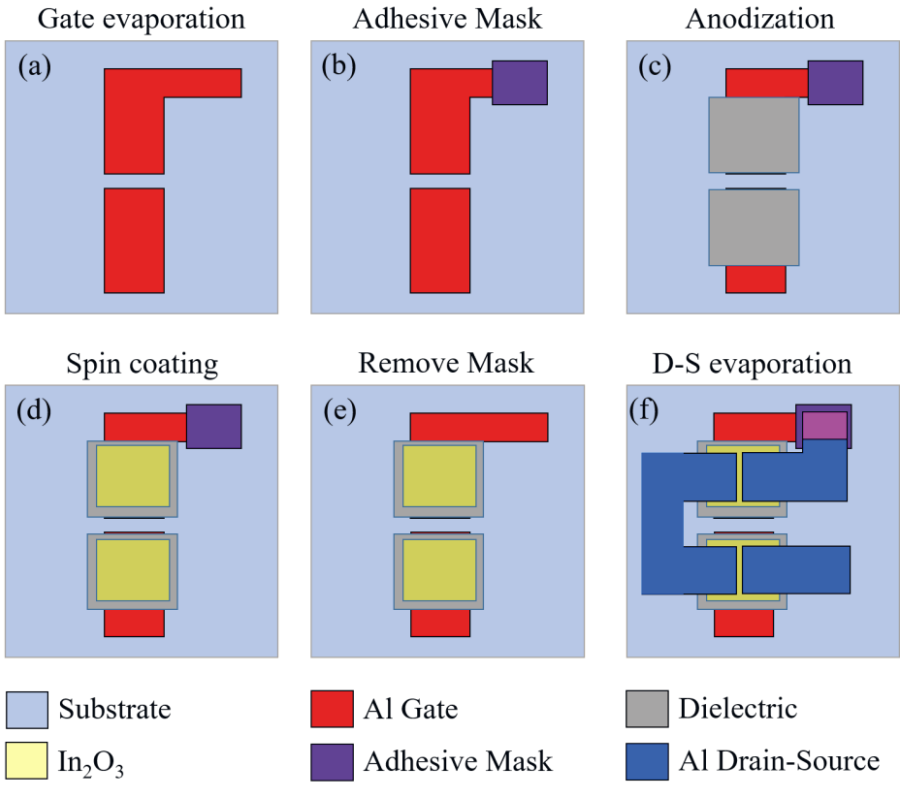

Figure 16. Solution processed metal oxide inverter circuit fabrication process flow with Al_2O_3 gate dielectric.

A photograph and optical micrograph of the fabricated flexible In_2O_3 inverter circuit on a Kapton substrate are represented in the Figure 17 (a) and (d), respectively.

Figure 17. Figure Heading Flexible inverter circuit (a) A photograph and (b) optical micrograph. Scale bar 500 µm. (From Publication III) © [2021], Materials Science in Semiconductor Processing.

5.4 Electrical performance characterization

The electrical characterization of the fabricated metal oxide TFTs was carried out using a Keysight B1500A semiconductor device parameter analyzer connected to a Cascade Microtech probe station with triaxially shielded probes.

5.4.1 Capacitance Voltage (CV)

The capacitance voltage (CV) analysis and the determination of leakage through the dielectric was performed using a two-terminal metal oxide semiconductor structure [Publication I]. The CV and the leakage current plot of the In_2O_3/Al_2O_3 are shown in Figure 18 (a) and (b), respectively. In the device operating range of 3 V, the anodized aluminum oxide displays low leakage current.

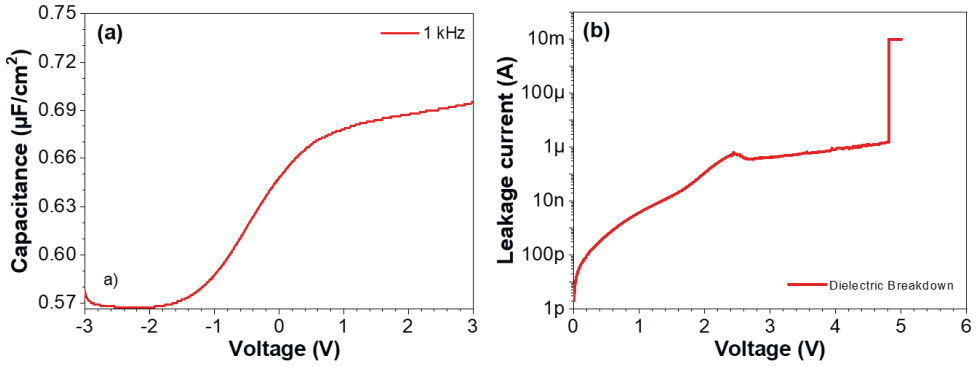

Figure 18. (a) The CV (capacitance voltage) characteristics measured at 1 kHz frequency and (b) Gate dielectric breakdown. (From Publication I) © [2019], IEEE.

5.4.2 Current Voltage (IV)

The performance of the metal oxide thin film transistors fabricated on glass and flexible Kapton substrates was evaluated by measuring the current voltage i.e., transfer (I_d vs. V_g) and output (I_d vs. V_d) characteristics.

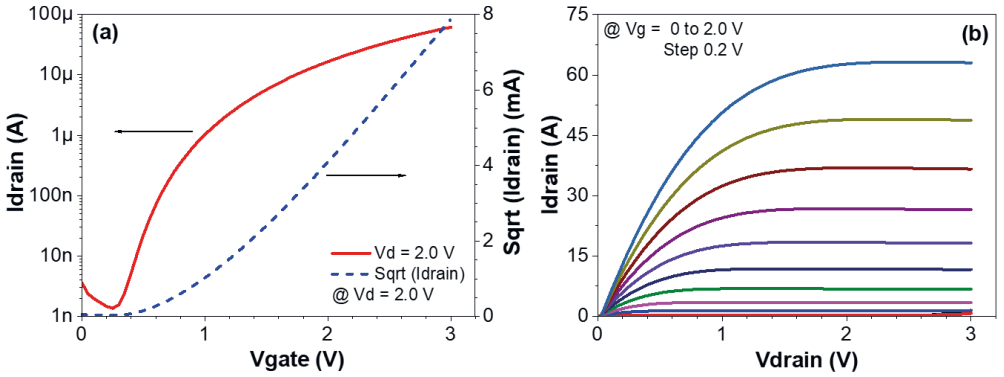

Figure 19. (a) Transfer and (b) Output characteristic of In_2O_3 TFT fabricated on glass substate. (From Publication I), © [2019], IEEE.

The transfer and output characteristics of the TFT with In_2O_3 channel semiconductor and room temperature anodized Al_2O_3 fabricated on glass substate are shown in Figure 19 (a) and (b) [Publication I]. Figure 20 (a) and (b) displays the transfer and output characteristics of the TFT with In_2O_3 channel semiconductor and room temperature anodized Al_2O_3 fabricated on flexible Kapton substrate [Publication III]. The TFTs comfortably operate well below 3 V. Furthermore, the

improved performance of flexible TFTs along with SPICE modeling are represented in the Figure 21 (a) and (b) [Publication III]. More details on electrical performance parameters are summarized in Table 2.

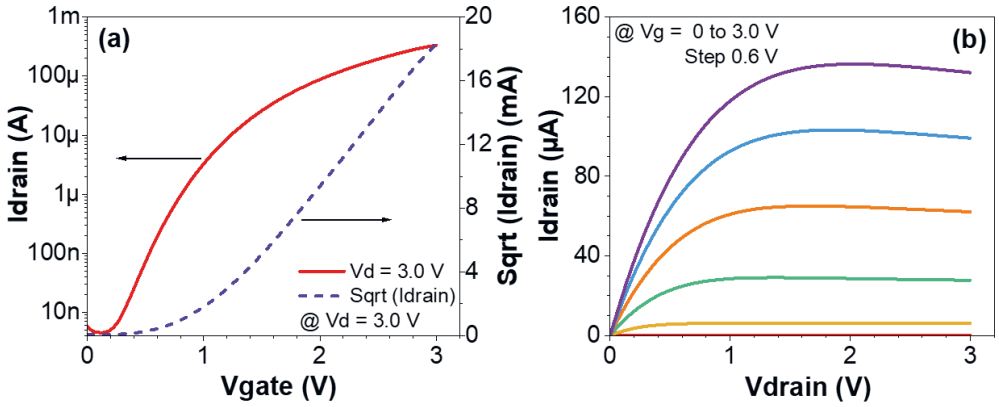

Figure 20. (a) Transfer and (b) Output characteristic of In_2O_3 TFT fabricated on flexible Kapton substrate. (From Publication III) © [2021], Materials Science in Semiconductor Processing.

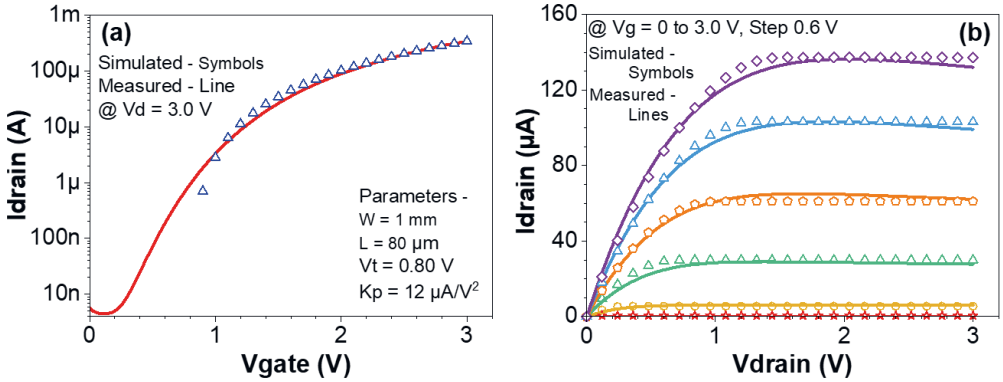

Figure 21. (a) Transfer and (b) Output characteristic of flexible In_2O_3 TFT along with modeling. (From Publication III) © [2021], Materials Science in Semiconductor Processing.

Similarly, the electrical performance of solution processed gallium oxide (Ga_2O_3) TFTs fabricated on a glass and flexible Kapton are presented in Figure 22 (a), (b) and Figure 23 (a), (b), respectively [Publication IV]. Additional details on electrical performance parameters are summarized in Table 2.

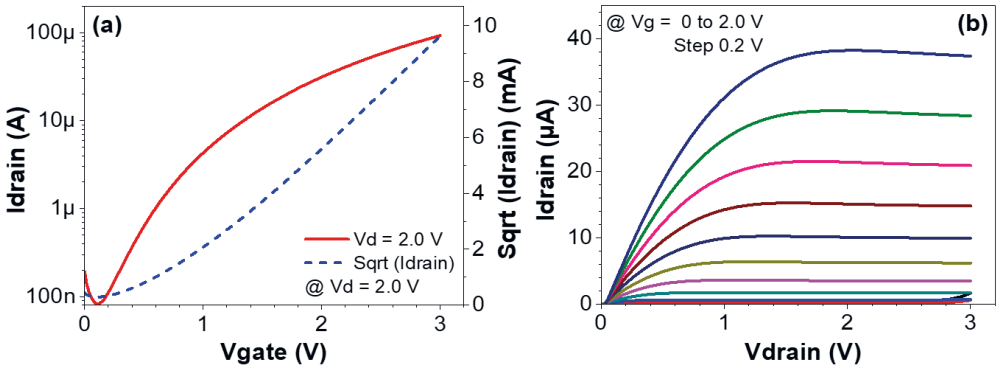

Figure 22. (a) Transfer and (b) Output characteristic of Ga_2O_3 TFT fabricated on glass substate.

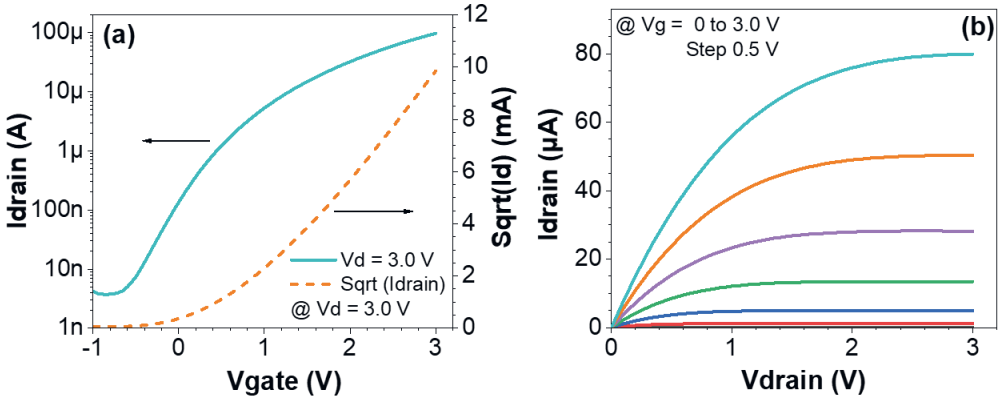

Figure 23. (a) Transfer and (b) Output characteristic of Ga_2O_3 TFT fabricated on flexible Kapton substrate. (From Publication IV) © [2021], IEEE.

Additionally, Figure 24 (a), (b) and Figure 25 (a), (b) shows the electrical performance of solution processed indium gallium zinc oxide (IGZO) TFTs fabricated on glass and Kapton, respectively [Publication V]. Table 2. and 3 summarizes additional information on bias conditions and electrical efficiency parameters, respectively.

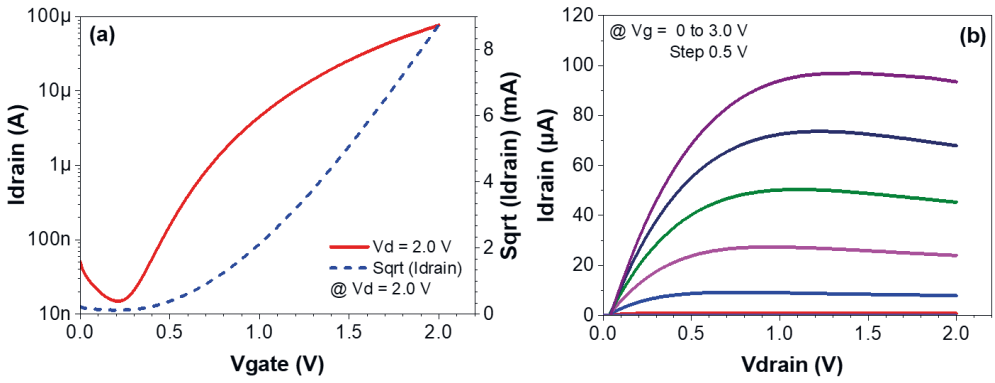

Figure 24. (a) Transfer and (b) Output characteristic of IGZO TFT fabricated on glass substate.

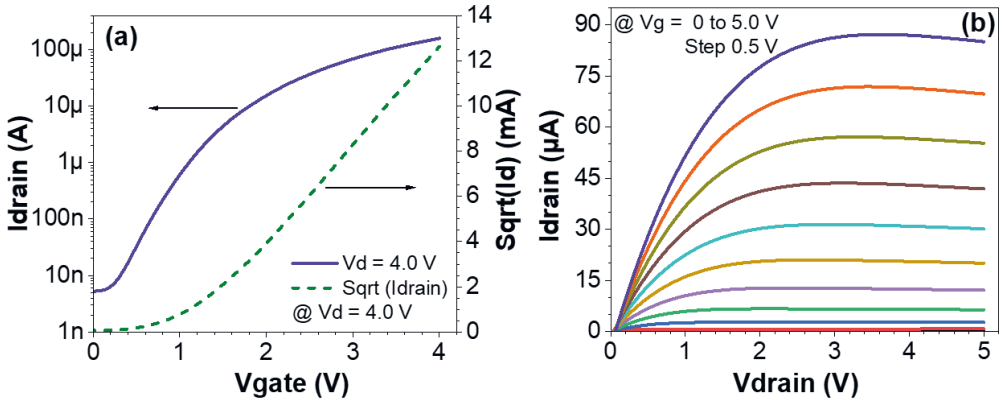

Figure 25. (a) Transfer and (b) Output characteristic of IGZO TFT fabricated on flexible Kapton substrate. (From Publication V) © [2019], IEEE.

Furthermore, The indium oxide (In_2O_3) TFTs' stability was evaluated under negative bias stress (NBS) at various gate bias stress intervals as shown in the Figure 26 (a) and (b). The transfer characteristics (I_d vs. V_g) of indium oxide TFTs clearly reveal that the TFTs function well under bias stress; with a very small change in threshold voltage (V_{th}) around 0.3 V, as illustrated in Figure 26 (b). Additionally, the dual-scan transfer characteristics of indium oxide TFTs at various drain biases were used to determine hysteresis as low as 0.12 V, as shown in Figure 26 (c). As a histogram of saturation mobility against device proportion and average, Figure 26 (d) displays a statistical examination of the electrical performance of the examined devices, signifying good device reliability and yield with 70% of devices having mobility in the range of 10 – 14 cm^2/Vs.

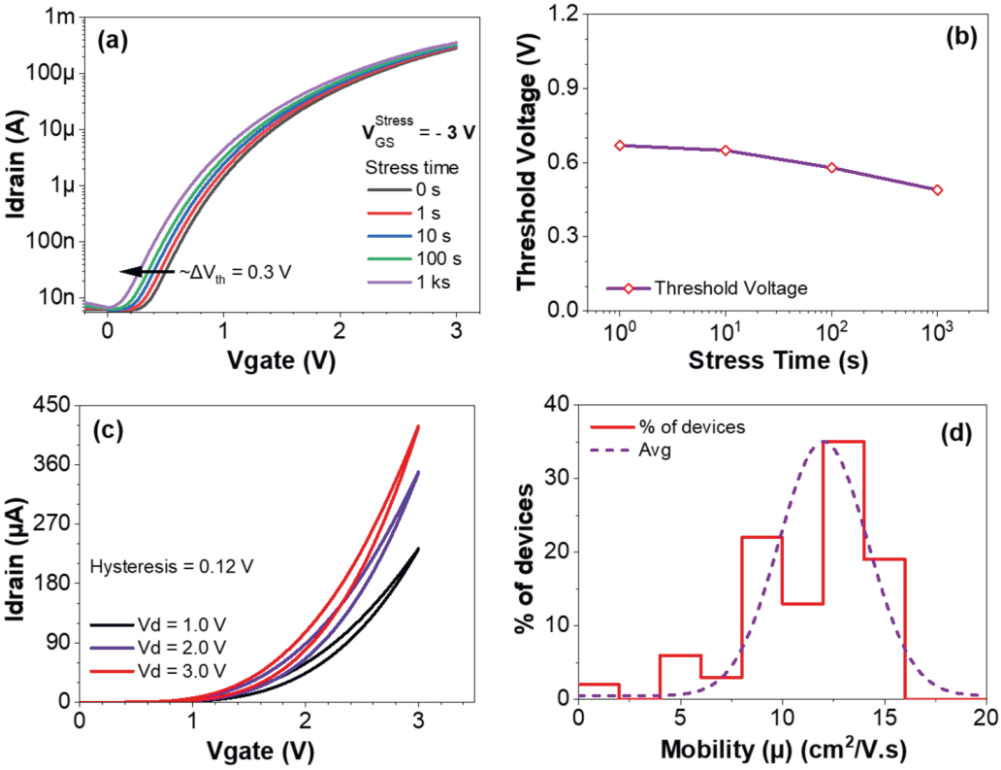

Figure 26. (a) Variation of transfer characteristics of In_2O_3 TFTs measured as a function of gate bias stress time, at negative gate bias stress (NBS) of -3 V, b) Bias stress-induced threshold voltage shift as a function of stress time. c) Transfer characteristics of In_2O_3 TFTs representing hysteresis, and d) Mobility histogram indicating device reliability and yield. (From Publication III) © [2021], Materials Science in Semiconductor Processing.

Table 2. TFT measurement bias conditions [Publications I-V] [122-126]

Sr. no.	Name	Gate V_g (V)		Drain-Source V_d (V)	
		Glass	Kapton	Glass	Kapton
1.	Indium oxide TFTs	0 to 3	0 to 3	2	3
2.	Gallium oxide TFTs	0 to 3	-1 to 3	2	3
3.	Indium gallium zinc oxide TFTs	0 to 2	0 to 4	2	4

Table 3. Summarized metal oxide TFT performance parameters [Publications I-V] [122-126]

Sr. no.	TFT Parameters	Indium oxide (In_2O_3)			Gallium oxide (Ga_2O_3)		Indium gallium zinc oxide (IGZO)	
		Glass	Kapton	Kapton	Glass	Kapton	Glass	Kapton
1.	Operating Voltage V	0 to 3	0 to 2	0 to 3	0 to 3	-1 to 3	0 to 2	0 to 5
2.	Threshold Voltage (V_{th}) V	0.6	0.42	0.82	0.43	0.61	0.75	1.05
3.	Mobility (μ) $cm^2V^{-1}s^{-1}$	3.5	2.85	14.5	2.5	2.74	2.82	4.77
4.	Transconductance (g_m) μS	53	38	140	70	64.8	73	90.8
5.	Subthreshold swing (S) V/dec	0.16	0.42	0.22	0.38	0.50	0.27	0.35
6.	On/Off ratio	10^5	10^3	10^5	10^4	10^4	10^4	10^4

5.4.3 Flexibility – Bending performance

Along with the electrical characterization of the TFT, the bendability of the flexible TFTs was also studied [Publication III-V]. The flexible TFTs were bent over a glass rods of different radius (3.5 cm to 5 mm) and electrical performance was measured as they were bent. The change in carrier mobility with respect to the bending is represented in Figure 27 (a) (b) and (c). The thin film transistors fabricated using metal oxide semiconductors show quite stable performance down to a bending radius of 5 mm.

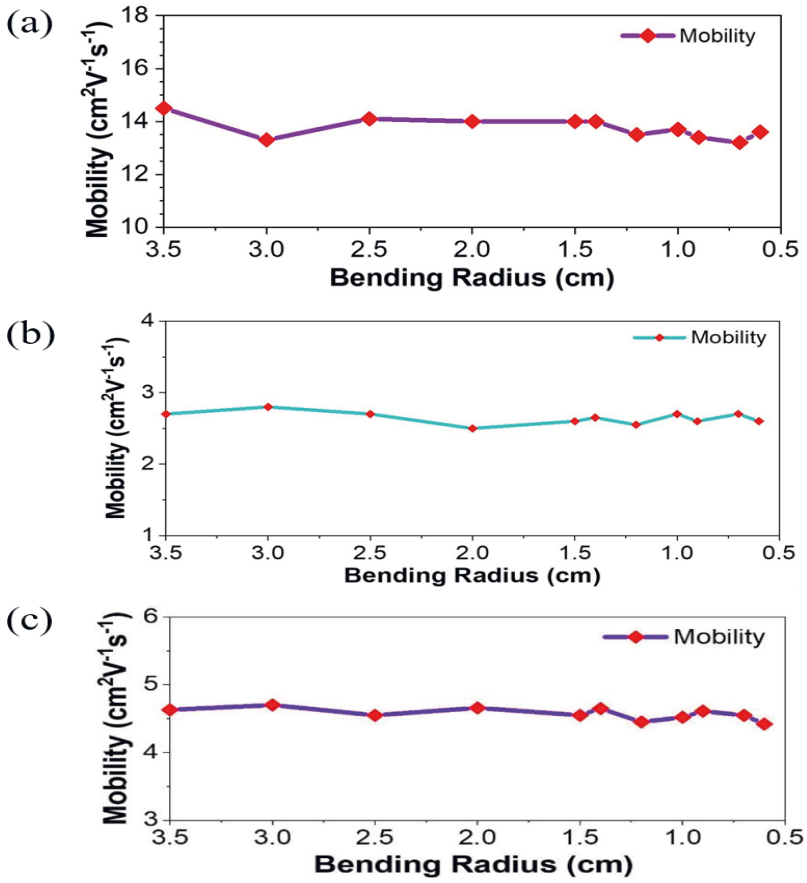

Figure 27. Bending performance of the flexible TFTS based on a) In_2O_3 (From Publication III) © [2021], Materials Science in Semiconductor Processing, b) Ga_2O_3 (From Publication IV) © [2021], IEEE and c) IGZO. (From Publication V) © [2021], IEEE.

5.4.4 Flexibility Inverter Circuit performance

The two TFT-based inverter circuit's electrical performance was also presented in the Figure 28 (a), (b) and (c), by measuring output voltage correspond to the input voltage over range of supply voltage (V_{DD}) [Publication III-V]. The measured voltage gains of the inverter circuits are represented in the table 4.

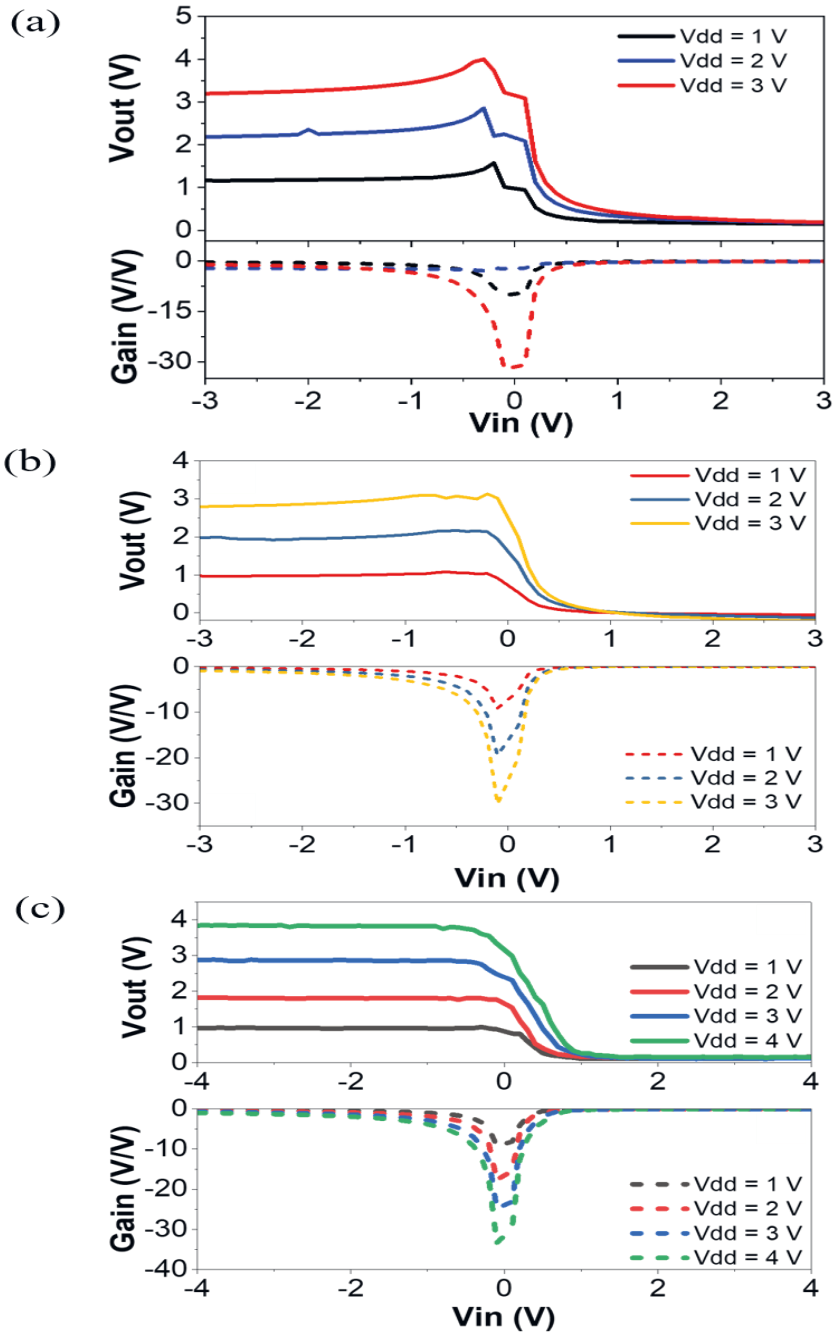

Figure 28. The output voltage and gain of the inverter circuit with respect to input voltage of flexible inverter circuit based on a) In_2O_3 (From Publication III) © [2021], Materials Science in Semiconductor Processing, b) Ga_2O_3 (From Publication IV) © [2021], IEEE and c) IGZO. (From Publication V), © [2021], IEEE.

Table 4. Summarized Inverter Circuit performance parameters [Publications III-V]					
Sr. no.	**Metal Oxide Semiconductor**	**Input voltage**	**Inverter Gain at V_{DD}**		
			1 V	**2 V**	**3 V**
1.	Indium oxide (In_2O_3) (Publications III)	– 3 V to + 3 V	10	22	32
2.	Gallium oxide (Ga_2O_3) (Publications IV)	– 3 V to + 3 V	9	19	30
3.	Indium gallium zinc oxide (IGZO) (Publications V)	– 4 V to + 4 V	9	17	24

5.4.5 Trap State Densities (D_{it})

The metal-oxide-semiconductor structure comprising of an indium oxide (In_2O_3) semiconductor and aluminum oxide (Al_2O_3) dielectric was used to understand the dielectric-semiconductor interface. The interface trap density (D_{it}) was investigated using the conductance method (eq. 8), sweeping from 1 kHz to 5 MHz [78, 145],

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \quad \text{……. (8)}$$

where G_p is the peak conductance per unit area, $\omega = 2\pi rf$ (f - frequency), and q is the electronic charge.

The (G_p/ω) was plotted as a function of frequency to quantify the interface trap density (D_{it}) [Publication I]. As shown in Figure 29 (a), G_p/ω increases with

frequency up to a limit, then, as expected with an interface trap model, it begins to fall at higher frequencies [146]. Furthermore, the frequency dependent (1 kHz to 1.3 MHz) values of MOS capacitance were found to be 0.6 - 0.8 μF/cm², Figure 29 (b).

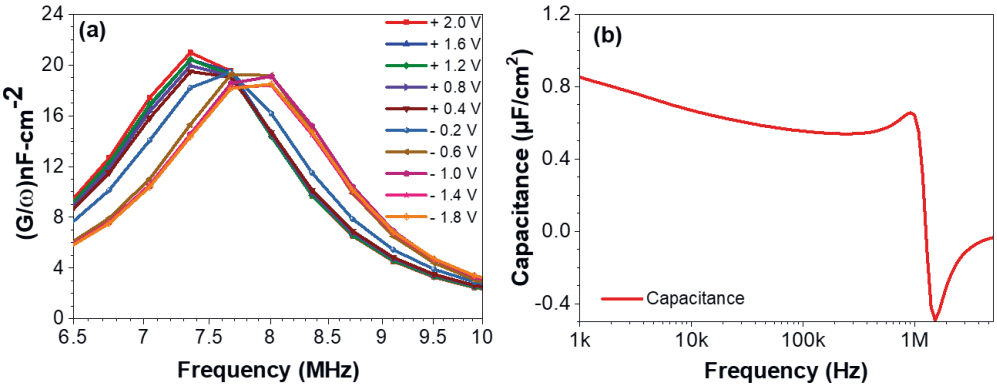

Figure 29. (a) The (G_p/ω) plot as a function of frequency (b) The frequency dependance of MOS capacitance. (From Publication I) © [2019], IEEE.

The value of the interface trap density extracted using the conductance method [147] was found to be $0.99 \times 10^{11} - 2.98 \times 10^{11}$ $eV^{-1} \cdot cm^{-2}$, [Publication I]. Figure 30 depicts the subsequent relationships among trap state densities with biasing voltage dependence, as well as the trap states' energy relative to the band gap [148-150] are displayed in Figure 30 (a) and (b).

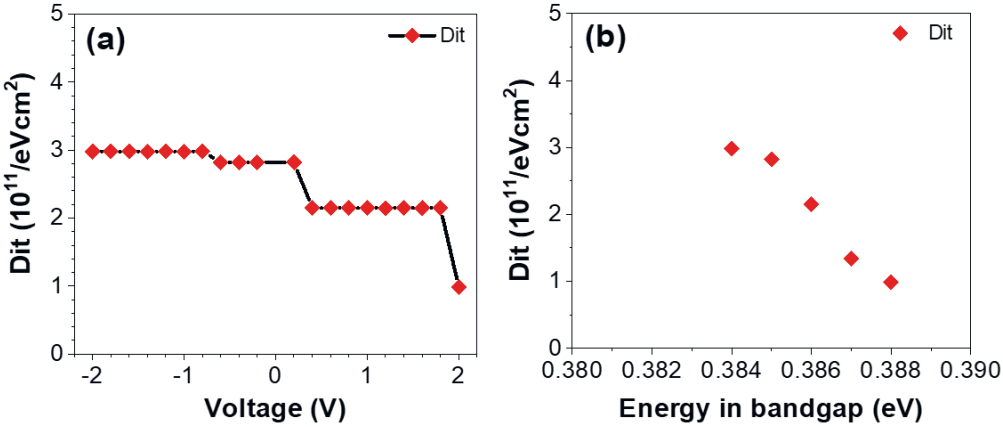

Figure 30. The trap state densities as function of (a) biasing voltage and (b) Energy in bandgap. (From Publication I) © [2019], IEEE.

5.5 Thin film and Material characterization

With the help of atomic force microscopy (AFM) and cross-sectional transmission electron microscopy (TEM) analysis, thin film and material characterization were also performed.

5.5.1 Atomic force microscopy (AFM)

The surface roughness of the anodized aluminum oxide (Al_2O_3) film was investigated using atomic force microscopy (AFM), over 5 × 5 μm² scanning area [Publication I]. The AFM analysis yielded with average roughness value 1.53 nm and as illustrated in Figure 31.

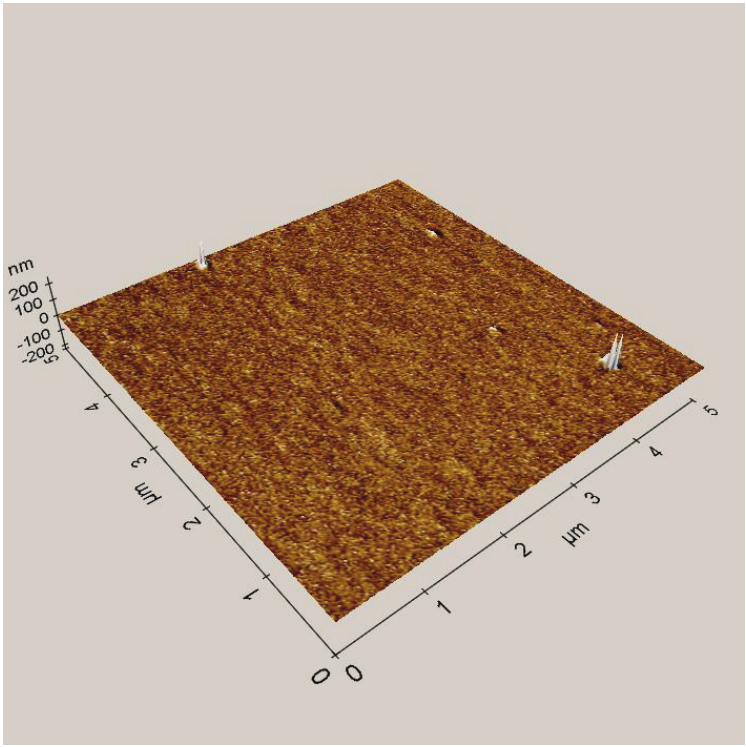

Figure 31. AFM image of the anodized aluminum oxide (Al_2O_3) showing average roughness value 1.53 nm. (From Publication I) © [2019], IEEE.

5.5.2 Transmission electron microscopy (TEM)

The cross-sectional transmission electron microscopy (TEM) study of the TFTs was also performed to determine the dielectric thickness with high accuracy [Publication-I]. The thickness of the dielectric oxide (Al_2O_3) layer was found to be 12 nm using cross sectional TEM, and it can be seen in Figure 32. Furthermore, using the parallel plate capacitance equation $C = \kappa\varepsilon_0 A/d$ [151], the dielectric constant, κ, was determined to be 9.3.

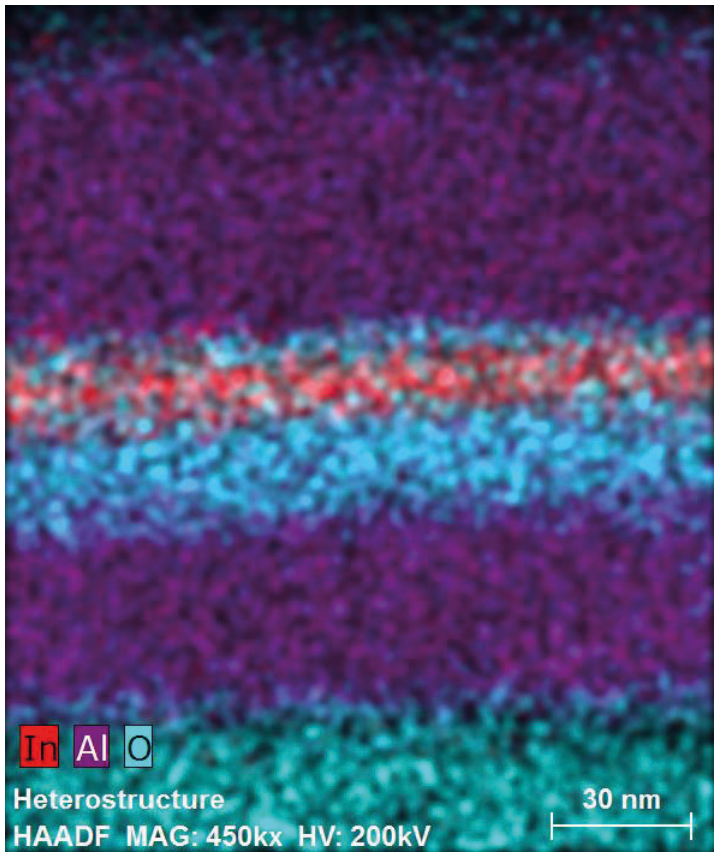

Figure 32. The cross-sectional image of the TFT, scale bar 30 nm. (From Publication I) © [2019], IEEE.

6 CONCLUSIONS

6.1 Major Finding

Metal oxide based thin film transistors have seen rapid progress in recent years, especially in terms of new materials and device architecture. Though high-temperature vacuum deposition techniques dominate the metal oxide TFTs, the device operating voltage and the need for high temperatures has hindered its use in new technologies like printed-flexible electronics, wearables and Internet of Things (IoT). As a result, metal oxide TFTs are now undergoing significant research to develop a low-temperature, solution-processed metal oxide deposition technique compatible for flexible substrates.

In this thesis, the successful fabrication and detailed characterization of low voltage (< 3 V) operating thin film transistors (TFTs) using the solution-processed metal oxide, such as indium oxide (In_2O_3), gallium oxide (Ga_2O_3) and Indium gallium zinc oxide (IGZO) on a glass and a flexible Kapton substrate was demonstrated. The low voltage device operation was achieved by the successful integration of the solution processed indium oxide with the room temperature anodization process for high-κ aluminum oxide gate dielectric.

The room temperature processed anodized high-κ aluminum oxide (Al_2O_3) aided in the reduction of operating voltage and threshold voltages, as well as improved carrier versatility. Solution-processing, on the other hand, enables low-temperature, large-area depositions while lowering fabrication costs. The excellent electrical performance of solution-processed metal-oxide TFTs at a bias voltage will allow novel applications in flexible electronics. The bending performance and SPICE simulation alongside electrical characterization of the metal oxide TFTs was provided.

Furthermore, by using characterization techniques, such as AFM (atomic force microscopy), C-V (capacitance-voltage profiling), and TEM (transmission electron microscopy), a thorough analysis of the thin film and interface between metal oxide

semiconductor and gate dielectric was performed. Additionally, the fabrication and characterization of two TFT based inverter circuit on a flexible Kapton substrate using solution-processed metal-oxide was successfully demonstrated. As a result, solution processed, low temperature processed, low voltage operating flexible thin film transistors and circuits enables a viable pathway for the flexible electronics, wearables and the Internet of Things (IoT) applications. The techniques suggested in this thesis for designing and fabricating flexible thin film transistors and circuits for flexible electronics are readily adaptable and cost-effective.

6.2 Future Work

This dissertation presents low-temperature, low-voltage, solution-processed metal oxide thin film transistors with operating voltages well below 3.0 V along with a low threshold voltage between 0.43 and 1.05 V. Although the development of such an electronic device might open-up new avenues for flexible wearables and Internet of Things, among other low energy applications, many additional improvements should be done before unleashing the true potential of the metal oxide TFT for flexible electronics. For example, TFTs with high mobilities are essential for better switching performance.

Additionally, ensuring compatibility with flexible substrates may necessitate a further reduction in process temperature. For example, in the case of polyurethane, the lowest processing temperature target is restricted to 120 °C. Also, considerable investigation on TFT integration is required to enhance the device's performance and its potential for flexible electronics. In order to accomplish reduced threshold voltages along with higher mobility, it is also essential to find the most suitable dielectric material. Although there are a variety of solution processing approaches for depositing metal oxide, for optimal performance, advancements in solution processing are necessary. Some of the strategies that may be used are: 1. Low temperature processing for the metal oxide deposition, like atomic layer deposition (ALD), or equivalent, followed by UV (ultraviolet) or laser "photonic" annealing for recrystallization. 2. Improved TFT device architecture with sub-micron (or tens of nanometer) gates, preferably through a self-assembled process, along with meticulous shadow mask designs. 3. Employment of printing processes for the metal oxide semiconductor deposition.

REFERENCES

[1] A. Nathan, G. R. Chaji and S. J. Ashtiani, Driving Schemes for a-Si and LTPS AMOLED Displays, *Journal of Display Technology*, vol. 1, no. 2, pp. 267-277, Dec. 2005.

[2] R. A. Street, Thin-Film Transistors, *Adv. Mater.,* vol. 21, no. 20, pp. 2007-2022, May 2009.

[3] E. Fortunato, P. Barquinha and R. Martins, Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances, *Adv. Mater.,* vol. 24, no. 22, pp. 2945-2986, June 2012.

[4] J. W. Park, B. H. Kang and H. J. Kim, A Review of Low-Temperature Solution-Processed Metal Oxide Thin-Film Transistors for Flexible Electronics, *Adv. Funct. Mater.,* vol. 30, no. 20, pp 1904632, May 2020.

[5] W. Gao, H. Ota, D. Kiriya, K. Takei and A. Javey, Flexible Electronics toward Wearable Sensing, *Acc. Chem. Res.,* vol. 52, pp. 523-533, Feb. 2019.

[6] G. Cantarella, J. Costa, T. Meister, K. Ishida, C. Carta, F. Ellinger, P. Lugli, N. Münzenrieder and L. Petti, Review of recent trends in flexible metal oxide thin-film transistors for analog applications, *Flex. Print. Electron,* vol. 5, no. 3, pp. 033001, Aug. 2020.

[7] P. Wang, M. Hu, H. Wang, Z. Chen, Y. Feng, J. Wang, W. Ling and Y. Huang, The Evolution of Flexible Electronics: From Nature, Beyond Nature, and To Nature, *Adv. Sci.,* vol. 7, no. 20, pp. 2001116, Oct. 2020.

[8] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors, *Nature,* vol. 432, pp. 488-492, Nov. 2004.

[9] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano And H. Hosono, Amorphous Oxide Semiconductors for High-Performance Flexible Thin-Film

Transistors, *Japanese Journal of Applied Physics,* vol. 45, no. 5S, pp. 4303-4308, May 2006.

[10] X. Cao, H. Chen, X. Gu, B. Liu, W. Wang, Y. Cao, F. Wu and C. Zhou, Screen Printing as a Scalable and Low-Cost Approach for Rigid and Flexible Thin-Film Transistors Using Separated Carbon Nanotubes, *ACS Nano,* vol. 8, no. 12, pp. 12769-12776, Dec. 2014.

[11] T. P. Brody, J. A. Asars and G. D. Dixon, A 6 × 6 inch 20 lines-per-inch liquid-crystal display panel, *IEEE Transactions on Electron Devices,* vol. 20, no. 11, pp. 995-1001, Nov. 1973.

[12] A. J. Snell, K. D. Mackenzie, W. E. Spear, P. G. LeComber and A. J. Hughes, Application of amorphous silicon field effect transistors in addressable liquid crystal display panels, *Applied Physics A,* vol. 24, pp. 357–362, Apr. 1981.

[13] H. Matsui, Y. Takeda and S. Tokito, Flexible and printed organic transistors: From materials to integrated circuits, *Organic Electronics,* vol. 75, pp. 105432, Dec. 2019.

[14] M. Magliulo, M. Y. Mulla, M. Singh, E. Macchia, A. Tiwari, L. Torsi and K. Manoli, Printable and flexible electronics: from TFTs to bioelectronic devices, J. *Mater. Chem. C,* vol. 3, no. 48, pp. 12347-12363, Nov. 2015.

[15] C. Cao, J. B. Andrews and A. D. Franklin, Completely Printed, Flexible, Stable, and Hysteresis-Free Carbon Nanotube Thin-Film Transistors via Aerosol Jet Printing, *Adv. Electron. Mater.,* vol. 3, no. 5, pp. 1700057, May 2017.

[16] G. E. Moore, Cramming more components onto integrated circuits, *Electronics,* vol. 38, no. 8, Apr. 1965.

[17] J. Meindl, Theoretical Practical and Analogical Limits in ULSI, *IEEE International Electron Devices Meeting,* Dec. 1983.

[18] Y. B. Zikria, R. Ali, M. K. Afzal and S. W. Kim, Next-Generation Internet of Things (IoT): Opportunities, Challenges, and Solutions, *Sensors,* vol. 21, pp. 1174, Feb. 2021.

[19] H. Hosono, Oxide TFTs, Handbook of Visual Display Technology, *Springer,* pp 729-749, 2012.

[20] Y. Kuo, Thin Film Transistor Technology - Past, Present, and Future, *The Electrochemical Society Interface,* Spring 2013.

[21] S. Gupta, W. Taube N., L. Lorenzelli and R. Dahiya, Ultra-thin chips for high-performance flexible electronics, *npj Flexible Electronics,* vol. 2, no. 8, Mar. 2018.

[22] S. Li and D. Chu, A review of thin-film transistors/circuits fabrication with 3D self- aligned imprint lithography, *Flex. Print. Electron.,* vol. 2, no. 1, pp. 013002, Mar. 2017.

[23] E. H. Nicollian and J. R. Brews, MOS (metal oxide semiconductor) physics and technology, Dec. 2002.

[24] M. Lorenz, M. S. R. Rao, T. Venkatesan, E. Fortunato, P. Barquinha, R. Branquinho, D. Salgueiro, R. Martins, E. Carlos and A. Liu, The 2016 oxide electronic materials and oxide interfaces roadmap, *Journal of Physics D: Applied Physics,* vol. 49, no. 43, Oct 2016.

[25] H. He, 2 - Metal oxide semiconductors and conductors, *Metal Oxides,* 2020.

[26] J. Srivastava, S. Nahas, S. Bhowmick and A. Gaur, Electronic structure and transport in amorphous metal oxide and amorphous metal oxynitride semiconductors, *J. Appl. Phys.,* vol. 126, no. 12, pp. 125702, Mar. 2019.

[27] H-X. Deng, J-W. Luo, S-H. Wei, Band structure engineering and defect control of oxides for energy applications, *Chinese Physics B,* vol. 27. no. 11, pp. 117104, Oct. 2018.

[28] Z. Yin, M. Tordjman, Y. Lee, A. Vardi, R. Kalish and J. A. d. Alamo, Enhanced transport in transistor by tuning transition-metal oxide electronic states interfaced with diamond, *Science Advances,* vol. 4, no. 9, pp. eaau0480, Sep 2018.

[29] S. R. Thomas, P. Pattanasattayavong and T. D. Anthopoulos, Solution-processable metal oxide semiconductors for thin-film transistor applications, *Chem. Soc. Rev.,* vol. 42, no. 16, pp. 6910-6923, Jun 2013.

[30] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos and G. Tröster, "Metal oxide semiconductor thin-film transistors for flexible electronics", *Applied Physics Reviews*, vol. 3, no. 2, pp. 021303, Apr. 2016.

[31] P. R. Berger, M. Li, R. M. Mattei, M. A. Niang, N. Talisa, M. Tripepi, B. Harris, S. R. Bhalerao, E. A. Chowdhury, C. H. Winter and D. Lupo, Advancements in Solution Processable Devices using Metal Oxides For Printed Internet-of-Things Objects, *Electron Devices Technology and Manufacturing Conference (EDTM)*, pp. 160-162, March 2019.

[32] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard and H. Sirringhaus, Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol–gel on chip' process, *Nature Materials,* vol. 10, pp. 45-50, Jan. 2011.

[33] M. Eslamian, Inorganic and Organic Solution-Processed Thin Film Devices, *Nano-Micro Letters,* vol. 9, no. 3, Sept 2017.

[34] F. P. G. d. Arquer, A. Armin, P. Meredith and E. H. Sargent, Solution-processed semiconductors for next-generation photodetectors, *Nature Reviews Materials,* vol. 2, no. 16100, 2017.

[35] S. Parka, C-H. Kim, W-J. Lee, S. Sung, M-H. Yoon, Sol-gel metal oxide dielectrics for all-solution-processed electronics, *Materials Science and Engineering: R: Reports,* vol. 114, pp. 1–22, Apr. 2017.

[36] Y. Choi, G. H. Kim, W. H. Jeong, H. J. Kim, B. D. Chin and J-W. Yu, Characteristics of gravure printed InGaZnO thin films as an active channel layer in thin film transistors, *Thin Solid Films,* vol. 518, no. 22, pp. 6249-6252, Sept. 2010.

[37] W. Scheideler and V. Subramanian, Printed flexible and transparent electronics: enhancing low-temperature processed metal oxides with 0D and 1D nanomaterials, *Nanotechnology,* vol. 30, no. 27, pp. 272001, July 2019.

[38] Y. Zhan, Y. Mei and L. Zheng, Materials capability and device performance in flexible electronics for the Internet of Things, *J. Mater. Chem. C,* vol. 2, no. 7, pp. 1220-1232, Nov. 2014.

[39] T. D. Ngo, A. Kashani, G. Imbalzano, K. T.Q. Nguyen and D. Hui, Additive manufacturing (3D printing): A review of materials, methods, applications and challenges, *Composites Part B: Engineering*, vol. 143, pp. 172-196, June 2018.

[40] K-Si Kwon, M. K. Rahman, T. H. Phung, S. D. Hoath, S. Jeong and J. S. Kim, Review of digital printing technologies for electronic materials, *Flex. Print. Electron.,* vol. 5, no. 4, pp. 043003, Dec. 2020.

[41] M. S. Hossain, T. Li, Y. Yu, J. Yong, J-H. Bahk and E. Skafidas, Recent advances in printable thermoelectric devices: materials, printing techniques, and applications, *RSC Adv.,* vol. 10, no. 14, pp. 8421-8434, Feb. 2020.

[42] B. D. Gates, Q. Xu, M. Stewart, D. Ryan, C. G. Willson and G. M. Whitesides, New Approaches to Nanofabrication : Molding, Printing, and Other Techniques, *Chem. Rev.,* vol. 105, no. 4, pp. 1171-1196, Mar. 2005.

[43] M. Geiger, R. Acharya, E. Reutter, T. Ferschke, U. Zschieschang, J. Weis, J. Pflaum, H. Klauk and R. T. Weitz, Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors, *Adv. Mater. Interfaces,* vol. 7, no. 10, pp. 1902145, May 2020.

[44] K. Kandpal and N. Gupta, Investigations on high-κ dielectrics for low threshold voltage and low leakage zinc oxide thin-film transistor, using material selection methodologies, *Journal of Materials Science: Materials in Electronics,* vol. 27, pp. 5972-5981, Feb. 2016.

[45] C. Avis and J. Jang, High-performance solution processed oxide TFT with aluminum oxide gate dielectric fabricated by a sol–gel method, *Journal of Materials Chemistry,* vol. 21, no. 29, pp. 10649-10652, Jun 2011.

[46] D. Spassov, A. Skeparovski, A. Paskaleva and N. Novkovski, A comparative study of charge trapping in HfO2/Al2O3 and ZrO2/Al2O3 based multilayered metal/high-κ/oxide/Si structures, *Thin Solid Films,* vol. 614, Part A, pp. 7-15, Sept. 2016.

[47] S. Mohsenifar and M. H. Shahrokhabadi, Gate Stack High-κ Materials for Si-Based MOSFETs Past, Present, and Futures, *Microelectronics and Solid State Electronics,* vol. 4, no. 1, pp. 12-24, 2015.

[48] J. Xie, Z. Zhu, H. Tao, S. Zhou, Z. Liang, Z. Li, R. Yao, Y. Wang, H. Ning and J. Peng, Research Progress of High Dielectric Constant Zirconia-Based Materials for Gate Dielectric Application, *Coatings,* vol. 10, no. 7, pp. 698, July 2020.

[49] S. Gierałtowska, L. Wachnicki, B. S. Witkowski, M. Godlewski and E. Guziewicz, Properties of thin films of high-κ oxides grown by atomic layer deposition at low temperature for electronic applications, *Optica Applicata,* vol. XLIII, no. 1, 2013.

[50] S. Kol and A.Y. Oral, Hf-Based High-κ Dielectrics: A Review, *ACTA Physica Polonica A,* vol. 136, no. 6, 2019.

[51] C. Zhao, C. Z. Zhao, M. Werner, S. Taylor and P. Chalker, Dielectric relaxation of high-κ oxides, *Nanoscale Research Letters,* vol. 8, no. 456, Nov. 2013.

[52] H-R Byun, E-A. You and Y-G. Ha, Room-temperature solution-processed, ZrOx-based hybrid gate dielectrics for low- voltage organic thin-film transistors on plastic substrates, *Appl. Phys. Lett.,* vol. 114, pp. 013301, Jan. 2019.

[53] H. S. Tan, T. Cahyadi, Z. B. Wang, A. Lohani, Z. Tsakadze, S. Zhang, F. R. Zhu, and S. G. Mhaisalkar, Low-Temperature-Processed Inorganic Gate Dielectrics for Plastic-Substrate-Based Organic Field-Effect Transistors, *IEEE Electron Device Letters,* vol. 29, no. 7, July 2008.

[54] W-Y. Lin, R. Müller, K. Myny, S. Steudel, J. Genoe and P. Heremans, Room-temperature solution-processed high-κ gate dielectrics for large area electronics applications, *Organic Electronics,* vol. 12, no. 6, pp. 955–960, June 2011.

[55] D. Akinwande, N. Petrone and J. Hone, Two-dimensional flexible nanoelectronics, *Nature Communications,* vol. 5, no. 5678, Dec. 2014.

[56] W. Wu, Stretchable electronics: functional materials, fabrication strategies and applications, *Science and Technology of Advanced Materials,* vol. 20, no. 1, pp. 187-224, Mar. 2019.

[57] H-P Phan, Implanted Flexible Electronics : Set Device Lifetime with Smart Nanomaterials, *Micromachines,* vol. 12, no. 157, 2021.

[58] H. Zhang, Y. Lan, S. Qiu, S. Min, H. Jang, J. Park, S. Gong and Z. Ma, Flexible and Stretchable Microwave Electronics : Past, Present, and Future Perspective, *Adv. Mater. Technol.,* vol. 6, no. 2000759, 2021.

[59] M. Zou, Y. Ma, X. Yuan, Y. Hu, J. Liu and Zhong Jin, Flexible devices: From materials, architectures to applications, *J. Semicond.,* vol. 39, no. 011010, 2018.

[60] T. Dinh, H-P. Phan, T-K. Nguyen, A. Qamar, A. Riduan M. Foisal, T. Nguyen Viet, C-D. Tran, Y. Zhu, N-T. Nguyen and D. V. Dao, Environment-friendly carbon nanotube based flexible electronics for noninvasive and wearable healthcare, *J. Mater. Chem. C,* vol. 4, pp. 10061-10068, 2016.

[61] M. Gao, L. Li and Y. Song, Inkjet printing wearable electronic devices, *J. Mater. Chem. C,* vol. 5, pp. 2971-2993, 2017.

[62] K J Yu, Z. Yan, M. Han and J. A. Rogers, Inorganic semiconducting materials for flexible and stretchable electronics, *npj Flexible Electronics,* vol. 4, 2017.

[63] Y. Kim, O Y. Kweon, Y. Won and J. H. Oh, Deformable and Stretchable Electrodes for Soft Electronic Devices, *Macromol. Res.,* vol. 27, no. 7, pp. 625-639, 2019.

[64] P. Bocchetta, D. Frattini, S. Ghosh, A. Mohanan V. Mohan, Y. Kumar and Y. Kwon, Soft Materials for Wearable/Flexible Electrochemical Energy Conversion, Storage, and Biosensor Devices, *Materials,* vol. 13, no. 12, pp. 2733, 2020.

[65] L. Yin, J. Lv and J. Wang, Structural Innovations in Printed, Flexible, and Stretchable Electronics, *Adv. Mater. Technol.,* vol. 5, no. 2000694, 2020.

[66] J. P. Seymour, F. Wu, K. D. Wise and E. Yoon, State-of-the-art MEMS and microsystem tools for brain research, *Microsystems & Nanoengineering,* vol. 3, no. 16066, Jan. 2017.

[67] N. Yamauchi, Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization : Theory, experiments, and thin-film transistor applications, *Journal of Applied Physics,* vol. 75, no. 3235, 1994.

[68] Y. Kuo, Thin Film Transistor Technology - Past, Present, and Future, *Electrochem. Soc. Interface,* vol. 22, no. 55, 2013.

[69] Y-H. Chen, S-J. Chang and T-J. Hsueh, Si-Based MOSFET and Thin Film Transistor Prepared via Hot Wire Implantation Doping Technique, *IEEE Electron Device Letters,* vol. 36, no. 2, Feb. 2015.

[70] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter and Y. Kawaguchi, The trench power MOSFET: Part I - History, technology, and prospects, *IEEE Transactions on Electron Devices,* vol. 64, no. 3, Mar. 2017.

[71] M. Chhowalla, D. Jena and H. Zhang, Two-dimensional semiconductors for transistors, *Nature Reviews Materials,* vol. 1, no. 16052, Nov. 2016.

[72] A. C Tickle, Thin-film Transistors. A New Approach to Microelectronics, *Wiley,* 1969.

[73] A. Tixier-Mita, S. Ihida, B-D. Ségard, G. A. Cathcart, T. Takahashi, Hiroyuki Fujita and H. Toshiyoshi, Review on thin-film transistor technology, its applications, and possible new applications to biological cells, *Japanese Journal of Applied Physics,* vol. 55, no. 04EA08, March 2016.

[74] S. D. Brotherton, Introduction to thin film transistors : Physics and technology of TFTs, *Springer,* 2013.

[75] N. Lu, W. Jiang, Q. Wu, D. Geng, L. Li and M. Liu, A Review for Compact Model of Thin-Film Transistors (TFTs), *Micromachines,* vol. 9, no. 11, pp. 599, 2018.

[76] S M Sze and K K Ng, Physics of Semiconductor Devices, 3rd edition, *New York: Wiley,* 2006.

[77] H. Shichman and D. A. Hodges, Modeling and simulation of insulated-gate field-effect transistor switching circuits, *IEEE J. Solid-State Circuits,* vol. 3, no. 3, pp. 285–289, Sept. 1968.

[78] D. K. Schroder, Semiconductor Material and Device Characterization, *Wiley-IEEE Press,* June 2015.

[79] A. Nair, P. Bhattacharya and S. Sambandan, Modulating Thin Film Transistor Characteristics by Texturing the Gate Metal, *Scientific Reports,* vol. 7, no. 17932, Dec. 2017.

[80] K. Ono, T. Aoyama, N. Konishi and K. Miyata, Analysis of Current-Voltage Characteristics of Low-Temperature-Processed Polysilicon Thin-Film Transistors, *IEEE Transactions on Electron Devices,* vol. 39. no. 4, Apr. 1992.

[81] S. Samanta, B. Tiwari, P. G. Bahubalindruni, P. Barquinha and J. Goes, Threshold voltage extraction techniques adaptable from sub-micron CMOS to large-area oxide TFT technologies, *Int. J. Circ. Theor.,* vol. 45, no. 12, pp. 2201-2210, Apr. 2017.

[82] R. Shringarpure, S. Venugopal, Z. Li, L. T. Clark, D. R. Allee, E. Bawolek and D. Toy, Circuit Simulation of Threshold-Voltage Degradation in a-Si:H TFTs Fabricated at 175 °C, *IEEE Transactions on Electron Devices,* vol. 54, no. 7, July 2007.

[83] A. F. Paterson and T. D. Anthopoulos, Enabling thin-film transistor technologies and the device metrics that matter, *Nat Commun.,* vol. 9, no. 5264, Dec. 2018.

[84] Y-H. Lin, H. Faber, J. G. Labram, E. Stratakis, L. Sygellou, E. Kymakis, N. A. Hastas, R. Li, K. Zhao, A. Amassian, N. D. Treat, M. McLachlan, T. D. Anthopoulos, High Electron Mobility Thin-Film Transistors Based on Solution-Processed Semiconducting Metal Oxide Heterojunctions and Quasi-Superlattices, *Adv. Sci.,* vol. 2, no. 1500058, May 2015.

[85] T. Uemura, C. Rolin, T-H. Ke, P. Fesenko, J. Genoe, P. Heremans and J. Takeya, On the Extraction of Charge Carrier Mobility in High-Mobility Organic Transistors, *Adv. Mater.,* vol. 28, no. 1, pp. 151–155, Nov. 2016.

[86] T. T. Mnatsakanov, M. E. Levinshtein, L. I. Pomortseva and S. N. Yurkov, Carrier mobility model for simulation of SiC-based electronic devices, Semicond. *Sci. Technol.,* vol. 17, no. 9, pp. 974, Feb. 2002.

[87] I. Katsouras, D. Zhao, M-J. Spijkman, M. Li, P. W. M. Blom, D. M. de Leeuw and K. Asadi, Controlling the on/off current ratio of ferroelectric field-effect transistors, *Scientific Reports,* vol. 5, no. 12094, July 2015.

[88] Y. Feng, K. Lee, H. Farhat and J. Kong, Current on/off ratio enhancement of field effect transistors with bundled carbon nanotubes, *Journal of Applied Physics,* vol. 106, no. 104505, Nov. 2009.

[89] C-J. Shih, Q. H. Wang, Y. Son, Z. Jin, D. Blankschtein and M. S. Strano, Tuning On–Off Current Ratio and Field-Effect Mobility in a MoS_2-Graphene Heterostructure via Schottky Barrier Modulation, *ACS Nano,* vol. 8, no. 6, pp. 5790-5798, May 2014.

[90] E. H. Nicollian, J. R. Brews, MOS (metal oxide semiconductor) physics and technology, *Wiley,* Dec. 2002.

[91] S. S. Li, Metal-Oxide-Semiconductor Field-Effect Transistors, Semiconductor Physical Electronics, *Springer,* pp. 567-612, 2006.

[92] K. J. Yang and C. Hu, MOS capacitance measurements for high-leakage thin dielectrics, *IEEE Transactions on Electron Devices,* vol. 46, no. 7, Jul 1999.

[93] D. E. Ward, R. W. Dutton, A charge-oriented model for MOS transistor capacitances, *IEEE Journal of Solid-State Circuits,* vol. 13, no. 5, Oct. 1978.

[94] A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu and M. Paniccia, A high-speed silicon optical modulator based on a metal–oxide–semiconductor capacitor, *Nature,* vol, 427, pp. 615–618, Feb. 2004.

[95] N. Arora, MOS Capacitor, MOSFET Models for VLSI Circuit Simulation, pp 121-166, *Springer-Verlag/Wien,* 1993.

[96] D. Varghese, V. Reddya, S. Krishnana, M. A. Alamb, OFF-state degradation and correlated gate dielectric breakdown in high voltage drain extended transistors: A review, *Microelectronics Reliability,* vol. 54, no. 8, pp. 1477-1488, Aug. 2014.

[97] B. E. Weir, C-C. Leung, P. J. Silverman, M. A. Alam, Gate dielectric breakdown : A focus on ESD protection, *IEEE International Reliability Physics Symposium,* July 2004.

[98] H. N. Chem, C. L. Lee and T. F. Lei, An analytical model for the above-threshold characteristics of polysilicon thin-film transistors, *IEEE Transactions on Electron Devices,* vol. 42, no. 7, July 1995.

[99] T. Zaki, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk and J. N. Burghartz, S-Parameter Characterization of Submicrometer Low-Voltage

Organic Thin-Film Transistors, *IEEE Electron Device Letters,* vol. 34, no. 4, Apr. 2013.

[100] R. R. Haering, Theory of thin film transistor operation, *Solid-State Electronics,* vol. 7, no. 1, pp. 31-38, Jan. 1964.

[101] M. Shur, A new analytic model for amorphous silicon thin-film transistors, *Journal of Applied Physics,* vol. 66, no. 7, pp. 3371, Aug. 1998.

[102] W. Y. Choi, B-G. Park, J. D. Lee and T-J. K. Liu, Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec, *IEEE Electron Device Letters,* vol. 28, no. 8, Augn 2007.

[103] W. Cao, D. Sarkar, Y. Khatami, J. Kang and K. Banerjee, Subthreshold-swing physics of tunnel field-effect transistors, *AIP Advances,* vol. 4, no. 4, pp. 067141, June 2014.

[104] Z. A. Lamport, K. J. Barth, H. Lee, E. Gann, S. Engmann, H. Chen, M. Guthold, I. McCulloch, J. E. Anthony, L. J. Richter, D. M. DeLongchamp and O. D. Jurchescu, A simple and robust approach to reducing contact resistance in organic transistors, *Nature Communications,* vol 9, pp. 5130, Dec. 2018.

[105] J. W. Borchert, B. Peng, F. Letzkus, J. N. Burghartz, P. K. L. Chan, K. Zojer, S. Ludwigs and H. Klauk, Small contact resistance and high-frequency operation of flexible low-voltage inverted coplanar organic transistors, *Nature Communications,* vol. 10, pp. 1119, Mar. 2019.

[106] M. Lijadi, F. Pardo, N. Bardou, J-L. Pelouard, Floating contact transmission line modelling: An improved method for ohmic contact resistance measurement, *Solid-State Electronics,* vol. 49, no. 10, pp. 1655-1661, Oct. 2005.

[107] T. Abbas and L. Slewa, Transmission line method (TLM) measurement of (metal/ZnS) contact resistance, *Int. J. Nanoelectronics and Materials,* vol. 8, pp. 111-120, Jan 2015.

[108] M. Geiger, L. Schwarz, U. Zschieschang, D. Manske, J. Pflaum, J. Weis, H. Klauk and R. T. Weitz, Quantitative Analysis of the Density of Trap States in Semiconductors by Electrical Transport Measurements on Low-Voltage Field-Effect Transistors, *Physical Review Applied,* vol. 10, pp. 044023, Oct. 2018.

[109] R. Engel-Herbert, Y. Hwang and S. Stemmer, Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces, *Journal of Applied Physics,* vol. 108, no. 12, pp. 124101, Oct. 2010.

[110] Y. Hwang, R. Engel-Herbert, N. G. Rudawski and S. Stemmer, Analysis of trap state densities at $HfO_2/In_{0.53}Ga_{0.47}As$ interfaces, *Applied Physics Letters,* vol. 96, no. 10, pp. 102910, Feb. 2010.

[111] R. Engel-Herbert, Y. Hwang and S. Stemmer, Quantification of trap densities at dielectric/III–V semiconductor interfaces, *Applied Physics Letters,* vol. 97, no. 6, pp. 062905, Aug. 2010.

[112] H. Matsubara, T. Sasada, M. Takenaka and S. Takagia, Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation, *Applied Physics Letters,* vol. 93, no. 3, pp. 032104, July 2008.

[113] S. C. Boehme, J. M. Azpiroz, Y. V. Aulin, F. C. Grozema, D. Vanmaekelbergh, L. D. A. Siebbeles, I. Infante and A. J. Houtepen, Density of Trap States and Auger-mediated Electron Trapping in CdTe Quantum-Dot Solids, *Nano Lett.,* vol. 15, no. 5, pp 3056-3066, May 2015.

[114] L. Zhang, W. Xiao, W. Wu and B. Liu, Research Progress on Flexible Oxide-Based Thin Film Transistors, *Appl. Sci.,* vol. 9, no. 4, pp. 773, Feb. 2019.

[115] J. Lee, D. Kim, H-Y. Ryoo and B-S. Shin, Sustainable Wearables: Wearable Technology for Enhancing the Quality of Human Life, *Sustainability,* vol. 8, pp. 466, May 2016.

[116] J. E. Medvedeva, D. B. Buchholz and R. P. H. Chang, Recent advances in understanding the structure and properties of amorphous oxide semiconductors, *Adv. Electron. Mater.,* vol. 3, no. 9, pp. 1700082, Sep. 2017.

[117] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K.A. Jones, R. J. Kaplar, S. Rajan, C. G. Van de Walle, E. Bellotti, C. L.Chua, R. Collazo, M. E. Coltrin, J. A. Cooper, K. R. Evans, S. Graham, T. A. Grotjohn, E. R. Heller, M. Higashiwaki, M. S. Islam, P. W. Juodawlkis, M. A. Khan, A. D. Koehler, J. H. Leach, U. K. Mishra, R. J. Nemanich, R. C. N. Pilawa-Podgurski, J. B. Shealy, Z. Sitar, M. J.Tadjer, A. F. Witulski, M. Wraback and J. A. Simmons,

Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges, *Adv. Electron. Mater.,* vol. 4, no. 1, pp. 1600501, Dec. 2017.

[118] W. Xu, L. Hu, C. Zhao, L. Zhang, D. Zhu, P. Cao, W. Liu, S. Han, X. Liu, F. Jia, Y. Zeng, Y. Lu, Low temperature solution-processed IGZO thin-film transistors, *Applied Surface Science,* vol. 455, no. 15, pp 554-560, Oct. 2018.

[119] M. Miyakawa, M. Nakata, H. Tsuji and Y. Fujisaki, Highly stable low-temperature aqueous solution-processed oxide thin-film transistors by the hydrogen injection and oxidation method, *Flexible and Printed Electronics,* vol. 3, no. 2, pp. 025005, June 2018.

[120] M. G. Kim, H. S. Kim, Y. G. Ha, J. Q. He, M. G. Kanatzidis, A. Facchetti and T. J. Marks, High-Performance Solution-Processed Amorphous Zinc-Indium-Tin Oxide Thin-Film Transistors, *J. Am. Chem. Soc.,* vol. 132, pp. 10352–10364, July 2010.

[121] J. H. W. De Wit, G. V. Unen and M. Lahey, Electron concentration and mobility in In_2O_3, *J. Phys. Chem. Solids,* vol. 38, no. 8, pp 819–824, 1977.

[122] S. R. Bhalerao, D. Lupo, A. Zangiabadi, I. Kymissis, J. Leppaniemi, A. Alastalo and Paul R. Berger, 0.6V Threshold Voltage Thin Film Transistors with Solution Processable Indium Oxide (In_2O_3) Channel and anodized high-κ Al_2O_3 Dielectric, *IEEE Electron Device Letters,* vol. 40, no. 7, pp. 1112-1115, July 2019. DOI: 10.1109/LED.2019.2918492

[123] S. R. Bhalerao, D. Lupo and P. R. Berger, 2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton, *IEEE International Flexible Electronics Technology Conference (IFETC),* Aug. 2019. DOI: 10.1109/IFETC46817.2019.9073721

[124] S. R. Bhalerao, D. Lupo and P. R. Berger, Flexible, Solution Processed, Indium Oxide (In_2O_3) Thin Film Transistor (TFT) and Circuits for Internet-of-Things (IoT), *Materials Science in Semiconductor Processing,* Aug 2021. (Accepted).

[125] S. R. Bhalerao, D. Lupo and P. R. Berger, Flexible Gallium Oxide (Ga_2O_3) Thin Film Transistors (TFTs) and Circuits for the Internet of Things (IoT)", *IEEE International Flexible Electronics Technology Conference (IFETC),* Aug. 2021. DOI: 10.1109/IFETC49530.2021.9580524

[126] S. R. Bhalerao, D. Lupo and P. R. Berger, Flexible Thin Film Transistors (TFTs) and Circuits for Internet of Things (IoT) based on Solution processed Indium Gallium Zinc Oxide (IGZO), *IEEE International Flexible Electronics Technology Conference (IFETC),* Aug. 2021. DOI: 10.1109/IFETC49530.2021.9580506

[127] J-W Jo, K-T Kim, H-H Park and S K Park, High-Speed and Low-Temperature Atmospheric Photo-Annealing of Large-Area Solution- Processed IGZO Thin-Film Transistors by Using Programmable Pulsed Operation of Xenon Flash Lamp, *Journal of the Korean Physical Society,* vol. 74, no. 11, pp. 1052-1058, June 2019.

[128] Y. He, X. Wang, Y. Gao, Y. Hou and Q. Wan, Oxide-based thin film transistors for flexible electronics, *J. Semicond.,* vol 39, no. 1, pp. 011005, 2018.

[129] J. J. Licari and L. R. Enlow, 3 - Thin Film Processes, Hybrid Microcircuit Technology Handbook (Second Edition) Materials, Processes, Design, Testing and Production, *William Andrew Inc.,* pp. 63-103, 1998.

[130] K. R. Sarma, Flexible Displays: TFT Technology: Substrate Options and TFT Processing Strategies, Handbook of Visual Display Technology, *Springer-Verlag Berlin Heidelberg,* pp 897-932, 2012

[131] S. Khan, L. Lorenzelli and R. S. Dahiya, Technologies for Printing Sensors and Electronics Over Large Flexible Substrates: A Review, *IEEE Sensors Journal,* vol. 15, no. 6, pp. 3164 – 3185, June 2015.

[132] P. R Berger, M. M. Hussain, F. Iacopi, J. Schulze, P. Ye, W. Rachmady, H-C. Wen and S. Krishnan, Foreword Special Issue on Low-Temperature Processing of Electronic Materials for Cutting Edge Devices, *IEEE Transactions on Electron Devices,* vol. 68, no. 7, July 2021.

[133] Y. Khan, A. Thielens, S. Muin, J. Ting, C. Baumbauer and A. C. Arias, A New Frontier of Printed Electronics: Flexible Hybrid Electronics, *Adv. Mater.,* vol. 32, no. 15, pp. 1905279, Nov. 2019.

[134] S. K. Garlapati, M. Divya, B. Breitung, R. Kruk, H. Hahn and S. Dasgupta, Printed Electronics Based on Inorganic Semiconductors: From Processes and Materials to Devices, *Adv. Mater.,* vol. 30, no. 40, pp. 1707600, June 2018

[135] S. Wilson, R. Hunt, B. Duffy, The rate of spreading in spin coating, *Journal of Fluid Mechanics,* vol. 413, pp. 65-88, June 2000.

[136] C.-C. Lai and F.-C. Chou, Effect of Relaxation Time on Spin Coating Instability, *Japanese Journal of Applied Physics,* vol. 47, no. 8R, pp. 6569, Aug. 2008.

[137] S. Bubel, S. Meyer, F. Kunze and M. L. Chabinyc, Ionic liquid gating reveals trap-filled limit mobility in low temperature amorphous zinc oxide, *Appl. Phys. Lett.,* vol. 103, no. 15, pp. 152102, Oct. 2013.

[138] M. Kaltenbrunner, P. Stadler, R. Schwödiauer, A. W. Hassel, N. S. Sariciftci, and S. Bauer, Anodized aluminum oxide thin films for room-temperature-processed, flexible, low-voltage organic non-volatile memory elements with excellent charge retention, *Adv. Mater.,* vol. 23, no. 42, pp. 4892-4896, Sep. 2011.

[139] Y. Qin, D. H. Turkenburg, I. Barbu, W. T. T. Smaal, K. Myny, W.-Y. Lin, G. H. Gelinck, P. Heremans, J. Liu and E. R. Meinders, Organic thin- film transistors with anodized gate dielectric patterned by self-aligned embossing on flexible substrates, *Adv. Funct. Mater.,* vol. 22, no. 6, pp. 1209-1214, Jan. 2012.

[140] R. Hu, Y. Pei, Z. Chen, J. Yang, Y. Li, J. Lin, Y. Zhao, C. Wang, J. Liang, B. Fan and G. Wang, Ultra-high field-effect mobility thin-film transistors with metal–organic chemical vapor deposition grown In_2O_3 channel treated by oxygen microwave plasma, *IEEE Electron Device Lett.,* vol. 36, no. 11, pp. 1163-1165, Nov. 2015.

[141] O. Bierwagen and J. S. Speck, High electron mobility In_2O_3(001) and (111) thin films with nondegenerate electron concentration, *Appl. Phys. Lett.,* vol. 97, no. 7, pp. 072103, Aug. 2010

[142] J.-W. Choi, S.-Y. Han, M.-C. Nguyen, A. H.-T. Nguyen, J. Y. Kim, S. Choi, J. Cheon, H. Ji and R. Choi, Low-temperature solution-based In_2O_3 channel formation for thin-film transistors using a visible laser- assisted combustion process, *IEEE Electron Device Lett.,* vol. 38, no. 9, pp. 1259-1262, Sep. 2017.

[143] J. H. Noh, S. Y. Ryu, S. J. Jo, C. S. Kim, S.-W. Sohn, P. D. Rack, D.-J. Kim, and H. K. Baik, Indium oxide thin-film transistors fabricated by RF sputtering at room temperature, *IEEE Electron Device Lett.,* vol. 31, no. 6, pp. 567-569, June 2010.

[144] M. Zirkl, A. Haase, A. Fian, H. Schön, C. Sommer, G. Jakopic, G. Leising, B. Stadlober, I. Graz, N. Gaar, R. Schwödiauer, S. Bauer-Gogonea and S. Bauer, Low-Voltage Organic Thin-Film Transistors with High-κ Nanocomposite Gate Dielectrics for Flexible Electronics and Optothermal Sensors, Adv. Mater., vol. 19, no. 17, pp. 2241-2245, Jul. 2007.

[145] K. Martens, C. O. Chui, G. Brammertz, B. D. Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes and G. Groeseneken, On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates, *IEEE Transactions on Electron Devices,* vol. 55, no. 2, Feb. 2008.

[146] S. Kundu, S. K. Roy and P. Banerji, GaAs metal–oxide–semiconductor device with titanium dioxide as dielectric layer: Effect of oxide thickness on the device performance, *Journal of Physics D: Applied Physics,* vol. 44, no. 15, pp. 155104, Apr. 2011.

[147] G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris and M. Heyns, Capacitance-voltage characterization of GaAs–oxide interfaces, *J. Electrochem. Soc.,* vol. 155, no. 12, pp. H945-H950, Oct. 2008.

[148] Y. Shi, Q. Zhou, A. Zhang, L. Zhu, Y. Shi, W. Chen, Z. Li and B. Zhang, Investigation of bulk traps by conductance method in the deep depletion region of the Al_2O_3/GaN MOS device, *Nanoscale Research Letters,* vol. 12, no. 342, May 2017.

[149] P. Xia, X. Feng, R. J. Ng, S. Wang, D. Chi, C. Li, Z. He, X. Liu and K.-W. Ang, Impact and origin of interface states in MOS capacitor with monolayer MoS_2 and HfO_2 High-κ dielectric, *Scientific Reports,* vol. 7, no. 40669, Jan. 2017

[150] E. H. Nicollian and A. Goetzberger, The Si-SiO_2 interface-Electrical properties as determined by the metal-insulator-silicon conductance technique, *Bell Syst. Tech. J.,* vol. 46, no. 6, pp. 1055–1133, Jul./Aug. 1967.

[151] T. T. Grove, M. F. Masters and R. E. Miers, Determining dielectric constants using a parallel plate capacitor, *Amer. J. Phys.,* vol. 73, no. 1, p. 52, July 2005.

PUBLICATIONS

Publication I Sagar R. Bhalerao, Donald Lupo, Amirali Zangiabadi, Ioannis Kymissis, Jaakko Leppaniemi, Ari Alastalo and Paul R. Berger, "0.6V Threshold Voltage Thin Film Transistors with Solution Processable Indium Oxide (In_2O_3) Channel and anodized high-κ Al_2O_3 Dielectric", IEEE Electron Device Letters, May 2019.
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Publication II Sagar R. Bhalerao, Donald Lupo and Paul R. Berger, "2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton", IEEE Xplore, IEEE International Flexible Electronics Technology Conference (IFETC), Aug. 2019.
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Publication III Sagar R. Bhalerao, Donald Lupo and Paul R. Berger, "Flexible, Solution Processed, Indium Oxide (In_2O_3) Thin Film Transistor (TFT) and Circuits for Internet-of-Things (IoT)", Materials Science in Semiconductor Processing, 2021
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PUBLICATION
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0.6V Threshold Voltage Thin Film Transistors with Solution Processable Indium Oxide (In_2O_3) Channel and anodized high-κ Al_2O_3 Dielectric

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0.6V Threshold Voltage Thin Film Transistors with Solution Processable Indium Oxide (In_2O_3) Channel and anodized high-κ Al_2O_3 Dielectric

Sagar R. Bhalerao, Donald Lupo, Amirali Zangiabadi, Ioannis Kymissis, Jaakko Leppaniemi, Ari Alastalo and Paul R. Berger, *IEEE Fellow*

***Abstract*— Low voltage operation and low processing temperature of metal oxide transistors remains a challenge. Commonly metal oxide transistors are fabricated at very high processing temperatures (above 500°C) and their operating voltage is quite high (30 – 50 V). Here, thin film transistors (TFT) are reported based upon solution processable indium oxide (In_2O_3) and room temperature processed anodized high-κ aluminum oxide (Al_2O_3) for gate dielectrics. The In_2O_3 TFTs operate well below the drain bias (V_{ds}) of 3.0 V, with on/off ratio 10^5, subthreshold swing (SS) 160 mV/dec, and low threshold voltage (V_{th}) 0.6 V. The electron mobility (μ) is as high as 3.53 $cm^2/V.s$ in the saturation regime and transconductance (g_m) 53 μS. Additionally, the detailed capacitance voltage (C-V) analysis to determine interface trap states density was also investigated. The interface trap density (D_{it}) in the oxide/semiconductor interface was quite low i.e. 0.99×10^{11} – 2.98×10^{11} $eV^{-1}\cdot cm^{-2}$, signifying acceptable compatibility of In_2O_3 with anodic Al_2O_3.**

***Index Terms*— Metal oxide semiconductors, solution processing, indium oxide (In_2O_3), low voltage, TFT, anodization, interface state density.**

I. Introduction

Metal oxide semiconductors have been extensively studied in the last few years for a wide range of devices and device applications such as thin film transistors (TFT) for transparent and flexible electronics, active matrix and flat panel displays, bio/medical sensors and radio frequency (RF) circuits [1-3]. Metal oxide semiconductors gained special attention due to their diverse spectrum of properties that distinguishes them from those of conventional silicon, such as wide band gap, wide optical transparency, high mobility and low temperature solution processable deposition [4]. They have paved the way for the next generation thin film and printed electronics [5]. Amongst all the metal-oxide semiconductors, indium oxide (In_2O_3) is the most favorable n-type semiconductors for thin film transistors with a band gap 3.6 – 3.75 eV and high carrier mobility [6]. However, most of the reported research on indium oxide thin film transistors has been based upon vacuum deposition techniques and high temperature annealing, with very high operating voltage 30 – 50 V [7, 8]. Whereas, TFTs based on solution processes have many desirable manufacturing advantages over conventional vacuum deposition processes, such as low cost, high yield and ease of processing [9, 10]. Although remarkable progress has been made, metal oxide TFTs still pose significant challenges, such as operating voltage, switching speed and on/off ratio.

Here we fabricated TFTs based upon In_2O_3 channels by combining the solution-processing route for the semiconductor and an anodization technique for the high-κ aluminum oxide Al_2O_3 gate dielectric, which enables a low operating voltage i.e. < 3V device operation. The anodization process was carried out as reported previously [11]. Anodization empowers the room temperature deposition of dielectric, bypassing high temperature, high vacuum processes, with added advantages such as nanoscale deposition, high quality and denser oxide layers to prevent gate leakage current [12]. Furthermore, the anodization process is a low cost, room temperature process, compatible with flexible and printed electronics devices. The detailed analysis of its electrical performance and thorough analysis of MOS capacitors for the interface trap states density was also investigated.

II. Experimental

The bottom gate, top contact (BGTC) topology was used here for the device fabrication as shown in Fig. 1. TFTs were fabricated on glass substrates. Prior to device fabrication, the glass substrates were ultrasonically cleaned with acetone, IPA

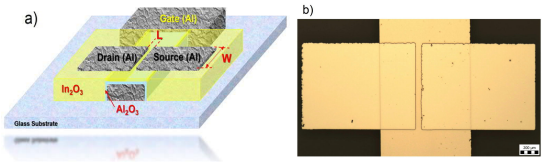

Fig. 1. a) Schematic structure of the In_2O_3 TFT with Al_2O_3 gate dielectric (for illustrative purposes). b) Optical image of the In_2O_3 TFT with 70 μm gate length. Scale bar is 200um.

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and deionized water for 30 minutes sequentially. Initially, to form a gate contact, 100 nm of aluminum (Al) metal was deposited on a glass substrate using a shadow mask for patterning.

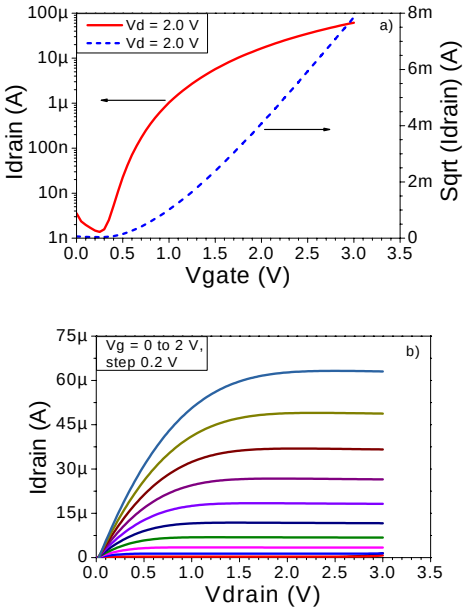

Fig. 2. a) Transfer characteristics of In_2O_3 TFTs with 70 µm gate lengths and b) Output characteristics for In_2O_3 TFTs with 70 µm gate lengths.

The anodization process was performed next to convert a top surface (~10 nm) of the aluminum metal into a high-κ dielectric, Al_2O_3. After the anodization, the substrates were thoroughly washed with deionized water. Furthermore, the In_2O_3 solution was prepared by dissolving Indium (III) nitrate hydrate $In(NO_3)_3{\cdot}xH_2O$ in anhydrous 2-methoxyethanol 99.8% in 0.2 M concentration as reported by Ari Alastalo *et al*. [13]. The solution was stirred for 12 hours at 75 °C prior to spin coating. All the precursors were purchased from Sigma-Aldrich and used as-is without any further distillation. Subsequently, the solution processed In_2O_3 semiconductor channel was deposited atop by first spin coating, followed by two-step annealing at 90 °C and at 300 °C for 15 min and 30 min in air, respectively. Finally, 100 nm of Al metal was deposited to form the drain and source electrodes. The channel width (W) and length (L) was 700 µm and 70 µm, respectively. The Al metal evaporation was performed using an e-beam evaporator under a high vacuum 10^{-6} Torr. Under the same conditions as the TFTs, MOS test structures consisting of $Al/Al_2O_3/In_2O_3/Al$ were also fabricated on the same substrates.

The electrical characterization (I-V and C-V) of the In_2O_3 TFTs were performed using a Cascade probe station connected to the semiconductor device parameter analyzer (Keysight B1500A) with triaxially shielded probes.

III. Results and Discussion

The transfer (I_d vs. V_g) and output (I_d vs. V_d) characteristics of the TFTs devices consisting of In_2O_3 as the semiconductor channel with anodized Al_2O_3 as the gate dielectrics are shown in Fig. 2. The devices exhibit n-channel behavior, with a very low operating voltage, 3 volts, and the threshold voltage, V_{th} is determined to be 0.6 V, which is much smaller than that of TFTs fabricated with conventional SiO_2 gate dielectric [14]. The operating voltage of the In_2O_3 TFTs with Al_2O_3 make them an ideal choice for integrated circuits (IC) applied to wearables and IoT applications where autonomous power sources would otherwise be depleted by TFTs operating at high voltages.

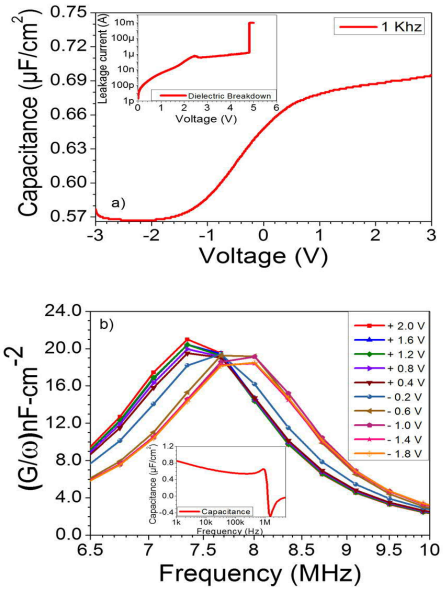

Fig. 3. a) Capacitance voltage characteristics of In_2O_3/Al_2O_3 MOS device measured at 1 KHz frequency. Inset: Breakdown voltage and b) G/ω vs ω characteristics representing conductance at selected bias voltage. Inset: capacitance vs. frequency

The devices exhibit on/off ratio ~10^5 and the electron mobility (µ) was measured as high as 3.53 $cm^2V^{-1}s^{-1}$ in saturation regime calculated using the equation

$$\mu_{(sat)} = \frac{\left(\frac{\partial(\sqrt{I_D})}{\partial V_G}\right)^2}{\frac{1}{2}C_G\frac{W}{L}},$$

where, I_D is the drain current, V_G is the gate voltage, C_G is the gate oxide capacitance, and W/L is the ratio of width to length of the TFT channel.

The 2-terminal MOS (Metal-Oxide-Semiconductor) structure consisting of $Al\text{-}Al_2O_3/In_2O_3/Al$ was used to perform the capacitance voltage analysis, Fig. 3(a), and the leakage current through the dielectric is shown in Fig. 3(a) inset. The Al_2O_3 formed with anodization, exhibits a relatively low leakage current in the operating voltage range of the device i.e. 3V [Fig. 3(a) inset]. The corresponding dielectric constant, κ was found to be 9.3. The TFT transconductance (g_m) gain is as high as 53 µS. Furthermore, the subthreshold swing S was 0.16 V/dec., which is proportional to previous report [15]. This implies there is a lower defect density of states within the gate

oxide. As shown in the Fig. 3(b) inset, the MOS capacitance per unit area was found to be quite constant over the range of frequencies, 1 KHz to 1.3 MHz, between 0.6 - 0.8 μF/cm^2 shows good dielectric properties.

To investigate this further, we have calculated the interface trap density (D_{it}) in the oxide by using the conductance method, sweeping from 1 KHz to 5 MHz [16],

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max}$$

where, G_p is the peak conductance per unit area, $\omega = 2\pi rf$ (f - frequency), and q is the electronic charge. To calculate the interface trap density (D_{it}), (G_p/ω) was plotted as a function of frequency. As shown in Fig. 3(b), as the frequency increases, G_p/ω also increases and reaches its maximum and as expected with an interface trap model, G_p/ω starts to decrease thereafter with further increase in frequency [17].

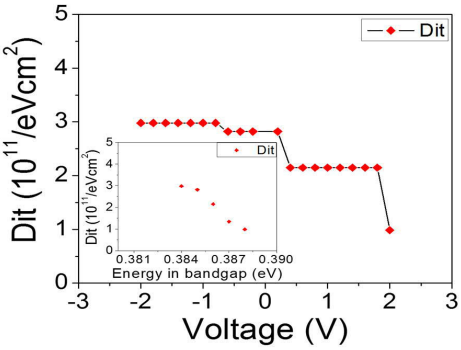

Fig. 4. Trap states density as function of biasing voltage, Inset: Trap states density as a function of energy.

The interface trap density extracted using the measured maximum conductance [18] was about 0.99×10^{11} – 2.98×10^{11} $eV^{-1}\cdot cm^{-2}$. The subsequent relationships among trap state densities with biasing voltage dependence are represented in the Fig. 4, and the trap states correspond to energy in the band gap are presented in the Fig. 4 inset.

Summarized results of In_2O_3 TFT performance parameters are shown in Table 1.

TABLE I
SUMMARIZED In_2O_3 TFT PERFORMANCE PARAMETERS

V_{th} (V)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	Gm (μS)	SS (V/dec)	I_{on}/I_{off}	D_{it} ($eV^{-1}.cm^{-2}$)
0.6	3.5	53	0.16	~10^5	0.986×10^{11}

Furthermore, for the film and dielectric thickness characterization, cross sectional transmission electron microscopy (TEM) analysis of the device was performed. From the cross sectional TEM, the measured thickness of the dielectric layer (Al_2O_3) was found to be 12 nm, shown in Fig 5(a). The material characterization of anodized aluminum oxide (Al_2O_3) film were carried out with the help of atomic force microscopy (AFM), the scanning area was 5 μm^2 and the average roughness of the anodized Al_2O_3 was 1.53 nm, representing smooth film quality, shown in Fig 5(b). Which is partially attributed to the lower density of the trap states. The few anomalous spikes (~160nm) in the AFM image might be due to some dust or foreign particles from transport and storage in room air.

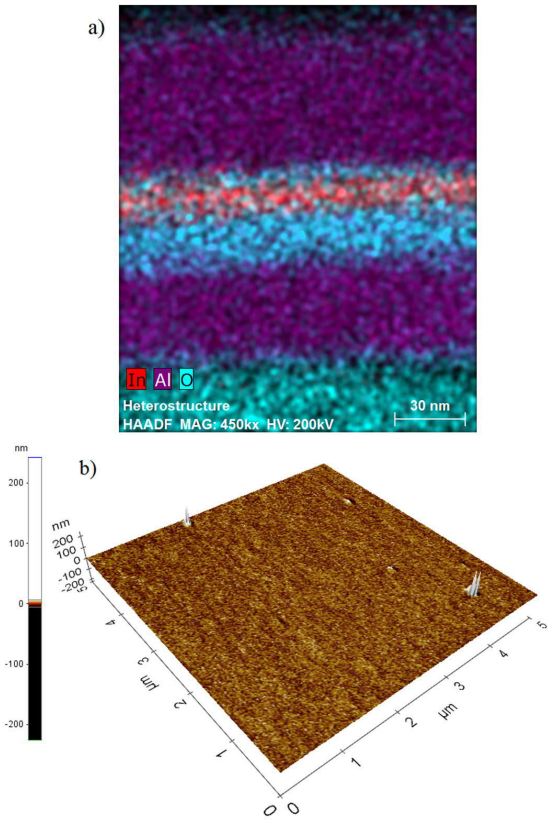

Fig. 5. A) Cross section TEM image of the In_2O_3 TFTs, scale bar 30nm and b) AFM image of the anodized Al_2O_3, average roughness 1.53nm.

IV. CONCLUSION

Thin film transistors (TFTs) based on low-temperature, solution-processable indium oxide (In_2O_3) with a very thin (< 10nm) anodic aluminum oxide (Al_2O_3) as gate dielectric were demonstrated here with very low voltage device operation. The TFTs show very good low voltage performance below 3.0 V and the electron mobility (μ) is as high as 3.53 cm^2/V.s. Furthermore, we also investigated the dielectric properties of the anodic aluminum oxide Al_2O_3 and its estimated interface trap density, D_{it} about 0.99×10^{11} – 2.98×10^{11} $eV^{-1}\cdot cm^{-2}$, suggests a very good compatibility of indium oxide (In_2O_3) with anodic aluminum oxide Al_2O_3. This study shows the low temperature fabrication compatibility for solution-processable metal oxide semiconductors for flexible and printed electronics devices.

ACKNOWLEDGMENT

The authors would like to extend a special thanks to Business Finland (40146/14) and the Academy of Finland (311458) for providing funding.

REFERENCES

[1] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, and G. Tröster, "Metal oxide semiconductor thin-film transistors for flexible electronics", *Appl. Phys. Rev.*, vol. 3, no. 2, pp. 021303(1–53), Feb. 1986. DOI: 10.1063/1.4953034.

[2] E. Fortunato, P. Barquinha, and R. Martins, "Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances", *Adv. Mater.*, vol. 24, no. 12, pp. 2945–2986, May 2012. DOI: 10.1002/adma.201103228.

[3] J. S. Park, W.-J. Maeng, H.-S. Kim, J.-S. Park, "Review of recent developments in amorphous oxide semiconductor thin-film transistor devices", *Thin Solid Films*, vol. 520, no. 6, pp. 1679–1693 Jan 2012. DOI: 10.1016/j.tsf.2011.07.018.

[4] J. E. Medvedeva, D. B. Buchholz, and R. P. H. Chang, "Recent Advances in Understanding the Structure and Properties of Amorphous Oxide Semiconductors", *Adv. Electron. Mater.*, vol. 3, no. 9, pp. 1700082(1–17), Sept. 2017. DOI: 10.1002/aelm.201700082.

[5] M.-G. Kim, M. G. Kanatzidis, A. Facchetti and T. J. Marks, "Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing", *Nature Materials*, vol. 10, pp. 382–388, May 2011. DOI: 10.1038/nmat3011.

[6] R. Hu, Y. Pei, Z. Chen, J. Yang, Y. Li, J. Lin, Y. Zhao, C. Wang, J. Liang, B. Fan, and G. Wang, "Ultra-High Field-Effect Mobility Thin-Film Transistors With Metal–Organic Chemical Vapor Deposition Grown In_2O_3 Channel Treated by Oxygen Microwave Plasma", *IEEE Electron Device Letters*, vol. 36, no. 11, pp. 1163 – 1165, Nov 2015. DOI: 10.1109/LED.2015.2476507.

[7] X. Yu, T. J. Marks and A. Facchetti, "Metal oxides for optoelectronic applications", *Nature Materials*, vol. 15, pp. 383–396, April 2016. DOI: 10.1038/nmat4599.

[8] Dhananjay, S.-S. Cheng, C.-Y. Yang, C.-W. Ou, Y.-C. Chuang, M. C. Wu and C.-W. Chu, "Dependence of channel thickness on the performance of In_2O_3 thin film transistors" *J. Phys. D: Appl. Phys.*, vol. 41, no. 9, pp. 092006(6), April 2008. doi:10.1088/0022-3727/41/9/092006.

[9] C.-M. Kang, H. Kim, Y.-W. Oh, K.-H. Baek, and L.-M. Do, "High–Performance, Solution-Processed Indium-Oxide TFTs Using Rapid Flash Lamp Annealing", *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 595 – 598, May 2016. DOI: 10.1109/LED.2016.2545692.

[10] J.-W. Choi, S.-Y. Han, M.-C. Nguyen, A. H.-T. Nguyen, J. Y. Kim, S. Choi, J. Cheon, H. Ji, and R. Choi, "Low-Temperature Solution-Based In2O3 Channel Formation for Thin-Film Transistors Using a Visible Laser-Assisted Combustion Process", *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1259 – 1262, Sept. 2017. DOI: 10.1109/LED.2017.2734905.

[11] M. Kaltenbrunner, P. Stadler, R. Schwödiauer, A. W. Hassel, N. S. Sariciftci, and S. Bauer, "Anodized Aluminum Oxide Thin Films for Room Temperature Processed, Flexible, Low Voltage Organic Non Volatile Memory Elements with Excellent Charge Retention", *Adv. Mater.*, vol. 23, no. 42, pp. 4892–4896, Sept. 2011. DOI: 10.1002/adma.201103189.

[12] Y. Qin, D. H. Turkenburg, I. Barbu, W. T. T. Smaal, K. Myny, Wan-Yu Lin, G. H. Gelinck, P. Heremans, J. Liu, and E. R. Meinders, "Organic Thin-Film Transistors with Anodized Gate Dielectric Patterned by Self-Aligned Embossing on Flexible Substrates", *Adv. Funct. Mater.*, 2012, vol. 22, no. 6, pp. 1209–1214, Jan 2012. DOI: 10.1002/adfm.201102266.

[13] J. Leppäniemi, O.-H. Huttunen, H. Majumdar, and A. Alastalo, "Flexography-Printed In2O3 Semiconductor Layers for High- Mobility Thin-Film Transistors on Flexible Plastic Substrate", *Adv. Mater.*, vol. 27, no. 44, pp. 7168–7175, Oct. 2015. DOI: 10.1002/adma.201502569.

[14] L. Lan and J. Peng, "High-Performance Indium–Gallium–Zinc Oxide Thin-Film Transistors Based on Anodic Aluminum Oxide", *IEEE Transactions On Electron Devices*, vol. 58, no. 5, pp. 1452 – 1455, May 2011. DOI: 10.1109/TED.2011.2115248.

[15] A. D. Mottram, Pi. Pattanasattayavong, I. Isakov, G. Wyatt-Moon, H. Faber, Y.-H. Lin, and T D. Anthopoulos, "Electron mobility enhancement in solution-processed low-voltage In2O3 transistors via channel interface planarization", *AIP Advances*, vol. 8, no. 6, pp. 065015 (8), June 2018. DOI:10.1063/1.5036809.

[16] Dieter K. Schroder, "Semiconductor Material and Device Characterization", 3rd ed., Wiley-IEEE Press, 2015, pp. 347–349. DOI:10.1002/0471749095.

[17] S. Kundu, S. K. Roy and P Banerji, "GaAs metal–oxide–semiconductor–device with titanium dioxide as dielectric layer: effect of oxide thickness on the device performance", *J. Phys. D: Appl. Phys.*, vol. 44, no. 15, pp. 155104 (6), April (2011). DOI:10.1088/0022-3727/44/15/155104.

[18] G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, "Capacitance–Voltage Characterization of GaAs–Oxide Interfaces", *Journal of The Electrochemical Society*, vol. 155, no. 12, pp. H945–H950 Oct. 2008. DOI: 10.1149/1.2988045.

PUBLICATION
II

2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton

Sagar R. Bhalerao, Donald Lupo and Paul R. Berger

IEEE International Flexible Electronics Technology Conference (IFETC), Aug. 2019
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2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton

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Abstract— **Semiconductor devices based upon silicon have powered the modern electronics revolution through advanced manufacturing processes. However, the requirement of high temperatures to create crystalline silicon devices has restricted its use in a number of new applications, such as printed and flexible electronics. Thus, developments with high mobility solution-processable metal oxides, surpassing α-Si in many instances, is opening a new era for flexible and wearable electronics. However, high operating voltages and relatively high deposition temperatures required for metal oxides remain impediments for the flexible devices. Here, the fabrication of low operating voltage, flexible thin film transistors (TFT) using a solution processed indium oxide (In_2O_3) channel material with room temperature deposited anodized high-κ aluminum oxide (Al_2O_3) for gate dielectrics are reported. The flexible TFTs operates at low voltage V_{ds} of 2 V, with threshold voltage V_{th} 0.42 V, on/off ratio 10^3 and subthreshold swing (SS) 420 mV/dec. The electron mobility (μ), extracted from the saturation regime, is 2.85 cm^2/V.s and transconductance, gm, is 38 μS.**

I. Introduction

Metal oxide semiconductors have gained significant attention during the past couple decades owing to their superior optoelectronics properties, such as wide band gap, charge transport mechanism, and thin film deposition techniques allowing for a new paradigm in electronics devices [1-2]. Amorphous metal oxide semiconductors have been widely studied for numerous opto-electronic, sensing and medical applications. Among all metal oxide semiconductors, indium oxide (In_2O_3) is a very promising candidate for the thin film transistor due to its attractive electrical performance [3-4]. However, despite significant progress, the goal of low-cost – low temperature deposition of metal oxides still faces major challenges. As most of the required device fabrication process steps use high temperature deposition techniques, especially for the gate oxide deposition, such as vacuum-based thin film deposition, metal oxide TFTs on flexible substrates remains elusive [5]. Thus, efforts have been taken to develop a low temperature, low-cost solution processable deposition process for metal oxide TFTs [6]. And even though, some progress has been made towards flexible TFTs, major challenges remain in terms of high operating voltage.

Herein, the fabrication of low operating voltage flexible thin film transistors has been reported. The TFTs were fabricated on flexible Kapton substrates using a solution processed indium oxide (In_2O_3) semiconductor as the TFT channel material with room temperature anodized high-κ aluminum oxide (Al_2O_3) gate dielectric [7-9].

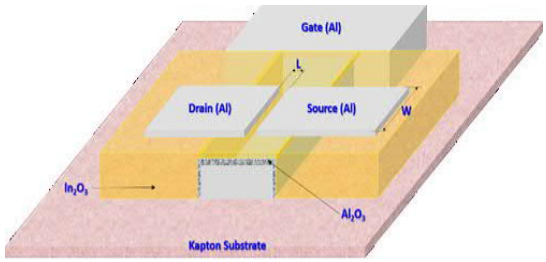

Fig. 1. Schematic structure of the In_2O_3 TFT with Al_2O_3 gate dielectric.

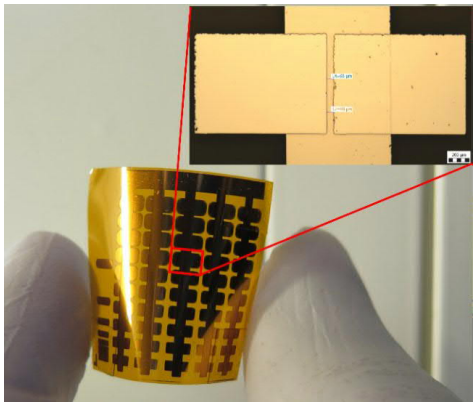

Fig. 2. Photograph of the In_2O_3 TFT fabricated on the flexible Kapton substrate, Inset: Optical image of In_2O_3 TFT with 70 μm gate length. Scale bar 200 μm.

II. Experimental

The schematic representation of the flexible TFTs is shown in Fig. 1. The TFTs, were fabricated on the flexible Kapton substrate with the use of bottom gate top contact (BGTC) topology, following a previous approach used by the authors atop glass that resulted in ultra-low threshold voltages [9].

Photograph of the In_2O_3 TFTs fabricated on the flexible Kapton substrate and optical image with 70 µm gate length is shown in Fig. 2 and Inset, respectively. Scale bar 200 µm.The Kapton substrates were thoroughly cleaned before the device fabrication, using acetone, isopropanol (IPA) and deionized water (DI) for 30 minutes successively. The top gate contact was formed by depositing the 100 nm aluminium (Al) using a patterned shadow mask. Subsequently, the anodization process has been performed to convert top 10 nm layer of the gate contact into the aluminium oxide, i.e. the high-κ gate dielectric. The substrates were cleaned thereafter several times with deionized water to purge any residual ions. Next followed was the indium oxide, In_2O_3, deposition by spin coating a precursor film and annealing in air at 90 °C for 15 min. and 300 °C for 30 min. for conversion. Prior to spin coating, the indium oxide (In_2O_3) ink was prepared by dissolving Indium (III) nitrate hydrate $In(NO_3)_3 \cdot xH_2O$ in anhydrous 2-methoxyethanol 99.8% in 0.2 M concentration [9], and stirring for 12 hours at 75 °C. All precursors used as-is without any further distillation and were purchased from Sigma-Aldrich. After the spin coating, the drain and source contacts of 100 nm thick aluminium (Al) was deposited using a shadow mask. The aluminium (Al) metal deposition was carried out under a high vacuum 10^{-6} Torr, using an e-beam evaporator. Furthermore, to perform the capacitance voltage (CV) analysis, on the same substrates and the under same conditions, MOS (Metal-Oxide-Semiconductor) test device comprised of $Al/Al_2O_3/In_2O_3/Al$ were also fabricated.

The electrical performance (I-V and C-V) of the flexible In_2O_3 TFTs was carried out with the aid of a Cascade probe station connected to a Keysight B1500A semiconductor device parameter analyzer with triaxially shielded probes.

III. Results and Discussion

The output (I_d vs. V_d) and transfer (I_d vs. V_g) characteristics of the fabricated flexible TFTs using the In_2O_3 semiconductor channel material and anodized Al_2O_3 gate dielectrics are shown in Fig. 3 and 4, respectively. The flexible TFTs operates at very low-voltage, i.e. 2 volts with a very low threshold voltage, V_{th}, 0.42 V, significantly smaller than previously reported metal oxide TFTs on flexible substrates [10].

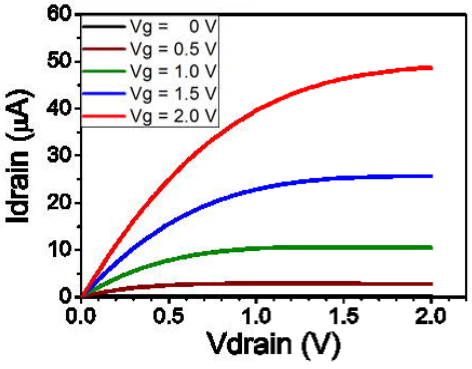

Fig. 3. Output characteristics for In_2O_3 TFTs with 70µm gate length.

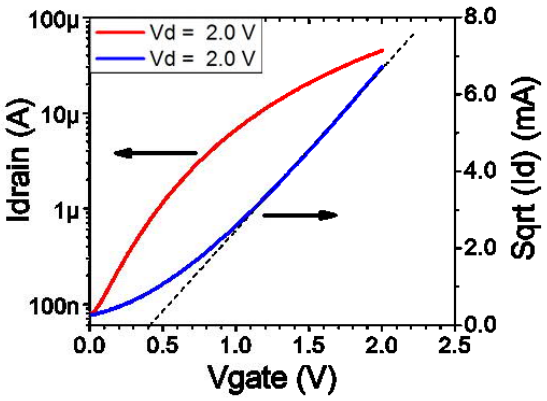

Fig. 4. Transfer characteristics of In_2O_3 TFTs with 70µm gate.

The electron mobility (µ) in the saturation regime was found to be 2.85 $cm^2V^{-1}s^{-1}$, calculated using the equation

$$\mu_{(sat)} = \frac{\left(\frac{\partial(\sqrt{I_D})}{\partial V_G}\right)^2}{\frac{1}{2}C_G\frac{W}{L}},$$

where, I_D is the drain current, V_G is the gate voltage, C_G is the gate oxide capacitance, and W/L is the ratio of width to length of the TFT channel.

Furthermore, the on/off ratio was up to ~10^3. The TFT transconductance (g_m) gain was as high as 38 µS and the subthreshold swing, SS, extracted was 0.42 V/dec.

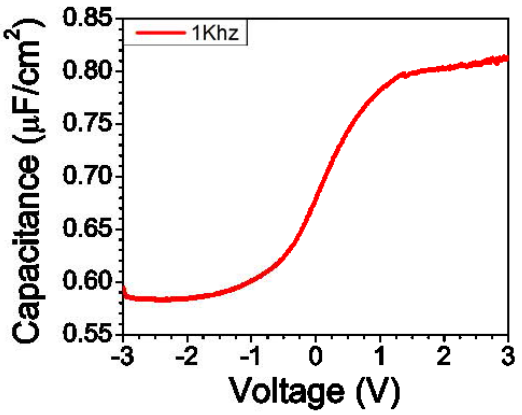

Fig. 5. Capacitance voltage characteristics of In_2O_3/Al_2O_3 MOS device measured at 1 KHz frequency.

The gate oxide thickness was found to be ~8nm and was calculated from the MOS capacitance voltage analysis as shown in Fig. 5. Our previous report [9] confirmed with transmission electron microscopy the close agreement the physical thickness with extracted electrical thickness. The

dielectric constant, κ was found to be 9.3, as calculated using parallel plate capacitance equation, $C = \kappa\varepsilon_0 A/d$ [11]. The gate dielectric formed with the anodization exhibits quite low leakage current, i.e. below 1.5 V as shown in Fig. 6, and demonstrates the good dielectric properties of anodized aluminium oxide.

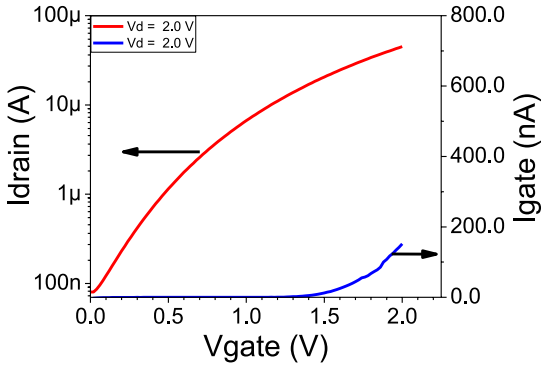

Fig. 6. Transfer characteristics of In_2O_3 TFTs showing gate leakage current with 70µm gate.

Table 1. Shows the combined results of electrical performance of the flexible indium oxide (In_2O_3) thin film transistors.

TABLE I
SUMMARIZED In_2O_3 TFT PERFORMANCE PARAMETERS

V_{th} (V)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	g_m (µS)	SS (V/dec)	I_{on}/I_{off}
0.42	2.85	38	0.42	~10^3

IV. CONCLUSIONS

Thin film transistors (TFTs) using a solution-processable indium oxide (In_2O_3) were fabricated on flexible Kapton substrates. The very thin ~8nm high- κ aluminum oxide (Al_2O_3) gate dielectric was deposited with the help of a room temperature anodization process, enabling low voltage operating devices. The flexible TFTs demonstrates very good low voltage performance at 2.0 V and the electron mobility (µ) is as high as 2.85 cm^2/V.s. In this study, we have successfully demonstrated low voltage TFTs by uniting low temperature solution processable In_2O_3 with room temperature anodized high-κ aluminum oxide Al_2O_3 gate dielectrics.

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REFERENCES

[1] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, and G. Tröster, "Metal oxide semiconductor thin-film transistors for flexible electronics", Appl. Phys. Rev., vol. 3, no. 2, pp. 021303(1–53), Feb. 1986. DOI: 10.1063/1.4953034.

[2] E. Comini, C. Baratto, G. Faglia, M. Ferroni, A. Vomiero, G. Sberveglieri, "Quasi-one dimensional metal oxide semiconductors: Preparation, characterization and application as chemical sensors", Progress in Materials Science, vol 54, pp. 1–67, June 2009. DOI:10.1016/j.pmatsci.2008.06.003

[3] Brian G. Lewis and David C. Paine, "Applications and Processing of Transparent Conducting Oxides", MRS 2000, vol. 25, issue 8 (Transparent Conducting Oxides), pp. 22-27, August 2000. DOI: https://doi.org/10.1557/mrs2000.147

[4] J. E. Medvedeva, D. B. Buchholz, and R. P. H. Chang, "Recent Advances in Understanding the Structure and Properties of Amorphous Oxide Semiconductors", Adv. Electron. Mater., vol. 3, no. 9, pp. 1700082(1–17), Sept. 2017. DOI: 10.1002/aelm.201700082.

[5] X. Yu, T. J. Marks and A. Facchetti, "Metal oxides for optoelectronic applications", Nature Materials, vol. 15, pp. 383–396, April 2016. DOI: 10.1038/nmat4599.

[6] J.-W. Choi, S.-Y. Han, M.-C. Nguyen, A. H.-T. Nguyen, J. Y. Kim, S. Choi, J. Cheon, H. Ji, and R. Choi, "Low-Temperature Solution-Based In2O3 Channel Formation for Thin-Film Transistors Using a Visible Laser-Assisted Combustion Process", IEEE Electron Device Letters, vol. 38, no. 9, pp. 1259 – 1262, Sept. 2017. DOI: 10.1109/LED.2017.2734905.

[7] M. Kaltenbrunner, P. Stadler, R. Schwödiauer, A. W. Hassel, N. S. Sariciftci, and S. Bauer, "Anodized Aluminum Oxide Thin Films for Room Temperature Processed, Flexible, Low Voltage Organic Non Volatile Memory Elements with Excellent Charge Retention", Adv. Mater., vol. 23, no. 42, pp. 4892–4896, Sept. 2011. DOI: 10.1002/adma.201103189.

[8] Y. Qin, D. H. Turkenburg, I. Barbu, W. T. T. Smaal, K. Myny, Wan-Yu Lin, G. H. Gelinck, P. Heremans, J. Liu, and E. R. Meinders, "Organic Thin-Film Transistors with Anodized Gate Dielectric Patterned by Self-Aligned Embossing on Flexible Substrates", Adv. Funct. Mater., 2012, vol. 22, no. 6, pp. 1209–1214, Jan 2012. DOI: 10.1002/adfm.201102266.

[9] Sagar R. Bhalerao, Donald Lupo, Amirali Zangiabadi, Ioannis Kymissis, Jaakko Leppaniemi, Ari Alastalo and Paul R. Berger, "0.6V Threshold Voltage Thin Film Transistors with Solution Processable Indium Oxide (In_2O_3) Channel and anodized high-κ Al2O3 Dielectric", IEEE Electron Device Letters, May 2019. DOI: 10.1109/LED.2019.2918492

[10] P. Heremans, N. Papadopoulos, A. de Jamblinne de Meux, M. Nag, S. Steudel, M. Rockelé, G. Gelinck, A. Tripathi, J. Genoe, K. Myny, "Flexible metal-oxide thin film transistor circuits for RFID and health patches", IEEE International Electron Devices Meeting (IEDM), vol. 16, pp. 151 – 154, DOI: 10.1109/IEDM.2016.7838360.

[11] T. T. Grove, M. F. Masters, and R. E. Miers, "Determining dielectric constants using a parallel plate capacitor", American Journal of Physics 73, 52, 2005. DOI: 10.1119/1.1794757.

PUBLICATION III

Flexible, Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors (TFT) and Circuits for Internet-of-Things (IoT)

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Flexible, solution-processed, indium oxide (In_2O_3) thin film transistors (TFT) and circuits for internet-of-things (IoT)

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ABSTRACT

Over the last decade, novel approaches to explore low voltage flexible devices and low power flexible circuits are being widely researched by the scientific community. To realize the true potential of energy thrifty Internet-of-Things (IoT) objects, low power circuits and hence their low-voltage operating devices are a paramount pre-requisite, especially when their power is constrained by autonomous energy scavenging. At present, through advanced manufacturing processes, silicon-based semiconductor devices are powering the modern electronics industry. However, processing temperatures are inhibiting them from flexible and printed electronics, as well as being too costly for scalability to the trillions of IoT objects anticipated. Therefore, development of solution-processed metal oxide semiconductors creates huge opportunities for IoT and wearables. Here, flexible solution-processed indium oxide (In_2O_3) thin film transistors (TFT) and inverter circuits with low operating voltage are reported. The operating voltage of the TFTs is $\leq$ 3 V with threshold voltage (V_{th}) 0.82 V, on/off ratio 10^5 and extracted mobility (μ) in saturation regime is 14.5 $cm^2/V{\cdot}s$. The gain of the inverter at V_{DD} 1, 2 and 3 V was determined to be 10, 22 and 32 respectively. Furthermore, measured transconductance (g_m) and sub-threshold swing (S) are found to be 140 μS and 0.22 V/dec, respectively.

1. Introduction

Metal oxide semiconductors have gained enormous interest in the design of modern electronics, particularly thin film transistors (TFT), due to their excellent electrical, optical, chemical and mechanical properties. With increasing demand for both high performance and low-voltage operation for low-power consumption, TFTs have been continuously scaled down to their physical limits [1–3]. On the other hand, to achieve low-voltage, high performance TFTs, high-κ dielectrics have been extensively explored for the replacement of silicon oxide. Similarly, tremendous efforts have been devoted to develop solution-processed metal oxide semiconductors for the active channel materials within thin film transistors [4,5]. Additionally, vacuum deposition processes are less scalable to roll-to-roll processing and can concurrently require high processing temperatures [6,7]. Despite dedicated efforts by the research community and industry, there is still only a handful of reports available showing low voltage operating devices with reliable device performance at relatively low temperature processing for semiconductor and high-κ gate dielectric deposition compatible to flexible electronics and Internet-of-Things [8–10]. Moreover, apart from the devices, circuits based on solution processed metal oxide have been given relatively little attention, resulting in a limited number of circuit publications [11–13].

Here, we report the enhanced device performance of flexible thin film transistors (TFTs) based on solution processed indium oxide and comprehensive device bendability study along with SPICE simulations. Furthermore, by utilizing the Transfer Length Measurement (TLM) technique, the contact resistance analysis was provided. In addition to the flexible TFTs, a thorough analysis of a low voltage operating inverter circuit fabricated on a flexible Kapton substrate was also presented.

Solution-processed indium oxide was used as an active semiconductor channel material, which was further combined with a room temperature anodization route to form a thin high-κ aluminum oxide (Al_2O_3) gate dielectric. The room temperature deposition of anodized aluminum oxide carried out as reported previously [14,15], which empowers lower voltage operation i.e. $\leq$ 3V. The flexible indium oxide TFTs were fabricated by following the bottom gate top contact (BGTC) approach. The schematic representation of the device structure of flexible indium oxide TFTs is shown in Fig. 1(a). Fig. 1(b) illustrates the proposed inverter circuit diagram. A photograph of inverter circuits

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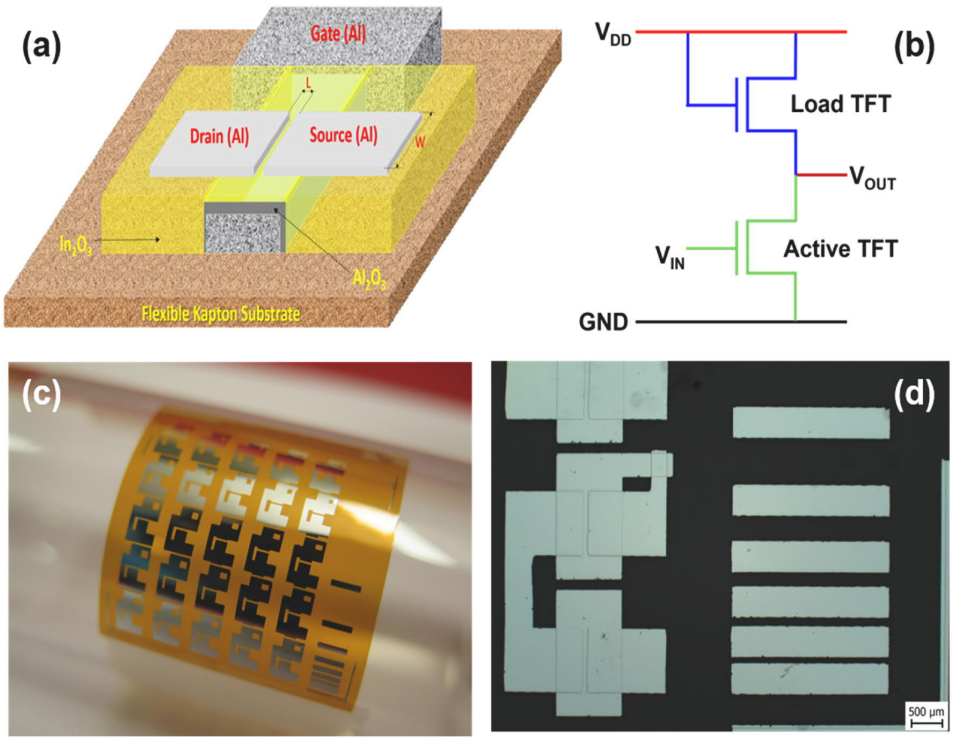

Fig. 1. a) Schematic structure of the In_2O_3 TFT with Al_2O_3 gate dielectric (for illustrative purposes – not on scale). b) Schematic of the proposed inverter circuit. c) A photograph of the fabricated flexible In_2O_3 inverter circuit on a Kapton substrate. and d) Optical micrograph of flexible inverter along with TLM (transfer length measurement) test structure. Scale bar 500 µm.

fabricated on flexible Kapton (Polyimide) is exhibited in Fig. 1(c) and the optical micrograph presented in Fig. 1(d). Additionally, the Transfer Length Measurement (TLM) [16–18] test structure was also fabricated on the same flexible Kapton substrate to investigate the contact resistance along with the electrical performance of the flexible indium oxide TFTs and Inverter circuit.

2. Experimental

As shown in the schematic diagram Fig. 1(a), TFTs were fabricated on a flexible Kapton substrate. Before the fabrication process, the Kapton substrates were thoroughly cleaned with acetone, IPA, and deionized water with subsequent ultrasonication for 30 min. To start with, 100 nm aluminum metal was deposited using a patterned metal shadow mask. Then, anodization process was carried out to form the aluminum oxide gate dielectric. As a result, the top surface of evaporated aluminum metal was transformed into an aluminium oxide (Al_2O_3). The thickness of the subsequent aluminium oxide layer was found to 12 nm thick, which is validated by electron microscopy in our previous report [19]. Following the anodization procedure, the Kapton substrates were rigorously rinsed with deionized water and dried by nitrogen jet to eliminate any residual surface ion impurities from the anodization.

Before applying the active semiconductor channel, a 0.2 M indium oxide solution (ink) was prepared by dissolving Indium (III) nitrate hydrate $In(NO_3)_3{\cdot}xH_2O$ in anhydrous 2-methoxyethanol 99.8%. This prepared solution was further heated at 75 °C for 12 h under continuous stirring prior to spin coating. Subsequently, the indium oxide ink was spun onto the substrate and annealed at 90 °C followed by 300 °C for 15 min and 30 min, respectively, in the air [19]. Finally, again by using a patterned metal shadow mask to form the drain and source contact, 100 nm of Aluminum metal was deposited, forming 1 mm channel width (w) and 80 µm channel length. The same mask also included Transfer Length Measurement (TLM) test patterns to correlate ohmic contact resistance (Fig. 1 (c) and (d)) through varying channel lengths. An e-beam evaporator was used for the aluminum metal deposition, which was performed under a high vacuum 4×10^{-6} Torr. The electrical characterization of the flexible indium oxide TFTs and inverter circuit was performed using a Cascade probe station attached to triaxial shielded probes connected to a Keysight B1500A semiconductor device parameter analyzer.

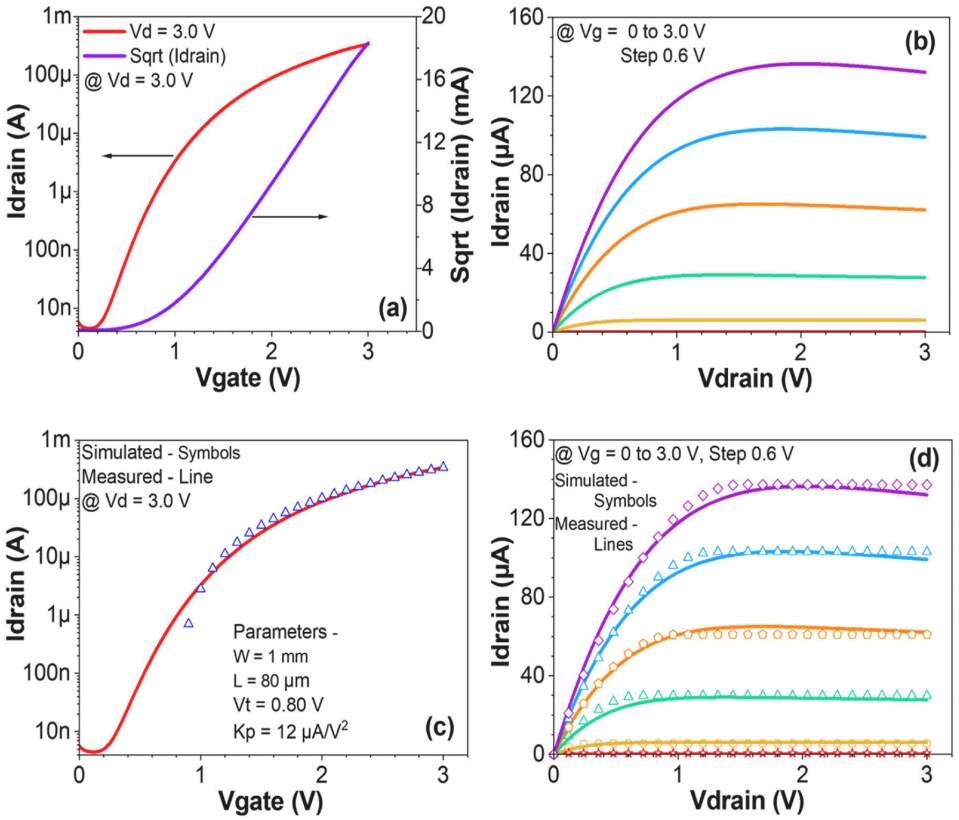

Fig. 2. a) Measured transfer characteristics of flexible In_2O_3 TFTs. b) Measured output characteristics of In_2O_3 TFTs, c) Fitting of a simulation data with a measured transfer characteristic of flexible In_2O_3 TFTs and d) Fitting of a simulation data with a measured output characteristic of flexible In_2O_3 TFTs.

Table 1
Summarized Flexible Indium Oxide TFT performance parameters.

Threshold Voltage (V_{th}) V	Mobility (μ_{sat}) $cm^2V^{-1}s^{-1}$	Transconductance (g_m) µS	Subthreshold swing (S) V/dec
0.82	14.5	140	0.22 V/dec

3. Results and discussion

The measured electrical performance of the flexible indium oxide TFT is shown in Fig. 2 - illustrating transfer characteristics in Fig. 2 (a) and output characteristics in Fig. 2 (b) respectively. Fig. 2 (c) and (d) shows the fitting of the SPICE simulation results superimposed with measured TFTs electrical performance.

The measured and simulated data fitting closely follow one another. The device simulations were performed using the analog devices LTspice software, with physical and measured device parameters, W = 1 mm, L = 80 µm, V_t = 0.82 V and K_p = 12 µA/V^2, which is calculated from equation (1),

$$K_p = \left(\frac{\sqrt{2.I_{d1}} - \sqrt{2.I_{d2}}}{V_{g1} - V_{g2}}\right)^2 \quad (1)$$

where, I_{d1} and I_{d2} are the drain currents at gate voltages V_{g1} and V_{g2}, respectively.

The electrical performance of the flexible TFT conclusively demonstrates low-voltage operation, i.e., functioning at less than 3 V, as well as a significantly lower threshold voltage (V_{th}) is 0.82 V. The flexible TFT exhibited relatively high on/off ratio, 10^5, and the best extracted mobility (µ) was found to be as high as 14.5 cm^2/V·s in saturation regime, which is much higher than previously reported solution-processed, low temperature indium oxide TFTs [20–23]. The electron mobility was calculated using equation (2),

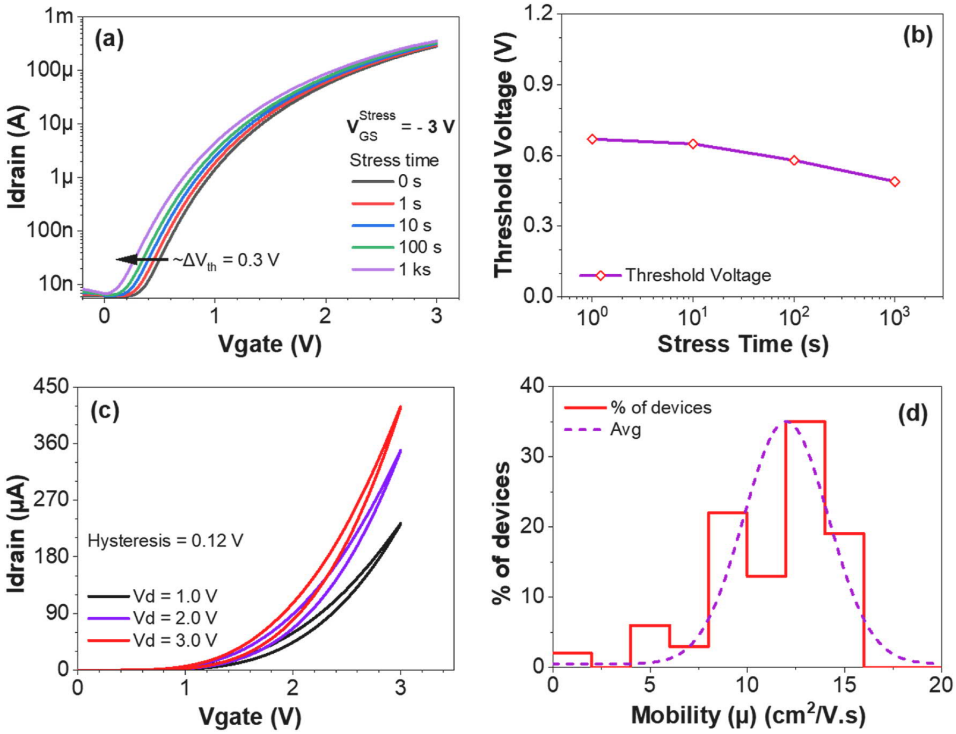

Fig. 3. a) Variation of transfer characteristics (I_d vs. V_g) of In_2O_3 TFTs measured as a function of gate bias stress time, at negative gate bias stress (NBS) of – 3 V, b) Bias stress-induced threshold voltage shift as a function of stress time. During bias stress, a constant gate-source voltage of −3 V was applied, c) Transfer characteristics (I_d vs. V_g) of In_2O_3 TFTs representing negligible hysteresis, and d) The mobility histogram indicating device reliability and yield.

$$\mu_{(sat)} = \frac{\left(\frac{\partial\left(\sqrt{I_D}\right)}{\partial V_G}\right)^2}{\frac{1}{2}C_G\frac{W}{L}} \quad (2)$$

where, I_D is the drain current, V_G is the gate voltage, C_G is the gate oxide capacitance, and W/L is the ratio of width to length of the TFT channel.

From the electrical measurements shown in Fig. 2 (a), the transconductance and subthreshold swing (S) values were also calculated and found to be 140 μS and 0.225 V/dec, respectively. From the Transfer Length Measurement (TLM) shown in Fig. 1 (d), the specific contact resistance (ρ_c) between the metal oxide semiconductor and the metal contacts, i.e. in this case indium oxide and aluminium electrodes, was also measured and was determined to be ~ 0.98 kΩ cm^2. Table 1, summarizes the electrical performance parameters of flexible thin film transistors (TFTs) based on solution processed indium oxide (In_2O_3).

To further investigate device potency, the stability of indium oxide (In_2O_3) TFTs was investigated under bias stress and hysteresis (double scan). Fig. 3 (a) illustrations the transfer characteristics (I_d vs. V_g) of indium oxide TFTs measured at various gate bias stress intervals. Under bias stress, the device performs excellently; nevertheless, a slight shift (negative) in threshold voltage around $\Delta V_{th} = 0.3$ V has been observed, as seen in Fig. 3 (b). It's very likely that this is attributable to joule heating. Furthermore, the indium oxide TFTs' dual-scan transfer characteristics, as shown in Fig. 3 (c), exhibit hysteresis values as low as 0.12 V. Fig. 3 (d) depicts a statistical analysis of the electrical performance of the measured devices as a histogram of saturation mobility versus devices proportion and average, demonstrating that approximately 70% of devices exhibit mobility in the 10–14 cm^2/V·s range, implying excellent device reliability and yield.

We have also studied the bending performance of the indium oxide TFTs with bending radius ranging from 3.5 cm to 5 mm. The specimens were bent around rods of known diameters and measured in the probe station while bent. The variation in mobility as a function of curvature bending is shown in Fig. 4 (a). From the measurements, it was found that there was a slight change in mobility values, ranging from 14.5 to 13.2, over the measurements of bending curvature with radius 3.5 cm to 5 mm. The results are a strong affirmation of the bending stability of this TFT platform technology for wearables [24,25]. The slight change in mobility observed might be attributed from the device handling and/or differences in probing the devices after each bending modification.

Additionally, the electrical performance of the flexible inverter

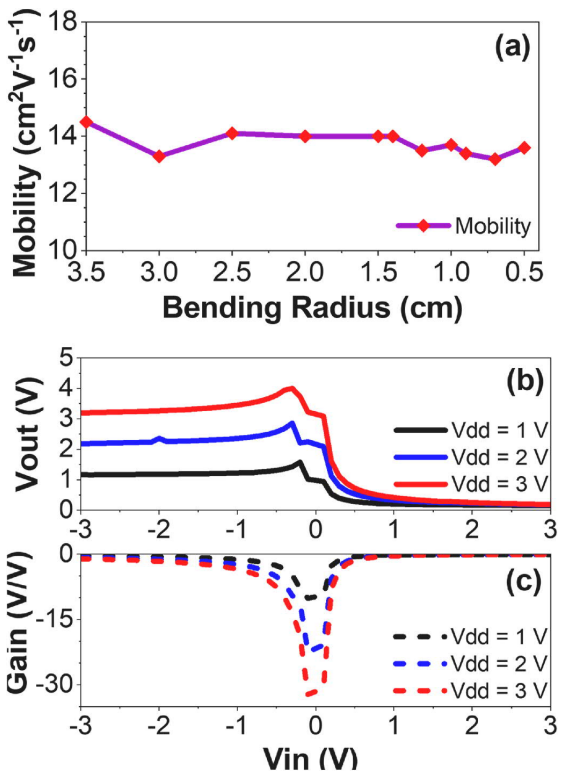

Fig. 4. a) Bending performance of the indium oxide TFTs, b) Voltage transfer characteristics of the flexible solution processed indium oxide inverter at different bias voltage and c) The gain of the flexible inverter circuit.

circuit fabricated based on the solution-processed indium oxide TFTs was also investigated. The voltage transfer characteristics of the indium oxide TFT based inverter circuit (shown in Fig. 1 (b)) at changing supply voltage (V_{DD}) are represented in Fig. 4 (b). From the electrical measurements shown in Fig. 4 (c), the gain of the inverter at V_{DD} was measured in 1 V increments equal to 1, 2 and 3 V and was found to be 10, 22 and 32 respectively.

4. Conclusion

In this work, we successfully demonstrated low voltage, flexible TFTs and inverter circuits based on solution processed indium oxide on the flexible Kapton substrates along with device simulation results. The room temperature anodized high-κ gate dielectric i.e., aluminum oxide enabled the lower device operating voltage below 3 V. The flexible indium oxide TFTs showed excellent electrical performance with electron mobility (μ) as high as 14.5 cm^2/V.s which is significantly higher in terms of state-of-the-art solution-processed, low temperature and low-voltage operating devices. Along with the electrical characteristics, bending performance of the flexible TFTs and inverter circuit also shows stable device performance. The inverter circuit also shows good operating performance over a full scale of input voltage and relatively high gain as high as 32. Therefore, herein not only the device, but also the inverter circuit on a flexible substrate (Kapton Polyimide) has been successfully investigated. Therefore, to envision the true potential of the energy thrifty Internet-of-Things (IoT), low power circuits and hence the low voltage wearables. This study presents, an alternative to the silicon-based semiconductor devices and subsequently, a way forward for flexible, printed electronics and the Internet-of-Things (IoT).

CRediT authorship contribution statement

Sagar R. Bhalerao: Conceptualization, Methodology, Formal analysis, Investigation, Data curation, Writing – original draft, Visualization, Writing – review & editing. **Donald Lupo:** Conceptualization, Resources, Writing – review & editing, Supervision, Project administration, Funding acquisition. **Paul R. Berger:** Conceptualization, Resources, Writing – review & editing, Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] X. Yu, T.J. Marks, A. Facchetti, Metal oxides for optoelectronic applications, Nat. Mater. 15 (2016) 383–396, https://doi.org/10.1038/nmat4599.
[2] A.D. Franklin, Nanomaterials in transistors: from high-performance to thin-film applications, Science 349 (2015) 6249, https://doi.org/10.1126/science.aab2750.
[3] B. Bayraktaroglu, K. Leedy, R. Neidhard, Microwave ZnO thin-film transistors, IEEE Electron. Device Lett. 29 (2008) 9, https://doi.org/10.1109/LED.2008.2001635.
[4] E. Fortunato, P. Barquinha, R. Martins, Oxide semiconductor thin-film transistors: a review of recent advances, Adv. Mater. 24 (2012) 2945–2986, https://doi.org/10.1002/adma.201103228.
[5] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors, Nature 432 (2004) 488–492, https://doi.org/10.1038/nature03090.
[6] Sangeon Jeon, Jaewan Cho, Sung Min Cho, Photolithography-free fabrication of a-IGZO thin film transistor with interconnecting metal lines, Mater. Sci. Semicond. Process. 121 (2021), 105417, https://doi.org/10.1016/j.mssp.2020.105417.
[7] N. Tiwari, A. Nirmal, M.R. Kulkarni, R.A. John, N. Mathews, Enabling high performance n-type metal oxide semiconductors at low temperatures for thin film transistors, Inorg. Chem. Front. 7 (2020) 1822–1844, https://doi.org/10.1039/d0qi00038h.
[8] J.W. Park, B.H. Kang, H.J. Kim, A review of low-temperature solution-processed metal oxide thin-film transistors for flexible electronics, Adv. Funct. Mater. 30 (2020), 1904632, https://doi.org/10.1002/adfm.201904632.
[9] M.T. Ghoneim, M.M. Hussain, Review on physically flexible nonvolatile memory for Internet of everything electronics, Electronics 4 (2015) 424–479, https://doi.org/10.3390/electronics4030424.
[10] M.R. Shijeesh, A.C. Saritha, M.K. Jayaraj, Investigations on the reasons for degradation of zinc tin oxide thin film transistor on exposure to air, Mater. Sci. Semicond. Process. 74 (2018) 116–121, https://doi.org/10.1016/j.mssp.2017.10.015.
[11] S.R. Bhalerao, D. Lupo, P.R. Berger, 2-volt solution-processed, indium oxide (In_2O_3) thin film transistors on flexible Kapton, IEEE Int. Flexible Electr. Technol. Confer. IFETC (2019) 1–3, https://doi.org/10.1109/IFETC46817.2019.9073721.
[12] K.K. Banger, Y. Yamashita, K. Mori, R.L. Peterson, T. Leedham, J. Rickard, H. Sirringhaus, Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol–gel on chip' process, Nat. Mater. 10 (2011) 45–50, https://doi.org/10.1038/nmat2914.
[13] H. Sirringhaus, T. Kawase, R.H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E. P. Woo, High-resolution inkjet printing of all-polymer transistor circuits, Science 290 (2000) 2123–2126, https://doi.org/10.1126/science.290.5499.2123.
[14] M. Kaltenbrunner, P. Stadler, R. Schwödiauer, A.W. Hassel, N.S. Sariciftci, S. Bauer, Anodized aluminum oxide thin films for room temperature processed, flexible, low voltage organic non volatile memory elements with excellent charge retention, Adv. Mater. 23 (2011) 4892–4896, https://doi.org/10.1002/adma.201103189.
[15] S.R. Bhalerao, D. Lupo, P.R. Berger, Flexible, gallium oxide (Ga_2O_3) thin film transistors (TFTs) and circuits for the Internet of things (IoT), in: IEEE International Flexible Electronics Technology Conference – IFETC, 2021, pp. 32–34, https://doi.org/10.1109/IFETC49530.2021.9580524.
[16] K.-C. Huang, D.B. Janes, K.J. Webb, M.R. Melloch, A transfer length model for contact resistance of two-layer systems with arbitrary interlayer coupling under the

contacts, IEEE Trans. Electron. Dev. 43 (1996) 676–684, https://doi.org/10.1109/16.491242.

[17] L.W. Guo, W. Lu, B.R. Bennett, J.B. Boos, J.A.d. Alamo, Ultralow resistance ohmic contacts for p-channel InGaSb field-effect transistors, IEEE Electron. Device Lett. 36 (2015) 546–548, https://doi.org/10.1109/LED.2015.2421337.

[18] N. Stavitski, M.J.H. van Dal, A. Lauwers, C. Vrancken, A.Y. Kovalgin, R.A. M. Wolters, Systematic TLM measurements of NiSi and PtSi specific contact resistance to n- and p-type Si in a broad doping range, IEEE Electron. Device Lett. 29 (2008) 378–381, https://doi.org/10.1109/LED.2008.917934.

[19] S.R. Bhalerao, Donald Lupo, Amirali Zangiabadi, Ioannis Kymissis, Jaakko Leppaniemi, Ari Alastalo, Paul R. Berger, 0.6V threshold voltage thin film transistors with solution processable indium oxide (In_2O_3) channel and anodized high-κ Al_2O_3 dielectric, IEEE Electron. Device Lett. 40 (2019) 1112–1115, https://doi.org/10.1109/LED.2019.2918492.

[20] I. Abdullah1, J.E. Macdonald, Y.-H. Lin, T. D Anthopoulos, N.H. Salahr, S.A. Kakil, F. F Muhammadsharif, Bias stability of solution-processed In_2O_3 thin film transistors, J. Phys. Mater. 4 (2021), 015003, https://doi.org/10.1088/2515-7639/abc608.

[21] Y. Zhou, J. Li, Y. Yang, Q. Chen, J. Zhang, Artificial synapse emulated through fully aqueous solution processed low-voltage In_2O_3 thin-film transistor with Gd_2O_3 solid electrolyte, ACS Appl. Mater. Interfaces 12 (2020) 980–988, https://doi.org/10.1021/acsami.9b14456.

[22] D. Khim, Y.-H. Lin, T.D. Anthopoulos, Impact of layer configuration and doping on electron transport and bias stability in heterojunction and superlattice metal oxide transistors, Adv. Funct. Mater. 29 (2019), 1902591, https://doi.org/10.1002/adfm.201902591.

[23] B.S. Kim, H.J. Kim, Influence of annealing on solution-processed indium oxide thin-film transistors under ambient air and wet conditions, IEEE Trans. Electron. Dev. 63 (2016) 3558–3561, https://doi.org/10.1109/TED.2016.2591622.

[24] S.R. Bhalerao, D. Lupo, P.R. Berger, Flexible thin film transistor (TFT) and circuits for Internet of things (IoT) based on solution processed indium gallium zinc oxide (IGZO), in: IEEE International Flexible Electronics Technology Conference – IFETC, 2021, pp. 23–25, https://doi.org/10.1109/IFETC49530.2021.9580506.

[25] P.R. Berger, M. Li, R.M. Mattei, M.A. Niang, N. Talisa, M. Tripepi, B. Harris, S. R. Bhalerao, E.A. Chowdhury, C.H. Winter, D. Lupo, Advancements in Solution Processable Devices Using Metal Oxides for Printed Internet-Of-Things Objects, Electron Devices Technology and Manufacturing Conference, EDTM), 2019, pp. 160–162, https://doi.org/10.1109/EDTM.2019.8731322.

PUBLICATION
IV

Flexible, Gallium Oxide (Ga_2O_3) Thin Film Transistors (TFTs) and Circuits for the Internet of Things (IoT)

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Flexible, Gallium Oxide (Ga_2O_3) Thin Film Transistors (TFTs) and Circuits for the Internet of Things (IoT)

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Abstract— **Even though present advanced silicon-based devices and technology could be reaching their zenith of performance levels, still there are many orthogonal applications, which are yet far from their reach. Also, due to their high process temperatures, there are still a number of applications that are out-of-reach for silicon, namely direct integration into flexible and printed electronics, as opposed to a hybrid integration of adding a prefabricated integrated circuit. These can find usage in low-cost and disposable wearable medical technologies. Therefore, the low temperature-solution processed oxide semiconductors that are complimentary to the performance of silicon are prerequisite for the forthcoming printed, flexible and wearable electronics revolution. Here, solution processed, flexible gallium oxide (Ga_2O_3) thin film transistors (TFT) and inverter circuit are reported. The high-κ aluminium oxide (Al_2O_3) for the gate dielectric, was deposited with the help of a room temperature anodization process. The gallium oxide TFTs show high performance, with extracted electron mobility (μ) 2.74 $cm^2/V{\cdot}s$, operating voltage as low as 3V and threshold voltage (Vth) 0.61 V. The on/off ratio 10^4 and subthreshold swing (SS) 0.5 V/dec, Hysteresis 0.1 V and transconductance, gm, is 64.8 μS.**

I. Introduction

Over the last half century, semiconductor devices and circuits based on silicon CMOS technology have dominated the electronic industries. So, in the search for higher scaling performance, we have almost reached to the atomic limit of scaling for silicon ICs, which pose major performance challenges. Therefore, in the hunt for new high-performance materials, a number of wide bandgap compound semiconductors are being aggressively explored where applications push the power density higher than silicon can withstand, including higher currents and powers [1]. These binary semiconductors, such as GaAs, SiC, and GaN, and their alloys, are quite promising for power switching and high frequency radio. However, these wide bandgap materials still face some technical limitations [2], such as lack of suitable large area native substrates, with suitable lattice matching. This directed our attention towards solution processed transparent conducting oxide semiconductors atop flexible substrates, bypassing lattice mismatch altogether [3, 4].

Devices based on gallium oxide (Ga_2O_3), indium oxide (In_2O_3) and Indium-gallium-zinc-oxide (IGZO) have shown great potential to revolutionize these new semiconductor applications [3-4]. From all of them, in recent years, gallium oxide has gained greatest attention due to its exceptional and attractive material properties, like wide bandgap (4.8 eV) and high sheet carrier density. Even though the devices with gallium oxide showed significant progress, almost all present state-of-the-art devices are based on expensive, high temperature and/or high vacuum techniques [5, 6], such as PLD (pulsed laser deposition), HVPE (halide vapor phase epitaxy), MBE (molecular beam epitaxy), MOVPE (metalorganic vapor phase epitaxy), etc.

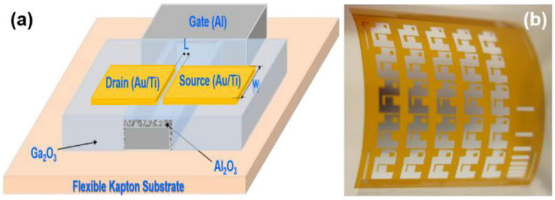

Fig. 1. a) Schematic representation of the flexible Ga_2O_3 TFT with Al_2O_3 gate dielectric (for illustrative purposes – not on scale). b) Photograph of the fabricated flexible Ga_2O_3 Inverter circuit on a Kapton substrate.

Here, in this paper, we report the low-temperature, solution-processed, flexible thin film transistors (TFTs) and inverter circuit based on gallium oxide (Ga_2O_3). Along with a room temperature deposited high-κ gate dielectric, aluminium oxide (Al_2O_3) using an anodization process. Both the process, solution processing and anodization have their own advantages, such as economical, low processing temperature, scalability [7, 8].

II. Experimental

The candidate TFTs and inverter circuit were fabricated on flexible Kapton substrates using a bottom gate top contact (BGTC) topology as illustrated in Fig. 1 (a). The photograph of the final fabricated flexible gallium oxide inverter circuit is shown in Fig. 1 (b). Before starting the device fabrication, the Kapton substrates were pre-cleaned with acetone, isopropanol (IPA) and deionized water (DI) with 15 min sonication each, respectively. The gate electrode was formed with e-beam evaporated 100 nm aluminium and metal shadow mask. To form the high-κ gate dielectric, an anodization process was performed on the gate electrode to convert the top surface, ~12 nm, into aluminium oxide (Al_2O_3) as evidenced previously through cross-sectional transmission electron microscopy [9]. Next followed the gallium oxide (Ga_2O_3) deposition by spin coating an in-precursor form and annealing the film for 1 hour

in air at 300 °C. Finally, the drain source electrode was formed using successive e-beam deposition of 10 nm Titanium (Ti) and 100 nm Gold (Au) and metal shadow mask. Both, the gate, and drain-source electrode deposition were performed under a high vacuum, 10^{-6} Torr.

Beforehand, the gallium oxide (Ga_2O_3) ink was prepared by dissolving Gallium (III) nitrate hydrate $Ga(NO_3)_3 \cdot xH_2O$ in deionized water (DI) in 0.1 M concentration. The solution was stirred for 12 hours at 75 °C. Gallium (III) nitrate hydrate $Ga(NO_3)_3 \cdot xH_2O$ was purchased from Sigma-Aldrich and used as-is without any further distillation. Furthermore, the metal oxide semiconductor (MOS) test structure ($Al/Al_2O_3/Ga_2O_3/Al$) was also fabricated on the same flexible Kapton substrate, following the same fabrication process for the gate oxide analysis.

The electrical performance of the flexible gallium oxide thin film transistors (TFTs) as well as inverter circuit were measured using a Keysight B 1500A semiconductor device parameter analyser connected through tri-axially shielded probes to a Cascade probe station.

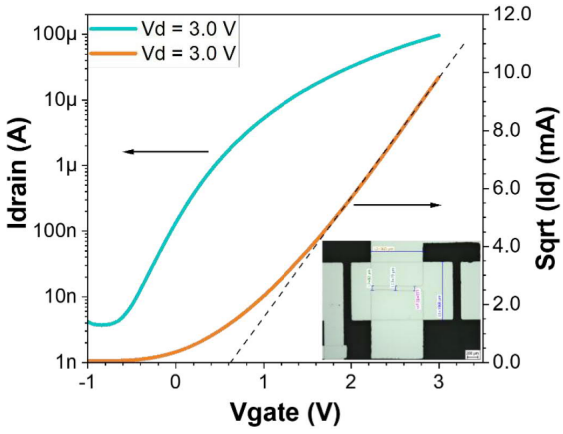

Fig. 2. Transfer characteristics of flexible Ga_2O_3 TFTs. Inset: Optical micrograph of flexible Ga_2O_3 TFT. Scale bar 200 µm.

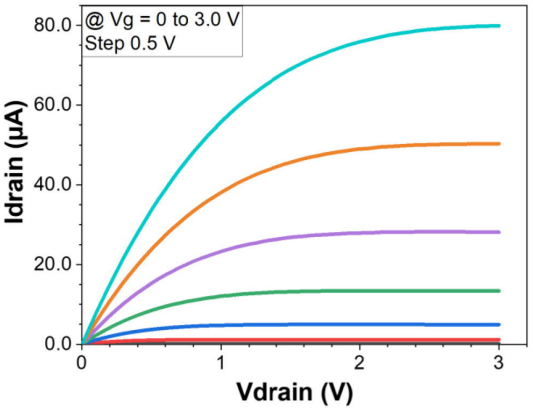

Fig. 3. Output characteristics of flexible Ga_2O_3 TFTs.

III. Results and Discussion

The fabricated flexible TFTs based on Ga_2O_3 as semiconductor channel and Al_2O_3 gate dielectric reveal good electrical performance with source-drain operating voltages as low as 3V. The transfer (I_d vs. V_g) and output (I_d vs. V_d) characteristics of the gallium oxide TFTs are represented in the Fig. 2 and Fig. 3, respectively. Fig. 4, represents the gate leakage current versus applied bias voltage. The Al_2O_3 formed with anodization, exhibits relatively low leakage current in the device operating voltage range as i.e., 3 V. The flexible TFTs demonstrated a quite low threshold voltage, V_{th}, as low as 0.61 V, with good On/Off ratio 10^4 and reasonably low hysteresis 0.1 V, which is shown in Fig. 5.

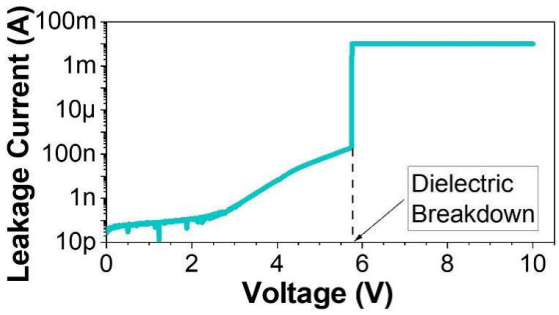

Fig. 4. Leakage current along with gate dielectric breakdown.

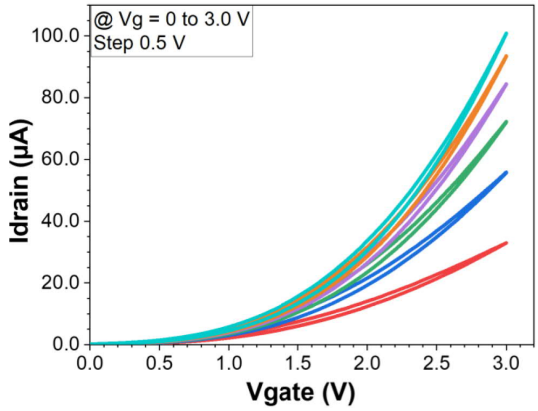

Fig. 5. Transfer characteristics of flexible Ga_2O_3 TFTs showing negligible hysteresis.

The extracted electron mobility (µ) was found as high as 2.74 $cm^2/V \cdot s$, which is very promising with respect to solution processed gallium oxide at comparatively low processing temperatures. The electron mobility in the saturation region was calculated using the equation

$$\mu_{(sat)} = \frac{\left(\frac{\partial(\sqrt{I_D})}{\partial V_G}\right)^2}{\frac{1}{2} C_G \frac{W}{L}},$$

where, I_D is the drain current, V_G is the gate voltage, C_G is the gate oxide capacitance, and W/L is the ratio of width to length of the TFT channel.

The gate oxide thickness was estimated from the measured MOS capacitance and was found to be ~12 nm, which was further confirmed by cross sectional transmission electron microscopy in our previous report [9]. The TFT transconductance (gm) gain is as high as 64.8 µS. Furthermore, the subthreshold swing S was only 0.5 V/dec, which is comparatively low.

The flexible gallium oxide TFTs' bending performance has also been studied. To bend the devices around, rods with known radii, ranging from 3.5 cm to 5 mm, were utilized. Fig. 6 depicts the change in mobility as a function of curvature bending. The slight variation in mobility values was observed, ranging from 2.5 to 2.7, across the measures of bending curvature from 3.5 cm to 5 mm. Which represent excellent bending stability of the TFTs.

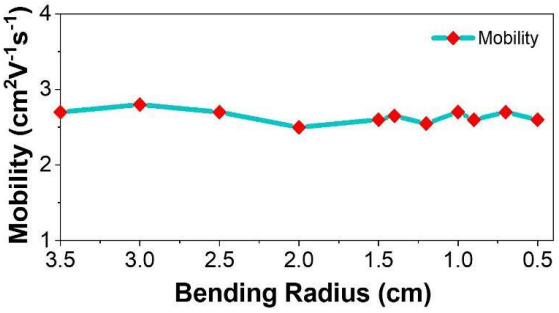

Fig. 6. Bending performance of the gallium oxide based flexible TFTs.

In addition, the electrical performance of a flexible inverter circuit built with gallium oxide TFTs was also investigated. The output voltage and the gain of the inverter circuit with respect to input voltage at different supply voltage (V_{DD}) are represented in Fig 7 (a) and (b). The measured gain of the inverter circuit was found to be 9, 19 and 30 at V_{DD} equal to 1, 2 and 3 V, respectively.

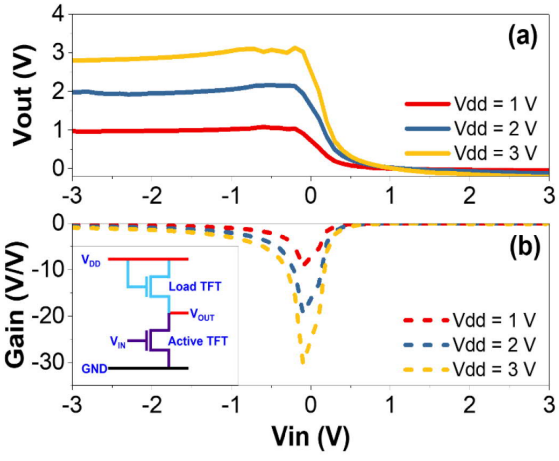

Fig. 7. (a) the output voltage and (b) the gain of the gallium oxide based flexible inverter circuit with respect to input voltage at different supply voltage.

Table I. shows summarised results of combined electrical performance parameters of the flexible gallium oxide (Ga_2O_3) thin film transistors (TFTs).

TABLE I
SUMMARIZED Ga_2O_3 TFT PERFORMANCE PARAMETERS

Threshold voltage, V_{th} (V)	Mobility μ_{sat} ($cm^2V^{-1}s^{-1}$)	Transconductance g_m (µS)	Subthreshold swing, SS (V/dec)
0.61	2.74	64.8	0.5

IV. CONCLUSIONS

Low temperature, solution processed gallium oxide (Ga_2O_3) thin film transistors (TFT) and inverter circuit were fabricated on flexible Kapton substrate. Along with the electrical characterization, the bending performance of the flexible gallium oxide TFTs was also presented. The anodization process was used to create a very thin high-κ aluminum oxide (Al_2O_3) for gate dielectric and the thickness was found to be ~12 nm. The thinner gate oxide enables the device operating voltage below the 3V with quite low threshold voltage (V_{th}) 0.61 V. The electron mobility for the solution process gallium oxide thin film transistor was 2.74 $cm^2/V{\cdot}s$, which is quite encouraging for solution processed low temperature devices. Therefore, this new solution processed gallium oxide deposition approach could be a pioneering pathway for the future printed and flexible wearable electronics devices.

REFERENCES

[1] X. Yu, T. J. Marks and A. Facchetti, "Metal oxides for optoelectronic applications", Nature Materials, vol. 15, pp. 383–396, April 2016. DOI:10.1038/nmat4599.

[2] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances", Adv. Mater., vol. 24, no.22, pp. 2945–2986, Jun. 2012. DOI: 10.1002/adma.201103228.

[3] Sagar R. Bhalerao, Donald Lupo and Paul R. Berger, "2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton", IEEE International Flexible Electronics Technology Conference (IFETC), Aug. 2019. DOI: 10.1109/IFETC46817.2019.9073721

[4] Paul R. Berger, Miao Li, Ryan M. Mattei, Maimouna A. Niang, Noah Talisa, Michael Tripepi, Brandon Harris, Sagar R. Bhalerao, Enam A. Chowdhury, Charles H. Winter, and Donald Lupo, "Advancements in Solution Processable Devices using Metal Oxides For Printed Internet-of-Things Objects", Electron Devices Technology and Manufacturing Conference (EDTM), 2019. DOI: 10.1109/EDTM.2019.8731322

[5] M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui and S. Yamakoshi, "Recent progress in Ga_2O_3 power devices," Semicond. Sci. Technol. 31, 034001 (11pp), Jan 2016.

[6] S. I. Stepanov, V. I. Nikolaev, V. E. Bougrov and A. E. Romanov, "Gallium Oxide: Properties and Applications – A Review," Rev. Adv. Mater. Sci. 44, pp. 63-86, 2016.

[7] M. Kaltenbrunner, P. Stadler, R. Schwödiauer, A. W. Hassel, N. S. Sariciftci, and S. Bauer, "Anodized Aluminum Oxide Thin Films for Room Temperature Processed, Flexible, Low Voltage Organic Non-Volatile Memory Elements with Excellent Charge Retention", *Adv. Mater.*, vol. 23, no. 42, pp. 4892–4896, Sept. 2011.

[8] Y. Qin, D. H. Turkenburg, I. Barbu, W. T. T. Smaal, K. Myny, Wan-Yu Lin, G. H. Gelinck, P. Heremans, J. Liu, and E. R. Meinders, "Organic Thin-Film Transistors with Anodized Gate Dielectric Patterned by Self-Aligned Embossing on Flexible Substrates", *Adv. Funct. Mater.* 2012. vol. 22, no. 6, pp. 1209–1214, Jan 2012.

[9] Sagar R. Bhalerao, Donald Lupo, Amirali Zangiabadi, Ioannis Kymissis, Jaakko Leppaniemi, Ari Alastalo and Paul R. Berger, "0.6V Threshold Voltage Thin Film Transistors with Solution Processable Indium Oxide (In_2O_3) Channel and anodized high-κ Al_2O_3 Dielectric", IEEE Electron Device Letters, May 2019. DOI: 10.1109/LED.2019.2918492

PUBLICATION V

Flexible Thin Film Transistor (TFT) and Circuits for Internet of Things (IoT) based on Solution Processed Indium Gallium Zinc Oxide (IGZO)

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Abstract— **Solution-processed metal oxide semiconductors are being extensively studied as a channel material for active semiconductor transistors. Among all metal oxide semiconductors, indium-gallium-zinc-oxide (IGZO) gained considerable attention for thin film transistors (TFTs) due to its promising electrical properties. Although metal oxide TFTs fabricated with vacuum deposition techniques enjoy the advantage of higher mobility in comparison with solution processing, vacuum deposition techniques are very costly due to expensive equipment, restricting its usage for emerging modern technologies, such as printed and flexible electronics. On the other hand, solution-processed metal oxide devices have an added advantage such as low cost, and compatible for flexible substrates. Therefore, developments of solution processed metal oxide TFTs on flexible substrates could open a new era of flexible and wearable electronics. Herein, we report the fabrication of flexible thin film transistors (TFT) and inverter circuit using solution-processed indium-gallium-zinc-oxide (IGZO) as a channel material by uniting with room temperature deposited anodized high-κ aluminium oxide (Al_2O_3) for gate dielectrics. The flexible TFTs operates at low voltage V_{ds} of 4 V, with threshold voltage V_{th} 1.05 V along with hysteresis as low as 0.4 V. The extracted electron mobility (μ) at saturation regime, is 4.77 $cm^2/V{\cdot}s$. The transconductance, gm, is 90.8 μS, subthreshold swing (SS) 357 mV/dec and on/off ratio 10^5.**

I. Introduction

Recently, amorphous metal oxide semiconductors have been largely used for many sensing applications and electronic circuits. TFTs based on solution-processed metal oxides have received much attention due to the advantages of low cost and scalable processing compared to high temperature and/or high vacuum, vapor deposition techniques. With increased demand for flexible, wearable and ultra-thin electronics, extensive effort has been made to develop the high performance solution-processed thin film transistors (TFT) and circuits for potential applications, such as Internet-of-Things (IoT) and radio frequency identification tags (RFID) [1]. To address the energy requirements of current electronic applications, such as self-powered internet of things (IoT), internet-of-everything (IoE), or medical wearables, devices must be more energy efficient. Flexible TFTs based on solution-processed metal oxide semiconductors might thus be viewed as potential candidate for the expensive and complex high vacuum, high temperature deposition techniques [2-4].

Indium gallium zinc oxide (IGZO) is arguably the most favoured and extensively investigated among all metal oxide semiconductors owing to its exceptional opto-electronic characteristics, like low temperature processing, high mobility, uniformity, and transmittance. [5-7]. Despite the fact that thin film transistors based on the indium gallium zinc oxide (IGZO) semiconductor have been reported in the past, the higher device operating voltage, high temperature deposition, and vacuum processing remain significant barriers to its application in flexible and wearable electronics [8].

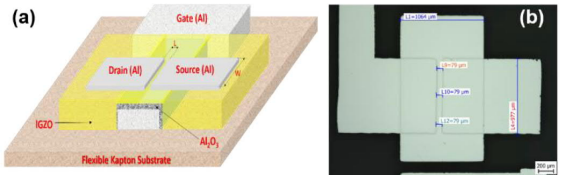

Fig. 1. a) Schematic representation of the flexible IGZO TFT with Al_2O_3 gate dielectric (for illustrative purposes – not on scale). b) Optical micrograph of flexible IGZO TFT. Scale bar 200 μm.

Here, we report low voltage (4.0 V) operating flexible thin film transistor (TFT) and inverter circuit with solution processed low temperature deposited indium gallium zinc oxide (IGZO) semiconductor film along with room temperature deposited anodized aluminium oxide Al_2O_3 as a high-κ gate dielectric. The schematic representation of the flexible TFTs is shown in Fig. 1 (a). We lowered the device operating voltage below 4 volts by uniting device fabrication with ultra-thin (10 nm) room temperature deposited anodic Al_2O_3 gate oxide with relatively low temperature, i.e., 300 °C annealed IGZO film.

II. Experimental

As shown in Fig. 1(a), flexible Kapton was used as a substrate to fabricate the flexible TFTs and inverter circuit using the bottom gate, top contact topology. Fig. 1(b), illustrates the optical micrograph of the fabricated flexible IGZO TFTs. To fabricate the flexible TFTs, the Kapton substrates were successively sonicated 30 minutes each in, acetone, isopropanol (IPA) and deionized water (DI) and carefully dried with air gun. The substrates were then mounted with a patterned metal shadow mask and transferred to the e-beam evaporator to form

gate electrodes by depositing 100 nm Aluminium (Al). The anodization process has been performed on deposited aluminium and shown to convert the top ~10 nm surface of it into an aluminium oxide dielectric [9]. The substrates were then rinsed several times with deionized water (DI). Subsequently, indium gallium zinc oxide (IGZO) was deposited by using spin coating of an IGZO precursor ink and annealing at 90°C for 15 min and 300°C for 30 min, both in air. The indium gallium zinc oxide (IGZO) ink was formed by dissolving indium nitrate hydrate ($In(NO_3)_3.xH_2O$), gallium nitrate hydrate ($Ga(NO_3)_3.xH_2O$), and zinc nitrate hydrate ($Zn(NO_3)_3.xH_2O$) in 2-methoxyethanol in a proportion of 0.085 : 0.0125 : 0.0275 M respectively [10].

Finally, using a metal shadow mask, the drain and source electrodes was formed by depositing 100 nm thick aluminium (Al) with e-beam evaporation. The aluminium (Al) metal deposition was performed under a high vacuum 10^{-6} Torr. The electrical performance of the fabricated flexible IGZO TFTs and inverter circuit was measured using a Keysight B1500A semiconductor device parameter analyser connected to a Cascade Microtech probe station via tri-axial shielded cables.

III. Results and Discussion

The electrical performance i.e., transfer (I_d vs V_g) characteristics and output (I_d vs V_d) characteristics of the fabricated flexible TFTs based on solution processed indium gallium zinc oxide (IGZO) as an active channel material and room temperature anodized Al_2O_3 high-κ gate dielectric are shown in Figs. 2 and 3, respectively.

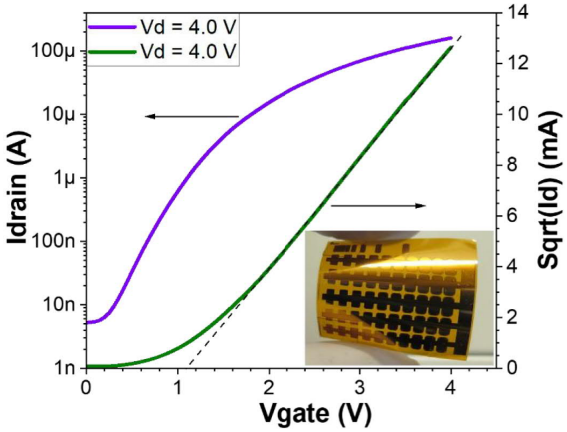

Fig. 2. Transfer characteristics of flexible IGZO TFTs and Inset: Photograph of the fabricated flexible IGZO TFT on a Kapton substrate.

The extracted electron mobility (μ) in the saturation regime was found to be 4.77 $cm^2V^{-1}s^{-1}$, calculated using the equation

$$\mu_{(sat)} = \frac{\left(\frac{\partial(\sqrt{I_D})}{\partial V_G}\right)^2}{\frac{1}{2}C_G\frac{W}{L}},$$

where, I_D is the drain current, V_G is the gate voltage, C_G is the gate oxide capacitance, and W/L is the ratio of width to length of the TFT channel.

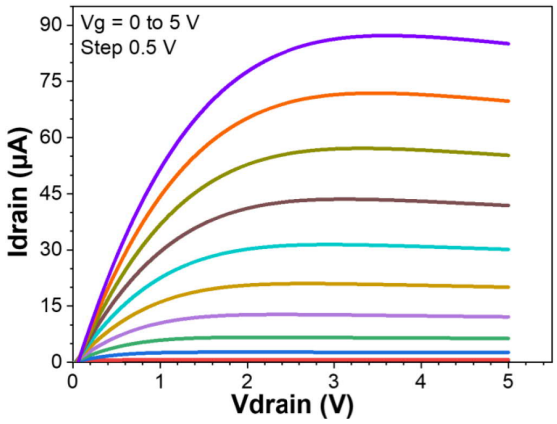

Fig. 3. Output characteristics of flexible IGZO TFTs.

The flexible IGZO TFTs shows a low-voltage performance, at 4 Volts with a threshold voltage, V_{th}, 1.05 Volts and On/Off ratio is 10^5. The measured transconductance (g_m) gain is 90.8 μS and the subthreshold swing, SS, is 0.357 V/dec. Fig. 4, represents the hysteresis, which is as low as 0.4 V.

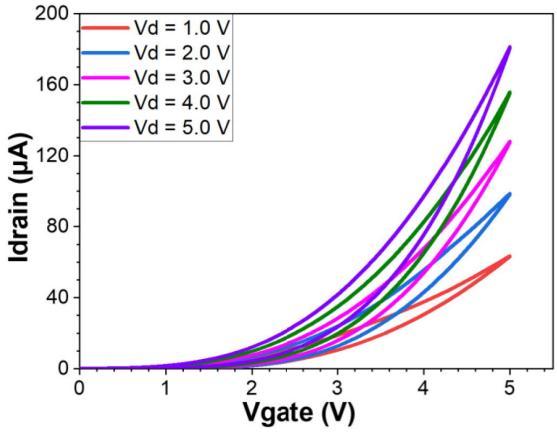

Fig. 4. Transfer characteristics of IGZO TFTs showing hysteresis.

The leakage through the dielectric is shown Fig. 5, showing a dielectric breakdown voltage at 5.5 Volts, corresponds to the electric field 4.5 × 10^6 V/cm and very low leakage current at device operating voltages, i.e., less than 10 nA below 4 V, verifying good quality gate dielectric.

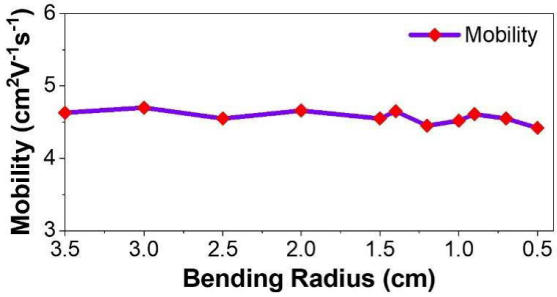

Fig. 5. Leakage current along with gate dielectric breakdown.

The TFTs were bent around rods with radii ranging from 5 mm to 3.5 cm to test their flexibility. The resulting change in mobility as a function of curvature bending is shown in Fig. 6, presenting quite constant mobility over a measured bending range, with minimal reduction (i.e., < 0.35). Furthermore, Fig. 7 (a) and (b), shows the electrical characterization, i.e., output and gain with respect to the input voltage, of two TFT based flexible inverter circuit. With a supply voltage (V_{DD}) at equal to 1, 2, 3, and 4 V, inverter circuit's measured gain was 9, 17, 24, and 33, respectively.

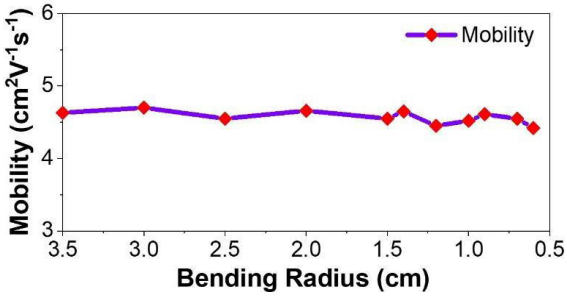

Fig. 6. Bending performance of the flexible IGZO TFTs.

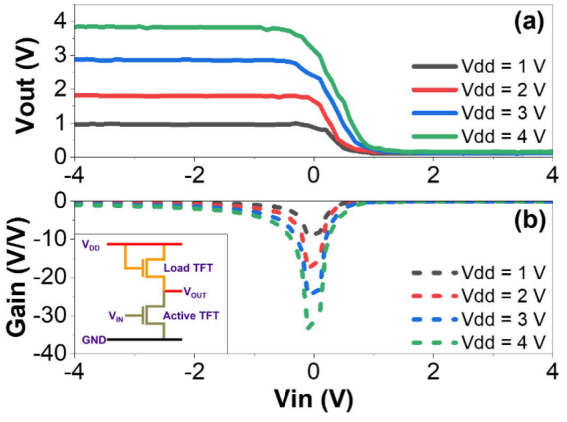

Fig. 7. (a) The output voltage and (b) the gain of the IGZO based flexible inverter circuit. Inset: Two transistor inverter circuit.

The combined electrical performance parameters of the flexible indium gallium zinc oxide (IGZO) thin film transistors (TFTs) are summarised in Table 1.

TABLE I
SUMMARIZED FLEXIBLE IGZO TFT PERFORMANCE PARAMETERS

Threshold voltage, V_{th} (V)	**Mobility μ_{sat} ($cm^2V^{-1}s^{-1}$)**	**Transconductance g_m (μS)**	**Subthreshold swing, SS (V/dec)**
1.05	4.77	90.82	0.35 V/dec

Therefore, all the measured parameters and electrical performance of the flexible indium gallium zinc oxide (IGZO) TFTs, relative to their evaporated counterparts, are very good, and with outstanding overall device performance in comparison with the recent reports on solution processed IGZO TFTs. We believe that the present study offers a new route for low voltage operating flexible TFTs based on solution-processed metal oxide semiconductor and dielectric films through anodized room temperature aluminium oxide focused towards flexible and/or wearable electronics, especially with energy scavenging internet of things (IoT).

IV. CONCLUSIONS

Flexible thin film transistors (TFTs) and inverter circuit based on solution-processable indium gallium zinc oxide (IGZO) were fabricated on flexible Kapton substrates. The very thin ~10nm high- κ aluminum oxide (Al_2O_3) gate dielectric was deposited with the help of a room temperature anodization process, enabling low voltage operating devices. The flexible TFTs have quite good electrical performance with low voltage 4.0 V and the electron mobility (μ) is as high as 4.77 $cm^2/V{\cdot}s$. The bending performance of flexible IGZO TFTs was also presented. In this study, by uniting low temperature solution processable IGZO with room temperature processed anodized aluminum oxide Al_2O_3 high-κ gate dielectric, we successfully demonstrated low voltage operating flexible TFTs. Therefore, flexible low voltage solution processed metal oxide TFTs are promising candidate that not only may replace the conventional semiconductor technology in some applications but also opens new era of wide range of applications.

REFERENCES

[1] Street, R. A. Thin-Film Transistors. Adv. Mater. 2009, 21, 2007– 2022.

[2] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard and H. Sirringhaus, Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol–gel on chip' process, Nature Materials, vol. 10, Jan 2011.

[3] S. R. Bhalerao, D. Lupo and P. R. Berger, "2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton", IEEE International Flexible Electronics Technology Conference (IFETC), Aug. 2019. DOI: 10.1109/IFETC46817.2019.9073721

[4] P. R. Berger, M. Li, R. M. Mattei, M. A. Niang, N. Talisa, M. Tripepi, B. Harris, S. R. Bhalerao, E. A. Chowdhury, C. H. Winter, and D. Lupo, "Advancements in Solution Processable Devices using Metal Oxides For Printed Internet-of-Things Objects", Electron Devices Technology and Manufacturing Conference (EDTM), 2019. DOI: 10.1109/EDTM.2019.8731322

[5] Fortunato, E.; Barquinha, P.; Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. Adv. Mater. 2012, 24, 2945–2986.

[6] W. Xu, L. Hu, C. Zhao, L. Zhang, D. Zhu, P. Cao, W. Liu, S. Han, X. Liu, F. Jia, Y. Zeng, Y. Lu, Low temperature solution-processed IGZO thin-film transistors, Applied Surface Science, vol. 455, 15 Oct. 2018, pp 554-560.

[7] M. Miyakawa, M. Nakata, H. Tsuji and Y. Fujisaki, Highly stable low-temperature aqueous solution-processed oxide thin-film transistors by the hydrogen injection and oxidation method, Flexible and Printed Electronics, vol. 3, No. 2, 2018.

[8] X Xiao, L Zhang, Y Shao, X Zhou, H He and S Zhang, Room-Temperature-Processed Flexible Amorphous InGaZnO Thin Film Transistor, ACS Appl. Mater. Interfaces 2018, 10, 31, 25850-25857.

[9] S. R. Bhalerao, D Lupo, A Zangiabadi, I Kymissis, J Leppäniemi, A Alastalo and P R Berger, 0.6 V threshold voltage Thin film transistors with solution processable (In_2O_3) channel and anodized high-κ al_2O_3 dielectric, IEEE electron device letters, vol. 40, no. 7, july 2019. DOI: 10.1109/LED.2019.2918492

[10] J-W Jo, K-T Kim, H-H Park and S K Park, High-Speed and Low-Temperature Atmospheric Photo-Annealing of Large-Area Solution-Processed IGZO Thin-Film Transistors by Using Programmable Pulsed Operation of Xenon Flash Lamp, Journal of the Korean Physical Society, Vol. 74, No. 11, June 2019, pp. 1052~1058.