Stability and Performance Analysis of Grid-Connected Inverter Based on Online Measurements of Current Controller Loop

1st Henrik Alenius
Faculty of Information Technology and Communication Sciences
Tampere University
Tampere, Finland
henrik.alenius@tuni.fi

2nd Matias Berg
Faculty of Information Technology and Communication Sciences
Tampere University
Tampere, Finland
matias.berg@tuni.fi

3rd Roni Luhtala
Faculty of Engineering and Natural Sciences
Tampere University
Tampere, Finland
roni.luhtala@tuni.fi

4th Tomi Roinila
Faculty of Engineering and Natural Sciences
Tampere University
Tampere, Finland
tomi.roinila@tuni.fi

***Abstract*—The amount of grid-connected three-phased inverters is increasing rapidly. In a weak grid, the non-ideal grid impedance decreases the control performance and can even compromise the system stability through load effect. The stability assessment of the inverter-grid interface has been assessed extensively through state-space and impedance-based methods. The current work presents stability analysis method based on the load-affected loop gain of the innermost control loop, which includes the effect of phase-locked loop and grid impedance. The stability analysis is carried out by assessing modeled and measured loop gains using the Nyquist criterion, step responses, and system closed-loop poles. The stability issues originating from grid impedance or too high phase-locked loop bandwidth are accurately predicted by examining the innermost control loop.**

***Index Terms*—Grid-connected inverter, Stability analysis, Control system analysis, Online measurement**

I. Introduction

THREE-PHASE grid-connected inverters have been widely adopted for power processing in modern power systems. The share of grid-connected inverters has increased rapidly over the past decade, mainly driven by tightened requirements for more precise power processing and the rise of renewable energy production [1], [2]. As the inverters have fast and complex control dynamics and often exhibit non-passive impedance characteristics, stability issues have become an important design factor in power-electronic-based systems [3]–[5]. Power quality and stability issues emerging from the unintentional interactions between the inverters and the grid have been studied extensively [6]–[8].

The grid impedance affects the operation of grid-connected devices, and may deteriorate the control performance and robustness. The most commonly used approaches for stability assessment are the impedance-based methods [3], [9], [10] as well as the conventional control-theory methods such as state-space analysis [11]–[13]. However, the dq-domain impedance measurements are often inaccurate or impractical [3], [14] and the state-space analysis requires significant modeling effort [15].

The transfer functions of the inverter control loops are used to describe the dynamic behavior. The load effect imposed by the grid impedance can be included in the transfer functions through small-signal modeling [3]. The most practical control loop for a stability assessment of the internal stability of an inverter is the innermost control loop with highest control bandwidth, which is typically the AC-current-control loop in grid-feeding inverters. The effect of other control loops on the current-control loop will take place through the load effect, which consists of the ratio of inverter and grid impedances.

This paper presents a small-signal model of a load-affected AC-current-control loop, which includes the grid impedance and the impact of synchronous reference-frame phase-locked loop (SRF-PLL). In addition, the loop gain is shown to predict accurately the control performance of the inverter and the stability margins related to the small-signal interactions. The model is validated with simulation measurements, and the performance and robustness indications are verified with simulations and experiments on kW-scale three-phase inverter.

The remainder of this paper is organized as follows. Section II presents the small-signal modeling of the load-affected current-controller loop gain. Section III shows the simulation validation of the modeled current controller loop and the effect of grid impedance and PLL bandwidth on the stability margins. In Section IV, experiments with power hardware-in-the-loop setup show online measurements of the current loop, based upon which the stability margin is indicated accurately. Section V draws the conclusion.

II. Dynamic modeling of CF-CO inverter

In renewable energy systems, the inverter is typically in grid-feeding mode, where a phase-locked loop is used to synchronize the inverter to grid voltages. In photovoltaic (PV) applications, the DC voltage must be controlled in order to achieve maximum-power-point operation of the PV panels. A single-stage PV inverter, which also controls the DC-link voltage, has been widely adopted as it removes the need for an additional DC-DC converter. The single-stage

$$\begin{bmatrix}\hat{\mathbf{v}}_{\text{in}}\\ \hat{\mathbf{i}}_{\text{o}}\end{bmatrix}=\begin{bmatrix}\mathbf{Z}_{\text{in}}+\mathbf{T}_{\text{oi}}[\mathbf{I}+\mathbf{Y}_{\text{o}}\mathbf{Z}_{\text{L}}]^{-1}\mathbf{Z}_{\text{L}}\mathbf{G}_{\text{io}} & \mathbf{T}_{\text{oi}}[\mathbf{I}+\mathbf{Y}_{\text{o}}\mathbf{Z}_{\text{L}}]^{-1} & \mathbf{Z}_{\text{ci}}+\mathbf{T}_{\text{oi}}[\mathbf{I}+\mathbf{Y}_{\text{o}}\mathbf{Z}_{\text{L}}]^{-1}\mathbf{Z}_{\text{L}}\mathbf{G}_{\text{co}}\\ [\mathbf{I}+\mathbf{Y}_{\text{o}}\mathbf{Z}_{\text{L}}]^{-1}\mathbf{G}_{\text{io}} & -[\mathbf{I}+\mathbf{Y}_{\text{o}}\mathbf{Z}_{\text{L}}]^{-1}\mathbf{Y}_{\text{o}} & [\mathbf{I}+\mathbf{Y}_{\text{o}}\mathbf{Z}_{\text{L}}]^{-1}\mathbf{G}_{\text{co}}\end{bmatrix}\begin{bmatrix}\hat{\mathbf{i}}_{\text{in}}\\ \hat{\mathbf{v}}_{\text{o}}\\ \hat{\mathbf{d}}\end{bmatrix} \tag{1}$$

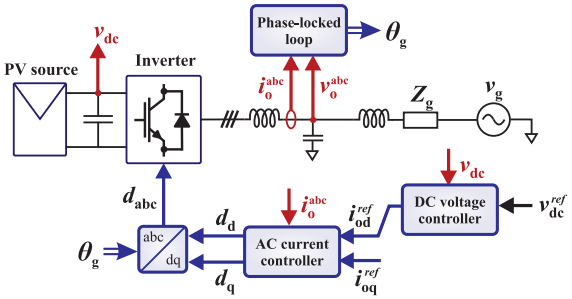

Fig. 1: Schematic of cascaded control system in CF-CO inverter.

inverter typically operates in cascaded control scheme, which consists of outer DC voltage control loop, inner output current control loop, and phase-locked loop for grid synchronization. An inverter with this configuration is known as current-fed current-output (CF-CO) inverter. Fig. 1 presents the simplified block diagram of the control system.

A. Open-loop dynamics on dq-domain

A common approach for control theory and stability assessment is small-signal analysis, where the system response to a small-signal variation around steady-state operation point is considered. Nonlinear systems can be approximated with linear equations by linearizing the system around a steady-state operation point. The small-signal approach is feasible when the superimposed AC signal has significantly lower amplitude than the steady-state DC signal.

In three-phase AC systems, the signals become matrices, instead of scalars found in DC systems. In addition, no small-signal equilibrium point exists as the variables fluctuate with the fundamental frequency. The inherent complexity of three-phase AC systems has led to introduction of advanced modeling techniques, in order to reduce the complexity of modeling and control design. The complexity can be decreased by, for example, approaches based on sequence domain or synchronous reference frame (dq domain). In the dq-domain analysis, the three phases are described as direct, quadrature, and zero components in rotating reference frame. As the frame rotates with fundamental frequency, the fundamental AC component is removed from the signals. Additionally, the system is usually assumed to be balanced, so the zero component can be neglected. The system is reduced to two DC signals, which allows straightforward Jacobian linearization.

The modeling of CF-CO inverter in the dq domain has been widely presented in previous work [3], [16]. The linearized multi-input multi-output (MIMO) open-loop transfer matrices can be given in the dq domain as

$$\begin{bmatrix}\hat{\mathbf{v}}_{\text{in}}\\ \hat{\mathbf{i}}_{\text{o}}\end{bmatrix}=\begin{bmatrix}\mathbf{Z}_{\text{in}} & \mathbf{T}_{\text{oi}} & \mathbf{G}_{\text{ci}}\\ \mathbf{G}_{\text{io}} & -\mathbf{Y}_{\text{o}} & \mathbf{G}_{\text{co}}\end{bmatrix}\begin{bmatrix}\hat{\mathbf{i}}_{\text{in}}\\ \hat{\mathbf{v}}_{\text{o}}\\ \hat{\mathbf{d}}\end{bmatrix} \tag{2}$$

B. Load effect of grid impedance

A non-ideal grid-connection of the inverter has grid impedance, which results in load effect and alters the transfer functions shown in (2). Fig. 2 presents the origin of load effect as a two-port model. The inclusion of load impedance $\mathbf{Z}_{\text{L}}$ changes the dynamics, as the original ideal-load output voltage is replaced by

$$\hat{\mathbf{v}}_{\text{o}}=\hat{\mathbf{v}}_{\text{o}}^{\text{L}}+\mathbf{Z}_{\text{L}}\hat{\mathbf{i}}_{\text{o}} \tag{3}$$

where superscript L denotes the load-affected variable. Substituting lower row of (2) to (3) yields

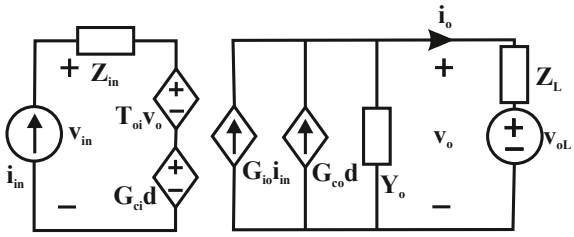

Fig. 2: Load-affected multivariable equivalent circuit of CF-CO inverter.

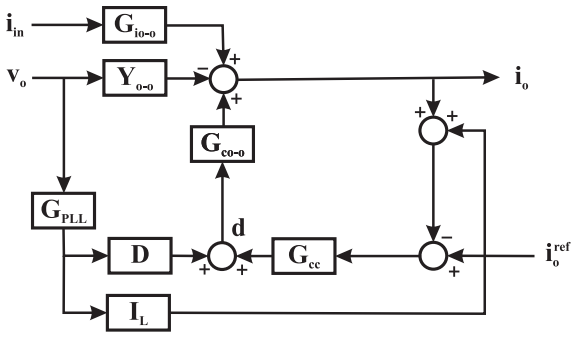

Fig. 3: Small-signal block diagram of output dynamics with current control and PLL.

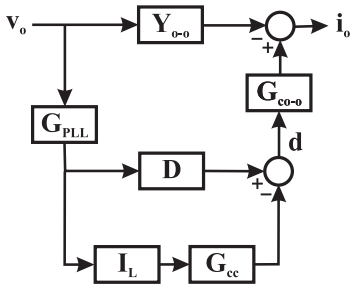

Fig. 4: Small-signal block diagram of PLL-affected output impedance.

$$\begin{aligned}\hat{\mathbf{v}}_{\mathrm{o}} =&[\mathbf{I}+\mathbf{Y}_{\mathrm{o}}\mathbf{Z}_{\mathrm{L}}]^{-1}\hat{\mathbf{v}}_{\mathrm{o}}^{\mathrm{L}}\\ &+[\mathbf{I}+\mathbf{Y}_{\mathrm{o}}\mathbf{Z}_{\mathrm{L}}]^{-1}\mathbf{Z}_{\mathrm{L}}\mathbf{G}_{\mathrm{io}}\hat{\mathbf{i}}_{\mathrm{in}}\\ &+[\mathbf{I}+\mathbf{Y}_{\mathrm{o}}\mathbf{Z}_{\mathrm{L}}]^{-1}\mathbf{Z}_{\mathrm{L}}\mathbf{G}_{\mathrm{co}}\hat{\mathbf{d}}\end{aligned} \tag{4}$$

Substituting (3)-(4) into (4) yields the load-affected multi-variable transfer functions shown in (1). In order to accurately model the load effect, the impact of grid-synchronization by PLL should be considered, as it affects the output admittance of the inverter. Fig. 3 presents the small-signal block diagram for the inverter output dynamics, where the PLL and current controller are included. The PLL adds a parallel signal paths from $\mathbf{v}_{\mathrm{o}}$ to $\mathbf{i}_{\mathrm{o}}$, which affects the total output admittance. Fig. 4 shows the PLL-affected output impedance derived from Fig. 3. The small-signal modeling of the PLL has been considered in [16]. The PLL-affected total output admittance is given by

$$\mathbf{Y}_{\mathrm{o\text{-}c}} = \mathbf{Y}_{\mathrm{o}} + \mathbf{Y}_{\mathrm{pll}} \tag{5}$$

where $\mathbf{Y}_{\mathrm{pll}}$ is the PLL-induced admittance component, which can be given as

$$\mathbf{Y}_{\mathrm{pll}} = \mathbf{G}_{\mathrm{co}}\mathbf{G}_{\mathrm{cc}}\mathbf{I}_{\mathrm{L}}\mathbf{G}_{\mathrm{pll}} - \mathbf{G}_{\mathrm{co}}\mathbf{D}\mathbf{G}_{\mathrm{pll}} \tag{6}$$

where

$$\mathbf{D} = \begin{bmatrix} 0 & -D_{\mathrm{q}} \\ 0 & D_{\mathrm{d}} \end{bmatrix} \qquad \mathbf{G}_{\mathrm{pll}} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{L_{\mathrm{pll}}}{V_{\mathrm{od}}(1+L_{\mathrm{pll}})} \end{bmatrix} \tag{7}$$

$$\mathbf{I}_{\mathrm{L}} = \begin{bmatrix} 0 & I_{\mathrm{Lq}} \\ 0 & -I_{\mathrm{Ld}} \end{bmatrix} \qquad \mathbf{G}_{\mathrm{cc}} = \begin{bmatrix} G_{\mathrm{PId}} & 0 \\ 0 & G_{\mathrm{PIq}} \end{bmatrix} \tag{8}$$

$$L_{\mathrm{pll}} = (K_{\mathrm{P\text{-}pll}} + K_{\mathrm{I\text{-}pll}}/s) * V_{\mathrm{od}}/s. \tag{9}$$

Finally, the load affected control-to-output transfer function, which is the plant for the current controller, is given by

$$\mathbf{G}_{\mathrm{co}}^{\mathrm{L}} = [\mathbf{I}+\mathbf{Y}_{\mathrm{o\text{-}c}}\mathbf{Z}_{\mathrm{L}}]^{-1}\mathbf{G}_{\mathrm{co}} \tag{10}$$

In this analysis, the outer DC voltage controller is omitted, as the impact can be considered negligible due to significantly lower bandwidth.

C. Full-order current control loop

A typical controller choice for the AC current controller is the PI-type compensator, which is usually identical for both channels. The cross-couplings are often assumed to be small and neglected, which results in simplified analysis as the d- and q-channels can be separated. The reduced-order current controller loop gain is

$$L_{\mathrm{cc\text{-}d}}^{\mathrm{RO}} = G_{\mathrm{codd}}^{\mathrm{L}} G_{\mathrm{PWM}} G_{\mathrm{PI\text{-}d}} H_{\mathrm{d}} \tag{11}$$

where $G_{\mathrm{codd\text{-}o}}$ is the open-loop control to output of d-channel, G_{PWM} is the pulse-width modulator, $G_{\mathrm{PI\text{-}d}}$ is the current controller, and H_{d} is the sensing gain. However, ignoring the cross-couplings may lead to inaccurate models. Fig. 5 shows the full-order control block diagram of the current control loop gain, which includes the cross-couplings. The dashed red lines indicate the interface where the loop is calculated or measured. Based on the block diagram, the full-order control loop can derived

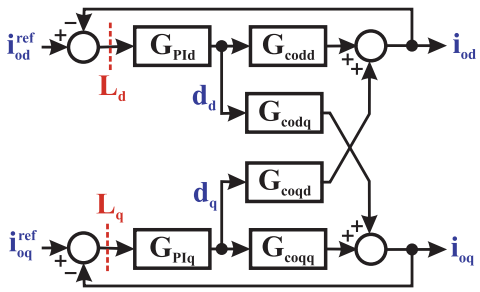

Fig. 5: Control block diagram of the current control loops.

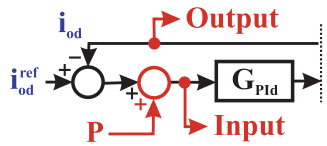

Fig. 6: Excitation injection diagram for d-channel loop measurement.

$$L_{\mathrm{cc\text{-}d}}^{\mathrm{FO}} = G_{\mathrm{codd}}^{\mathrm{L}} G_{\mathrm{PId}} - \frac{G_{\mathrm{codq}}^{\mathrm{L}} G_{\mathrm{Gcoqd}}^{\mathrm{L}} G_{\mathrm{PIq}} G_{\mathrm{PId}}}{1 + G_{\mathrm{PIq}} G_{\mathrm{coqq}}^{\mathrm{L}}} \tag{12}$$

where G_{PWM} and H_{d} are incorporated into G_{PId} and G_{PIq}. The system control characteristics can be predicted based on the closed-loop transfer function from input to output, where the control feedback loops are closed. The closed-loop transfer function from d-current reference to output d-current of the current controller can be given as

$$G_{\mathrm{c\text{-}cod}} = \frac{L_{\mathrm{cc\text{-}d}}^{\mathrm{FO}}}{1 + L_{\mathrm{cc\text{-}d}}^{\mathrm{FO}}} \tag{13}$$

and similarly for $G_{\mathrm{c\text{-}coq}}$ of the q-channel.

III. Simulations

The simulations are performed in MATLAB/Simulink environment with a three-phase grid-connected CF-CO inverter shown in Fig. 1. The nominal output voltage is 120 V and the output power is 2.7 kW, which match the parameters used in the experimental setup. The output current measurements are taken from the middle of the LCL-filter so that the CL-part appears in grid impedance. Table I in Appendix presents the controller parameters used in the simulation experiments.

A. Loop-gain measurements

Frequency-response measurements have been widely used for model verification and assessment of system behavior. In general, the measurements are performed by injecting an excitation signal to the system and measuring the response [17]. In this work, a broadband ternary pseudo-random excitation was used to measure the current controller loop gains in varying operation conditions. The system was perturbed by a ternary sequence with length of $N = 1999$ generated at $f_{\mathrm{gen}} = 4$ kHz. Thus, the frequency resolution and the lowest obtainable frequency are 2 Hz [17]. The feasible highest frequency of the measurement is approximately 2 kHz, due

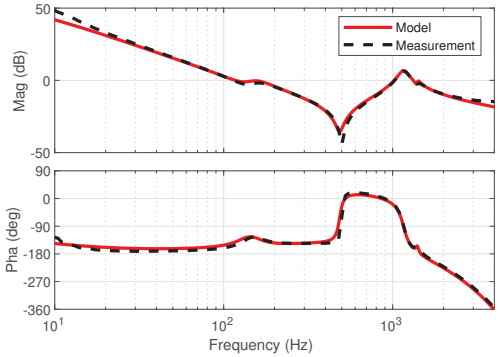

Fig. 7: Modeled and measured load-affected loop gain transfer function from the q-channel of current controller.

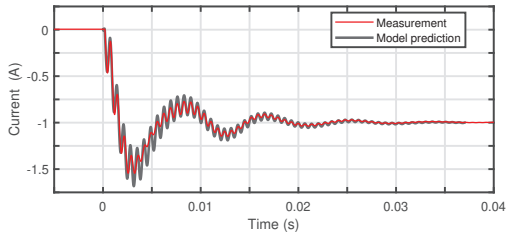

Fig. 8: Modeled (grey) and measured (red) q-channel current response to a step change in current reference (from 0 to -1 A at 0 s).

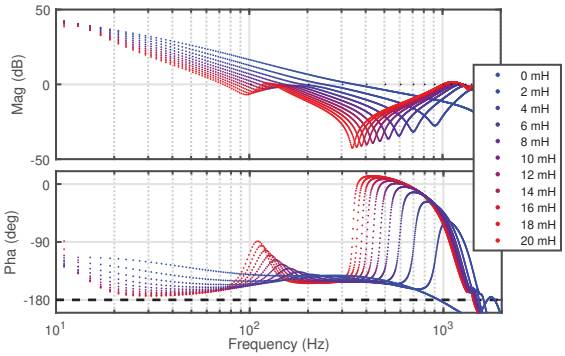

Fig. 9: Measured load-affected loop gain from q-channel with varying grid impedance.

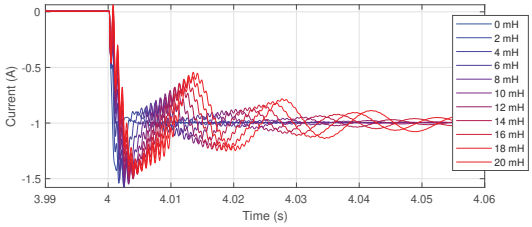

Fig. 10: Current q-component response to step change with varying grid inductance values.

to decreasing power of the excitation. Fig. 6 schematically presents the measurement implementation, supplementing the full-order block diagram of the control loops shown in Fig. 5. The ternary sequence is injected to the current controller loop, and the input and output signals are measured and Fourier-transformed, which yields the current-control-loop transfer function. The presented load-affected current-controller loop gain model was verified with measurements from the simulation. Fig. 7 presents the measured and modeled loop gain transfer function of the current controller q-channel for a grid inductance of 10 mH.

The control performance can be predicted from the closed loop transfer function derived in (13). To further verify the presented modeling method and predictions of the system behavior, a step-change to q-channel current reference was performed in simulation and the current response was measured. Fig. 8 presents the current response predicted from the modeled transfer function (grey) and the simulated current response (red) for the system with 10 mH grid inductance. The modeled transfer function predicts the system response to the transient with high accuracy, as the overshoot, oscillation frequency, and settling time are accurately captured.

B. Load-affected control performance

The sensitivity of the current controller loop gain to the varying grid impedance is illustrated by measuring the load-affected current loop with different grid inductance values. Fig. 9 presents the measured q-channel loop gain with the grid inductance ranging from 0 to 20 mH, which corresponds to a short-circuit ratio (SCR) decrease from 40 to 2. The increase in grid inductance magnifies the load effect, which results in decreased magnitude and phase margin. This decreases the control bandwidth, thus reducing the stability margins and control performance. Fig. 10 presents a set of step responses showing the output current q-component when the reference value is stepped from 0 to -1 A. Increasing the grid inductance deteriorates the control performance, validating the hypothesis. Thus, modeled load-affected control loop can be used to assess the performance and stability of an inverter in a weak grid.

C. PLL impact on current loop robustness

A high control bandwidth of PLL is known to cause stability issues in weak grids, due to the negative-resistance-like behavior of the inverter output admittance q-component [13], [18]. Previous research has mostly assessed the stability impact of the PLL based on the impedance-based stability criterion [18], [19]. The PLL affects the output admittance of the inverter, which is included in the load-affected control-to-output transfer function in (10). The proposed current-control-loop model incorporates the load effect and, consequently, the effect of the PLL.

Fig. 11 shows the q component of the PLL-affected current-control loop when the PLL-controller settings are varied. The phase margin reduces significantly when the PLL-control bandwidth is increased. The Nyquist criterion can be applied for the stability assessment of the control loop. Fig. 12 provides an overview of the Nyquist contour. Based on the modeled loop, the open-loop transfer function has a RHP pole,

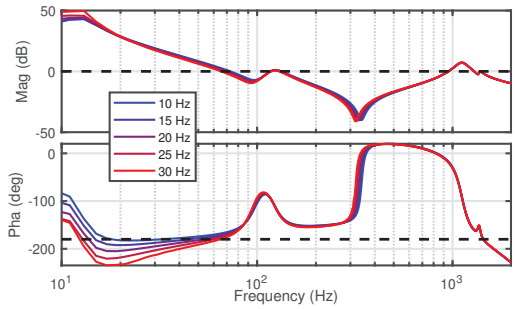

Fig. 11: Measured q-channel current control loop gain with different PLL control bandwidths.

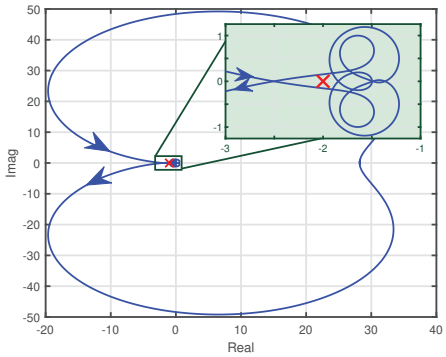

Fig. 12: Nyquist contour of the q-channel current controller open-loop gain (zoomed figure on green background).

so the locus must encircle the critical point once counter-clockwise in order for the closed-loop system to be stable. Increasing the PLL bandwidth shifts the crossing point on the real axis towards the critical point, as shown in Fig. 13. With control bandwidths above 31 Hz, the open-loop locus no longer encircles the critical point, indicating that the closed-loop system would be unstable.

The prediction is verified by simulations. The PLL-induced stability issues were tested by changing the PLL bandwidth by adjusting the PI-controller gains during simulation. Three cases were considered: the PLL bandwidth was changed from 20 Hz to 27, 31, or 35 Hz. Nyquist criterion (see Fig. 13) predicts that the systems will be stable, marginally stable, and unstable, respectively. Fig. 14 presents the time-domain waveforms of the output current d-component for the three

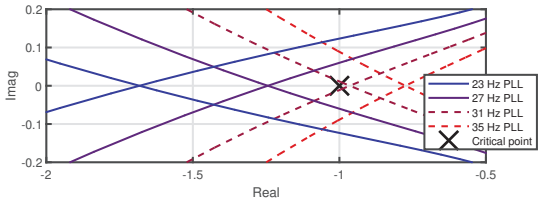

Fig. 13: Nyquist loci of the current controller loop for varying PLL bandwidths, where the unstable closed-loops are shown with dashed line.

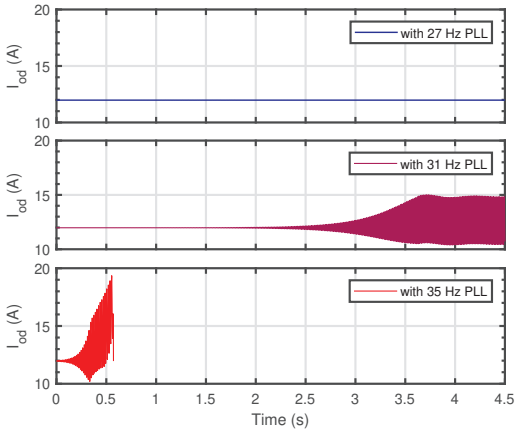

Fig. 14: Output current d-component when the PLL bandwidth is changed from 20 Hz to 27 Hz (blue), 31 Hz (purple), or 35 Hz (red) at $t = 0$ s.

experiments. The response is dominated by the pole pair, which causes oscillation at the main oscillatory frequency around 70 Hz. When the PLL bandwidth is changed to 27 Hz, the stability margins are sufficient and no visible transient occurs. When the bandwidth is changed to 31 Hz, the system initially appears stable. However, after a few seconds the oscillation has increased to the state of sustained resonance, which indicates marginal stability. In the third scenario, the PLL controller is changed to bandwidth of 35 Hz, which instantly results in unstable oscillation and the system shuts down at $t = 0.6$ s. Consequently, the Nyquist contours in Fig. 13 predicted the system stability with high accuracy.

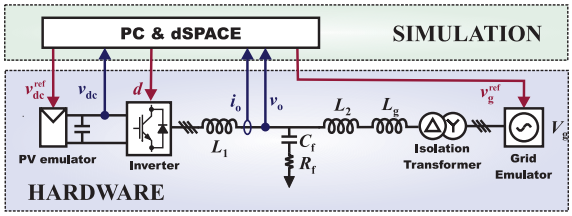

Fig. 15: Experimental power hardware-in-the-loop setup.

IV. Experiments

The experimental power hardware-in-the-loop setup consists of a PV emulator (*Spitzenberger Spies PVS 7000*), a 10 kW three-phase inverter (*Myway Plus MWINV-9R144*), and a voltage amplifier (*Spitzenberger Spies PAC 15000*). An isolation transformer connects the inverter to the grid voltages, and inductors (12 mH) are connected before the voltage amplifier to emulate the grid impedance (see Fig. 1). The inverter control system is implemented to a dSPACE real-time simulation. Fig. 15 provides an overview of the experimental setup. The parameters are shown in Table I in Appendix.

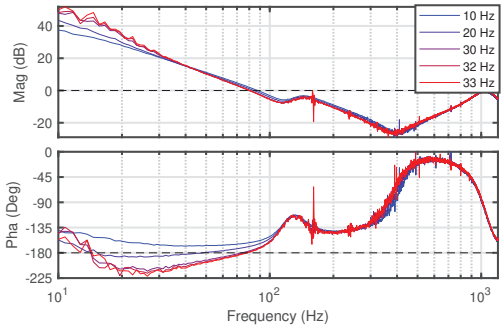

Fig. 16: Measured experimental current controller q-channel loops with different PLL bandwidths.

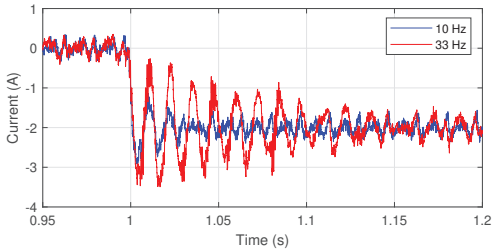

Fig. 17: Current step responses with different PLL controller tunings.

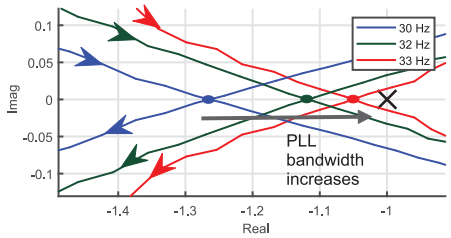

Fig. 18: Nyquist loci of measured current-controller loops with different PLL bandwidths.

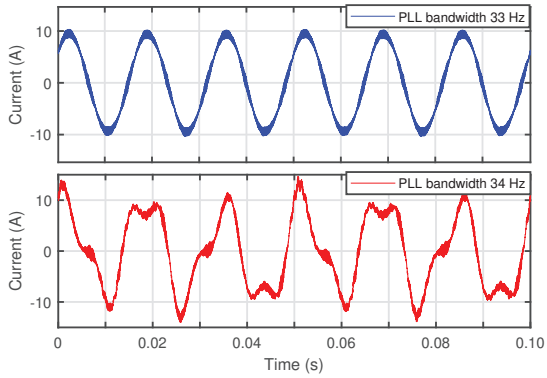

Fig. 19: Steady-state phase A currents with PLL tunings of 33 and 34 Hz.

A. *Stability and performance analysis*

Fig. 16 shows the measured current-controller loop q components with PLL control bandwidths of 10, 20, 30, 32, and 33 Hz. As predicted from models and simulation, the phase decreases significantly when the PLL bandwidth increases. With 33 Hz control tuning, the measured loop indicates a phase margin of only 1.0 degrees, and the high sensitivity produces noise to the loop measurements. Fig. 17 shows the q-current step tests with PLL tunings of 10 and 33 Hz, where the highly oscillatory response validates the very low phase margin. Fig. 18 shows the Nyquist loci calculated from the measured loop gains, which clearly indicate that increasing bandwidth shifts the contour closer to the critical point. Based on 32 and 33 Hz contours, tuning the PLL to 34 Hz bandwidth would result in marginal stability. Fig. 19 shows the phase A output current waveforms in steady state for PLL tunings with 33 Hz and 34 Hz. As predicted from the current-controller loop measurements and the Nyquist analysis, the 34 Hz PLL results in marginal stability with highly distorted waveforms. Despite the very low stability margins for 33 Hz PLL, the steady-state current waveform shows no signs of stability issues. However, the low margins manifest in system transients, such as the step responses shown previously.

B. *Discussion*

The impedance-based stability criterion has been widely applied for stability analysis of grid-connected inverters. However, measuring the grid and inverter impedances is not always possible, as special hardware may be required. This work presents a method to access the stability margins directly from the online measurements of the AC current controller loop. The implementation of the method is straightforward and can be directly included in the current controllers of inverters. In addition, the use of wideband-identification techniques makes it possible to perform the required frequency-response measurements, typically within few seconds. Thus, the proposed method can be used for real-time stability assessment or adaptive control of inverters.

V. Conclusion

The grid impedance affects the grid-connected inverters through the load effect, which may deteriorate system performance and robustness. This paper proposes a method for assessing the stability of a grid-connected inverter based on the current controller loop gain. The loop gain can be modeled accurately to include the effect of the grid impedance and the PLL, which are known to compromise the stability in weak grids. Another approach is to measure the current controller loop gain online in normal operation conditions. The inverter robustness can be assessed by calculating the Nyquist contour or directly from the indicated phase margin. The presented methods were verified by simulations and power hardware-in-the-loop experiments.

APPENDIX

TABLE I: Parameters for inverter and grid in simulations and experiments.

Parameter	Symbol	Value
Grid frequency	f_{n}	60 Hz
Nominal power	P_{n}	2.7 kVA
Nominal phase voltage	V_{n}	120 V
Switching frequency	f_{sw}	8 kHz
DC voltage reference	V_{dc}^{*}	414 V
D-current reference	i_{d}^{*}	10.6 A
Q-current reference	i_{q}^{*}	0 A
DC capacitance	C_{dc}	1.5 mF
Inverter-side inductance	L_1	2.2 mH
Inverter-side resistance	R_{L1}	100 mΩ
Filter capacitance	C_{f}	10 μF
Filter capacitor resistance	R_{Cf}	1.8 Ω
Grid-side inductance	L_2	0.9 mH
Grid-side resistance	R_{L2}	400 mΩ
Grid inductance	L_{g}	0...20 mH
AC current control P gain	$K_{\mathrm{P\text{-}CC}}$	0.0149
AC current control I gain	$K_{\mathrm{I\text{-}CC}}$	23.442
DC voltage control P gain	$K_{\mathrm{P\text{-}VC}}$	0.0962
DC voltage control I gain	$K_{\mathrm{I\text{-}VC}}$	1.2092
PLL control P gain	$K_{\mathrm{P\text{-}PLL}}$	0.39...1.36
PLL control I gain	$K_{\mathrm{I\text{-}PLL}}$	9.77...119.7

REFERENCES

[1] B. Bose, "Global Energy Scenario and Impact of Power Electronics in 21St. Century," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2638–2651, 2013.

[2] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed Power-Generation Systems and Protection," *Proceedings of the IEEE*, vol. 105, no. 7, pp. 1311–1331, 2017.

[3] T. Suntio, T. Messo, M. Berg, H. Alenius, T. Reinikka, R. Luhtala, and K. Zenger, "Impedance-Based Interactions in Grid-Tied Three-Phase Inverters in Renewable Energy Applications," *Energies*, vol. 12, no. 464, 2019.

[4] T. Suntio, T. Messo, and J. Puukko, *Power Electronics Converters - Dynamics and Control in Conventional and Renewable Energy Applications*. Wiley-VCH, 2017.

[5] X. Wang, L. Harnefors, and F. Blaabjerg, "Unified Impedance Model of Grid-Connected Voltage-Source Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1775–1787, 2018.

[6] C. Li, "Unstable Operation of Photovoltaic Inverter from Field Experiences," *IEEE Transactions on Power Delivery*, vol. 8977, no. c, pp. 1–1, 2017.

[7] C. Buchhagen, C. Rauscher, A. Menze, and J. Jung, "BorWin1 - First Experiences with harmonic interactions in converter dominated grids," *International ETG Congress 2015; Die Energiewende - Blueprints for the new energy age*, pp. 27–33, 2015.

[8] C. Zou, H. Rao, S. Xu, Y. Li, W. Li, J. Chen, X. Zhao, Y. Yang, and B. Lei, "Analysis of Resonance between a VSC-HVDC Converter and the AC Grid," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 157–10 168, 2018.

[9] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3075–3078, 2011.

[10] A. Rygg, M. Molinas, C. Zhang, and X. Cai, "On the equivalence and impact on stability of impedance modelling of power electronic converters in different domains," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1–1, 2017.

[11] M. Amin, A. Rygg, and M. Molinas, "Impedance-based and eigenvalue based stability assessment compared in VSC-HVDC system," *ECCE 2016 - IEEE Energy Conversion Congress and Exposition, Proceedings*, 2016.

[12] Y. Wang, X. Wang, F. Blaabjerg, and Z. Chen, "Harmonic instability assessment using state-space modeling and participation analysis in inverter-fed power systems," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 806–816, 2017.

[13] J. Z. Zhou, H. Ding, S. Fan, Y. Zhang, and A. M. Gole, "Impact of short circuit ratio and phase locked loop parameters on the small signal behavior of a VSC HVDC converter," *IEEE Transactions on Power Delivery*, vol. 29, no. 5, pp. 2287–2296, 2014.

[14] H. Gong, D. Yang, and X. Wang, "Impact of Synchronization Phase Dynamics on DQ Impedance Measurement," *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, no. 1, pp. 1–7, 2018.

[15] J. Sun, "Small-signal methods for AC distributed power systems-A review," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2545–2554, 2009.

[16] T. Messo, R. Luhtala, A. Aapro, and T. Roinila, "Accurate Impedance Model of Grid-Connected Inverter for Small-Signal Stability Assessment in High-Impedance Grids," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, no. 1. IEEJ Industry Application Society, 2018, pp. 3156–3163.

[17] K. Godfrey, *Perturbation Signals for System Identification*. Prentice Hall, UK, 1993.

[18] T. Messo, J. Jokipii, A. Mäkinen, and T. Suntio, "Modeling the grid synchronization induced negative-resistor-like behavior in the output impedance of a three-phase photovoltaic inverter," *2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems, PEDG 2013 - Conference Proceedings*, pp. 1–7, 2013.

[19] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue, "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 310–321, 2015.