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THINNING OF GALLIUM ARSENIDE WAFERS USING ADVANCED ABRASIVES AND ETCHANTS FOR LASER APPLICATIONS

Master of Science Thesis
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ABSTRACT

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Nowadays, lasers are used in many different applications, like telecommunications, radars, and medical treatments. These types of applications use semiconductor lasers which are commonly fabricated on top of GaAs wafers. To produce laser chips or dies with high efficiency, the GaAs wafer needs to be thinned. The aim of this thesis is to unify the process of thinning and polishing of GaAs and to improve the durability of a GaAs wafer by removing the stress caused by thinning from the wafer structure. In general, most of the wafer thickness is removed from the semiconductor wafer by thinning using slurry containing a coarse abrasive grain and liquid like water or oil, as well as a lapping or grinding machine. However, this causes various micro-damage to the surface of the wafer, which in turn, cause stress in to the structure of the wafer. The tension in wafer reduce the mechanical strength of the wafer, which however, can be improved by using slurry with smaller grain size that used in thinning.

In this work, double-sided polished 3" GaAs wafers were studied, which had initial thickness of 600 μm. The wafers were first thinned to 100–150 μm thickness. It was observed that the size of the abrasive grain significantly affects to the thinning rate. With larger, 9 μm abrasive grain slurry, the semiconductor material could be removed at a clearly faster rate compared to a smaller abrasive grain slurry with 0.3 μm grain size, which was used in polishing. In addition, it was noted that during polishing, a soft pad is needed as without the polishing pad the surface quality of the wafer was not high enough, i.e., not shiny enough.

Two different polishing pads have been used in the thesis. The polishing results obtained on these pads were contrary, when compared to each other. The first pad tested, effectively polished the center of the wafer, leaving the edges of the wafer almost intact. In addition, the increased polishing time did not increase the size of the polished area. In turn, the second tested pad polished the wafer more effectively from the edges of the wafer than from the center. With increased polishing time, a better polishing result was observed in contrary to the first pad. Lastly, few microns of GaAs were wet etched from the polished wafer as a finishing process. Wet etching removed material evenly from the entire area of wafer, but left the surface of the wafer looking very uneven and unfinished. In addition, atomic force microscopy images were taken from various samples to assess the effect of polishing on surface roughness. As a conclusion, it can be stated that polishing with small grain size slurry can be used as a finishing process of the GaAs wafers if the polishing time is long enough. Moreover, other polishing parameters need to be optimized to achieve a smooth outcome.

Keywords: semiconductor wafer, gallium arsenide, laser, thinning, lapping, polishing, abrasive grain

TIIVISTELMÄ

Erika Nojonen: Lasereissa käytettävien galliumarsenidikiekkojen ohentaminen hionta- ja etsausaineilla
Diplomityö
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Teknis-luonnontieteellinen DI-tutkinto-ohjelma
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Lasereita käytetään useissa eri sovelluksissa, kuten esimerkiksi tietoliikennetekniikassa, tutkissa tai lääketieteellisissä hoidoissa. Näissä sovelluksissa käytettyjen puolijohdelaserien teollisessa valmistuksessa käytetään yleisesti GaAs-kiekkoja alustamateriaalina. Valmistusprosessissa GaAs-kiekko tulee ohentaa, jotta saadaan tuotettua mahdollisimman tehokkaita lasersiruja. Tämän opinnäytteen taustalla on halu yhtenäistää GaAs-kiekon ohentamis- ja kiillotusprosessia sekä parantaa kiekon kestävyyttä poistamalla ohennuksen aiheuttamaa jännitettä kiekon rakenteesta. Yleisesti, puolijohdekiekosta poistetaan suurin osa massasta ohennuksen avulla käyttämällä karkean hiontarakeen ja nesteen, kuten esimerkiksi veden, muodostamaa seosta sekä hiontakonetta. Tämä kuitenkin aiheuttaa erilaisia mikrovaurioita kiekon pintaan, jotka puolestaan aiheuttavat kiekon rakenteeseen erilaisia jännitteitä. Nämä jännitteet puolestaan heikentävät kiekon mekaanista kestävyyttä. Tämän työn tavoitteena on poistaa ohentamisen synnyttämät mikrovauriot ja sitä kautta jännitteet käyttämällä kiillotusseosta. Käytetyn kiillotusseoksen hiomarakeet ovat pienempiä verrattuna ohennuksessa käytettyyn seokseen.

Kokeellisessa osuudessa käytettiin molemmin puolin kiillotettuja 3” GaAs-kiekkoja, joiden alkuperäinen paksuus oli noin 600 μm. Kiekot ohennettiin noin 100–150 μm paksuisiksi. Ohennuksessa huomattiin, että hiomarakeen koko vaikuttaa merkittävästi kiekon paksuuden muutosnopeuteen, sillä karkean hiontorakeen seoksella puolijohdemateriaalia saatiin poistettua selkeästi nopeammalla tahdilla verrattuna hienon hiomarakeen seokseen, jota käytettiin kiillotuksessa. Tässä opinnäytteessä hyvä kiillotustulos saatiin kiillotusseoksen, hiomakoneen sekä kiillotusalustan avulla. Työssä huomattiin selkeä tarve pehmeälle kiillotusalustalle kiillotuksen aikana, sillä ilman kiillotusalustaa kiekon pinnanlaatu oli erittäin huono.

Työssä käytettiin kahta erilaista kiillotusalustaa. Näillä alustoilla saadut kiillotustulokset olivat vastakkaiset keskenään. Ensimmäinen testattu alusta kiillotti kiekon keskiosaa tehokkaasti jättäen kiekon reunaosat lähes ennalleen. Lisättäessä kiillotusaikaa saatiin yhä parempi kiillotustulos, mutta kiillotetun alueen koko ei juurikaan kasvanut. Toinen testattu alusta puolestaan kiillotti kiekkoa tehokkaammin reunoista verrattuna keskustaan. Kiillotusaikaa lisäämällä saatiin parempi kiillotustulos. Jälkimmäisellä kiillotusalustalla kiekko oli jo lähes kauttaaltaan kiillottunut 30 min kiillotuksen jälkeen. Työn lopuksi testattiin märkäetsausta viimeistelevänä toimenpiteenä. Märkäetsaus poisti tasaisesti materiaali koko kiekon alalta, mutta jätti kiekon pinnan hyvin epätasaisen ja viimeistelemättömän näköiseksi. Osasta näytteistä otettiin lisäksi atomivoimamikroskooppikuvat, jotta kiillotuksen vaikutusta pinnan karheuteen voitiin arvioida. Yhteenvetona voidaan todeta, että hyvä kiillotustulos on mahdollista käyttämällä kiillotusseosta, kunhan kiillotusaika on tarpeeksi pitkä. Lisäksi, vielä paremman GaAs-kiekon kiillotustuloksen aikaansaamiseksi, muut kiillotusparametrit tulee optiomoida.

Avainsanat: puolijohdekiekko, gallium arseeni, laser, ohennus, hionta, kiilotus, hiomarae

PREFACE

This thesis was made for Modulight. I would like to thank Modulight for this opportunity to complete my thesis flexibly between studies and work. I thank Seppo Orsila and Petteri Uusimaa for this great opportunity to be a part of the laser family. The thesis have gave me valuable information about semiconductor production and processing. I want to thank my supervisors, Dr. Timo Aho and Dr. Lasse Orsila, for their support throughout the project and for their active participation on commenting my thesis.

I would also like to thank Ville Vilokkinen, Petri Melanen and Kirsi Rantanen for their theoretical skills and practical experience in the field of semiconductors. Without your help, many challenges would have remained unresolved. In addition, I am grateful for the entire cleanroom team and our hard-working technicians who have helped me with wafer processing during this thesis. Your help has been priceless. I would like to thank Jarno Reuna and Marianna Raappana for the opportunity to include AFM imaging to this thesis. AFM images brought new perspectives to the review of results. Thank you, Riina Ulkuniemi, Matius Hurskainen and Riina Hietikko for for your support during this spring, especially over difficult times.

These six years that I have been able to spend on the Hervanta campus have been the best years of my life. I have found wonderful people around me and made a lot of new friends. Thank you, Hiukkanen, for the opportunity to participate in the most wonderful events and being part of your operation. Special thanks to the KoIRaS for the great time, great events and great conversations I have had with you. I have gained many invaluable experiences together with you. I also thank the Vetoketju, that has helped me let go of my thesis from time to time. Finally, I want to tank you, Rasmus, for your endless support and encouragement during this thesis.

Tampereella, 24th May 2021

Erika Nojonen

CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

0CON-353	Chemcloth polishing pad
0CON-363	Polishing pad
$Al_xGa_{1-x}As$	Ternary compound form from Al, Ga and As
AlAs	Aluminum arsenide
AlGaAs	Aluminium gallium arsenide
α	Lattice constant
As	Arsenide
As_4	Cubical form of arsenide
AVG	Average
Br_2CH_3OH	Bromine-methanol
Br_2O_3	Dibromtrioxid
CBN	Cubic boron nitride
CeO_2	Cerium dioxide
CG10	Contact measurement gauge for thickness measurements
C_L	Impurity concentration in liquid
CMP	Chemical-mechanical polishing
C_S	Impurity concentration in solid
CW	Continuous wave
DBR	Distributed Bragg reflector
DH-laser	Double-heterostructure laser
E_1, E_2	Energy of lower and upper energy level
E	Energy
E_C	Energy of the conduction band
E_F	Energy of the Fermi level
E_g	Band gap energy
E_V	Maximum energy of valence band
$f(E,T)$	Fermi–Dirac distribution

$FeAs_2$	Iron arsenide mineral
FeAsS	Arsenopyrite
g_1, g_2	Degeneracy of lower and upper energy level
Ga	Gallium
GaAs	Gallium arsenide
$g_C(E)$	Density of states in the conduction band
$g_V(E)$	Density of states in valence band
$\hbar$	Reduced Planck constant
HeNe-laser	Laser based on helium and neon gas mixture
III–V semiconductors	Elements from group III and V of the periodic table
$In_{1-x}Ga_xAs_yP_{1-y}$	Quaternary compound form from In, Ga, As and P
IPA	Isopropanol
$\mathbf{k}$	Wave vector
k_B	Boltzmann constant
k_d	Distribution coefficient
l	Cavity length
λ	Wavelength
LEC	Liquid-encapsulated Czochralski method
LED	Light Emitting Diode
L_i	Internal losses per pass in the laser cavity
LiDAR	Light Detection And Ranging
ln	Natural logarithm
LP50	Lapping and polishing system
MBE	Molecular beam epitaxy
m_e^*	Effective mass of electron
MgF	Magnesium fluoride
m_h^*	Effective mass of hole
MOCVD	Metal-organic chemical vapour-phase epitaxy
μ	Chemical potential
N_1, N_2	Population of lower and upper energy level
n	Electron density
N_2	Nitrogen molecule

N_c	Critical inversion
Nd:YAG	Neodymium-doped yttrium aluminum garnet
N_{eff}^C	Effective nuber of states in conduction band
N_{eff}^V	Effective number of states in valence band
n_i	Number of electrons in intrinsic semiconductor
NRD	Non-radiative decay
O_2	Oxygen molecule
p	Hole concentration
PECVD	Plasma-enhanced chemical vapor deposition
p_i	Number of holes in intrinsic semiconductor
PLJ2, PP5, PLJ7, PP6, PP5GT	Types of precision jigs
R_1, R_2	Reflectivities of mirrors 1 and 2
RMS	Root mean square
rpm	Revolutions per minute
SiC	Silicon carbide
σ	Absorption cross-section
SiO_2	Silicon dioxide
STD	Standard deviation
T	Temperature
TEM_{00}	Lowest transverse electromagnetic mode order
TTV	Total thickness variation
V	Volume
VCSEL	Vertical cavity surface-emitting laser
WBS1	Wafer bonding station unit with one sample chamber
x, y	chemical composition ratios
ZnSe	Zinc selenide

1. INTRODUCTION

The word "laser" is an acronym for Light Amplification by Stimulated Emission of Radiation. The first laser was created already in 1960 by Theodore H. Maiman in the form of a ruby rod with silver-coated surfaces [1]. Lasers started to appear in different commercial and other applications already in 1961. In fact, the first laser based medical treatment was given in the end of 1961, when retinal tumor was successfully destroyed with optical ruby laser. [1]

The journey to create the first laser has been long and and eventful. Many famous physicists have been part of the development of lasers. One of the big milestone has been the understanding of the electromagnetic nature of light and discovering the elementary energy quanta in which he was awarded with Nobel Prize in 1918 by discovering the energy quanta. [1, 2] Another big name in the field of early photonics was Einstein, who proposed in 1917 that, in addition to spontaneous emission, electrons can be stimulated to emit light with specific wavelength. This stimulated emission is the basis of lasers, and it was proved almost 40 years later to be correct. [1]

Over time, this invention has become a multi-billion dollar industry ($15.13 billion in 2019), where semiconductor lasers account for 41 % of the total revenue of the laser market [3]. The demand for various lasers is constantly growing and various new applications are being actively developed by researchers. For example, semiconductor lasers are vital part of developing LiDAR (Light Detection And Ranging) systems for autonomous driving, optical fiber communications and different facial recognition applications [4, 5, 6].

Semiconductors are very versatile materials since their conductivity properties can be modified for example by doping. In technical point of view, the most important semiconductors are silicon, germanium and group III and V semiconductors [7]. Lasers and other optoelectronic applications require a direct band gap to operate efficiently, which is why silicon and germanium are not the most suitable materials for these applications as they have indirect band gap. Instead, optoelectronic applications use composite semiconductors with a direct band gap, like gallium arsenide (GaAs). The first reference of stimulated emission by GaAs-based p-n junction has been reached as early as 1962 [8].

As the demand of different semiconductor applications is increasing, modern semiconductor industry have an interest to try to minimize the production costs related to wafer

processing. One way to do this is to increase the production yield. Increasing yield involves process optimization, resulting in fewer erroneous units. Another way to meet the growing demand would be by increasing the production volume. This can be done by increasing the size of the wafer and/or reducing the size of the individual units.

Figure 1.1 illustrates how wafer diameter, wafer thickness and die (small block of semiconducting material) thickness have developed over years in case of silicon.

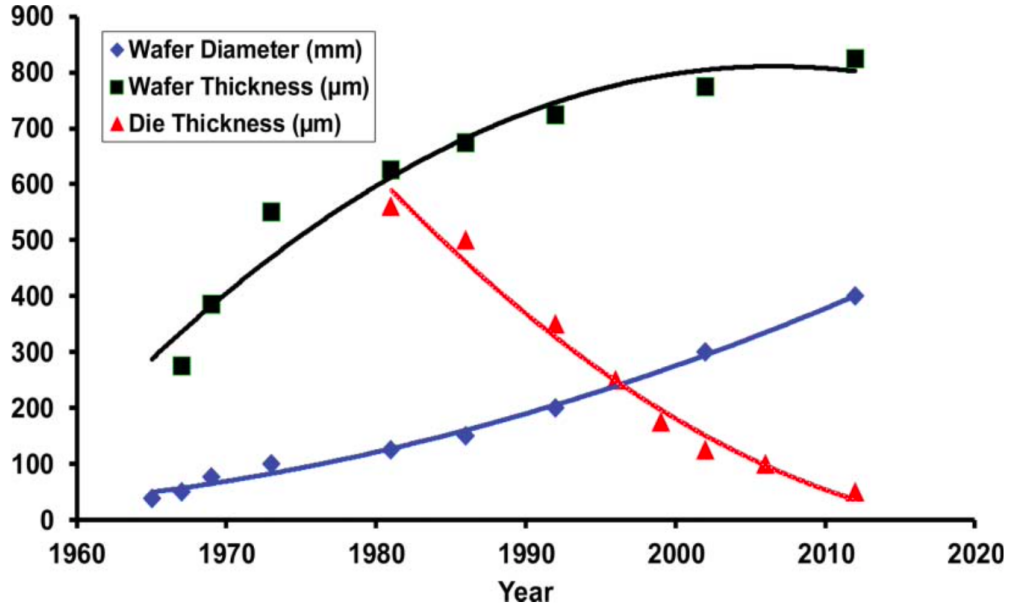


Figure 1.1. *Trends for wafer thickness, diameter and die thickness over years in case of silicon [9].*

Crystalline silicon is a very convenient material for integrated circuits as it is cheap and easily available and processed. Silicon is abundant element on earth and it can be found for example in rocks or sand. These raw materials can be melted in furnace to form silicon and carbon monoxide, following by silicon purification by letting it react with oxygen. This reaction decreases the amount of aluminum and calcium impurities. [10] However, with optoelectronic devices the interest is in III–V semiconductors and in this thesis especially in GaAs. The size development of GaAs wafers has been slower compared to silicon, since GaAs is more brittle material compared to silicon [11]. However, the trend is also growing. First GaAs-wafers were only 25 mm in diameter compared to nowadays wafers, where commercially available wafer size can be as high as 203 mm [12, 13].

As can be seen in the figure 1.1, the wafer thickness is increasing and simultaneously the die thickness is decreasing. Increasing the wafer thickness may seem contradictory with the desire to reduce the die size. The need for a thicker wafer rises from the fact that the wafer needs to have enough mechanical tolerance to support its own weight during various processing steps that are including in micromachining and thicker wafers have better mechanical tolerance [14].

Due to this conflict between the interest of decreasing the unit size and increasing wafer diameter and simultaneously its thickness, thinning techniques has became extremely relevant part of the semiconductor wafer processing. In addition, since the electrical performance (phase shift, output power, efficiency, gain) of semiconductor devices is related to the temperature of the devise, it is important to have proper thermal management to divert out any excess heat load [15]. One way to enhance heat dissipation is to have thinner device. For example thinner semiconductor lasers have better performance due to their relatively low thermal conductivity of semiconductors [9].

Thinning techniques can be divided into four primary methods that are mechanical grinding, chemical mechanical polishing, wet etching and atmospheric downstream plasma dry chemical etching. These techniques can be further divided to two groups: mechanical thinning and etching. [16] This thesis is focused on lapping using abrasive slurries. Lapping can be defined as the consumption of material using an abrasive slurry or an attached sanding pad, so it can be categorized as mechanical thinning process. Different thinning methods cause surface damage to the wafer, which is removed with polishing. [17] Simplified lapping process is illustrated in figure 1.2.

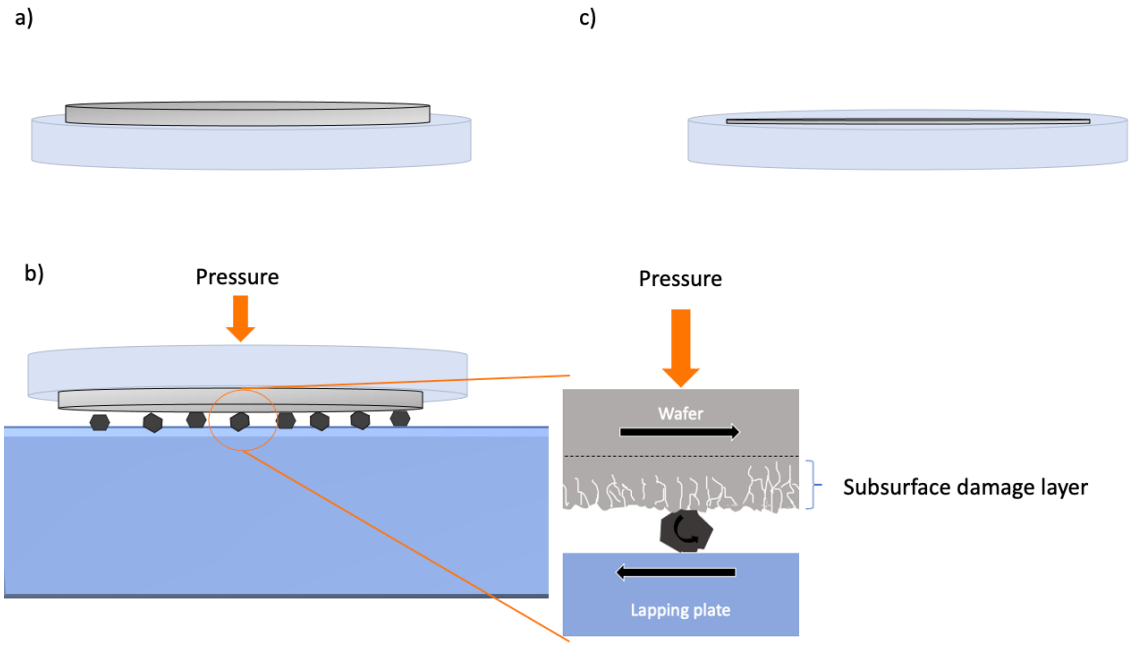


Figure 1.2. *Basic idea of thinning process by lapping. a) Wafer is attached against the glass substrate. The bonding can be done, e.g., with wax. b) Abrasive grains cause micro-cracks to the brittle material, which when combined creates small chips. c) Thinned wafer supported by the glass substrate.*

Typically GaAs wafers are thinned for 50 μm to 150 μm total thickness. As the wafers become thinner, their handling becomes more and more challenging. Thin wafers may bend due to their own weight, so moving them with flat surfaces is essential. Thin wafers must also be stored flat at all times. At the same time, special care must be taken to

ensure that the surface of the wafer is not damp, since wafer can stick to its storage box or table surface due surface tension forces. As the wafers are so light, smallest air flow can cause wafer flutter, which on the other hand can cause the breakage of delicate wafer. In addition, the thinning of the wafer by abrasive removal of semiconductor material causes surface damage, which further causes high compressive stress to the bottom side of wafer. Simultaneously, possible active region on frontside of the wafer experiences tensile stress. Combination of these stresses results in wafer bow, which increases the possibility to wafer breakage during micromachining process. [9]

Usually, the diameter of abrasive particles in the slurry are 5–20 μm [18]. In this work, smaller particle size of 0.3 μm were used alongside a bigger particle size of 9 μm aiming to reduce surface damage created during lapping process. With fewer surface damage created the wafer flatness should improve due less compressive stress [9]. Different thinning tests with these slurries were performed during this thesis project to find the most suitable way to thin the wafers. In addition, goal is to produce the least surface damage as well as the smoothest possible end result. In addition, parameters related to the thinning process were evaluated to find their effect on the thinning process. Parameters evaluated were jig pressure over the glass substrate and wafer to be thinned and rotation speed of the polishing pad.

The above paragraph summarizes the aims of this thesis: By decreasing the surface damage created during wafer lapping, thinning process could be enhanced. Simultaneously, attention can be focused on smooth and planar wafer surface as it is advantageous to create as flat and smooth wafers as possible. Smooth and planar surface of the wafer is extremely important since surface roughness have a great impact on semiconductor device performance [19].

The thesis is divided in following chapters: Chapter 2 considers about semiconductors as material, physics behind laser function and different applications based on semiconductor materials. Chapter 3 introduces different thinning methods by going through their operating principles and explaining why thinning is needed. In addition, in chapter 3 different abrasives are introduced. Chapter 4 explains the experimental part of the thesis by going through the equipment and methods used. Chapter 5 compile the results of the thinning tests and chapter 6 discusses about them in more detail. Finally, chapter 7 concludes the thesis.

2. MANUFACTURING OF III–V SEMICONDUCTOR MATERIALS AND THEIR LASER APPLICATIONS

Semiconductors have properties of both conductors and insulators. Their conductivity lies between conductors and insulators and their key feature is that their electrical conductivity can be controlled by temperature, illumination, impurities and chemical structure of the semiconductor. This possibility to customize the component as needed makes semiconductors versatile materials. [20]

To be more specific, the difference between the conduction band and valence band is significantly smaller compared to insulators, but not as small as conductors. In semiconductors, there is a certain energy band that is completely filled (valence band) and the next band at higher energy is completely empty (conduction band) at zero temperature. At valence band, electrons are bound and cannot move. At conduction band, on the other hand, electrons are free to move. Usually, material is consider as semiconductor, if its band gap is smaller than 3 eV. In real situations, where temperature is finite, the electrons have to be distributed on both bands according to the Fermi–Dirac distribution, meaning that there are electrons also on the conduction band and the material can conduct electricity. [21]

The conductivity of a semiconductor is determined by the number of valence electrons. Germanium, one of the earliest semiconductor material used, has four valence electrons. Today, it is not as used since silicon, which also has four valence electrons, has conquered the semiconductor industry. Silicon is easily available and its extraction, purification and crystallization processes are both economical and efficient. Gallium arsenide, on the other hand, has eight valence electrons, which is why it is very fast to respond to electronic signals. It is more expensive compared to silicon, but it has other explicit advantages like electron mobility and higher heat and moisture resistance. [22]. On the other hand, its manufacturing process is more difficult compared to manufacturing process of silicon and more hazardous chemicals are needed to process it. [7]

Most of the electronic devices today are based on silicon. However, when light absorption or emission is needed, direct band gap compound semiconductor are used. Light emitting diodes or LEDs are made using GaN or other III–V compounds. On the other hand, semiconductor lasers are based on GaAs, AlGaAs and other ternary and quaternary

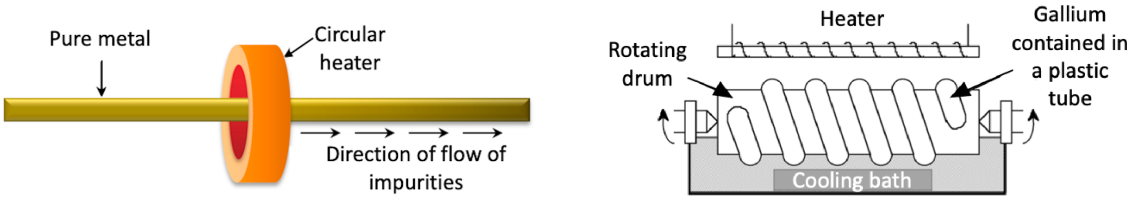
compounds. [20] This thesis focuses on GaAs wafers as well as GaAs applications in the laser industry.

2.1 GaAs wafer production

In order to manufacture high quality wafers, high purity of grown material accompanied by single crystal structure in the semiconductor ingot, is needed. For example, optoelectronic devices that are based on GaAs, acquire at least 99.9999 % or six nines purity level [23].

2.1.1 Isolation and purification of substances for GaAs

Gallium can be found in many rocks and ores of other metals, but its concentration is very small in these. In fact, most of the produced gallium is originated from bauxite industry, achieved by so called Bayer process, where alumina is obtained from bauxite. Gallium obtained from the Bayer process is about 98–99 % pure gallium. This is further purified to 99.99 % purity with acids and O_2 at high temperatures. Purification up to 99.99999 % or seven nines, is done with zone refining, which is based on impurities having a higher solubility in the molted metal. Typically metal goes though this process with > 500 passes. [23, 24] Zone refining method is illustrated in figure 2.1. Figure 2.1 a) shows the basic equipment for zone refining. Since the need for purification level in semiconductor applications is six nine or more, the semiconductor needs to go through purification process several times. In order to accelerate the process, the equipment is modified for this purpose as shown in Figure 2.1 b).



(a) *(b)*

Figure 2.1. *Different setups for zone refining. a) Basic setup for zone refining [25]. b) Modified setup for zone refining [24].*

Elemental arsenide can be found in two forms: yellow form, i.e., cubical form of As_4 and gray/metallic, i.e., parallelepiped form of As_4. However, elemental arsenide is quite rare material. Arsenide can be found as a compound form also in several minerals, where it can be isolated relatively easily. Commercially arsenide is obtained from $FeAs_2$ or FeAsS by smelting them at high temperatures of 650 °C to 700 °C. Gaseous arsenide is obtained as a reaction product and when cooled down to <613 °C, solid arsenide is obtained. Obtained arsenide is combined with lead and sublimed in 614 ° which binds

any sulfur impurities. Again, > 99.9999 % arsenide purity level is achieved with zone refining. [24]

2.1.2 Synthesis methods for GaAs

Synthesis of gallium arsenide can be done with direct reaction of gallium and arsenide in high temperature as shown below:

$$\mathrm{Ga\ (l) + As\ (g)} \xrightarrow{>1240\ ^\circ\mathrm{C}} \mathrm{GaAs\ (s)}. \tag{2.1}$$

However, challenges are posed by different vapor pressures as well as the highly exothermic nature of the reaction. In addition, since the arsenide is in vapor form, the reaction must be carried out under an overpressure of arsenide and in a sealed reaction tube. [24]

The resulting high purity GaAs has polycrystalline structure. This structure is not suitable for high-quality wafers and their application. Instead, single-crystal structure is needed. In order to create single-crystal ingots of GaAs, purified GaAs is melted and grown with crystal growth method like Czochralski method or Bridgman technique. [20] During crystal growing some of the semiconductor properties must be taken into account. These are the melting point of the semiconductor material and its vapor pressures at the melting point [24].

Czochralski method is a process for growing bulk, single-crystal semiconductor material. In order to produce single-crystal material, proper seed is needed. The seed provides a template for growing the desired structure. In order to prevent any inhomogeneous solidification due to temperature variations during growth, the growing crystal is slowly rotated to create slight stirring to the melted material. Czochralski method is generally used with silicon, germanium and some compound semiconductors. [20] In case of GaAs, some precautions are needed to prevent the volatile arsenide from vaporizing. To do this, boron oxide (Br_2O_3) is used. Boron oxide is a dense and viscous liquid when melted and it floats on the surface of GaAs and therefore prevents the arsenide from escaping through vaporization. This method is called liquid-encapsulated Czochralski (LEC) growth. [20] The setup for LEC is shown in figure 2.2.

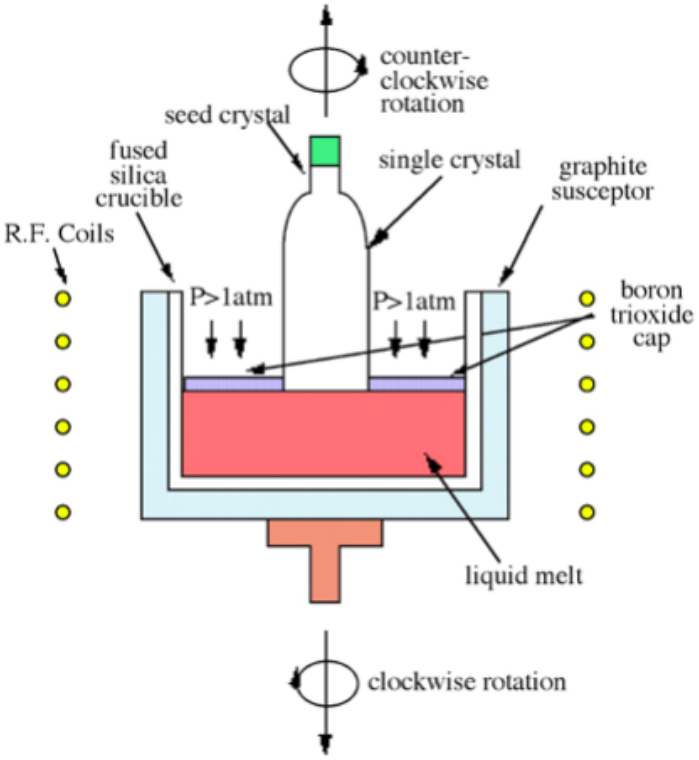


Figure 2.2. *Illustration of liquid-encapsulated Czochralski method [24].*

In **Bridgman technique**, two-zone furnace is needed. Oven should be able to keep a certain temperature at one end of the oven and another temperature at other end of the oven. In case of GaAs, the other end of furnace is held at 610 °C. This allows arsenide overpressure to be sufficient enough to prevent any arsenide loss from GaAs. The other end of the furnace with polycrystalline GaAs is held at 1240 °C, which is just over the GaAs melting temperature. The Bridgman technique setup is shown in figure 2.3.

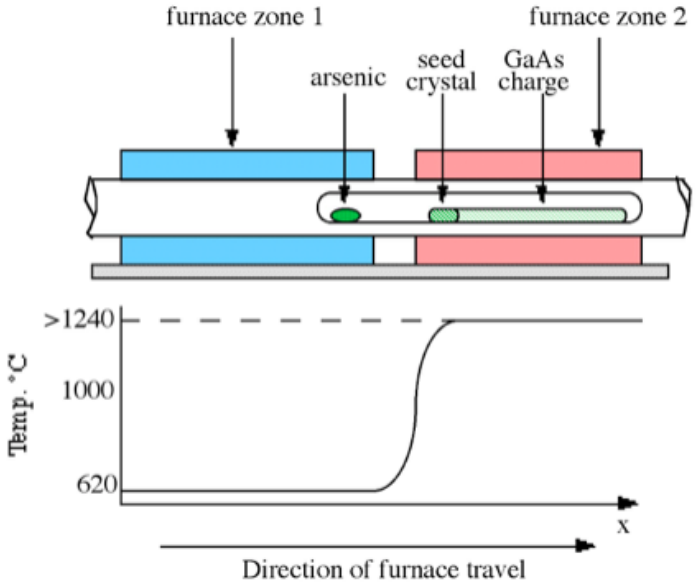


Figure 2.3. *Illustration of the setup in Bridgman technique [24].*

Finally, the grown ingot is mechanically ground to create perfect cylinder whose diameter is precisely defined and sawed into wafers, whose thickness depend on the diameter of the wafer [20]. The sawing is done with wire saw or with diamond-tipped inner-hole blade. Since sawing the wafers causes surface damage to the surface of the wafers, they are ground at least from one side or on both sides to create flat surface. Also, the edges of the wafers are rounded in order to prevent any chipping that might occur during processing. [20] Thickness obtained during sawing and grinding the wafer is not necessarily the final thickness of processed die or chip. For example in the laser manufacturing process, the wafers generally go through thinning process after the top side has been fully processed to achieve actual thickness needed for dies or chips to function properly. Additional semiconductor structures can be grown on top of the wafer with, e.g., molecular beam epitaxy (MBE) or with metal-organic chemical vapour-phase epitaxy (MOCVD) as shown in section 2.4.2.

2.2 Band gap of semiconductors

For GaAs as well as other semiconductors the band gap between conduction and valence bands is one of the most important characteristic of a semiconductor. For example, the band gap determines the wavelength, that can be absorbed or emitted by the semiconductor. In fact, semiconductors laser diodes cover a wide wavelength range from the beginning of visible light spectrum to the far infrared range [26]. Figure 2.4 shows the band structures GaAs compared to germanium and silicon. As can be seen from figure 2.4, GaAs have a direct bandgap, i.e., the lowest point of conduction band occurs at same **k**-value as the valence band highest point. Indirect band gap occurs, when the lowest point of conduction band and highest point of valence band are not in line, as can be seen in the case of germanium and silicon.

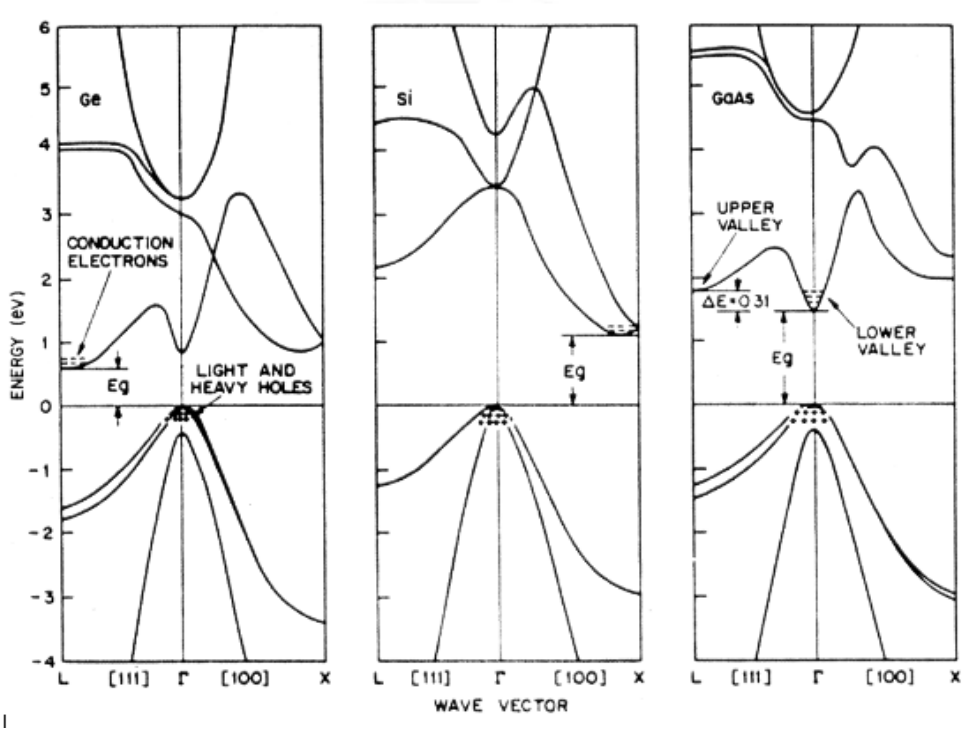


Figure 2.4. *Energy band diagram of germanium, silicon and gallium arsenide [27].*

The total energy and momentum must be conserved through any electronic transition. The magnitude of electron wavevector varies between $\pm\pi/\alpha$ within the first Brillouin zone, where α is the lattice constant. On the other hand, the magnitude of photon wavevector is given by $2\pi/\lambda$, where λ is the wavelength. Typically α is in the range of couple of angstrom and λ is in the range of hundreds of nanometers to couple of micrometers. As can be seen from the size difference of α and λ, electron have significantly larger wavevector magnitude, meaning that photon have very little effect on the electron and hence only vertical transition between bands are granted. In the case of direct band gap, these transitions can occur. If the band gap is indirect, transition from conduction band to valence band require interaction with third particle, which is called phonon. Since the interaction involves three particle, the probability of transition between the bands gets significantly reduced and hence, the stimulated emission is inhibited in indirect band gap semiconductors. [28]

2.3 Impurities

The electrical and optical properties of semiconductors are dependent on the impurities in the semiconductor material. For example, the conductivity of semiconductors and its optical properties depends strongly of the amount of impurities or dopants. The amount of dopants can be controlled extremely precisely and already a small amount of dopants can make a huge difference to the conductivity of semiconductor [20]. Semiconductors

can be divided in two groups based on the impurity level. These two groups are intrinsic semiconductors or pure semiconductors, which do not have impurities in their structure, and doped semiconductors or extrinsic semiconductors.

2.3.1 Intrinsic semiconductors

In case of intrinsic semiconductor, every electron in the conduction band must have come from the valence band since no external impurities are present. This requirement determines also the chemical potential to be in the middle of the gap between the valence band maximum and conduction band minimum. The missing states left by the transferred electrons at valence band are called holes. When electric field is applied, electrons can use holes to travel to the positive potential. When discussed about conductivity of semiconductors, the interest is often at the density of charge carriers. The electron density n can be expressed as [21]

$$n = \frac{1}{V}\int_{E_C}^{\infty} g_C(E) f(E,T) dE, \tag{2.2}$$

where V is volume, $g_C(E)$ is the density of states in the conduction band, $f(E,T)$ is Fermi–Dirac distribution and E_C is the energy of the conduction band minimum. The hole density p can be stated similarly as [21]

$$p = \frac{1}{V}\int_{-\infty}^{E_V} g_V(E)[1 - f(E,T)] dE, \tag{2.3}$$

where E_V is the maximum energy of valence band. Let's define E_V as zero and $E_C = E_g$, where E_g is the band gap. The dispersion of the conduction band can be written as [21]

$$E = E_g + \frac{\hbar^2 k_B^2}{2m_e^*}, \tag{2.4}$$

where $\hbar$ is the reduced Planck constant, k_B is the Boltzmann constant and m_e^* is the effective mass of electron. In case of free electron model, the density of states can be stated as [21]

$$g_C(E) = \frac{V}{2\pi^2}\left(\frac{2m_e^*}{\hbar^2}\right)^{3/2}(E - E_g)^{1/2} \tag{2.5}$$

Distribution of valence band can be stated as [21]

$$E = -\frac{\hbar^2 k_B^2}{2m_h^*}, \tag{2.6}$$

where m_h^* is effective mass of hole. The density of states of valence band is [21]

$$g_V(E) = \frac{V}{2\pi^2}\left(\frac{2m_h^*}{\hbar^2}\right)^{3/2}(-E)^{1/2}. \tag{2.7}$$

Naturally, density of states between the valence and conduction band is zero.

Since (2.5) and (2.7) cannot be solved manually, some simplification is needed. In room temperature $(E-\mu) \gg k_B T$ so Fermi–Dirac distribution can be simplified as [21]

$$f(E,T) = \frac{1}{e^{E-\mu/k_B T}+1} \approx e^{-E-\mu/k_B T}, \tag{2.8}$$

where μ is chemical potential and T is temperature. With this simplification, the integrals can be solved and the results are [21]

$$n = \frac{1}{\sqrt{2}}\left(\frac{m_e^* k_B T}{\pi\hbar^2}\right)^{3/2} e^{-(E_g-\mu)/k_B T} = N_{eff}^C e^{-(E_g-\mu)/k_B T} \tag{2.9}$$

and

$$p = \frac{1}{\sqrt{2}}\left(\frac{m_h^* k_B T}{\pi\hbar^2}\right)^{3/2} e^{-\mu/k_B T} = N_{eff}^V e^{-\mu/k_B T}, \tag{2.10}$$

where N_{eff}^C and N_{eff}^V is an effective number of states per volume for the conduction band and valence band, respectively.

If equations (2.9) and (2.10) are multiplied, it can be noticed that electron and hole concentrations are constant at any given temperature and it is independent of chemical potential's position as shown here:

$$np = 4\left(\frac{k_B T}{2\pi\hbar^2}\right)^3 (m_e^* m_h^*)^{3/2} e^{-E_g/k_B T}. \tag{2.11}$$

The relationship above is called the law of mass action. In intrinsic semiconductors the concentrations of n and p can be stated as

$$n_i = p_i = \sqrt{np}, \tag{2.12}$$

since the density of charge carriers are equal.

2.3.2 Extrinsic semiconductors

Since the carrier concentration is low in intrinsic semiconductors, the conductivity is improved by adding electrically active impurities. This is called doping and this process changes an intrinsic semiconductor to an extrinsic semiconductor. Impurities can be added during ingot growth, when the semiconductor material is melted. A quantity that identifies the distribution of impurities in melt-solid interface is the distribution coefficient

k_d as shown in equation (2.13):

$$k_d = \frac{C_S}{C_L}, \tag{2.13}$$

where C_S is the impurity concentration in the solid and C_L is the impurity concentration in the liquid, in equilibrium. [20]

The dopant atoms can be either donors or acceptors depending on whether they are donating electrons to conduction band or accepting electrons from valence band, respectively. These two types of doping are further called n- and p-doping depending on if they increase the number of electrons in conduction band or increase the number of holes in valence band, respectively. In doped semiconductors number of other carrier type (n or p) is greatly larger compared to other. The charge carrier density in doped semiconductors can be measured with Hall effect. The measurement provides information on the mark and density of the carrier. [21]

When considered the energy gap viewpoint after doping, it can be seen that impurities have created energy levels within the band gap. Donor atoms have created the so called donor level near the conduction band and acceptor atoms have created similarly the acceptor level near the valence band. The band structure of extrinsic semiconductors is shown in figure 2.5.

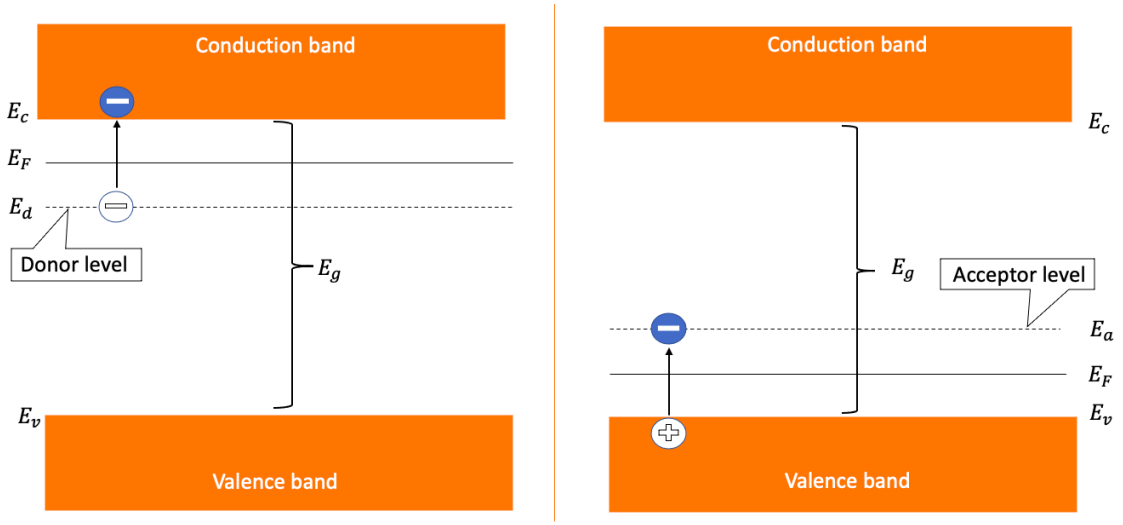


Figure 2.5. *Illustration of band structure of extrinsic semiconductors. Adapted from [29].*

In a case of donors, the Fermi level E_F is shifted upwards compared to intrinsic semiconductors and is about halfway between the donor level and conduction band. Acceptors, in turn, shift the Fermi level downward compared to intrinsic semiconductors. Fermi level is located halfway between the valence band and acceptor level in this case. [29]

Electrons can be easily excited from the donor level to the conduction band and these electrons are said to be the majority carriers. Similarly, since the acceptor level is close to the valence band, electrons in the valence are easily excited to the acceptor level and simultaneously create holes to the valence band. [29]

2.4 Principle of lasers operation and semiconductor lasers

The operating principle of the laser is based on light oscillation between two mirrors surrounding an active material. The active material is based on semiconductor material in case of semiconductor lasers. Other possible active materials used in lasers are, for example, gases or gas mixtures (e.g. HeNe-laser), liquid solutions in case of laser dyes and laser crystals or laser glasses (e.g. neodymium-doped yttrium aluminum garnet laser or Nd:YAG laser) [30]. Laser output beam is achieved, if the other mirror is partially transparent. The two mirrors, which reflects the light creates positive feedback for active material, which act as a amplifier after certain threshold condition is set. The setup for laser operation is shown in figure 2.6.

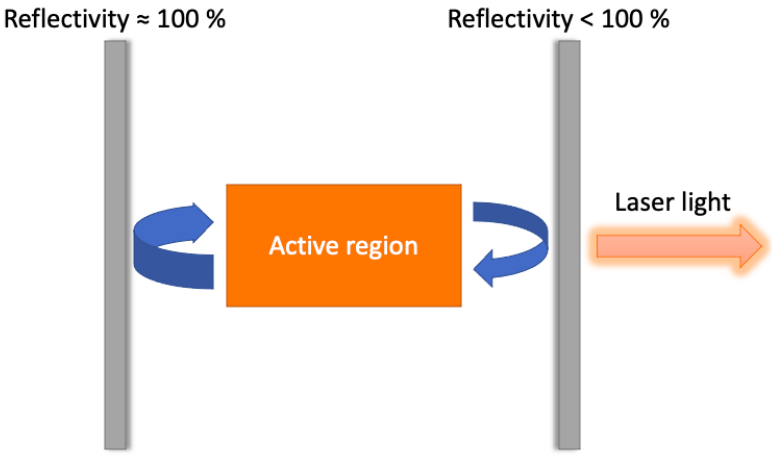


Figure 2.6. *Principle of laser operation. Adapted from [31].*

In addition, the active material needs some external energy source, e.g., light or electric current. This is called pumping and it is responsible for creating population inversion in given material. For semiconductor laser, the most convenient way of pumping is to use electric current in the forward direction and use the semiconductor laser in a form of diode [31, p. 406].

2.4.1 Spontaneous emission, stimulated emission and absorption

When considered two-level laser system with energies E_1 and E_2 like shown in figure 2.7, their population can be stated as

$$\frac{N_2}{N_1} = \frac{g_2}{g_1} e^{-\frac{E_2 - E_1}{kT}}, \tag{2.14}$$

where N_2 and N_1 are populations of upper and lower energy level, and levels are g_1-fold and g_2-fold degenerate in temperature T. Population inversion is achieved when $N_2 > \frac{g_2}{g_1} N_1$. The material will act as an amplifier, if a population inversion exists between the energy levels. In addition, the threshold condition must be fulfilled for lasing activity. This means that the gain of active material must compensate the losses in the laser system, e.g., mirror losses. At threshold, some critical inversion N_c is reached. Critical inversion can be stated as

$$N_c = -\frac{ln(R_1 R_2) + 2ln(1 - L_i)}{2\sigma l}, \tag{2.15}$$

where R_1 and R_2 are the power reflectivity of two mirrors, L_i is internal losses per pass in the laser cavity, l is the cavity length and σ is the absorption cross section. [31]

When critical inversion is reached, oscillation starts to build up from spontaneous emission. In fact, laser action needs total of three different processes to function. These are spontaneous emission, stimulated emission and absorption. These processes are illustrated in figure 2.7.

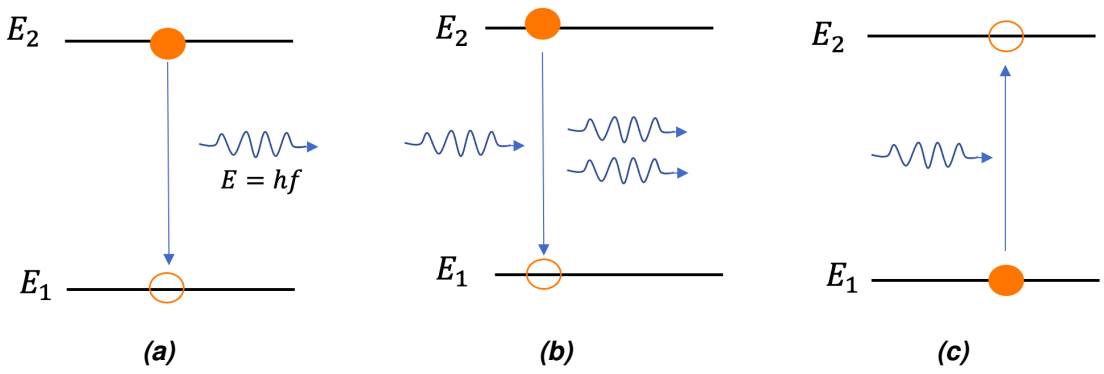


Figure 2.7. *Schematic illustration of different processes needed in laser action. a) Spontaneous emission, b) stimulated emission and c) absorption. Adapted from [31].*

During spontaneous emission, atom is initially at higher energy level and tend to decay to lower energy level. Energy difference between these to levels is released by the atom in form of photon, as shown in figure 2.7 a). In fact, spontaneous emission is responsible for initiation of the amplification process as it creates the first photon, that will cause stimulated emission. From this, formation of photons increases rapidly due stimulated emission. Atom may decay to the lower level also with non-radiative decay (NRD). In this

case, the energy emitted by the atom is delivered with other form than electromagnetic radiation, for example as heat absorber by the lattice. [31]

In stimulated emission, incident electromagnetic wave is needed to initiate the process. When incident wave has the same frequency as the atomic frequency, it can force the atom to go through transition from higher energy level to the lower energy level. Emitted electromagnetic wave from the atom transition adds to the incident one as shown in figure 2.7 b). Emitted electromagnetic wave has same direction and phase with the incident wave. [31]

In the case of absorption, atom is originally its lower energy level and is exited to higher energy level. For this to happen, some external stimulus is needed as shown in figure 2.7 c), where incident electromagnetic wave stimulates the transition, and is lost during the process. Also, the incident electromagnetic wave is required to have energy corresponding the energy difference between the energy levels for absorption to happen. [31]

It is stated that two-level system like in figure 2.7 cannot work in steady state due to two-level saturation [31]. In two-level saturation stimulated emission and absorption occurs in same rate and populations of the two levels are equal causing material to become transparent. In order to avoid two-level saturation, more energy levels are needed to produce the population inversion. Figure 2.8 shows three-level and four-level laser systems.

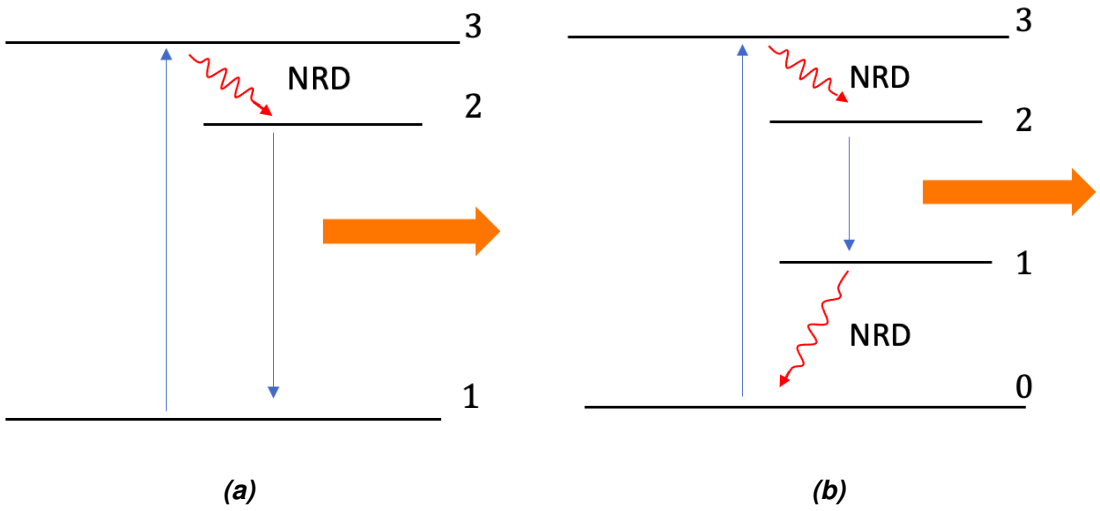


Figure 2.8. *Schematic of a) three-level and b) four-level laser. Adapted from [31].*

The idea is that the highest energy level remains empty since atoms quickly decays to near-by lower energy level by non-radiative decay. Since the energy level remains empty, it is therefore able to receive atoms from the lowest energy level. In four-level laser system, atoms quickly decay from level 1 to the lowest level, which is needed in continuous wave (CW) operation. From these two systems, four-level laser system is preferred since population inversion can be obtained more easily compared to three-level system. [31]

The operation of semiconductor lasers is well described by a 4-level laser. Electrons are excited from valence band to the conduction band with suitable pumping scheme. After this, electron will decay to lowest unoccupied level within this band. This decay is very rapid and occurs after around 1 ps. Simultaneously, electron in the valence band experiences a similar event: it decays to the lowest available level within this band and leaves a hole behind. Electromagnetic wave is emitted, when electron in the conduction band decays back to valence band and is recombined with hole in the valence band. [31]

2.4.2 Different laser diode structures

There are different possibilities for the laser diode structures. Firstly, the structure of the diode can be lateral or vertical. These are called edge-emitting laser diodes and vertical-cavity surface-emitting laser (VCSEL), respectively. Secondly, the laser structure can use the same material or different material between pn-junction. Edge-emitting and vertical-emitting laser structures are shown in figure 2.9.

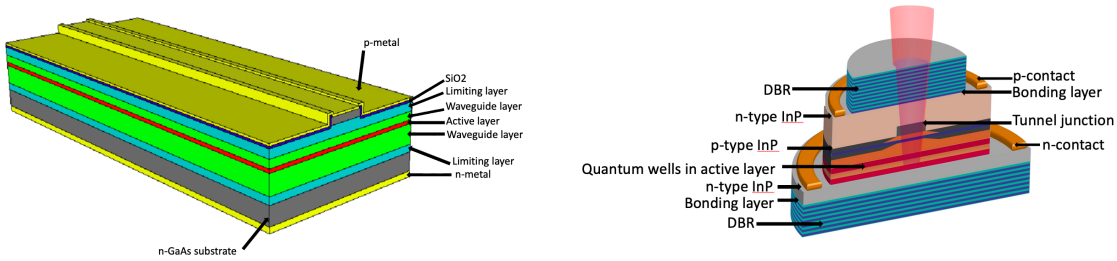


Figure 2.9. *Illustration of two different laser configurations. a) Edge-emitting laser diode and b) VCSEL. Adapted from [32] and [33].*

These two different laser structures have slightly different properties, when compared to each other. The edge emitting laser has an elliptical output beam, while the VCSEL has a beam that remains round even in the far field. In addition, the threshold current needed to operate VCSEL is significantly lower, when compared to edge-emitting laser. However, generally one VCSEL emitter cannot produce as high output power as one edge-emitting laser can. [31]

2.4.2.1 The double-heterostructure laser

The first laser diodes manufactured used same material for both side of one pn-junction. Therefore, such a structure is referred as homojunction lasers. Nowadays, homojunction lasers are not used since it can operate CW only at very low temperatures. [31] Limitations of homojunction laser can be prevented with double-heterostructure laser (also DH laser). Both homojunction and double-heterostructure lasers are edge-emitting lasers.

In the double-heterostructure, one material with low band gap is sandwiched between material with high band gap. Example of DH laser is shown in figure 2.10, where active GaAs layer is implemented between two AlGaAs layers.

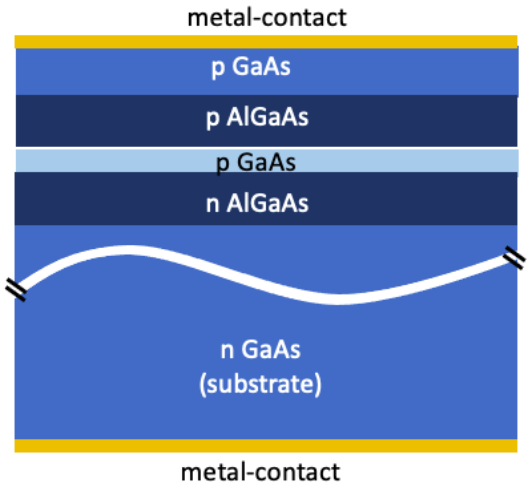


Figure 2.10. *Schematic of DH laser structure. Adapted from [20].*

With DH laser structure, injected charge carriers are confined to the active region and further helps to reduce the total current needed to drive the laser. In addition, the boundaries of GaAs and AlGaAs confines the generated light or, in other words, acts as a waveguide for the light due different refractive indexes. [20, pp. 459–462]

In order to take full advantage of DH laser structure, the lattice constant of active materials must be within 0.1 % to that of the surrounding layers. If this is not fulfilled, mismatched lattices causes compression or tension along the surface plane. After some critical thickness of the mismatched layer, strain energy give rise to formation of defects in the interface of different materials [20, pp. 19–20]. These defects will act as effective centers for electron-hole non-radiative recombination, which further decreases the efficiency of laser structure. For example, with quaternary compound $In_{1-x}Ga_xAs_yP_{1-y}$ lattice matching is done with suitable x/y ratio in the alloy. However, in some cases there is no need for lattice matching since the lattice constants are already very close in value, like with GaAs (0.564 Å) and AlAs (0.566 Å). [31, pp. 408–413] Since GaAs and AlAs have very close value lattice constants, the composition of ternary compound $Al_xGa_{1-x}As$ can be choose to fit the particular need for device requirement [20, p. 38]. Thus, the designing of the laser structure and selecting semiconductor materials for the structure plays an important role in the field of diode laser development.

In the DH laser, the carrier confinement and the optical waveguide depend on the same heterojunctions. For optimal operation, it would be beneficial, if narrower carrier confinement region and wider waveguide region is adapted. This kind of structure is called separate confinement laser. Narrower carrier confinement region keeps the charge carri-

ers in high recombination region, i.e., where the band gap is smallest. Wider waveguide is achieved with refractive index step in heterojunction that differs from the refractive index of confine carrier heterojunction. [20, pp. 460–462]

2.4.2.2 Vertical-cavity surface emitting lasers

In VCSEL, the mirrors of the laser is replaces by distributed Bragg reflectors or DBRs. DBR structure confines several partial reflectors, that are spaced in a way that the reflection is constructive. In order to achieve constructive reflection, thickness of the mirrors needs to be one quarter of the emitted wavelength. The bottom DBR can be constructed, for example, with alternating AlAs and GaAs layers. The top DBR, on the other hand, can be composed of alternating dielectric layers, like ZnSe and MgF. [20, 31]

Typically VCSEL have very narrow active material between the mirrors, meaning that obtained gain is also quite small. Small gain is compensated with relatively high reflective mirrors. In addition, decent output power can be achieved with high number of VCSELs in one array. The size of one VCSEL-structure is extremely small, when compared to edge-emitting laser. Due to the small size of VCSEL, its cavity is also very short. With short cavity, the laser modes are separated, meaning that single-mode operation can be achieved easily. The narrow outlet results in small cross-sectional area, which in turn, causes VCSELs to oscillate on TEM_{00} mode even if the current used is clearly higher than the threshold current. Furthermore, threshold current needed to operate single VCSEL is very small due small losses [31, pp. 423–425].

3. THINNING OF SEMICONDUCTOR WAFERS

A good surface quality of semiconductor wafers is essential characteristic in semiconductor industry. In laser industry, various structures are processed on the top side surface of the wafer by the means of lithography. This is why the uniformity of the wafer and its surface is particularly important, since defects or inequalities on the wafer surface can produce lithography errors. On the other hand, the bulk material removal takes place on the bottom side of the wafer. Again, the processed wafer surface is desired to be as smooth and stress-free as possible to ensure high-quality further wafer processing like metallization and wafer or die bonding.

Usually the wafer thinning process contains two phases: bulk material removal or coarse thinning, where most of the wafer material is removed, and removal of subsurface damage layer caused by the thinning process. In the thinning process, the cutting edge of abrasive grain penetrates into the material, which leads to formation of radial and lateral cracks. For this to happen, grains need to be harder than the material machined. Formation of micro-cracks is typical behaviour of brittle materials, like GaAs and other semiconductors, since material separation start to dominate when penetration depths is increased. [34] Material removing methods are shown in figure 3.1.

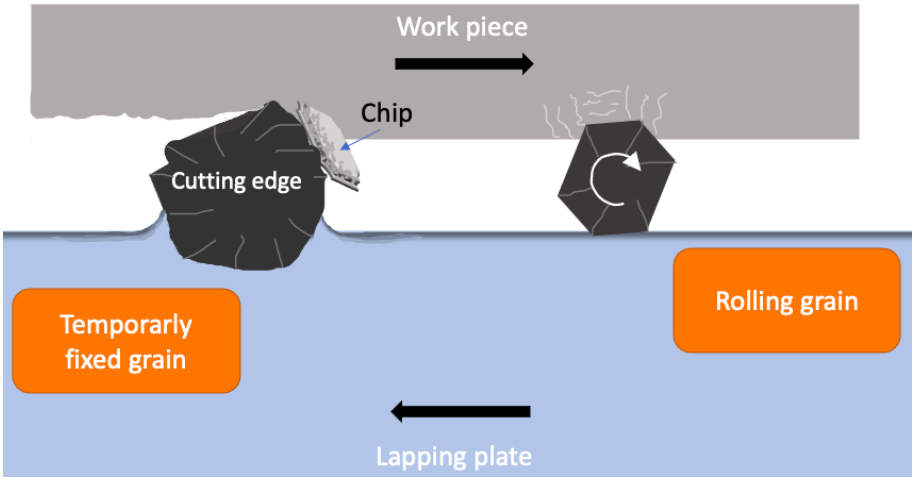


Figure 3.1. *Illustration subsurface damage caused by thinning process. Adapted from [34].*

High brittleness is material property, which directly affects its workability and machinability due material's low fracture-resistance and hardness of the material [34]. Usually, individual micro-cracks formed during coarse thinning process are invisible to naked eye. However, due to these micro-cracks the surface of the thinned wafer seems matte.

The damaged layer depth is comparable to the size of the abrasive grain used during coarse thinning [18]. The depth of the damaged layer can be measured with, e.g., X-ray topography or interference contrast microscopy [16]. By measuring the depth of the damaged layer, it is possible to find out how much material should be removed from the surface of the wafer to achieve damage-free wafer.

Commonly used thinning methods are grinding and lapping, whose operation is based on the mechanical removal of material from wafer surface, with help of abrasive grains [9, 16]. The key difference between the two is that grinding uses a grinding wheel, where abrasive grains have been bonded, and lapping uses free abrasive grains on the lapping plate [35]. Since abrasives are bound to the grinding wheel, they are able to cut deeper to the machined wafer compared to case, where abrasive grains can roll freely [36]. When grinding takes place from the back of the wafer, the process is commonly referred as back-grinding. [37] Similarly, lapping can be referred as back-lapping in case there is a need to specify on which side of the wafer thinning occurs. Grinding generally has the highest thinning rate and therefore it is widely used for bulk material removal technique [9]. Lapping, on the other hand, is slower process compared to grinding [37]. However, it creates better surface compared to grinding in micro scale but at the nano-scale grinding has a better end result in surface roughness [38].

In general, after coarse thinning step the wafer surface is matte due micro-cracks [17]. In order to have stress-free wafer with high-quality surface, subsurface damage layer needs to be removed. This can be done with for example with polishing or etching. During this step, the thickness change of the wafer is very small. In fact, both polishing and etching focuses only on near-the-surface activity. After subsurface damage layer is removed, the surface is reflective or mirror like [17]. The resulting wafer after removing the subsurface damage layer is stronger and more responsive [39]. If the wafer suffers from mechanical stress, it can cause wafer to bow. Illustration of wafer bow is shown in figure 3.2.

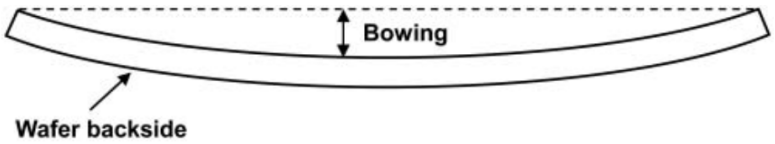


Figure 3.2. *Illustration of wafer bow [9].*

Wafer bow refers height difference between center of a wafer and edges of a wafer. Wafer bow can be defined as positive bow or negative bow. In negative bow, the edges of the

wafer are higher than its center [9], as also shown in figure 3.2. In general, wafer bow is is caused by compressive and tensile stress affecting on the wafer. These tensions rises from different sources, like mismatched lattice between different material layers and subsurface damage [9, 20]. Wafer bow is noticeable especially in the case of thin wafers. The mechanical strength of the wafer decreases significantly as the wafer gets thinner, making bowing more apparent in a case, where mechanical stress is present in the thin wafer [9]. In addition, handling of bowed wafers becomes particularly difficult or even impossible in the case of automated equipment due to changed shape of the wafer. When additional wafer bow is present, there is a high risk of the wafer breakage during handling and processing [16]. Naturally, wafer breakage is unwanted situation, since it decreases the yield dramatically.

3.1 Grinding

Grinding removes bulk semiconductor material with help of grinding wheel. Abrasive grains are attached to the grinding wheel. Generally, the grinding process consists of three different steps: coarse grinding, fine grinding and polishing. Coarse grinding has the highest thinning rate and polishing has the lowest as the coarse grinder has larger abrasive particles included and fine grinder has smaller abrasive particles, respectively.

3.1.1 Different grinder types

Grinders can be divided to three types, i.e., Blanchard type, creep-feed type and in-feed type, of which Blanchard type and creep-feed type have the same basic structure. Blanchard type and in-feed type grinder are shown in figure 3.3.

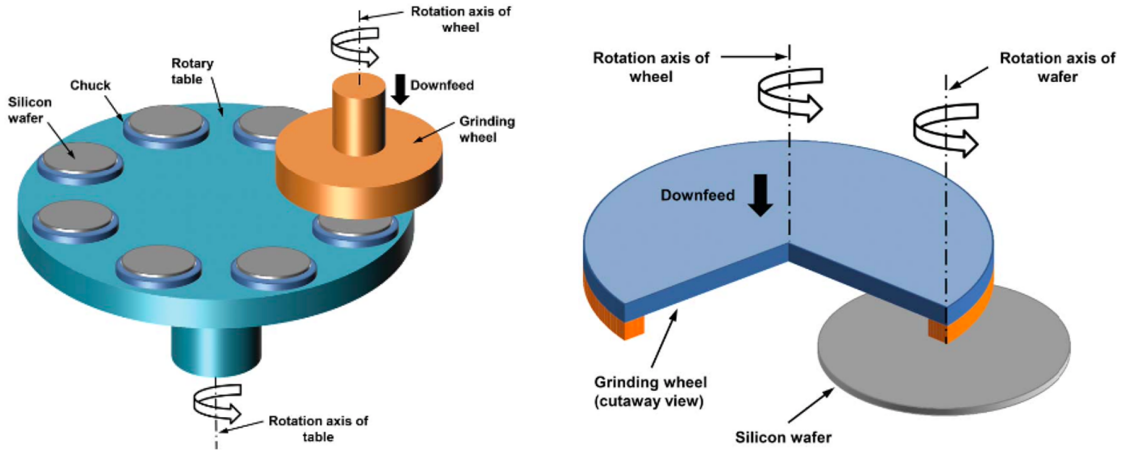


Figure 3.3. *Different grinder types. a) Blanchard type grinder and b) in-feed type grinder. Adapted from [9].*

Blanchard grinder is shown in figure 3.3 a). Blanchard-type grinder has several spots for wafers and therefore several wafers can be machined during same run. In this type, wafers do not rotate around their own axis. Only the grinding wheel, which has a cup-like shape, rotates. The rotation axis is located in a way that it is aligned with wafer centers. The grinding wheel is fed above the wafer with certain feed rate. Wafers are attached to rotation table, which feeds the wafers each in turn for grinding wheel. [9]

A creep-feed grinder is quite similar with Blanchard-type grinder as it has also several spots for wafers and wafers do not rotate around their own axis. The significant difference between the two is, that creep-feed grinder has several grinding wheels with different grain sizes ranging from coarse to fine. In addition, it should be taken into account that the space between two wafers must be spacious enough to fit all the grinding wheels used. For example with three different grain size wheels, there should be enough space for three grinding wheel between two wafers. Generally, creep-freed grinder types have better control over the target thickness. However, both produce poor total thickness variation (TTV). [9]

The third type, the in-feed grinder, can produce better TTV compared to other two types. In this type the wafer and the grinding wheel rotate simultaneously around their own axis. In addition, the grinding wheel has a offset to the wafer machined by the length of wheel radius relative to the rotation axis for the wafer. This produces contact length, that is constant during the process and hence improving TTV. [9] In-feed type grinder is shown in figure 3.3 b).

3.1.2 Surface damage caused by grinding

Grinding creates several different micro-cracks to the wafer structure [40]. The incidence of various micro-crack was investigated in the case of silicon wafer [40]. Different micro-crack types created during grinding are show in in figure 3.4.

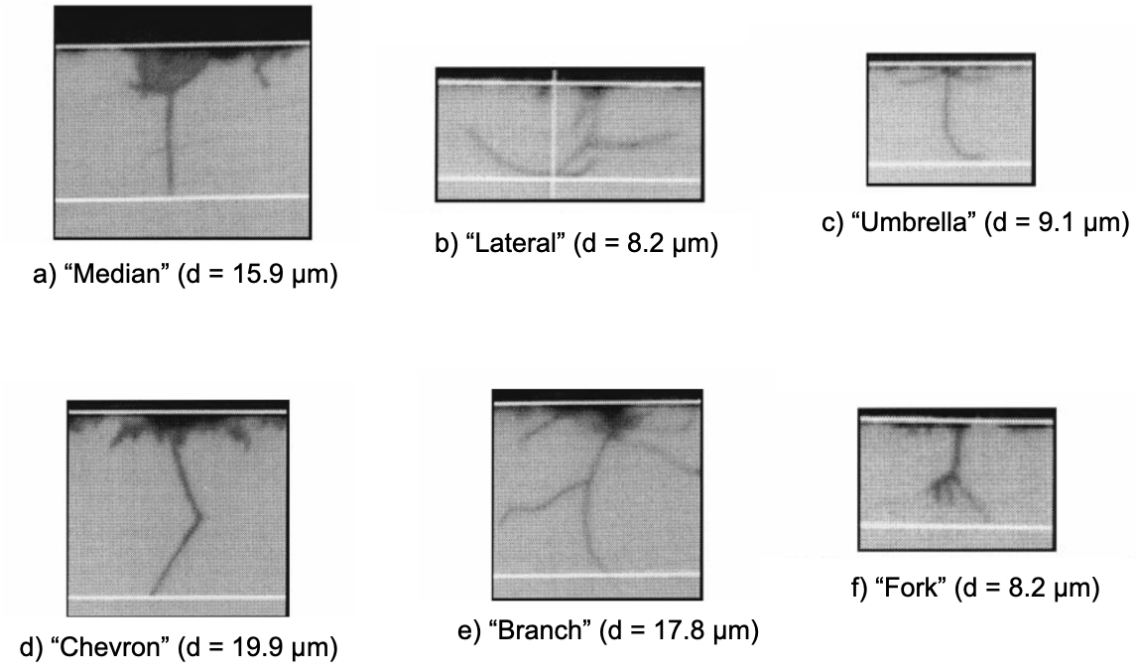


Figure 3.4. *Several micro-cracks types present in silicon after grinding. Adapted from [40].*

It is discovered, that the depth of the crack is dependent of the used grit size and it is independent on the location on the wafer. In fact, the crack depth is approximately half of the used grit size. [40] Micro-cracks are removed by fine-grinding and polishing. These processes have lower thinning rate compared to coarse grinding as shown in figure 3.5.

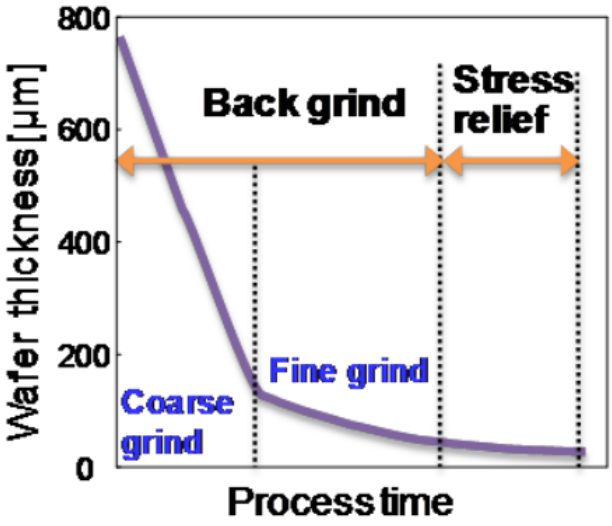


Figure 3.5. *Thinning rates during back-grinding [41].*

In a case, where abrasive grains are bound, they are able to cut deeper to the machined material, resulting deeper micro-cracks compared to free-rolling grains in similar condi-

tions [36]. With combination of coarse grinding, the fine grinding and final stress relief, as small as 0.5 μm TTV can be achieved when at least 50 μm is removed with fine grinding method and 1–5 μm is removed with stress relief method like chemical mechanical polishing [41].

3.1.3 Grinding modes

Grinding can occur with two different modes: ductile mode and brittle mode. These two modes can occur in same brittle material. From these two modes, ductile mode is preferred since it causes less subsurface damage. In ductile mode machining, the area under influence of abrasive grain experiences simple plastic deformation. The transition between these two modes can be controlled by controlling the grinding conditions. Critical parameters during grinding in order to achieve ductile mode is that the machining depth should be less than 1 μm, usually ranging from 50 nm to 1 μm. In addition to cut depth, high loop stiffness, full flood coolant, high-accuracy machine tools with resolution around 1.25 to 10 nm are needed to produce ductile mode machining on brittle materials. In a case of 100 % ductile mode grinding, mirror like surface, i.e., surface roughness less than nanometre can be obtained. Since these ultra-precision machine and cutting tools are quire expensive, they are not widely used worldwide. [42]

However, by fine-tuning the grinding parameters, a partial or near-ductile mode can be achieved, at least when silicon is ground. It was found that the grit size and grit concentration were important parameters when aiming for partial ductile mode. [42] Since the thinning tests in this theses are done using lapping, grinding parameters are not discussed in detail here. However, many parameters of the grinding process follow the same behavior as the parameters of the lapping process, so it could be concluded that the most suitable parameters of the lapping process are also suitable for the grinding process [34].

3.2 Lapping

Lapping can be defined as a surface finishing process that utilizes loose abrasive grains in together with a lapping plate to produce high flatness, parallelism and exact wafer thickness. In some cases, the difference to grinding is purely kinematic since lapping can be thought to be very passive form of grinding [43]. On the other hand, with low processing rate, it is possible to achieve the desired thickness with great precision [44]. Lapping uses relatively low forces, which makes it an excellent alternative for machining brittle materials [45]. In addition, no thermal damage is caused to the machined wafer during lapping, since the slurry used acts also as a cooling lubricate. This is not the case with grinding, and therefore cooling lubricants are needed. [34, 45]

Lapping uses material like aluminum oxide or other metal oxides like SiO_2 and CeO_2

as the abrasive grain mixed with water, oil or another liquid substance to mechanically remove the bulk material from the wafer. In addition to metal oxides, also other materials like SiC or diamond are suitable abrasive materials [44]. The mixture of abrasive grain and liquid is called slurry. The slurry affects the wafer to be machined between the wafer and the lapping wheel.

The sharp edges of the grains, i.e., cutting edges will penetrate the wafer material to depth depending on the grain size. Usually this penetration depth is around 5 % to 10 % of the average grain diameter. In addition, the grain is also penetrated to the lapping plate [45]. Semiconductor material is removed from the bulk via breakaway of microscopic chips after formed micro-cracks connects. [34] Similarly, chips can be detached from the lapping plate by shearing [45]. For this to happen, abrasive grains need to have enough energy in order to penetrate the machined wafer surface [43]. Through the work of the grains, the flatness of the lapping plate can be transferred to the machined wafer [45]. For this reason, lapping plate flatness is very important property during lapping.

Machined wafer is attached to carrier or jig. The jig and the lap tool moves parallel to each others forcing grains to a rolling movement between the two. This rolling causes fine material removal. [43] Schematic of lapping equipment and principle is shown in figure 3.6.

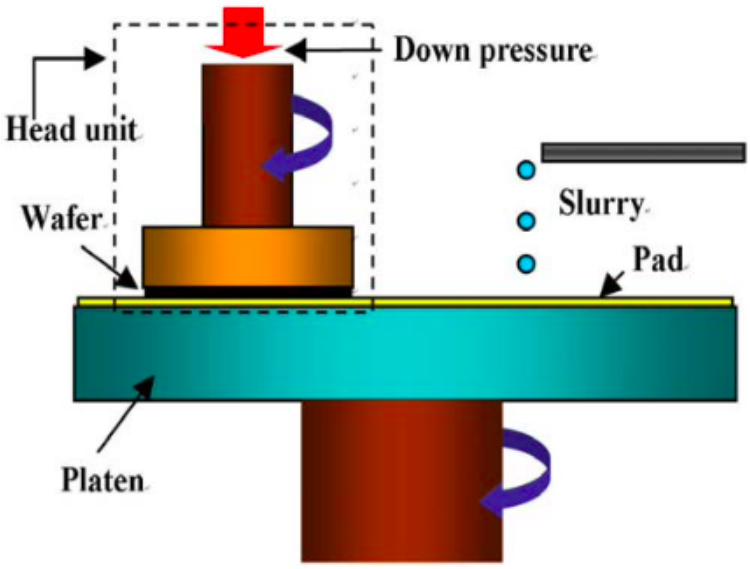


Figure 3.6. *Lapping equipment in use [46].*

The slurry is pored on lapping plate. The machined wafer is attached to the jig with help of vacuum. Lapping has an averaging effect meaning that the highest material removal is obtained at points higher than their surroundings [43]. This leads to relatively good uniformity and flatness. Generally, lapping is consider as gentle process producing wafers with low-stress levels [43]. During lapping, the machined component should not be in direct contact with the lapping plate in order to prevent uneven lapping results.[43].

3.3 Parameters used in lapping

Several factors affect the lapping outcome. Firstly, the material being processed affects on the lapping process. It, e.g., determines the type of slurry used during lapping process. With harder machined material also harder abrasive grains are needed. In addition, the plate material should also be considered. Generally, it is preferred to use softer plate compared to machined material. [43] Overall, lapping pressure and lapping speed can be consider as main parameters in lapping process [34].

3.3.1 The lap and lapping plate speed

When harder lap is used, it can cause more scratches compared to softer lap. This is because harder lap resists abrasive grains to be embedded to it. This, in turn, affects the rotation of the grains as they tend to roll more than slide. This causes material removal to occur through stress-induced micro-fracture. With softer lap, the material removal occurs by plowing and results finer surface. In optoelectronic materials, glass is generally used as lap material. [36]

The lapping speed should be selected in a way that the surface of the component does not experience oscillation, vibration or any other unwanted movement [43]. The component should move as smoothly as possible on the lapping plate in order to guarantee the best possible result. The lapping speed affects on material removal rate. However, high plate speed should be avoided since it produces excessive centrifugal forces which further force the grains to move towards the edges of the wafer and lapping plate [34]. In addition, high lapping speed will cause slurry to splash, meaning uneven slurry input [44].

3.3.2 Lapping pressure

Lapping pressure can increase material removal rate, if the pressure is relatively low. In a situation, where the pressure continues to increase, the material removal rate will start to decrease. If the pressure is further increased, the rate of material removal will start to increase again. [45] The effect of pressure to the material removal rate is shown in figure 3.7.

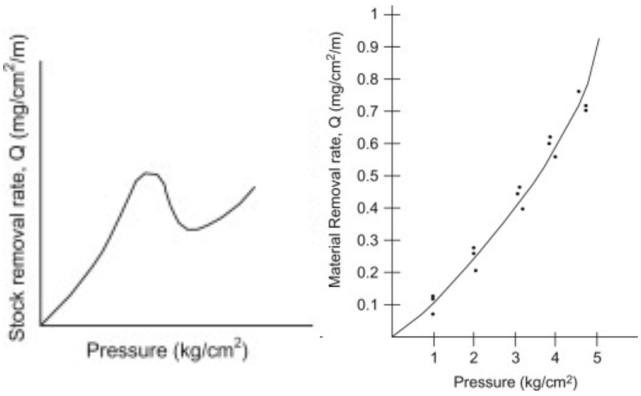


Figure 3.7. *Material removal rate dependence of pressure. Adapted from [45].*

Material removal rate decrease is due to breakage of lapping grains as the pressure is increased [34]. It can be seen, that the dependence is not completely linear even with relatively low pressure range. In addition, in case of wafers with thickness of 200 μm or below, the pressure acting on the wafer should be kept low, or even reduced, to prevent cracking. [17] With higher pressure, the chance of rubbing the component directly to the lapping plate is increased, which is unwanted situation [43].

Furthermore, with free abrasive, the used pressures during processing are usually lower compared to bound abrasive case, like grinding. This is due to the fact that with free abrasive, the grains are subjected to the machined wafer with higher uncertainty, causing that the grains may experience high pressures locally. In bound abrasives the pressure is divided more evenly. [43]

3.3.3 Abrasive grain used during lapping

Typical abrasive size is between 5 μm and 20 μm [18]. The size of the abrasive grain is directly related to material removal rate and surface roughness. With larger grain size, also the material removal rate is higher, and respectively with smaller grain size the material removal rate is lower. On the other hand, smaller grain produces lower surface roughness compares to larger grain size. In addition to actual size of the grain, also concentration of abrasive is important. Concentration can be though to be number of grains in contact with the machined wafer surface. Concentration changes therefore directly affects on load distribution throughout the wafer. In other words, local grain concentration has a lower effective load compared to a low grain location. [36]

3.3.4 Types of abrasives

Common abrasive materials are silicon carbide, aluminum oxide and diamond. Aluminum oxide is suited for general lapping having low surface roughness, and silicon carbide is

suited for fast material removal [36]. The choice between different abrasives depends on intended use, and the material to be machined. Hard abrasive, like diamond, causes sub-surface damage with greater depth. [47] Generally, larger and harder grains will produce surface with higher roughness [36]. In semiconductor industry, aluminum oxide is widely used since it is softer material and has lower cost compared to others [43].

Diamond is the sharpest and hardest known abrasive. It can be obtained naturally or synthetic. Both natural and synthetic diamond has hardness of 10 on the Mosh scale meaning of hardest known material. Table for different material hardness on Mosh scale is shown in table 3.1. Since diamond is very hard material, it is best suited for lapping other very hard materials like tungsten. [36]

Table 3.1. *Different materials and their hardness in Mosh scale. Adapted from [36, 48, 49, 50]*

Abrasive	Mosh scale
Diamond	10.0
Cubic boron nitride (CBN)	9.9
Silicon carbide	9.5
Aluminum oxide	9.0
38 White aluminum oxide	9.0
Chromium oxide	8.5
Garnet	8–9
Quarts	7
Aluminas (hydrates)	5–7
GaAs	4–5
Ge	6
Si	6.5

Aluminum oxide is a good option for lapping in a case, when the lapping conditions are rough. It is fused abrasive with relatively hard crystal structure. In addition, aluminum oxide grains do not break easily. Aluminum oxide can be used for lapping also in unfused form or hydrate-calcined form. This materials is relatively soft compared to its fused relative, and it can be used for polishing also.

3.4 Polishing of semiconductor wafers

The purpose of polishing is to finish the surface to its mirror like quality. During this step, the geometry of the machined wafer will hardly change. Chemical mechanisms can be utilized to remove material from machined wafer surface. In fact, polishing process can be purely chemical polishing, e.g., in form of wet or dry etching.

Different polishing processes can be divided into four categories accordingly to used abrasive grain size and carrier materials. This categorization is shown in figure 3.8.

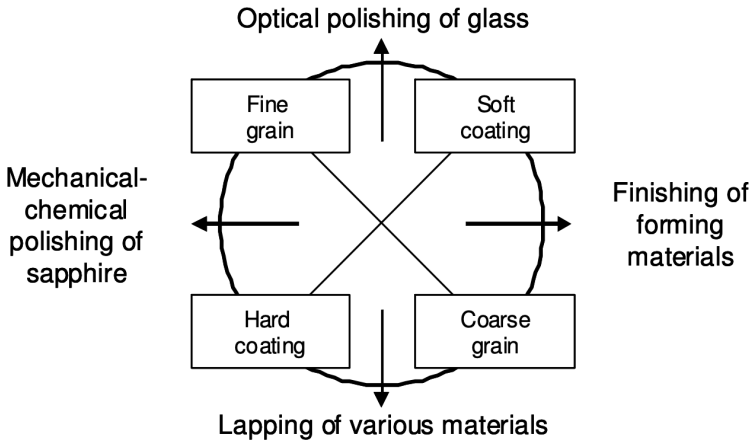


Figure 3.8. *Four different categories for polishing [34].*

Polishing principle is similar to lapping principle. When polishing is done with abrasives, very fine grain size, e.g., colloidal silica grain size of 0.125 μm or aluminum oxide 0.3 μm can be used to achieve the finished surface. The damaged layer depth can be further reduce if the load on the wafer is reduced as the target thickness approaches, and at the end the process the load experienced by the wafer is held low. [47] In addition, soft pad is used as an abrasive carrier when polishing with slurry [44]. Abrasive carrier takes care of even distribution of slurry on their surface, and binds the grains loosely [34].

Since the size of abrasives used in polishing is small compared to size of abrasives used in lapping, abrasive effect is limited. This results directly decreased material removal rate. Because of this, the physical and chemical interactions between abrasives, workpiece and carrier material become more important. These interactions are abrasive removal hypothesis, yield hypothesis, chemical hypothesis and friction wear hypothesis. Of these four, abrasive removal hypothesis has the same principle as lapping. Similarly, as in lapping, abrasive removal is possible in a case where abrasive particle is harder material compared to workpiece material. The difference between lapping is the smaller scale due smaller grain size. [34]

The yield hypothesis is applied to a situation where abrasives are a softer material compared to the material being machined. According to the yield hypothesis, pressure is introduced to contact point between polishing pad or foil, polishing grains and machined material. This pressure increase causes temperature increase due relative movement between the three element in contact. The temperature can be up to several hundred degrees Celsius. The high temperature will cause a local plasticization and melting of any roughness peak in the area. The molted material flows into roughness valley and finally will solidify. [34]

3.4.1 Other polishing methods

Etching is effective way to achieve smooth and clean semiconductor surface that is needed in semiconductor industry [19]. In a case of III–V semiconductors like GaAs, bromine containing etching solutions are widely used. For example, bromine-methanol (Br_2CH_3OH) can give the finished, mirror like surface for GaAs. [19] The polishing process can be a mixture of chemical and mechanical mechanisms. Chemical mechanical polishing or CMP utilizes both of these mechanisms to produce nano-level smooth surface for GaAs wafers [51].

4. METHODS AND THE LAPPING EQUIPMENT

This chapter introduces the equipment used in this thesis for lapping and polishing processes. In addition, sample preparation is reviewed in detail. The lapping is done to decrease series resistance and therefore, increase wafer's thermal conductivity and to speed up signal transmission across the device [52]. In addition, with thinner wafers also smaller dies can be manufactured.

4.1 Sample preparation for thinning process

The samples used in this thesis were 3" GaAs wafers with initially both top and bottom sides polished. The different sides of the wafer were determined visually from the initial quality of the surface by selecting the more scratched side as the bottom side and the cleaner side as the top side. The initial thickness of the wafers was about 600 μm. The wafers had both a major flat and a minor flat.

The surface of the sample is cleaned using acetone and methanol. The cleanliness of the surface was checked by microscopic examination. After obtaining the approved purity, sample preparation is continued with SiO_2 growth. Total of 600 nm of SiO_2 was grown on top side of GaAs substrate by Oxford Instruments plasma-enhanced chemical vapor deposition (PECVD). The quality of the grown SiO_2 was checked by microscopic examination. Once the top side has been processed, the sample thickness is measured. The measuring points are shown in figure 4.1.

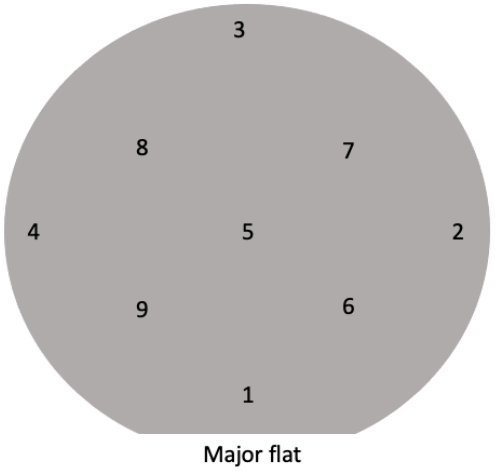


Figure 4.1. *Used measuring points during different process phases.*

The major flat is located towards the user when measurements are taken. The thickness measurements were performed with the processed top side against the reference plane to ensure same orientation compared to the thinned wafer. Thickness measurements were performed using Logitech contact measurement gauge (CG10). CG10 is a measuring system for linear dimensional measurement applications. The accuracy of CG10 can be as low as to 1 μm over its measuring range of 10 mm [53].

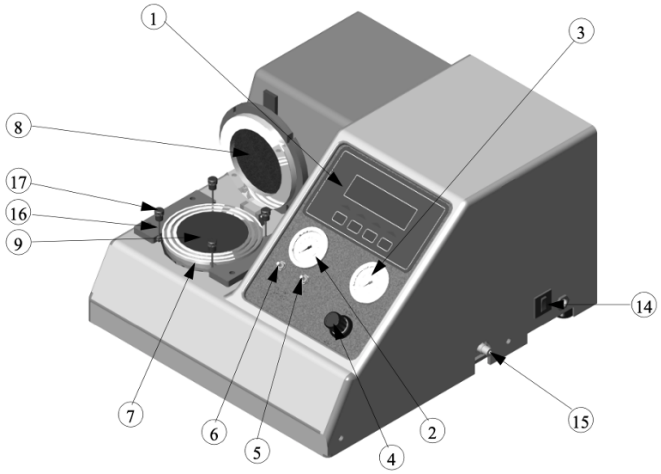
Preparation for wafer bonding begins by applying a photoresist to the top side of the wafer. The purpose of the photoresist is to protect the top side of the wafer, as the top side has to be mounted against a glass substrate during back-lapping. A total of 4.5–4.8 ml of photoresist is applied to the wafer using a spin coater. The flatness and quality of the photoresist is checked visually and any excess resist on the back of the wafer is removed using acetone. The sides of the wafer are also cleaned. Finally, an area about 1 mm wide throughout the top side edges of the wafer is removed from the photoresist with acetone to prevent etching materials to reach the photoresist during the polishing by wet etching.

The wafer is now ready to be bonded to glass substrate. The glass substrate will provide support to the wafer and will keep the wafer in one level during lapping and polishing. Bonding can be divided in two phases: pre-bonding and actual bonding. The pre-bonding is done by hand using wax, hotplate and tweezers. The wax is applied to a heated glass substrate over the entire area of the wafer or sample. The aim is to achieve as even layer of wax as possible. After this, the wafer is placed on wax top side against the wax, and the pressure is applied to the wafer with tweezers. With external pressure, any excess wax is forced to move from the center of the wafer toward its edges. The goal is to have even layer of wax with thickness of around 15 μm or less. The wax thickness is verified by measuring the thickness of pre-bonded wafer and compared measured values to unbonded thickness values.

After the pre-bonding phase has been successful, the pre-bonded wafer is placed on Logitech WBS1 unit, which handles the final bonding of the wafer. After bonding, the sample thickness is measured, and measured values are compared to unbonded values. The wax thickness should be < 5 μm. After this, the wafer is ready to be thinned.

4.1.1 Operating principle of WBS1 unit

Schematic of bonding unit used in this thesis is shown in figure 4.2. The WBS1 unit is suitable for glass substrates with either 83 mm or 105 mm diameter. In this work, 3" wafers were processed, resulting in the use of 83 mm glass substrate. The sample is placed on sample chamber (number 9 in figure 4.2) after pre-bonding. Couple of filter papers are placed on top of the sample to soak up any excess wax, which exits between the wafer and the glass during bonding. The chamber is closed using thumb screws shown in figure 4.2 by the number 17. After closing the chamber and sealing it with O-ring(s), the chamber is evacuated. Pressure of $1 \cdot 10^{-1}$ mbar can be achieved during evacuating. The pressure is applied to the wafer with using diaphragm (number 8 in figure 4.2). [54]



1. Process Data display and touch panel controls
2. Vacuum/pressure gauge
3. Applied pressure gauge
4. Air supply regulator
5. Chamber air/positive pressure inlet
6. Sample air inlet
7. Bonding head
8. Bonding diaphragm
9. Sample chamber
10. Vacuum connector (Figure 1)
11. Oil vapour outlet (Figure 1)
12. Water inlet*
13. Water outlet*
14. Mains On/Off switch (Figure 2)
15. Positive pressure inlet connector (Figure 2)
16. Swing bolt (Figure 2)
17. Thumb screw (Figure 2)

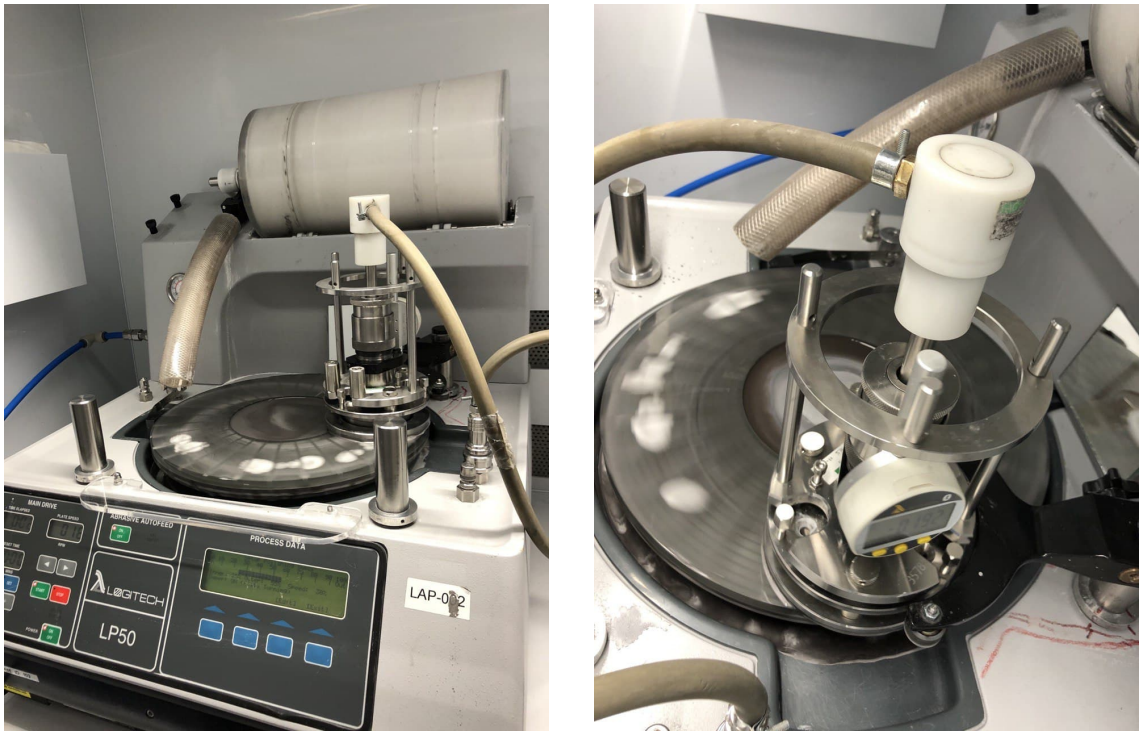
Figure 4.2. *Schematic of WBS1 unit. Adapted from [54]*

During bonding cycle, temperature of the sample chamber is raised to the preset point, which is determined by the used. The temperature should be selected in a way, that is is near wax melting point. In this temperature, the wax will get softer, but do not liquefy. After the correct temperature is reached and evacuating is completed, soak time will be started. This is a 10 minute delay, which is required to ensure a stabilized temperature throughout the head and wafer, and the wax to outgas [54]. When soak time is finished, atmospheric or positive pressure is applied in a space above diaphragm at a controlled rate. This causes diaphragm to get in contact the wafer and press the wafer into the softened wax. The pressure to the wafer caused by diaphragm is held through bonding

time. After bonding time, bonding head (number 7 in figure 4.2) is cooled in a controlled way using water or oil circulation while pressure is held on the sample, until the sample chamber reaches temperature of 40 °C. Finally, the chamber evacuation is released at a controlled way. [54]

4.2 Lapping and polishing unit LP50

Lapping, as well as polishing processes were performed using Logitech LP50 equipment. Usually, the lapping is carried out at the end of device fabrication process once the top side of the wafer has been processed. Figure 4.3 shows the main body of LP50 as well as other relevant parts needed in the total thinning process.



(a) *(b)*

Figure 4.3. *a) The lapping and polishing is done with Logitech LP50 auto precision lapping and polishing machined. b) The wafer has been attached to precision jig.*

The LP50 auto precision lapping and polishing machine can achieve an accuracy of up to $\pm$ 1 μm of the target thickness [55]. The device provides three workstations, of which two workstations have a static arm. The third workstation, in turn, can be operated with sweeping arm mode. During this thesis the sweeping arm was used during lapping and polishing.

Suitable jigs for the device are standard PLJ2 lapping or PP5 polishing jigs, or larger PLJ7 or PP6 jigs, respectively [55]. In this thesis, PP5GT jig was used during lapping and polishing. In the lapping process, the bonded sample to be processed is mounted to

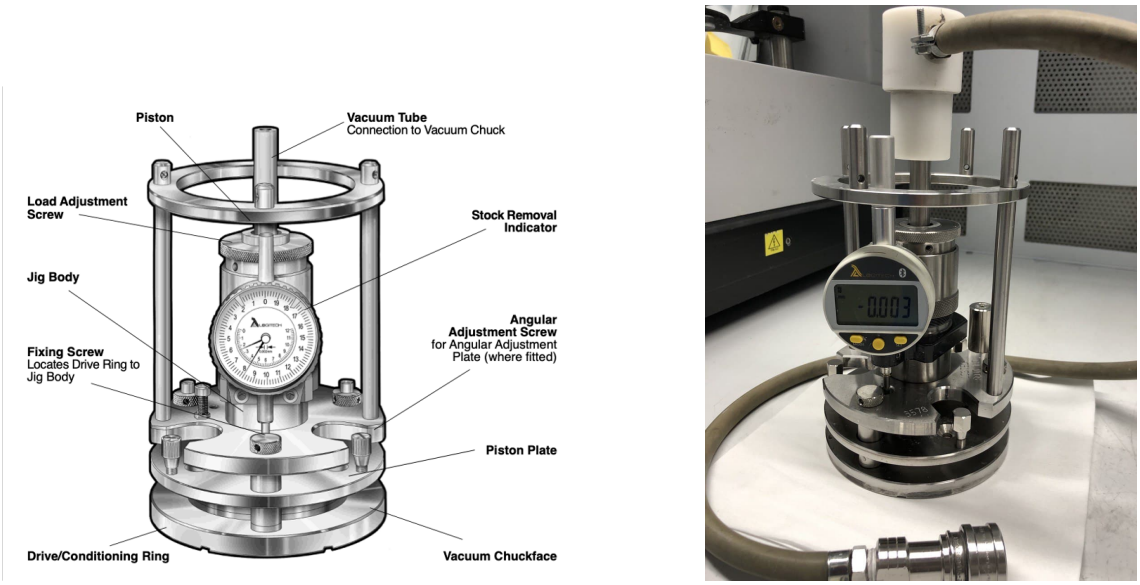
the precision jig by vacuum connection. The jig is responsible for the orientation of the sample as well as the load applied to it. During lapping and polishing, the jig was adjusted to press the wafer with a load of 2 kg.

LP50 machine has an integrated abrasive autofeed system including a slurry tank and a drain tube for slurry. The slurry tank can be seen at the top of figure 4.3 a). The aim is, that the slurry is released from the tank into the tube at a steady pace and eventually drains along the tube onto the lapping plate. A steady flow of slurry drainage aims to ensure a smooth lapping and polishing result. In this thesis the abrasive grain used was aluminium oxide, mixed with deionized water (DI-water). The slurry used in lapping is prepared to the slurry tank in a way, that the aluminium oxide volume is 20 % of the total tank volume. The maximum volume of slurry tank was 4.5 liters. Coarser grain and finer grain had their own tanks to prevent any mixing between the two grain options.

The operation of the LP50 system is controlled from the touch panel on the front of the device. One operation parameter is plate speed, which can be adjusted up to 70 rpm [55]. For wafers lapped in this thesis, the rotating speed was adjusted to 50 rpm, whereas during polishing, slower rotation speed of 20 to 30 rpm was used. The lapping plate which was used in this thesis is made from glass and has 14” diameter. During polishing, two different polishing pads were used on top of the lapping plate. Polishing pads used were Logitech 0CON-363 polishing pad and Logitech 0CON-353 Chemcloth polishing pad.

4.2.1 Precision jig PP5GT

Generally, jigs are made of steel to make them as sturdy as possible and easy to maintain. Precision jig used in this thesis is Logitech PP5GT precision lapping and polishing jig, which is shown in figure 4.4.



(a) *(b)*

Figure 4.4. *Precision jig PP5GT. a) Schematic of jig structure [56] and b) PP5GT-jig used in this thesis.*

The PP5GT jig has digital dial gauge for measuring thickness change of the wafer during lapping. With help of jig, the orientation of the sample can be adjusted as its angular adjustment range is $\pm$ 1.5°. Angular adjustment is done with three angular adjustment screws located above the piston plate. In addition, the load applied to the sample by jig can be adjusted between 0.2 kg and 2.8 kg. The total mass of the jig is 5.4 kg. [57, 58]

For vacuum chuckface to operate, vacuum source must be connected to vacuum tube on top of the jig. The adaptor used to connect the vacuum source to the jig allows normal rotating of jig during lapping and polishing. [58] The jig used in this thesis had angular grooves pattern as a vacuum chuck.

4.3 The lapping and polishing process

The thinning process can be divided in two categories: coarse thinning and final polishing. In this thesis, the coarse thinning is done via lapping. The slurries used in bulk material removal and polishing had 9 μm and 0.3 μm grain sizes, respectively. The thickness of the semiconductor wafer samples were measured before processing, after bonding, after lapping and after final polishing. Thickness measurements were used to estimate the thickness variation throughout the wafer and assess whether the target thickness has been reached. The measurement points are shown in the figure 4.1. The target thickness of the semiconductor wafers was decided to be 100 μm in order to be able to detect possible wafer bow more clearly. However, it was quickly discovered that the 100 μm wafers were mechanically too brittle to handle, resulting in a change in the target thickness to 150 μm. In addition, some wafers were thinned in parts to allow multiple

polishes to be performed on a single wafer.

Experimental part of this thesis was started with using only coarse grain size, i.e., 9 μm grain size. The aim of this test was to establish a reference point for evaluating the performance of different polishing methods. In addition to this, it was desired to see how much bowing is generated on the wafer when the surface damage caused by lapping is not removed in any way.

Next, various polishing tests were performed using 0.3 μm grain size slurry. The sample was first thinned using the coarse 9 μm grain size slurry to create the matte surface to be polished. This surface was subjected to various polishing methods designed to obtain a mirror-like surface. Initially, a fine grain size slurry was used directly with a glass lapping plate. Later, fine grain slurry was used in conjunction with various polishing pads. In addition to polishing pads, also wet etching were attempted to remove the last damaged layer. The etching solution was prepared in a ratio of 1:1:20 using NH_3, H_2O_2 and H_2O, respectively. With this mixture ratio, the etching rate of the solution should be about 1 μm per minute. Total etching time was decided to be 10 min resulting around 10 μm material removal.

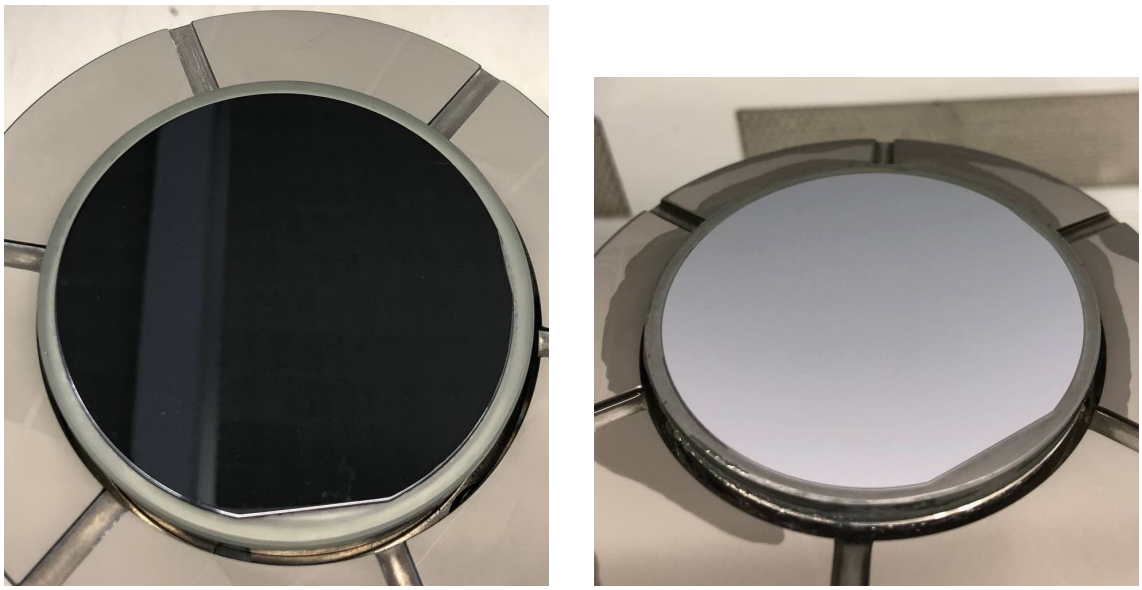
In the final step of the testing process, the sample was detached from the glass substrate. This processing step is referred as wax removal. During wax removal, a posistrip solution, which is organic blend, is used to remove positive photoresist from substrate surfaces [59]. Once the wafer has been detached from the glass substrate, it went through isopropanol (IPA), water and methanol baths. Finally, after methanol bath, the wafer was dried with N_2. In general, wax removal is a very critical phase in processing, as a thin and potentially tensioned wafer will break very easily.

5. RESULTS

This chapter presents the results of various lapping and polishing tests. First, GaAs wafers were only thinned and characterized. These results serve as benchmarks for subsequent polishing test results. Next, the results from the first polishing tests are reviewed. Based on subsequent polishing tests, a polishing process was developed to obtain as uniform GaAs wafers as possible. All experimental tests performed were performed using LP50 lapping and polishing equipment with varying settings.

5.1 Removal of bulk material - coarse thinning

Coarse thinning is needed to remove bulk material from the semiconductor wafer within a reasonable time. The slurry used contained 20 % by volume of Al_2O_3 abrasive grain with grain size of 9 μm. Rotating speed of the lapping plate was set to be 50 rpm. In addition, 2 kg load was applied to the GaAs wafer via jig during lapping. GaAs wafers were processed by lapping until the target thickness was reached. This took about 45 minutes to up to an hour. Figure 5.1 shows the unprocessed and lapped surface of a GaAs wafer.



(a) *(b)*

Figure 5.1. *Comparison of GaAs wafer surface a) before thinning and b) after thinning with 9 μm slurry.*

It can be seen from figure 5.1 a) that the surface of unprocessed GaAs wafer have a mirror like surface. Figure 5.1 b), in turn, shows the surface of the wafer after lapping. The wafer thickness was measured from unbonded wafer, after bonding the wafer to glass substrate and after lapping. The measurement results for unpolished GaAs wafer shown in table 5.1 corresponding to the numbering of the Measurement points shown in the figure 4.1.

Table 5.1. *Unpolished GaAs wafer thickness measurement results. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

Measurement point	Unbonded (μm)	Bonded (μm)	Lapped (μm)
1.	607	607	101
2.	617	618	109
3.	602	605	100
4.	590	596	94
5.	608	612	111
6.	615	616	111
7.	610	613	111
8.	599	605	103
9.	604	606	104
AVG	606	609	105
TTV	27	22	17
STD	8.3	6.8	6.0

The total thickness variation (TTV) is calculated between the thickest and thinnest point. In addition, standard deviation (STD) was calculated for each case in order to neglect the effect of one measurement point. The GaAs wafer was initially unevenly thick having up to 27 μm variation between the thickest and thinnest points. Lapping decreased the total thickness variation, which is the desired effect.

As can be seen from figure 5.1, the surface of the GaAs wafer is matte due to various scratches and other micro damage obtained during lapping process, and due surface roughness. It can be concluded that these micro-damages on the surface of the wafer cause tension to the wafer structure and therefore, wafer bow can be seen. The formed wafer bow is shown in the figure 5.2.

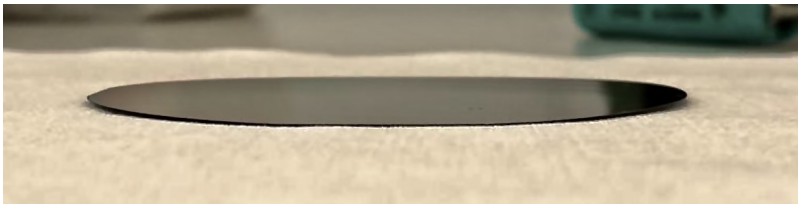


Figure 5.2. *The wafer bow is visible after lapping.*

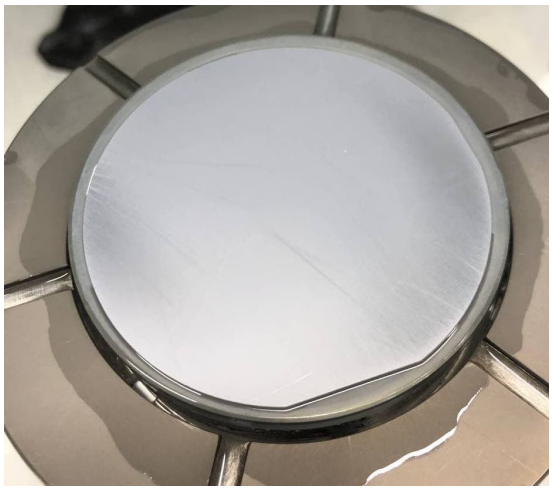
In the figure 5.2, the lapped side of the GaAs wafer rests against the table, i.e., the bottom side of the wafer is against the table. It can be seen that the wafer bow is negative as the wafer edges are higher compared to the center of the wafer.

5.2 Final polishing using polishing slurry

In this section, different polishing methods are applied to the GaAs wafer surface after it has gone through bulk removal via lapping process. In other words, the surface of the GaAs wafer prior polishing corresponds to the surface shown in figure 5.1 b). In this section, 0.3 μm Al_2O_3 slurry is used for polishing. From the total slurry volume, Al_2O_3 concentration was the same as with 9 μm slurry, i.e., 20 %.

5.2.1 Polishing with glass lapping plate

In the first polishing test, a polishing slurry was used in conjunction with a glass lapping plate. The idea behind the experiment was to study how the LP50 equipment and PP5GT jig behaves when the thinning slurry is switched to a polishing slurry. The aim was to keep the settings of the equipment similar to section 5.1, i.e, the lapping plate speed was 50 rpm and the wafer was subjected to the same load via jig. It was quickly noticed that the lapping equipment used was not working properly with the polishing slurry. The jig did not rotate on top of the lapping plate as it should have, which resulted in very uneven results. These results are shown in figure 5.3.



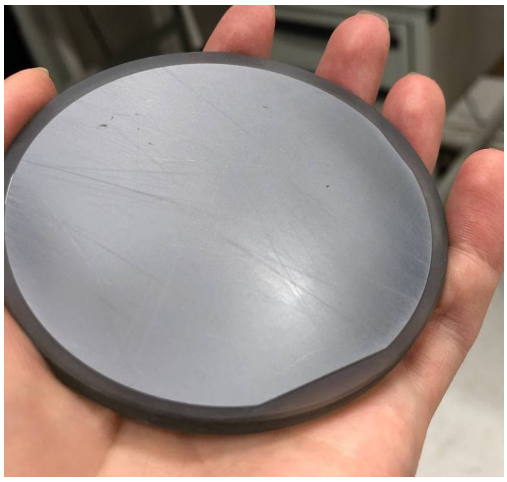


Figure 5.3. *GaAs wafer surface after polishing with 0.3 μm slurry and glass lapping plate. Major scratches on wafer surface after polishing.*

Thickness variation can be seen even visually as the wafer edges are darker compared to its center of the wafer. In addition, there are large, visible scratches on the surface of the wafer. Table 5.2 shows the thickness measurements for GaAs wafer shown in 5.3.

Table 5.2. *Thickness measurement results after 5 min polishing with 0.3 μm slurry and glass lapping plate. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

Measurement point	Unbonded (μm)	Bonded (μm)	Lapped (μm)	Polished (μm)
1.	610	606	164	162
2.	621	615	158	157
3.	611	605	156	153
4.	587	595	157	154
5.	614	627	160	160
6.	613	619	165	165
7.	619	626	161	159
8.	608	620	158	158
9.	604	620	164	164
AVG	610	615	160	159
TTV	34	32	9	12
STD	10.0	10.7	3.4	4.1

The thickness of the wafer after polishing has remained almost unchanged. In addition, it can be noted that the wafer TTV and STD increased after polishing, which is an unwanted outcome. It was concluded that the uneven rotation of the jig caused large irregularities on the surface of the GaAs wafer. However, since lapping smoothed the wafer, the TTV and STD are both significantly smaller compared to unbonded wafer TV and STD.

Efforts were made to improve the polishing result by polishing the wafer completely by hand. In manual polishing, the wafer was rotated against cleanroom paper on which polishing slurry had been poured. This test was to evaluate the effect of soft polishing pad. The result is shown in figure 5.4.

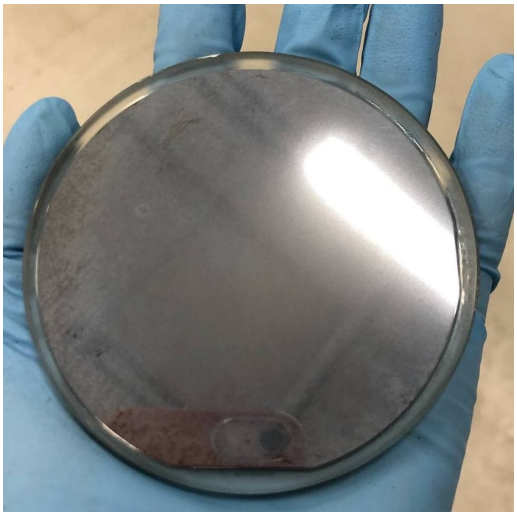


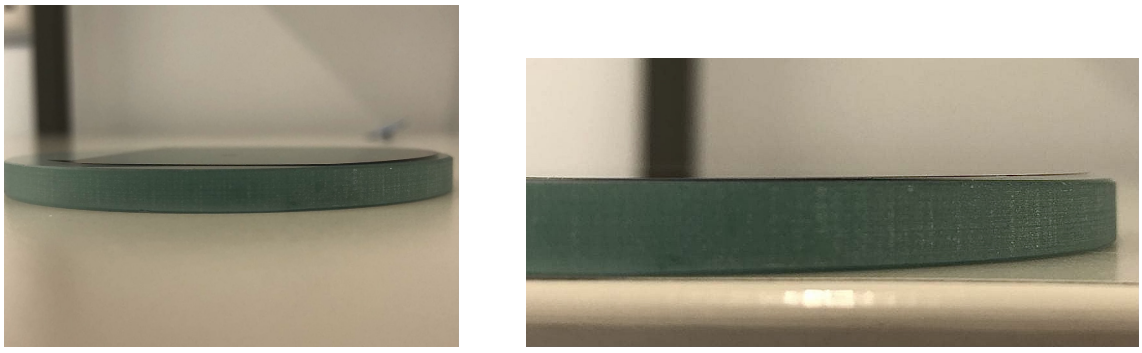
Figure 5.4. *Polishing done by hand. The total polishing time was 20 min.*

It can be seen that the polishing result is very smooth compared to previous situation. In addition, slurry residues can be observed on the surface of the GaAs wafer. No special effort was made to remove these residues in order to avoid scratching the wafer. Later, in section 5.3, similar slurry residues were encountered. These residuals were sought to be removed by wiping the wafer lightly with cleanroom paper. In that case, the slurry residues were eliminated from wafer surface. It is likely that wiping could also have cleaned the wafer shown in figure 5.4 from slurry residues. The thickness of hand-polished wafer was measured in different processing steps. These measurement results are shown in table 5.3.

Table 5.3. *Hand-polished GaAs wafer thickness measurement results. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

Measurement point	Unbonded (μm)	Bonded (μm)	Lapped (μm)	Polished (μm)
1.	609	611	94	100
2.	622	615	96	95
3.	610	616	104	104
4.	595	596	108	108
5.	609	603	114	115
6.	616	624	103	100
7.	620	628	100	105
8.	603	605	113	111
9.	601	607	110	110
AVG	609	612	105	105
TTV	27	32	20	20
STD	8.9	10.2	7.2	6.3

Again, the wafer was unevenly thick in the beginning of the process. The end result was also in the desired direction at the end of the lapping as the total thickness variation had been reduced. On the other hand, there had been no change in TTV despite the polishing but the STD was increased, meaning some flattening has happened. In addition, slurry residues could affect the measurement results, since some of the measurement points had increased after polishing. The average thickness of the GaAs wafer had not changed between lapping and polishing, meaning that wafer structure probably still had some subsurface damage. This seems to be the case, since wafer bow can be detected after hand polishing as seen in figure 5.5.



(a) ***(b)***

Figure 5.5. *Wafer bow visible after hand polishing. a) The whole wafer and b) a clearer picture of the wafer bow.*

The wafer bow is clearly visible although a small portion of the wafer has cracked during

wax removal as seen from figure 5.5 a). The cracking has removed some of the tension from the wafer, but the wafer has still enough tension to create the bow. Since the thickness of this wafer is in the same thickness range as the wafer of figure 5.2, the two wafer bows can be compared with each other. It can be seen, that the wafer bow in the hand polished wafer is smaller compared to wafer bow in the unpolished wafer.

5.3 Polishing with polishing pad

In previous section, it was noted that soft pad will give better polishing result compared to hard glass lapping plate. Based on the result, a lapping plate was covered with polishing pad. The polishing pads used in these experiments were Logitech 0CON-353 14" Chemcloth and Logitech 0CON-363 14" Pellon pad. The 0CON-353 pad had a velvety surface, manufactured from proprietary polyurethane. The 0CON-363 pad, in turn, had a fabric-like appearance, with absorbent fibres [60, 61]. The GaAs wafers used in this section have been thinned in several parts so that more polishing tests can be performed on one wafer. However, prior to each polishing test, the wafer has been thinned at least 200 μm with a 9 μm slurry to create of new rough surface that could be polished. The polishing tests in this section are presented using different polishing times instead of the thickness change, as the PP5GT precision jig thickness gauge did not work properly on a soft surface.

5.3.1 0CON-363 polishing pad

The following polishing test was performed using a 0CON-363 polishing pad. The back of the pad had a tape surface that was used to attach the pad to the lapping plate. Any air bubbles formed during attachment were rolled off with a heavy stone roller. Since the jig did not rotate properly with original lapping settings in section 5.2.1, the test was started with lower lapping plate speed. Used lapping plate speed was 20 rpm in this test. The jig load was kept at 2 kg in this test. The results obtained after 15 minutes of polishing with using 0CON-363 polishing pad is shown in figure 5.6.

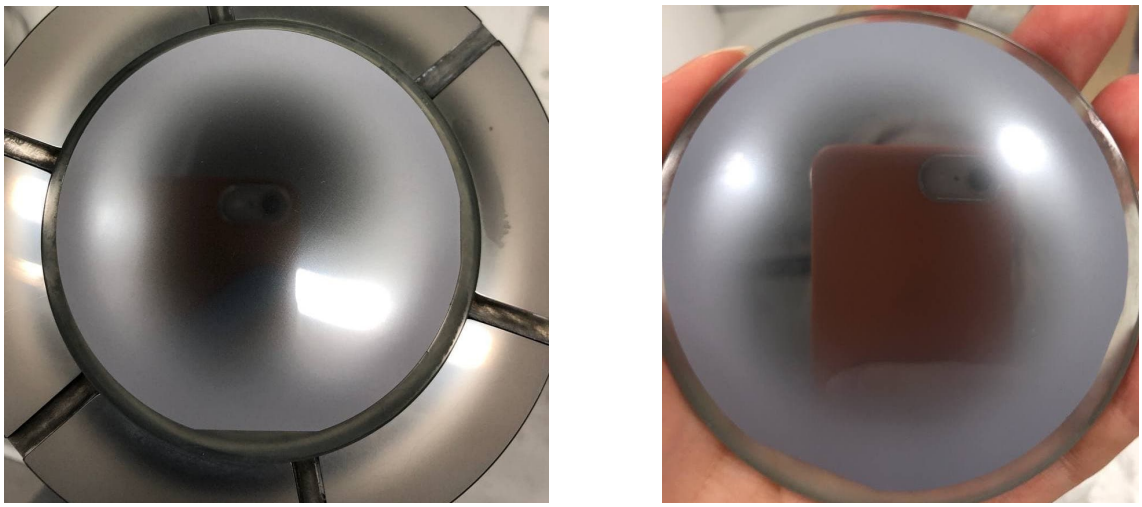


Figure 5.6. *GaAs wafer surface as seen from two different angles. The wafer is polished for 15 min with 0CON-363 polishing pad.*

As can be seen, the edges of the wafer had remained more blurred compared to the center region of the wafer. This could be caused, for example, by the thickness differences of the GaAs wafer after lapping. The thicknesses of the GaAs wafer at different phases of the process are shown in table 5.4.

Table 5.4. *Thickness measurement results for GaAs wafer polished by 0CON-363 polishing pad. Total polishing time was 15 min. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

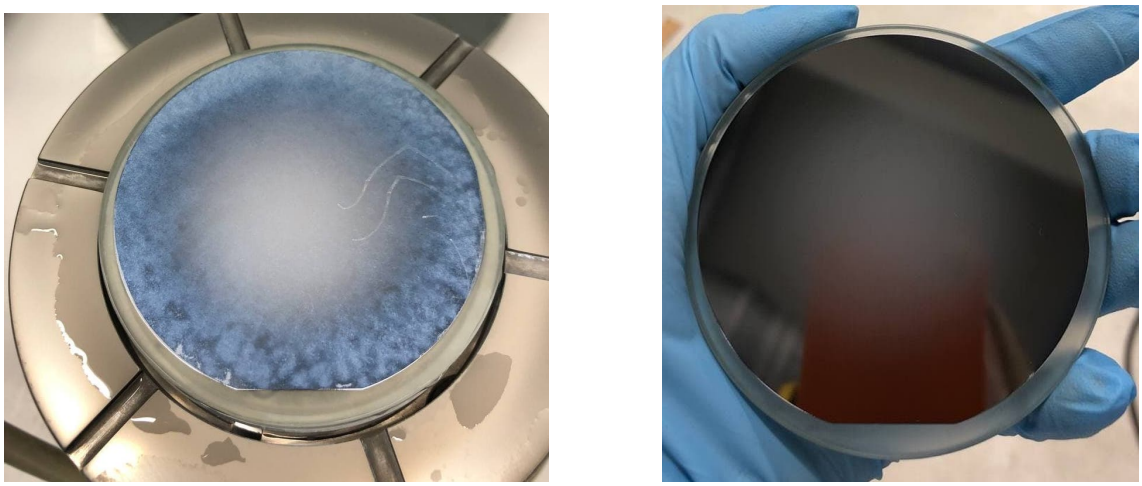
Measurement point	Unbonded (μm)	Bonded (μm)	Lapped (μm)	Polished (μm)
1.	612	610	410	410
2.	600	595	413	410
3.	610	608	420	416
4.	615	618	420	420
5.	612	617	426	424
6.	607	605	411	410
7.	600	610	418	418
8.	612	617	423	424
9.	616	615	417	418
AVG	609	611	418	417
TTV	16	23	16	14
STD	5.9	7.4	5.4	5.7

It can be seen from the table 5.4, that the thickness of the wafer has decreased according to the middle Measurement points, i.e., points 5, and 6. This is clearly visible also from the look of the GaAs wafer surface as the center have mirror like presence compared to edges. After thickness measurements, wafer lapping was continued with a 9 μm abrasive

slurry to a thickness of 200 μm to obtain new matte surface, which was further polished with different polishing pad.

5.3.2 0CON-353 polishing pad

The second polishing pad test was done with 0CON-353 pad. Also this pad had a tape surface, which allowed the pad to be attached to the lapping plate. Similarly, the lapping plate speed was started at 20 rpm, but was increased to 25 rpm since the jig did rotate quite well with this polishing pad. Same jig load of 2 kg was again used in this test. Total polishing time was again 15 minutes. The polishing result is shown in figure 5.7. It was found that at the end of the polishing that there was a large amount of slurry residue on the surface of the GaAs wafer. Efforts were made to remove residues by gently wiping the surface of the wafer with cleanroom paper. The cleaned wafer is shown in Figure 5.7 b).



(a) ***(b)***

Figure 5.7. *GaAs wafer surface after 15 min of polishing with 0CON-353 polishing pad. a) Before surface cleaning and b) after surface cleaning.*

It can be seen that the wafer is unevenly polished as there is clear difference between center of the wafer and edges of the wafer. However, the polishing results is contrary compared to 5.6 as the center has been remained blurred compared to edges of the GaAs wafer. Table 5.5 shows the thickness measurements after this polishing test.

Table 5.5. *Thickness measurement results for GaAs wafer polished by 0CON-353 polishing pad. Total polishing time was 15 min. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

Measurement point	Unbonded (μm)	Bonded (μm)	Lapped (μm)	Polished (μm)
1.	612	610	203	201
2.	600	595	199	193
3.	610	608	202	200
4.	615	618	206	201
5.	612	617	213	212
6.	607	605	207	207
7.	600	610	207	201
8.	612	617	209	205
9.	616	615	209	208
AVG	609	611	206	203
TTV	16	23	14	19
STD	5.9	7.4	4.2	5.6

Again, the wafer center were thicker compared to the wafer edges as seen in measurement point 5 after lapping This can further explain polish difference between the center and edges. All in all, a mirror-like surface could be obtained by using a polishing pad with the aid of polishing. Since the polishing result was not ideal, it was decided to try how a longer polishing time affects the final result.

5.3.3 Longer polishing tests

Polishing time was increased from 15 minutes to 30 minutes. The lapping plate speed was kept again at 20 rpm for 0CON-363 pad and 25 rpm for 0CON-353 pad. The jig load was kept at 2 kg. The result from longer polishing test with 0CON-353 is shown in figure 5.8.

Figure 5.8. *GaAs wafer surface after 30 min of polishing with 0CON-353 pad.*

Again, some blurred area is visible at wafer center, but the size on the blurred area is smaller compared to figure 5.7 and it is less intense. Thickness measurements with this wafer in different process phases is shown in table 5.6.

Table 5.6. *Thickness measurement results for GaAs wafer polished by 0CON-353 polishing pad. Total polishing time was 30 min. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

Measurement point	Unbonded (μm)	Bonded (μm)	Lapped (μm)	Polished (μm)
1.	596	590	117	112
2.	586	578	125	118
3.	582	596	122	120
4.	596	594	114	111
5.	586	599	130	128
6.	587	586	129	122
7.	590	587	130	127
8.	598	601	123	123
9.	594	589	122	123
AVG	591	591	124	120
TTV	16	23	16	17
STD	5.6	7.2	5.6	4.7

In addition to examining the surface of the wafer, a wafer bow was considered. It was found that no wafer bow was formed after long polishing test. The wafer presented in figure 5.9 is after the wafer has been detached from the glass substrate.

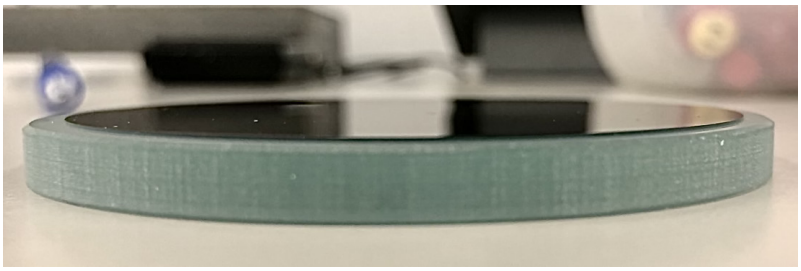


Figure 5.9. *Wafer bow is hardly present after 30 min of polishing (the wafer has been already detached from glass substrate).*

The glass substrate were only used as flat surface for aids in detecting the possible wafer bow. It was found that no significant wafer bow was formed, that could be detected visually. It should be noted, however, that the GaAs wafer in the figure 5.9 is about 20 μm thicker compared to the wafer in the figure 5.2. With thicker wafer, the wafer bow may be covered due to better mechanical resistance caused by the thickness of the wafer.

The result of the long polishing test of the 0CON-363 pad is shown in figure 5.10. Compared to the result of the long polishing test of the 0CON-353 pad in figure 5.8, now the difference in gloss between the center area and the edges of the GaAs wafer has not leveled off. In turn, it appears that the center of the GaAs wafer is further polished compared to the 15 min polishing result in figure 5.6.

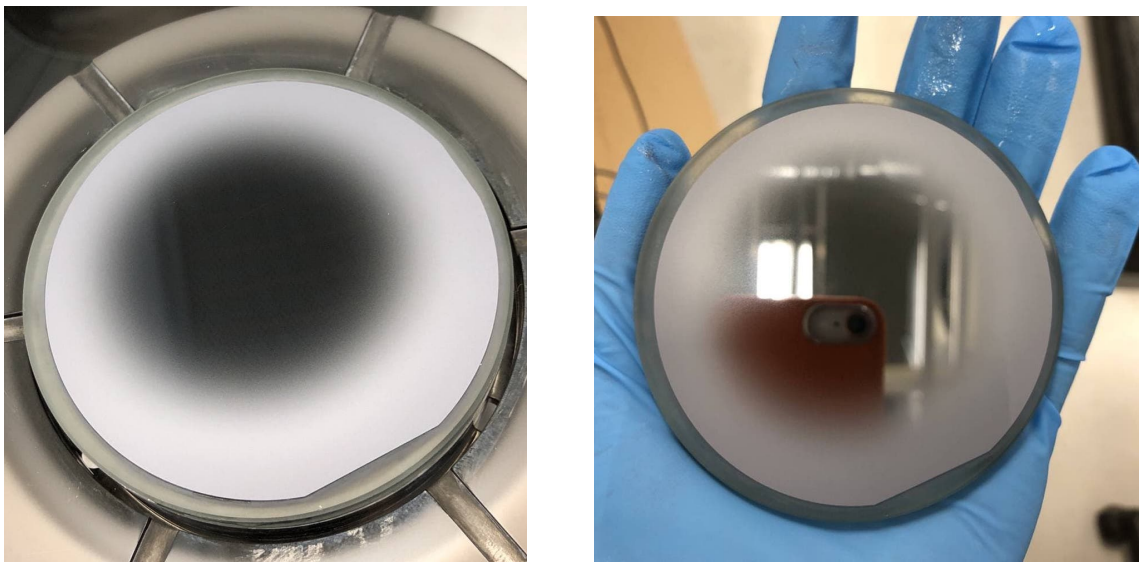


Figure 5.10. *GaAs wafer surface after 30 min of polishing with 0CON-363 polishing pad.*

The polished wafer center is also visible in table thickness measurement results. Thickness measurements for polished GaAs wafer in figure 5.10 are shown in table 5.7.

Table 5.7. *Thickness measurement results for GaAs wafer polished by 0CON-353 polishing pad after 30 minutes of polishing. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

Measurement point	Unbonded (μm)	Bonded (μm)	Lapped (μm)	Polished (μm)
1.	600	602	368	368
2.	616	613	363	362
3.	593	598	366	365
4.	585	584	371	370
5.	599	608	380	374
6.	606	614	359	371
7.	603	613	371	369
8.	588	597	377	374
9.	592	600	378	373
AVG	598	603	370	370
TTV	31	30	21	12
STD	9.7	9.9	7.1	4.1

A clear difference can be seen between the lapping center measurement point and polished center Measurement point, as the thickness of GaAs wafer center has decreased 6 μm. In addition, the edges of the wafer have remained more or less at the same thickness.

5.4 Additional wet etching after polishing

The effect of wet etching was tested as a finishing process on already slurry-polished wafer. The GaAs wafer used in this test is the same as in figure 5.10. This wafer was processed again with 9 μm slurry to remove 200 μm of bulk material to create new matte surface. This surface was further processed with 30 min polishing with 0CON-353 pad and a 0.3 μm slurry.

The etching solution was prepared with mixture ratio of 1:1:20 and used solutions were NH_3, H_2O_2 and H_2O, respectively. With this mixture ratio the etching rate should be about 1 μm / min. The wafer was etched total of 10 minutes. The etched GaAs wafer is shown in figure 5.11.

(a) ***(b)***

Figure 5.11. *GaAs wafer surface before a) and after b) etching.*

It can be seen that the surface of the GaAs wafer is very uneven and the essence of the wafer is very unfinished. The wafer thickness was measured after second lapping, polishing with 0CON-353 pad and etching. The measurement results are shown in table 5.8.

Table 5.8. *Thickness measurements of etched GaAs wafer. Average thickness (AVG), total thickness variation (TTV) and standard deviation (STD) is shown at the bottom of the table.*

Measurement point	Lapped (μm)	Polished (μm)	Etched (μm)
1.	168	164	159
2.	170	167	162
3.	163	161	156
4.	160	156	151
5.	176	176	169
6.	178	175	170
7.	174	172	163
8.	166	165	158
9.	169	168	162
AVG	169	167	161
TTV	18	20	19
STD	5.9	6.5	5.8

The etching removed an average of 6 μm of semiconductor material from the etched surface. This is slightly less than what the original etching rate suggested. The change in etching rate could be due to the large size of the wafer, since with smaller semiconductor pieces the etching rate is quite accurate. On the other hand, the etching did remove the material quite evenly throughout the GaAs wafer. Since the etching did not have much effect on the TTV nor STD and the etched surface had quite unfinished essence, it was concluded that etching with this solution as such is not a durable solution for the polishing process.

5.5 Surface roughness by AFM imaging

The roughness of the samples was evaluated using atomic force microscopy (AFM) imaging for different samples. In the AFM imaging, an extremely sharp needle tip attached to a flexible cantilever is brought very close to the sample to be examined. This causes the force interaction between the tip and the specimen and furthermore a deviation in needle position or movement. [62] Figure 5.12 shows the basic setup for AFM operating with tapping mode.

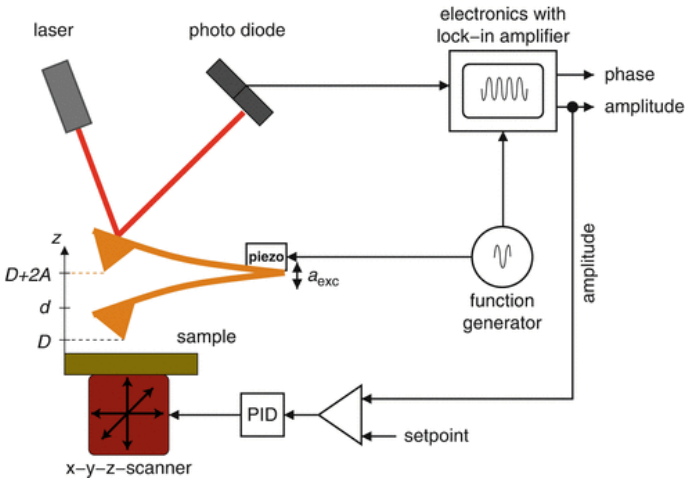


Figure 5.12. *AFM operating with tapping mode [62].*

During tapping mode operation, the cantilever is vibrating close to its resonance frequency while being close to the sample surface. This close distance between the tip and the sample will cause the force interaction between the tip and the sample surface, which further causes a deviation in needle position or movement. [62]

The purpose of this study was to evaluate the surface roughness and evaluate how the polishing process is affecting to sample surface. It is important to note that the AFM imaged area was 3 μm x 3 μm, so these images are not a representative shot of the entire area of the whole 3" GaAs wafer. A larger imaging area, in turn, would have taken so long that it would not be profitable to take the images.

Samples chosen to be imaged were unpolished sample as in figure 5.1 b), hand-polished sample as in figure 5.4 and two samples polished with 0CON-353 polishing pad. From these samples, one of the 0CON-353 polished samples were measured before and after wet etching the sample. Figure 5.13 shows the 3D-images of the samples imaged.

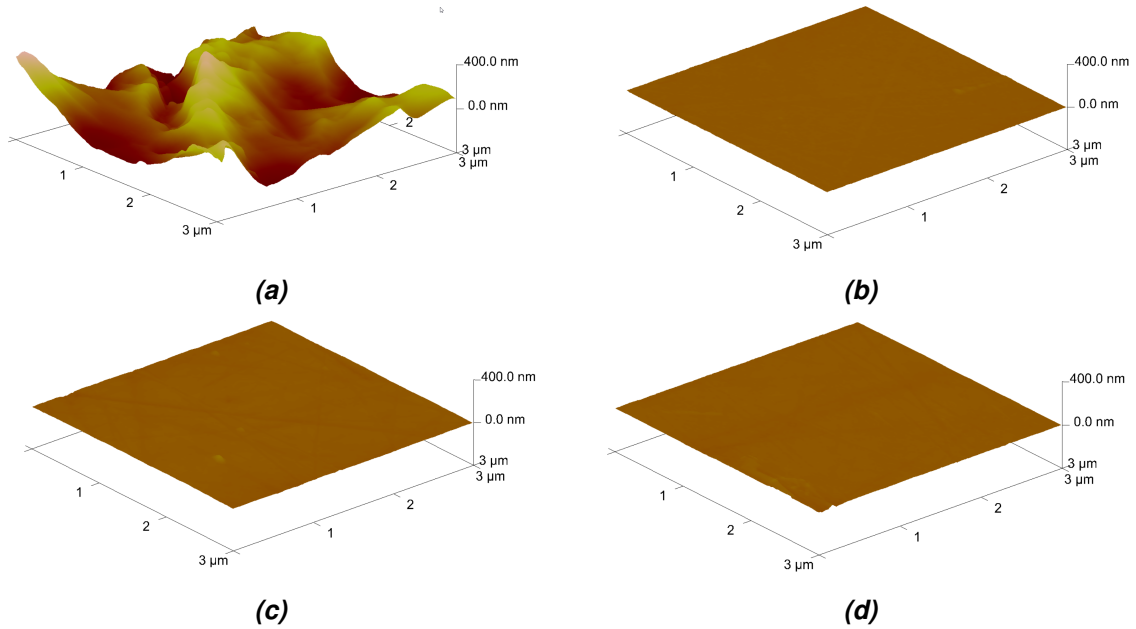


Figure 5.13. *3D-images from sample surface taken with AFM. a) Unpolished sample b) polishing done by hand with 0.3 µm abrasive grain and cleanroom paper c) and d) are parallel samples with polishing done using 0.3 µm abrasive grain and 0CON-353 chemcloth.*

It was noted that the image height scale was quite large for the polished samples. On the other hand, the sample surface has been clearly leveled out since the polished samples look completely flat in this height scale compared to unpolished sample in 5.13 a). To have a clearer view to the polished sample surfaces, the height scale has been decreased in figure 5.14 for polished samples.

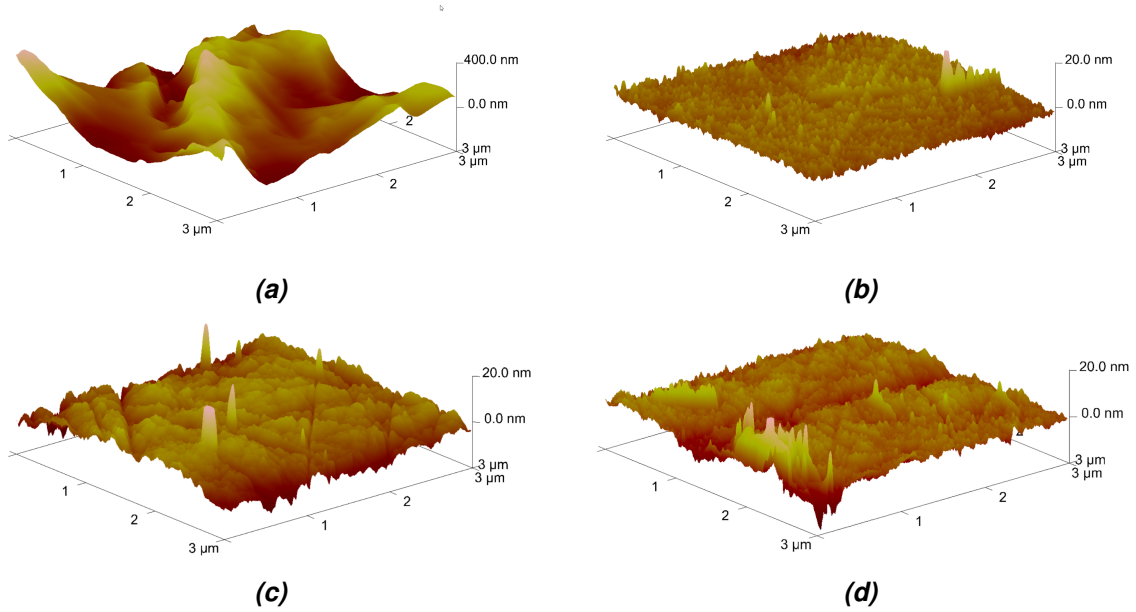


Figure 5.14. *Height scale adjusted for polished samples. a) Unpolished sample b) polishing done by hand with 0.3 μm abrasive grain and cleanroom paper c) and d) are parallel samples with polishing done using 0.3 μm abrasive grain and 0CON-353 chemcloth.*

It is important to note that in figure 5.14 the height scale of figure 5.14 a) is from -400 nm to 400 nm, compared to height scale of figures 5.10 b) – d) being only from -20 nm to 20 nm. Now the unevenness of the polished surfaces is visible. To have better sense of the surface morphology, 2D-images are studied. Figure 5.15 shows 2D-images of sample surface.

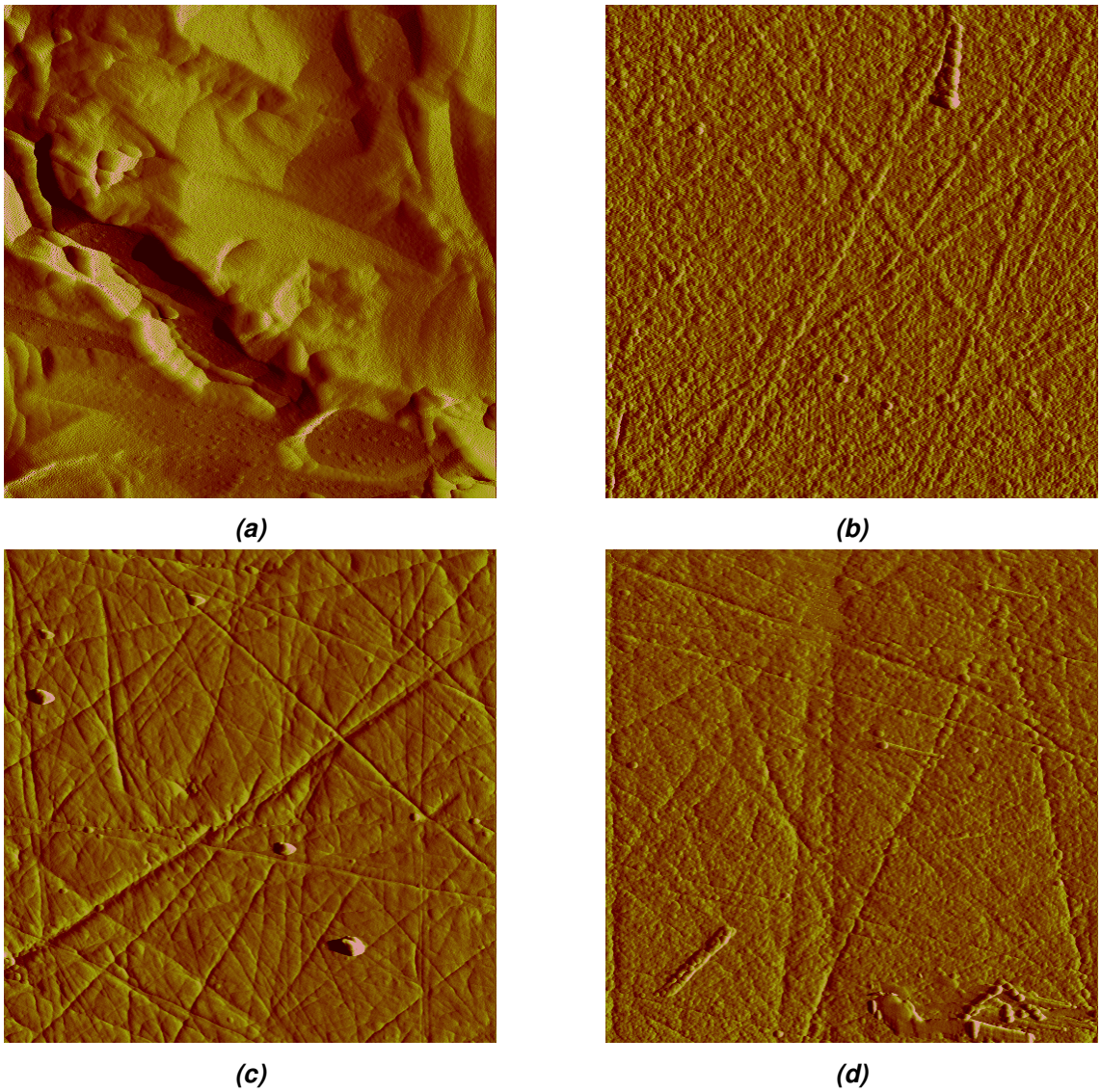
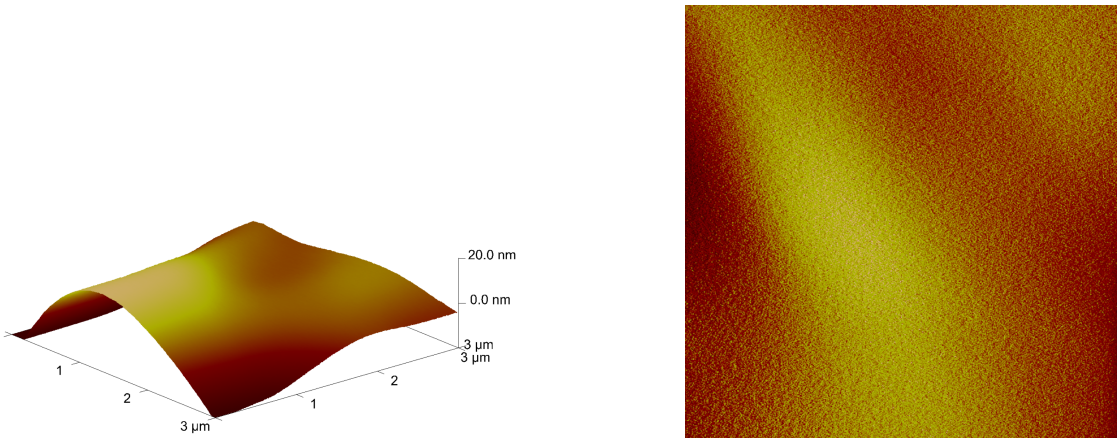


Figure 5.15. *Surface morphology in 2D format. a) Unpolished sample b) polishing done by hand with 0.3 μm abrasive grain and cleanroom paper c) – d) polishing done using 0.3 μm abrasive grain and 0CON-353 chemcloth.*

In these figures the image scaling is not directly a height scale but an amplitude scale. The scale is from 0 mV to 150 mV with unpolished sample adn from 0 mV to 60 mV with polished samples. Long traces seen from the figure 5.15 b) – d) were suspected to have been caused by the use of slurry in polishing.. With the use of slurry, traces like this are unlikely to get rid of since the use of abrasive slurry is based on scratching the surface. The depth of scratch can be decreased by using a smaller grain size.

The sample showed in figure 5.13 c) and 5.15 c) was wet etched after AFM-imaging. The wet etching was done using 1:1:20 NH_3:H_2O_2:H_2O etching solution. After etching, the sample was imaged again with AFM. Unfortunately, imaging failed due to etching-induced sample charge as well as a possible water molecule layer on the sample surface. AFM images for wet etched sample are shown in in figure 5.16.



(a) *(b)*

Figure 5.16. *Etching resulted formation of charge or water layer on top of the sample surface resulting unsuccessful AFM-images. a) 3D-image on the sample surface and b) 2D-image on sample surface with amplitude scale from 0 mV to 5 mV.*

The cantilever tip did not reach the surface of the sample due to the charge of the sample and possible water layer on top of the sample surface, which is why no conclusions can be drawn from these images.

Finally, roughness estimates were taken from the AFM-images. Table 5.9 shows the most essential values R_a, R_q, and R_{max}. R_a gives the arithmetic average of the absolute height values measured from the mean plane. It can be seen from the table 5.9, that polishing had decrease this value in all cases. R_q, on the other hand, is the root mean square (RMS) average measured from image data plane. Again, polishing has decrease this value. Finally, the R_{max} is the height difference between the highest and lowest point of the image. [63] The upper half of the table 5.9 shows values related to whole image area. The bottom half, on the other hand, represents roughness estimates from smaller area. The area was selected so that the largest contaminants and defects were excluded from the area.

Table 5.9. *Roughness values obtained from the AFM-images.*

Sample	R_a (nm)	R_q (nm)	R_{max} (nm)
Unpolished	105	84.4	662
Hand-polished	1.72	1.27	29.4
0CON-353 pad, 1	3.13	2.30	63.0
0CON-353 pad, 2	2.54	1.73	45.6
Values taken from defect free area			
Hand-polished	1.43	1.13	11.7
0CON-353 pad, 1	2.05	1.64	14.1
0CON-353 pad, 2	1.63	1.31	11.2

The roughness estimates obtained from table 5.9 support the information observed from the 3D and 2D images that the unpolished sample is very coarse. From the polished samples, it appears that the hand-polished sample has a smoothest surface. However, very precise conclusions cannot be drawn, as AFM images do not provide a representative shot of the morphology of the entire wafer surface.

6. DISCUSSION

This chapter discusses the results obtained during different lapping and polishing tests in more detail. In addition, the relationship between the theory and the results is considered.

It was noted that the 9 μm grain size had a greater effect to the wafer compared to 0.3 μm grain size, since the material removal rate was greater with 9 μm grain size. This observation is well in line with the theory presented in chapter 3. In addition to this, it was observed in the lapping tests that the lapping plate speed had a great effect on the material removal rate. The results are presented in figure 6.1.

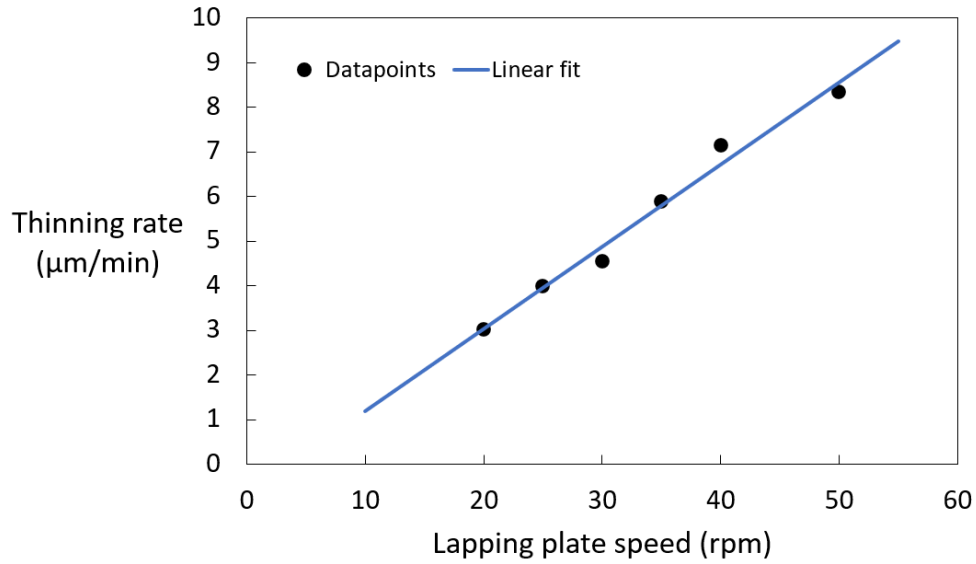


Figure 6.1. *The effect of the lapping plate speed to the material removal rate.*

As can be seen from figure 6.1, with increased lapping plate speed also the material removal rate increased. Since the 9 μm grain size had a greater effect on the wafer, it also created more micro-surface damage to the wafer. This can be seen as a matte surface after the use of 9 μm grain size.

One of the big insights of this thesis was that the 0.3 μm grain size would not work properly without a soft polishing pad. Without the polishing pad or other soft pad, polishing performance was highly uneven. The reason for the unevenness was thought to be that the very fine grain size could not support load caused by the jig with mounted wafer on it. This caused the semiconductor wafer to adhere to the glass lapping plate due to the

interaction of adhesion forces. After the polishing pad was introduced, the jig was allowed to rotate freely without interference from adhesion. From this, it was concluded that the polishing pad served as a supportive substrate for the jig allowing the 0.3 μm abrasive grains to function properly between the plate and the semiconductor wafer.

6.1 The effect of the overall thinning process on TTV and STD

It was found that lapping reduces height difference between highest and lowest point as after each lapping test made the value of TTV was reduced. This is a desired effect, as the physical properties of the wafer, like heat distribution, remain more uniform throughout the wafer area. On the other hand, the polishing process had only little effect on the value of TTV. In some cases the TTV value increased between the lapping and polishing. The results from different polishing tests have been collected to table 6.1.

Table 6.1. *Results from different polishing tests.*

	AVG_L-AVG_P (μm)	TTV_L-TTV_P (μm)	STD_L-STD_P (μm)	Appearance
Glass plate	1	-3	-0.7	Uneven, scratchy
Hand-polished	0	0	0.9	Even, slurry residuals
0CON-363, 15 min	1	2	0.3	Uneven, polished at the center
0CON-363, 30 min	0	9	3	Uneven, polished at the center
0CON-353, 15 min	3	-5	-1.4	Uneven, polished at the edges
0CON-353, 30 min	4	-1	0.9	Even, blurred area at the center
Wet-etching	6	1	0.7	Uneven, defect at the center

In the table 6.1, the AVG, TTV and STD values were obtained when polished value was substracted from lapped value. It was concluded that during polishing the total thickness should decrease more than observed in these tests to obtain some effect to TTV and STD. Due to the low material removal rate of polishing, formation of new micro-cracks is slower and their size is smaller. As formation of new damage slow down, existing surface roughness has an opportunity to level off. When the total material removal is high enough, subsurface damage layer can be reduced. During the experiments performed in this thesis, the total thickness reduction during polishing was less than 5 μm. To increase

the total thickness reduce during polishing, a longer polishing time would be required. However, even though the polishing did not have as high effect on the TTV or STD as desired, the both TTV and STD were improved after the total thinning process compared to unbonded wafer TTV and STD. However, it should be noted that extremely long polishing time will slow down production rate. One other way to achieve better surface quality would be the use of several different grain sizes throughout the fabrication process. Also, the benefit obtained from several different grain sizes should be estimated in relation to the time spent as well as the equipment required.

In addition to decrease of TTV and STD, the wafer bow leveled during the polishing process. After the wafer surface had a mirror like appearance, the wafer bow was no longer visible to the naked eye. Since the mirror like surface were achieved, it was concluded that surface damage formed during lapping had been reduced or possibly even eliminated. From this it can be concluded that the tensions inside the wafer would have decreased.

6.2 Evaluation of the surface of a semiconductor wafer after polishing

Polishing tests with 0.3 μm grain size slurry and Logitech polishing pads showed very variable results. Using a 0CON-353 pad, the polishing result obtained was blurry in the middle and clearly polished at the edges, as shown in figure 5.7. With a longer polishing time, the blurring of the center was clearly reduced, but still noticeable as shown in figure 5.8. In order to obtain a fully polished wafer, the polishing time should have been further increased from half an hour to possibly up to an hour.

On the other hand, the result obtained with the 0CON-363 pad was contrary to that of the 0CON-353 pad. In the case of 0CON-363, the center of the wafer was clearly polished and the edges of the wafer, in turn, had remained matte as shown in figure 5.6. The longer polishing time with this pad did increase the polished area, but the change was not as clear as with 0CON-353 pad. In addition, it seemed that the central area had become even more polished. A longer polishing time would probably have offset the wafer polishing differences. In addition, since the polishing pads used in this thesis gave contrary polishing results, a process combining the use of both pads could have resulted an excellent polishing result.

The clear difference between the center of the wafer and edges of the wafer was thought to be caused by uneven wafer thickness. In both cases, the processed wafer was thicker in the middle compared to the edges. On the other hand, it is unclear why the polishing results are contradictory. The polishing pads used had different surfaces, which may be an influencing factor for opposite polishing results. The 0CON-353 pad had a velvety surface, while the 0CON-363 pad had a fabric-like appearance.

6.3 Wet etching

Wet etching was tested as a finishing step on a slurry-polished wafer. It was found that the wet etching solution did remove material evenly throughout the wafer. However, the wet etching did not improve the surface quality. On the contrary, the essence of the surface appeared to become more uneven. This could be due to a possible chemical reaction between the wet etching solution and air, N_2, or polishing slurry.

Since the wet etching did remove material evenly throughout the wafer, it could be a good way to remove the subsurface damage layer formed during bulk material removal. To prevent formation of clear defect on wafer surface as shown in figure 5.11, the wafer could be polished after the wet etching. This combination could create an even and uniform surface with high brightness. In addition, if the subsurface damage layer could be removed with wet etching, this could probably have a great effect on wafer bow formation. Without the subsurface damage layer the wafer has stress free structure and wafer bow is decreased or even removed.

Wet etching should be studied more. The solution ratio could be change to slower or speed up the etching and see if the defect will form with different wet etching solution ratio. In addition, also other solutions should be studied. Many other solutions will etch GaAs, for example bromide. In case of other solutions, formation of defect on wafer surface should be observed.

6.4 AFM imaging to evaluate surface roughness

AFM images were taken from the processed samples to allow a closer look at the surface roughness. From the images obtained, it could be seen that the unpolished sample was very rough and uneven. In addition, it was observed from the AFM images that the surface smoothness was greatly affected by the polishing, as the 3D images of the polished samples on the same height scale were practically completely smooth compared to the unpolished sample. Only after reducing the height scale with polished samples, some surface unevenness was observed.

The polished samples showed traces of the abrasive grains used in the polishing process. Such traces of grain were not visible in the unpolished sample. This was thought to be due to the scaling of the image, as the 9 μm grain leaves such a large mark on the surface of the semiconductor that the 800 nm height scale is not sufficient to show it. In section 3.2, the penetration depth of the grain was reported to depend on the size of the grain as it is about 5 to 10 % of the average diameter of the grain. With 9 μm average grain size, the penetration depth is 0.45 to 0.9 μm, meaning that the 800 nm (or 0.8 μm) is not a wide enough height scale to display these deep traces.

7. CONCLUSIONS

Laser industry is a fast-growing business and lasers are used in many different applications. For example, LiDAR and difference medical treatment methods utilize lasers in their operation. These semiconductor lasers are based on GaAs, which is a common material used in optoelectronics due to its direct band gap. To create GaAs laser chips with high efficiency, the GaAs wafer needs to be thinned before dicing the chips. The thermal management is better with thinner devices due to decreased series resistance and therefore, increased thermal conductivity. The aim of this thesis was to study the total thinning process of semiconductor wafers used in laser fabrication. The thinning included bulk material removal via lapping and final polishing with small grain size slurry.

In this thesis, it was found that lapping has a great effect on total thickness variation throughout the wafer, and has an overall smoothing effect on the wafer when compared to original wafer. After lapping, the surface was matte due surface roughness and micro damage on the wafer surface. The depth of the resulting micro damage depends on the average diameter of the abrasive grain used. The damaged layer was removed by taking advantage of a smaller grain size than in coarse thinning. The abrasive grains grind the surface of the semiconductor wafer as in lapping, but due to the smaller size of the grains, equally radical micro damage would not occur, resulting smaller or non-existent subsurface damage layer. At the same time, a mirror-like appearance was created to the surface, hence polishing process occurred. Seven different finishing processes were performed on the GaAs wafers. The unpolished GaAs wafer served as a reference for polishing results. It was found that the polishing slurry did not work properly when used directly with the lapping equipment. However, with soft polishing pad and slower lapping plate speed, the equipment was working properly and wafer could be polished quite evenly. In addition, the mirror-like appearance could be achieved almost throughout the wafer.

Since the polishing with LP50 equipment needed soft pad in order to function properly, two polishing pads were studied. The two pads gave contrary polishing results, the other having matte wafer center and shiny edges and the other one vice versa. This could be caused by thickness differences that were initially present after coarse thinning. Perhaps, the combination of the two pads during one polishing session could have produce a perfect mirror-like appearance for the wafer. In addition, it was observed that longer polishing time will produce shinier and more even polishing result. This enables the optimization

of the polishing process parameters to meet the quality requirements for low resistance lasers.

Finally, wet etching was utilized as a finishing process. It was found that wet etching did remove material evenly throughout the wafer. However, after the wet etch, the wafer surface had some pattern, whose exact origin is not known. This means that the used wet etching solution is not suitable as such for wafer surface finishing process. On the other hand, since the material removal was even throughout the wafer, wet etching should be studied more, e.g., study different solution ratio or different wet etchants.

It was observed in the experiments that the material removal of GaAs was minor during polishing process. For future work, precisely this low material removal during the polishing should be studied and it should be increased in order to have a greater effect on the wafer surface and subsurface damage layer. This could be achieved with longer polishing time or adjusting the lapping plate speed or the jig load. In addition, slightly larger grain size than 0.3 μm, e.g., 1 μm could possibly remove the damages and produce a mirror-like surface. In addition to polishing, better surface quality could be achieved by performing thinning in stages with different grain sizes. When moving from coarser grain size to finer grain size, the subsurface damage layer could be decreased, since finer grain size is more gentle material removal method. However, the benefits of using multiple slurries should be evaluated in relation to the increased workload and increased processing time. In case with several slurries, due the contamination risk increases when moving from coarser grain size to smaller grain size, the need for additional lapping equipment or the used procedures to maintain the cleanness in the lapping station should be reviewed. As a conclusion, to be able to utilize the promising results of this thesis, the polishing process should be further studied.

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