Tampereen yliopisto

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DESIGNING A CMOS OPERATIONAL AMPLIFIER

IC design by superficial computer aided analysis

Bachelor's thesis
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ABSTRACT

Petteri Toivanen: Designing a CMOS Operational Amplifier

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Operational amplifiers are widely used electronic components. They implement diverse functions in circuits, like arithmetic operations or signal generation. The operational amplifier itself is technically only an amplifying device and the desired operations are controlled by the external components connected around it. General operational amplifier properties include high amplification, high input impedance and low output impedance.

The target of this work is to design an operational amplifier that works with 2.2 V supply voltage and maximum idle current of 500 µA in integrated circuit use. Minimum load resistance target is 100 Ω. The amplifier is designed with free circuit simulator LTspice and elementary circuit theory.

An existing amplifier structure of Texas Instruments LM358 is used as structural reference. Bipolar junction transistors of LM358 are replaced with field-effect transistors because they are better suited for integrated circuits' needs due to lower operating currents and supply voltages as well as simpler transistor structure. Ideal components are replaced with respective transistor configurations when practical, pursuing realistic integrated circuit design.

The design is executed with emphasis on iterative graphic analysis. Input stage's transistors' operation regions are estimated, after which the suitable operating point is iterated by changing transistor geometries. The buffer and output stage transistor sizing is done by interpreting bias currents and voltages obtained by initial guess. Transistor current and voltage plots are used to inspect individual transistor operating points and block functionality is evaluated by examining signal propagation of a sinusoidal input.

The amplifier designed in this thesis works with 2.2 V supply voltage with 100 Ω load in simulated test circuits. It offers 59.7 dB gain for bandwidth of 11.9 kHz with internal compensation. Idle current of the amplifier settles in 634 µA so the targeted minimum 500 µA is exceeded. Equal comparison in performance of simulated and manufactured operational amplifier proved unreasonable due to excessive effort of simulating process variations' effect.

Keywords: CMOS, integrated circuit, operational amplifier

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TIIVISTELMÄ

Petteri Toivanen: CMOS-operaatiovahvistimen suunnittelu

Kandidaatintutkielma
Tampereen yliopisto
Sähkötekniikka
Toukokuu 2021

Operaatiovahvistin on elektroniikassa laajalti käytetty komponentti, jonka avulla virtapiireissä toteutetaan erilaisia toimintoja. Pelkistetysti operaatiovahvistin itsessään on vain vahvistin, jonka toiminta määrittyy ulkoisten komponenttien kytkentöjen perusteella. Yleiskäyttöisen operaatiovahvistimen tyypillisiin ydinominaisuuksiin kuuluu suuri vahvistus, korkea sisäänmenoimpedanssi ja matala ulostuloimpedanssi.

Tämän työn tavoitteena on suunnitella 2,2 V:n käyttöjännitteellä ja enintään 500 µA:n tyhjäkäyntivirralla toimiva operaatiovahvistin mikropiirikäyttöön. Minimikuormatavoitteena on 100 Ω:n resistanssi. Suunnittelutyössä käytetään ilmaista piirisimulaattoria ja alkeellisia sähkötekniikan yhtälöitä.

Vahvistinpiirin pohjana käytetään Texas Instrumentsin LM358-operaatiovahvistimen rakennetta. LM358:n bipolaaritransistorit vaihdetaan kuitenkin eristehilatransistoreihin, koska ne soveltuvat bipolaaritransistoreja paremmin integroitujen piirien tarpeisiin muun muassa pienemmän virrankulutuksen, matalamman käyttöjännitteen ja yksinkertaisemman rakenteen ansiosta. Ideaaliset komponentit korvataan mahdollisuuksien mukaan vastaavilla transistorirakenteilla pyrkien realistiseen mikropiirisuunnitteluun.

Suunnittelussa painotetaan iteratiivista graafista analyysia. Sisääntulolohkon transistorien toiminta-aluetta arvioidaan, minkä jälkeen tarkempi toimintapiste haarukoidaan iteratiivisesti transistorien mittoja muuttamalla. Vahvistimen puskuri- ja ulostulolohkon transistorien mitoitus tehdään alkuarvauksen jälkeisten biasvirtojen ja -jännitteiden numeerisen ja visuaalisen tulkinnan pohjalta. Transistorien virta- ja jännitekuvaajia käytetään yksittäisten transistorien toiminta-aluetarkasteluun ja sinimuotoisen sisääntulosignaalin etenemisen seurannalla arvioidaan lohkojen toimintaa.

Tässä työssä suunniteltu operaatiovahvistin toimii 2,2 V:n käyttöjännitteellä 100 Ω:n kuormalla simuloiduissa testikytkennöissä. Se tuottaa 59,7 dB:n vahvistuksen 11,9 kHz:n kaistanleveydellä ja on sisäisesti vakautettu. Vahvistimen tyhjäkäyntivirta on 634 µA, joten 500 µA:n enimmäistyhjäkäyntivirtatavoite ylittyy. Simulaatiomallin ja tuotetun komponentin välinen tasapuolinen vertailu todetaan liian monimutkaiseksi prosessivaihteluiden aiheuttamien epäideaalisuuksien mallintamisen haasteellisuuden vuoksi.

Avainsanat: CMOS, integroitu piiri, operaatiovahvistin

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SYMBOLS AND ABBREVIATIONS

BJT	bipolar junction transistor
CB	common base configuration
CD	common drain configuration
CE	common emitter configuration
CG	common gate configuration
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
CS	common source configuration
EF	emitter follower configuration
FFT	fast Fourier transform
FET	field-effect transistor
IC	integrated circuit
I/O	input/output
MOSFET	metal-oxide-semiconductor field-effect transistor
SF	source follower configuration
SPICE	simulation program with integrated circuit emphasis
op-amp	operational amplifier
p-p	peak to peak
V_{DS}	drain-source voltage
V_{GS}	gate-source voltage
V_G	gate voltage
V_{TH}	threshold voltage

1. INTRODUCTION

Modern integrated circuit (IC) design must consider broad range of physical phenomena including not only the unidealistic nature of components but also the effects caused by different materials and interconnects [1, p. 608]. That is why the design today takes advantage of calculative power of computers to model the complex nature of circuits. Complexity of non-linear transistor characteristics and their parasitic phenomena demand tedious calculations when done by hand, so the designing is often executed by a simulation program with integrated circuit emphasis (SPICE).

Transistor behaviour in circuitry can be examined by inspecting single transistors as amplifier configurations, which means individual blocks with distinctive characteristics. They are named after the terminal that is common to input and output of the block. For bipolar junction transistors (BJT) the amplifier topologies are called common emitter (CE), common base (CB) and common collector (CC), which is also called emitter follower (EF). CE characterizes as inverting voltage amplifier with moderate input and output impedances. CB differs from CE by having lower input impedance and no signal inversion. EF is an attenuator with impedances high in the input and low in the output. [2, p. 253]

The field-effect transistor (FET) counterparts are respectively named common source (CS), common gate (CG) and common drain (CD) or source follower (SF). CS, like CE, inverts and amplifies the input with moderate output impedance but it also presents high input impedance. CG's and SF's properties are superficially the same as CB's and EF's, respectively. [2, p. 340]

The key benefits of using metal-oxide semiconductor field-effect transistors (MOSFET) in IC design, instead of BJTs, are superior energy efficiency and smaller size [3, p. 414]. These features are beneficial because they offer less heat production, lower operating voltages and power consumption, and denser circuitry. Another major upside is the ease of scaling. Due to simpler structure than the one of BJT, for MOSFETs it can be done by simply changing the physical dimensions, especially channel length and width of the device [2, p. 277] [4, pp. 17—18].

MOSFET-based circuits are further divided into three main technologies: NMOS, PMOS and CMOS (complementary metal-oxide semiconductor). NMOS- and PMOS-logics use only one channel polarity transistors, whereas in CMOS both are used. For IC Design CMOS is a good choice, because it generally dissipates the least power and operates at smaller total currents compared to other main MOS-logics [5, p. 5].

Different generations of MOS technologies are traditionally separated by the minimum feature size or gate length the manufacturing process can generate. The node size has shrinked over time and in today's consumer electronics it has reached 5 nm [6]. However, the 350 nm process used in this work is still in use for operational amplifier design research [7] [8].

On course Microelectronics II, spring 2020, a version of Texas Instruments LM358 operational amplifier was designed by simulating performance with PSpice. The amplifier was constructed in the simulator using discrete BJTs and it is presented in appendix A. A new approach on the same circuit is to recreate the op-amp in CMOS using only freeware SPICE LTspice, along with simple formula. The target of this work is to create a fully functional version of the real op-amp using easy-access tools and basic algebra.

Because of requirements of the amplifier structure, like several transistors supplied in series, a very small node process would potentially cause unwanted structural changes in the circuit. This is due to lower supply voltages used in smaller nodes. It would also require excessive research on suitable transistor model files for LTspice. The parasitic phenomena and physical limitations manifesting at sub-100 nm processes as mentioned in [9, p. 1] would need very sophisticated component and circuit models. As an older technology node, 350 nm has more reliable and accessible models and its common 3.3 V supply voltage seems high enough for this design. However, a lower 2.2 V supply is used to experiment on design limits.

Operational amplifier is essentially a high-gain amplifier used to apply different operations in circuits [5, p. 344]. These arithmetic or functional operations are performed by the use of external components around the amplifier [10, pp. 122—127]. Ideal op-amp properties include infinite input resistance, infinite amplification and zero output resistance [1, p. 7].

The op-amp to be designed in this work aims at full functionality in test circuits, ability to drive 100 Ω load and gain as high as possible. Maximum of 500 µA total current consumption is considered a secondary goal. The input resistance of MOSFET gate is given by the transistor model and is therefore not a design goal in this work.

The structure of the original BJT amplifier and designing the CMOS version is examined in chapter 2. The latter amplifier's performance is tested in chapter 3 and results and evaluation are concluded in chapter 4.

2. DESIGNING THE OPERATIONAL AMPLIFIER

The real LM358 is a BJT amplifier designed for single and dual supply op-amp use. Its structure was chosen because it is simplistic and easy to break in functional blocks. The functional schematic in Figure 1 is deliberately designed to give enough information for estimated analysis on performance and nature of the amplifier. To be able to mimic its behaviour it is necessary to understand the circuit topology and signal propagation within.

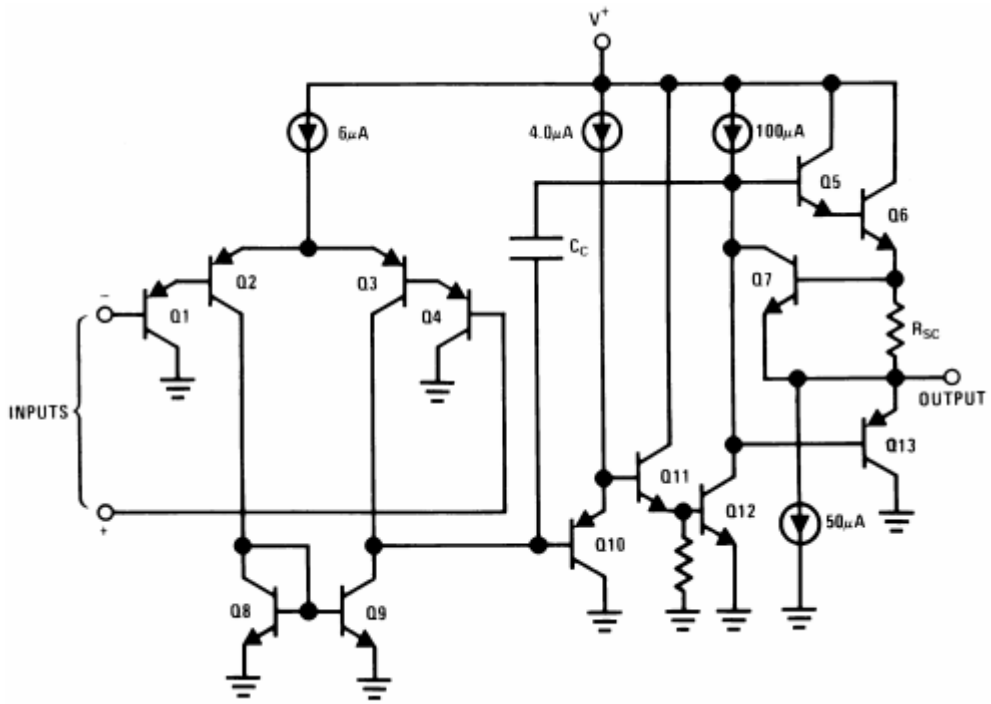

Figure 1. *The functional schematic of LM358 as presented in TI datasheet [11, p. 13].*

The amplifier's inputs are connected to differential input stage Q1—Q4 loaded with active load of current mirror Q8—Q9. This provides high impedance inputs and some amplification. [2, p. 486]

The next stage is a buffer consisting of Q10 and Q11. They separate the input from the output to avoid loading in between stages. Input stage's differential amplifier's performance would suffer significantly if it was affected by output stage's potentially lower impedances. Q12 is a CE amplifier. Q5—Q6 and Q13 form a push-pull output stage and Q7 with R_{SC} is acting as a current sink to ground if the current in the amplifier output rises too high compromising the endurance of the output transistors.

2.1 Signal propagation of the CMOS amplifier on individual transistor level

Alterations in the structure of the BJT amplifier had to be made to maintain similar operation for the CMOS version (Figure 2). Additional current sources were added to provide biasing for M1 and M4, which was done because MOSFETs do not conduct current through their gates. The output offset resistor was replaced with two diode connected NMOS transistors and the source resistor of Q11 was replaced with a transistor in resistor configuration. The reason for the changes was to pursue realistic IC design in which resistors are unwanted due to their larger size and bigger heat production compared to their transistor counterparts. The overload protection from the output stage was omitted because the output current did not become excessive even with grounded output due to low operating voltage and big output transistors.

The voltage of inverting signal input Vin- is transferred from gate of M1 to the source terminals of M2 and M3 by the SFs M1 and M2. SFs express very high input impedance [2, p. 334] which is beneficial for the input stage as it minimizes the differential pair's effect on the signal source [2, p. 355]. From there the signal propagates through CG M3 where the inverting and non-inverting inputs are subtracted. The CG amplifies the difference in between inputs by the transconductance of M3 multiplied by high dynamic resistance of M9, current of which is very stiff due to diode connected M8 controlling it [2, p. 486].

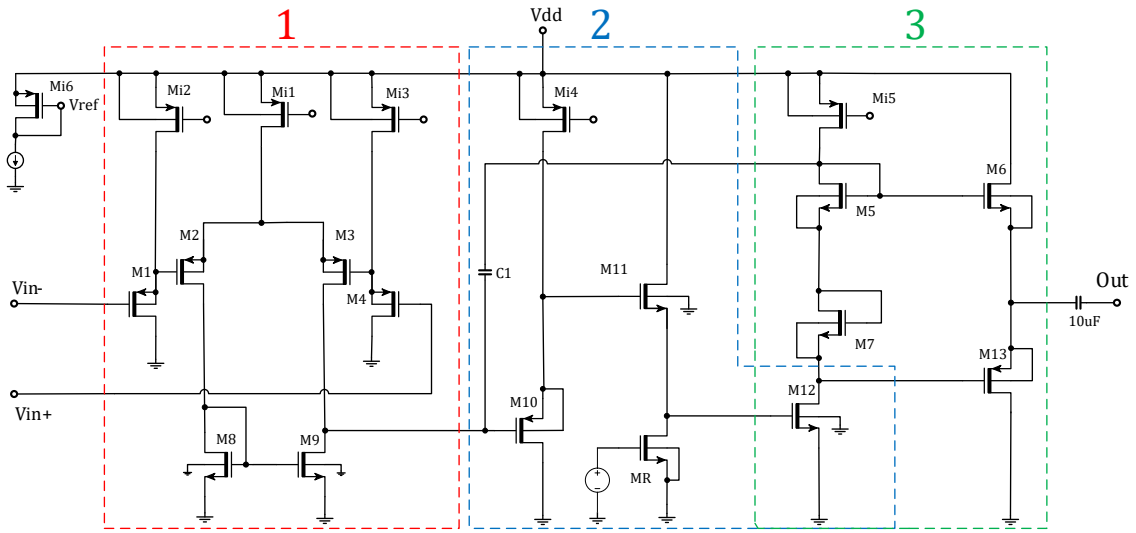

Figure 2. *The CMOS-compatible structure of the amplifier. 1: input, 2: buffer, 3: output.*

The signal in the output of the differential stage is again followed by SFs M10 and M11 which provide effective isolation in between the stages causing some attenuation. Transistor MR both biases the M12 gate and delivers the signal from the buffer.

M12 is a CS amplifier loaded with a current source and two diode-connected transistors M5 and M7, allowing its amplification to be potentially very high. Output of M12 is controlling gates of M6 and M13, which take turns conducting depending on the magnitude of the signal. As SFs, they provide low output impedance for the amplifier.

2.2 Designing input stage

The main function of the input stage is to amplify the input signal to the next stage with minimum amount of distortion and a virtue to it is to also support low-impedance sources. One way to fulfil these goals is to take the input on MOSFET gate which ideally resembles an open circuit and thus infinite resistance. Differentiating input is beneficial because of its superior noise performance by reduction of common mode noise [4, pp. 2—3] meaning the part of the input that both terminals receive. In this application, albeit being slower in frequency domain than N-channel devices due to major charge carriers' lower mobility, P-MOSFETs are not only loyal to the original structure, but a justified choice for the input because of their better noise figure [5, p. 232].

The goal was to keep the structure as unchanged as possible, but the first input transistors M1 and M4 were biased with additional current sources because the transistors itself cannot drag any reasonable current through the MOSFET gates of M2 and M3.

It is desirable to maintain the current consumption at minimum to minimize wearing and power consumption. Long channel transistors' capacitive parasitics at higher frequencies and relatively slower p-type transistors suggest that the channel length of the transistors should be kept as short as possible. The 350 nm CMOS technology offers 350 nm as the minimum possible channel length, so it is the starting point for every iteration. After the length is set, width is varied to find operating point which satisfies desired DC voltages, currents and other design constraints.

For connecting the fourth transistor terminal the rule of thumb is that transistors' bulk is connected to same potential with it's source. Other connections are also possible for example using a lower voltage for n-channel MOSFET to decrease the threshold voltage, which means sufficient gate-source voltage for opening the transistor channel [4, p. 17]. If the source terminal is not tied to a steady voltage reference, the threshold voltage can

vary with the signal. This alteration is called body effect [5, pp. 20—22] and it is useful to acknowledge as a design choice.

Bias design of the input stage starts from single key parameter tying the whole stage together, which is the voltage on sources of M2 and M3, referred as *Vx*. Its magnitude is approximately supply voltage V_{DD} minus voltage drop over the positive channel MOSFET current source. Relations to *Vx* within the input stage are presented in Figure 3.

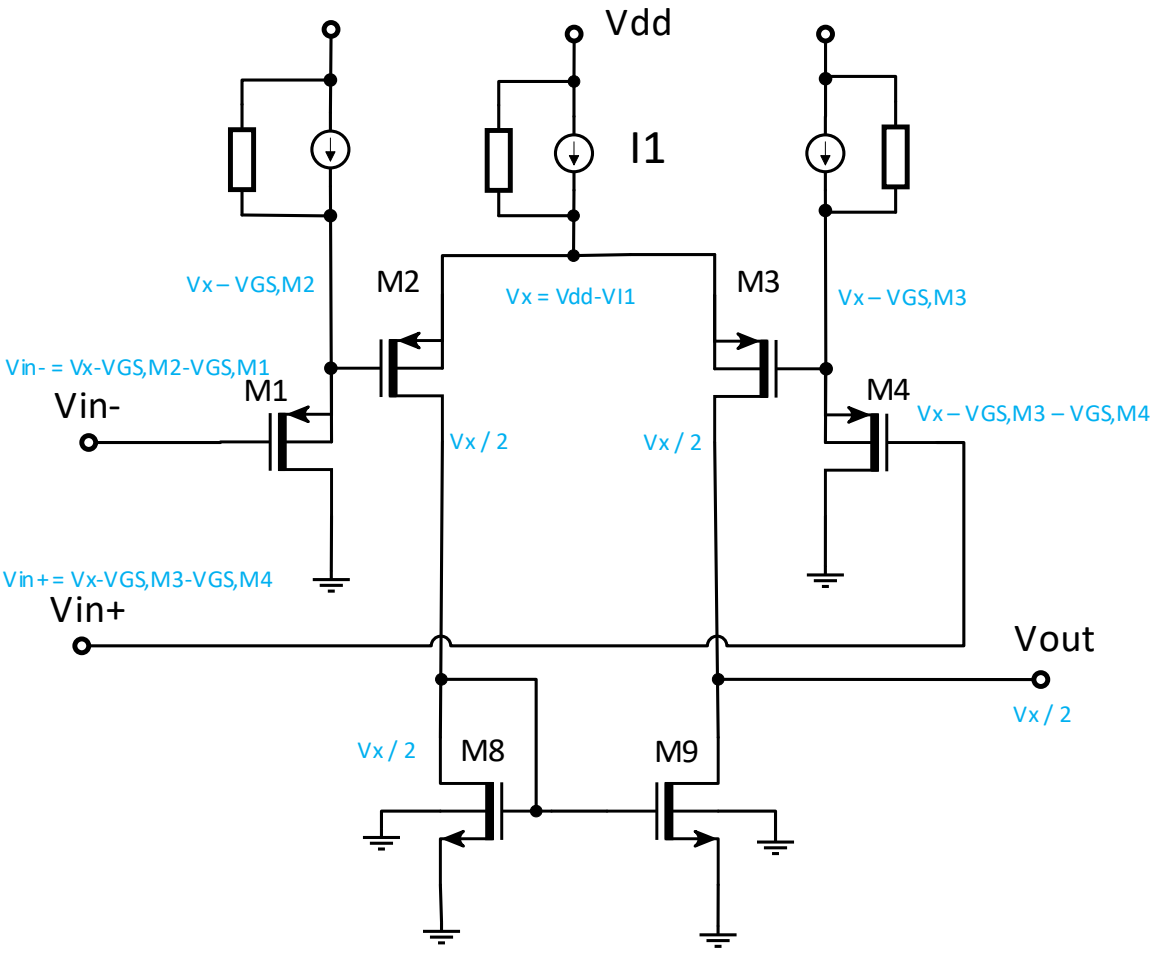

Figure 3. *The relations to* Vx *in the input stage.*

Vx dictates maximum input bias voltage to be two PMOS gate-source voltages below it. In the LM358 datasheet [11, p.13] it is recommended for single-supply applications to bias the input DC levels to half of the supply voltage when possible to maximize input range. 2.2 V supply used in this design cannot reach that goal because inputs are always more than two PMOS voltage thresholds below the supply meaning it would be less than a volt.

The output DC bias should be around half of the *Vx* to pursue maximum output swing range. Later in the design it can be optimized to some other value if a following stage is a more strict bottleneck for the range or a large fluctuation headroom for this node is otherwise unimportant. The largest range of symmetric voltage amplification is preferred until further information.

To determine the voltage *Vx*, PMOS current source test bench (Figure 4) was simulated to find out the voltage headroom required for such. Voltage supply V1 provides the bias voltage on the sources of the transistors and is scaled to match the supply voltage of the amplifier circuit. Current source I1 sets current through P-MOSFET M2 which forces the gate voltage to match the current which is thus copied by M1 since the gates are at same potential. Voltage source V2 is swept to define the minimum drain-source voltage in which the current mirror arrangement can keep its nominal current. The multiplier parameter m represents amount of parallel devices which effectively multiplies the current reference. Using the multiplier arrangement lowers the current consumption because the reference current does not need to be more than a fraction of target current. Current mirrors perform better with long channel transistors due to being less sensitive to channel length modulation, meaning the variation in the current in saturation region [2, pp. 288—289].

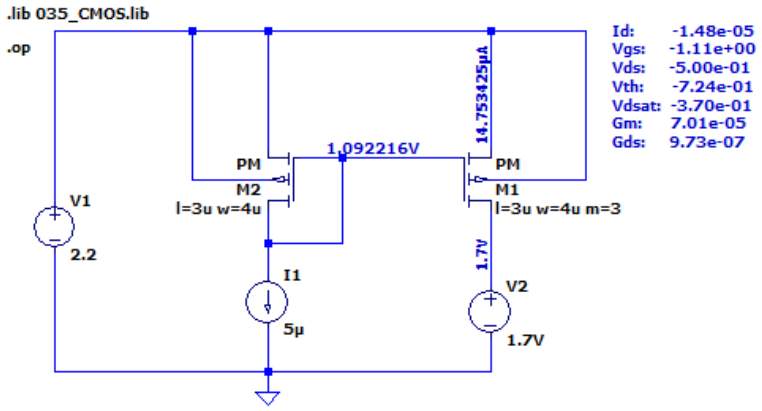

Figure 4. *The current source scaled for pushing 15 µA current. Certain useful copying transistor M1's parameters are presented next to the circuit.*

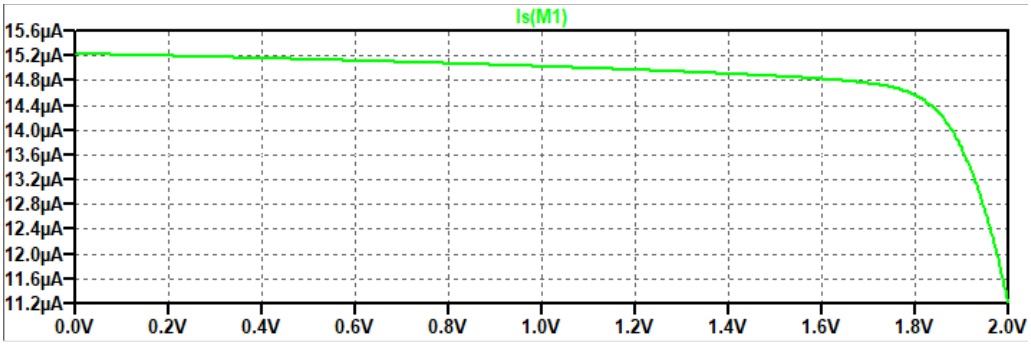

Figure 5. *Relatively steady current achieved with sizing L=3u W=4u. It shows stable behaviour ranging until around 500 mV VDS.*

With V2 voltage at 1.7 V, the transistor has 500 mV left over it from the 2.2 V of V1 (Figure 5). This 1.7 V can be used as initial guess for the voltage to reserve for the rest of the differential stage.

In the transistor properties (Figure 4) it is stated that VDSat equals 370 mV. VDSat expresses how much the gate-source voltage is above the threshold. To keep enough safety margin in maintaining transistor in saturation, the same previously approximated 500 mV holds and can be used to define the *Vx*. Hence the voltage headroom for rest of the circuit will be 1.7 V. Next task is to scale the dynamic load, which essentially is a current source as well.

In this design the current fluctuation is not very critical after the circuit is in balance, so trading steady current to smaller size is possible as long as the current remains at the correct range to offer the great load of dynamic resistance for the amplifying transistor. The small size is desired to decrease the effect of transistor's internal capacitances to the speed of the stage.

When scaling the NMOS current mirror for the load, the right range is considered sufficient instead of exact numbers. It is because the primitive test bench is not ideally fit for the final circuit in question. One major benefit of using a SPICE is the ease of iteration, so it is justified to first bias the whole stage and then finetune the complete circuit to inspect the more delicate relations within. In NMOS current mirror test bench (Figure 6) the control current is set with I1 and the V_{DS} of M1 representing M8 of the op-amp is swept with V2 to define its range of successful current copying. Transistor sizes are parametrized for smoother iteration; current values are presented in *.param* statement to be 500 nm of length and 700 nm of width. These values provide V_{DS} operating margin up from 400 mV (Figure 7).

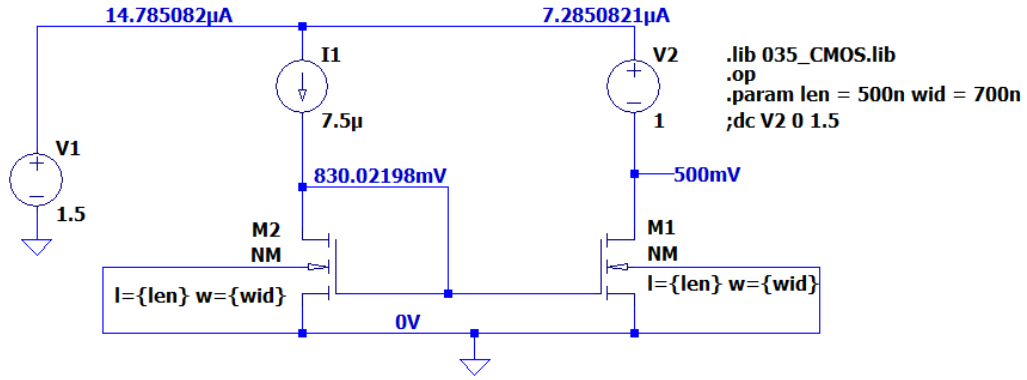

Figure 6. *Completed initial scaling for the active load at operating point with bias at 500 mV over the load.*

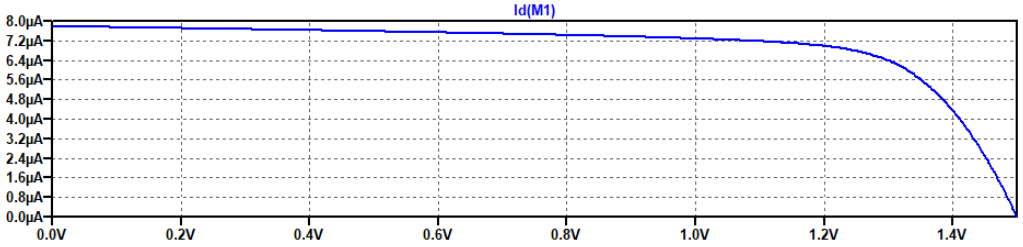

Figure 7. *The current of M1. The current mirror performs up to around 1.5 V - 1.1 V = 400 mV V_{DS} with some safety margin.*

The next phase is to balance the drain of M2 to drain of M8, which in the end should be around the same 850 mV point to match the output DC level. As the current is known as well, all there is to scale is the gate voltage and size of the transistor.

Suitable operating point can be narrowed by plotting the input characteristics of M2. The transistor can be initially biased to a little lower current than the 7.5 µA to make it more conductive in order to provide more of the voltage headroom on the active load, it will also compensate for the little error caused by channel length modulation in both the current source and the sink.

A simple PMOS test bench (Figure 8) was used to fit M2 to the chosen bias point.

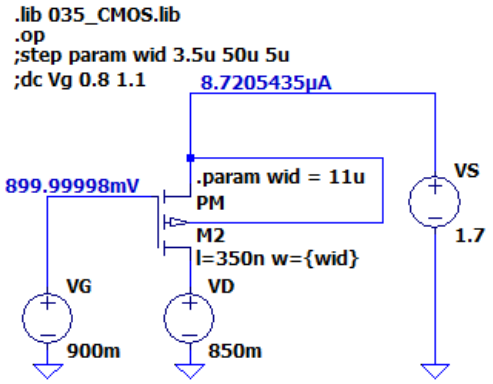

Figure 8. *A PMOS test bench for defining the component values with a decent fit for the design.*

After being satisfied with M2's performance, the Gate voltage of M2 is set to 900 mV, which determines the Source voltage of M1. M1 V_{DS} is then also locked to 900 mV as the drain is grounded in the circuit. The body terminal gives some freedom in IC but usually it is at best when connected to the source as it will keep the V_{TH} flexible which is crucial when working around a narrow marginal. M1 scaling is focused on splitting the V_{DD} with the current source on top in the right proportion to produce the already set V_G of M2.

As M1 is the last undefined component, the whole stage can be built. For indicators of good bias the source current magnitude was monitored while setting M2 gate voltage, which was supposed to be 900 mV.

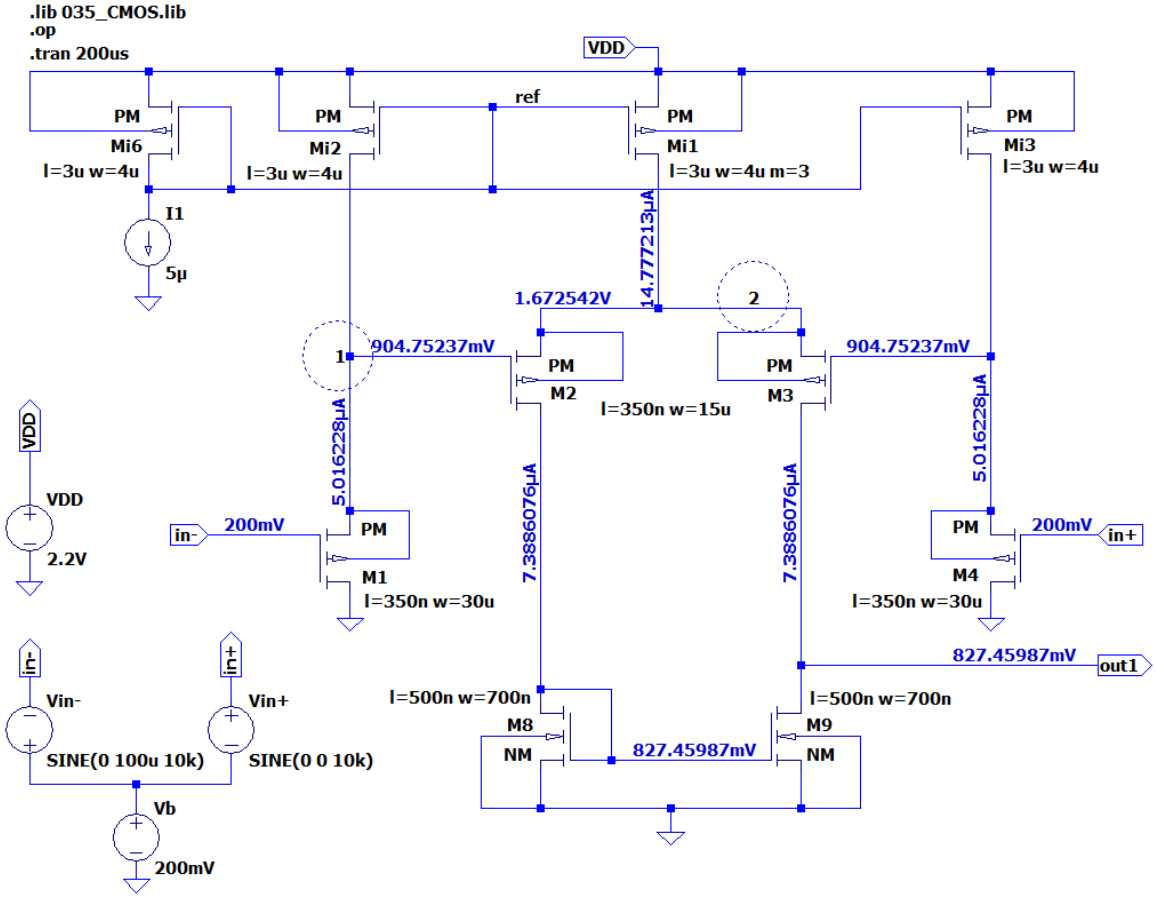

Figure 9. *The first iteration bias construct of the differential input stage showing bias point succesfully in the ranges derived in the individual test benches.*

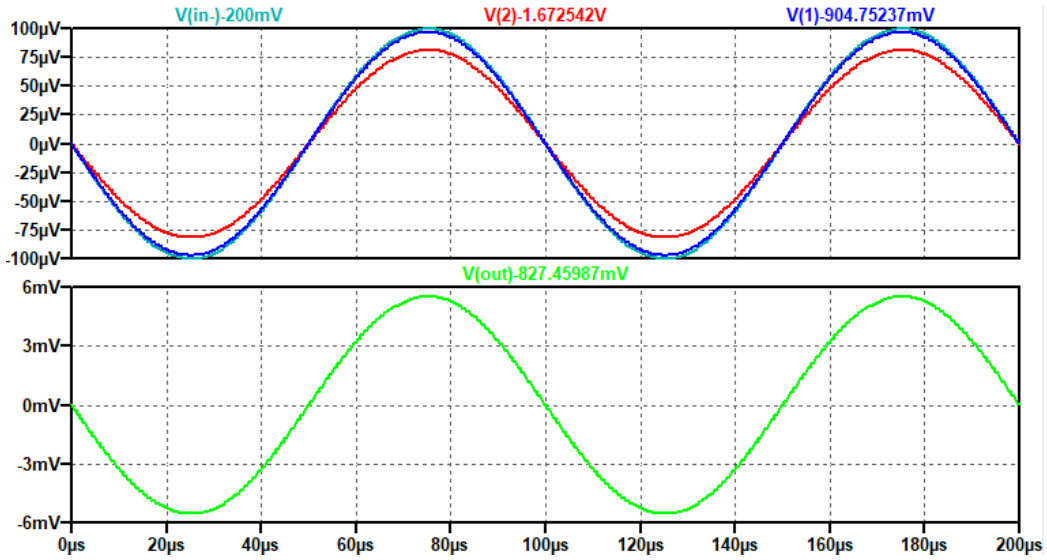

Figure 10. *The transient plot of the signal propagation through the stage shows that the input signal is expectedly attenuated over first two transistors (top pane) and amplified in the output (bottom pane).*

As seen in Figure 10, the input stage combined at Figure 9 is superficially serving its purpose. The input is amplified by a factor of 30 and attenuation over the first transistors seems modest. Further inspection could be made but as the output voltage is just the initial guess, the rest of the amplifier can be done next and input stage re-worked if found necessary, latest in the final performance inspection.

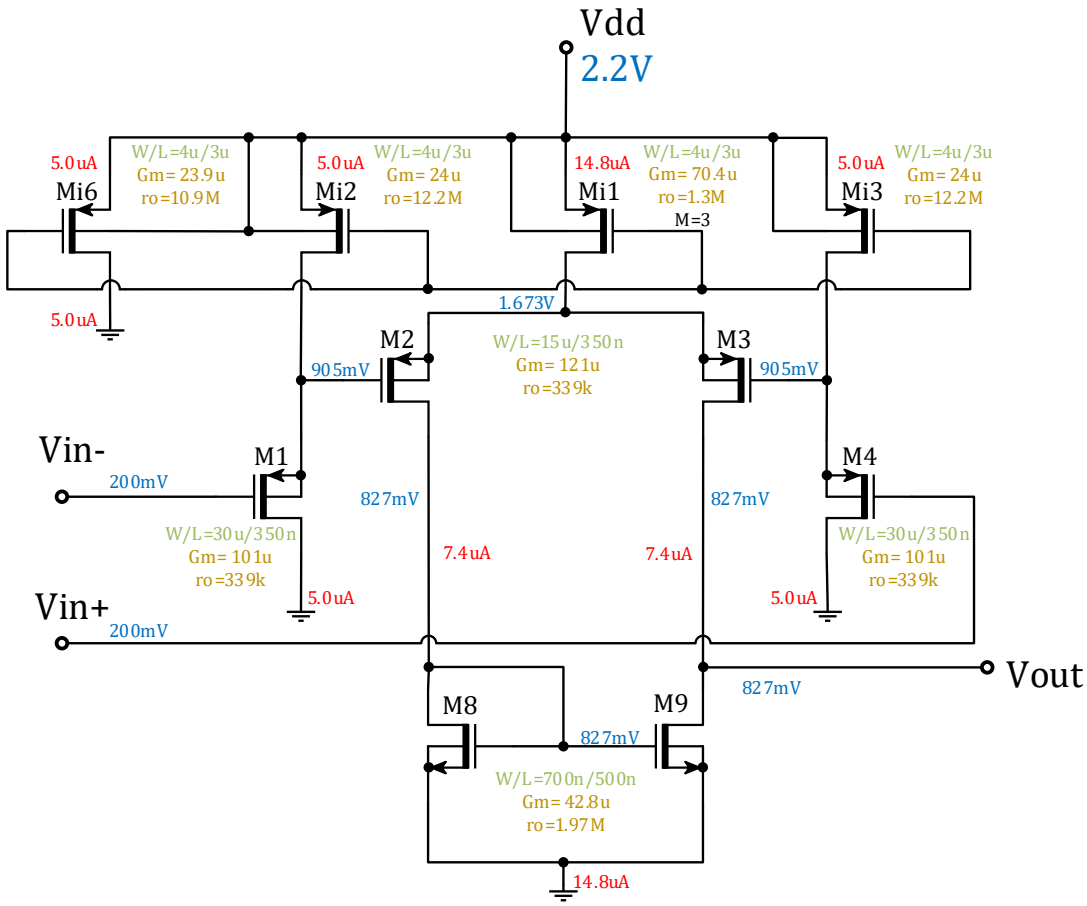

Figure 11. *The CMOS version of the input stage.*

Figure 11 presents the finished idle bias point of the differential input stage and certain distinguishing transistor parameters.

2.3 Designing buffer and output stage

The intermediate stage could be also biased separately if the desired output stage DC bias was known in advance.

In this design process the buffering stage is merged with the output because the separate evaluation is not beneficial due to optimal buffer output being heavily dependent on the output setup's bias requirements. As the buffer is functioning as a control point for the output, it can be effectively constructed with the buffer stage attached to it. The input can straight away be included as well, although the bias hardly interacts with output due to heavy buffering so it does not probably provide further integrity to avoid possible compatibility issues. This may help with evaluation of bottlenecks in performance.

The function of the output stage is to ensure that the amplifier remains under safe and stable performance even when driving very small loads when the current can become very high, and in this case that the amplifier can drive very small loads without major losses in performance. Both can be expressed as having small output impedance. As in the BJT emulated circuit, the deadzone of the push-pull output stage is removed with a voltage shift in between the gates but instead of a resistor, two diode-connected transistors are used. The inital structure is presented in Figure 12.

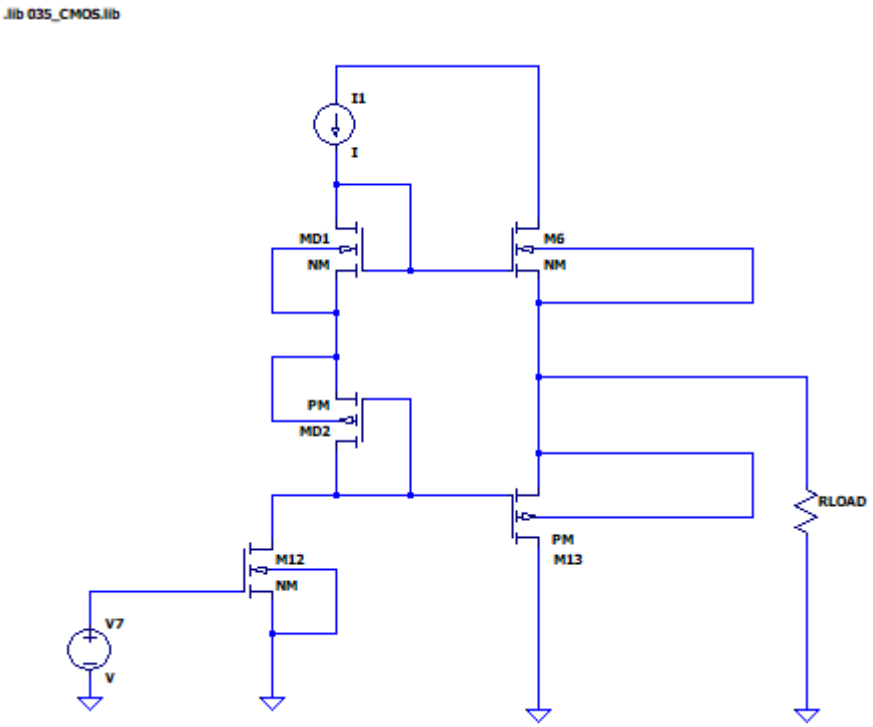

Figure 12. *The initial schematic of the output stage.*

Due to symmetric structure, the DC bias of the output should be half of the supply voltage to aim for maximum output range. That equals 1.1 V in this design. The swing in the gates of M6 and M13 will be the bottleneck of the voltage swing, as it is experiencing the largest small-signal swing due to the last amplifying device being M12. Hence, the output will face an attenuated signal from the two SFs M6 and M13 and it is not as restricted from either side.

Since the objective is to drive a load as low as 100 Ω, the current each device should aim to be able to conduct is relatively high given supply voltage of 2.2 V. This can in this structure offer up to 2 V over the 100 Ω resulting in 20 mA current according to Ohm's law. To achieve high current endurance, large physical size cannot be avoided. The current can also be restricted with less sensitive output transistors but it would cause bigger attenuation and output impedance because the transistors idle and work in less conductive state.

Instead of excessive calculations, some arbitrary values were set for the transistors to get started with the optimization. The current should be high for gain in M12, assumed moderate 2-3 times the current of the input stage. In this phase it is set to 40 µA. Integer multiplier for the input stage current mirror is practical as the whole circuit can be biased with a single reference current generated externally to the op-amp.

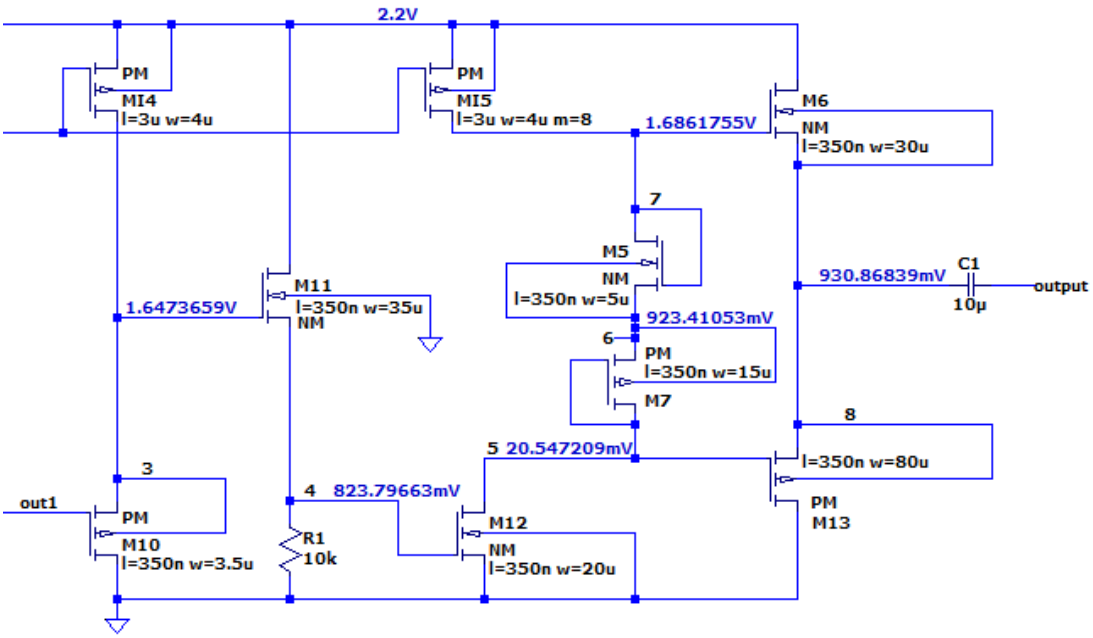

Figure 13. *Merged buffer and output with an approximated scaling shows clear errors in bias voltage levels.*

Unsurprisingly, most of the initial guess values need heavy optimization as seen in Figure 13. The most apparent problem is the 20 mV on the drain terminal of M12. The desired value is one PMOS threshold voltage below output target 1.1 V which leads to the range of 1.1 V minus PMOS V_{GS}. With V_{TH} being around 700 mV, this results in 400 mV. One possible cause can be tracked to the voltage shift diodes consuming too much voltage. Initial solution attempt is to change the PMOS to an NMOS and making both diodes wider. If the voltage shift is then not enough to remove the deadzone the size can be downscaled.

Another thing to tune is the second buffer stage consuming huge current. An optimal gate voltage for M12 could be around 600 mV. This is because NMOS of this model tend to have V_{TH} of up from 500 mV and with only 400 mV on its drain there is not much headroom for V_{DS} to go below V_{GS}-V_{TH} to satisfy saturation condition $\mathrm{VDS} \geq \mathrm{VGS} - \mathrm{VTH}$ [12, p. 75].

The last thing to control the M12's drain is to tune the channel width of M11 to steer the current flowing through the resistor R1. 700 mV on M12's gate will also be over the resistance of 10 kΩ, current of which would then be 70 µA according to Ohm's law, which is still much but not intolerable. Yet, the resistance should also be increased to match the voltage to the current generated by M11. The current is depending on too many variables to calculate different scenarios effectively by hand, so iterative simulation in this situation with SPICE is beneficial.

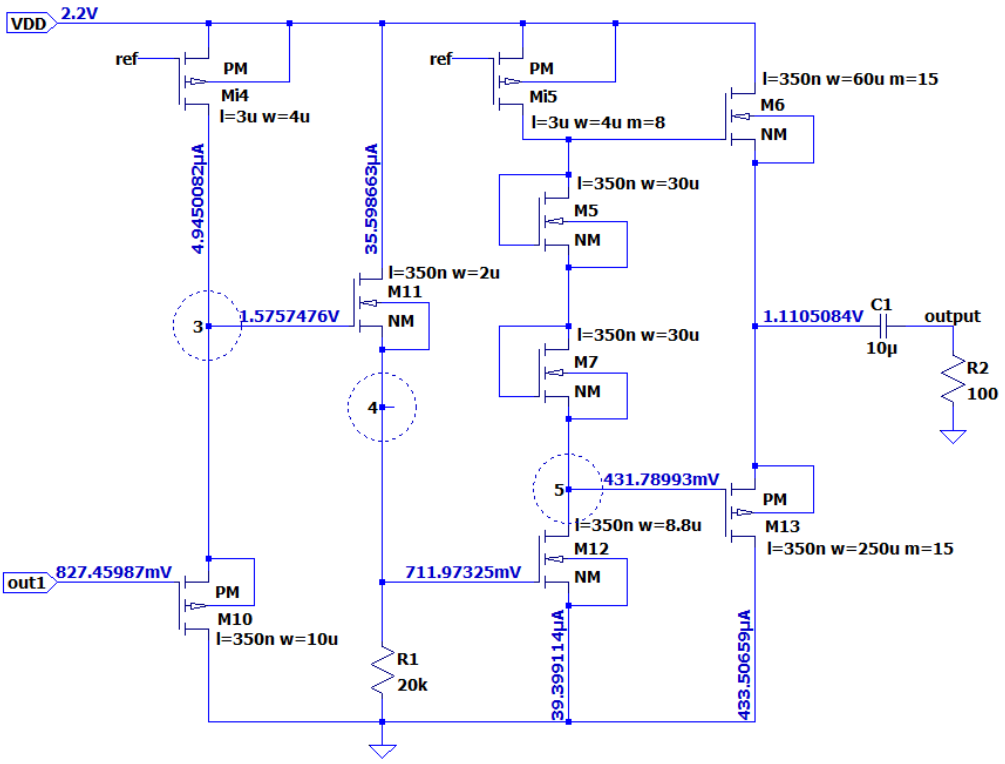

Figure 14. *The first improved scaling for buffer and output with bigger resistor R1 and tuned transistor sizes presents superficially acceptable bias point.*

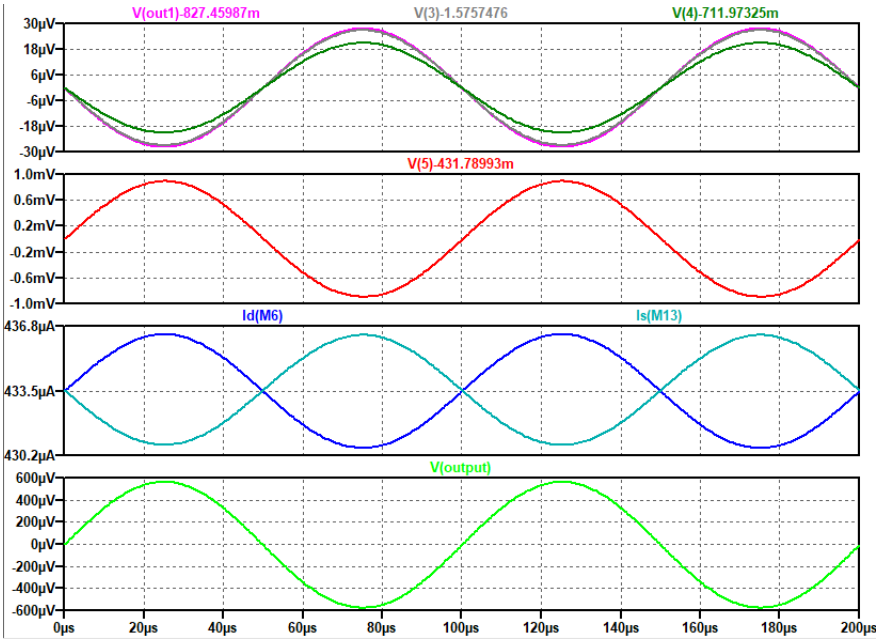

Figure 15. *The signal propagation through the buffer and output stage from top to bottom: attenuation in the buffer, signal after M12, currents of output transistors and the output signal of the low buffer current biasing.*

The improved buffer stage presented in Figure 14 is attenuating the signal a lot (Figure 15) by almost halving it, but it seems to be a trade-off for having proper gate voltage for M12 with reasonable bias current. To decrease the attenuation factor, M11 could be deeper in saturation, meaning it should have wider channel given the gate voltage would remain the same, but this would also mean radical increase in bias current.

This iteration's output circuitry biasing provides small attenuation in transition to output stage. This is caused by the bias current through the output transistors being remarkably high 433.5 µA. Idle bias current is high because the transistors need to be turned on to follow the signal with minimum latency. The minimal attenuation feature could be maximized by making the buffer current large as well and enlarging the output transistors with bigger multiplier and if needed, the diodes finetuned.

The output stage is not in this form behaving as push-pull output stage as both transistors are conducting simultaneously which makes the idle current consumption very high but lowers the output impedance. In IC design, however, the high bias currents are usually not desired and lower power consumption is to be considered a realistic goal because MOSFETs cannot compete against BJTs in plain amplification due to worse transconductance [2, p. 299]. To lower the output bias current significantly, the transistors M6 and M13 could be pushed to triode or even cut-off operating region. They would be slower to respond to incoming signal because they need time to open the channel, which would also attenuate the signal more but there would be next to zero bias current flowing through them when the amplifier is idle.

As the restriction to output impedance of supporting 100 Ω load is higher priority goal for the design, current target is omitted. Since the circuit is a compromise, the next improvement attempt will accept even further elevated power consumption to reduce the attenuation.

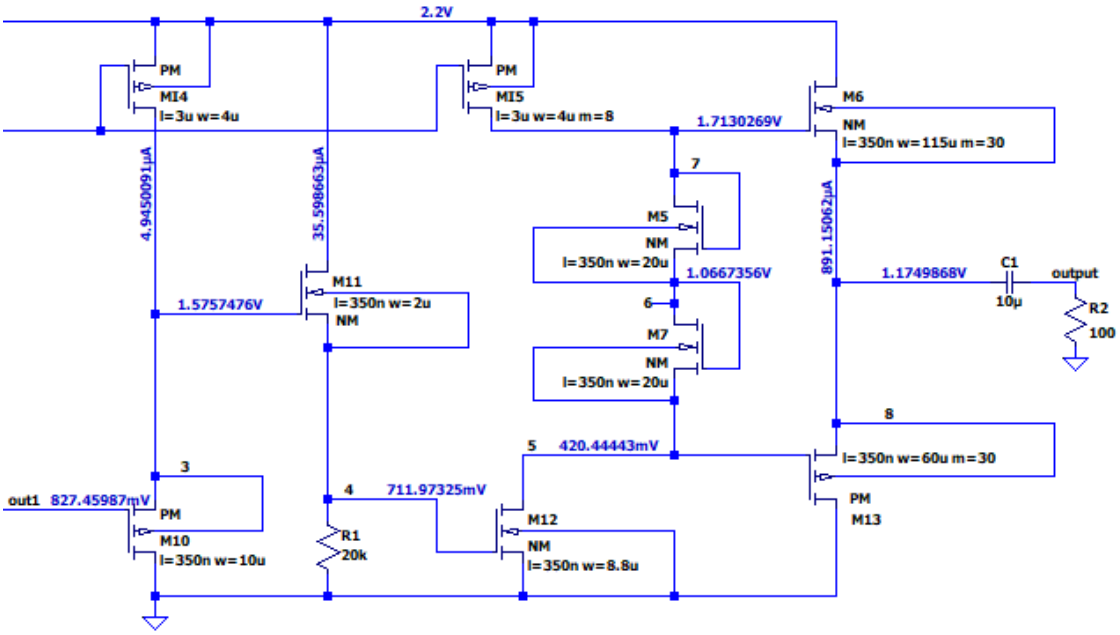

Figure 16. *Further improved output stage with emphasis on higher power consumption to preserve the signal level through the output stage shows increase in the idle current through last transistor pair.*

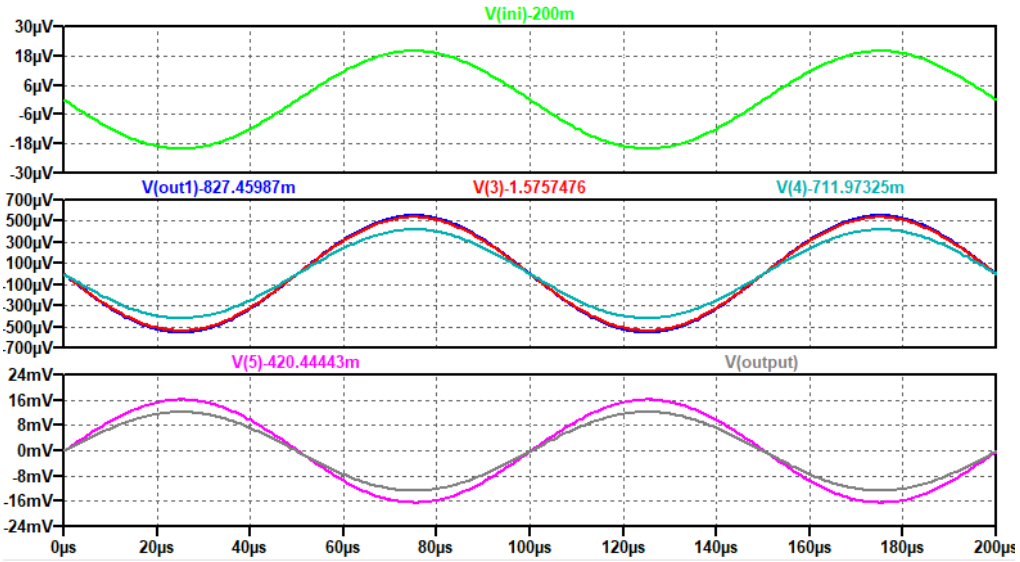

Figure 17. *Signal propagation through the whole amplifier from top to bottom: Input signal, differential stage and buffer output, M12 drain and output of the amplifier.*

The compromised biasing (Figure 16) of 25 % attenuation in the buffer and higher idle current consumption in the output results (Figure 17) show promising current range with still relatively heavy attenuation in the output. As the output attenuation seems like a bad choice, next iteration will again have focus on reducing current consumption.

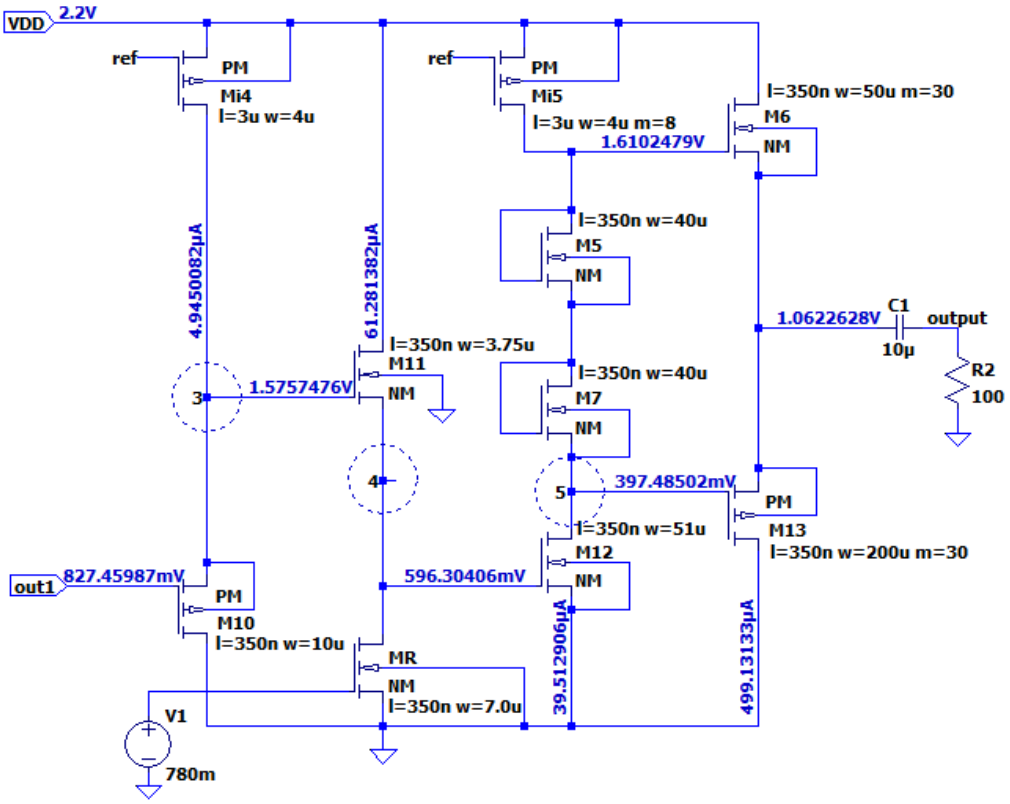

Figure 18. *The final version of the buffer and output stage transistor sizes and bias conditions performs with decent attenuation and moderate idle power consumption; the resistor is in this point replaced with a transistor.*

More convenient build introduced in Figure 18 is not as picky what comes to attenuation but is more suited for broad stable output swing range with decent gain and reduced but not minimal bias current.

Optimizations were done by resetting the M12 gate to around 600 mV and sized to provide 400 mV on its drain. This increased the current consumption of the buffer but along with tuning the offset diodes it decreased the bias voltage on M6 gate which provides better fit for the output DC level. The resistor was in this phase replaced with a transistor according to [5, p. 58] to decrease the physical size of the op-amp which is essential in IC design. The performance in time domain (Figure 19) was deemed satisfactory at this point with 20 % attenuation over the buffer, additional amplification of 66 times and 33 % attenuation over the output transistors with 100 Ω load and 1 µV differential input signal.

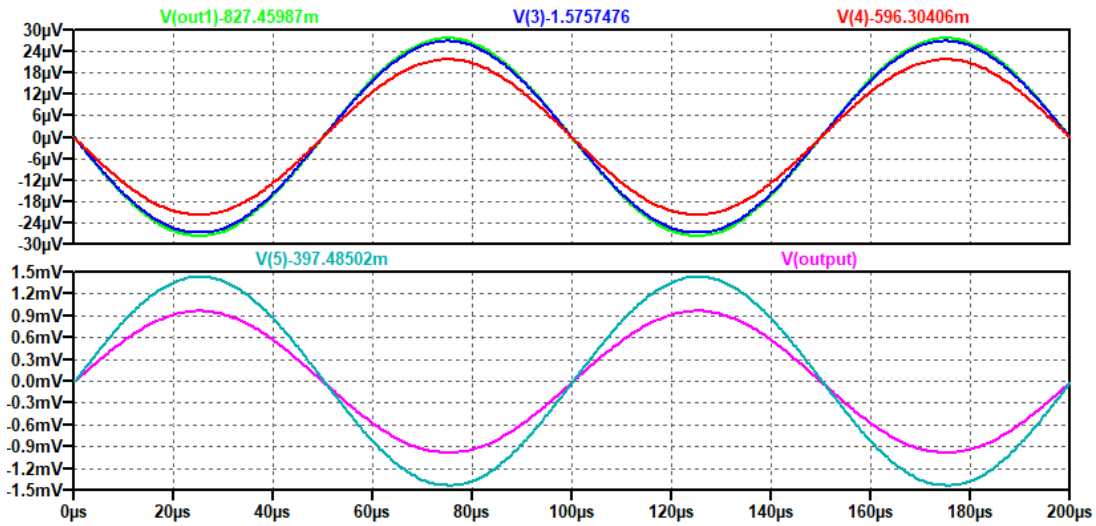

Figure 19. *The signal propagation through the buffer (top pane) and output stage (bottom pane) with biasing of* ***Figure 18*** *with 100 Ω load and 1 µV input signal.*

Stability inspection had to be done before proceeding to broader performance analysis, as the inverting amplifier can cause instability [3, p. 616].

The AC response (Figure 20) of buffer and output stage was examined to evaluate stability and supported bandwidth.

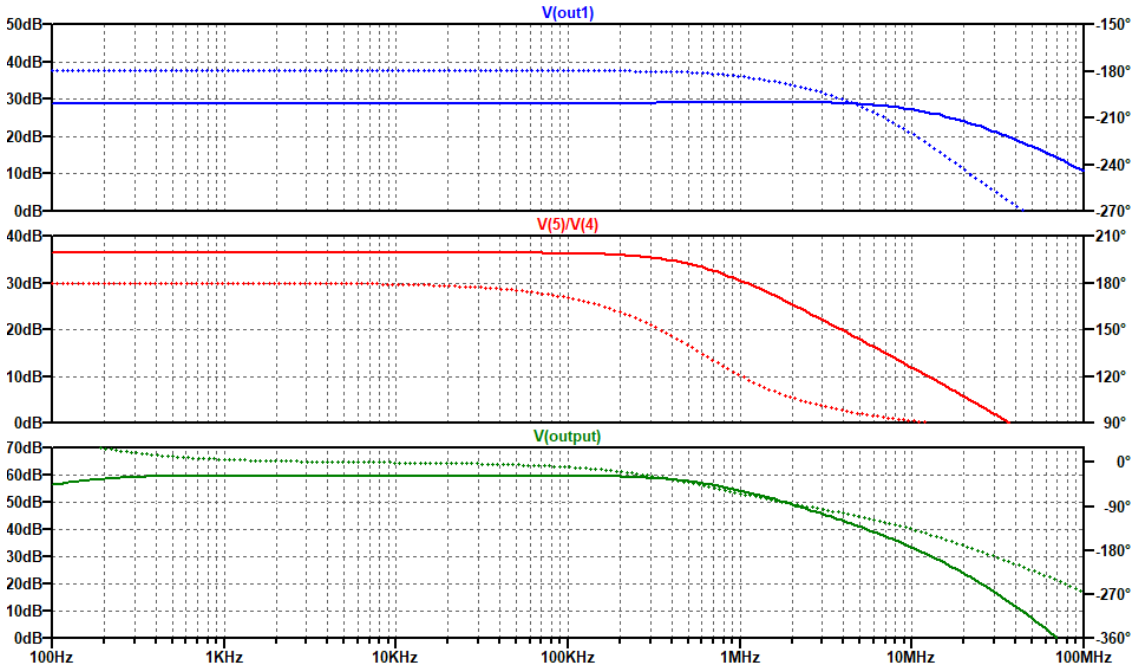

Figure 20. *Upmost plot presents the behaviour of the differential stage, middle plot is CS amplifier M12 and the bottom is output. Lower corner frequency results from coupling capacitor to maintain bias neglecting the load.*

The CS stage of M12 is clearly to blame for restricted bandwidth as further inspected in Figure 21. This is to be expected due to Miller effect amplifying the transistor's internal input capacitance by a multiplier equal to the gain of the stage [13, ch. 8.2].

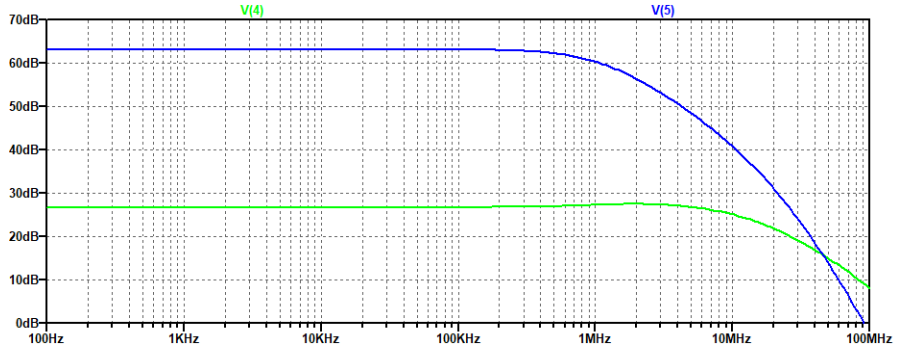

Figure 21. *The frequency response at node 4 before M12 and node 5 after M12 shows the radical decrease in useful frequency band.*

The output of the whole circuit (Figure 22) is the point of interest considering stability. The 300° phase shift at 0 dB level is not desirable for general purpose op-amp. An op-amp should be internally compensated to make it easier to use, although external compensation could be an option. For the amplifier to stay in stable operation, its amplification should reach 0 dB before the phase has shifted 180°. [3, p. 617] There must also be a safety margin of at least 45° [14, p. 195]. 60° phase margin would be safer, as described in [2, p. 623] but it would also require a bigger compensation capacitor. The choice depends on the required capacitor size to reach each phase margin. This means that the output's amplification should reach 0 dB before phase has shifted 120—135°.

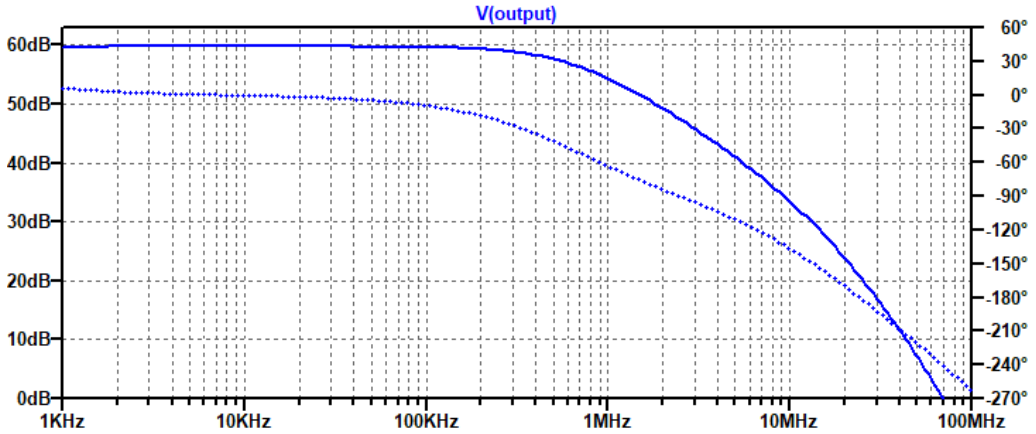

Figure 22. *The result of output's AC analysis shows around 240° phase shift at 0 dB level, indicating imminent instability.*

To increase the circuit's phase margin, a compensation capacitor will be added. It is to be placed as a negative feedback for an amplifying stage, in this design the CS stage M12. The Miller effect comes in handy in this arrangement as smaller capacitance can be used for compensation which is beneficial to spare silicon area. Compensation could be connected to various points for tuning the feedback properties, but original design has it over the buffer and the amplifying transistor hence that is the initial placing (Figure 23).

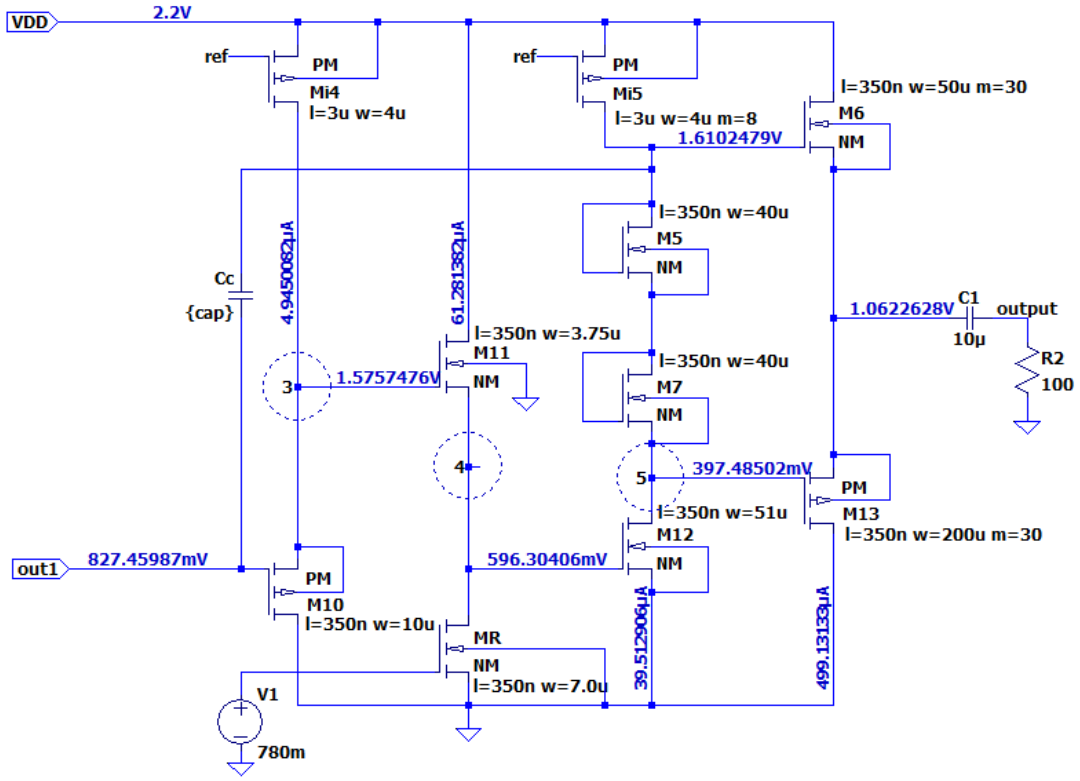

Figure 23. *The compensation capacitor Cc is initially placed over the buffer and M12 along with the voltage shift transistors.*

Keeping in mind that too big a capacitance would excessively narrow the bandwidth, it was examined starting from very small values. [3, p. 412] suggests that typical values for capacitors in IC range from 1 pF to 100 pF. First iteration is seen in Figure 24 where the 100 fF capacitor is offering some 100 kHz frequency band while 1 pF capacitance can provide around 10 kHz. The most promising trace in this sweep is the one of 1 pF as it is the first value with phase shift less than 135° at 0 dB level. More accurate value is further evaluated in Figure 25.

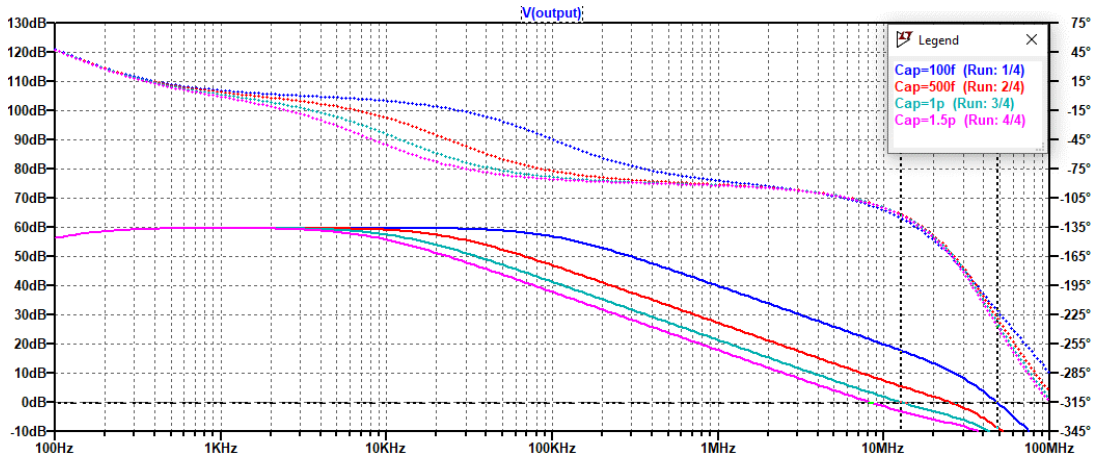

Figure 24. *Sweeping the capacitance of Cc shows that the amplification starts to drop on smaller frequency when the capacitance increases.*

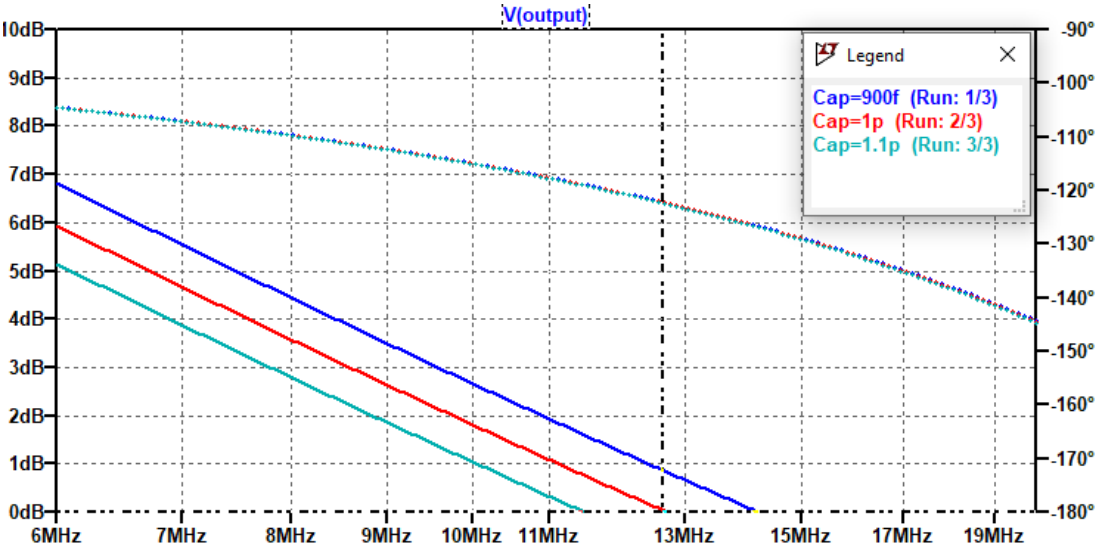

Figure 25. *1 pF capacitor offers 122° shift meaning 58° phase margin.*

1 pF capacitor was chosen as 58° seems decent phase margin exceeding the absolute minimum of 45°.

The bandwidth was measured to be 11.9 kHz. Narrow bandwidth is expected because aiming at high gain during the design process causes lousy frequency band due to the need to start limiting the gain on a lower frequency. To increase the bandwidth, the overall gain could have been lowered by degenerating the performance of CS M12 which would have led to smaller compensation. However, this was a satisfactory result for this work at this point.

3. PERFORMANCE ANALYSIS

Now that the amplifier design was ready, its performance was analyzed. Table 1 presents certain characteristic values. The simulated performance is not reliably comparable with real datasheets because proper benchmarking would better fit more honed product. Accurate and considerate measurements would take much more effort than designing the whole amplifier this way, as test conditions should be standardized. The values are meant for superficial examination and for finding clear errors in design.

Table 1. *Simple benchmarks of the operational amplifier with 100 Ω load.*

SUPPLY VOLTAGE	2.2 V	
CURRENT CONSUMPTION	634 µA (idle)	
POWER CONSUMPTION	1.4 mW (idle)	
VOLTAGE GAIN	59.77 dB	973 V/V
BANDWIDTH	11.9 kHz	
INPUT RANGE	240 µV p-p	
OUTPUT RANGE	222 mV p-p	
INPUT IMPEDANCE	1 kHz: 30 GΩ 11.9 kHz: 2.55 MΩ	
OUTPUT IMPEDANCE	1 kHz: 44.5 Ω 11.9 kHz: 45 Ω	

3.1 Power consumption

Idle power consumption can be measured as the product of voltage power supply and its current without an input signal. Idle current consumption of power supply is 634 µA, which means the power consumption is 1.4 mW. Current consumption of the offset voltages can be omitted as MOSFET gates cannot draw DC.

Targeted minimum of 500 µA idle current was exceeded. This was a design compromise to support the 100 Ω load.

3.2 Dynamic range

Maximum input and output ranges were examined through the whole design process to control the amplifier's limitations and abilities along the way. The ranges are no longer known in this design after adding the internal compensation. Looking at the waveform to determine the integrity of the signal by eye can lead to the correct range but more accurate way is to use the fast Fourier transform (FFT) to analyze the purity of the output's sinusoid. This was done by plotting hundred periods of the output and using the FFT to plot the frequency components of the output.

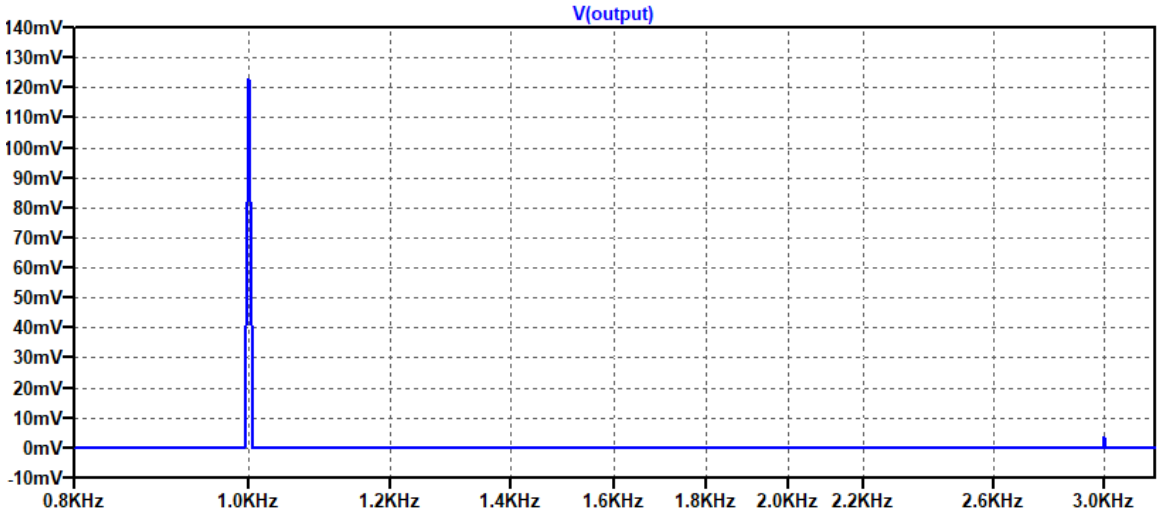

Figure 26. *The FFT for 100 periods of the output signal at 240 uV p-p differential input voltage with 1.9 % peak at 3 kHz.*

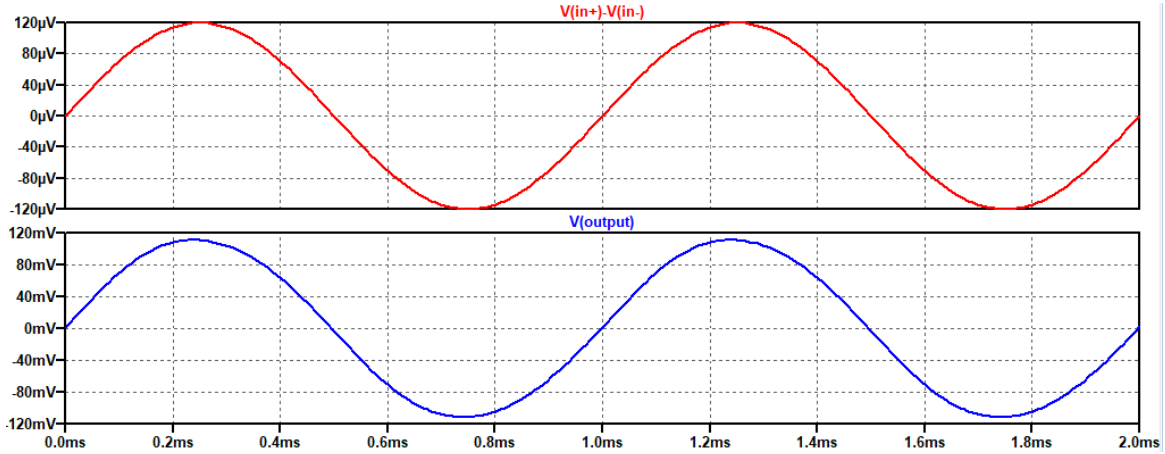

Figure 27. *The input (upper) and output (lower) waveforms with 240 µV p-p differential input at 1 kHz frequency.*

The maximum input range is in here considered as the level when the third harmonic frequency reaches 2 % of the signal magnitude in the output which occurs at 120 µV peak-to-peak (p-p) differential voltage amplitude (Figure 26). It provides output of 338 mV p-p, seen in Figure 27.

3.3 Amplification and Bandwidth

The amplification or voltage gain was also simulated as the AC response. The analysis does not consider limitations of the circuit, but it expresses the theoretical amplitude of the AC signal at chosen point calculated via a linearization of the circuit at given DC bias point.

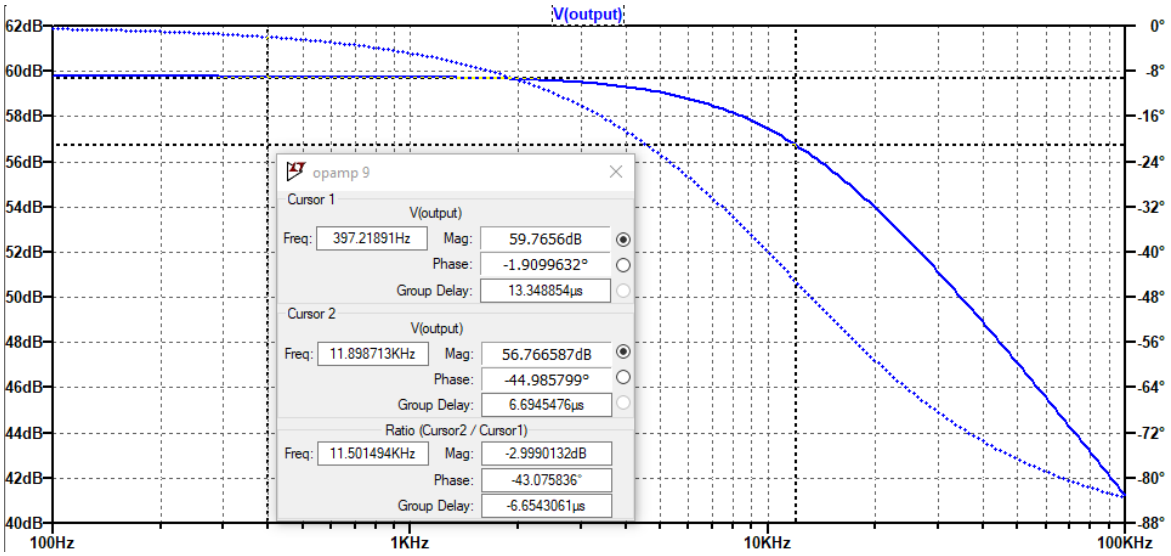

Figure 28. *The Bode plot of the output with cursors for exact values. AC gain is 59.77 dB and corner frequency 11.9 kHz.*

The bandwidth of 11.9 kHz is measured as the frequency range before the point where amplification reaches 3 dB below the middleband value (Figure 28).

3.4 I/O Impedances

Input or output impedance can be analyzed as the impedance a signal source perceives looking into the circuit. It was measured as the ratio of test source's nominal voltage and conducted current.

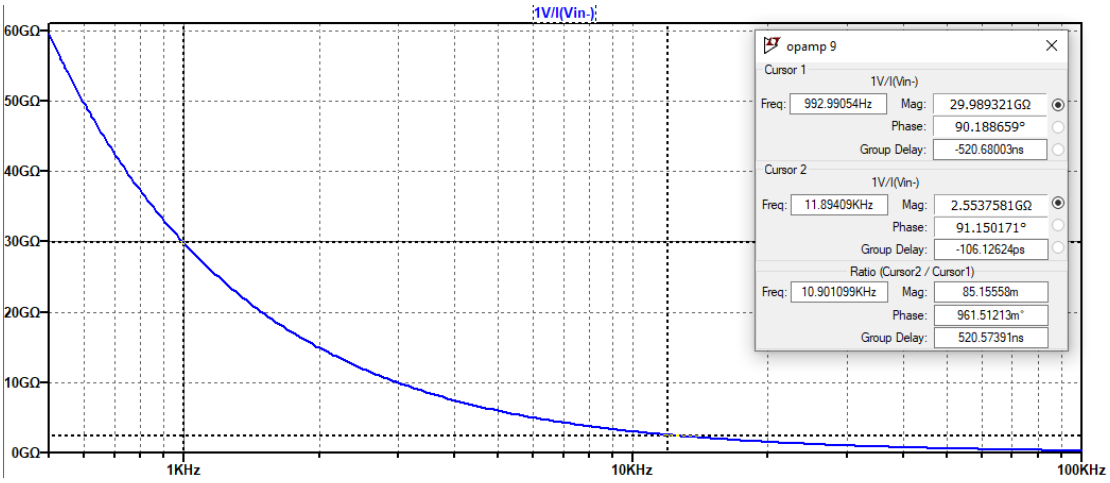

Figure 29. *The input impedance is 29.99 GΩ at 1kHz and 2.55 GΩ at 11.9 kHz.*

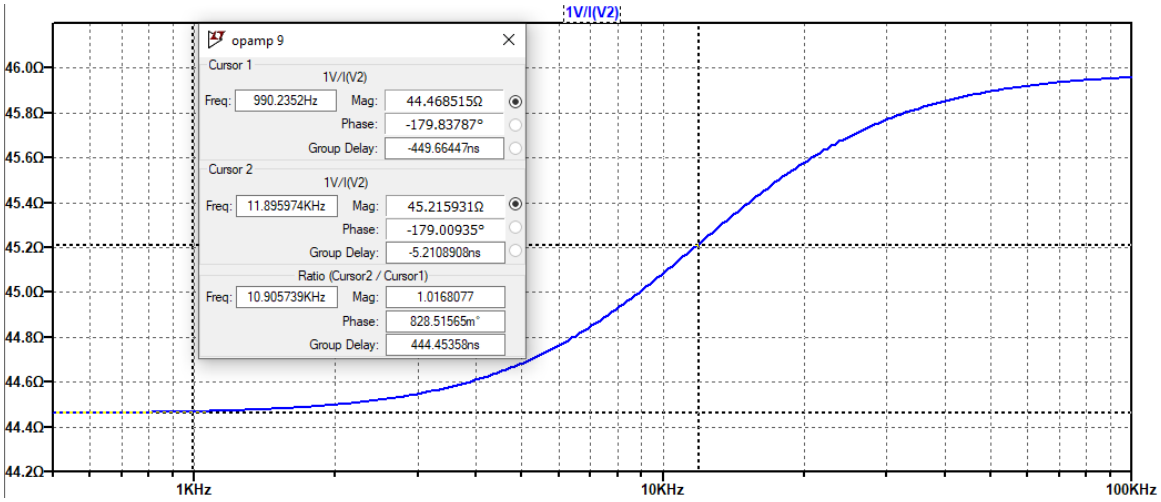

Figure 30. *The output impedance at 1kHz is 44.5 Ω and at 11.9 kHz 45 Ω.*

Figure 29 shows the input impedance of 2.55—29.99 GΩ and Figure 30 the output impedance of 44.5—45 Ω, both measured at 1kHz for lower middleband value and on the upper corner frequency 11.9 kHz.

3.5 Test circuits

The datasheet of the LM358 suggests several circuits for typical applications, two of which were used for testing the design. A non-inverting DC gain circuit (Figure 31) and

a square wave oscillator circuit (Figure 33) were constructed in the LTspice to test whether the design will work in simple real-use circuit.

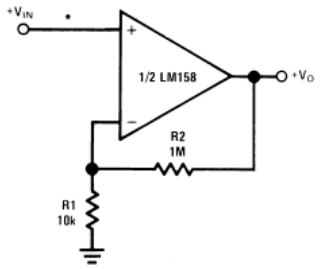

Figure 31. *A non-Inverting DC Gain circuit presented in LM358 datasheet [11, p. 14].*

The circuit should give a steady gain formulated as $Av = (R1 + R2) / R1$ [11, p. 14].

The circuit works with tested resistor values providing gain of 2 and 10 times with corresponding resistor values (Figure 32). The circuit is presented in appendix B.

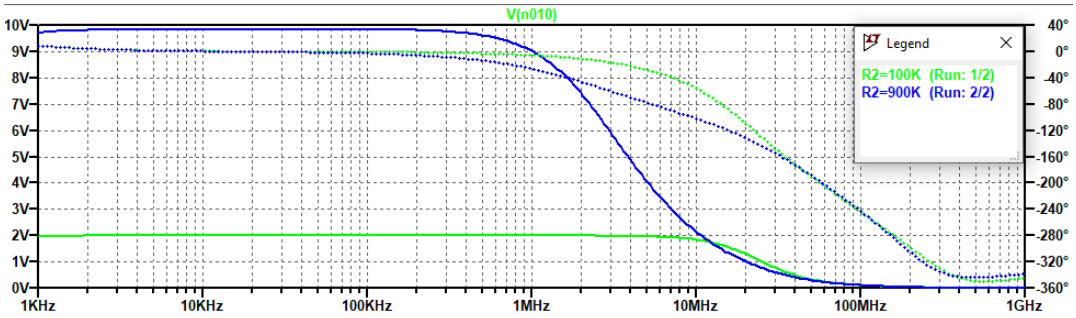

Figure 32. *Non-inverting DC gain circuit's amplification configured for gains of 2 and 10 shows respective successful amplifications.*

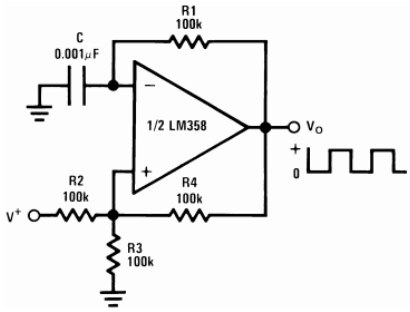

Figure 33. *A square wave oscillator circuit presented in LM358 datasheet [11, p. 17].*

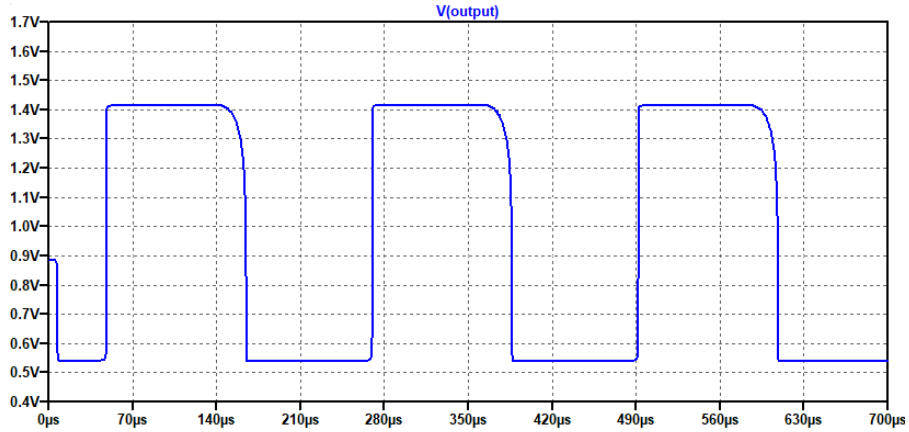

Figure 34. *Default external component values provide oscillation at 4.4 kHz frequency.*

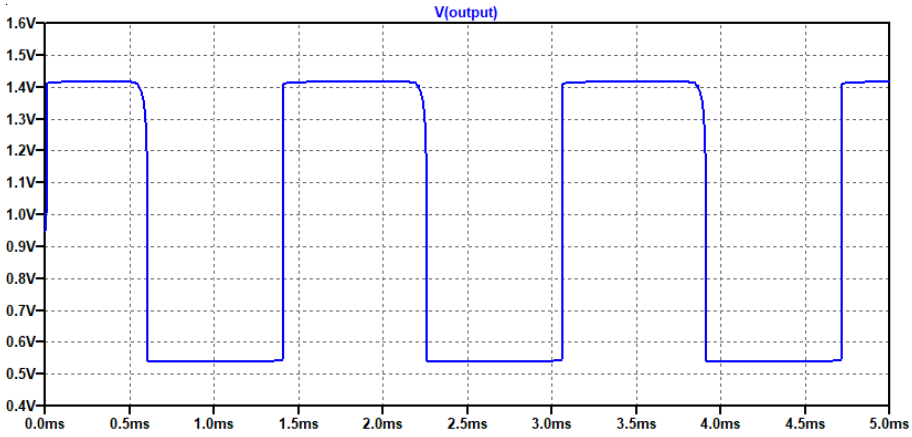

Figure 35. *Changing C1 to 10 nF and V2 to 1.85 V changed the frequency to 600 Hz.*

In the oscillator build the points of interest are the oscillation frequencies controllability by the choice of external component values, which succeeded (Figure 34 & Figure 35). The circuit is presented in appendix C.

4. CONCLUSIONS

The designed amplifier turned out decent, fulfilling all primary targets of functioning in test circuits and driving 100 Ω load resistance. Maximum of 500 µA total current consumption was exceeded due to output stage design choice.

The output stage's assumed push-pull operation is current-wise a bad compromise. Both transistors are conducting and operation resembles a PMOS loaded NMOS SF stage instead of actual push-pull where each transistor conducts only for respective polarity of signal. The output impedance to be able to support 100 Ω load was maybe too small to be effectively implemented for class A or AB output. 2.2 V supply voltage was also maybe too ambitious because it restricted voltage headrooms and thus design choices.

The amplifier fits into some basic specifications of op-amps introduced in [4, p. 12] by landing the DC voltage gain in between 40—120 dB and ideal infinite common-mode rejection ratio (CMRR) but fails at offset voltage specification of less than 5 mV. The ready design was superficially tested to perform with zero input offset but the performance was degraded. With minor changes in component bias points it would probably work with no major differences in performance because the bottleneck of the design lies in output stage. Noise and slew rate were not tested.

Comparing the performance to the original LM358 would not be of much worth because the real datasheets use tested values of manufactured components so their designs have taken into account process variations meaning different mismatch percentages within components. For example CMRR with perfectly balanced differential stage is not meaningful with a simulation program without the knowledge of difference magnitudes manifesting while manufacturing; the CMRR would be ideal and thus infinite. This is also a shortcoming in the op-amp designed in this work since the mismatching effects are not considered in the process.

As the amplifier is a result of iterative design, it is not very optimized at this point. It could be made better in the same method by changing each component's values to further examine the range of options. The tuning could be done to increase any single area of performance, often by harming some other.

For future research, the ready design could be tested with some more advanced SPICE and other transistor model of same or smaller technology node.

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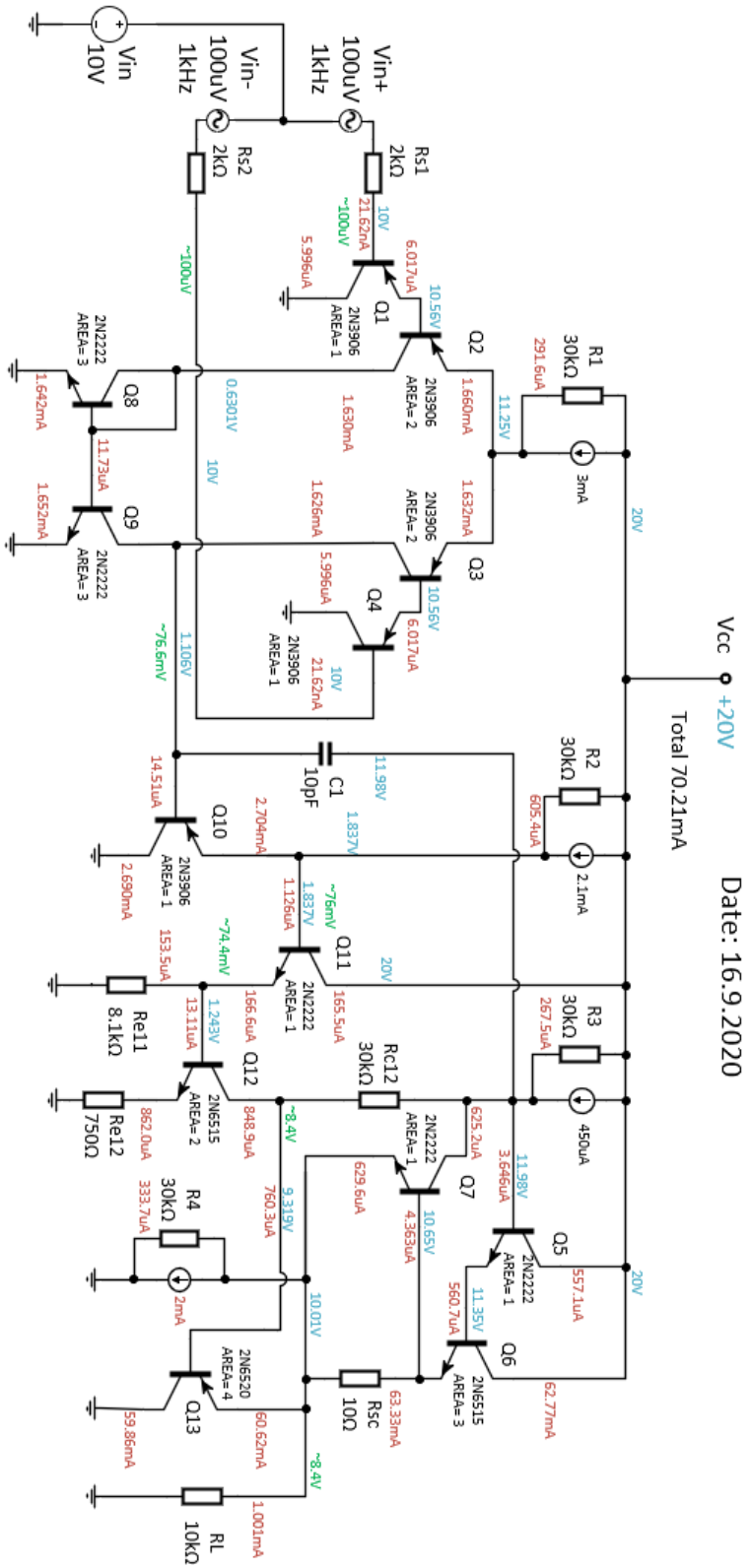
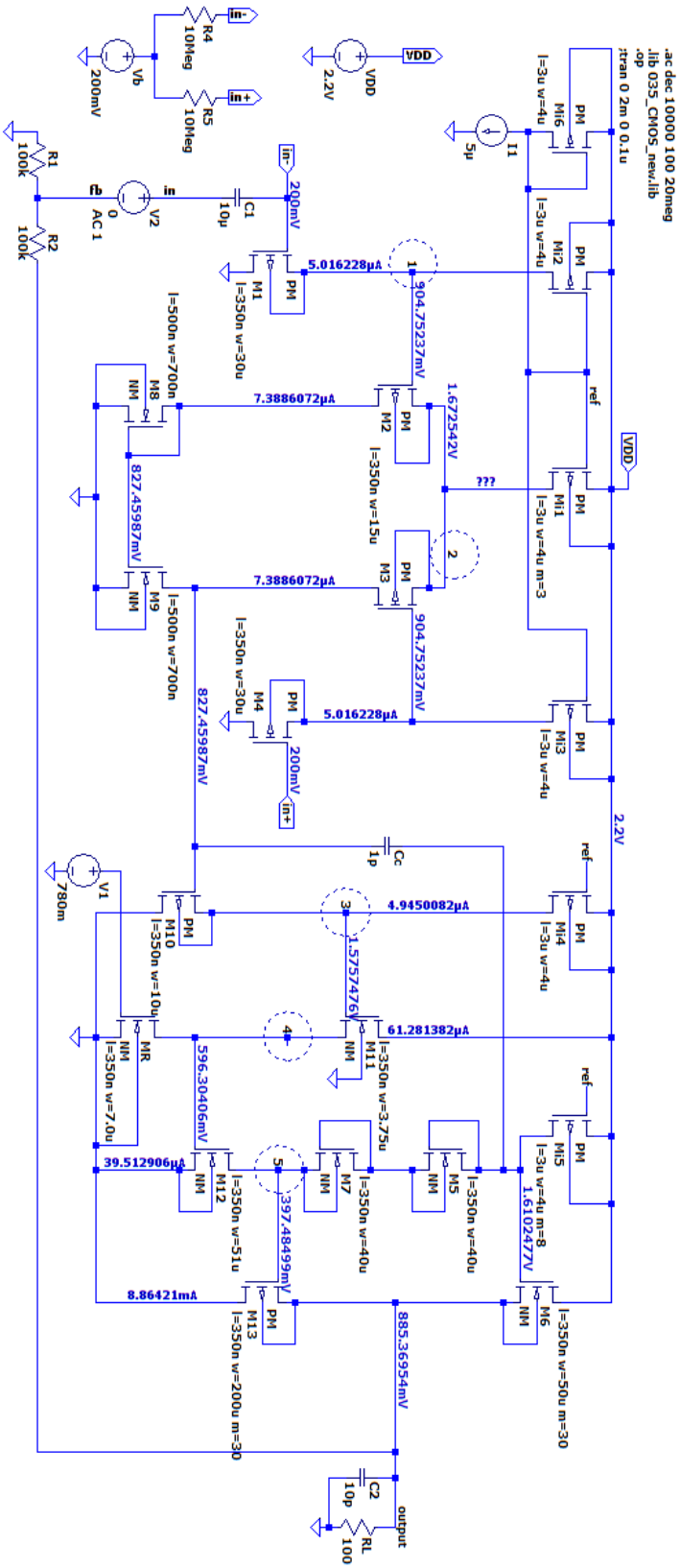
APPENDIX A The BJT version of Texas Instuments LM358 designed with PSpice



APPENDIX B The noninverting DC gain circuit



APPENDIX C The oscillator circuit