

# A Delay-Based LO Phase-Shifting Generator for a 2-5GHz Beamsteering Receiver in 28nm CMOS

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**Abstract**—This paper proposes a wideband 2-5GHz LO phase-shifting generator based on two digitally controlled delay lines. The concept is verified on a two-channel beamsteering direct-conversion receiver prototype implemented in 28nm CMOS. The novel generator provides both tunable phase-shifting and generation of I/Q components, achieving picosecond time resolution. The generator consumes 4.5-11.2mW and occupies 0.021mm<sup>2</sup>.

**Index Terms**—CMOS, LO phase-shifting, wideband, beamsteering receiver, delay line, quadrature generation, RF front-end

## I. INTRODUCTION

Both sub-6GHz and mm-wave 5G systems [1] embed significant number of transceivers in arrays (TX BS) to steer directivity (beamsteering) towards concurrent users and to parallelize data streams for traffic growth. The sub-6GHz bands guarantee backwards compatibility with existing communication systems and provide new services with beamsteering, e.g. anti-collision radars or vehicle-to-vehicle communications [2].

In the array transceivers signal composition can be implemented in different stages. Existing architectures bring signal to the baseband summation after applying analog phase shifts at either RF [3], [4] or LO [5], [6] blocks of the receiver, or operate directly at the baseband [7], [8]. Currently, the typical approach is to use passive phase shifters at the mm-wave region while the sub-6GHz designs are shifting towards digitally friendly solutions, leveraging downscaling trend, highest integration level and lowest cost offered by CMOS technology. In addition of fully digital transceiver arrays, the digital LO phase-shifting techniques are gaining interest since digital LO phase-shifter is decoupled from the RF signal path, thus not affecting its frequency and dynamic ranges. In all traditional analog phase-shifting mechanisms the beamsteering is based on the adjustment of the phase between received waveforms relative to each other. This leads to narrowband operation frequencies. In 5G systems, where the operation bands can span several GHz, the preferred method for phase-shift should be based on controllable delays.

In this paper we propose a wideband LO phase-shifting generator, outlined in Fig. 1. Proposed arrangement has the following advantages: a) small die area, owing to no bulky arrays of passive components, b) prospective digital-flow compatibility, c) wide frequency band and wide delay range

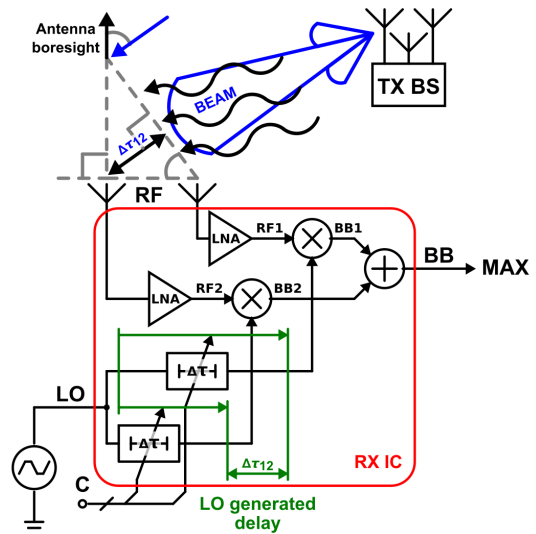


Fig. 1: Delay-based LO phase-shifting verified in the paper.

programmability realized by delay line, d) 2×4-phase I/Q generation from a single LO input, e) I/Q pulse position tuning for optimum conversion gain, f) re-use of the same delay cell for paths calibration, pulse generation and beamsteering functions, thanks to the cell encompassing both coarse and fine latencies and g) upscaling for more RX channels by adding more phase-shifting stages to an existing LO input. Integrated in the prototype receiver (RX IC), proposed phase-shifting generator drives 2×4 passive mixers for the two quadrature channels, operates in the 2-5GHz range, consumes 4.5-11.2mW, and achieves picosecond time resolution.

Section II of the paper discusses target application for the implemented LO phase-shifting generator. Section III describes circuit details of the full LO chain, with subsections detailing generator building blocks. Measurement results are discussed in Section IV and section V concludes the paper.

## II. IMPLEMENTED ANTENNA ARRAY RECEIVER

Fig. 1 outlines an implemented two channel receiver front-end. It encompasses two RF paths, with LNA and quadrature mixers in each path, baseband summation node (BB) and a delay-based phase-shifting generator (LO) to prototype beam-

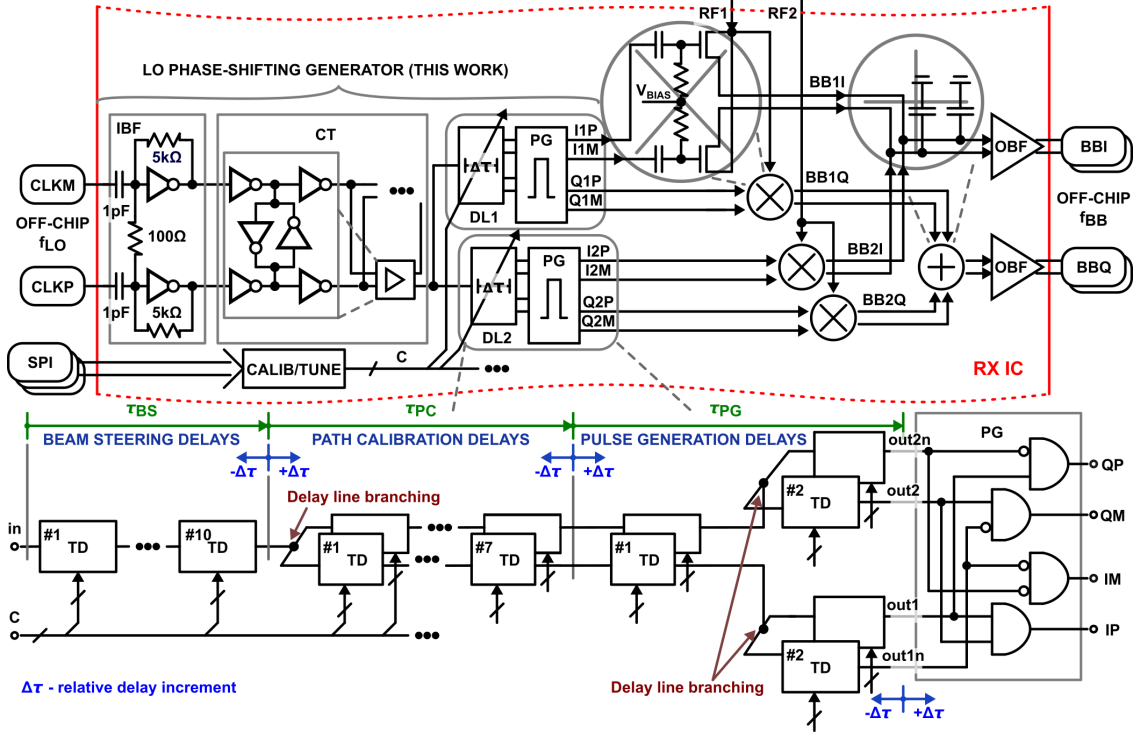


Fig. 2: Delay-based multi-phase LO chain for the quadrature passive mixers in the implemented beamsteering receiver.

steering functionality on two-antenna array receiver. Our paper focuses on LO phase-shifting generator, shown in Fig. 2.

Unlike dividers with phase selectors (DIV+PSELs) or polyphase filters with weighting amplifiers (PPF+VGAs), this design provides *both* tunable phase-shifting *and* generation of in-phase/quadrature LO components. Achieved via passives-less branched delay lines and combinational logic *with no dividers*, proposed design simplifies the integration of large number of channels with a single LO input and enables future implementations solely with digital place and route tools.

Key idea of the proposed LO phase-shifting mechanism is built upon digitally controlled delay lines, where desired beamsteering delay is produced as difference ( $\Delta\tau_{12}$  in Fig. 1) between latencies enabled on individual lines. Individual line latency is constructed with  $\Delta\tau$  increments, available from chained delay cells (TD), and demonstrates tunability sufficient for practical low-GHz beamsteering applications.

### III. IMPLEMENTED LO PHASE-SHIFTING GENERATOR

The LO phase-shifting generator comprises input buffer, clock tree and functional delays arranged as in Fig. 2. The differential off-chip LO is first buffered via simple inverting amplifier with on-chip 100 Ohm input termination (IBF). Signals from this input interface are then brought to individual delay lines by the clock tree (CT) buffers featuring positive feedbacks for faster settling to static levels. Current design supports up to eight RX channels thanks to two-level differential clock tree.

#### A. Branched delay line

In order to drive quadrature passive mixers, individual delay line needs to generate eight output phases with  $45^\circ$  mutual shifts. In the proposed design, this was accomplished with delay line branching as indicated with arrows in Fig. 2. By applying branching we also reduce power consumption by sharing common parts, compared to  $2 \times 4$  otherwise needed independent full delay lines.

Branch points break the line into several sections, the functional purpose of which is explained in the following paragraphs. Realized delay values can be viewed as absolute or relative, the latter being referenced from the smallest absolute value produced by the tunable delay cell. Proposed operation is built upon incrementing *relative delays* along the line and constructing the needed phase shifts.  $\pm\Delta\tau$  in Fig. 2 indicate positive and negative directions for relative delay increments.

1) *Beam steering*,  $\tau_{BS}$ : The main purpose of beam steering section of the delay line is to compensate for delays  $\Delta\tau$  in arrival to the antennas, which is meant to provide spatial filtering of interferers and to increase SNR of the receiver. There are 10 tunable delays in the section, giving 0-150ps  $\Delta\tau$  range.

2) *Path calibration*,  $\tau_{PC}$ : Path calibration section of the delay line cancels delay differences between RX channels due to PVT variations and on-chip proximity of multichannel arrangements. There are 7 tunable delays per each branch in the section, providing 0-100ps  $\Delta\tau$  range.

3) *Pulse generation*,  $\tau_{PG}$ : To generate quadrature signals for the mixers, pulse position needs to be adjusted with

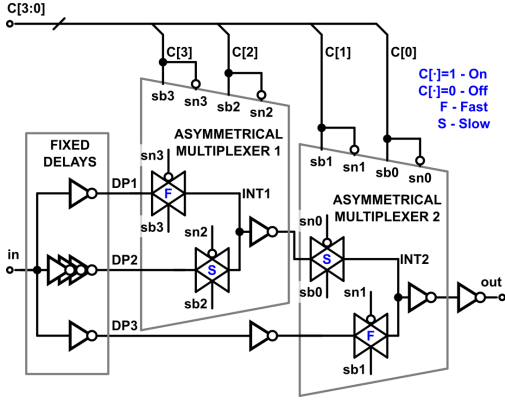


Fig. 3: Tunable delay schematic.

TABLE I: RC-extracted simulation summary of the tunable delay modes

TD mode	Control word code book	Delay (ps) @1V@3.5GHz	
		Abs., $\tau$	Rel., $\Delta\tau$
Fine	1011	83.75	0
	1010	84.53	0.77
	1110	84.62	0.86
	0110	86.51	2.76
	1111	86.73	2.98
	0010	87.23	3.47
Coarse	0111	98.81	15.06
	1001	101.82	18.07
	1101	107.68	23.93
	0101	129.18	45.43
No passage	0000	$\infty$	$\infty$

pulse generation delays. In addition, these delays provide non-overlapping quadrature signals to improve downconversion mixer gain. There are 2 tunable delays per section path.

To simplify design and improve matching all tunable delay cells use identical structure.

### B. Tunable delay cell

Designed delay cell (Fig. 3) includes fixed inverter-based delays and 3-to-1 multiplexing, providing *independently* controlled delay paths DP1-DP3. The inverters replicate incoming pulse to create multiple copies that will be subject to multiplexing and delaying through fast and slow transmission gates. Developed approach encompasses both coarse and fine latencies within a single cell, yielding altogether 10 distinct latencies summarized in Table I. All-zeros code impedes the through-passage when delay line is deactivated.

### C. Pulse generator

To achieve 25% duty-cycle quadrature waveforms for the 4-phase passive mixers in direct-conversion receiver, four streams obtained from the branches of delay line are combined via AND gates in the pulse generator (PG in Fig. 2). Duty-cycle is modified at the end of the delay line, since 25% duty-cycle waveform, having 50ps pulse width at 5GHz, can not reliably propagate through the entire line.

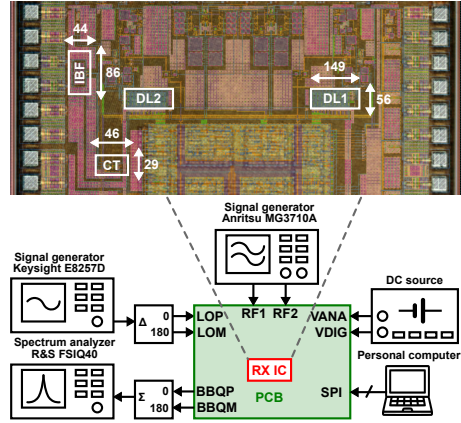


Fig. 4: Verification setup and annotated chip micrograph.

## IV. MEASUREMENT RESULTS

The chip in Fig. 4 was processed with 28nm CMOS technology. Total LO phase-shifter area (DL1, DL2, IBF and CT blocks) equals 0.021mm<sup>2</sup>.

To measure beam patterns, two 2-5GHz range RF signals with a variable well-controlled phase difference are applied as in Fig. 4 from signal generator to emulate the incident signals impinging the receiver antennas from different spatial directions. The differential baseband outputs of quadrature component are connected to the spectrum analyzer through off-chip combiner and the full chip hardware is externally controlled by an SPI.

In order to calibrate the tunable delays, we use CALIB block in Fig. 2 as calibration interface for the LO phase-shifting mechanism. Automated calibration of delays proceeds as follows. First, RC-extracted layout simulations [12] provide initial code-delay library. This library is then supplied to control program as initial data vector for loading into CALIB block. Second, control program performs guided search of delay codes in the vicinity of the initial data, attempting to maximize channel gain. Finally, settings that yielded maximum channel gain for particular RF frequency and RF phase-shift are stored as corrected vector in the block.

Fig. 5 shows two RX channels maximum gains as a function of incident RF signals mutual phase shift. Figs. 6 and 7 show the measured beam patterns when the beam direction is set to -45° and 45°, respectively. As can be observed the proposed delay line can provide wideband 2-5GHz tuning with 1° phase resolution. Performance summary and comparison with other works in low-GHz range are given in Table II. As it can be seen we are able to provide wideband tuning range with compact chip area.

## V. CONCLUSION

By implementing LO phase-shifting with passives-less branched delay lines presented in this paper, 2-channel receiver prototype demonstrates beamsteering in sub-6GHz range utilized by the 5G system. The LO phasing supports 2-5GHz frequency range, with 4.5-11.2mW power consumption and

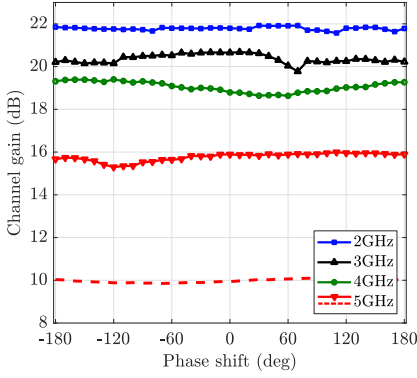


Fig. 5: Measured 2 beams channel gain for 2, 3, 4 and 5GHz RF signals. Dashed line shows single channel at 5GHz.

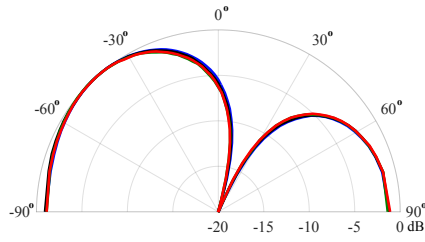


Fig. 6: Measured 2 beams pattern at  $-45^\circ$  for 2, 3, 4 and 5GHz RF signals, assuming antenna spacing of  $\lambda/2$  for all frequencies.

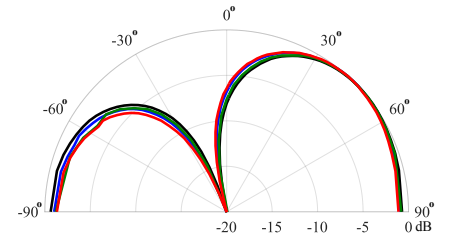


Fig. 7: Measured 2 beams pattern at  $45^\circ$  for 2, 3, 4 and 5GHz RF signals, assuming antenna spacing of  $\lambda/2$  for all frequencies.

TABLE II: Performance summary and comparison of low-GHz implementations

	This work	ESSCIRC'18 [9]	JSSC'14 [10]	ISSCC'12 [11]	ISSCC'11 [7]
CMOS process (nm)	<b>28</b>	65	28	140	65
Phase-shifter area (mm <sup>2</sup> )	<b>0.008 (one DL) 0.005 (shared IBF+CT)</b>	0.16 <sup>(1)</sup>	0.03 <sup>(1)</sup>	0.068 <sup>(1)</sup>	0.047 <sup>(1)</sup>
Nominal supply (V)	<b>1.0</b>	1.5	1.0	1.8	1.2
Power consumption (mW)	<b>2.23 (2GHz, one DL) 5.6 (5GHz, one DL)</b>	31.75 (9GHz, one RX)	34 (0.6GHz, four RX) 119 (4.5GHz, four RX)	90	77 (2.5GHz, four RX)
Channel gain (dB)	<b>22 (2GHz) 20.5 (3GHz) 18.5 (4GHz) 15 (5GHz)</b>	N/A <sup>(2)</sup>	N/A <sup>(2)</sup>	15	16 (2.5GHz)
Frequency range (GHz)	<b>2.0 - 5.0</b>	7.0 - 11.0	0.6 - 4.5	1.0 - 2.5	1.0 - 4.0
Phase / Delay measured resolution ( $^\circ$ / ps)	<b>1<math>^\circ</math> (2GHz) 2.4<math>^\circ</math> (5GHz)</b>	Not reported	14.5 $^\circ$	14ps	11.25 $^\circ$
Implementation type / Topology used	<b>Passives-less DLs LO phase-shifting</b>	PPF+VGAs LO phase-shifting	DIV+PSELS LO phase-shifting	Tapped gm-C DLs RF phase-shifting	Switched-cap modulator BB phase-shifting

<sup>(1)</sup> Estimated from annotated chip micrograph.

<sup>(2)</sup> Normalized gains/array patterns were only reported.

picosecond resolution. Generator was processed with 28nm CMOS and occupies only 0.021mm<sup>2</sup>. Proposed digitization-ready arrangement drives 8-phases quadrature downconversion LO chain and can be easily upscaled for more RX channels.

#### ACKNOWLEDGMENT

This work has been supported by Academy of Finland, Business Finland and European Union's Horizon 2020 Research and Innovation Programme under the Marie Skłodowska-Curie Grant 704947. The authors are grateful to I. Smirnov for his cooperation and tenacity in completing the project.

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