Live Demonstration: 4K100p HEVC Intra Encoder

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***Abstract*— This paper describes a demonstration setup for real-time 4K HEVC intra coding. The system is built on Kvazaar open-source HEVC encoder partitioned between 22-core Xeon processor and two Arria 10 FPGAs. The demonstrator supports 1) live streaming of up to three 4K30p videos; or 2) offline video streaming up to 4K100p format. Live feeds are shot by three cameras whereas offline video is accessed from a local hard drive. In both cases, encoded bit stream is sent over a wired connection and played back by laptop(s). The demonstrated HEVC coding speed is over three times as fast as that of a pure software solution.**

Keywords*— *High Efficiency Video Coding (HEVC); real-time intra coding; 4K; Kvazaar; field-programmable gate array (FPGA)

I. Introduction

The explosive growth of live Internet video arouses a need for efficient real-time video compression. The latest video coding standard, *High Efficiency Video Coding* (*HEVC/H.265*) [1], brings about significantly higher coding efficiency but at the cost of substantially increased coding complexity over that of earlier standards. Therefore, implementing a real-time HEVC encoder with a reasonable coding efficiency requires efficient encoder optimizations and powerful computing platforms.

This work focuses on the *all-intra* (*AI*) coding configuration of HEVC Main Profile. The setup is built on Kvazaar HEVC encoder [2] that is shown to be the fastest fully-fledged open-source implementation for AI coding [3]. Our recent work [4] shows that a pure software implementation of Kvazaar is able to attain 4K30p coding speed on a 22-core 2.2 GHz Intel Xeon E5-2699 v4 processor. This demonstrator setup more than triples the coding speed attained in [4] by accelerating the same processor with two Altera Arria 10 FPGA cards connected via PCIe buses.

II. Setup for Kvazaar 4K100p HEVC Encoding

Fig. 1 depicts the demonstrator equipment showcased to the visitors. The implementation details of Kvazaar encoder are given in [5] on Nokia AirFrame Cloud Server which is, however, replaced by a more compact workstation in this demonstrator setup.

In the case of live streaming, three Sony FDR X1000V 4K action cameras are used to shoot three 4K (3840×2160) streams at 30 *frames per second* (*fps*). These raw feeds are captured by Epiphan AV.io HDMI capture cards and converted by three FFmpeg instances from RGB to YUV 4:2:0 format. Three Kvazaar instances encode the converted YUV streams in real-time on a FPGA-accelerated Xeon E5-2699 v4 processor. The encoded HEVC bit streams are then encapsulated by three FFmpeg instances to MPEG-2 TS format and sent over the Ethernet cables to three Asus VivoBook Pro 15 laptops for 4K playback. The average bit rate is ca. 21 Mb/s per stream.

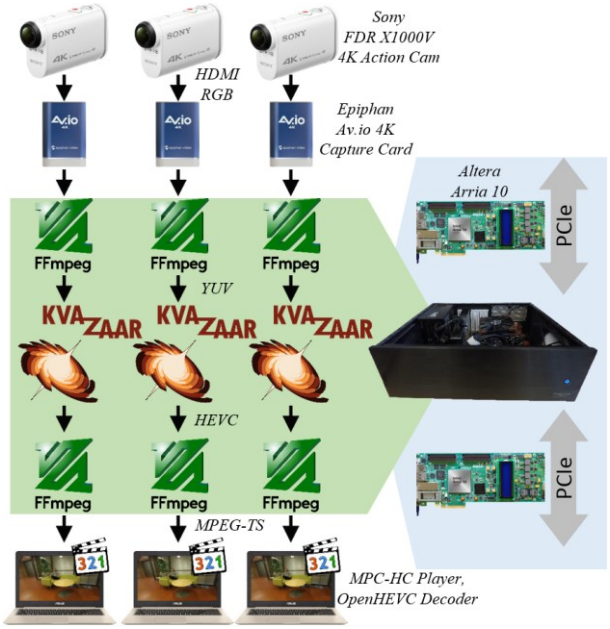

Fig. 1. Demonstration setup for Kvazaar live 3×4K30p HEVC intra coding.

In the offline case, a single YUV 4K100p video is read from a local hard drive, encoded by a single Kvazaar instance at 100 fps, converted to TS, and sent to Asus laptop for playback (with the frame rate limited to 60 fps).

The demonstrator seeks to make the visitors understand the stringent requirements of live 4K HEVC encoding. The visitors can monitor Xeon CPU usage and Kvazaar coding statistics in real time. They can also move cameras to see how the texture of the video affects the bit rate and CPU load.

References

[1] *High Efficiency Video Coding*, document ITU-T Rec. H.265 and ISO/IEC 23008-2 (HEVC), ITU-T and ISO/IEC, Apr. 2013.

[2] *Kvazaar HEVC encoder* [Online]. Available: https://github.com/ultravideo/kvazaar

[3] A. Lemmetti, A. Koivula, M. Viitanen, J. Vanne, and T. D. Hämäläinen, "AVX2–optimized Kvazaar HEVC intra encoder," *in Proc. IEEE Int. Conf. Image Processing,* Phoenix, Arizona, USA, Sep. 2016.

[4] A. Ylä-Outinen, A. Lemmetti, M. Viitanen, J. Vanne, and T. D. Hämäläinen, "Kvazaar: HEVC/H.265 4K30p intra encoder," *in Proc. IEEE Int. Symp. Multimedia*, Taichung, Taiwan, Dec. 2017.

[5] P. Sjövall, V. Viitamäki, J. Vanne, T. D. Hämäläinen, and Ari Kulmala, "FPGA-powered 4K120p HEVC intra encoder," *in Proc. IEEE Int. Symp. Circuits Syst*., Florence, Italy, May 2018.