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LOW VOLTAGE METAL OXIDE TRAN- SISTORS

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ABSTRACT

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In this thesis the objective is to determine if a functional thin film transistor (TFT) with a bottom gate – top contact structure is possible to make with Evonik's commercial semiconductor. Ixsenic is a solution processable indium oxide -based metal oxide semiconductor. Another goal is to determine how storing the transistor in different gases affects its performance and how the density of interface states is changed during the storing.

The transistors were optimized by changing the processing parameters concerning the semiconductor layer formation. The gate dielectric was deposited by anodization of Al and the semiconductor was deposited by spin-coating and annealed with ultraviolet (UV) light and hotplate. The optimized transistors have a mobility of 1-3 cm²/Vs, on-off ratio of 10⁴, subthreshold swing of 0,2-0,3 V/dec, threshold voltage of 0,9-1,4 V and gate leakage current of 0,7-3 μA. This compares favorably with Evonik's reported mobility, up to 10 cm²/V·s, using Evonik's spin-on dielectric.

Samples were stored either in nitrogen, or air, for two weeks to see the difference the gas has in the changes happening within the transistor. The on current of the transistor stored in air was an order of magnitude lower after storing and the off-current of the transistors stored in nitrogen rose considerably. A Matlab-code was developed to characterize changes in the density of interface states at the anodized Al and Ixsenic interface, but the work was not finished in this thesis.

The transistors made in this thesis have a high enough on-off ratio to be used in circuits. The mobility value is corrected with reliability calculations, which gives it more credibility. The work on the density of interface states should be continued to determine the changes happening in the interface while storing the transistors.

TIIVISTELMÄ

ANNA-SOFIA AIRIO: Matalajännitteiset metallioksidi transistorit

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Tämän diplomityön tavoitteena on selvittää, onko mahdollista valmistaa ohutkalvotransistori indiumoksidiin pohjautuvasta liuosprosessoitavasta Ixsenic puolijohdemateriaalista. Transistorit tehdään rakenteella, jossa hila on pohjalla ja lähde ja nielu rakenteen päällä. Toinen tavoite on selvittää, miten transistorin säilyttäminen eri kaasuissa vaikuttaa sen toimintaan ja miten rajapinnan energiatilojen tiheys muuttuu säilytyksen aikana.

Transistorien toiminta optimoitiin muuttamalla puolijohdekerroksen valmistamiseen liittyviä prosessiparametrejä. Kannan eriste tehtiin anodisoinnin avulla, ja puolijohdemateriaali levitettiin spin-coaterin kanssa ja hehkutettiin UV-valolla ja kuumennuslevyn päällä. Optimoitujen transistorien varausten liikkuvuus oli 1-3 cm²/Vs, on-off virtojen ero oli 10⁴, kynnysjännitteen alainen virran kasvunopeus oli 0,2-0,3 V/dec, kynnysjännite oli 0,9-1,4 V ja kannan vuotovirta oli 0,7-3 μA. Tulos on hyvin vertailukelpoinen Evonikin ilmoittaman varausten liikkuvuuden, maksimissaan 10 cm²/V·s, kanssa.

Näytteitä varastoitiin työssä ja ilmassa kaksi viikkoa, jotta kaasujen aiheuttama ero saatiin selvitettyä. Ilmassa varastoitujen transistorien on-virta oli kertaluokkaa pienempi varastoinnin jälkeen ja työssä varastoitujen transistorien off-virta nousi huomattavasti. Rajapinnan energiatilojen tiheyden muutoksen selvittämiseksi tehtiin Matlab-koodi, mutta sen kehitystä ei saatu tämän työn aikana loppuun.

Tässä diplomityössä tehdyillä transistoreilla oli tarpeeksi suuri on-off virtojen ero niiden käyttämiseksi piireihin. Varausten liikkuvuuden arvo korjattiin luotettavuuskertoimella, mikä antaa sille arvolle enemmän uskottavuutta. Rajapinnan energiatilojen tiheyden selvittämistä pitäisi jatkaa, jotta säilytyksen aikana transistoreissa tapahtuneet muutokset saataisiin selville.

PREFACE

This master's thesis was done for the Tampere University Electronics department. It was done as part of the research in the transistor team in the Future electronics laboratory. The instructor was Professor Donald Lupo, who is also the examiner with Professor Paul Berger.

I would like to give my thanks to the whole Future electronics group. The help and advice from Professor Lupo and Professor Berger, as well as from Sagar Bhalerao were invaluable. Thanks to Prof. Dr. Ralf Anselmann and Evonik Resource Efficiency GmbH for providing the semiconductor material used in this thesis. I would also like to thank Doctor Jari Keskinen, Doctor Thomas Kraft and Miao Li for their help teaching the handling of equipment in the laboratory. Great thanks also to Rohan Paul Binoy at Ohio State University for writing the Matlab-code according to my instructions.

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LIST OF SYMBOLS AND ABBREVIATIONS

ALD	Atom layer deposition
a-Si	Amorphous silicon
CVD	Chemical vapor deposition
DI-water	Deionized water
DOD	Drop on demand
FET	Field effect transistor
IGZO	Indium-gallium-zinc-oxide
JFET	Junction field effect transistor
MESFET	Metal semiconductor field effect transistor
MISFET	Metal-insulator-semiconductor field effect transistor
MOSFET	Metal-oxide-semiconductor field effect transistor
MOS	Metal oxide semiconductor
PVD	Physical vapor deposition
TFT	Thin film transistor
C_{ox}	Oxide capacitance
E_c	Conduction band energy
E_f	Fermi level energy
E_v	Valence band energy
g_d	Conductance
g_m	Transconductance
L	Channel length
n	n-type charge carrier density
p	p-type charge carrier density
r	reliability factor
S	Subthreshold swing
V_T	Threshold voltage
W	Channel width
μ	Charge carrier mobility
μ_{EF}	Field effect mobility
μ_{eff}	Effective mobility
μ_{sat}	Saturation mobility
σ	Conductivity

1. INTRODUCTION

Electronic devices have long relied on transistors made of silicon. However, when new requirements have risen, such as transparency and flexibility of the materials, silicon is no longer a suitable material. To replace silicon, there are materials like solution processable metal oxide semiconductors and organic semiconductors.

Some promising results with solution processing have been achieved with both organic semiconductors, especially p-type, and metal oxide semiconductors, which can be used to make thin film transistors, especially n-type. Metal oxide semiconductors have charge carrier mobilities comparable to polycrystalline silicon [1-10] and organic semiconductors can be processed in low temperatures, which offers the possibility to use plastic [11-16] and paper [17-20] as flexible substrate materials. Another interesting prospect is the printability of metal oxide and organic semiconductors, which makes for low-cost large area high-throughput manufacturing possible.

However, the structure of a thin film transistor differs from a conventional field effect transistor, which limits the application of the physics of the conventional field effect transistor on thin film transistors. The thin film transistors are evaluated using parameters like mobility, threshold voltage and sub-threshold swing to assess their suitability to circuits and to compare different device structures and materials to each other [21].

One important aspect in making thin film transistors is the operating voltage of the device. The transistors should have a low operating voltage, especially for portable applications. High operating voltage would mean a high power consumption, which would limit the use of the transistors for example in portable medical wearables, for instance, with limited available power. Metal oxide semiconductors have been studied as a potential material for low voltage thin film transistors. [22-27]

In this thesis, the focus is on a metal oxide semiconductor material, Ixsenic from Evonik. Ixsenic is a solution processable indium oxide -based semiconductor material. The first objective was to see if Ixsenic was a suitable material for a thin film transistor structure used for indium oxide in the research group and to optimize the architecture and processes for the best performance. The second objective was to characterize the transistor more precisely to determine the density of interface states at the semiconductor channel interface with the gate dielectric. This is important, as this work extends Evonik's Ixsenic by replacing a SiO_x dielectric with alternatives. The Al_2O_3 used as dielectric in this work has a dielectric constant of 9,3 [25], whereas SiO_2 has lower dielectric constant of 3,9 [28].

First, the processing parameters for an optimal device are determined and then the stability of the transistors is studied further. The optimization is done by making transistors and changing processing parameters one by one and comparing the results. The transistors are also stored in different gases to see how the environment affects the operation of the devices. The analyzing of density of interface states is also begun to see how the density is changed during storing.

In the second chapter, the basic operation of a thin film transistor is explained and the effect of the high- κ gate insulator and semiconductor materials on the operation of the transistor is considered. In the third chapter, the most important characteristics for evaluating the operation of a thin film transistor are introduced. In the fourth chapter, the deposition methods for metal oxide semiconductor and gate insulator are discussed with special focus on the deposition methods used in this work. The process of inkjet printing is also explained briefly. In the fifth chapter, the structure of the samples and transistors made in this work is explained, the processing parameters to make them are discussed and the characterization of the transistor is explained. In the sixth chapter the results from the research are presented and discussed and in the seventh chapter conclusions from this work are drawn.

2. THIN FILM TRANSISTOR

The basic idea of a TFT is old. Already in 1930 J.E. Lilienfeld and O. Heil patented it. [29-32] Amorphous silicon (a-Si) based thin film transistors were commercialized in the 1970s. [33] However, because the materials used as metal oxide semiconductors were not well known and the techniques available to make TFTs were not well researched, the development of metal oxide TFTs has only resurfaced during the 90s and 00s. [34]

The development of TFTs has become topical because of new requirements the devices have for new display and Internet-of-Things (IoT) applications. The most plentiful transistors are made of silicon using a complementary metal-oxide-semiconductor (CMOS) configuration, as dense, low-power, and ultra-small, which is great for digital computer chips, but much less suitable for new flexible IoT applications. These applications can require, in addition to low voltages, properties like transparency and/or printable materials and flexibility. To achieve these properties, the processing temperatures often need to be lower, which is difficult to achieve in printed devices, due to high heat of formation of high- κ dielectrics. Low voltage operation is also necessary for the transistors to be used in IoT with limited portable power supplies. New materials are researched to meet all the necessary properties. Sometimes high dielectric permittivity is sacrificed to achieve low processing temperatures. Good examples of high dielectric constant gate dielectric (high- κ) materials, which enable lower voltages, with transparent metal oxide semiconductors, are in Sun *et al.*. [35]

Even though TFTs have new properties compared to conventional field effect transistors, they operate in a very similar way. The main difference in the structure is the absence of doped areas in the semiconductor. TFT has a film of undoped or doped semiconductor, but there are no separate areas with different doping within the film. However, a TFT behaves like a conventional MOSFET. [21]

2.1 Field effect transistor

A field effect transistor (FET) is a device, which modulates the current between the drain and source terminals with the influence of an electric field to a third terminal, the gate. Field effect transistors are usually made on a silicon wafer by doping and adding contacts. In an n-channel transistor the source and drain electrodes are on top of n-doped areas, which are separated by a lightly p-doped channel. On top of the channel is an insulator layer, commonly SiO_2 , or more recently HfO_x , which separates the gate electrode from the channel. The basic structure of an n-channel field effect transistor can be seen in Figure 1. [36, 37]

The structure described above is one of a metal-insulator-semiconductor FET's, or in short, MISFET. There are other structures, for example, a junction FET (JFET) and metal-semiconductor FET (MESFET), but the MOSFET is closest in structure and operation to the TFT, which is why the MOSFET is the focus of this chapter. The MISFET explained here is a metal-oxide-semiconductor FET, or MOSFET, which is a special case of MISFET just like the TFT.

In a MOSFET, the voltage applied to the gate electrode controls the channel. When the transistor is on, there is a thin layer in the semiconductor next to the insulator surface, which allows current to flow from drain to source. This layer is called the inversion channel. In depletion mode transistor the inversion channel is present when the gate voltage is at zero bias, and current can flow. An n-channel transistor requires a negative voltage to switch it off. In the other kind, enhancement mode transistor, the inversion channel must be created with a positive voltage on the gate. Hence, the transistor is off at zero bias voltage. Most MOSFETs are enhancement mode transistors and JFETs mostly operate in depletion mode. Most thin film transistors behave like enhancement mode devices in theory, although their working principle is different from the conventional MOSFET. [36, 37] For a p-channel transistor, the polarities of the voltage are changed for the same modes of operation. [37] The transistors in this thesis are made of a metal oxide semiconductor which behaves like an n-type semiconductor, making it more meaningful to explain the theory for an n-channel enhancement mode transistor. However, while it behaves like a doped semiconductor, a TFT is usually undoped, so that some of the underlying physical processes are different [21].

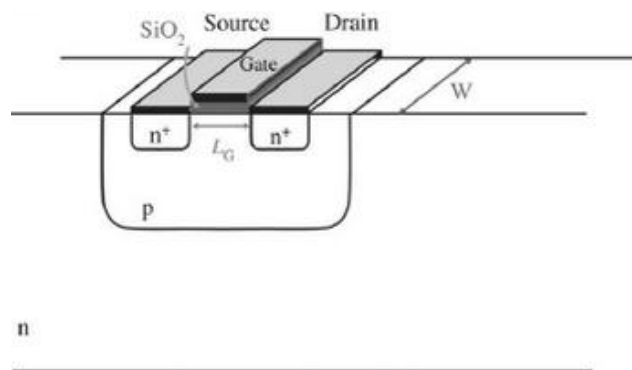


Figure 1. The basic structure of an n-channel field effect transistor on a silicon wafer. The W in the picture is the channel width and L_G the channel length. [36]

When a positive voltage is applied to the gate of an n-channel transistor, the gate metal becomes positively charged. A depletion layer is formed when the positive charge causes a negative charge in the semiconductor-insulator interface to deplete the holes in the p-type semiconductor. This is called the depletion region. Increasing the voltage in the depletion region increases the width of the depletion layer. When the positive voltage applied to the gate exceeds the value of threshold voltage, an inversion layer starts forming.

An inversion layer is formed by electrons near the semiconductor-insulator interface. The electron concentration is large enough for the material to conduct like an n-type semiconductor. This is the inversion region. When the inversion layer has enough electrons to make it as strong an n-type region as the substrate is p-type, it is called strong inversion. Strong inversion happens when the voltage is twice the threshold voltage. The third region of operation is accumulation, which happens when a negative voltage is applied on the gate. This causes an accumulation of holes in the semiconductor.

The flat band with no voltage applied to the gate can be seen from the band diagram of a MOSFET, Figure 2. However, normally the Fermi levels do not match, and a flat band voltage is required. In equilibrium, the Fermi level is flat and close to the conduction band of the n-type source and drain. However, in the p-type area between the source and drain the Fermi level is closer to the valence band. This means that there is a potential barrier preventing the electrons from flowing from drain to source. A positive voltage on the gate moves the position of the p-type area energy levels so that the valence band moves further away from the Fermi level. With high enough positive voltage, the current from drain to source can grow significant. [37]

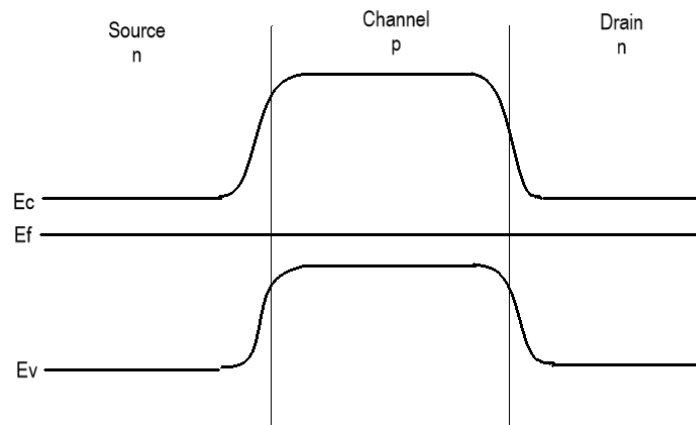


Figure 2. Band diagram of a MOSFET along the channel in equilibrium. E_c is the conduction band, E_f the Fermi level and E_v the valence band.

The minimum voltage required at the gate to induce a channel is called the threshold voltage, V_T . After this point, the current increases linearly when increasing the gate voltage, which is the linear region of the transistor. The current increases linearly until the voltage drop across the channel becomes more ohmic. The voltage difference between the gate and the drain becomes equal to the threshold voltage and after that point the channel is pinched off and the current increase is not significant. At the pinch off point the depletion regions of the transistor extend through the channel near the drain which causes the channel to be pinched off and the current does not increase from the saturation level it has achieved. The transistor is then in the saturation region. [37]

2.2 TFT structure and working principle

A TFT differs from a MOSFET structure in two principal ways. Firstly, the semiconductor layer is not divided into different areas by doping, but the whole layer is doped uniformly the same, or frequently is undoped. These layers do not have to be doped for the TFT to work and the n-type and p-type refer to the dominant mobility of the material rather than doping. However, doping can be used to change the properties of the semiconductor layer. Secondly, a thin film transistor is made of thin films of material, which is placed atop a myriad of rigid and flexible substrates, regardless of lattice constant, while MOSFETs are synthesized atop a silicon wafer, either leveraging the Si substrate itself to fashion the crystalline channel, or a channel is epitaxially grown atop the crystalline substrate to that the epitaxy is in registry with the Si substrate. [21]

TFTs have four different basic configurations they can be built in. They differ in the placement of the drain/source and gate terminals compared to the active layer. When the gate is under the active layer, the structure is called bottom-gate and when above, it is called top-gate. If the drain and source terminals are on the same side of the active layer as the gate, the structure is called coplanar and if they are on the other side, the structure is called staggered. The different structures can be seen in Figure 3.[21]

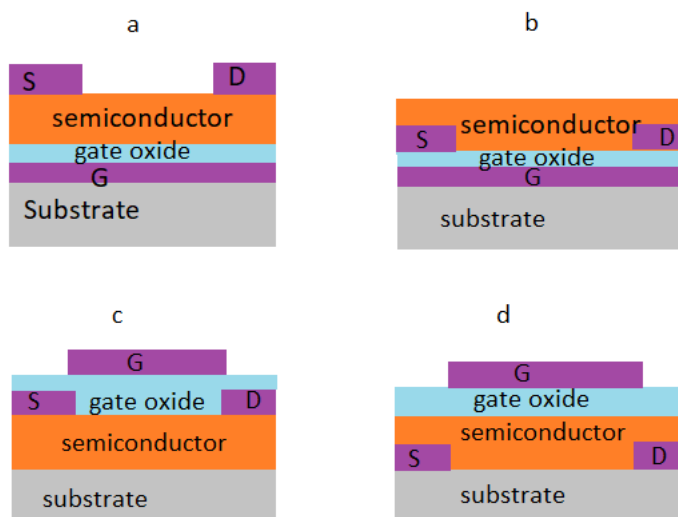


Figure 3. The TFT structures: a) bottom-gate staggered structure, b) bottom-gate coplanar structure, c) top-gate coplanar structure and d) top-gate staggered structure.

Since the doped areas are missing from the TFT structure, instead nominally undoped, the source and drain contacts are metal electrodes instead of the semiconductor source and drain in a conventional MOSFET. The current is controlled with the gate voltage, similarly to a MOSFET. The voltage at the gate, if positive, creates an accumulation of electrons in the case of a n-type semiconductor. A negative voltage at the gate would create a depletion layer if the semiconductor was doped, but in the case of thin film transistors, the semiconductor is usually intrinsic, and a depletion layer is not formed. When

a positive voltage is needed to create the accumulation, the TFT is said to operate in enhancement-mode, if it is a n-type semiconductor. A depletion-mode device already has accumulation at zero voltage, but a negative voltage turns off the transistor by depleting the accumulation. Just like with MOSFETs, in the case of p-type semiconductor, the polarities of the voltages just have to be reversed. [21]

In TFTs the imperfections of the materials can have significant effects on the operation of the transistor. [21] These effects are discussed more on the chapters concerning the TFT characteristics.

2.3 Gate insulator material

The gate insulator material has a critical role in the operation of the transistor. The gate insulator is an important part of the capacitor, which is used to control the current in the channel. The channel current is dependent on the capacitance according to the following equation [38]:

$$I_{D,sat} = \frac{W}{L} \mu C_{ox} \frac{(V_G - V_T)^2}{2}, \quad (1)$$

where W and L are the width and the length of the channel respectively, μ is semiconductor mobility, V_G is the voltage at the gate terminal and V_T is the threshold voltage. To achieve larger saturation currents with low voltages the dimensions of the transistor can be changed, the semiconductor material can be chosen with appropriate mobility, or the capacitance can be increased.

The capacitance is proportional to the dielectric constant of the gate insulator material and inversely proportional to the thickness of the gate insulator layer as can be seen from Equation 2. To achieve higher capacitance, the layer thickness can be reduced, or a high dielectric constant insulator material can be chosen. [39]

$$C = \frac{\kappa \epsilon_0 A}{t}, \quad (2)$$

where κ is the dielectric constant, ϵ_0 is the permittivity of free space, A is the dielectric layer area and t is the thickness of the dielectric layer.

The limitations of reducing the gate insulator layer thickness limit the use of conventional materials, such as silicon oxide. The leakage current increases when the layer is thin enough and quantum tunneling starts happening. To prevent this problem, high- κ dielectric material can be used, which allows the increase of the insulator layer thickness while maintaining the same capacitance of a thinner capacitor with low dielectric constant material. In other words, double the permittivity and double the insulator thickness results in the same capacitance per unit area. This prevents the leakage current from increasing by reducing the tunneling leakage pathway. [39]

When choosing a suitable material for the gate insulator, some aspects have to be considered. Firstly, the bandgap of the dielectric has to be large enough. The conduction band minimum of the dielectric material should be at least 1 eV higher than that of the n-type semiconductor to prevent gate leakage current by thermionic emission over the barrier. For a p-type semiconductor the valence band minimum of the dielectric should be at least 1 eV lower than that of the semiconductor. [39]

Secondly, the quality of the insulator film must be considered. The film should be preferably amorphous, because polycrystalline materials have grain boundaries, which can create paths for current and increase leakage. Although crystalline gate oxides can be quite advantageous too, but challenging to achieve. The film should also be as defect free as possible. This can be affected greatly by the chosen deposition method and possible annealing after the deposition. [39]

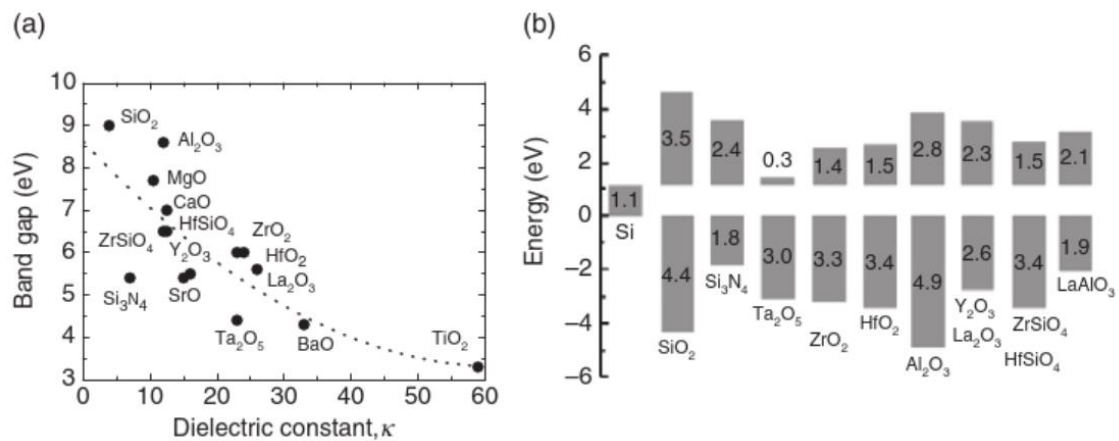


Figure 4. a) Bandgap of some gate oxide materials as a function of dielectric constant. b) The distance (eV) of the valence- and conduction-bands of some gate oxide materials to those of crystalline silicon (bandgap 1,1 eV). [39] modified from [40]

In Figure 4 are some representative gate oxide materials as a function of their dielectric constant and their bandgap compared to that of silicon. Silicon has a relatively small bandgap compared to oxide semiconductors, which makes finding a suitable gate dielectric material for an oxide semiconductor more difficult than for silicon. Some materials used are Al_2O_3 [41-45], and HfO_2 [22-24, 46, 47].

2.4 Amorphous metal oxide as semiconductor

Amorphous metal oxides have qualities making them possible candidates for semiconductor materials on thin film transistors. As per their name, they are amorphous, which means their large area properties are constant, making the device characteristics uniform. Amorphous materials also require lower processing temperatures, because crystallinity is not a goal. In fact, too high processing temperature can cause crystallization and create nonuniform structure. [48]

Amorphous metal oxide semiconductors have post-transition-metal cations, which make the conductivity of the materials higher. Instead of covalent bonding, the metal cations bond with oxygen. However, the conductivity is due to the s-orbitals of the metal cations. They are spherical and overlap with neighboring cations, creating high conductivity [48, 49], as shown in Figure 5.

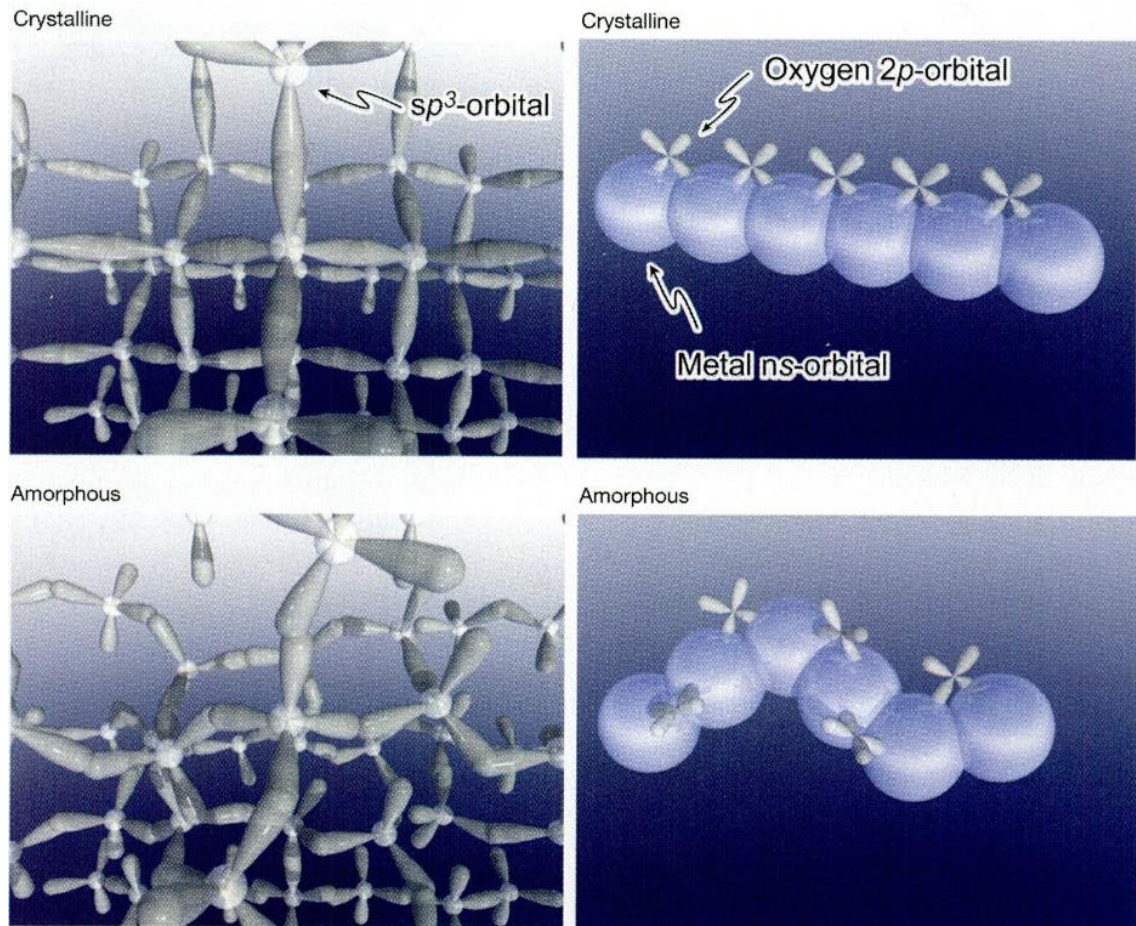


Figure 5. On the left, the crystalline structure of silicon and bottom left the amorphous silicon. On the right, the crystalline structure of a post-transition-metal oxide and bottom right it the amorphous structure. [48]

The conductivity of the amorphous metal oxide does not suffer greatly from the amorphous structure compared to the crystalline structure and makes the material an attractive alternative especially for applications requiring low temperature fabrication. The s-orbitals of the metal cations still have sufficient overlap even in amorphous structure, which allows the charge carriers to move freely in both crystalline and amorphous structures. [48] Amorphous metal oxides also have a relatively large bandgap, making the materials transparent, which could be advantageous for display applications. [49] Some amorphous metal oxide semiconductor materials are In_2O_3 [1-5] and indium gallium zinc oxide (IGZO) [7-10, 50].

While metal oxides have many good properties, there are also some drawbacks with amorphous metal oxides. The large bandgap makes the material transparent, but it also means the choosing of a dielectric is much more restricted, as explained in the previous section. Another minus are the imperfections in the material. There are defects in the semiconductor because of interstitial atoms and vacancies. Most influential are oxygen vacancies, which are empty places in the material structure, where oxygen atoms belong. They have shallow donor levels, less than 0,05eV, depending on the material, but they are responsible for the n-type behavior of the semiconductor [28]. On the other hand, by affecting the oxygen vacancy concentration, the carrier concentration of the material can be controlled. This can be done by controlling the oxygen vapor pressure during annealing. [49]

2.5 Metal oxide semiconductor compared to other semiconductor materials

The most common semiconductor material, silicon, has been studied and perfected for making high-speed and low voltage transistors. However, as the devices made of transistors have new requirements, even the most cutting-edge silicon transistor is not suitable. One example is flexible substrates. For the applications, where Si is no longer suitable, amorphous silicon has been researched. Amorphous silicon, a-Si, in thin film transistors has enabled the making of flat-panel displays, but it has some unfavorable properties, such as opacity. [35]

The mobility of a-Si as an n-doped material is three orders of magnitude lower than that of crystalline silicon. If the a-Si material is deposited on a flexible substrate, the mobility is even lower than that. The mobility is better when using a nano- or microcrystalline silicon or polycrystalline silicon, but it will not be as flexible device as a-Si can make. Although it is recognized that single crystalline silicon devices and circuits can be exfoliated from crystalline silicon substrates and affixed to flexible substrates, this is largely impractical for large volume production. So, a-Si would be the more suitable silicon choice here. But, the device lifetime of an a-Si transistors is also low, because the threshold voltage is not stable. [35] Another downside to a-Si is the low mobility when printing the material. [51]

Table 1. Comparison of TFT properties with different semiconductor material types. [28] collected from [52-56]

TFT properties	Oxides	a-Si:H	poly-Si (LTPS)	Organics
μ (cm ² V ⁻¹ s ⁻¹)	1 to 100	1 max	50 to 100	0.1–1
S (V dec ⁻¹) ⁺	0.1 to 0.6	0.4 to 0.5	0.2 to 0.3	0.1 to 1.0
Leakage current (A) ⁺	10 ⁻¹³	~10 ⁻¹²	~10 ⁻¹²	~10 ⁻¹²
Reproducibility	High	High	Low	Low
TFT for AMOLEDs	4 to 5 masks	4 to 5 masks	5 to 9 masks	Poor applicability*
Manufacturing cost	Low	Low	High	Low
Long term TFT reliability	High (forecast)	Low	High	Low in air
Yield	High	High	Low	High
Process temperature (°C)	RT to 350	~250	<550	RT
CMOS fabrication	Yes and large areas	Very low performance	Yes, not for large areas	Low performance

⁺Highly dependent on the dielectric layer.

*Most organic semiconductor layers are patterned using shadow masks.

Another group of materials used as semiconductors is organic semiconductors. They are promising for applications where flexibility and large area manufacturing in low temperature are preferred. However, the n-type organic semiconductors still have relatively low mobility and they are not reliable long term. The p-type organic semiconductors are much better. While organic semiconductors are still being developed, they might be widely used in the future. [21, 57]

As can be seen from Table 1, the different semiconductor materials vary in their properties in a TFT. Polycrystalline silicon has high mobility, but the reproducibility is low, and manufacturing is expensive and done at a relatively high temperature, incompatible, for instance with glass substrates used for active-matrix liquid crystal displays (AM-LCD). Amorphous silicon is less expensive to make and done in lower temperature but has low mobility. Organic semiconductors have their biggest problems in the device structure, which is an issue that will get better with further development. Oxide semiconductors seem the best alternative, in the near term, compared to the other ones in the table. Their biggest problems are in the long-term stability, which is also studied and developed. [28]

When designing circuitry, both n-type and p-type devices are needed. Then a good solution is to make hybrid circuitry with different semiconductor materials. For example, since p-type organics are working reasonably well and n-type metal oxide semiconductors are good, both can be used to make complementary devices for the circuit. [57-61] And this pathway is only expected to improve as each technology improves and printing is mastered.

2.6 Metal-semiconductor- and Insulator-semiconductor-interfaces in TFTs

The metal-semiconductor interfaces are between the drain and the channel, and the source and the channel. In the presence of an accumulation in the channel, the source metal terminal injects electrons to the channel. The electrons are withdrawn from the channel at the semiconductor-drain interface. The metal-semiconductor interfaces should be ohmic. In an ideal ohmic contact, it does not matter if a negative or a positive voltage is applied on the electrode. There is no appreciable energy barrier, which could prevent the current from flowing. [49]

If there is a great difference between the work functions of the metal and the semiconductor, a Schottky barrier is formed, which can lower the on-current of the device considerably. [49] This is seen as the contact resistance. If there is significant contact resistance compared to the resistance from the semiconductor material, channel resistance, it may cause non-linearity between the drain current and the drain voltage. [62] Additional, interfacial layers between the semiconductor and metal, such as native oxides, can form that also lead to effective Schottky barriers. Work function differences can be avoided by choosing suitable combination of materials or using a layer between the two materials, which makes the electron injection easier. [49]

The insulator-semiconductor interface is between the channel and the gate-insulator material. It has a huge impact on the properties of the device, because only a thin layer of atoms in the semiconductor material comprise the active region of an FET along the insulator-semiconductor interface. Any impurities or traps in the semiconductor layer affect the properties of the device. [49] The gate-insulator layer should be as smooth as possible, to ensure a good surface for the active layer deposition for bottom gate devices. When making top gate devices, the gate insulator deposition should be done so that the quality of the active layer under it is not affected adversely.

3. TFT CHARACTERISTICS

The performance of a TFT needs to be evaluated to see how well the device is functioning and to quantitatively compare devices to each other. A TFT is also never perfect. There are always little flaws in the structure and the materials cannot perform ideally. However, to be a functional transistor, a TFT does not have to be perfect; just good enough to function well in the intended circuit. To measure the quality of a TFT, there are some characteristics to help. [21]

The most important characteristics are on-off ratio, threshold voltage, mobility and sub-threshold swing, which are extracted from the transfer- and output-curves of the TFT. The oxide capacitance is also included here, because it is used when determining the mobility as well as further information about the TFT.

3.1 On-off ratio

The first characteristic is the on-off ratio of a TFT. The on-off ratio determines the difference in the drain-source current between the on- and off-stages of the transistor, as can be seen from Figure 6. The x-axis is the voltage at the gate electrode and the y-axis is the current between drain and source electrodes.

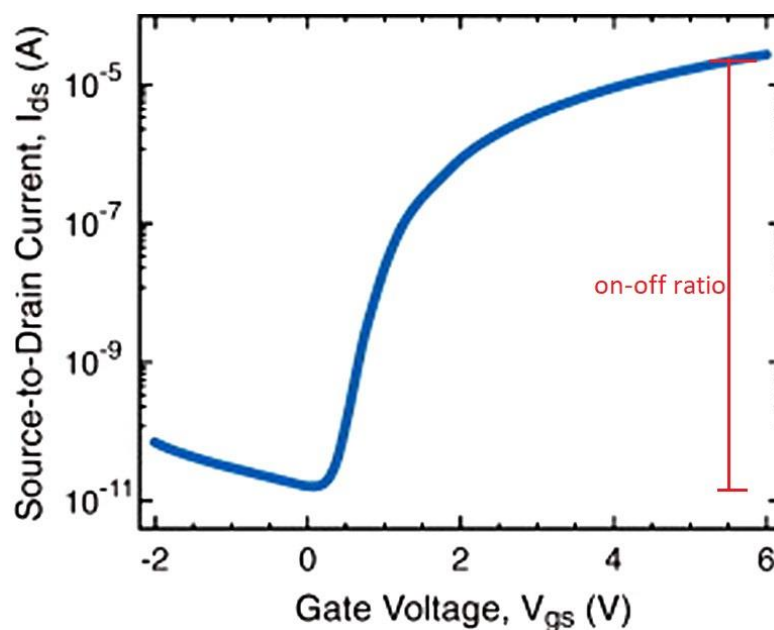


Figure 6. The on-off ratio. Modified from [63]

The minimum value for on-off ratio should be in the magnitude of 10^3 , but preferable to be 10^5 to 10^6 , possibly higher. Then the difference between the on and off currents is large enough and the transistor can be used in a digital circuit. [21] The larger the on-off ratio

is, the better. The on-off ratio in a-Si transistors researched has been around $10^5 - 10^7$ [64-66], in organic transistors researched around $10^3 - 10^7$ [67-72] and in transparent metal oxide transistors researched around $10^3 - 10^9$ [73-78].

3.2 Threshold voltage

The threshold voltage of a transistor shows the point at which the transistor turns on. At some gate voltage the transistor starts to conduct current from drain to source, and the magnitude of that voltage is the threshold voltage. [79] This point can be seen in the drain to source current – gate voltage-curve like that in Figure 7.

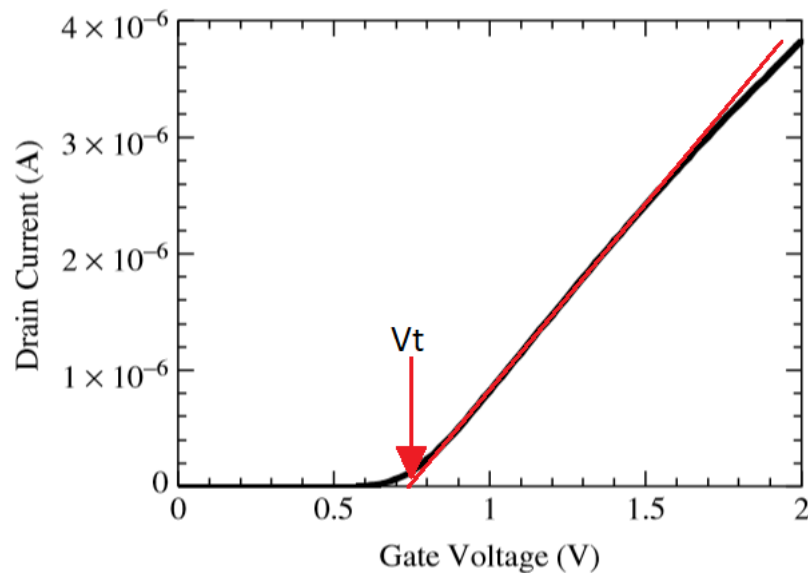


Figure 7. The linear region of the transfer curve is extrapolated to find threshold voltage (V_t). Modified from [79]

In a MOSFET, the threshold voltage is the voltage needed to create a conducting channel between the drain and source [79] while in an ideal TFT made of an intrinsic material the threshold voltage is zero. A low threshold voltage is highly desirable because it delineates the amount of power needed to switch the TFT output. In an ideal TFT all the charge induced at the electrodes is from free carriers and linearly increases the current with voltage. However, in a real TFT there are always localized states, such as traps, donors and acceptors, which need to be filled before the induced charge can be free. This creates a non-zero threshold voltage. [21]

The threshold voltage of a TFT can be extracted from the linear region of the transfer curve, or the square root of the transfer curve, by extrapolating to zero current. However, the resulting value of threshold voltage can be different when extracted from the linear region or the square root of the curve. This has to be considered when comparing values. Non-idealities in the TFT can cause the curve to be non-linear, which can make finding

the threshold voltage difficult, or even impossible in worst cases, because when the curve is not linear, the threshold voltage can change with the chosen bias point. [21]

Localized states affect the threshold voltage, if there are too many of them. Too many localized states will make the threshold voltage higher, because more voltage is needed for filling the trap states. This is a bad thing for a device which should, in an ideal case, be operated at low voltages. Also, the traps and doping in the semiconductor material can cause the V_T to change with temperature or light, as more traps are depopulated by the external stimulus. It is beneficial to take care in the processing of the TFT to make sure the layers are well made, to make sure excessive traps are not formed, as well as doing the measurements in the same temperature and lighting, when comparing devices. On the other hand, one way of defining the concentration of localized states in the semiconductor layer is with the help of temperature changes during the measurement. [21]

3.3 Mobility

The mobility of a TFT describes how easy it is for charge carriers to move in the channel. This has a big effect on the switching times and frequency response the device will have. If the mobility is low, the charge carriers move slowly through the channel as well as charging the oxide capacitor, which is regulating the transistor, more slowly, because the overall current in the channel will be lower. This means the transistor cannot keep up with high frequencies, because the charges are not moving fast enough to work properly. Another aspect affecting the speeds to which a transistor can achieve is its channel length. The longer the channel, the longer it takes for charges to travel across it. [79]

The mobility affects the conductivity of a semiconductor according to the following equation [79]:

$$\sigma = q(\mu_n n + \mu_p p), \quad (3)$$

where q is the elementary charge, μ_n is the mobility of the n-type charge carriers, n is the n-type charge free carrier density, μ_p is the mobility of the p-type charge carriers and p is the p-type charge free carrier density.

When a TFT is described to be n-type, it is usually not doped, but the majority charge it carries are n-type, making it behave as if was doped n-type. Doping can be used, but it adds to the already existing charge carriers and can adversely influence the mobility.

Defining the mobility of a TFT can be done from the transfer curve. The square root of the curve is drawn, and the slope of the linear part is measured, as shown in Figure 8. The mobility derived this way is called the saturation mobility, because when considering conventional FETs, the channel of the transistor is pinched off in the linear part, which means the transistor is in saturation. [79]

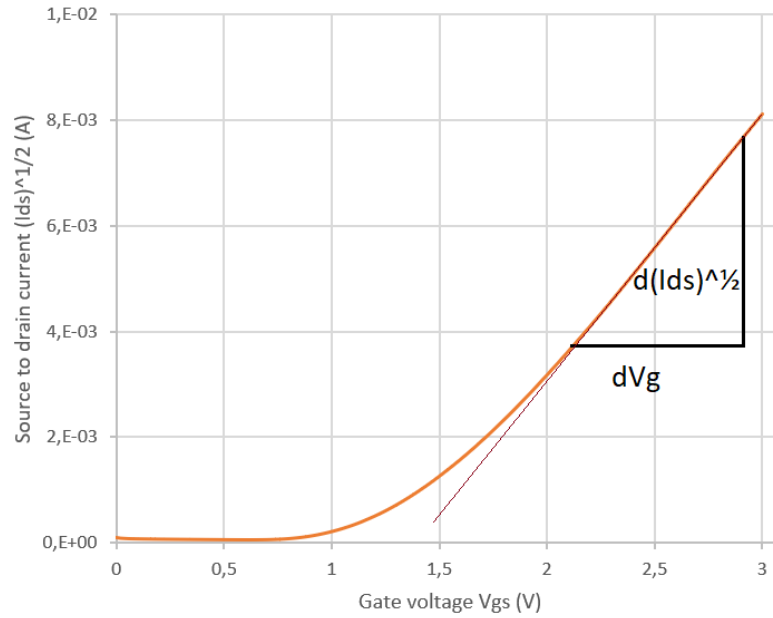


Figure 8. Measuring the slope of the square root of the transfer curve. The linear part is used for the saturation mobility value.

The saturation mobility is derived from Equation 4 [34, 79]:

$$\mu_{sat} = \frac{2}{C_{ox}} \frac{W}{L} \left(\frac{d\sqrt{I_{ds}}}{dV_g} \right)^2, \quad (4)$$

where C_{ox} is the oxide capacitance, W is the width of the channel and L is the length of the channel. The linear mobility is derived from the equation 5 [80] :

$$\mu_{lin} = \frac{L}{WC_i V_{SD}} \left(\frac{\partial I_{SD}}{\partial V_G} \right), \quad (5)$$

where C_i is the insulator capacitance.

The mobility can be calculated different ways. For example, effective mobility from the conductance [34, 79] :

$$\mu_{eff} = \frac{g_d}{C_{ox} \frac{W}{L} (V_g - V_T)}, \quad (6)$$

where g_d is the conductance and V_g is the gate voltage. Another way is to use the transconductance to calculate the field-effect mobility [34, 79] :

$$\mu_{EF} = \frac{g_m}{C_{ox} \frac{W}{L} V_{ds}}, \quad (7)$$

where g_m is the transconductance.

3.4 Subthreshold swing

The subthreshold swing is a characteristic which describes how much the gate voltage has to rise for the drain-to-source current to rise for one decade. It can be determined from the transfer curve as can be seen from Figure 9. Equation 8 shows how to calculate the subthreshold swing [34] :

$$S = \left(\frac{d \log(I_{ds})}{dV_g} \Big|_{max} \right)^{-1}. \quad (8)$$

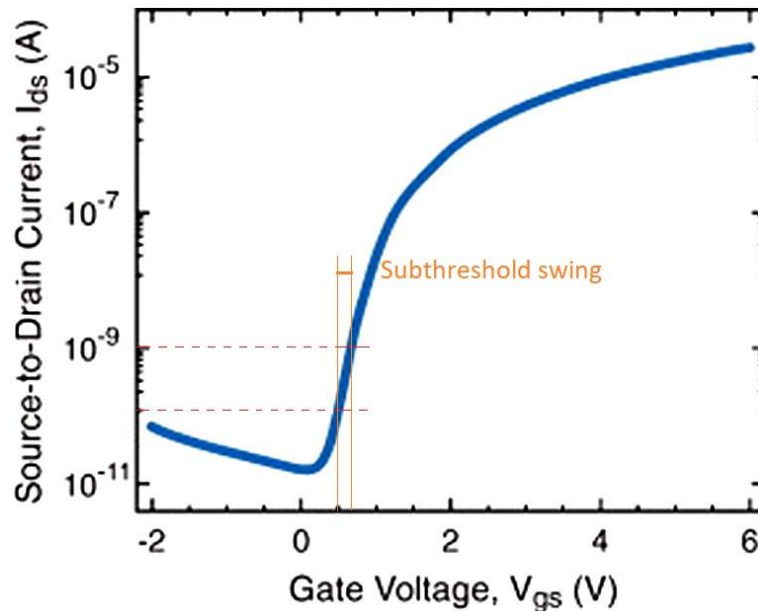


Figure 9. The subthreshold swing is determined from the inverse of the maximum slope of the transfer curve. Modified from [63]

A small value of subthreshold swing means the gate voltage has to be increased very little to increase the drain-to-source current for one decade. This is a good thing for a transistor, for it means the operating voltages are low and power consumption is lower. For a good TFT the subthreshold swing should be around 0,01 – 0,03 V/dec⁻¹, although this is much higher than conventional Si CMOS with ~60 mV/dec⁻¹. [34]

3.5 Oxide capacitance

The current of the TFT is modulated with the metal-insulator-semiconductor -capacitor. The insulator is often an oxide, which is why the term oxide capacitance is used when this value is discussed. The oxide capacitance has an effect on the drain-to-source current, as can be seen from Equation 1, and mobility, as can be seen from Equations 4, 5, 6 and 7.

As mentioned in Section 2.3, oxide capacitance can be affected in two ways: the thickness of the insulator layer and the dielectric constant of the insulator material. Both of these features are highly dependent on the chosen material, but TFTs have some special requirements as well. When fabricating a TFT, high temperatures cannot always be used, especially when the substrate material is plastic or paper. This limits the fabrication methods that can be used for the insulator material. [28]

Another reason for considering fabrications methods is solution processing. The insulator material has to be mixed with a solvent for printing and usually requires some sort of heat treatment after the deposition. This also combines the limitations of substrate material heat resistance. [28]

Because the oxide capacitance plays a critical role in the operation of the TFT, the material and processing method have to be considered carefully. If the capacitance is too low, the TFT needs higher operating voltages, as it will not perform well in high frequencies. Too high leakage current from the gate also affects the operation of the TFT. [28]

4. TFT PROCESSING TECHNIQUES

The processing techniques used during the making of a TFT have an impact on many things. Firstly, some techniques are more expensive or time consuming than others. Secondly, not all techniques can be used in every case, because there are limitations on, for example, the used temperatures and exposure to chemicals from the materials used. Thirdly, the processing techniques have an impact on the properties the device will have. Some deposition methods can create a more uniform, or defect free, layers than others. These aspects are important when choosing the correct deposition method for each material. In this chapter, some popular techniques are introduced, and the ones used in this work are focused on more. Inkjet printing is explained, because it is a possible topic for further studies on these metal-oxide based transistors.

4.1 Metal oxide deposition

Metal oxides are the active layer of the TFT, which has to be deposited on the substrate with some technique. These techniques can be roughly separated in two categories: vacuum deposition or solution-based processes. Vacuum deposition processes require a vacuum at some point of the process as indicated by their name, and solution-based processes have the active material diluted into a solution, which is used to spread it uniformly to make the layer. [81]

As mentioned in Section 2.6, only the first few monolayers, or even the first one, have significant impact on the properties of the transistor. The chosen processing method has to form a good quality layer especially in the first monolayers. There is some difference between the layer qualities made with different deposition methods, but sometimes there are other aspects to consider in addition to the layer quality, which might impact the chosen method, such as temperature considerations.

4.1.1 Vacuum deposition

Vacuum deposition methods as a group require a vacuum during the process to provide ample mean-free path for deposition material to reach the substrate without encountering stray gas molecules. They are used more in the industry already, which makes developing TFTs made with these processes faster for industrial manufacturing. Especially sputtering is a technique widely used in industrial capacity already. Other vacuum deposition methods are atomic layer deposition (ALD) and pulsed-laser deposition to name a few. [81]

Sputtering is a physical vapor deposition method (PVD). In physical vapor deposition methods there is a target source in solid form, from which atoms are removed in a physical process by energetic ions created from a process gas, usually inert (i.e. Ar), accelerating

onto the target and liberating atoms, or clusters of atoms. If the substrate is placed in close proximity, these sputtered materials deposit onto the substrate. A low-pressure chamber is needed to provide sufficient mean-free path lengths for target atoms to deposit well. [82]

ALD, which was invented in Finland, is a gas phase deposition method, which is studied and heavily researched currently. It is a self-limiting chemical vapor deposition method (CVD). ALD is also highly conformal, and pinhole-free, due to the self-limiting reactions. The substrate is in a vacuum chamber where the deposited material is injected as a gas. The gas sources are usually molecules, such as an organometallic, containing a metal atom, and an oxidizer, like water. If the material has more than one element in it, which is most common, like a metal-oxide, one source is injected first, forming a monolayer of molecules bonded to the surface, and the second source reacts with the monolayer, forming the compound layer. Each material requires a certain temperature for the reaction to happen, but the temperature does not have to be exact, rather in a certain temperature window, in which the reaction will happen well. [83]

Sputtering is used widely, because the capacity to manufacture with the method is already there and the deposition rates are faster than with ALD. However, the thin films deposited with ALD are better quality and stoichiometry, and thinner films of tens or less nanometres are much more uniform than sputtered ones. Because small fluctuations in the temperature of the substrate or the gas flow do not affect the uniformity of the deposited layer in ALD, the thickness of the film is more uniform in ALD than sputtering, especially with thinner layers. However, some materials require somewhat higher temperatures in the ALD process, which limits the use of this deposition method as well. [82, 83]

4.1.2 Solution-based deposition

In a metal oxide solution-based deposition method the material is diluted into a solution, or ink, with appropriate solvents. The metal oxide solution is then used to fashion the thin film. The material can be mixed into the solution as nanoparticles, sol-gel mixture, or a hybrid of both of those like seen in Figure 10. The solution is spread on the surface and the solvent and other organic parts of the solution, for example dispersion agents, are removed by evaporation during/after application. The advantage of solution processes is that they do not require a vacuum. Some printing processes also have great potential for large area, low cost manufacturing. [81]

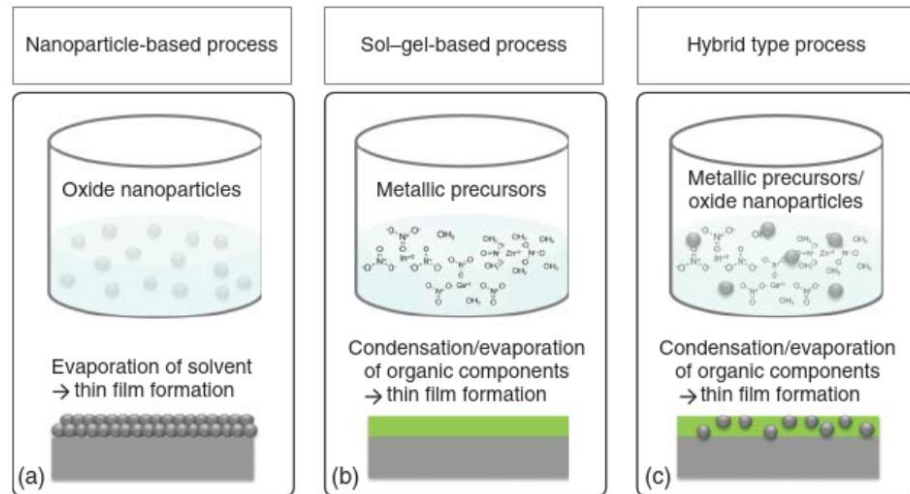


Figure 10. Different solutions used in metal oxide thin film formation. a) is a film made with a solution of nanoparticles, b) has a sol-gel solution and c) is a hybrid solution of nanoparticles and metallic precursors. [81]

In the case of nanoparticles, the evaporation process is usually done in relatively low temperatures, but the particles have to attach to each other to create a uniform film, which might require a higher temperature. In the case of a sol-gel solution, the molecules in the solution form an oxide network during the post-deposition annealing and an amorphous thin film is created. To make a crystalline film, the annealing temperature has to be higher. [81]

Nanoparticle based solution process usually requires lower temperatures than sol-gel processes, but in case of oxide semiconductors the goal is usually an amorphous film, which is easier to make with sol-gel solution. Also, the grain boundaries between the nanoparticles can lower the charge carrier mobility of the material. Metal-oxide semiconductor films are widely made with sol-gel based deposition processes. [81]

When low temperature processes are preferable, the annealing temperature can be changed by some modifications in the process or materials. The composition of the solution can be modified, the annealing environment can be altered or an alternative method for annealing can be used. [81] Sol-gel inks are easy to modify and developing the ink usually requires experimenting with different compositions to find the best proportions. [34]

The annealing environment can be modified in several ways to lower the annealing temperature and reduce the number of defects in the film. Some modifications are, for example, changing the humidity [84, 85], using ozone dilutions, O_2/O_3 in the atmosphere, [86] and pressure [87-89]. The annealing process can also be partly or completely done with alternative methods, such as ultraviolet (UV) light [90] or photochemical annealing [91-95]. The idea of alternative annealing is bringing the needed energy for the solidification and evaporation from other sources than heat.

Several different techniques can be used to spread the solution into a thin film. One is inkjet printing, which is discussed more on Section 4.3. A second one, spin coating, is used in the transistors made in this work. The basis of spin coating is using a high-speed rotation to spread a liquid into a thin film. It is simple to implement, and a facile pathway for rapid prototyping. The spinning speed and duration can be changed to achieve the best possible combination for each ink. Changes in viscosity and wettability are some aspects to consider when choosing the right speed. Low viscosity materials spread more easily, so lower speed is enough. However, if the wettability of the material is bad and surface tension is not sufficient, the resulting film might not be uniform. To avoid bad wetting, the substrate material has to be chosen correctly, cleaned well and if required, a surface modification process can be done before spin coating. [96]

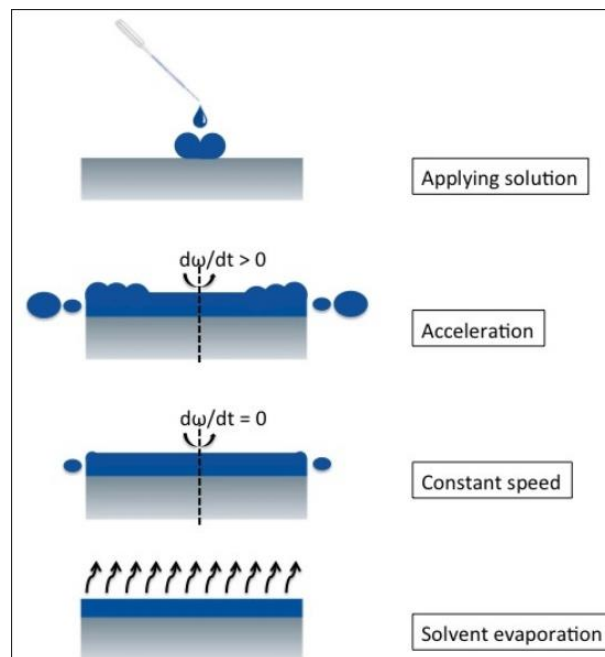


Figure 11. The spin coating process: first the solution is applied to the substrate, then the coater accelerates to the required speed in certain time, which allows the solution to spread, then the substrate is spun with constant speed until the required thickness is achieved and lastly the solvent is evaporated. [97]

In Figure 11, the basic spin coating process steps can be seen. With spin coating, a film thickness of a few nanometers can be achieved with the right parameters. The substrate must be clean and defect free, the solution of the right constitution and viscosity, and the spinning parameters well chosen. The amount of solution dispersed on the substrate at the start of the process as well as the atmosphere where the spinning is done have an effect as well. If the humidity changes a lot, it can have a significant effect on the quality of the film. [96]

4.2 Gate insulator anodization

The material used as gate insulator in this work is aluminium oxide (Al_2O_3), which is a high- κ dielectric material. There are many deposition methods used to make thin Al_2O_3 films for gate dielectric. Methods like solution processing [98, 99], PVD [100-102], CVD [103] – especially ALD [104, 105] – and anodization [106-110] are used. Since anodization is the method used in this work, and the other methods are already discussed in Section 4.1, this chapter will focus on anodization as a thin film deposition method for the gate oxide.

Anodization, or anodic oxidation, is a process in which, in this case, an aluminium surface is put into an electrolyte with a counter electrode, such as platinum, and a positive voltage is applied to the aluminium, which starts to oxidize in the solution. The basic set up can be seen in Figure 12.

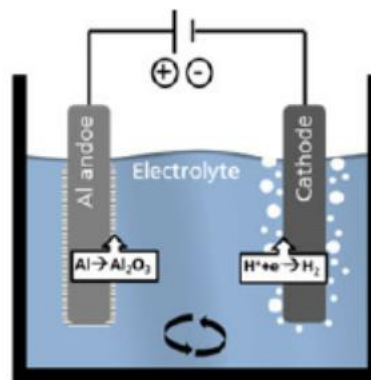


Figure 12. Anodization process set up, where aluminum anode and cathode, in this work platinum, are put in an electrolyte solution and a positive voltage is applied to the anode. [111]

The anodization can be done as a potentiodynamic or as a potentiostatic process. In a potentiodynamic process the voltage applied to the anode is changed with time until a desired voltage is reached, and the oxide layer thickness is satisfactory. In a potentiostatic process a constant voltage is applied to the anode, and the current goes down with time, when the oxide layer grows. In both cases the magnitude of the voltage determines the thickness of the oxide layer. [107, 112, 113]

The anodization process has some good qualities. Firstly, it can be done in room temperature, and it does not require a vacuum. Second, the thickness of the oxide layer is easy to control in the process with the voltage. Thirdly, the resulting layer is amorphous and has few pinholes, as they are filled during the process. The cost of anodization is low as well, because it does not require any expensive equipment. [112, 113]

4.3 Inkjet printing

Inkjet printing is an additive deposition method, where a nozzle releases drops only on places where they are intended to be, which is called drop-on-demand (DOD), or the nozzle releases drops continuously and the excess drops are filtered out before they reach the surface. In piezoelectric printers a pulsed voltage is used to create pressure when a drop is needed. There are printers that use thermal pulses for drop formation, but for temperature sensitive inks, the piezoelectric printer is better. The basic setup can be seen in Figure 13. The printers have two directions of movement for movement within a plane, as well as a changeable z-direction height point for the start position, which is used to position the printed pattern above the right place on the substrate. [114]

The ink used in the printer has to be relatively low viscosity, around 1-20 centipoise. The drops formed by the nozzle are a few picolitres in volume. The drop size can be controlled to a point with the voltage amount and duration. The voltage should be large enough to produce stable droplets, but too large a voltage will create a satellite droplet, which can cause the ink to spread to unwanted places on the substrate. [114]

When the droplet reaches the surface, it should have good enough wetting, or the ink will not form a uniform layer on the surface. The distance of drops, drop spacing, has to be considered as well. The drops should be close enough to have contact and create a smooth layer, but not too close, or the ink might flow to wrong places on the substrate. Each ink has its own viscosity and surface energy and reacts differently on different substrates, which means each combination needs their own settings when printing. [115]

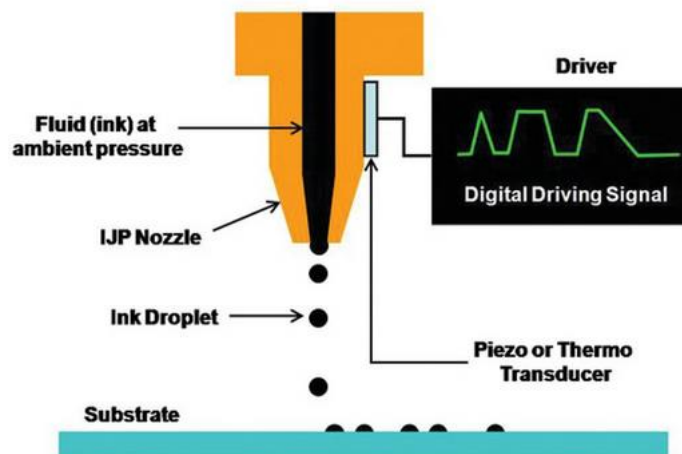


Figure 13. Inkjet printing process, modified from [116]

Inkjet printing has some favorable qualities as a deposition method. As an additive method it has less process steps than subtractive methods. It also wastes less material especially as a DOD process. Being a low temperature process, which requires no vacuum, it can be used on different substrates including flexible and plastics. Inkjet printing

is also a noncontact process, which means only the droplets are in contact with the substrate. This creates much less damage and contamination to lower layers. The layers are also easily focused in right places relative to each other. As the printing patterns are in digital form, they are easily modified. [114]

Some aspects of inkjet printing are not ideal and other printing methods might be better. Large area manufacturing is not as fast as, for example, gravure printing. Gravure printing also has better resolution than inkjet printing. However, in gravure printing, changing the pattern is more difficult, because new plates need to be designed and manufactured, and positioning the layers relative to each other with exact alignment is more difficult. [114]

While inkjet printing itself is a low temperature deposition method, annealing the ink requires higher temperatures, when considering metal oxide semiconductors. MOSs might need annealing temperatures in the range of 300-400°C, which rules out many flexible substrate materials. To address this problem, some alternative annealing methods have been studied, like combustion process [117] and UV-annealing [118].

5. SAMPLE STRUCTURE, FABRICATION AND MEASUREMENT

In this chapter, the transistors made for this work are discussed. Their device structure and used materials are explained and the methods to make the transistors are discussed. Also, the processes used for measurement and characterization of the devices are explained.

5.1 Device structure and materials

The TFTs made for this work are bottom gate, top contact staggered structures. The substrate is a 25×25mm glass plate. The gate on top of the glass is aluminium, and the gate insulator material is aluminium oxide. The semiconductor is an indium oxide -based material called Ixsenic from Evonik, which is transparent. On top of the semiconductor are the source and drain contacts, which are made of evaporated aluminium. The TFT structure can be seen in Figure 14.

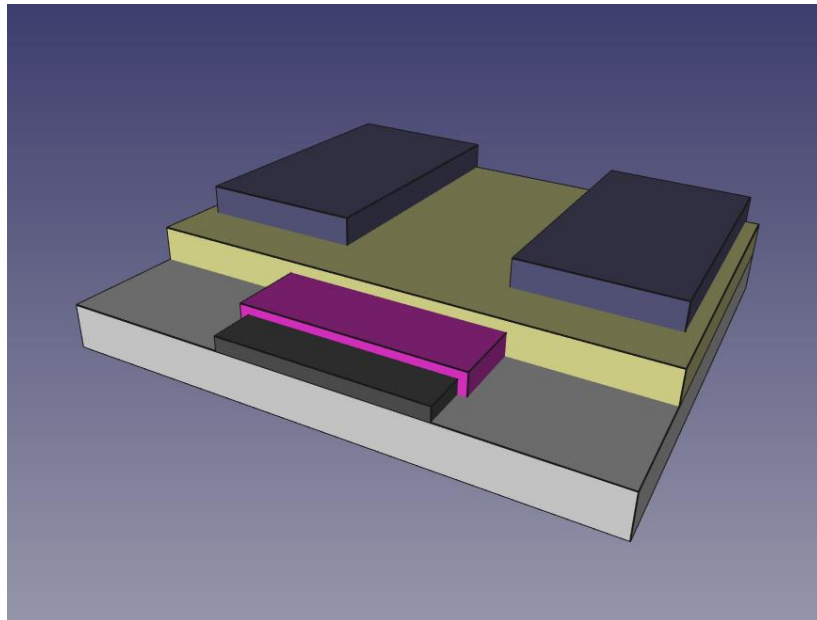


Figure 14. The TFT structure: the grey area in the bottom is the glass substrate, the black on top of it is the gate electrode, the pink is the gate insulator, the yellow is the Ixsenic semiconductor and the dark grey areas on top are the source and drain contacts.

The channel length in the transistor is 60 μm , the channel width 700 μm , the thickness of the gate electrode layer is 50 nm, the thickness of the gate insulator approximately 10 nm, the thickness of the semiconductor layer between 5 to 30 nm depending on processing parameters and the thickness of the drain and source electrodes is 100 nm.

The materials of the TFT stay the same in all the devices made for this work, but some dimensions and processing parameters are changed when optimizing the device. The transistors are made on a glass plate with 5-6 vertical gate electrodes, each of which has 6-9 operational transistors on them. Figure 15 shows two vertical gate electrodes and each has 3 transistors. This way there are at least 30 transistors of the same kind to compare to each other.

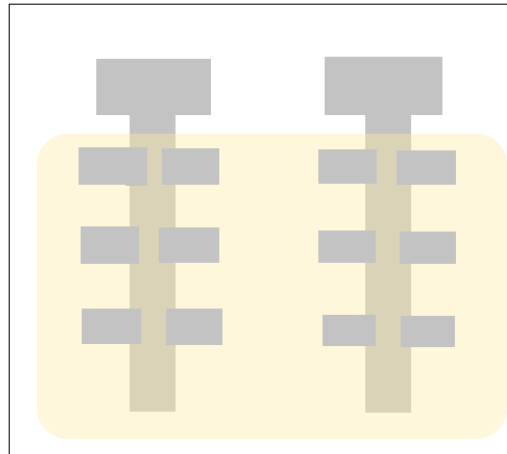


Figure 15. *Two vertical gate electrodes on a glass plate, they are covered with the semiconductor (in light yellow) and 3 sets of source and drain electrodes on both gate electrodes. This equals 6 transistors in the sample.*

In the real transistors, the light yellow as seen in Figure 15, the semiconductor, is spread on the whole plate and the gate electrode is probed through the semiconductor layer. Some of the transistors on the edge of the plate might not be useful if the electrodes are not perfect or the semiconductor is not spread uniformly. However, there are many transistors on the sample, so the defective ones can be removed from the data set.

5.2 Fabrication and processing parameters

The TFTs were made by first cleaning a glass substrate; evaporating the gate electrode on the substrate; anodizing the gate insulator; spin-coating the semiconductor; and lastly evaporating the source and drain electrodes on top. The basic processes stay the same in all samples, but some processing parameters are changed while optimizing the devices. The range of processing parameters can be seen in Table 2.

Table 2. The constant processing parameters used during making the TFTs on the top part of the table and below the variable processing parameters used when optimizing the device.

constant parameters	evaporation rate	anodization voltage	anodization time	annealing temperature	
	3 Å	5 V	30 min	350°C	
variable parameters	storing before anodization	spincoater speed	UV curing time	annealing atmosphere	annealing time
	air or nitrogen	1000-8000 rpm	99-300 s	air or nitrogen	1-3 h

The glass substrate plate was cleaned in several stages. First the plate was washed with soap to remove any grease stains. It was then rinsed with DI-water. After drying the plate with pressured air, it was sonicated in room temperature for 10 minutes first in DI-water, then in acetone and lastly in isopropanol. After sonication in DI-water, the plate is rinsed with DI-water and dried with pressured air before sonication with acetone. After sonication in isopropanol the plate is dried with pressured air and moved to a glove box with nitrogen atmosphere.

The evaporation of the gate electrode is done as quickly as possible after the cleaning to minimize contamination and defects on the plate. The gate electrode is aluminium evaporated with electron beam (e-beam) evaporation at roughly $1,3 \cdot 10^{-6}$ mBar (10^{-6} Torr) chamber pressure. The evaporation rate is 3 Å per second to ensure uniform layer. The final thickness of the aluminium is 100 nm. If the thickness of the electrode is too high, it will affect the spreading of the semiconductor during spin-coating, which is why thicker gate electrodes are not made. After evaporation, the sample is either anodized immediately or stored in nitrogen or air. Nitrogen prevents the formation of native oxide on the aluminium but storing the sample in air for a set time allows the native oxide layer to form, which can be compared to samples anodized straight from nitrogen environment.

The anodization is done in a mild citric acid solution with 200 mg of citric acid in 100 ml of DI-water which makes a solution of $0,01 \text{ mol/dm}^3$. The counter electrode in the system is a platinum wire. The anodization is done by applying a 5 V voltage in the circuit. The current is limited to 500 mA, which means that the voltage rises to 5 V and then the current starts to drop, while the voltage stays constant. This reaction is done for 30 minutes, after which the sample is rinsed with DI-water and dried with pressured air a few times to clean it. The current at the end of the reaction is around $3 \mu\text{A}$ if the reaction is successful. This creates a layer of aluminium oxide about 10 nm thick.

After anodization the semiconductor layer is applied with a spin-coater. After dispensing the solution onto the sample in a puddle, the sample is first accelerated to 500 rpm for a few seconds and then accelerated to 1000-8000 rpm, depending on the sample, for 30

seconds to create the layer. After spinning, the layer is first annealed with UV-light for a minimum time of 99 seconds to get a minimum dose of 15 J/cm^2 for UV-curing. The UV-light source was a Dymax Blue Wave spot lamp with the wavelength of the UV-light being 300-450 nm. The measured power of the lamp was 154 mW/cm^2 . Then the sample is annealed on a hotplate at 350°C for 1 to 3 hours in air or nitrogen atmosphere.

After annealing, the source and drain electrodes are evaporated with e-beam on top of the semiconductor. The evaporation rate is again 3 \AA per second. The thickness of the source and drain electrodes is 50 nm. The samples are characterized, and they can be left in air or nitrogen for a time and characterized again to see the effect of different atmospheres have on the devices in time.

5.3 Measurement and characterization

After making the samples, they are characterized in the same day or the next day to minimize aging of the samples. If there are visible defects in some of the transistors on the sample, those transistors are not characterized. These defects could be dust particles in the structure or imperfectly evaporated electrodes at the edge of the sample for example. The characterization is done with a Keysight B1500A Semiconductor device analyser. The Keysight analyser is used to measure transfer and output curves, gate leakage current and oxide capacitance of the transistors.

The transfer curve is measured with the gate voltage from 0V to 3V in most cases. The drain-source voltage values from 0V to 2V with 0,5 V intervals are used. The gate leakage current is measured for each of the transfer curves at the same time with the transfer curve. The output curve is measured with drain-source voltage from 0V to 3V with the gate voltage from 0V to 3V with 0,2 V intervals. The oxide capacitance is measured with voltage from -3V to 3V.

The optimal spinning speed for the best uniformity of the semiconductor layer was determined with the help of diode structures, where the transistor structure was made without the gate electrode. The current-voltage curve from these diode structures was measured with the Keysight analyser as well.

6. RESULTS AND DISCUSSION

The goal of this work is to determine if Ixsenic semiconductor material can be used in a transistor structure with bottom gate – top contact with aluminium electrodes and anodized aluminium oxide as gate insulator. If the transistor is possible to make with this structure and materials, it will be optimized and then researched further to determine the function of the transistor more closely, or alternatively the semiconductor could be tried to print with inkjet printer.

The transistor was possible to make and was optimized, but when characterizing the devices, the need arose for a closer look on the density of interface states between the insulator and the semiconductor. Therefore, the printing was not done, and this work focuses on the more precise characterization of the transistor leaving printing for the further studies.

6.1 First transistors

The first samples were made with the following processing parameters: spinning speed 1000 rpm on one sample and 4000 rpm on the second, UV annealing time 99 s, annealing in air for 1 hour. The spin-coating was done straight after anodization, so the samples were not stored in between.

The first transistors were made with glass substrates cleaned with sonication with each chemical for 5 minutes only and there were a lot of defects on them because the substrate was not clean enough. The transistors had very high gate leakage current of tens of microamperes. This made it impossible to see how the transistor performed. To fix this problem a second batch of samples was made with special focus on doing the anodization as well as possible.

In the second batch of transistors the problem of not cleaning the substrates for long enough time was crucial. The pinholes created because of lack of cleaning can be seen in Figure 16. One pinhole is shown more closely in Figure 17. The middle of the pinhole clearly has dirt on it.

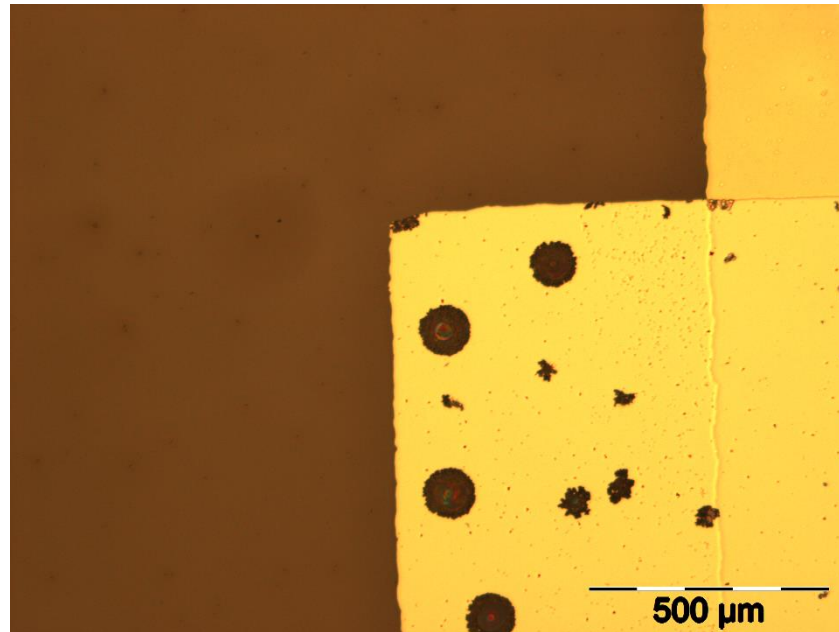


Figure 16. Pinholes in the source electrode in the second batch of transistors. The image is taken with microscope with 5x magnification.

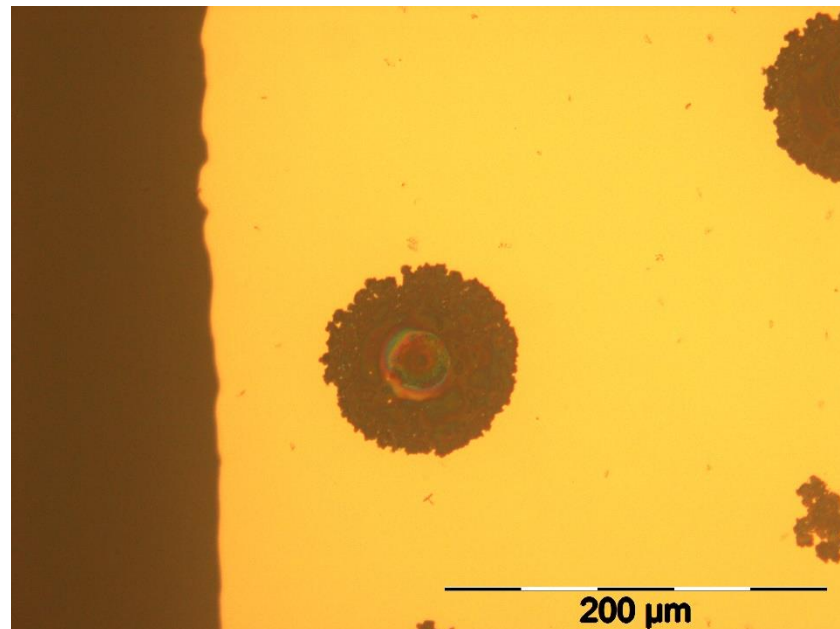


Figure 17. One pinhole seen more closely with 20x magnification.

The third batch of transistors was made with special focus on cleaning the substrates to make sure no pinholes would be in the transistors.

6.2 Changing the processing parameters of the semiconductor layer

The next batches of transistors were made changing some processing parameters in the making of the semiconductor film. First, the substrate was cleaned for 10 min with each

sonication. Second, the spinning speed was changed from 1000 rpm to 2000 rpm. The gate leakage current of the new transistors was lower than in the first transistors, which was a factor in the better performance of the third transistors. The change can be seen in Figure 18.

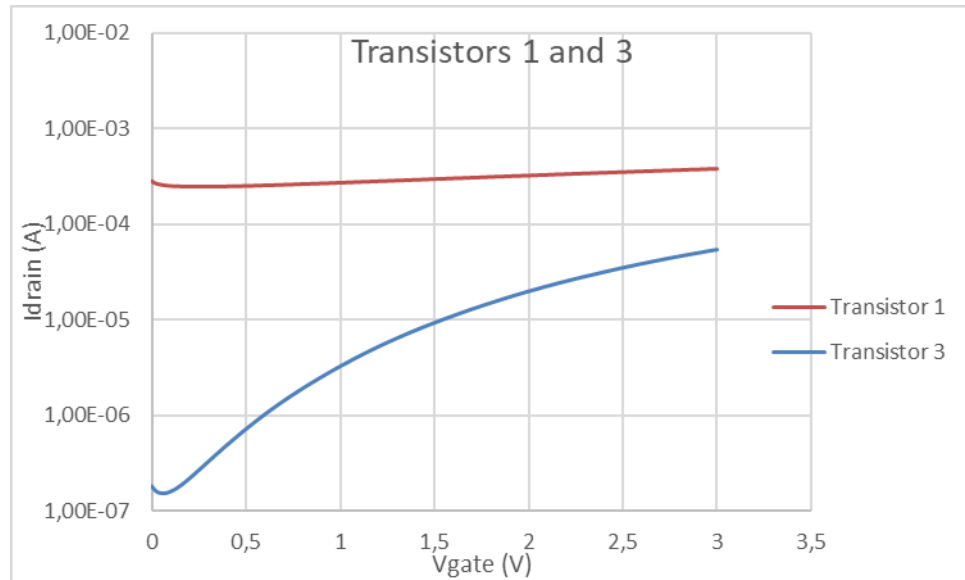


Figure 18. The transfer curves of the transistors 1 and 3 with drain voltage of 2 V.

The first transistor is not good, and it might have an alternative conductive path, because the current stays very similar with different gate voltages. The gate leakage current went up to 7 μA in the first transistor, but in the third transistor it was only 2 μA . The operating voltages can be seen from the third transistors. The gate voltage is 3 V, after which the gate leakage current rises too high. The drain voltage is 2 V at the highest. After that point, the current does not change noticeably, if the gate voltage is kept at 3 V.

The next batch of transistors was made with the same parameters as the third one, but the UV annealing time as well as the hotplate annealing time was altered using 99 s, 200 s, or 300 s UV annealing time and 1 h, 2 h, or 3 h hotplate annealing time. However, the resulting transistors were so unstable, that comparing them was pointless. A negative gate voltage was applied to these transistors to see if the semiconductor layer was doped. Because the negative voltage did not shut the accumulation channel, it was deduced there was no doping in the semiconductor. This means there are most likely some leakage pathway in the semiconductor.

In the fifth batch of transistors the effect of UV annealing time and hotplate annealing time was studied again. In Table 3, the mobility, threshold voltage, on-off ratio, gate leakage current and yield, percentage of working transistors in a sample, can be seen. There are three samples compared to each other. The spinning speed is 2000 rpm in each of them, but the first sample was UV annealed for 99 s and annealed on a hotplate for 1 h in air at 350°C, when the second sample had longer UV annealing time of 300 s and the

third one had longer hotplate annealing time of 3 h in air at 350°C. With the power of the UV-light being 154 mW, the 99 s exposure means a 15,2 J/cm² dose of UV-light.

Table 3. The results from the fifth transistors. The first row is the reference sample with old processing parameters, the second has longer UV-curing time of 300 s and the last has longer annealing of 3 h.

sample	mobility (cm ² /Vs)	Threshold voltage (V)	on-off ratio (Vd = 2 V)	gate current (A)	yield
reference	2,6	1,05	1940	4,43E-06	25 %
300 s UV	1,95	1,08	2668	5,2E-06	29 %
3 h annealing time	4,09	1,34	2741	2,43E-06	61 %

The quality of the semiconductor layer seemed better in the fifth dataset of transistors. The mobility was reasonable, and the threshold voltage settled between 0,5 and 1,5 V in all the transistors. The on-off ratio of the fifth batch of transistors reached a magnitude of 10³. The transfer curves of transistors 3 and 5 are drawn in Figure 19 for comparison.

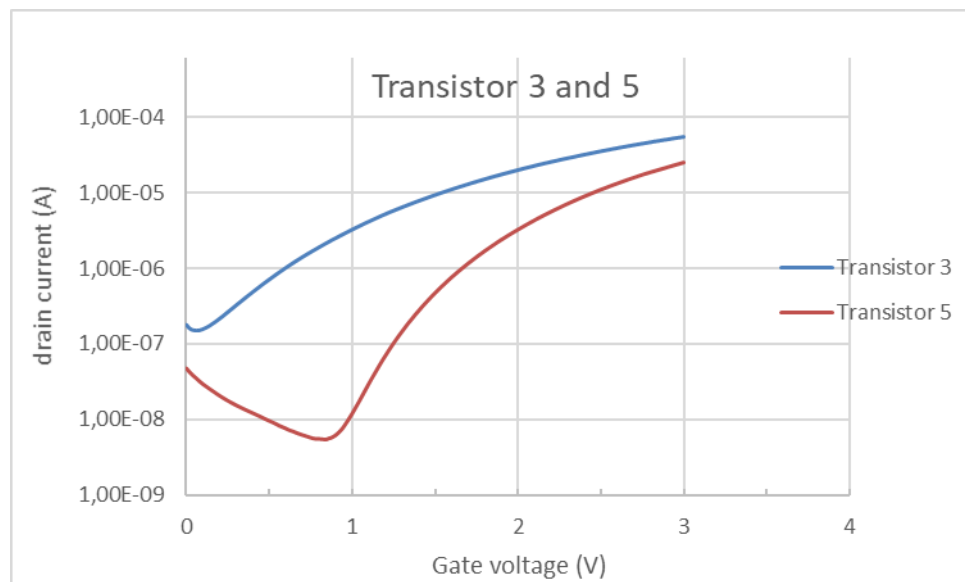


Figure 19. Transfer curves of transistors 3 and 5.

The results from the fifth transistors show that longer annealing is beneficial for mobility and percentage of working transistors. However, it slightly raised the threshold voltage. Both the longer annealing with UV and hotplate are studied further later.

There were some pinholes in the semiconductor layer. To solve this problem, the cleaning after anodization is considered in the next samples. The fifth transistors were also characterized again after 5 days and their off current had risen with one order of magnitude. The effect of storing the transistors is focused on later in this work.

6.3 Effect of cleaning after anodization and semiconductor layer thickness

The sixth batch of transistors was done to see if cleaning the samples with different methods after the anodization influences the quality of the semiconductor layer. The basic cleaning done with the samples is rinsing with DI-water and then drying with air gun for 3 times. With these samples also heating on a hotplate with 120°C for 30 minutes, rinsing with ethanol and cleaning with UV-ozone treatment were tried. Each of the samples had the spinning speed of 2000 rpm, UV-curing time of 300 s and annealing time of 3 h.

The different cleaning methods did not have a noticeable effect on the transistor quality, so the additional cleaning methods after anodization were not used on following transistors. The seventh samples were made to see how the different duration of UV-curing affects the transistors. The average results from the seventh transistors can be seen in Table 4.

Table 4. The average results from samples 7. The first sample was UV-cured for 300 s and the second 99 s. The main differences are in the mobility and the percentage of working transistors on the sample.

sample	mobility(cm ² /Vs)	Threshold voltage (V)	on-off ratio (Vd = 2 V)	Gate current (A)	working
UV 300 s	2,42	1,25	1039	1,57E-05	69 %
UV 99 s	1,01	1,32	918	9,81E-06	41 %

The mobility and percentage of working transistors on the sample were better with the longer UV-curing time. A slight decrease in threshold voltage was seen as well. Another observation from the results was the correlation between the gate leakage current and the on-off ratio. This can be seen in Figure 20.

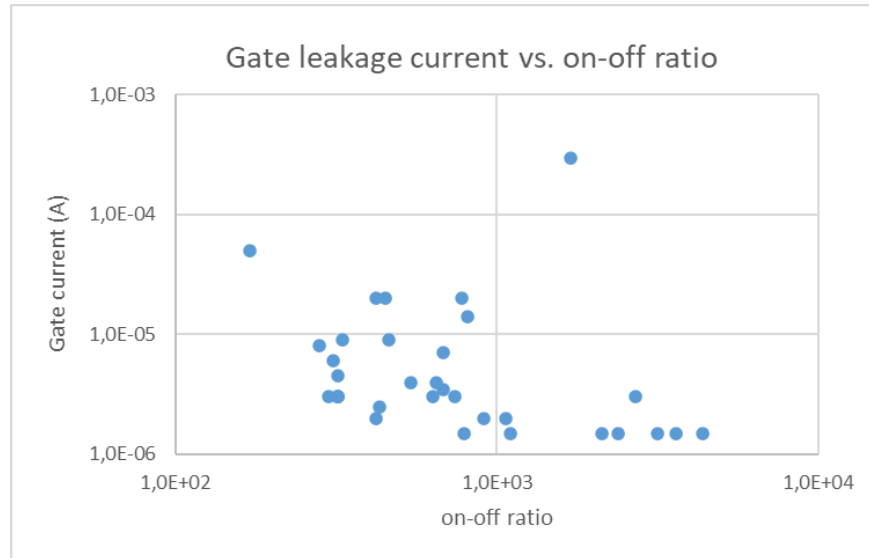


Figure 20. *The correlation between gate leakage current and on-off ratio of transistors. Each point in the figure represents one transistor.*

The transistors with on-off ratio closer to 10^4 magnitude all have gate leakage current lower than $5 \mu\text{A}$. Lowering of the gate leakage current was a targeted goal with the next batch of transistor samples. Before proceeding with more transistors, some samples with diode only structures were made to see the differences the spinning speed has on the uniformity of the semiconductor layer on the substrate. Diodes were made with 2000, 4000, 6000 and 8000 rpm to achieve different thicknesses of the semiconductor layer. The I-V curves of the diodes were measured and the diodes on one substrate were compared to each other to see how much variation their I-V curves had compared to each other.

The diodes from one substrate had the least variation, when using 6000 rpm as spinning speed. Then eight more transistors were made with spinning speeds of 6000 rpm to see how it affects the performance of the transistors. The difference between transistors 5 and 8 can be seen in Figure 21.

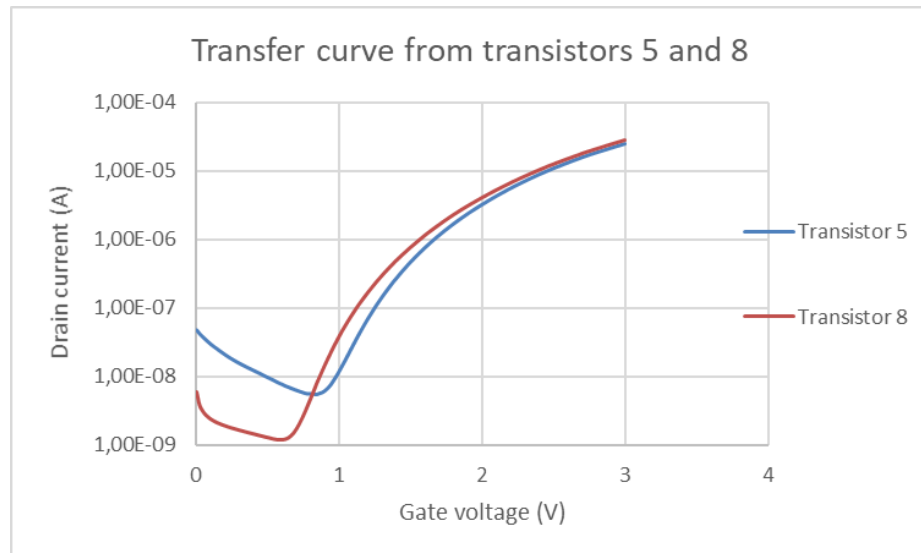


Figure 21. The transfer curves of transistors 5 and 8. The transistors were otherwise the same except the spinning speed in transistor 5 was 2000 rpm and in transistor 8 6000 rpm.

The on-off ratio of the transistor rose to the magnitude of 10^4 and the average mobility to $4 \text{ cm}^2/\text{Vs}$. The subthreshold swing was 0,2-0,3 V/dec. The percentage of working transistors also rose to 86%. The output curve from the eight transistors can be seen in Figure 22.

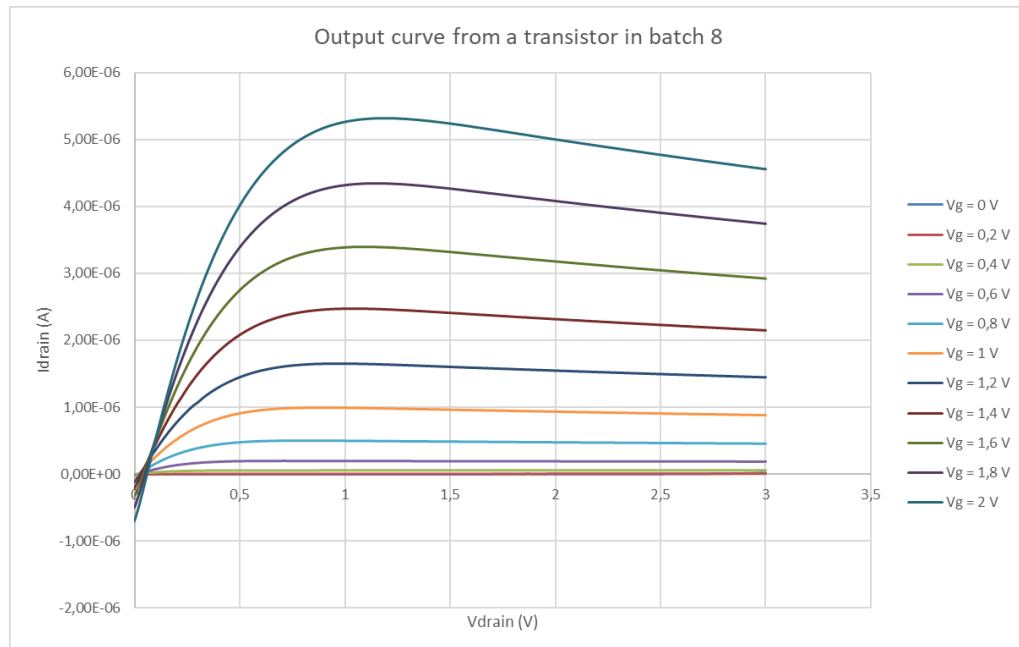


Figure 22. Output curve from representative transistor in batch 8.

Based on the transistors fabricated so far, the optimal process conditions are: the spinning speed is best at 6000 rpm; the annealing time at 3 h in air; and the UV-curing time of 99 s and 300 s were both used. These processing parameters are used in the following samples. The spinning speed of 6000 rpm gives a thinner layer of semiconductor than 2000

rpm and 4000 rpm. Because only the first monolayer is important to the operation of the device, the extra thickness in 2000 rpm and 4000 rpm layers is not needed. When comparing transistors from batches 5 and 8, the off-current seems to be larger with the lower spinning speed. The thicker film has more room for defects in the layer, which might explain the lower off-current in the thinner film. When increasing the spinning speed to 8000 rpm, the uniformity of the semiconductor layer seems to suffer, because more devices on the substrate were not functional.

The annealing time on the hotplate was 1 hour at first, which seems to produce decent transistors, but increasing the time gives better results. One hour might not be enough time for the bonding of the metal and oxygen atoms in the semiconductor and increased time allows the reaction to happen further in the material, giving more stable transistors on the substrate with better mobility. Longer annealing time also allows further densification and more byproducts are removed. The components of the semiconductor ink are not known, which makes it difficult to know exactly why the longer annealing time gives better results.

The increase of the UV-curing time has some benefit, mainly better mobility, and a larger number of functional transistors on a substrate. This points to the same conclusion as with the hotplate annealing time: The reactions in the material are still continuing after 99 seconds, offering better results with longer exposure time. However, the difference in mobility is small, which is why both exposure times are used later.

6.4 Storing the samples in N₂ and air

When characterizing the fifth transistors after storing them for a few days, they were different from their original values. The effect of storing the transistors in different environments was studied with the ninth batch of samples by storing them in nitrogen and air. These transistors were made with spinning speed 6000 rpm, annealing time 3 h and UV-curing time of 99 s and 300 s. They were characterized straight after processing, then stored in either air or nitrogen environment for two weeks and then characterized again. The resulting transfer curves can be seen in Figure 23.

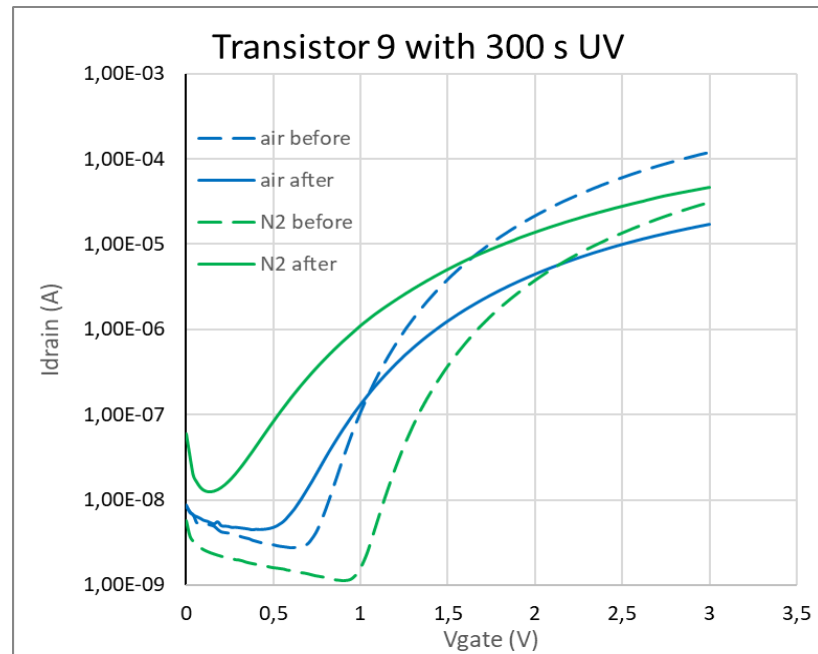


Figure 23. The transfer curves from transistor 9 with 300s UV-curing. The air and N2 refer to the gases they were stored in, and “before” means curve measured before storing and “after” means curve measured after storing.

The curves in Figure 23 show how the sample stored in air had lower on current after storing. The off current of the sample stored in nitrogen was higher and the threshold voltage had sifted noticeably. The samples were a bit different in the beginning, but in Figure 24, the samples with 99 s UV-curing are very similar at the start, so the changes can be seen more clearly.

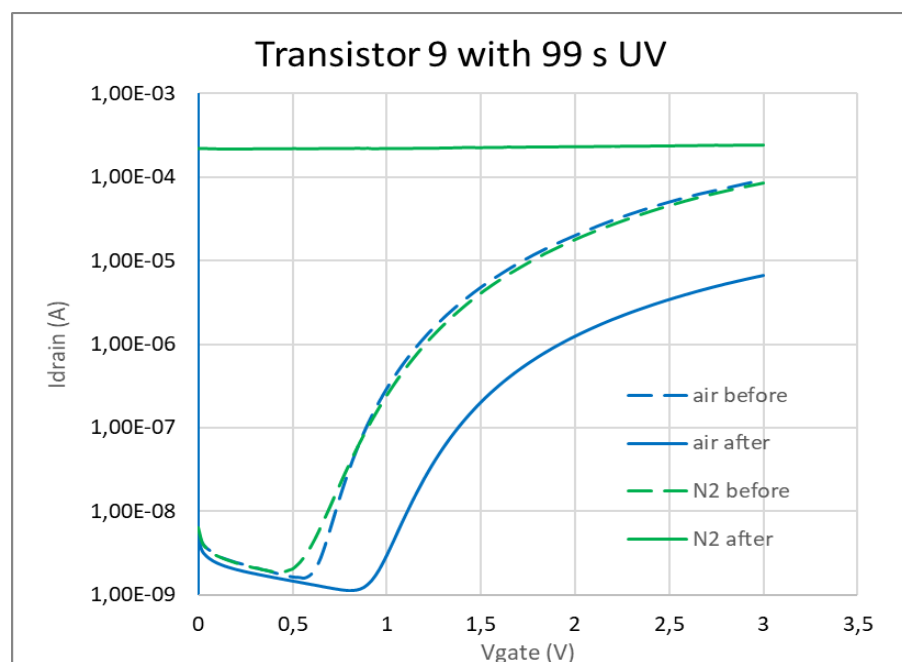


Figure 24. The transfer curves from transistor 9 with 99s UV curing before and after storing in air and nitrogen for two weeks.

The on current of the sample stored in air is again lower than previously and the transistors stored in nitrogen do not have a measurable off current anymore with positive gate voltages. To make sure the samples were not different before leaving them in different atmospheres for two weeks the mean values and standard deviations for those values were calculated. Those values can be seen in Table 5.

Table 5. The mean values of mobility, on-off ratio, threshold voltage, gate leakage current, on current and off current as well as the standard deviations for each value. The upper part of the table is for the sample with UV-curing time of 99 s and the lower sample with 300 s. The air and N2 refer to different samples, but they have not been in different atmospheres at the time of characterization, so they are added together to form the Both row of the table.

UV-curing 99 s		mobility (cm ² /Vs)	on-off ratio	Vt (V)	I _{gate} (A)	on current (A)	off current (A)
Mean	air	7,2	4,3E+04	1,3	6,1E-06	8,7E-05	2,3E-09
	N2	6,2	3,6E+04	1,2	8,7E-07	7,4E-05	2,1E-09
	Both	6,9	4,1E+04	1,3	4,7E-06	8,3E-05	2,2E-09
Standard deviation	air	1,6	1,1E+04	0,1	9,7E-06	2,7E-05	1,6E-09
	N2	1,0	1,3E+04	0,3	2,9E-07	3,1E-05	2,3E-10
	Both	1,5	1,1E+04	0,2	8,5E-06	2,8E-05	1,4E-09
UV-curing 300 s		mobility (cm ² /Vs)	on-off ratio	Vt (V)	I _{gate} (A)	on current (A)	off current (A)
Mean	air	7,2	4,3E+04	1,3	6,1E-06	8,7E-05	2,3E-09
	N2	5,1	3,1E+04	0,9	3,0E-06	6,5E-05	1,9E-09
	Both	6,3	3,8E+04	1,1	4,8E-06	7,7E-05	2,1E-09
Standard deviation	air	1,6	1,1E+04	0,1	9,7E-06	2,7E-05	1,6E-09
	N2	2,4	1,5E+04	0,5	3,4E-06	3,0E-05	5,9E-10
	Both	2,2	1,4E+04	0,4	7,7E-06	3,0E-05	1,3E-09

There is also a shift in the gate leakage current as can be seen from Figure 25. Storing in air moves the leakage current lower and storing in nitrogen makes it higher. However, the shift is not large enough to explain the changes in the transfer curves of the transistors.

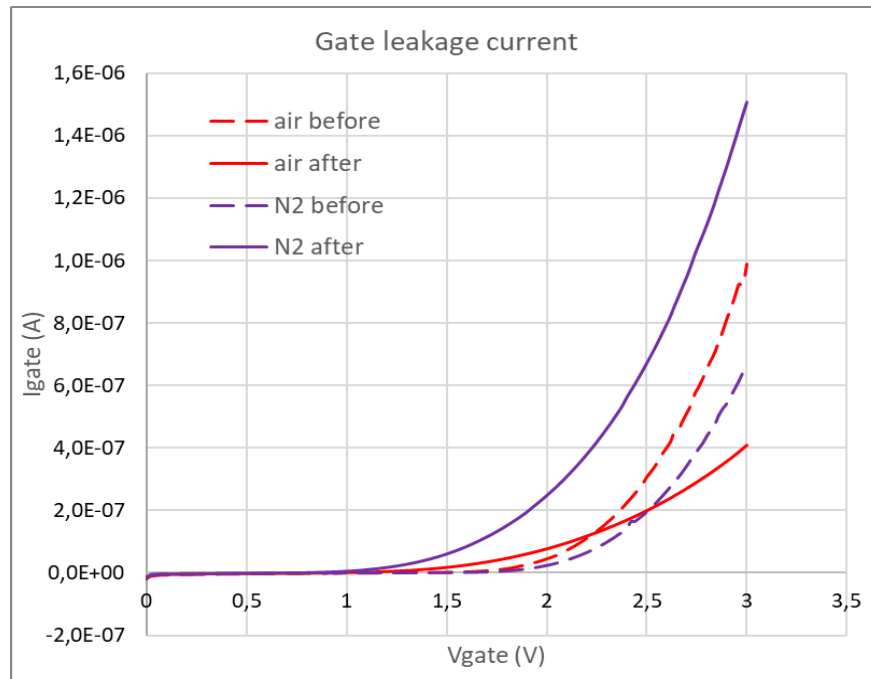


Figure 25. *The gate leakage current in transistor 9 before and after storing.*

Based on these results, there is some changes happening in the semiconductor layer while storing in different gases. When applying a negative voltage to the transistors stored in nitrogen, the off-current goes down. This points to doping in the material, which could be caused by oxygen defects in the semiconductor. Turn off would probably happen if a sufficient negative voltage was applied to the gate. However, because the high negative voltage might break the transistor, this could not be tried. To study these changes, the density of states in the interface should be measured.

6.5 Density of interface states

The changes happening in the density of interface states are likely the explanation to the changes happening when storing the transistors in different gases. The materials are not fully stabilized, but flow between materials can happen and a change in the density of interface states can occur. Because only the first few monolayers of the semiconductor are important to the operation of the device, as explained in the theory part, it is meaningful to focus on the interface states. To see this effect, the changes in the density of interface states should be measured.

The density of interface states can be measured in multiple ways, but methods for metal oxide semiconductors are not too common. An attempt was made to measure it with a Matlab code based on the conductance method [119], but the physics of the method are for silicon based transistors. A method developed for TFTs was found [120]. The new method was suitable, because it does not require characterization in different temperatures, which was not possible with the available equipment.

The new method is based on C-V measurements done at multiple frequencies. The series resistance is extracted from impedance measurements done at different frequencies with an LCR-meter. As the oxide capacitance is known, the capacitances of localized and free states are calculated using the equivalent circuits shown in Figure 26.

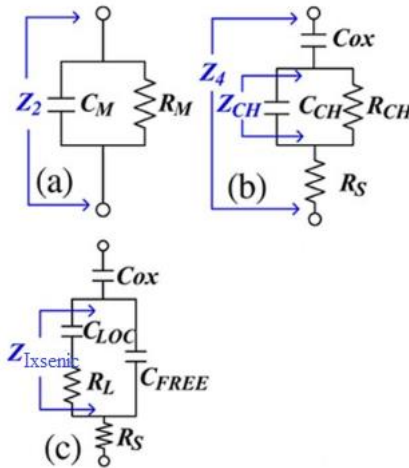


Figure 26. a) The Z_2 is the impedance measured with the LCR-meter, which consists of capacitance and resistance. b) The measured impedance can be split to the oxide capacitance C_{ox} , series resistance R_s and the impedance from the channel, which consists of capacitance and resistance. c) The capacitance in the channel can be divided to capacitance from localized states and free states. Modified from [120]

The impedances of Figure 26 (a), (b) and (c) are equal, but divided into different parts. In Figure 26(a) is the measured impedance from the LCR-meter, which sees a capacitance and a resistance component. In Figure 26(b) the series resistance and the oxide capacitance are split from the impedance in the channel. In Figure 26(c) the impedance in the channel is divided into capacitance caused by local and free states. The impedance Z_2 from gate to source was measured with an LCR-meter and the capacitance from gate to source was measured with the Keysight semiconductor device analyzer. An example of a measured C-V curve can be seen in Figure 27.

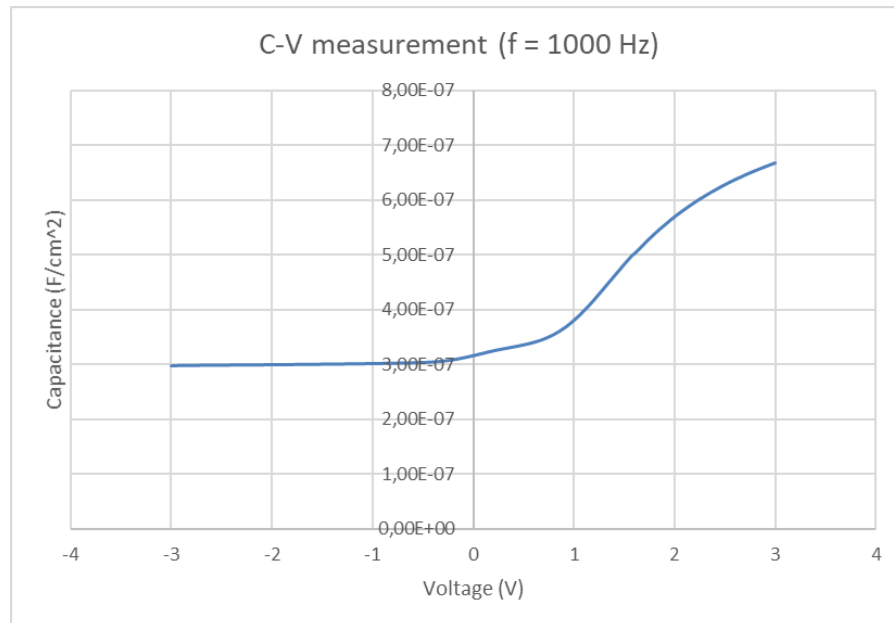


Figure 27. A measured C-V curve from gate to source with 1000 Hz frequency.

To complete the calculations a Matlab code was designed and written with help from Rohan Paul Binoy from Ohio State University, in Columbus, Ohio USA, advised by Prof. Paul R. Berger. This code can be seen in Appendix A. The C-V curves, such as in Figure 27, were measured in three different frequencies which were used in the operation of the code as well as the LCR-meter measurement of the impedance. The development of the code was not completed, because there was not enough time for it. Therefore, the density of interface states of the transistors was not extracted during this work.

6.6 Reliability of the results

The calculated values for mobility, threshold voltage and on-off current should be considered critically to ensure they do not give a faulty assessment of the operation of the transistors. On-off current is straightforward and easily extracted, but threshold voltage and mobility should be looked at more closely.

The values for threshold voltage and mobility are extracted from the square root of the transfer curve. An example of the curve can be seen in Figure 28. The threshold voltage could be extracted from the transfer curve itself, but the square root gives a somewhat more linear curve, which is easier to extrapolate for the threshold voltage. The curve is very close to linear and does not change the slope much, which means the threshold voltage is more precise as discussed before in Section 3.2.

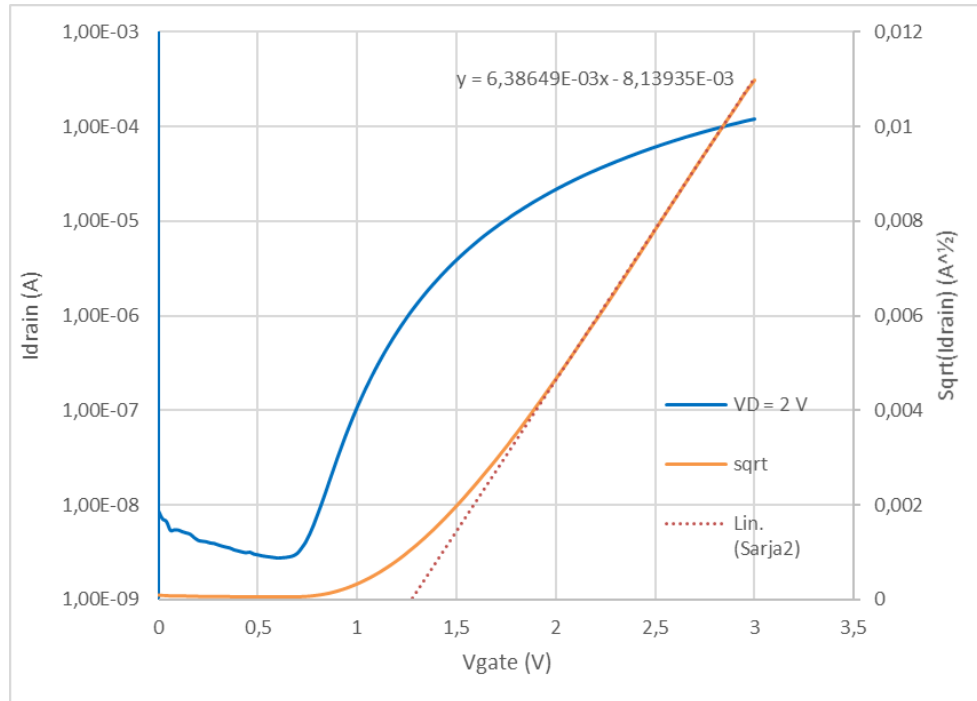


Figure 28. The transfer curve of a transistor and the square root of that curve, which is used to extract the threshold voltage and the charge carrier mobility of the transistor.

The square root curve is used to extract the mobility as well. The slope of the curve is part of the equation, which means it should be as linear as possible. To assess the uncertainty of the rightness of the mobility value, a reliability factor, r , can be calculated [80]:

$$r_{sat} = \left(\frac{\sqrt{|I_{SD}|^{max}} - \sqrt{|I_{SD}^0|}}{|V_G|^{max}} \right)^2 \bigg/ \left(\frac{\partial \sqrt{|I_{SD}|}}{\partial V_G} \right)^2_{claimed} \quad (9)$$

where $|I_{SD}|^{max}$ is the maximum drain to source current measured at the maximum gate voltage $|V_G|^{max}$ and $|I_{SD}^0|$ is the drain to source current at 0 gate voltage.

When using Equation 8 to calculate the reliability factor for the transistor, which is shown in Figure 27, the result is $r = 0,32$. This can be used to calculate the effective mobility for the transistor [80]:

$$\mu_{eff} = r \times \mu_{claimed} \quad (10)$$

where $\mu_{claimed}$ is the mobility extracted from the square root of the transfer curve. The extracted mobility from the transistor in Figure 27 is $9,99 \text{ cm}^2/\text{Vs}$, which makes the effective mobility, according to Equation 10 calculation, $3,23 \text{ cm}^2/\text{Vs}$. The effective mobility is lower than what is extracted from the curve, but it stays in the same order of magnitude.

The difference of properties between transistors in the same sample as well as between different samples was addressed in Table 5, where the mean values and standard deviations for those values were calculated for transistors in one sample, and two samples made in the same batch of samples. The results showed some difference in the values, but the differences were small enough for the results to still be meaningful.

There are many factors causing differences during the processing of the transistors. The evaporation of the electrodes was done using shadow masks, which were assembled on top of the samples by hand. Some of the masks were also not completely level, which caused some variations in the thickness of the electrodes especially on the edges of the sample.

The equipment used in the anodization was also prone to some changes. The sample was connected to the voltage source using an alligator clip and the sample was lowered into the solution by hand. This allows some room for variation. However, because the same reaction was done multiple times, the result of the reaction could be compared to reactions done before and unsuccessful anodizations could be filtered out.

The spin-coating of the semiconductor was done with a program in the device, which stays the same every time. However, when the annealing is done on the hotplate, the temperature of the hotplate was not the same in every part of the plate, plus the gap between the sample and the hotplate could be altered by some residual dirt that would temper the thermal conductivity from the hotplate to the sample with an intervening air gap. The temperature was measured with an infrared thermometer, and the samples were placed on the spots with most precise temperature, but there is possibility for changes.

When evaporating the source and drain electrodes, the positioning of the shadow masks was again done by hand. The position of the channel might change a little because of the positioning of the mask. If the mask was not put on the sample carefully, it could also scratch the surface of the semiconductor material. These aspects were considered while positioning the mask, so their effect could be minimized.

Considering all the aspects listed above, the results from the transistors were good enough to compare different samples to each other. Also, the effective mobility calculated with the reliability factor can be compared to values in the literature.

7. CONCLUSIONS

The purpose of this work was to test if Ixsenic could be used in a staggered bottom gate-top contact transistor structure with aluminum electrodes and anodized aluminum oxide gate insulator. Then the characterization of the transistor would be done more precisely or the semiconductor printability with inkjet could be tested. Because of results from the transistors, the further characterization of the transistor was chosen.

The best processing parameters for the transistors are collected in Table 6. The results from the characterization of the transistors are collected in Table 7.

Table 6. The optimized processing parameters for transistor processing.

Electrode evaporation	Anodization	Semiconductor deposition	Semiconductor annealing
Deposition rate: 3 Å/s	Solution: 0,01 mol/dm ³ citric acid	Spinning speed: 6000 rpm	UV-curing time: 300 s
Gate electrode thickness: 100 nm	Voltage: 5 V	Spinning dura- tion: 30 s	Annealing time: 3 h
Source and drain electrode thick- ness: 50 nm	Duration: 30 min		

Table 7. Results from the transistor characterization with 3 V gate voltage and 2 V drain voltage. The mobility values have been corrected with the reliability factor.

mobility (cm ² /Vs)	on-off ra- tio	Gate leakage current (μA)	Threshold voltage (V)	Subthreshold swing (V/dec)
1-3	10 ⁴	0,7-3	0,9-1,4	0,2-0,3

The mobility is on the typical range for oxide semiconductors if comparing to Table 1. The on-off ratio is large enough for the transistors to be used in circuits. The subthreshold swing is in the typical range for oxide semiconductors as well. The value of gate leakage current is high compared to other metal oxide transistors, but this could be improved by trying other aluminum oxide deposition methods such as ALD.

There are two pressing issues with the transistors made in this work. First, the annealing temperature of the semiconductor is relatively high, 350°C, which limits the use of flexible substrates. Second, the transistors are not stable, but there are notable changes in their operation after two weeks and the changes are dependent on the gas the transistors are stored in.

For the transistors to be processable on flexible substrates, some alternative annealing techniques should be studied to lower the processing temperature. The issue with the stability of the transistors was studied a bit further in this work by trying to see the change in interface states that happens in the devices. There seems to be doping in the transistors stored in nitrogen, which could be caused by oxygen deficiencies. However, determining the density of interface states was not completed because of limited time. If the changes in the devices could be determined, a solution for the problem could be developed. For example, if there is flow between the insulator and semiconductor material, a protective barrier could be deposited between them to prevent the flow.

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Appendix A: The matlab code for density of interface states characterization

Written by Rohan Paul Binoy

Import Data

```
V_gs = Cm1S1{:,1};
Cm1 = Cm1S1{:,2};
Cm2 = Cm2S1{:,2};
Cm3 = Cm3S1{:,2};
Length = length(V_gs);
G = Rm{:,2};
R_m = [];
for i = 1:length(G)
    R_m(i) = 1/(G(i));
end

% %For testing purposes
% V_gs = V_gs(1:20);
% Cm1 = Cm1(1:20);
% Cm2 = Cm2(1:20);
% Cm3 = Cm3(1:20);
% R_m = R_m(1:20);
% Length = length(V_gs);
```

Set constants

```
Rs = 200;
Dm = [];
DOS = [];
V_gs_Max = max(V_gs);
fi_s = [];

Cch1 = [];
Rch1 = [];
aConstant1 = [];
bConstant1 = [];

Cch2 = [];
Rch2 = [];
aConstant2 = [];
bConstant2 = [];

Cch3 = [];
Rch3 = [];
aConstant3 = [];
bConstant3 = [];

%Constants
Cox = 2e-9;
Tm = 10e-9;
w = 700e-6;
L = 60e-6;
vfb = -2.9;
q = 1.602176634E-19;

%Angular frequency
```

```

f1 = 10000;
f2 = 100000;
f3 = 1000000;
w1 = 2 * pi * f1;
w2 = 2 * pi * f2;
w3 = 2 * pi * f3;

```

Calculate Dm, a, b, Cch, and Rch for w1, w2, and w3.

```

%w1
for i = 1:Length
    Dm(i) = D_m(w1, Cm1(i), R_m(i));
    aConstant1(i) = a(R_m(i), w1, Cm1(i), Dm(i), Rs);
    bConstant1(i) = b(Cm1(i), Dm(i));
    Cch1(i) = C_ch(bConstant1(i), Cox, aConstant1(i), w1);
    Rch1(i) = R_ch(w1, Cm1(i), Dm(i), Cox, Cch1(i));
end

%w2
for i = 1:Length
    Dm(i) = D_m(w2, Cm2(i), R_m(i));
    aConstant2(i) = a(R_m(i), w2, Cm2(i), Dm(i), Rs);
    bConstant2(i) = b(Cm2(i), Dm(i));
    Cch2(i) = C_ch(bConstant2(i), Cox, aConstant2(i), w2);
    Rch2(i) = R_ch(w2, Cm2(i), Dm(i), Cox, Cch2(i));
end

%w3
for i = 1:Length
    Dm(i) = D_m(w3, Cm3(i), R_m(i));
    aConstant3(i) = a(R_m(i), w3, Cm3(i), Dm(i), Rs);
    bConstant3(i) = b(Cm3(i), Dm(i));
    Cch3(i) = C_ch(bConstant3(i), Cox, aConstant3(i), w3);
    Rch3(i) = R_ch(w3, Cm3(i), Dm(i), Cox, Cch3(i));
end

Vgs = [];
for i = 1:Length
    Vgs(i) = V_gs(i);
end

%write to file
T = array2table([Vgs; Rch1; Cch1; Rch2; Cch2; Rch3; Cch3]');
T.Properties.VariableNames{'Var1'} = 'Vgs';
T.Properties.VariableNames{'Var2'} = 'Rch_w1';
T.Properties.VariableNames{'Var3'} = 'Cch_w1';
T.Properties.VariableNames{'Var4'} = 'Rch_w2';
T.Properties.VariableNames{'Var5'} = 'Cch_w2';
T.Properties.VariableNames{'Var6'} = 'Rch_w3';
T.Properties.VariableNames{'Var7'} = 'Cch_w3';
filename = 'Data1.xlsx';
writetable(T, filename, 'Sheet', 1);

```

Calculate Cloc, Cfree, and Cg

```

C_loc = [];
C_free = [];

```

```

C_g = [];

%Simultaneous equations
syms Cloc Cfree
for i = 1:Length
    eq1 = ((w1*w1)*(Cch1(i))*(Rch1(i)*Rch1(i))*(Cloc+Cfree)*(Cloc+Cfree-Cch1(i))-
(Cloc+Cfree))/((w1*w1)*(Cloc*Cloc)*Cfree*(1+(w1*w1)*(Cch1(i))*(Rch1(i)*Rch1(i))*(Cch1(i)
-Cfree)));
    eq2 = ((w2*w2)*(Cch2(i))*(Rch2(i)*Rch2(i))*(Cloc+Cfree)*(Cloc+Cfree-Cch2(i))-
(Cloc+Cfree))/((w2*w2)*(Cloc*Cloc)*Cfree*(1+(w2*w2)*(Cch2(i))*(Rch2(i)*Rch2(i))*(Cch2(i)
-Cfree)));
    eq3 = ((w3*w3)*(Cch3(i))*(Rch3(i)*Rch3(i))*(Cloc+Cfree)*(Cloc+Cfree-Cch3(i))-
(Cloc+Cfree))/((w3*w3)*(Cloc*Cloc)*Cfree*(1+(w3*w3)*(Cch3(i))*(Rch3(i)*Rch3(i))*(Cch3(i)
-Cfree)));
    S = solve(eq1 == eq2, eq2 == eq3, eq1 == eq3, "PrincipalValue", true);
    C_loc(i) = S.Cloc;
    C_free(i) = S.Cfree;
    C_g(i) = ((S.Cloc + S.Cfree) * Cox) / (S.Cloc + S.Cfree + Cox);
end

%Plotting Cloc, Cfree, and Cg
figure(1)
plot(Vgs, C_loc);
title("Cloc, Cfree, Cg");
hold on
plot(Vgs, C_free);
plot(Vgs, C_g);
hold off
legend("Cloc", "Cfree", "Cg");

%Writing Cloc, Cfree, and Cg to file
T = array2table([Vgs;C_loc;C_free;C_g]');
T.Properties.VariableNames{'Var1'} = 'Vgs';
T.Properties.VariableNames{'Var2'} = 'Cloc';
T.Properties.VariableNames{'Var3'} = 'Cfree';
T.Properties.VariableNames{'Var4'} = 'Cg';
filename = 'Data1.xlsx';
writetable(T, filename, 'Sheet', 2);

```

Density of states

```

%Density of states
for i = 1:Length-1
    DOS(i) = (C_loc(i + 1) - C_loc(i))/(q * q * W * L * Tm);
end

%Writing DOS to file
T = array2table([Vgs(1:Length - 1);DOS]');
T.Properties.VariableNames{'Var1'} = 'Vgs';
T.Properties.VariableNames{'Var2'} = 'DOS';
filename = 'Data1.xlsx';
writetable(T, filename, 'Sheet', 3);

```

fi(s)

```

%Determine values of Vgs which are greater than vfb
index = 0;

```

```

condition = true;
for i = 1:Length
    if vgs(i) > vfb && condition == true
        index = i;
        condition = false;
    end
end

%Calculate fi(s)
syms VGS
j = 1;
for i = index:Length
    funct = 1 - (C_g(i) / Cox);
    fi_s(j) = int(funct, VGS, [vfb, vgs(i)]);
    j = j + 1;
end

%Writing DOS-fi(s) to file
T = array2table([fi_s(1:length(fi_s) - 1);DOS(index:length(DOS))]');
T.Properties.VariableNames{'Var1'} = 'fi_s';
T.Properties.VariableNames{'Var2'} = 'DOS';
filename = 'Data1.xlsx';
writetable(T, filename, 'Sheet', 4);

%Plotting DOS-fi(s)
figure(2)
semilogy(fi_s(1:length(fi_s) - 1), DOS(index:length(DOS)));
title("DOS vs fi(s)")
xlabel("fi(s)")
ylabel("DOS")

```

a

```

function out = a(Rm,w,Cm,Dm,RS)
denominator = w * Cm * (1 + (Dm * Dm));
out = (Rm / denominator) - RS;
end

```

b

```

function out = b(Cm,Dm)
out = Cm * (1 + (Dm * Dm));
end

```

C_ch

```

function out = C_ch(b,Cox,a,w)
numerator = (b * Cox * Cox) - (b * b * Cox);
denominator = (((a * a * b * b * w * w) + 1) * Cox * Cox) - (2 * b * Cox) + (b * b);
out = numerator / denominator;
end

```

D_m

```
function out = D_m(w,Cm,Rm)
out = 1/(w * Cm * Rm);
end
```

R_ch

```
function out = R_ch(w,C_m,D_m,C_ox,C_ch)
numerator = C_m * (1 + (D_m * D_m)) - C_ox;
denominator = ((w * w) * (C_ch * C_ch) * C_ox) - ((w * w) * C_ch * C_m * (1 + (D_m *
D_m)) * (C_ch + C_ox));
out = sqrt(numerator / denominator);
end
```

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