Tampere University

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DESIGN AND CONSTRUCTION OF AN INTERFACE BOARD FOR A HARDWARE-IN-THE-LOOP (HIL) SYSTEM

Laboratory of Power Electronics
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ABSTRACT

Saana Kaario: Design and construction of an interface board for a hardware-in-the-loop (HIL) system
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Real-time simulators are commonly used in contemporary research in the field of power electronics because of their ultimate versatility. With these real-time simulators, it is possible to study the control logic of the real controller equipment and its effect on the emulated power electronic system. Often such a hardware-in-the-loop (HIL) simulator device requires a user interface board to connect the hardware components to enable the transmission of signals between the devices as desired.

This work introduces the reader to circuit board design where the finished circuit board functions as the interface board of the aforementioned simulator system. The purpose of this work is to enable the use of a hardware-in-the-loop simulator for the control of a three-phase three-level neutral-point-clamped (NPC) inverter by designing a user interface board to connect the simulator components. The thesis first introduces the basics of hardware-in-the-loop simulation and the hardware and their internal operating methods used in the simulator system.

The bachelor's thesis presents the circuit board design process both in general and in the form of the printed circuit board (PCB) designed during the thesis. The PCB design process is described with the help of the design software Altium Designer used during the process. Details of the design and design choices made during the process are presented in detail to illustrate the progress of the process.

Keywords: PCB, design process, hardware-in-the-loop, simulation, NPC inverter, field programmable gate array (FPGA), Altium Designer

PREFACE

I would like to thank my supervisor Dr Petros Karamanakos for giving me this opportunity to learn something completely new and trusting my ability to complete the given task. Thank you for being patient and understanding. In addition, I would like to thank M. Sc Eyke Liegmann from the Technical University of Munich about the technical support given in the design process and verification of the boards. Finally, I would like to thank B. Sc Thomas Kreppel. Access to his thesis provided me a reference during the thesis project by helping me to understand the overall flow of the design process a lot better.

Tampere, 14th of April 2020

Saana Kaario

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LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

AC	Alternating current
AD	Analog-to-digital
ADC	Analog-to-digital converter
ARM	Advanced RISC machine
DC	Direct current
DUT	Device under testing
EMI	Electromagnetic interference
FMC	FPGA-Mezzanine Card
FPGA	Field programmable gate array
HDL	Hardware descriptive language
HIL	Hardware-in-the-loop
HPC	High-pin-count
HVDC	High-voltage-direct-current
I/O	Input / output
LPC	Low-pin-count
LVDC	Low-voltage differential signalling
MPSoC	Multi-processor-system-on-chip
MSB	Most significant bit
Msps	Mega samples per second
NPC	Neutral-point-clamped (inverter)
PCB	Printed circuit board
PWM	Pulse-width-modulation
SAR	Successive approximation register
SMC	Surface-mounted component
SoC	System-on-chip
TUT	Tampere University of Technology

1. INTRODUCTION

Power electronic converters are gradually becoming an essential part of a modern electrical system. The converters are utilized, for example, in electric motor drive applications and to connect renewable energy technologies, such as solar panels, to the power grid. One of the biggest challenges in converter utilization is to optimize energy efficiency and high quality. Advanced converter control logic methods can significantly improve the efficiency of the system. Control logic research and development of new methods are therefore an essential part of contemporary research in power electronics. To facilitate such research, equipment that simulates the system in real time can be employed. The so-called, hardware-in-the-loop (HIL) approach reduces the time required for development and enables safe testing of the control logic.

Simulator hardware is typically not developed for a specific task in mind, but to provide a multi-functional basis for varying applications. The simulator system often requires a separate piece of hardware to provide a signal connection and additional functions between the simulator hardware setup. The purpose of this bachelor's thesis is to familiarize the reader with the design process of an interface board developed during the thesis. This thesis describes the process for the design of a circuit board required for HIL testing of power electronic systems.

The thesis is structured as follows. In Chapter 2, the reader is introduced to the motivation of the design and construction of the circuit board and the eventual use of the circuit board. The chapter clarifies the ultimate purpose of the circuit board. Furthermore, the simulator setup to be connected via the interface board and the main features of the simulator hardware are introduced. Understanding the operating principles of the simulator hardware is the basis for understanding the entire simulator system, as the hardware ultimately defines the functions to be implemented on the interface board.

Chapter 3 presents an overview of the circuit board design process, focusing on the design software and methods used in this thesis. This way, understanding of the progress of the process is achieved.

Chapter 4 describes the choices made during the design and introduces the functionalities and the components to be implemented on the circuit board.

Finally, the outcome and summary of the design process are discussed in Chapter 5. Tips for further development of the circuit board are provided.

2. MOTIVATION AND INTRODUCTION TO USED HARDWARE

The motivation of the design project is to implement a completely new HIL-simulator system for a three-phase, three-level neutral-point-clamped (NPC) converter-based power electronic system. In order to provide a functioning simulator setup, an interface board must be introduced to the system. The goal of this thesis is to describe the design process and development of the interface board between control hardware and inverter emulator. More specifically, this thesis focuses on the design process of the interface board between the platform used to emulate the power electronic system, namely, the Plexim RT-Box, and the control platform, i.e., Trenz TEBF0808.

2.1 Introduction to HIL-simulation

HIL-simulation is one type of real-time simulation. In HIL-simulation the behaviour of some parts of real-world systems is emulated in real time. To give an example, real controller hardware is connected to a system that only emulates the controllable system i.e. a motor. The simulator hardware receives real control signals from the controller and emulates how the motor would react to the signals. The simulator sends similar signals as the real motor would send to the controller, which in turn "thinks" that it's controlling a real motor. [1] Figure 1 below presents the main difference between traditional testing and HIL-simulation.

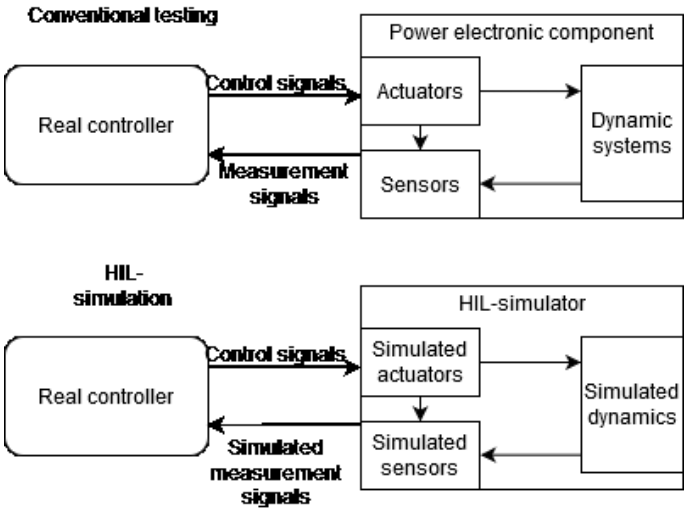

Figure 1. *The basic idea of HIL-simulation compared to conventional testing, (modified from source [2])*

HIL-simulation is usually embedded in the testing of very expensive and high-power components. It is widely utilized in the industry and research for example in safe and reliable testing of control hardware of electrical drives [3]. In the field of power electronics, the power plants that the devices under testing (DUTs) control usually consist of complex machines such as cranes and high-voltage converters.

2.1.1 Benefits of HIL-simulation

HIL-simulation is used particularly when modelling and developing the control logic functions during faults and error situations. While designing the control logic, it is important to understand and be able to regulate the operation of the controller during fault conditions so that the end-product does not pose a potential risk to humans when introduced to the market. Often situations, where the controllable hardware works in an abnormal way, are challenging to test. [4] Hence, HIL-simulation can provide a safe way to verify the correct functionality of both components and systems, thus avoiding potentially dangerous real-world experiments.

In many cases, the electrical drives are very expensive and if their performance cannot be predicted, running tests may create potentially hazardous situations for the testers involved. Large machines or machines operating with high voltages can threaten human lives when tested during the design process. The HIL system can be utilized to intentionally drive test simulations (e.g. short-circuits) that would cause grave damage or completely destroy the real hardware without posing any real risk to the tester. [3] These tests and their following results provide valuable information on how to control the hardware at the time of the error. For example, the tests may reveal information about what kind of signals the hardware under control sends just before the

error situation. Using this knowledge and predicting the errors in advance can be used to minimize the resulting damage.

It is advisable to introduce the HIL-simulation into the design process at a very early stage, thus making the most of it. Compared to traditional testing, HIL-simulation enables a cheap way of testing products without producing or building prototypes and therefore betters the quality of the final products. The possibility of simulation speeds up the design process since after each change to the control logic it is possible to test the effect on the operation of the controlled equipment in all operational situations. [1] The tests can be automated, allowing every design change to be tested rapidly and to gain immediate information about every choice made in the design process. Since it's possible to notice the malfunctioning of the control logic already during the design process, HIL-simulation brings significant savings in the development stage.

One of the biggest benefits of real-time simulation, including HIL simulation, is the speed of executing the simulation. The conventional simulation within the software can take several minutes, even if the modelling period is only a few seconds. Real-time simulation, by its name, takes place at the same pace as the real hardware system would work. The system behaviour is simulated in such a high ratio (in a matter of a few microseconds) that it emulates the behaviour of the actual system.

HIL-simulation equipment is quite expensive as the used processors are optimized for extremely heavy computing power. Those processors often house reprogrammable logic circuits to utilize the simulator in the development of almost any hardware. The functionality of the simulator can be changed by only reprogramming the logic circuit. Therefore, the same simulator hardware is applicable in multiple totally different setups, thus bringing more economical value and versatility to the simulator equipment. In the long run, the economic benefits of HIL simulation are many times the investment in simulator equipment. To conclude, using HIL, the overall product development accelerates, the need for expensive and time-consuming field tests decreases and product quality and safety improve.

2.2 Three-Level, Three-Phase Neutral-Point-Clamped Inverter

Neutral-point-clamped (NPC) inverter, sometimes referred to as diode clamped inverter [5], was first introduced in 1981 by A. Nabae, I. Takahashi and H. Akagi [6]. NPC inverter is a voltage-fed inverter, whose core function is to transform direct current (DC) to three-phase alternating current (AC). Multilevel NPCs are mostly utilized in high- to medium-voltage applications such as medium-voltage motor drives, high-voltage-direct-current (HVDC) applications and renewable energy applications [7].

Figure 2 presents the topology of the 3-level 3-phase NPC inverter. As seen in Figure 2, the power stage of the inverter consists of a DC source, 2 DC -side capacitors, 12 semiconductor controllable switches with anti-parallel diodes and 6 clamping diodes.

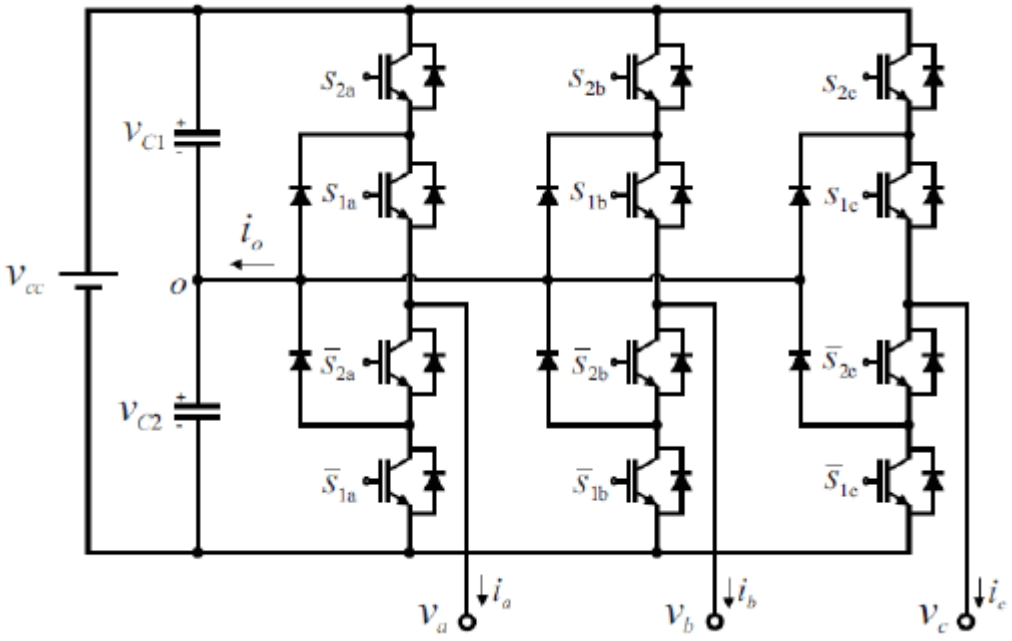

Figure 2. *The power stage of 3-level 3-phase NPC inverter [8]*

The three-level inverter, by its name, achieves three separate voltage levels: the positive voltage of the DC source, the negative voltage of the DC source and a third neutral point valued $\frac{V_{DC}+(-V_{DC})}{2}\ V$. Figure 2 presents the neutral point denoted with "*O*". If a neutral point is used as a reference voltage level, i.e. its voltage is grounded at $0\ V$, the two other voltage levels in use are $\frac{V_{DC}}{2}\ V$ and $\frac{-V_{DC}}{2}\ V$ [6].

In order to operate the inverter safely and prevent control-induced short circuits, only two switches are turned on simultaneously in one inverter leg. To produce a $\frac{V_{DC}}{2}\ V$, S_{2a} and S_{1a} are turned on, for neutral point $0\ V$, S_{1a} and $\bar{S}_{2a}$ are activated and for $\frac{-V_{DC}}{2}\ V$, $\bar{S}_{2a}$and $\bar{S}_{1a}$ are turned on simultaneously. These switching signals are generated by the controller of the inverter.

In order to determine the switching state, the inverter outputs the phase current values to the controller. The circuit is a three-phase system in star connection, therefore two phase currents are enough to execute the control logic.

Compared to a conventional two-level inverter, the three-level inverter has several advantages. The main benefits are reduced harmonic distortion in the output current and voltage and diminished problems associated with electromagnetic compatibility. A three-level inverter can operate at both its base frequency and high frequency. As with other inverters, lower frequency

operation reduces switching losses and thus improves the total efficiency of the inverter. [8] Furthermore, multilevel inverters can safely operate at higher DC voltages, since the circuit components are exposed to a voltage half or less of two-level inverter ones [6].

One disadvantage of a three-level inverter can be considered the larger number of components. The total cost of the inverter increases as the component number rises and simultaneously the unit has more parts prone to breaking. [8] In addition, a more complex controller is required due to the higher number of switches. As a result, the control logic for the three-level inverter is much more challenging to implement than that for a conventional two-level inverter.

2.3 Plexim RT-Box

RT-Box is a cutting edge real-time simulation hardware unit developed by Plexim GmbH. The RT-Box is specifically designed to be used as a platform for power electronic applications and it can be utilized in both HIL-simulation and rapid control prototyping. When used in HIL simulation, the RT-Box emulates the power plant itself, for example, a solar panel inverter or AC drive system. In rapid control prototyping, the RT-Box is used as the control platform. [9] RT-Box can be used as a standalone system as well as multiple boxes linked together to form a larger platform with an increased number of input/output (I/O) ports and shorter simulation time steps [10]. The overview of one unit is presented as a block diagram in Figure 3.

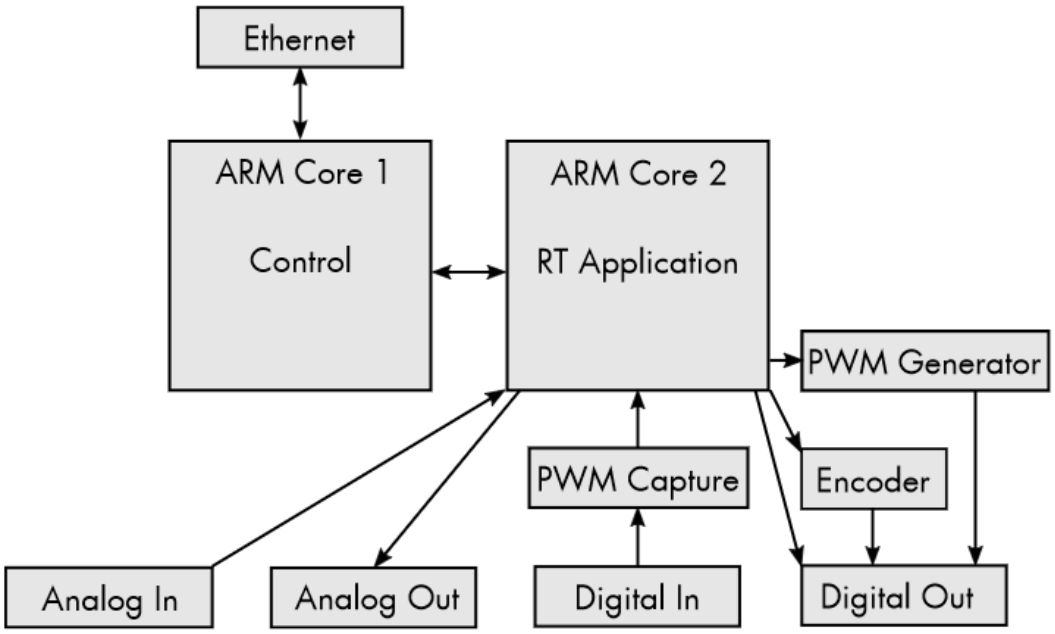

Figure 3. *Overview to RT-Box operation [10]*

The RT-Box houses the Xilinx Zynq Z-7030 system-on-chip (SoC) processor with a clock rate of 1GHz. The SoC module consists of a field programmable gate array (FPGA) and two advanced RISC Machine (ARM) cores. The first ARM Core communicates between the RT-Box and the software that controls its operation, PLECS. As can be seen from Figure 3 the second ARM Core focuses on the real-time emulator activity itself and deals with the connections to external devices. [10]

The RT-Box has 32 analog I/Os and 64 digital I/Os, of which 7 analog outputs and 14 digital inputs are utilized in this thesis. Analog outputs provide the simulated inverter output current measurement data to the controller and voltage measurements between one inverter leg and the neutral point for monitoring the switch state. The measurement data of the output currents from the RT-Box is transmitted as voltage signals to the controller. As the controller used in this thesis is not able to directly receive analog signals the analog-to-digital conversion must first be implemented with external hardware.

The RT-Box design enables the selection of the voltage ranges to be used in its analog output ports with the help of PLECS software. The voltage ranges available are presented in Table 1. All voltage outputs can be defined with a software to work as either differential or single-ended outputs. All voltage levels are protected inside the RT-Box.

Table 1. *RT-Box analog output voltage ranges [10]*

Available voltage ranges
0…5 V
-5…5 V
0…10 V
-10…10 V

To ensure excellent emulator performance the simulated measurement data should be transferred to the controller with the highest possible accuracy. Therefore, the resolution of the signal should be as high as possible. The voltage range is selected to be as small as possible and not interfere with other tasks. In this case, the voltage range of 0 ... 5 V is suitable for the components used in the external hardware. According to the RT-Box user manual, the analog outputs of the RT-Box have a resolution of 16 bits. Thus, the resolution of the output signal with the selected voltage range is calculated as follows: $\frac{range}{2^{bit\ amount}} = \frac{5\ V}{2^{16}\ bit} = 0.0763\ {}^{mV}/_{bit}$. The resolution of the output signal is very high. The maximum sampling frequency of the analog outputs of the RT-Box is 2 Megasamples per second ($Msps$) i.e. 2 MHz. The value of the output signal can thus be changed every 0.5 μs.

The controller under testing provides the switching signals of the inverter as digital signals to the RT-Box digital inputs. The input ports are able to read control signals with speed up to 10 ns. As a result, the switching state is simulated in a few microseconds [11]. The simulated voltages and currents resulted from the applied control commands are measured and fed back to the addressed analog outputs of the RT-Box. This interaction and exchange of signals occur so fast, without any latency inside the RT-Box, that the DUT “sees” the emulator as a real controllable inverter.

In this thesis, the RT-Box emulates the three-level NPC inverter introduced in Section 2.2. The actual emulator operation can be modelled using the PLECS software and the simulation blocks its library provides. This thesis does not cover the topic of modelling the emulator operation. For additional information about the use of PLECS software consider consulting the Plexim website and PLECS software manual [12].

2.4 Trenz Electronics TEBF0808

The TEBF0808 is a carrier board designed by Trenz Electronic GmbH. The board is able to house one of the two Xilinx Zynq Ultrascale+ multi-processor-system-on-chip (MPSoC) modules (TE0808 and TE0803) at a time and the components and connectors related to the module. TEBF0808 board is commonly used to test other Zynq Ultrascale products and widely utilized in research use [13]. A 3D overview of the carrier board is presented in Figure 4. Figure 5 presents all of the functions of the hardware.

Figure 4. *Overview of Trenz TEBF0808 carrier board with red circle encircling the connectors to which the MPSoC module should be placed (modified from source [14])*

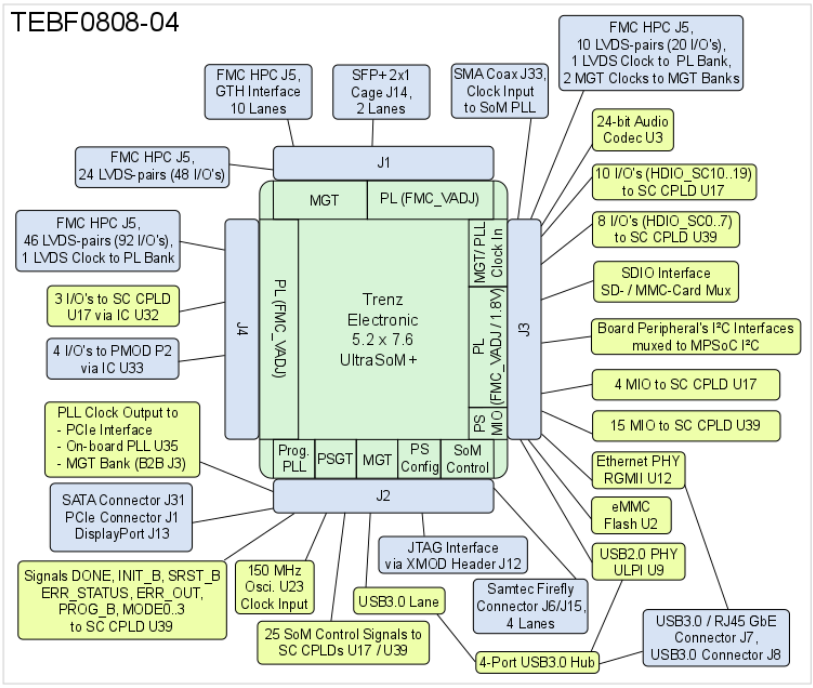

Figure 5. *Block diagram of TEBF0808 [13]*

The MPSoC unit, working as the heart of the carrier board, enables versatile usage of the TEBF0808. The unit houses 4 different processor units, in which perhaps the most important for this thesis is the FinFET+ field programmable gate array (FPGA) logic unit [15]. Multipurpose and reprogrammable processors ensure variable use for the baseboard. To guarantee that all processors and their multiple benefits are widely utilized, the carrier board includes several different connectors shown as blocks around the MPSoC in Figure 5. Versatile connectivity options contribute to the diverse usability of the board.

The hardware setup used in this thesis utilizes the TEBF0808 as the controller of the previously presented NPC inverter. The inputs of the controller are the simulated measurement AC currents coming from the RT-Box. The current measurement signals require an external analog-to-digital (AD) conversion since the TEBF0808 does not have any analog input ports for the incoming signals. The signals are transmitted to the controller as differential signals using the low-voltage differential signalling (LVDS) method discussed in more detail here [16, p. 36]. The carrier board uses the same LVDS standard also in routing the I/O signals from the connector to the FPGA banks [13].

As stated previously, the carrier board includes a number of different connectors. However, in this thesis, the most important connector on the board is the High-Pin-Count (HPC) FPGA-Mezzanine Card (FMC) -connector. The FMC-connector connects the FPGA processor unit and the to-be-designed interface board.

This presentation of the carrier board provides just a brief review of its main for reason of completeness. The interested reader is referred to [13] for a better understanding and in-depth description of the functionalities of the TEBF0808 board.

2.4.1 FMC-connector

The FMC-connector is a standardized connector module between a base board and an external mezzanine-interface board. The standardized connector (ANSI / VITA 57.1 [17]) has been developed to work between the FPGA and the external interface card to ease the reuse of the FPGA unit and clarify the transfer of data between the boards. With a standardized connector, external interface cards can be changed according to the needs of the current research, and by reprogramming the FPGA unit, it is possible to utilize the carrier board for completely different tasks. This versatility increases the use of the carrier board and reduces the cost of hardware since only the connected interface board must be changed in the system instead of redesigning the whole processing unit.

Figure 6 presents two interconnectable FMC-connectors. The carrier board houses one connector and the mezzanine interface card is connected to the top of the carrier board with the FMC-connector.

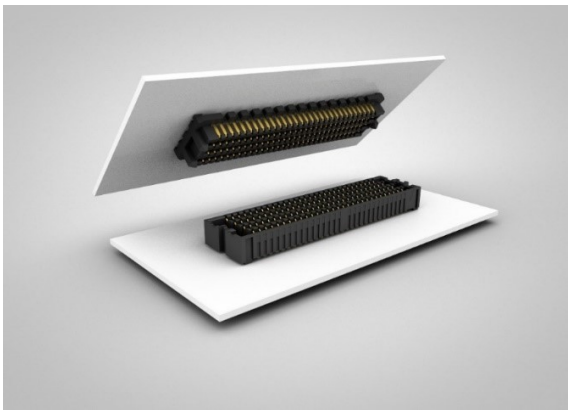

Figure 6. *Two interconnecting FMC-connectors [18]*

Perhaps the most significant benefit of the FMC-connector is its large number of I/O pins. Each transmittable signal has an addressed signal path directly from the mezzanine board to the FPGA and vice versa. There are no structural limitations in data transfer (buses connecting peripheral units), as in traditional protocol standards, since the information between the boards can be transferred immediately. When I/O ports are directly connected to the FPGA, the circuit board designer does not require knowledge about the number of challenging signal transfer protocols and the specific requirements of each protocol [19]. Thus, the FMC standard is specifically designed to facilitate and speed up the design of connectable boards.

The FMC-connector is designed specifically for industrial applications. The module combines small exterior dimensions, a high number of connections, relatively low price and versatility. There are two different versions of connectors sharing the same external dimensions. High-pin-count -connectors have 400 pins, and low-pin count (LPC) -connectors 160 pins. The aforementioned connectors are fully compatible and interconnectable with each other. [20] The TEBF0808 carrier board includes an HPC-connector, but the interface board designed in this thesis is able to implement all of the board functions with a cheaper LPC-connector. The LPC-connectors interface either 68 single-ended signal buses or 34 differential signalling pairs. The remaining connector pins have functions like a clock signal bus, serial transceiver pair, and signal ground.

The FMC-standard specifies the functionalities of the module pin connections. The functions of the LPC-connector pins are presented in Appendix C. The table in Appendix C shows which module pin is connected to which of the functions of the FPGA (for example, a clock signal lane, a differential signalling lane). Using the table, the signals on the external interface board can be easily assigned to the respective function pin for the FPGA. All the pins support signal speeds up to 2 Gb/s.

Furthermore, the FMC-connector enables power to be supplied to the interface board from the carrier board. The ANSI / VITA 57.1. standard defines three power supply voltages that can be exchanged between the carrier board and interface board. The aforementioned voltages are 12 V, 3.3 V and one adjustable voltage level with a range of 0…3.3 V. The adjustable voltage level determines the logic level used by the FPGA for external signals and is selected to be 1.8 V in this thesis. In doing so, the logic level of all the output signals is set to this value [13]. In this thesis, all available power supply voltages are connected from the carrier board to the to-be-designed external interface board.

The final signal assignment of the FMC-connector is presented in the table in Appendix D. The table does not include e.g. ground connections but focuses on the signals transmitted.

2.5 Field Programmable Gate Array

An FPGA is a reprogrammable integrated digital microcircuit. FPGAs can be defined as an array or matrix of fully configurable logic blocks [21]. These logic blocks are connected to each other via a reprogrammable interconnection network [22]. FPGAs do not have any built-in functionalities when manufactured, but the designer has full power to program the desired application of the microcircuit. Its fully programmable structure virtually enables the implementation of any digital circuit functionality that the designer is able to program. FPGAs are widely utilized in embedded systems, prototyping and research for the ability to change the functionality with ease [23]. The outline of the FPGA architecture is presented in Figure 7.

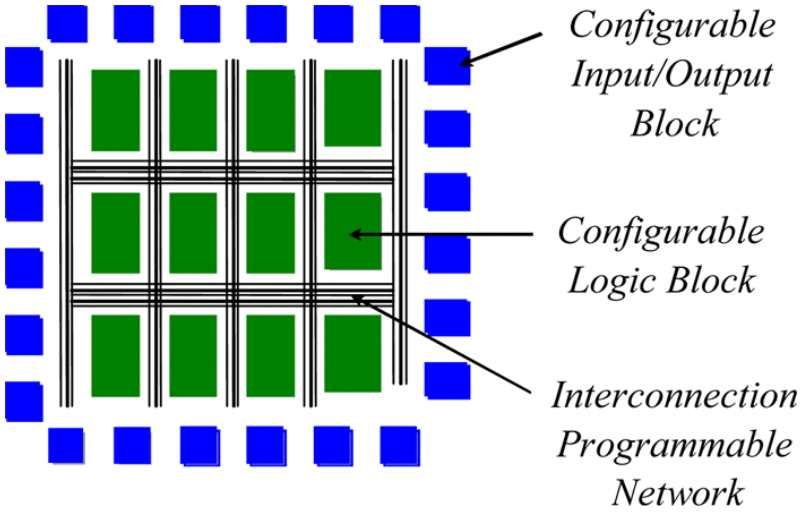

Figure 7.*Overview of basic FPGA architecture [22, p. 1825]*

The logic gates of the FPGA and their connections are usually programmed using hardware descriptive language (HDL) in which the two most common languages are VHDL and Verilog [22]. HDLs enable programming of generic logic blocks to complete certain combinatorial logic. These combinatorial blocks are then connected to each other with an interconnection network and to external devices using the I/O blocks in the network. In other words, by programming the FPGAs with HDL the user is fundamentally designing the architecture of an electrical circuit.

One of the main benefits of FPGAs is its unique structure. Individual processing tasks are completed in separate block sections in parallel. These processing tasks do not interfere with each other in any way, therefore making them autonomous. [21]

Understanding the operational logic and structure of the FPGA can be challenging if the reader is not familiar with microcircuits. If there is a need for additional basic information about the FPGAs, consider consulting, for example, this video [24]. In the sequel, the operation and architecture of the microcircuit will be demonstrated by means of illustration and at a fairly general level of understanding.

The hardware configuration used in the thesis houses FPGA units in both the RT-Box and the TEBF0808 board. The control logic and processing of measurement signals is completed with the FPGA in the TEBF0808. As stated before, the FPGA functionalities must be programmed in order to enable the testing and research use of the hardware in the simulator system. The programming of the microcircuits is out of the scope of this thesis and therefore not included.

3. INTRODUCTION TO PRINTED CIRCUIT BOARD DESIGN

The goal of this thesis is to design and construct the interface board for a new simulator system used in power electronic applications. As stated in the previous chapter, in order to connect the two simulator hardware components TEBF0808 and RT-Box an interface board is introduced to the setup. This interface board houses conducting copper routes, connectors and integrated circuits required to enable data flow between the two devices. This chapter is an introduction to a design process overflow of printed circuit boards (PCBs). Figure 8 presents an overview of the design process used in this thesis.

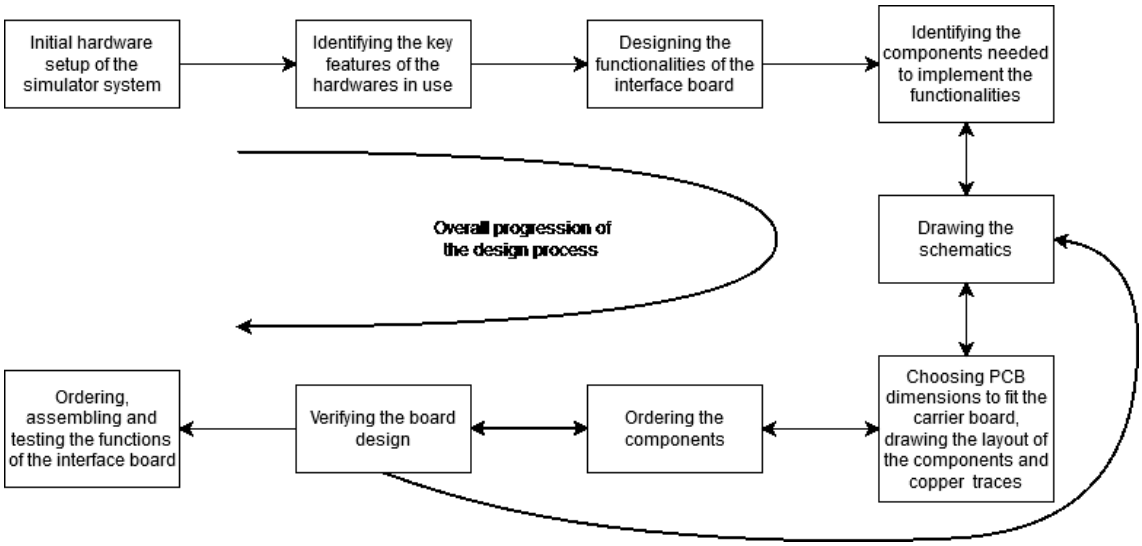

Figure 8. *The design process of the interface board*

From Figure 8 it can be seen that the design process is not completely linear, but adjustments to previous stages are made if necessary.

3.1 Starting the design process

In the first step of the design of the interface board, the hardware introduced in the previous chapter is studied. By studying hardware datasheets, it is possible to attain in-depth knowledge about the device features, for example, what signals it is able to receive, the I/O-properties of the device and the connectors available for use. When the hardware-specific limitations and special requirements are known, the next thing to consider is what the simulator setup has to achieve and what functions are used in the said operation. The planned functional operation of the simulator system, as well as the initial hardware setup, largely determines which functionalities should be implemented to the interface board in order to enable the desired simulator operation.

The purpose of this thesis is not to design an interface board completely from the beginning, but rather modify existing designs of an interface board by adapting them to the available equipment while considering the needs of the case study in question. The basis for this thesis is an interface board developed at the Technical University of Munich [16], the design files of which as well as [16] wherein the relevant design process is described were available during the course of the design project conducted in this thesis. A similar interface board between the Trenz TEBF0808 carrier board and an actual 3-phase NPC inverter was designed and implemented in [16]. The differences between the board in [16] and the to-be-developed in this thesis are practically related to the differences between the actual inverter used in the former, as compared with the system emulator considered here. Due to the similarity of the PCBs, it is completely unnecessary to start the design process from the beginning, but by utilizing the results and knowledge of the reference board and its design files, it is possible to significantly speed up the circuit board design process in this thesis.

After identifying the initial hardware setup and functionalities to be implemented, the most practical way to proceed with the design is by examining the reference board. The reference PCB is known to work on the setup, making it logical to start the selection of the components by examining the components used therein. Component datasheets contain for example descriptions of the operation of each component, detailed tables of component specifications and parameters, instructions for varying applications, as well as circuit board layout guidelines. By studying the datasheets, it is possible to attain knowledge of whether the components are suitable for use in the interface board to be designed in this thesis. Accordingly, for example, the operating voltages required, the connectivity possibilities of the components and the operation logic required for the system to be functional are known.

First, the active components, such as microcircuits, that perform the required functions in the interface board are selected. Subsequently, according to the application instructions of their datasheets, passive components, such as resistors, that enable the operation of the microcircuits are added to the design. In general, by changing some values and routings between the components, almost all of the components from [16] are suitable for the circuit board being designed in this thesis.

Subsequently, when the components are chosen, the next step is to draw a schematic design. This step is executed with the help of the Altium Designer PCB design software.

3.2 Altium Designer

Altium Designer is a computer-aided design software that is widely utilized by industry to enable comprehensive PCB design workflow. The ultimate benefit of Altium Designer is that only one software is needed for the whole PCB design process. Altium combines all the tools needed for the schematic design to tools used when finishing files needed for professional PCB manufacturing. Altium provides holistic documentation of the software on its website [25]. The documentation provides instructions for PCB design, from defining the design settings and constructing the layout of components to finalizing the circuit board. In this thesis, the documentation is used to get familiar with the fundamentals of circuit board design, to support the use of the software during the design process, and to assist in design choices [26].

Besides Altium documentation, general guidelines for PCB design, component layout and signal routing are available, for example, in [27] and [28]. Articles provide comprehensive advice on the circuit board layout process.

3.2.1 Schematic design

The following step in the design process after selecting the components is the schematic design of the circuit. All of the components and the signal paths (wires) between them are designed to the Altium Designer schematic design file using a computer. The electrical symbols of the components and, for example, voltage sources are added to the schematic file and the connections between the connectors and component pads are routed so that the schematic ultimately describes how the components are electrically connected to each other.

Altium includes component libraries, from which the components used in the design can be added to the schematics. If the desired component cannot be found from the Altium libraries, a retailer or manufacturer website may have provided a software-compatible schematic model of the component. Alternatively, another way to include a schematic symbol to the design is to determine the component dimensions, electrical properties, and pin configuration by using the design software itself. The aforementioned data and dimensions required for component modelling can be found in the component datasheets.

To facilitate the readability and troubleshooting of the schematic design the wiring should be kept as clean and neat as possible. The software provides an easy way to wire the connections between components while naming networks makes it significantly easier to understand the signal routes in the circuit. The components have unique designators that ease the assembly of the interface board when components are easily identifiable. Figure 9 presents the schematic picture of one component in the design. Additional components are wired to the microcircuit and power supplies and ground connections are presented.

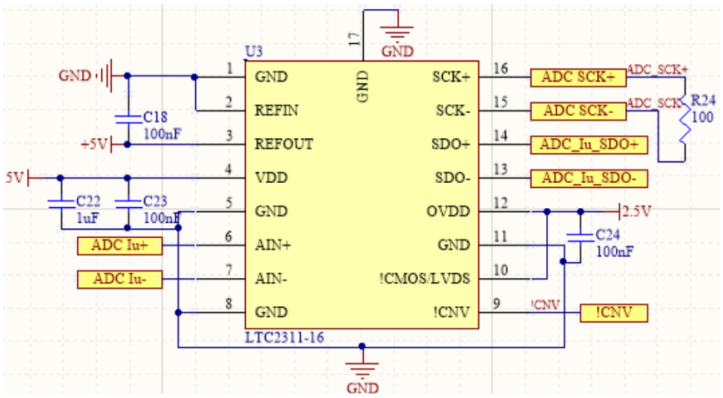

Figure 9. *Schematic picture of a component*

If necessary, the operation of the circuit board can be simulated with software developed for that purpose. For example, the values of the passive components can be determined by simulation if the microcircuit datasheet does not contain a recommended and tested value for them.

Schematic design figures of this thesis are presented in Appendix A. The design sheets are separated into functional blocks to increase the readability of the schematics. The main functions are presented in different sheets and the networks have designators to demonstrate connections between the sheets.

3.2.2 PCB layout design

When the schematic design is complete and the connections between the components are defined, the next step in the PCB design process is the design of the physical layout. This includes determining the dimensions and shape of the circuit board to be manufactured, the layout of the components on the PCB, and the routing of the signal paths defined in the schematics. Altium facilitates the design process so that the schematics can be directly transferred to the layout design editor when the schematic design is ready. In that way, in case some changes are made to the schematic design they can be updated directly into the layout editor. The software runs tests for detecting potential design errors, such as open circuits during the transition from schematics to the layout. Figure 10 presents the Altium Designer layout editor window with the final board design completed during this thesis.

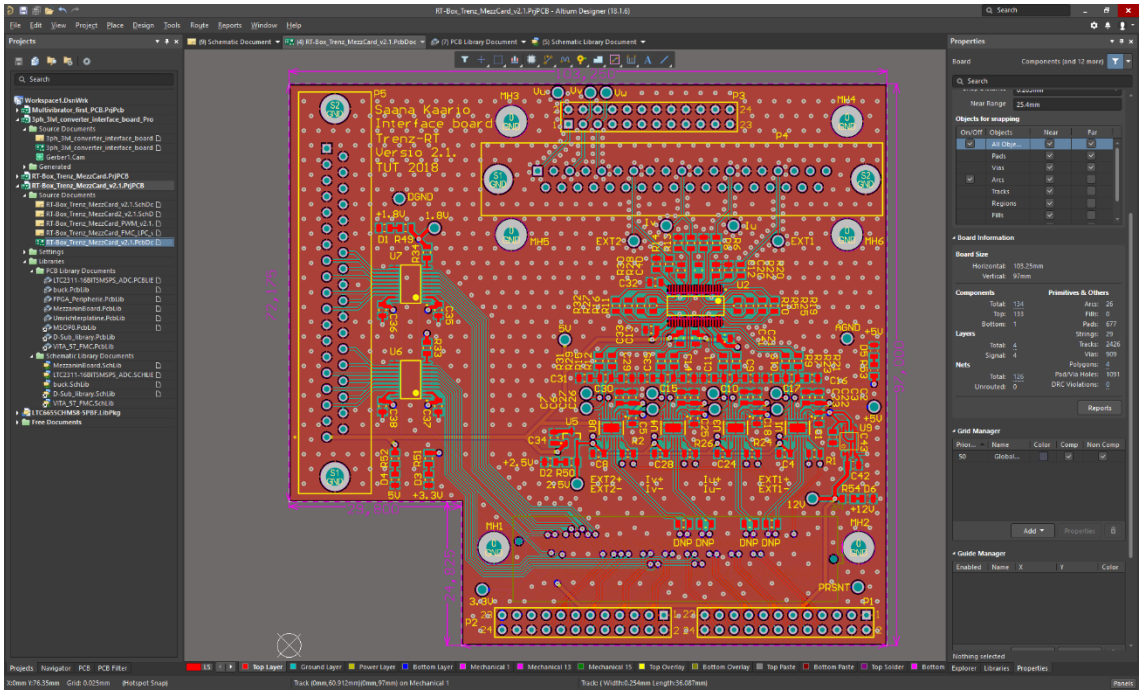

Figure 10. *Altium editor window for designing the layout with the designed board*

Before starting the layout design itself, it is very important to determine the layout settings and limitations of the design. If the to-be-designed PCB is going to be, for example, very small in size or multi-layered, it must be professionally manufactured to ensure the quality of the board. Every PCB manufacturer has their own design limitations that are determined by their manufacturing capabilities. These design limitations can be found from the website of the manufacturer and they should be strictly adhered to in PCB design. In this thesis, the interface board is to be ordered

from JCL PCB. The chosen manufacturer imposes restrictions on, for example, the minimum and maximum diameters of the holes to be drilled in the PCB, hole layering (only through-PCB vias are allowed) and the minimum width of the copper tracks [29]. Bearing these limitations in mind from the beginning of the design is practical, as this saves time and costs as the design progresses, avoiding unnecessary redesigns.

At the beginning of the layout design, all of the components in the schematic design appear in real-world size in the layout editor. The components are connected to each other by thin lines that have been created between the component pads to show their connections to be routed. Initially, the components are placed on the board in a way that the active components and required passive components are placed approximately according to the layout recommended by the datasheet. At this point, the dimensions of the components and the board space needed to house them are realized. The components should be placed on a circuit board so that the copper tracks to be routed between component pads are as straight and short as possible. Furthermore, the lines should not intersect if not necessary, since crossing tracks must be routed through the circuit board to a different layer using vias that increase impedance in the circuit. It is possible to change the component layout at a later stage if the routing poses challenges.

The next step in layout design is routing copper tracks according to the network of lines between component pads. The skilled layout of the components makes the routing process significantly easier, thus previous experience in PCB layout also speeds up the routing. Copper traces are interactively routed by Altium facilitating, for example, the tracing around components and snapping to the target pad. An illustration of a routed section of a circuit board is presented in Figure 11. The blue tracks on the board define the signal paths between the components.

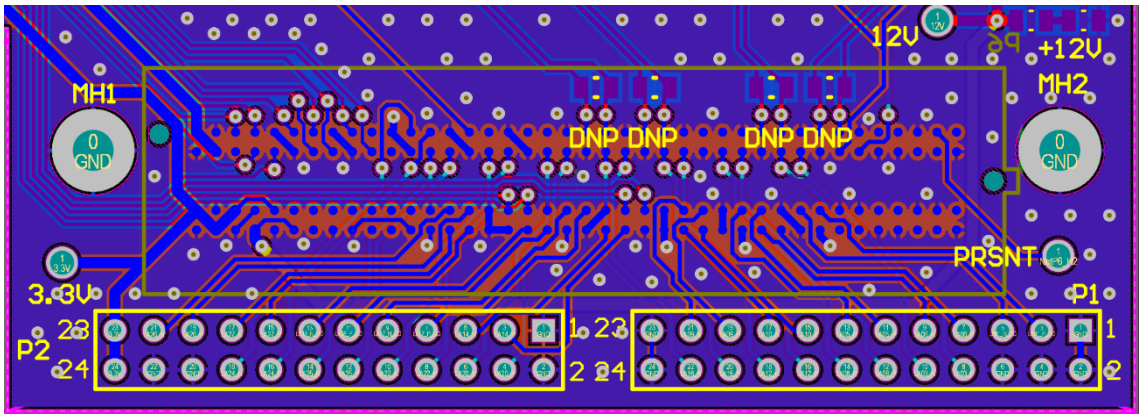

Figure 11. *Routed section of the interface board*

During the above-mentioned process, the component datasheets provide valuable information that should be taken into account in the layout design. The datasheets might present instructions for routing signal paths, as the components may have special restrictions, or they require noise-free areas on the PCB. To give an example, in general, it is better to route analog and digital signals as far apart as possible as digital signals are often noisy whereas analog signals are sensitive to interferences and noise. For instance, in order to ensure the desired function of the components, the routing of the clock signals may be subject to constraints so that the signals do not interfere with the operation of the component. Analog signals can also be protected against interferences by shielding. Using the shielding-method, Altium adds close-to-line vias on both sides alongside the analog signal tracks. In this way, the interference in the signal path is significantly reduced. [30]

Once the routing is complete, a large copper plane area is almost always added to the layout of the entire PCB area. The copper plane can be connected, for example, to ground potential, whereby the components always have a short connection to the ground plane, and the ground potential of all the PCB components is the same. Another benefit of the copper plane is its

extremely low impedance. In multi-layer circuit boards, copper planes can be placed on all layers. In this case, the layers must be connected to each other by the so-called via stitching-method, according to which a grid of vias is added to the copper plane area. The vias connect the copper planes evenly across the entire PCB and enable short return loops [30]. For more information on finalizing PCB design in Altium, see [31].

The final step in designing a circuit board before ordering the PCB is to verify the schematic design and layout. Interface board similarities allow the verifier to provide tips and suggestions for further development of the circuit board. During the design process of this thesis, the placement of additional connectors was modified, and a component for generating a voltage reference was added to the design.

Figure 12 presents the Altium-generated 3D-model (shown in two dimensions for visualization purposes) of the verified design. Some components are modelled only with their placings since they do not have a pre-made 3D-model in Altium.

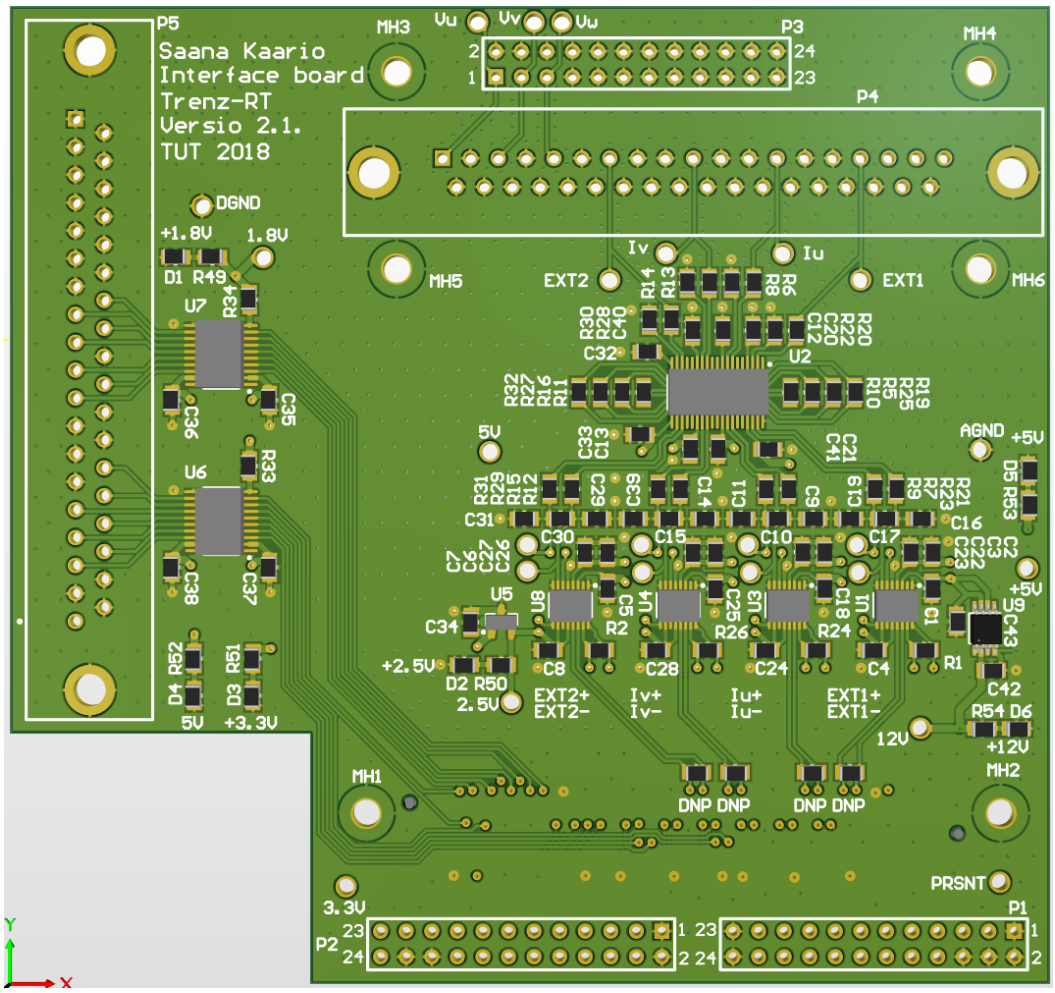

Figure 12. *3D-model of the final PCB design with most components on their place presented in 2D*

3.3 Assembly of printed circuit boards

Once the board design is complete and the design is verified, the PCB must be ordered and assembled. The design software exports industry-standard Gerber files that include all details of the design information required by the PCB manufacturer. If the circuit board design is very simple and contains only a few components, it can be manufactured by utilizing facilities that can be commonly found in a university. Instructions for such simple PCB manufacturing are provided in Finnish [32].

However, the number of layers on the circuit board is frequently more than just one or two. For example, the interface board designed in this thesis utilizes 4 conductive layers. Moreover, the routed tracks are very narrow, and the design requires extremely precise manufacturing not achievable with the manufacturing hardware available in the university laboratory. It is not possible to fabricate a multi-layer PCB without dedicated special tools, so commonly circuit boards are ordered from a manufacturer specialized in producing the PCB. The industrial manufacturing process of PCB is presented closely in [33].

Once the factory-made PCB and the components included in the design are available, the next step is the assembly of the PCB. Components are attached to the circuit board by soldering. Soldering is a method of creating an electrically conductive mechanical bond between the component pin and the conductive part of the circuit board by heating the tin compound. The component is first placed accurately on the PCB, after which the parts to be joined are heated simultaneously and a tin alloy is introduced into the joint. The solder melts between the circuit board and the component, and when the heat source is removed, the solder solidifies almost instantly thus creating the desired connection between the components. [34] The soldering can be roughly divided into two different types, according to the method and amount of the components to be soldered, namely, hand soldering and reflow soldering.

Traditionally, circuit board components have been relatively large in size (dimensions closer to centimetres). These through-hole components have long legs that are used when assembling the PCB. At the PCB manufacturing stage, holes for the component legs are drilled, and the components are assembled through the holes using the legs to hold them in the place and provide the connection. Such through-hole components, by their size, can be soldered easily by hand using a soldering iron for heating joints and tin alloy. In modern PCB design, the size of the assembled board is a really important feature. This implies large through-hole components are often undesirable in the circuit.

Nowadays, almost all components are surface-mount components (SMCs) with the greatest benefit being a considerably smaller component size (dimensions in millimetre size). For SMCs, it is not necessary to drill holes in the circuit board, but the components are soldered directly to the circuit board surface. The small size of the SMCs and generally their very large number in individual circuit boards affect the assembling process in a way that it is not possible or sensible in any way to attach the components one by one by soldering by hand. The method used to attach either a number of components or SMCs simultaneously is the reflow soldering.

The fundamental idea of the reflow soldering method is to add soldering paste to each joint before placing the component. The components are placed on the PCB and the entire circuit board is simultaneously heated in a reflow soldering oven. Thus, all of the joints can be connected at once diminishing the time required for soldering greatly.

Assembling of the circuit board is a follow-up step and was out of the scope of this thesis. This can be done by using, for example, a reflow soldering station. The reflow soldering process to be used in the assembly is described in-depth with illustrations in [16, p. 26-28].

The final step in the circuit board design process is to test the assembled PCB. The circuit board is tested for possible short and open circuits that would interfere with the desired operation of the PCB. These manufacturing flaws could connect components to an undesired operating

voltage, thus possibly destroying the component. A multimeter can be used to test the connections between parts of the circuit. All signal paths must be tested to ensure that all routed traces are connected, and all other connecting parts are isolated from said traces. The operation of the circuit board can also be tested by attaching a voltage source to the circuit and measuring the voltage levels at different parts of the circuit. Finally, the circuit board can be tested as part of the system to see if it performs as assigned.

4. DESIGN PROCESS OF RT-BOX – TRENZ INTERFACE BOARD

This chapter describes the design process of the interface board designed specifically between Plexim RT-Box and Trenz TEBF0808 carrier board. The board is designed to provide a connection between the two systems and to modify the signals transferred between the hardware. Figure 13 depicts the block diagram of the designed main functions of the board.

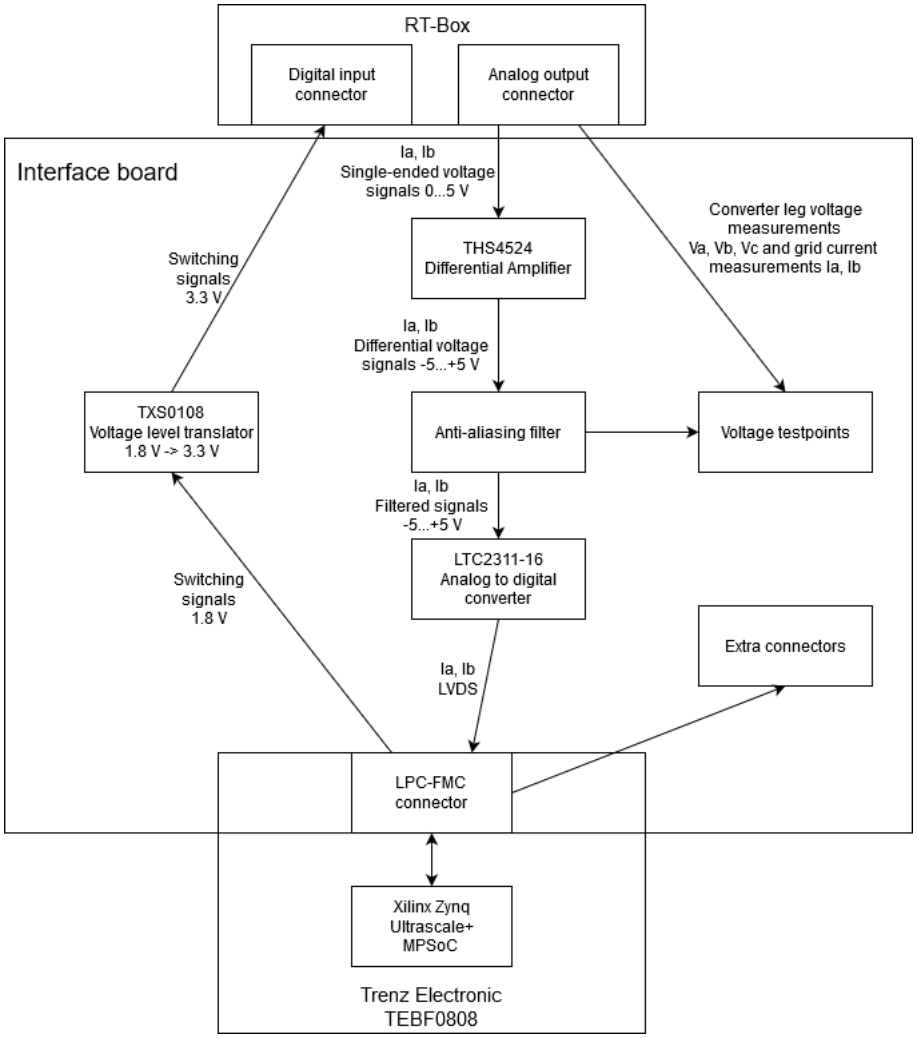

Figure 13. *Block diagram of the Trenz- RT-Box interface board*

This chapter describes the design of the board functions and the design choices that were made. The main functionalities are explained in more detail to give a thorough understanding of the design process of the interface board.

4.1 The power supply of the PCB

Integrated circuits located at the interface board need a power supply to operate. In addition, since TEBF0808 and RT-Box are using different logic levels in their operation all the signals that are transferred from one device to another must be scaled to the recipient device level in the interface board. Therefore, voltage regulators and voltage level shifters must be introduced to the board to provide all voltage levels needed.

The interface board does not need any additional external power source since all voltage levels and power can be drawn from the RT-Box and TEBF0808 and applied either directly to the component or through a voltage regulator. The RT-Box supplies the 5 V voltage level to the PCB and the TEBF0808 supplies 3.3 V, 12 V, and one freely adjustable voltage level as stated in the FMC- standard [17, p. 69]. The maximum allowable adjustable voltage level of the ANSI/VITA 57.1. standard is 3.3 V [17, p. 69], but the TEBF0808 limits the maximum voltage to 1.8 V and limits the available range to four voltage levels (1.2 V, 1.25 V, 1.5 V, and 1.8 V) [13, p. 37]. In Table 2 all voltage levels used in the interface board are presented along with their supplier.

Table 2. *Voltage levels used in the interface board*

Voltage level	Supplier	Used in
12 V	FMC-connector, pins C35, C37	The power supply of LTC6655 voltage regulator
5 V	RT-Box, DI pin 19	Differential Amplifier, ADC, Voltage Regulator
+5 V	LTC6655 Voltage Reference	ADCs as the reference voltage level of conversion
3.3 V	FMC-connector, pins D40, D38, D36, C39	TXS0108 as the reference voltage level of RT-Box
2.5 V	REF2925 Voltage Reference	I/O interface digital power of the ADCs
1.8 V	FMC-connector, adjustable pin G39	TSX0108E as the reference logic voltage level of FPGA

As can be seen from Table 2, two different suppliers of 5 V are introduced to the interface board. The 5 V voltage supplied by the RT-Box is used as a power supply for almost all devices on the interface board, whereas the +5 V supplied by LTC6655 applies to the AD-converters to provide the reference voltage level of the AD-conversion. LTC6655 is a low-noise, precision 5 V voltage reference from Linear Technology [35]. LTC6655 uses a supply voltage of 12 V supplied by the FMC-connector. The LTC6655 must be added to the PCB to ensure a very accurate and stable reference voltage for the AD-converter since it must not have any ripple or fluctuations to enable the desired operation of the ADC. If the voltage level used as a reference in the conversion changes, the quality of the conversion diminishes greatly or is even rendered impossible. Such problems might have occurred if the 5 V voltage level supplied from the RT-Box had been used as a reference. The RT-Box 5 V voltage level is used to power also other components on the PCB and constantly changing load would possibly cause ripple to the ADCs thus deteriorating the conversion.

REF2925 is a low-power 2.5 V voltage reference from Texas Instruments [36]. The REF2925 uses a supply voltage of 5 V drawn from the RT-Box and its output is 2.5 V reference voltage. The 2.5 V voltage produced by the device is used in AD-converters to select LVDS mode, as well as provide power to digital I/O interfaces.

4.2 The logic level shift of switching signals

In order to change the switching state of the semiconductor switches, control signals are introduced from the controller to the emulated NPC inverter. As presented in Figure 13, the control logic of the inverter is implemented on the TEBF0808 base board and the switching signals are transferred to the RT-Box digital inputs via the interface board. The two devices use different internal logic levels, meaning that the controller outputs the signals in voltage levels that the emulator cannot process correctly if routed directly to the input pins. The internal logic levels of the devices are presented in Figure 14.

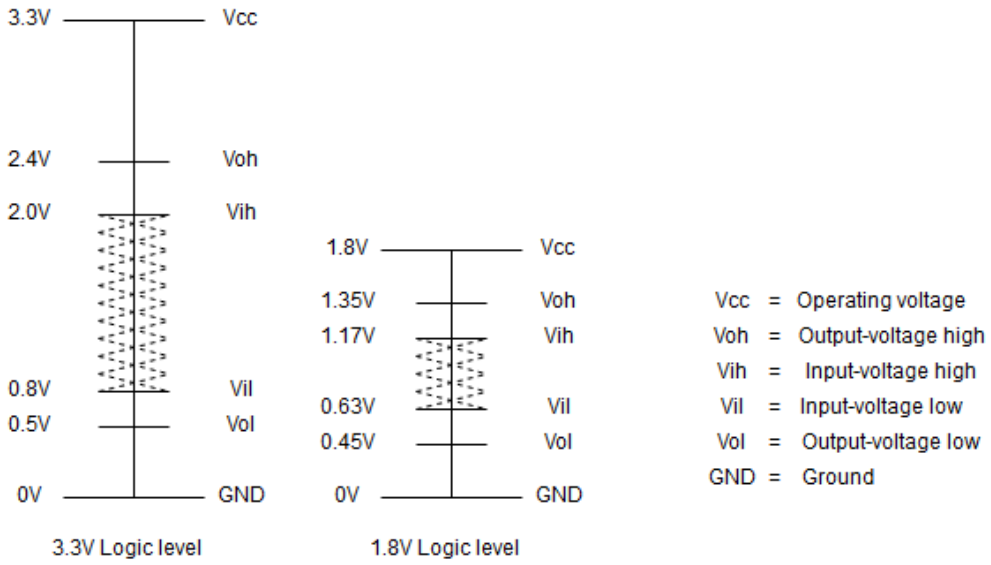

Figure 14. *Logic levels used internally in RT-Box (left) and TEBF0808 (right), (modified from source [37, p. 4])*

As shown in Figure 14, the two logic levels have significant differences between their operating and threshold voltage levels. In order for the RT-Box to detect the control signal to be 1, i.e. the switch must be turned on, at least 2.0 V and at most 3.3.V threshold voltage (V_{IH}) must be introduced to the input pin. Figure 14 shows that the output voltage level of the ON signal of the controller is between 1.35 V and 1.8 V (V_{OH} to V_{CC}). Therefore, the switch control signals must not be routed directly to the inverter, but the logic level of the control signals must be increased to 3.3 V in the interface board. The logic level shift is implemented with two Texas Instruments TXS0108 voltage translators.

TXS0108 is an 8-bit, 8-channel, two-directional, level-shifting voltage translator from Texas Instruments [38]. The pin configuration of the voltage translator is presented in Figure 15.

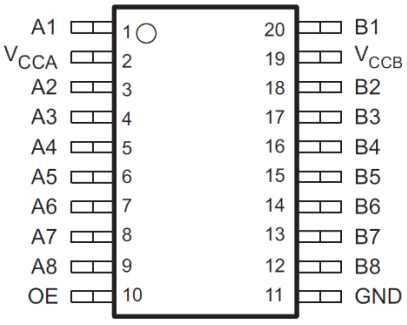

Figure 15. *TXS0108 Voltage translator pin configuration [38]*

According to the TXS0108 datasheet, the logic level reference voltages are applied to V_{CCA} and V_{CCB} pins, 1.8 V and 3.3 V respectively [38, p. 4]. The reference voltage thus determines the logic level of the pins on the same side of the chip as the voltage reference. In addition, both voltage references are connected to a 100 nF bypass capacitor according to the instructions in the component datasheet. The bypass capacitor smooths the variations of the operating voltage reference. Using this method, possibly low-quality operating voltage does not spoil the logic level translation.

Connected to the “A-side” of the device (pins 1 to 10) are 1.8 V logic level switching signals from the controller (6 out of total 12 switching signals are connected to one TXS0108 device) and one additional signal. The additional empty signal path is connected to the RT-Box in case there is a need for an additional signal route in the future. The inclusion of the additional signal path may possibly increase the lifetime of the interface board. On the “B-side” of the device (pins 11 to 20), the pins are connected to the emulator. The microchip handles the logic level transformation according to the 3.3 V reference voltage supplied to V_{CCB}, and the level-shifted control signals are fed directly to the RT-Box via a cable-connected D-Sub -connector. Table 3 presents the signal assignment of the RT-Box digital input connector and the signal routes between the connector and TXS0108.

Table 3. *Signal assignment between TXS0108 and RT-Box digital input connector*

Signal	TXS0108 pin	RT-Box pin	RT-Box channel	Description
		Voltage translator U6		
S11 RT-Box	18	17	DI29	Level shifted switch 11 control signal
S12 RT-Box	17	35	DI28	Level shifted switch 12 control signal
S13 RT-Box	16	16	DI27	Level shifted switch 13 control signal
S21 RT-Box	15	34	DI26	Level shifted switch 21 control signal
S22 RT-Box	14	15	DI25	Level shifted switch 22 control signal
S23 RT-Box	13	33	DI24	Level shifted switch 23 control signal
Extra 1 RT-Box	12	32	DI23	Unused digital signal path to RT-Box
		Voltage translator U7		
S31 RT-Box	18	11	DI18	Level shifted switch 31 control signal
S32 RT-Box	17	29	DI17	Level shifted switch 32 control signal
S33 RT-Box	16	10	DI16	Level shifted switch 33 control signal
S41 RT-Box	15	9	DI15	Level shifted switch 41 control signal
S42 RT-Box	14	27	DI14	Level shifted switch 42 control signal
S43 RT-Box	13	8	DI13	Level shifted switch 43 control signal
Extra 2 RT-Box	12	26	DI12	Unused digital signal path to RT-Box

Unlike in [16], there is no need to transmit the switching signals to the inverter using optical fibres [16 p. 39]. Compared to the real inverter there are no sources of electromagnetic interference (EMI) in simulator operation. This is due to the fact that the emulator setup lacks any hard-switching IGBTs that are known to be a great source of EMI. The latter interferes with the highly sensitive switching signals transmitted via the copper cables.

The OE-pin is connected to 1.8 V via a 100 Ω pull-up resistor to always enable the operation of the device. The resistor is added to limit the current that charges the internal capacitors when the board is powered up. As a result, the beginning of the operation of the device is delayed.

4.3 Measurements

The RT-Box enables the monitoring of the emulated signals by means of the PLECS software. As an alternative option for monitoring the signals, test points are added to the interface board from where the signals can be driven through differential probes to an oscilloscope [39], [40]. Signals of interest in this setup are the simulated inverter phase current values, and phase to neutral point (NP) voltages of the inverter.

In this thesis the three phases are noted as a, b and c. However, in the Altium design documents (Appendix A and appendix D) the notations used for the phases are u, v and w. When studying the design, it should be kept in mind that **a** corresponds to **u**, **b** to **v** and **c** to **w**.

The analog outputs of the RT-Box are voltage signals and thus the phase current values cannot be measured as a current. Table 4 presents the signal assignment of an analog output connector. The phase current values are expressed in magnitudes of voltage, scaled between 0 ... 5 V. As shown in Section 2.3, the resolutions of the RT-Box outputs are 16 bits, so the accuracy of the output signal is $\frac{range}{2^{bit\ amount}} = \frac{5\ V}{2^{16}\ bit} = 0.0763\ {}^{mV}/_{bit}$. [41]

Table 4. *Signal assignment of the analog output connector*

Signal	RT-Box pin	RT-Box channel	Description
ANALOG Ia	13	AO12	Phase current Ia
ANALOG Ib	10	AO9	Phase current Ib
ANALOG Va	1	AO0	Phase-NP voltage Va
ANALOG Vb	3	AO2	Phase-NP voltage Vb
ANALOG Vc	5	AO4	Phase-NP voltage Vc
ANALOG EXT1	16	AO15	Unused signal path to ADC U1
ANALOG EXT2	7	AO6	Unused signal path to ADC U8

The positions of the switches can be determined by measuring the voltage between the phase and the neutral point of the inverter. This measurement takes place within the simulator system using PLECS software. Voltmeters are introduced to the inverter model to be built in PLECS and the outputs of the voltmeters are routed to analog output blocks of the RT-Box. As stated in Section 2.2, when two upper switches are in the conductive state, the phase-neutral voltage is equal to $\frac{V_{DC}}{2}$, when the two middle switches are on the output phase voltage is 0, and when the two lower switches are turned on the output phase voltage is $\frac{-V_{DC}}{2}$. As discussed previously, the voltage range of the analog outputs of the RT-Box is selected to be 0… 5 V, meaning that the emulated output phase voltages of the converter must be shown at the designated voltage range. For all three possible values of the output phase voltage, the corresponding voltage values within the available range are predetermined. Table 5 presents the phase-neutral point voltages with the corresponding RT-Box output voltages.

Table 5. *Actual phase-neutral point voltages with corresponding output voltages*

Actual phase-NP voltage	Corresponding output voltage
$\frac{V_{DC}}{2}\ V$	$5.0\ V$
$0\ V$	$2.5\ V$
$\frac{-V_{DC}}{2}\ V$	$0\ V$

The corresponding output voltages are routed from the analog output connector of the RT-Box to a separate connector on the PCB for future extensions. In addition, voltage measurement points for the oscilloscope are placed on the interface board.

4.4 Analog-to-digital conversion circuit

To be able to control the inverter, the controller requires information about the output currents of the inverter. Since the inverter operation is only emulated inside the RT-Box, the current measurements are not carried out using conventional sensors, but using the PLECS software to implement measurements to the simulation model and assigning the results to analog output pins with a voltage range of 0…5 V. The TEBF0808 processes all information digitally and in order to introduce the measurement signals to the controller, the signals must be converted from analog to digital in the interface board. For this purpose, an analog-to-digital converter is introduced to the circuit board, the task being to convert the analog signals to digital as accurately as possible [41, p. 1].

Analog signals are continuous-time signals, while digital signals are discrete-value presentations of the corresponding data included in analog signals. The basic idea of the analog-to-digital conversion is to determine the instantaneous value of the analog signal with a given sampling frequency and to convert the instantaneous value into a corresponding digital form by means of the AD-converter. In selecting the AD-converter, the most important attribute is the sampling frequency. The sampling frequency determines how frequently the analog signal is sampled and thus its instantaneous value recorded.

According to the Nyquist sampling theorem, an AD-conversion should be performed so that the sampling frequency is at least twice the maximum frequency component of the signal to be converted [42]. A frequency that is half the sampling frequency is called the Nyquist frequency, and in order for the AD-conversion to be successful, none of the frequency components of the converted signal must exceed it. This means that at least two samples of the signal must be taken during one cycle. As the sampling frequency increases, the accuracy of the digital signal also increases as the instantaneous values of the analog signal are sampled more frequently and the changes between the samples are smaller. A high sampling frequency is, therefore, a desirable feature of an AD-converter. Figure 16 presents the effect of sampling frequency on the accuracy of the digital signal. The input is a continuous-time analog signal and the output a discrete digital signal constructed in the ADC.

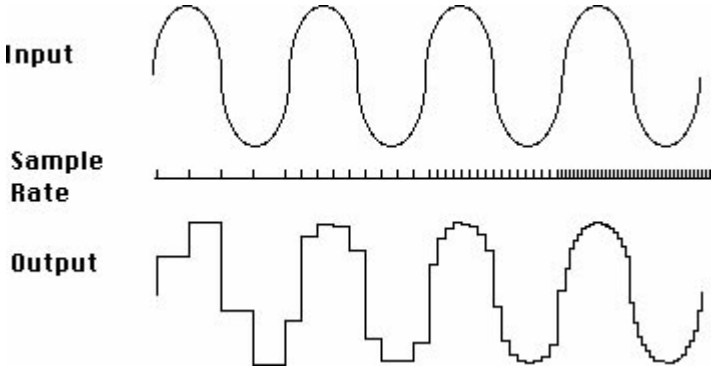

Figure 16. *Effect of sampling frequency to digital signal accuracy [43]*

In this thesis, the AD-conversion is implemented by combining a simple sample-and-hold mechanism with a successive approximation register (SAR) AD-conversion method. The sample-and-hold mechanism, the operation of which is discussed in more detail here [16, p. 42], takes a sample of the analog signal and stores the instantaneous value of the signal as a voltage to a capacitor. The SAR then compares the voltage of the capacitor to the centre of the signal range determined for the AD-converter and examines whether the sample is larger or smaller than the most significant bit (MSB) of the digital result. The potential voltage range decreases after each MSB comparison, and the SAR moves to determine the value of the next bit. When all available bits are compared, the best possible digital result is constructed from the sample. [44] Thus, SAR

compares the instantaneous value of the sampled analog signal to possible discrete voltage levels and attempts to determine the value closest to it.

This thesis utilizes an LTC2311-16 AD-converter by Linear Technology. The LTC2311-16 is a 16-bit, differential input ADC capable of 5 Msps throughput rate [45]. It utilizes the above-described SAR method for the digitisation of an analog signal. Figure 17 presents the pin configuration of the ADC.

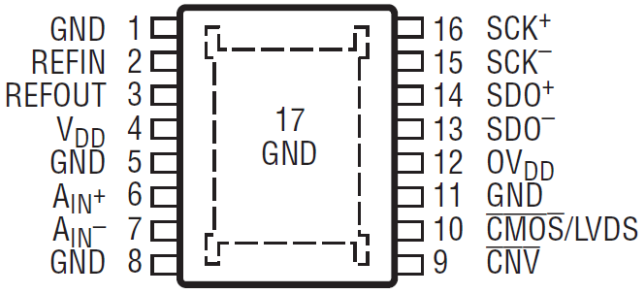

Figure 17. *LTC2311-16 ADC pin configuration [45]*

The LTC2311-16 uses 5 V main power supply in pin V_{DD}. The REFOUT pin determines the maximum range of analog inputs A_{IN+} and A_{IN-}, which is desired to be -5… 5 V. The REFOUT is internally connected to the 4.096 V voltage, thus being unsuitable for the converter use. However, the REFOUT can be overridden with the desired analog signal range by connecting the REFIN pin to the ground plane and connecting the 5 V to REFOUT.

The success of the AD-conversion is highly dependent on the right timing. The $\overline{CNV}$ connector and its voltage determine the timing of the ADC conversion. When high voltage is applied to the pin, the sample-and-hold circuit samples the instantaneous value of the analog input. As the voltage applied to the $\overline{CNV}$ pin drops, SAR compares the voltage to the discrete values and the output data is clocked out. For more information on $\overline{CNV}$ timing, see the datasheet [45, p. 21].

Similar to the conversion process, the output of the digital signal must be timed as well. For this, a differential clock signal from the FPGA is connected to the SCK^+ and SCK^- pins. At the falling edge of the clock signal, the conversion result of the SAR is transferred to the differential output pins SDO + and SDO.

The LTC2311-16 is capable of both $\overline{CMOS}$ and LVDS I/O data transfers (Figure 17, pin 10). In this thesis, the LVDS I/O mode is selected, to allow the data to be transferred differentially. The carrier board uses the same signalling method for its internal communication between FMC-connector and FPGA. According to the instructions in the datasheet, the OV_{DD} supply voltage pin is connected to 2.5 V to select the LVDS communication. Additionally, OV_{DD} provides the I/O interface power supply to the ADC.

4.5 Differential signalling and differential amplifier

In differential signalling, the information of one signal is transmitted via two neighbouring wires so that one of the signals is transmitted as the original signal and the other is its corresponding inverted signal [46]. Figure 18 presents the principles of differential signalling. It is possible to achieve excellent noise immunity and low device-generated switching noise (EMI) by means of differential signalling method [47]. The drawback of the differential signalling is, for example, a larger PCB space required when two wires are used instead of one and an increased number of components to allow differential data transmission.

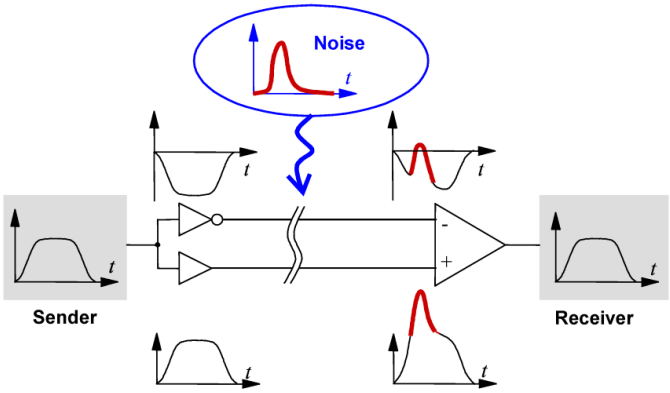

Figure 18. *Fundamentals of differential signalling* [48]

The signal inputs of the LTC2311-16 ADC introduced in Section 4.4 are differential, while the phase current outputs of the RT-Box are single-ended signals. Thus, a conversion from the single-ended signals to the differential pair prior to the AD-converter must be implemented on the interface board. For this purpose, the Texas Instruments differential amplifier is utilized. The amplifier is used not only as a signal converter but also as a driver of the ADC for driving capacitive components inside the ADC [16, p. 43]. The amplifier provides a low output impedance for the signals to be converted and isolates the signal source and the ADC from each other.

The THS4524 is a very low-power, 4-channel, fully differential amplifier from Texas Instruments [49]. The pin configuration of the device is presented in Figure 19.

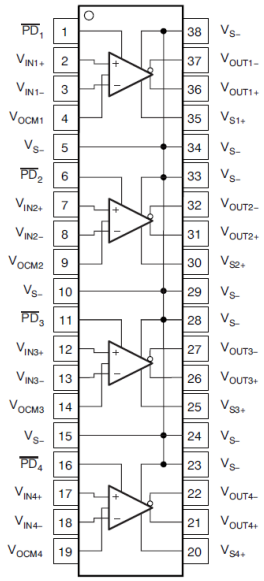

Figure 19. *THS4524 differential amplifier pin configuration [49]*

The THS4524 houses four amplifier circuits inside one device chip. In this thesis, only two phase current outputs of the inverter are required, as a three-phase star connection makes it possible to determine the third current from the other two known phase current values. The two remaining amplifier circuits are connected to extra outputs from RT-Box for future use.

The inputs of the differential amplifier are the phase current values from the analog outputs of the RT-Box in the form of voltages. The output voltage range of RT-Box is 0…5 V, as stated in Section 2.3. The single-ended signals to be converted are connected to the non-inverting inputs V_{INX+} of the differential amplifier and ground plane to the inverting inputs V_{INX-}. Furthermore, the ADC input voltage range is set to -5…5 V, hence the common-mode voltage pins V_{OCMX} should be connected to the ground plane via a capacitor.

In order for the device to function normally $\overline{\mathrm{PD}}_x$ (power down) connectors must be left open in all 4 amplifier circuits. The device is supplied with 5 V supply voltage from RT-Box to V_{SX+} pins.

A Differential amplifier acts as an amplifier by its name. In this thesis, the gain of the amplifier is set equal to 1 in order to transmit the signal to the ADC within its input range limits. The gain is determined by comparing the resistor R_F value with the value of the resistor R_G, both presented in Figure 20. The resulting gain is $G = \frac{R_F}{R_G}$. In this thesis, 1 kΩ resistors are used in accordance with the datasheet instructions.

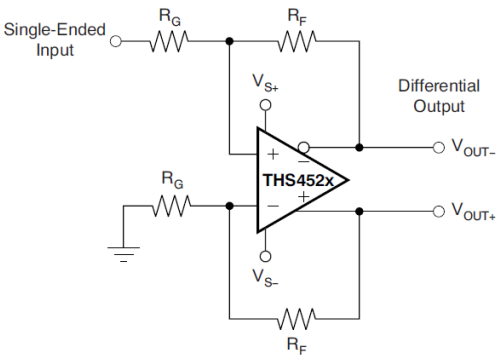

Figure 20. *Single-ended to differential amplifier circuit [49, p. 50]*

4.5.1 Anti-aliasing filter

The datasheets of the differential amplifier and AD-converter recommend the use of a filter circuit between these components to reduce the interference caused by high-frequency signals. High-frequency interferences cause inaccuracy to the AD conversion, which is undesirable for the correct operation of the system [42].

The signals transmitted on the circuit board may contain components with a frequency higher than the Nyquist frequency (see Section 4.4), for example, as a result of transmission line stray signals [42]. Interference from high-frequency components can be removed using a low-pass filter. The low-pass filter allows low-frequency signals to pass through the filter circuit normally while interfering high-frequency signal components are filtered out. To this end, an anti-aliasing filter, in the form of a low-pass filter, is introduced to the circuit to remove the interfering signals.

As a consequence of the similarity between the board developed in this thesis and that in [16], this pre-simulated filter circuit [16, p. 44] can be utilized using the same component values. The filtering-behaviour of the anti-aliasing filter circuit is simulated in the reference [16, p. 43], and the results show that the phase shift of the sampling frequency starts at 100 kHz. Signals that have lower frequency will pass through the filter circuit normally. The utilized filter circuit is presented in Figure 21.

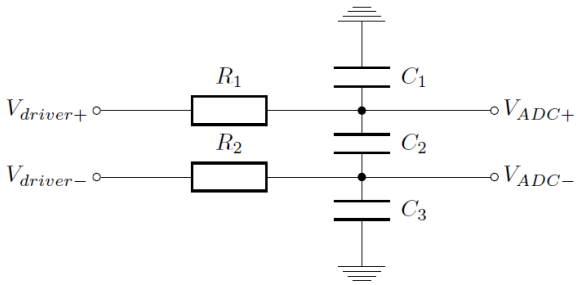

Figure 21. *Low-pass filter circuit [16, p. 44]*

The anti-aliasing filter circuit is placed at the output of the differential amplifier. The $V_{driver+}$ signal is routed from the positive output of the differential amplifier and the $V_{driver-}$ from the negative output to the filter circuit. The resistors R_1 and R_2 are recommended to be added when connecting a filter with the output of differential amplifiers.

4.6 Additional connectors and components

The interface board designed for the simulator setup does not utilize all signal paths provided by the RT-Box and Trenz TEBF0808. Unused pins are routed to additional connectors for more versatile utilization of the interface board in the future. There is no use for the extension connectors in this thesis. However, the possibility of expanding the interface board by providing additional features to the FPGA via unused signal paths is maintained.

Two additional signal paths are connected to the digital input connector of the RT-Box. The unused pins of the voltage translators are utilized as an additional signal path from the FPGA to the RT-Box. Table 6 presents the unused signals, their connection to the voltage translators, the signal source from the FMC-connector and the RT-Box input pin.

Table 6. *Additional signals to RT-Box digital inputs*

Signal	Device	Pin	FPGA I/O	RT-Box DI pin
EXTRA 1 RT-Box	Voltage translator U7	12	LA32_N	32
EXTRA 2 RT-Box	Voltage translator U8	12	LA29_N	26

Of the four amplifier circuits of the differential amplifier used in the AD-conversion circuit, only two are utilized in the interface board. The remaining two amplifier circuits are connected to the analog output connector of the RT-Box, like the measured current signals, and the corresponding AD-conversion circuits are implemented for future use. There is no need for the additional AD-conversion circuits in the current simulator setup. In any case, the possibility of additional signal transfer in the future remains. The analog output pins of the RT-Box and the designated amplifier circuits of the differential amplifier are presented in Table 7.

Table 7. *Additional signals to differential amplifier for additional AD-conversion*

Signal	Device	Pin	RT-Box AO pin
ANALOG EXT1	Differential amplifier U2	2	16
ANALOG EXT2	Differential amplifier U2	17	7

The LPC-FMC-connector used in the interface board houses 68 general-use signal lanes, according to the standard [17] while the interface board utilizes only 23 of them. 38 of the remaining lanes are connected to two additional connectors P1 and P2 and 7 lanes are completely unused. 6 of the signal lanes connected to the extension connectors P1 and P2 are capable of clock signal usage (lanes denoted with _CC). Table 8 presents the signal configuration between FMC-connector and the extension connectors P1 and P2.

Table 8. *Signal assignment of additional connector's pins*

Connector	Pin	FPGA I/O / Signal
P1	1,2,4,6,23,24	Ground
P1	3	LA01_P_CC
P1	5	LA01_N_CC
P1	7	LA06_P
P1	9	LA06_N
P1	11	LA05_P
P1	13	LA05_N
P1	15	LA10_P
P1	17	LA10_N
P1	19	LA09_P
P1	21	LA09_N
P1	8	LA03_P
P1	10	LA03_N
P1	12	LA08_P
P1	14	LA08_N
P1	16	LA12_P
P1	18	LA12_N
P1	20	LA16_P
P1	22	LA16_N
Connector	**Pin**	**FPGA I/O / Signal**
P2	1,2,20,22	Ground
P2	23,24	3P3V
P2	3	LA14_P
P2	5	LA14_N
P2	7	LA17_P_CC
P2	9	LA17_N_CC
P2	11	LA18_P_CC
P2	13	LA18_N_CC
P2	15	LA27_P
P2	17	LA27_N
P2	19	LA26_P
P2	21	LA26_N
P2	4	LA20_P
P2	6	LA20_N
P2	8	LA22_P
P2	10	LA22_N
P2	12	LA25_P
P2	14	LA25_N
P2	16	LA24_P
P2	18	LA24_N

5. RESULTS AND CONCLUSIONS

The goal of this bachelor's thesis was to enable the use of a new HIL-simulator system that can be used for power electronic applications, such as the control of a three-phase, three-level NPC inverter. For this purpose, an interface board was designed for interconnecting the simulator (i.e., HIL system) with the control platform. Within the scope of the thesis, the relevant design files of the interface board were completed. Although the board was not assembled during the thesis, debugging and performance verification has been partly performed. Thus, potential errors that may appear when the physical board will be tested have been (mostly) avoided.

The design and implementation of the PCB is meant to be used in a power electronic system based on an NPC inverter. Given this, it should be pointed out, that the design of the board is case-specific, i.e., it can be utilized only for the aforementioned case study since it is tailored to its needs. This implies that for different case studies a different interfacing board needs to be designed.

5.1 In the future

Future steps include soldering and testing of the board. Note that instructions about these steps are provided in this thesis. Moreover, when testing the electrical properties of the board it is important to measure the voltage levels used on the circuit board as well as to check for possible open and short circuits

The purpose of the thesis was to design a physical link between the two simulator devices without realizing the simulator performance itself to the hardware. The programming of the simulator equipment and the control signals required by the components of the user interface board, for example, clock signals, must be implemented in order to provide a fully functioning simulator system. The actual performance of the designed circuit board can only be tested after the simulator and control platform have been programmed and the circuit board is used for providing the connection between them. The detailed process of programming of the simulator equipment was intentionally excluded from the design process since it was out of the scope of the thesis.

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APPENDIX A: ALTIUM DESIGNER SCHEMATIC DOCUMENTS

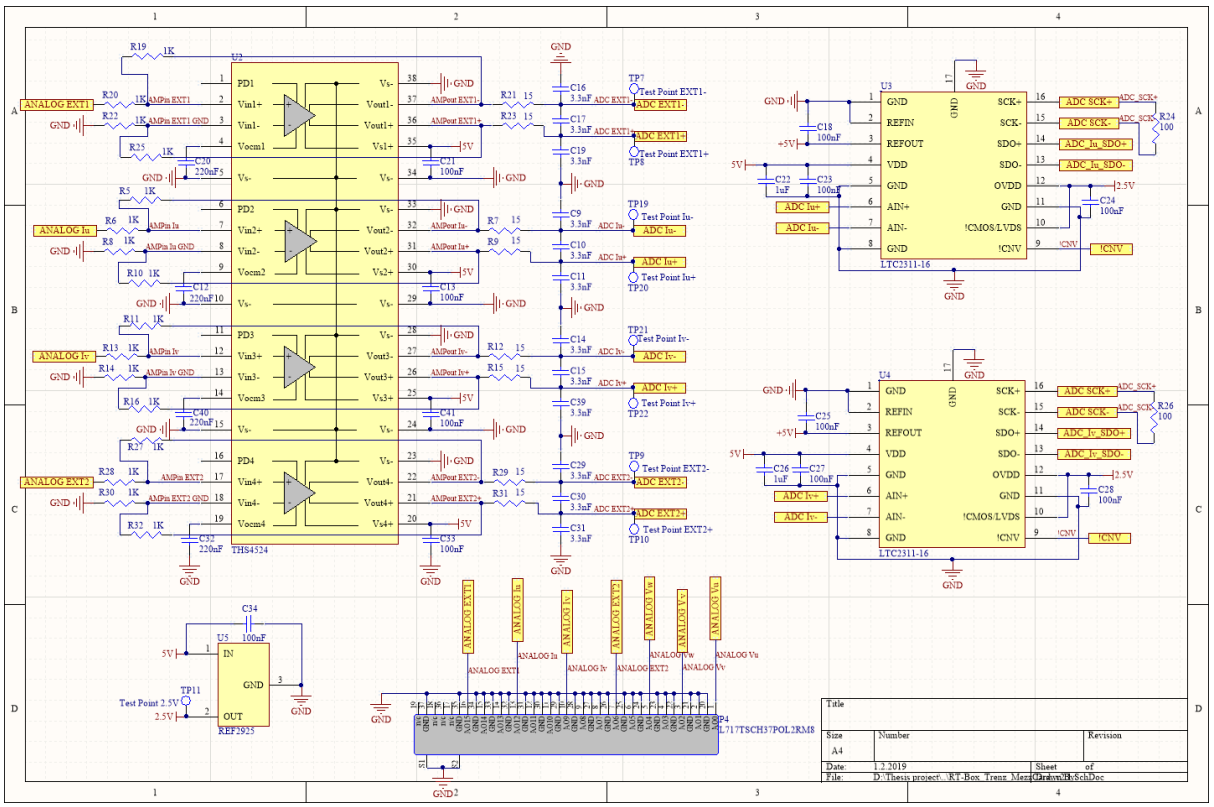

Figure A. 1. *Schematic of differential amplifier, analog output connector, voltage reference and ADC 1&2*

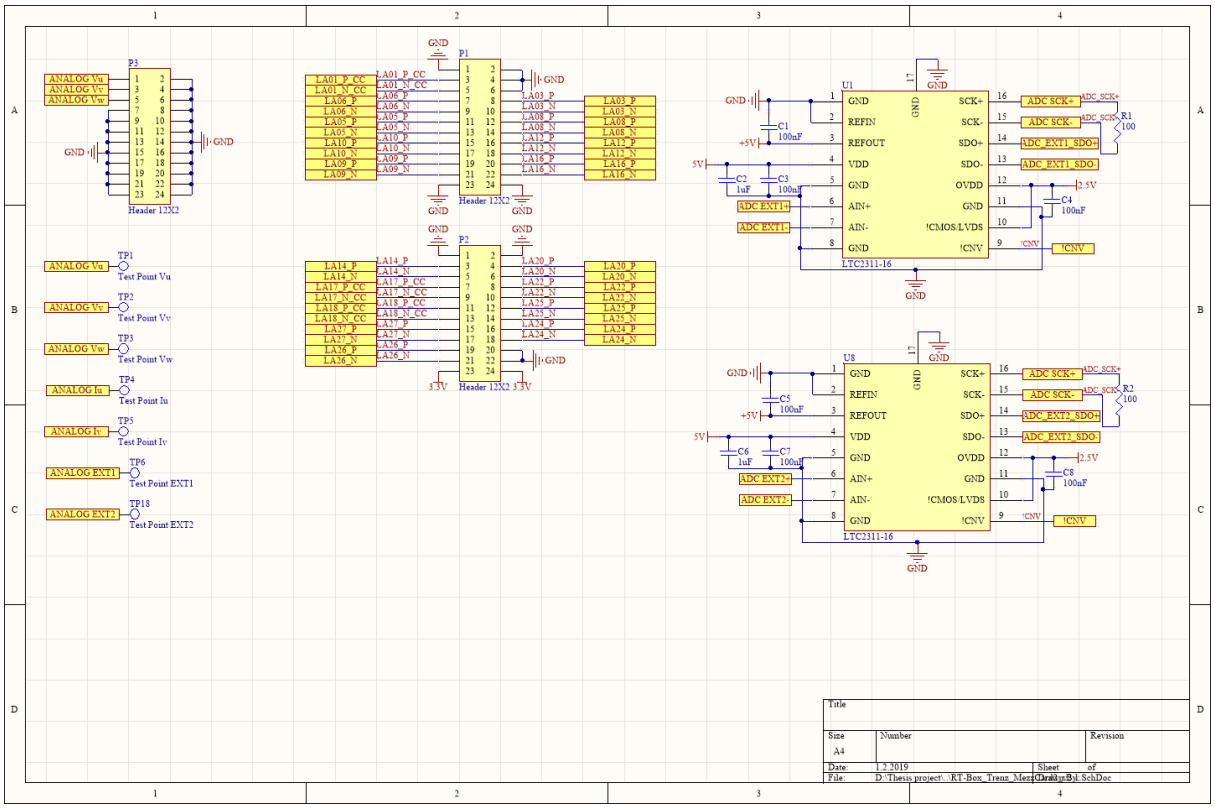

Figure A. 2 *Schematic of extra connectors, voltage testpoints, and ADC 3&4*

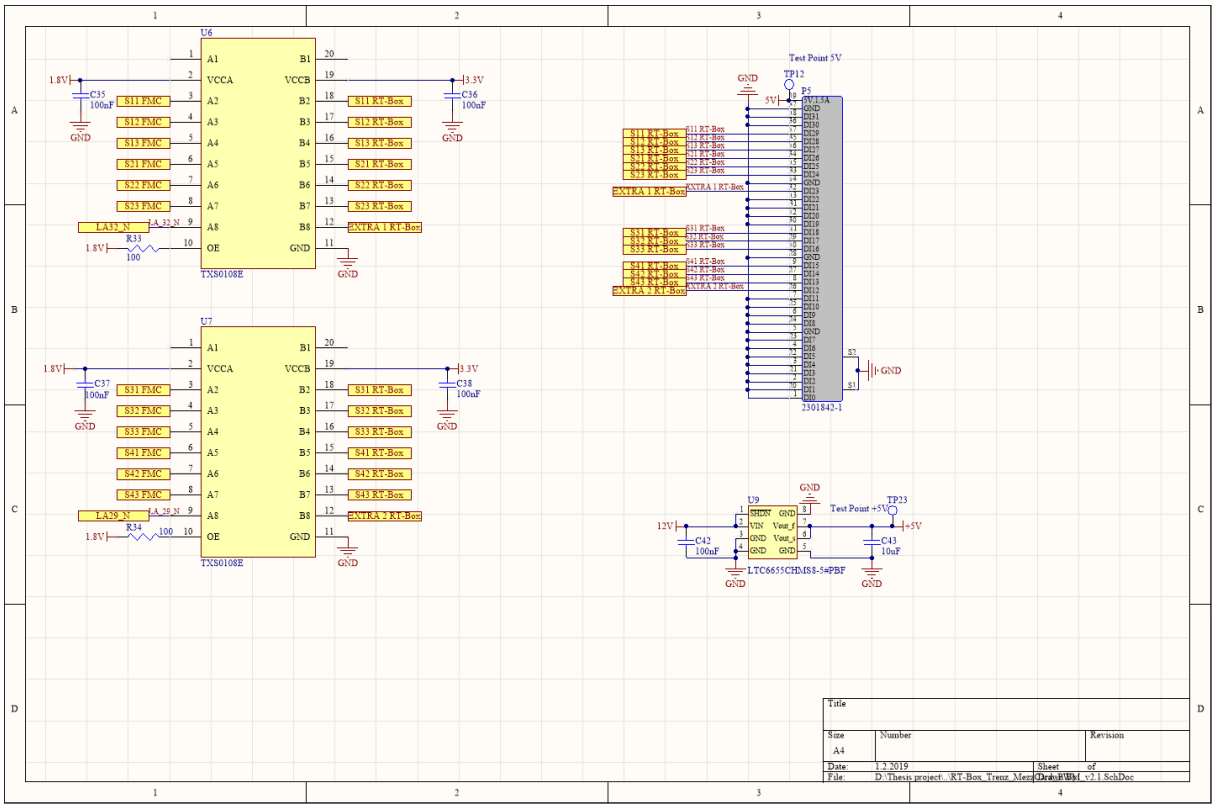

Figure A. 3. *Schematic of digital input connector, voltage translators U6 & U7 and 5 V voltage reference*

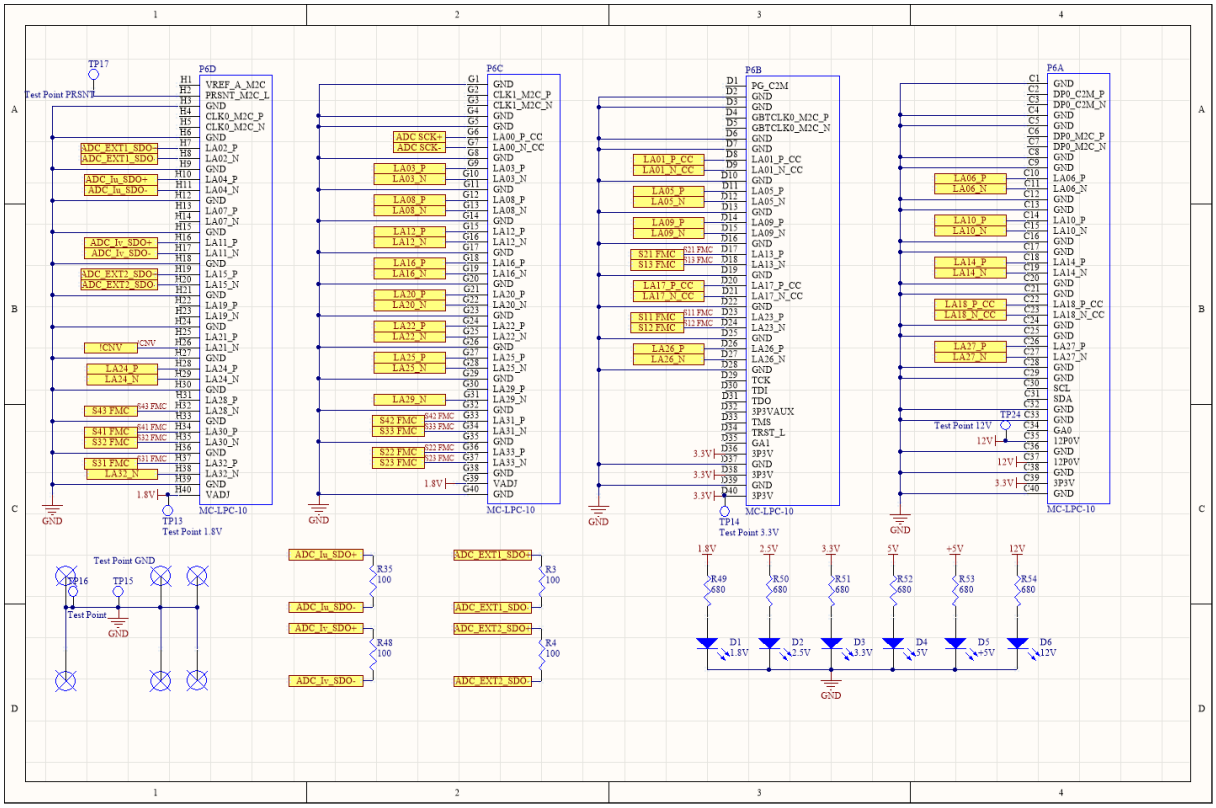

Figure A. 4. *Schematic of FMC-connector, mounting holes and LEDs*

APPENDIX B: LIST OF MATERIALS

Component	Quantity	Ordercode
ASP-134604-01, LPC FPGA-connector	1	2433507
TXS0108E, Voltage level translator	2	595-TXS0108EPWR
LTC2311-16, AD-Converter 16Bit	4	LTC2311CMSE-16#PBF-ND
THS4524, Differential Amplifier	1	2496350
REF2925AIDBZT, 2.5V Voltage Reference	1	2781885
LTC6655CHM8-5#PBF, 5.0V Voltage Reference	1	
Header 12x2	3	1593448
Test-1-R, PCB Test Point	24	1701997
L717TSCH37POL2RM8, D-Sub connector, male	1	2401258
2301842-1, D-sub connector, female	1	2857981
Capacitor, 220nF	4	1759172
Capacitor, 3.3nF	12	3019901
Capacitor, 100nF	22	2673142
Capacitor 10uF	1	81-GJ821BR61E106KE1L
Capacitor, 1uF	4	1833845
Resistor 15Ω	8	2057671
Resistor 1kΩ	16	2303550
Resistor Kit, 100-976Ω, 19200 pcs	1	RSM2C-ND
APTD2012LCGCK, Standard Green LED	6	604-APTD2012LCGCK

Figure B. 1. *List Of Materials*

APPENDIX C: FMC-CONNECTOR PIN CONFIGURATION

	K	J	H	G	F	E	D	C	B	A
1			VREF_A_M2C	GND			PG_C2M	GND		
2			PRSNT_M2C_L	CLK1_M2C_P			GND	DP0_C2M_P		
3			GND	CLK1_M2C_N			GND	DP0_C2M_N		
4			CLK0_M2C_P	GND			GBTCLK0_M2C_P	GND		
5			CLK0_M2C_N	GND			GBTCLK0_M2C_N	GND		
6			GND	LA00_P_CC			GND	DP0_M2C_P		
7			LA02_P	LA00_N_CC			GND	DP0_M2C_N		
8			LA02_N	GND			LA01_P_CC	GND		
9			GND	LA03_P			LA01_N_CC	GND		
10			LA04_P	LA03_N			GND	LA06_P		
11			LA04_N	GND			LA05_P	LA06_N		
12			GND	LA08_P			LA05_N	GND		
13			LA07_P	LA08_N			GND	GND		
14			LA07_N	GND			LA09_P	LA10_P		
15			GND	LA12_P			LA09_N	LA10_N		
16			LA11_P	LA12_N			GND	GND		
17			LA11_N	GND			LA13_P	GND		
18			GND	LA16_P			LA13_N	LA14_P		
19			LA15_P	LA16_N			GND	LA14_N		
20			LA15_N	GND			LA17_P_CC	GND		
21			GND	LA20_P			LA17_N_CC	GND		
22			LA19_P	LA20_N			GND	LA18_P_CC		
23			LA19_N	GND			LA23_P	LA18_N_CC		
24			GND	LA22_P			LA23_N	GND		
25			LA21_P	LA22_N			GND	GND		
26			LA21_N	GND			LA26_P	LA27_P		
27			GND	LA25_P			LA26_N	LA27_N		
28			LA24_P	LA25_N			GND	GND		
29			LA24_N	GND			TCK	GND		
30			GND	LA29_P			TDI	SCL		
31			LA28_P	LA29_N			TDO	SDA		
32			LA28_N	GND			3P3VAUX	GND		
33			GND	LA31_P			TMS	GND		
34			LA30_P	LA31_N			TRST_L	GA0		
35			LA30_N	GND			GA1	12P0V		
36			GND	LA33_P			3P3V	GND		
37			LA32_P	LA33_N			GND	12P0V		
38			LA32_N	GND			3P3V	GND		
39			GND	VADJ			GND	3P3V		
40			VADJ	GND			3P3V	GND		

Figure C. 1. *FMC-connector pin configuration*

LA[00..33]_P, LA[00..33]_N	*LA_XX - LPC, FPGA Bank A,* 68 user-defined, single-ended signals or 34 user-defined, differential pairs (mandatory for LPC)
HA[00..23]_P, HA[00..23]_N	*HA_XX - HPC, FPGA Bank A,* 48 user-defined, single-ended signals or 24 user-defined, differential pairs
HB[00..21]_P, HB[00..21]_N	*HB_XX - HPC, FPGA Bank B,* 44 user-defined, single-ended signals or 22 user-defined, differential pairs
XX_P_CC, XX_N_CC	User-defined clock capable (CC) pins. These pins can be used for clock signals.
CLK[0..3]_M2C_P, CLK[0..3]_M2C_N	4 user clock, differential pairs (CLK[2..3]_M2C only for HPC), bidirectional
GBTCLK[0..1]_M2C_P, GBTCLK[0..1]_M2C_N	Clock signals for multi-gigabit transceiver data pairs (GBTCLK1_x only for HPC)
DP[0..9]_M2C_P, DP[0..9]_M2C_N	multi-gigabit transceiver data pairs (one is mandatory for LPC, 10 in total with HPC)
DP[0..9]_C2M_P, DP[0..9]_C2M_N	multi-gigabit transceiver data pairs (one is mandatory for LPC, 10 in total with HPC)
GA[0..1]	Geographical address of the module (can be used for adressing on I2C bus). These pins are driven by the carrier card.
VREF_A_M2C	Reference voltage for signaling standard of bank A (LAxx and HAxx). Can be left floating, if not required.
VREF_B_M2C	Reference voltage for signaling standard of bank B (HBxx). Can be left floating, if not required.
VIO_B_M2C	This voltage is sourced by the mezzanine module which supports the HB bus. It is used to power the IO Bank of the FPGA.
3P3VAUX	3.3 V auxiliary power supply (max. 20 mA, max. 150 uF cap. load).
VADJ	Adjustable voltage level (0 .. 3.3 V) from the carrier to the mezzanine card (max. 4 A, max. 1000 uF cap. load).
3P3V	3.3 V power from the carrier to the mezzanine card (max. 3 A, max. 1000 uF cap. load).
12P0V	12 V power from the carrier to the mezzanine card (max. 1 A, max. 1000 uF cap. load).
TRST_L	JTAG Reset
TCK	JTAG Clock
TMS	JTAG Mode Select
TDI	JTAG Data In, if JTAG chain is not used by mezzanine card, short TDI and TDO.
TDO	JTAG Data Out, if JTAG chain is not used by mezzanine card, short TDI and TDO.
PRSNT_M2C_L	Present signal. Indicates that a mezzanine module is attached to the carrier. Low active (tie to GND on FMC)
PG_C2M	Active high power good signal. High indicates that VADJ, 12P0V, and 3P3V are within tolerance.
PG_M2C	Active high power good signal. High indicates that VIO_B_M2C, VREF_A_M2C, and VREF_B_M2C are within tolerance.
SCL	I2C serial clock. Interface can support Intelligent Platform Management Interface (IPMI) commands.
SDA	I2C serial data. Interface can support Intelligent Platform Management Interface (IPMI) commands.
RES[0..1]	Reserved, left floating
GND	Signal ground
*_M2C_*	*Mezzanine-to-Carrier, signal is driven by the mezzanine module and received by the carrier card*
*_C2M_*	*Carrier-to-Mezzanine, signal is driven by the carrier card and received by the mezzanine module*

Figure C. 2. *Explanation of the pin signals*

APPENDIX D: FMC-CONNECTOR SIGNAL ASSIGNMENT

Table 9. *Signal assignment of FMC-connector pins*

Signal	Pin	FPGA I/O	Signal description
Switching signals			
S11 FMC	D23	LA23_P	Switch 11 control signal
S12 FMC	D24	LA23_N	Switch 12 control signal
S13 FMC	D18	LA13_N	Switch 13 control signal
S21 FMC	D17	LA13_P	Switch 21 control signal
S22 FMC	G36	LA33_P	Switch 22 control signal
S23 FMC	G37	LA33_N	Switch 23 control signal
S31 FMC	H37	LA32_P	Switch 31 control signal
S32 FMC	H35	LA30_N	Switch 32 control signal
S33 FMC	G34	LA31_N	Switch 33 control signal
S41 FMC	H34	LA30_P	Switch 41 control signal
S42 FMC	G33	LA31_P	Switch 42 control signal
S43 FMC	H32	LA28_N	Switch 43 control signal
ADC operation signals			
ADC_Iu_SDO+	H10	LA04_P	Conversion data output + of ADC U3
ADC_Iu_SDO-	H11	LA04_N	Conversion data output - of ADC U3
ADC_Iv_SDO+	H16	LA11_P	Conversion data output + of ADC U4
ADC_Iv_SDO-	H17	LA11_N	Conversion data output - of ADC U4
!CNV	H26	LA21_N	$\overline{\mathrm{CNV}}$ conversion signal for all ADCs
ADC SCK+	G6	LA00_P_CC	Serial data clock input + for all ADCs
ADC SCK-	G7	LA00_N_CC	Serial data clock input - for all ADCs
Additional operation signals for unused ADCs			
ADC_EXT1_SDO+	H7	LA02_P	Conversion data output + of ADC U1
ADC_EXT1_SDO-	H8	LA02_N	Conversion data output - of ADC U1
ADC_EXT2_SDO+	H19	LA15_P	Conversion data output + of ADC U8
ADC_EXT2_SDO-	H20	LA15_N	Conversion data output - of ADC U8
Additional digital signals to RT-Box			
LA32_N	H38	LA32_N	Unused digital signal path to RT-Box
LA29_N	G31	LA29_N	Unused digital signal path to RT-Box

Signal	Pin	FPGA I/O	Signal description
Additional signals to extension connector P1			
LA01_P_CC	D8	LA01_P_CC	Unused extension signal, clock capable
LA01_N_CC	D9	LA01_N_CC	Unused extension signal, clock capable
LA06_P	C10	LA06_P	Unused extension signal
LA06_N	C11	LA06_N	Unused extension signal
LA05_P	D11	LA05_P	Unused extension signal
LA05_N	D12	LA05_N	Unused extension signal
LA10_P	C14	LA10_P	Unused extension signal
LA10_N	C15	LA10_N	Unused extension signal
LA09_P	D14	LA09_P	Unused extension signal
LA09_N	D15	LA09_N	Unused extension signal
LA03_P	G9	LA03_P	Unused extension signal
LA03_N	G10	LA03_N	Unused extension signal
LA08_P	G12	LA08_P	Unused extension signal
LA08_N	G13	LA08_N	Unused extension signal
LA12_P	G15	LA12_P	Unused extension signal
LA12_N	G16	LA12_N	Unused extension signal
LA16_P	G18	LA16_P	Unused extension signal
LA16_N	G19	LA16_N	Unused extension signal
Additional signals to extension connector P2			
LA14_P	C18	LA14_P	Unused extension signal
LA14_N	C19	LA14_N	Unused extension signal
LA17_P_CC	D20	LA17_P_CC	Unused extension signal, clock capable
LA17_N_CC	D21	LA17_N_CC	Unused extension signal, clock capable
LA18_P_CC	C22	LA18_P_CC	Unused extension signal, clock capable
LA18_N_CC	C23	LA18_N_CC	Unused extension signal, clock capable
LA27_P	C26	LA27_P	Unused extension signal
LA27_N	C27	LA27_N	Unused extension signal
LA26_P	D26	LA26_P	Unused extension signal
LA26_N	D27	LA26_N	Unused extension signal
LA20_P	G21	LA20_P	Unused extension signal
LA20_N	G22	LA20_N	Unused extension signal
LA22_P	G24	LA22_P	Unused extension signal
LA22_N	G25	LA22_N	Unused extension signal
LA25_P	G27	LA25_P	Unused extension signal
LA25_N	G28	LA25_N	Unused extension signal
LA24_P	H28	LA24_P	Unused extension signal
LA24_N	H29	LA24_N	Unused extension signal