TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY
Julkaisu 764 • Publication 764

Matti Karppanen

Issues in Dynamic Analysis and Design of Interconnected DC-DC Power Supply Systems

Tampere 2008

Tampereen teknillinen yliopisto. Julkaisu 764
Tampere University of Technology. Publication 764

Matti Karppanen

Issues in Dynamic Analysis and Design of Interconnected DC-DC Power Supply Systems

Thesis for the degree of Doctor of Technology to be presented with due permission for public examination and criticism in Tietotalo Building, Auditorium TB109, at Tampere University of Technology, on the 21st of November 2008, at 12 noon.

Tampereen teknillinen yliopisto - Tampere University of Technology
Tampere 2008

ISBN 978-952-15-2056-3 (printed)
ISBN 978-952-15-2096-9 (PDF)
ISSN 1459-2045

Abstract

This thesis studies issues in dynamic analysis and design of interconnected DC-DC power supply systems. The history of the dynamic analysis dates back to the 1970s, when the modeling method for an individual switched-mode converter was introduced. Later on, the methods to analyze stability and performance of interconnected systems have been widely discussed in literature. However, a full understanding of many issues regarding the impedance interactions within the systems still seems to be missing. Therefore, the main objective of the thesis is to show that the minor-loop gain, which is commonly used in the interaction analysis, contains perfect information on the stability of the interconnected system but not necessarily much information on the robustness of the stability and the interactions taken place inside the converters. As a consequence of this, the second objective is to introduce techniques with which the interactions can be reduced or totally removed, thus making the dynamic analysis and design of the systems deterministic.

The thesis utilizes two-port networks and the concept of dynamic profile introduced recently in the analyses of converters. Comprehensive formalism is derived to analyze also the effect of output-voltage remote sensing on converter dynamics. Such formalism is not found in literature, although remote sensing is widely used to improve voltage regulation of a converter. The effect of source and load interactions on the converter dynamics are discussed by the general interaction formalisms and the minor-loop gains defined at the input and output of the converter.

Peak-current-mode, input-voltage feedforward and output-current feedforward controls are treated in the thesis as an example of the methods with which the interactions can be reduced. It is shown that a converter under peak-current-mode or input-voltage feedforward control can have ideal input-voltage noise attenuation. Dynamically, this means that the converter would be invariant to source interaction and the converter would act as a buffer within a system preventing the interactions from propagating through the converter. It is shown that the output-current feedforward control can improve the load-transient response of the converter. However, the converter can be more prone to source interaction if the implementation of the feedforward is not made for a converter which has high invariance to source interactions. In addition, the ideal reverse current transfer function is introduced to be an important parameter of the dynamic profile defining the ideality of output-voltage feedback or output-current feedforward control. Extensive experimental measurements are provided to support the theoretical findings with conventional buck converters under different control methods and a fourth-order step-down converter known as superbuck under peak-current-mode control.

Preface

This work was carried out at the Department of Electrical Energy Engineering at Tampere University of Technology (TUT) during the years 2006 – 2008. The research was funded by TUT, Efore Plc and Graduate School in Electrical Engineering. Financial supports in the form of personal grants from Walter Alhström Foundation, Finnish Foundation for Technology Promotion (Tekniikan edistämissäätiö) and Ulla Tuominen Foundation are also greatly appreciated.

First of all, I express my gratitude to Professor Teuvo Suntio for supervising the thesis and providing an excellent research environment. It has been a pleasure to work under his guidance. I thank my former colleague Mikko Hankaniemi, Dr. Tech., for research cooperation and providing answers and insight to numerous problems faced during the research. I am also thankful to all the personnel in the Department of Electrical Energy Engineering for providing enjoyable discussions during coffee breaks. Mikko Kuisma and Kai Zenger deserve special thanks for reviewing and improving the quality of the text in the thesis. I would also like to thank Sirpa Järvensivu for proofreading the manuscript of the thesis.

Finally, I wish to thank my parents for encouragement and patience during the past years.

Tampere, October 2008

Matti Karppanen

Contents

List of Publications

The thesis is based on the following scientific journal and conference publications, which are referred to as P1, P2, P3, P4, P5, P6 and P7 in the text.

[P1] M. Hankaniemi, M. Karppanen, T. Suntio, "Load-imposed instability and performance degradation in a regulated converter," *IEE Proc. Electric Power Applications*, vol. 153, issue 6, November 2006, pp. 781–786.

[P2] M. Karppanen, M. Sippola, T. Suntio, "Source-imposed instability and performance degradation in a regulated converter," in *Proc. IEEE Power Electronics Specialists Conference*, Orlando, USA, June 2007, pp. 194–200.

[P3] M. Karppanen, T. Suntio, M. Sippola, "Impact of output-voltage remote sensing on converter dynamics," *International Review of Electrical Engineering (IREE)*, vol. 2, issue 2, April 2007, pp. 196–202.

[P4] M. Karppanen, T. Suntio, J. Kelkka, "Load and supply invariance in a regulated converter," in *Proc. IEEE Power Electronics Specialists Conference*, Jeju, Korea, June 2006, pp. 2663–2668.

[P5] M. Karppanen, M. Hankaniemi, T. Suntio, M. Sippola, "Dynamical characterization of peak-current-mode-controlled buck converter with output-current feedforward," *IEEE Trans. on Power Electronics*, vol. 22, issue 2, March 2007, pp. 444–451.

[P6] M. Karppanen, T. Suntio, M. Sippola, "Dynamical characterization of input-voltage-feedforward-controlled buck converter," *IEEE Trans. on Industrial Electronics*, vol. 54, issue 2, April 2007, pp. 1005–1013.

[P7] M. Karppanen, J. Arminen, T. Suntio, K. Savela, J. Simola, "Dynamical modeling and characterization of peak-current-controlled superbuck converter," *IEEE Trans. on Power Electronics*, vol. 23, issue 3, May 2008, pp. 1370–1380.

Author's Contribution

In [P1], the author contributed to planning and carrying out the experimental measurements. The theoretical analysis and writing of the publication was mainly done by the first author. Publications [P2]–[P7] were mainly contributed to by the author. Professor Teuvo Suntio – the supervisor of the thesis – gave useful comments and insights regarding the theoretical and experimental findings. In [P3], the second author formulated the analysis method used to evaluate the effect of remote sensing. In [P5] and [P7], the second authors helped with the experimental measurement and analysis.

List of Notations, Symbols and Abbreviations

Notations

$\hat{x}$	Small-signal component of x
X	Steady-state or average component of x
x	Sum of small-signal and steady-state components (i.e., $x = \hat{x} + X$)
$\dot{x}$	Time derivative of x
$\lvert x \rvert$	Absolute value or magnitude of x
$\angle x$	Angle of x
$\mathbf{x}$	Column vector $\mathbf{x} = [x_1, ..., x_n]^{\mathrm{T}}$

Symbols

A_i	Refers to an interface between two subsystems
$\mathbf{A}$	System matrix
a	Coefficient
α	Real part
$\mathbf{B}$	Input matrix
b	Coefficient
β	Imaginary part
$\mathbf{C}$	Output matrix
C	Capacitor
C_{x}	Capacitor to form input-voltage-dependent ramp signal
c	Coefficient or general control variable
$\hat{c}$	Perturbed general control variable
$\hat{c}_{\mathrm{r}}$	Perturbed reference variable
$\mathbf{D}$	Input-output matrix
D	Averaged duty ratio
D'	Averaged complementary duty ratio (i.e., $1 - D$)
$\hat{d}$	Perturbed duty ratio
F_{m}	Duty-ratio gain
f_{CG}	Gain-crossover frequency
f_{CP}	Phase-crossover frequency
$\mathbf{G}$	Transfer function matrix
GM	Gain margin
G_{a}	Modulator gain
G_{c}	Control gain
G_{cc}	Controller transfer function
G_{ci}	Control-to-input-current transfer function
G_{co}	Control-to-output-voltage transfer function
G_{i}	Input-voltage feedforward gain
G_{io}	Input-to-output-voltage or forward voltage transfer function
G_{ioc}	Input-to-output-voltage transfer functions of an impedance block

G_o	Output-voltage feedforward gain
H_i	Output-current sensing gain
H_v	Output-voltage sensing gain
$\mathbf{I}$	Identity matrix
I_{in}	Averaged input current
I_o	Averaged output current
$\hat{i}_{co}$	Perturbed control current
$\hat{i}_{in}$	Perturbed input current
$\hat{i}_{inc}$	Perturbed input current of an impedance block
$\hat{i}_{inL}$	Perturbed input current of subsystem $\mathbf{L}$
$\hat{i}_{inS}$	Perturbed input current of subsystem $\mathbf{S}$
$\hat{i}_N$	Perturbed current of Norton's equivalent current source
$\hat{i}_o$	Perturbed output current
$\hat{i}_{oc}$	Perturbed output current of an impedance block
$\hat{i}_{oL}$	Perturbed output current of subsystem $\mathbf{L}$
$\hat{i}_{oS}$	Perturbed output current of subsystem $\mathbf{S}$
$\hat{j}_o$	Perturbed current of a current sink
k	Coefficient
$\mathbf{L}$	Subsystem transfer function matrix
L	Inductor
L_{ij}	Transfer function of subsystem $\mathbf{L}$
L_M	Minor-loop gain
L_v	Voltage-loop gain
M	Constant
M_1	Upslope of an inductor current
M_2	Downslope of an inductor current
M_c	Slope of an inductor current compensation ramp
PM	Phase margin
q_c	Inductor-current gain
q_i	Input-voltage gain
q_{io}	Output-current gain
q_o	Output-capacitor-voltage gain
R_{s1}	Equivalent sensing resistor of an inductor current
R_{s2}	Equivalent sensing resistor of an output current
R_x	Resistor to form input-voltage-dependent ramp slope
r_C	Equivalent series resistance of capacitor C
r_D	Dynamic resistance of a diode
r_{DS}	Drain-to-source resistance of a MOSFET during on-time
r_E	Equivalent resistance
r_L	Equivalent series resistance of inductor L
$\mathbf{S}$	Subsystem transfer function matrix
S_{ij}	Transfer function of subsystem $\mathbf{S}$
S_M	Sensitivity function (i.e., $1/(1+L_M)$)

s	Laplace variable
T_0	Voltage-loop gain of a converter supplied by an ideal voltage source
T_∞	Voltage-loop gain of a converter supplied by an ideal current source
T_M	Complementary sensitivity function (i.e., $L_\mathrm{M}/(1+L_\mathrm{M})$)
T_oi	Output-to-input-current or reverse current transfer function
T_oic	Output-to-input-current transfer function of an impedance block
T_s	Switching cycle
$\mathbf{U}$	Laplace transformed input variable vector
U_D	Diode forward voltage drop
U_E	Equivalent voltage
U_in	Averaged input voltage
U_o	Averaged output voltage
$\mathbf{u}$	Input variable vector
$\hat{u}_\mathrm{co}$	Perturbed control voltage
$\hat{u}_\mathrm{in}$	Perturbed input voltage
$\hat{u}_\mathrm{inc}$	Perturbed input voltage of an impedance block
$\hat{u}_\mathrm{inL}$	Perturbed input voltage of subsystem **L**
$\hat{u}_\mathrm{ins}$	Perturbed input voltage of a non-ideal voltage source
$\hat{u}_\mathrm{inS}$	Perturbed input voltage of subsystem **S**
$\hat{u}_\mathrm{o}$	Perturbed output voltage
$\hat{u}_\mathrm{oc}$	Perturbed output voltage of an impedance block
$\hat{u}_\mathrm{oL}$	Perturbed output voltage of subsystem **L**
$\hat{u}_\mathrm{oS}$	Perturbed output voltage of subsystem **S**
$\hat{u}_\mathrm{T}$	Perturbed voltage of Thevenin's equivalent voltage source
V_m	Peak-to-peak amplitude of a constant sawtooth-ramp signal
$\mathbf{X}$	Laplace transformed state-variable vector
$\mathbf{x}$	State-variable vector
$\mathbf{Y}$	Laplace transformed output-variable vector
Y_in	Input admittance
Y_inc	Input admittance of an impedance block
$Y_\mathrm{in-sc}$	Short-circuit input admittance
$Y_\mathrm{in-\infty}$	Ideal input admittance
$\mathbf{y}$	Output-variable vector
Z_in	Input impedance (i.e., $1/Y_\mathrm{in}$)
Z_inc	Input impedance of an impedance block (i.e., $1/Y_\mathrm{inc}$)
$Z_\mathrm{in-sc}$	Short-circuit input impedance (i.e., $1/Y_\mathrm{in-sc}$)
$Z_\mathrm{in-\infty}$	Ideal input impedance (i.e., $1/Y_\mathrm{in-\infty}$)
Z_L	Load impedance
Z_N	Impedance of Norton's equivalent current source
Z_o	Output impedance
Z_oc	Output impedance of an impedance block
Z_of	Output impedance of an EMI filter
Z_s	Source impedance

Z_T	Impedance of Thevenenin's equivalent voltage source
ϕ	Phase angle
°	Degree

Subscripts

-c	closed-loop transfer function
-L	Refers to load side
-o	open-loop transfer function
-S	Refers to source side
dB	Refers to decibels

Superscripts

c	Refers to impedance block
L	Load-affected transfer function
RS	Refers to remote sensing
S	Source-affected transfer function
ss	Refers to state space

Abbreviations

AC-DC	AC-to-DC conversion
ACM	Average current mode
CCM	Continuous conduction mode
CM	Current mode
DC	Direct current
DC-DC	DC-to-DC conversion
DCM	Discontinuous conduction mode
EET	Extra element theorem
EMI	Electromagnetic interference
IBA	Intermediate bus architecture
IVFF	Input-voltage feedforward
LTI	Linear time invariant
MIMO	Multi-input multi-output
OCF	Output-current feedforward
PCM	Peak-current mode
PCMC	Peak-current-mode control
PCMC-OCF	Peak-current-mode control with output-current feedforward
POL	Point of load
PWM	Pulse-width modulation
RHP	Right-hand plane
SISO	Single-input single-output
SSA	State-space averaging
VM	Voltage mode
VMC	Voltage-mode control

1 Introduction

This chapter presents the essential background of the thesis and explains the motivation for conducting the research. The prevailing methods and ideas proposed by other researchers to model and analyze switched-mode converters and the systems composing of them are overviewed briefly. Finally, the structure, objectives and the scientific contribution of the thesis are stated.

1.1 Overview of DC-DC Power Supply Systems

Efficient and reliable conversion of electric power from distribution network or other sources such as solar arrays to a variety of DC electric loads has become more and more important in ensuring the functioning of modern society. The rapid evolution of power electronics and development of semi-conductors have enabled more sophisticated methods to performing the necessary conversion [1]. Consequently, the high-frequency switched-mode converters have substituted the linear regulators – commonly used earlier in implementing the conversion – with improved efficiency and reduced space and weight. A multitude of topologies and control methods have been developed for the AC-DC and DC-DC conversions, especially for telecommunication, automotive and information technology applications during the past decades [2]–[4].

Modern electric loads usually require multiple different voltages ranging from 15 V to 1 V or even lower [2]. In addition, the current levels and the rate of change of currents that the loads draw are increasing [5]: For example, the load current of a modern microprocessor can change from 0 A to over 100 A within a few tens of nanoseconds while allowing only 100-mV voltage deviation at the point of load [6]. These kinds of requirements have made the design of switched-mode converters and power supply systems extremely challenging and prone to dynamic problems.

During the past two decades, distributed architectures have substituted the traditional centralized power system architectures, where the rectified mains voltage is converted into multiple different load voltages directly by a single DC-DC converter [2]–[4], [7]–[11]. In the distributed systems, multiple conversion stages are used instead of one to produce the point-of-load voltages. Fig. 1.1 shows the typical configuration of a distributed system based on intermediate bus architecture (IBA) [2], where a front-end rectifier supplies an isolated bus converter, which in turn supplies multiple point-of-load (POL) converters via the distribution bus.

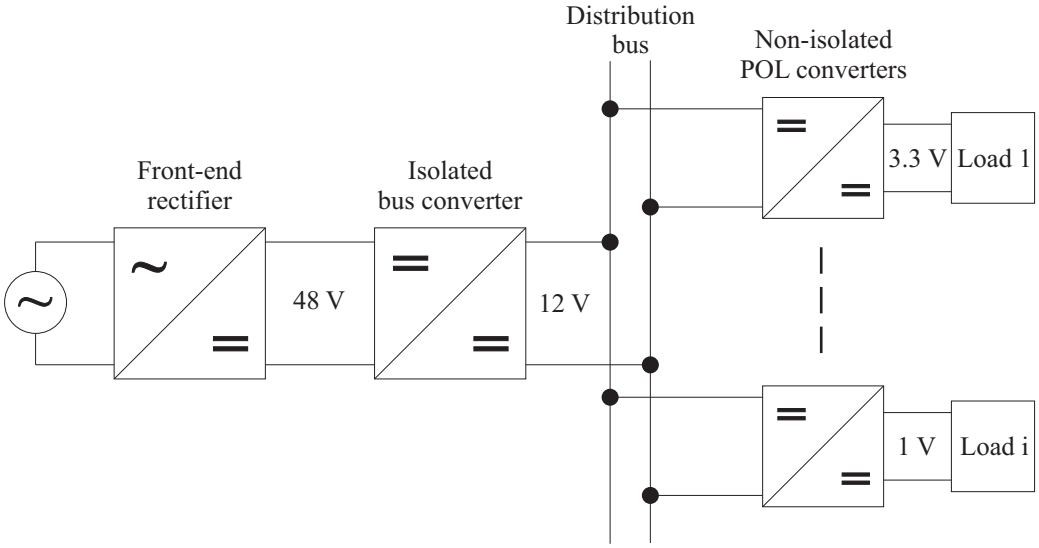


Fig. 1.1 *A distributed power supply system based on intermediate bus architecture.*

The bus converter is used to provide isolation and to convert the rectified voltage (e.g. 48 V) to a lower voltage level such as 12 V. The bus converter can be fully regulated, semi-regulated or even unregulated depending on the requirements set for the bus voltage accuracy [2], [8]. If the bus voltage is used only to power other POL converters, the requirements can be loosened substantially and the cost of the bus converter can be reduced by omitting the feedback control circuitry. The unregulated bus converter operates at fixed duty-ratio and, consequently, does not provide either line or load regulation. The semi-regulated bus converter usually regulates the variations in the rectified voltage adequately, but does not provide load regulation [9]. The POL converters within the IBA system are used to convert the bus voltage to actual loads with tight line and load regulation. The POL converters are usually non-isolated to reduce cost and to increase efficiency. The IBA system can also contain a storage battery connected in parallel with the front-end rectifier and additional EMI filters at the input of converters.

The use of distributed systems seems to be very easy due to the modular structure, and therefore they are an attractive choice for system designers. However, their design processes are not easy and straightforward despite the many advantages they provide over the centralized systems. Many design issues such as power and voltage coordination, beat frequencies and impedance interactions between the converters need to be carefully considered [12]. The individual converters used in distributed systems are usually commercial power supply modules designed for general usage. Their control systems are designed to be stable and to provide excellent transient dynamics in stand-alone operation with the laboratory supplies and loads. This means that their transient dynamics and stability in the final system are not necessarily guaranteed, when the converter modules are connected in cascade and/or in parallel as an interconnected system.

The analysis and design methods of the interconnected power supply systems have been widely discussed in public and scientific literature during the past two decades. Different converter topologies and optimal bus voltages to implement the systems as well as methods to analyze their stability and performance degradation are proposed and discussed widely. This thesis concentrates on the methods to analyze the interactions taking place in the systems and proposes actions with which those interactions can be eliminated or substantially reduced. The theoretical formulation used in the analyses is general in nature and, therefore, applicable to any electrical device or system. However, the theory is applied only to DC-DC voltage converters and DC-DC distributed power systems in this thesis.

1.2 Overview of Existing Methods to Model Converters and Systems

The foundation for power-supply-system modeling and analysis is the appropriate modeling of switched-mode converters, which originates from the mid 1970s, when Dr. Middlebrook and Dr. Ćuk developed the state-space averaging (SSA) technique and the canonical equivalent circuits [13], [14] for the direct-duty-cycle or voltage-mode (VM) controlled converters. In SSA, the circuit equations representing the dynamics of a fixed-switching-frequency converter during the different sub-cycles are averaged over one switching cycle yielding a non-linear averaged model. The model is usually linearized by developing the proper partial derivatives to obtain linear-time-invariant (LTI) small-signal models. Therefore, the extensive variety of mathematical methods developed for LTI systems can be utilized. The method is shown to give accurate models up to half of the switching frequency in continuous conduction mode (CCM) [15]. The SSA method was also modified to model the discontinuous conduction mode (DCM) with additional constraints [16], which resulted in reduced-order models predicting only the low-frequency behavior correctly [15]. Different methods to develop full-order models for the DCM operation exist as discussed in [17]. Since the seminal work done by Middlebrook and Ćuk, there have been wide discussions concerning the modeling of switched-mode converters. A comprehensive overview of different modeling techniques such as the large-signal averaging and the sampled-data modeling can be found in [18].

Typically, the switched-mode converters are modeled by using resistive loads [14], [19], which results in load-affected dynamic models. The practical loads are very seldom resistors as depicted in Fig. 1.1 and, therefore, the actual dynamic representation should be that both the load and the source effects are removed [20]–[22]. This means that the analytical modeling and experimental frequency-response measurements should be made by using an ideal constant-current sink as a load and an ideal constant-voltage source as a source [22]. The load and source effects can be removed computationally by applying the methods given, e.g., in [22].

The use of linear two-port networks [22]–[25] may be the most consistent and practical way to analyze large power supply systems containing multiple switched-mode converters and other system elements. In the two-port representation with the modified g-parameters [25], a switched-mode voltage converter is represented with Norton's equivalent current source as its input port and Thevenin's equivalent voltage source as its output port [22], as illustrated in Fig. 1.2 inside the dashed line. Similarly, other electrical subsystems such as EMI filters, loads and other passive components can be represented by similar two-port networks. Consequently, a large system can be divided into smaller subsystems and the interactions caused by the subsystems can be solved by applying basic circuit theory as explained in [22] and [26]–[28].

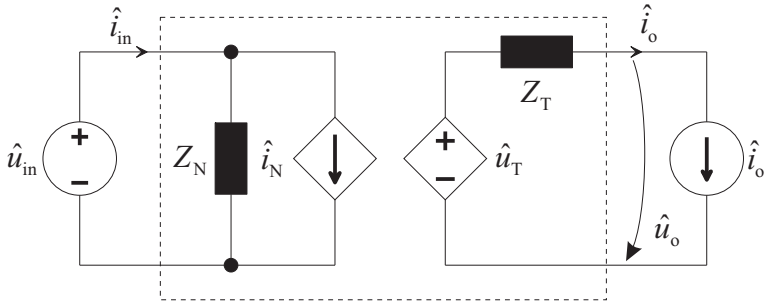


Fig. 1.2 *A general two-port network with Norton's equivalent current source (Z_N , $\hat{j}_N$) as its input port and Thevenin's equivalent voltage source ($\hat{u}_T$, Z_T) as its output port.*

Recently, a concept of dynamic profile [26], [29] has been introduced to uniformly characterize the different types of switched-mode converters based on the small-signal transfer functions constituting the g-parameter set at open and closed loop as discussed above. In addition to the six open-loop transfer functions, two special input admittances are defined based on the transfer functions. These two sets form the foundation for understanding the dynamics of the converter, designing their feedback controllers, and analyzing the external interactions caused by the impedances in the other source and load subsystems. The applicability and usefulness of the different control methods such as voltage-mode, peak-current-mode (PCM), and average-current-mode (ACM) control can be compared by studying the changes the control methods cause in the corresponding dynamic profile. On the other hand, the dynamic profile can be utilized to point out or reveal the vital elements or factors in the profile with which the beneficial consequences such as source and load invariance [27], [28] can be achieved. The invariance means that the load and source impedances do not change the converter dynamics from the nominal or internal dynamics.

The methods to analyze stability and dynamic performance of power supply systems have evolved simultaneously with modeling techniques of the individual switched-mode converters. Middlebrook introduced the concept of minor-loop gain in the 1970s, when developing the EMI-filter-design rules for a switched-mode converter [30], [31]. Actually, an EMI filter and a switched-mode converter form a cascaded system.

Therefore, it is natural that the design rules and analysis methods applied for the EMI-filter design are also applicable for the other interconnected systems. The basic analysis tool, which Middlebrook developed, is known as the minor-loop gain constituting of the ratio of the output impedance of the source subsystem and the input impedance of the load subsystem. It is stated in [30] that the minor-loop gain must satisfy the Nyquist stability criterion [32] for the cascaded system to be stable. Actually, Middlebrook did not prove scientifically that the minor-loop gain contains the desired information on the stability of the cascaded system. That was later proved in [33]. Middlebrook also presented additional criteria, which are more restrictive than the stability criterion that needs to be satisfied in order to ensure that the transient dynamics remain unaffected. In [30], he introduced a practical design rule by a region in the complex plane in which the minor-loop gain should stay for stability and good transient performance. This region is defined as a circle having radius equal to the inverse of a certain gain margin, i.e., the radius has to be sufficiently less than unity. This will ensure stability for sure, but it does not necessarily guarantee that the transient performance of the converter is unaffected, if the margin is too small. The stability of the converter with an EMI filter can be easily evaluated with the minor-loop gain, but the performance degradation can not be analyzed without more detailed information of the inner properties of the converter.

Before proceeding further with the overview of the system-level analysis, the terms stability and performance are discussed briefly. There are a number of ways to determine the stability of a feedback system. Applying the Nyquist stability criterion for different loop gains within the converters and systems may be the most convenient way to determine stability. The terms phase and gain margins – PM and GM – are used to measure the relative stability of feedback systems in control theory [32] and are therefore important parameters in defining the level or robustness of stability. Similarly, the phase and gain margins are used to define the relative stability of different minor-loop gains.

The performance of a feedback system can also be evaluated in different ways depending on the type or purpose of the system. Usually, the reference signal of a switched-mode converter is kept constant and it may even be unavailable as physical input. Therefore, the time (i.e., transient dynamics) and frequency-domain (i.e., disturbance rejection) methods can only be applied to the input and output of the converter containing information both on the feedback loop and the internal open-loop dynamics related to the corresponding variables [32], [34]. In this thesis, the term performance means the transient dynamics and disturbance rejection of a system. However, the requirements for adequate transient dynamics and/or disturbance rejection can vary from one application to another, and therefore it is difficult to define the term performance explicitly. Consequently, if the converter is originally designed to have adequate performance and that is verified by laboratory experiments, then the application of the converter as a subsystem is assumed not to change the overall

performance from the original too much. The reality is, however, that the performance of the individual converters can change and it usually deteriorates due to impedance interactions.

The minor-loop gain can be utilized more generally in the stability analyses than its application in the EMI-filter design may imply [30], [31]. It can be equally used to study the stability of a large system at an arbitrary interface between two general subsystems [23], [33], [35]. In power supply systems based on the IBA concept, the common practice seems to be to define the minor-loop gain at the interface between the bus converter and POL converters [36]–[40]. Hence, the analysis concerns the bus converter. Although the criterion for system stability is well treated in literature, there seems to be a number of viewpoints for the relative stability and performance degradation of the converters and systems based on the information obtainable from the minor-loop gain. As a result, different forbidden regions have been developed, out of which the minor-loop gain should stay to ensure stability and adequate performance. Middlebrook's forbidden region does not allow impedances at the interface to overlap (i.e., the resulting minor-loop gain is required to stay inside a circle that has radius equal to the inverse of gain margin at origin), which is usually considered to be too restrictive and conservative. Therefore, other forbidden regions have been defined, which allow the impedances to overlap with certain restrictions. A variety of such regions are defined, such as *GMPM* [36], [37], *opposing argument* [38], [39] and *ESAC* [41], [42] regions based on the different argumentations or criteria as illustrated in Fig. 1.3. A comprehensive summary of the existing forbidden-region-based criterions can be found in [43], where also a new criterion is proposed based on the allowed peaking of a complementary sensitivity function defined by the minor-loop gain.

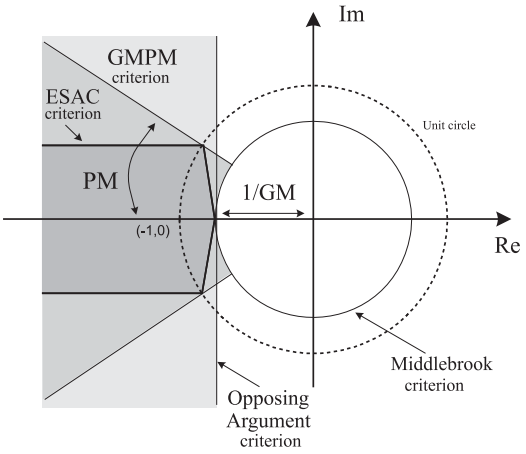


Fig. 1.3 *Different forbidden regions developed for the minor-loop gain.*

The forbidden region defined by Middlebrook [30] is the area outside the circle with the radius $1/GM$. The opposing argument criterion defines the forbidden region to be left of the vertical line at $-1/GM$ on the real axis. The GMPM criterion [37] defines the forbidden region as an area formed by the intersection of Middlebrook's criterion and

two sectors defined by the phase margins and the negative portion of the real axis. The ESAC criterion [42] also defines the forbidden region by the gain and phase margins occupying less space in the complex plane than the corresponding GMPM criterion, as shown in Fig 1.3. The ESAC criterion is declared to be insensitive to component grouping within the system, which actually means that the minor-loop gain defines the stability regardless of the interface at which it has been defined. However, the discussions in [42] concentrate only on stability analysis and do not consider the possible performance degradation at all even if the gain and phase margins clearly have a role in the definition of the forbidden region. It should be pointed out that the minor-loop gain defined at different interfaces within the system will have different stability margins as briefly discussed in [42]. Hence, a question arises: what are the key interfaces and what should the margins be in order to ensure robust stability, adequate transient performance and input-voltage noise rejection of the converters within the system? The common practice seems to be to use the same margins that are typical for the voltage-loop gain, i.e., the phase margin of 60 degrees and gain margin of 6 dB [37], [38], [40].

It should be pointed out that the goal of Middlebrook's forbidden region is to ensure both stability and also adequate performance, whereas the ESAC and opposing argument criterions are derived to ensure stability with certain phase and gain margins, without considering the performance degradation. Only in [36], the relation between the gain and phase margins of the load-side minor-loop gain and the peaking of certain transfer functions of the corresponding converter are analyzed. However, the analysis is not extended to other frequencies than those where the phase and gain margins are determined and therefore the obtained design rules are actually incomplete. Although the system stability is a very important aspect, the lack of discussion on the performance degradation is difficult to understand because of the stringent supply-voltage-accuracy requirements [6].

In [44], the load interactions are discussed for a specific type of converters with the assumption that the load is a negative resistor, which is usually only a good approximation of the input impedance of a regulated converter at low frequencies. Therefore, the analysis results are not general and can not be generalized. In [36], the load interactions are treated based on the minor-loop gain defined at the output of a converter. An equation is derived to analyze the effect of a load on the internal voltage loop of the loaded converter including the minor-loop gain. However, some of the conclusions are vague and can not be generalized directly. Another group of researchers [45]–[47] have also derived the same equation for the load-affected voltage-loop gain of a converter as a function of the minor-loop gain defined at the output of the converter. Similarly, as in [36], the same incomplete conclusions are made. Some of the vagueness of [36] is corrected in [48], where it is also claimed that the minor-loop gain directly determines the crossover frequency and phase margin of the load-affected voltage-loop gain. However, this is not evident based on the experimental results provided in [48].

The seminal work reported in [30] is the basis for the source interaction analysis for converters under voltage-mode control (VMC) in CCM. Middlebrook's analysis method is extended to the current-mode-controlled converters in [49]–[51] by applying the two-port representations based on the y-parameters [25] for converters that have the current loop closed and outer voltage loop open. The converter operates then at open loop. It was noticed in the experiments in [49] that the traditional design rules did not give the expected results regarding to the stability of the converter. The reason for that was however not found. Later in [52] it was shown that the increased attenuation of the input-to-output transfer function caused the unexpected behavior of the converter. A general formulation to analyze the source interactions on converter dynamics is given in [22] without the restrictions of [30] and [49]–[51].

The authors of [53] propose an experimental method to analyze performance degradation under the influence of arbitrary source impedance. Basically, the equations characterizing the influence are the same as defined in [30], but the method is applied to a system consisting of a PCM-controlled converter that has internal and external input filters. The analyses are done at the interface between the two filters and not at the actual input of the switched-mode converter. Therefore, the validity and meaning of the obtained results are not clear. In [54] and [55], the formulation to analyze source interactions is derived by the extra element theorem (EET) [56], which naturally complies with the formulation presented in [22] and [53]. However, the experimental evidence is provided in [55] with VM and PCM-controlled boost converters, which are modeled with resistitive load and, therefore, the true internal dynamics of the converters are not discussed. Similarly, the analyses are done with PCM-controlled buck converters in [53] and [54] without considering the effect of the slope of the compensation ramp used in duty-cycle generation. The slope is known to affect the level of source interactions substantially.

A common deficiency of contemporary methods to analyze and predict accurately the load and source interactions on the dynamics of a converter is that information on the inner properties of the converters is lacking. The power supply manufacturers do not usually provide such information and the measurement of the required open-loop or special transfer functions is usually impossible to make afterwards. There are, however, methods with which the internal dynamics of a switched-mode converter can be made deterministic and their interaction sensitivity can be reduced [57]. Consequently, the use of such converters would also make the system behavior deterministic and its analysis more accurate and also straightforward. The application of these methods has to be done in the design phase of converters and, hence, can not be applied to commercial converter modules afterwards.

The stability analysis and performance prediction are vital tasks in the design of efficient, reliable and competent interconnected power supply systems. One can always choose the analysis method which fits best for a certain design phase. It is important

that the formalism or the analytical equations the method provides are general, easy to apply and explicitly provide the necessary information. The approach to treating the converters and systems used in this thesis is based on the dynamic profile introduced in [26] and the two-port linear model characterized by g-parameters [25], which together provide a powerful tool for the intended usage.

1.3 Control of Switched-Mode Converters

Commonly, switched-mode converters need to be equipped with feedback circuitry to precisely control the output variable at the predefined value (i.e., usually output voltage or current) under different disturbances constantly affecting the operation of the converters. Basically, the feedback from the regulated variable is provided with an error amplifier constituting the controller. The design of the controller determines the basic control dynamics, i.e., the crossover frequency and the phase and gain margins of the feedback loop. In reality, controller design has its limitations in terms of robustness of stability and transient dynamics, which are determined by the internal dynamics of the associated converter. The external interactions affect the converter via open-loop parameters and can change its dynamics despite perfect controller design. Therefore, the rest of this section mainly concentrates on the open-loop internal dynamics of voltage-output converters and the methods to change them for obtaining beneficial effects for preserving the designed control dynamics. In the end of the section, the output-voltage remote sensing is briefly covered because of the surprising effects it can provide.

The most basic control method is known as direct duty-cycle or voltage-mode control. The duty-cycle generation under VMC is established by comparing the control signal to a constant ramp signal repeating at the switching frequency [19]. Characteristic to the dynamics of the VM-controlled converter is its resonant nature in CCM [14], which actually makes the converter sensitive to the source and load interactions [30]. The DCM operation damps the resonances and makes the converter somewhat more insensitive to the interactions [26]. The implementation of the control mode is easy and cost effective. It usually provides fast response to load current disturbances. Therefore, the POL converters are usually VM-controlled buck converters.

Peak-current-mode control (PCMC) was introduced in the late 1970s [58]. In PCMC, the ramp signal in the duty-cycle generation is made proportional to the up slope of the inductor current or to the up slope of sum of many inductor currents. This changes the dynamics of the converter profoundly, i.e., the converter behaves as a current source at open loop and the resonances characteristic to the VMC operation are totally or partially damped depending on the order of the converter and the type of the inductor current feedback. The first attempt to model the dynamics of the PCM-controlled converter was introduced in [59]. Since then, there have been numerous attempts to accurately model the dynamics of current-mode-controlled converters. However, no generally accepted modeling method exists yet. The model presented in [60] and [61] is based on an idea that the origin of the peculiar behavior observed in the PCM-controlled converter is

resonance taken place at half the switching frequency due to the sampling of the inductor current. Commonly, these models are considered to be the most accurate models although their accuracy has been argued [62]. Another method is introduced in [63], where the small-signal model of the VM-controlled converter is modified by replacing the perturbed duty-ratio with the duty-ratio constraints derived from the inductor-current waveforms to obtain the state space representation of the corresponding PCM-controlled converter. This modeling method is applied in the thesis.

The main advantages of the PCMC are the cycle-by-cycle current limiting of the active switches, greatly increased input-voltage noise attenuation as well as first-order control dynamics. The load transient response of the PCM-controlled converter is typically slower than the response of the corresponding VM-controlled converter [28] due to rather high low-frequency open-loop output impedance. Characteristic to PCMC is also the limited duty-ratio range, which can be extended with a proper compensation of the feedback current signal [63]. When the slope of the compensation ramp is made equal to a certain value in a PCM-controlled buck converter, the input-to-output voltage transfer function (i.e., audiosusceptibility) can theoretically become zero yielding perfect input-voltage-noise attenuation and invariance to source interactions [57].

In control theory, a typical way of improving the system dynamics is using feedforward from the disturbance or input variables in addition to the feedback from the regulated variable [32]. For a voltage-output switched-mode converter, the disturbance variables are the input voltage and output current. Actually, the goal of applying the feedforward from the input voltage and output current is to obtain zero open-loop input-to-output voltage transfer function and output impedance. The research on the feedforward schemes for the switched-mode converters started in the 1970s and it was observed that the use of input-voltage feedforward (IVFF) can substantially ease the EMI-filter design [64]. The feedforward schemes for the current-mode-controlled buck converter are introduced and discussed in [65]. It is stated that the hysteretic-current-mode-controlled converter provides inherently perfect IVFF and the load-transient behavior can be significantly improved by using unity feedforward from the output current.

The ideal IVFF gains that yield nearly zero input-to-output transfer function at low frequencies are derived explicitly in [66] for basic buck, boost and buck-boost topologies and in [67] also for topologies having quadratic conversion ratios. Different pulse-width modulation techniques to implement the IVFF are discussed in [68]–[72]. In a VM-controlled buck converter, the IVFF control can be implemented by making the PWM ramp signal proportional to the input voltage [68]. In a boost converter, the ramp signal is made proportional to the control voltage, which is compared to the scaled input voltage [70].

The application of IVFF and PCM controls can significantly ease the design of distributed systems by providing deterministic input impedance of the converter and

immunity to the source interactions as discussed in [57]. Characteristic of IVFF control is that it maintains the small-signal output dynamics identical to VMC. There are, however, several aspects such as the limited duty ratio, which can deteriorate the expected dynamic improvements, if not carefully considered [73].

As demonstrated in [65], the proper output-current feedforward (OCF) can significantly improve the load transient response. Basically, the OCF control is implemented by summing a signal proportional to the output current with the control signal produced by the feedback controller. Therefore, the changes in the output current instantaneously affect the duty ratio. Dynamically, this is reflected as a significantly reduced open-loop output impedance [74], [75]. It is claimed in [75], that the zero output impedance can be implemented in every converter by means of the OCF control, but the claim is not true, because some of the converters would require using feedforward gains with unstable poles. The experimental evidence provided in the paper is based only on the use of buck-type converter, which actually implies the deficiency of the theoretical treatment.

In [74], the effect of OCF control is theoretically analyzed for the PCM-controlled converter by using the unity-gain-feedforward scheme proposed in [65], i.e., the measured output-current-based signal is directly used without any additional compensators in the feedforward loop. In principle, the conclusions presented in [74] are correct, but the open-loop output impedance of the OCF-controlled converter is never the same as the output impedance of the corresponding VM-controlled converter as shown in [76]. The implementation of the OCF control in a boost converter is treated in [77] and [78]. It is shown that the OCF control produces a slight improvement in the load-transient response. However, the zero output impedance can not be obtained in a boost converter by using the OCF control method as described above, because of the non-minimum phase nature of the converter [76]. The technique proposed in [77] and [78] actually utilizes a non-linear control technique, where the feedforward scheme contains feedforward from the input voltage and the output current as well as feedback from the output voltage.

The open-loop output impedance of the VM-controlled converter is known to be small except at the vicinity of the resonant frequency [19]. When the same resonance also affects the voltage-loop gain, the closed-loop output impedance is quite small. A method to improve the load-transient response of a VM-controlled buck converter is reported in [79] based on the use of a current transformer. However, the current transformer only provides information on the transients of the output current and, therefore, the zero output impedance can not be implemented. The paper treats the optimum design of the transformer by minimizing the integral of output-voltage squared error and does not discuss the zero output impedance conditions. The experimental responses show clear improvements in the load-transient response, but the sensitivity of the frequency-domain dynamics on the operating point, current transformer parameters, and power-stage component variations are not analyzed.

It is claimed in [80], that the feedforward from the output current is not actually feedforward when the load resistor is included in the model of the converter, because the control-to-output transfer function is affected by the feedforward signal. The conclusion is, however, misleading, because the control-to-output transfer function changes due to the load interactions and not due to the feedforward. In [81] and [82], the authors introduce methods with which the closed-loop output impedance can be designed to be a pure resistance by applying direct output-current feedforward. According to [82], the required feedforward gain for the VM-controlled buck converter is a high-pass filter and for the PCM-controlled buck converter a low-pass filter, respectively, where the filter elements are the inductor and output capacitor of the converter and the derived resistor. The OCF is used to improve the load transient response of a power-factor-correction boost converter under ACM in [83], where also the ideal OCF gain is derived for steady-state operation.

Significant improvements in the input-voltage-noise attenuation of a buck converter can be obtained by applying either IVFF or PCM control. The operation-point dependent maximum duty ratio caused by the application of IVFF control leads to a significant reduction in the load-transient dynamics [57]. This means that the technique may not be feasible to apply in the practical converter even if significant improvements in the source interactions can be obtained. The PCM-controlled buck converter with optimal compensation and unity-output-current feedforward can provide both high source and load invariance as well as improved load transient dynamics [76].

The switched-mode converters are sometimes equipped with remote sensing terminals. These terminals are used to alternatively take the output-voltage feedback directly from the output of the converter or from the point of load (e.g., from inside a microprocessor). The remote sensing, when connected into the load terminals, can introduce an additional impedance network (e.g., due to cabling and capacitor banks) inside the feedback loop. Consequently, the dynamics of the converter can change and deteriorate significantly, if not carefully considered and analyzed. The use of remote sensing is obvious in many publications such as [84]–[86] and [89]. The explicit formulation to completely analyze the effects of remote sensing on the internal dynamics of converters is not, however, presented in literature. A stability analysis tool is proposed in [85] and [86], where the use of remote sensing is clear and its effect on voltage loop gain is calculated. However, the methods to analyze its effect on the other parameters characterizing the dynamics of a switched-mode converter such as input-to-output transfer function, input impedance and short-circuit input impedance are not presented. Therefore, the real characteristics and importance of the application of remote sensing is not known.

1.4 Structure of the Thesis

In addition to the introduction presented in Chapter 1, the thesis contains 4 chapters, which are summarized as follows:

In Chapter 2, the basic formalism to model individual converter at open and closed loop and to analyze load and source interactions are presented. The effects of different control methods as well as the output-voltage remote sensing on the dynamic profile of a converter are derived via the consistent formalism. The interaction formalism of arbitrary cascaded systems is presented.

In Chapter 3, theoretical and experimental system-level interaction analyses are presented. Stability as well as performance degradation of the systems and individual converters are discussed under load and source interactions. The chapter reviews the key findings of [P1], [P2] and certain items presented in previous publications by other authors. It is shown that the minor-loop gain contains information on stability, but does not necessarily contain information about performance degradation and robustness of stability. Hence, the usefulness of the minor-loop-gain-based forbidden region criteria in interaction analysis is argued. The effect of output-voltage remote sensing on stability and performance is discussed in view of [P3].

In Chapter 4, the techniques with which the interactions can be reduced are discussed. It is shown based on the theoretical and practical evidence presented in [P4]–[P6] that the proper control methods and feedforward schemes facilitate the system design significantly by reducing the possible interactions and performance degradation and, therefore, making the system design more deterministic. The PCM-controlled fourth-order step-down converter known as superbuck introduced in [P7] is used to contrast the possible peculiar dynamics of a higher-order converter with the conventional buck converter.

Chapter 5 concludes and summarizes the thesis. Short summaries of the publications [P1]–[P7] are presented. Final conclusions and the scientific contribution of the thesis are recapitulated and future topics are discussed.

1.5 Objectives and Contribution of the Thesis

The history of the dynamic analyses of interconnected regulated systems dates back to the 1970s, when Middlebrook developed the SSA method for individual converters [13] and the input-filter-design rules including the minor-loop gain concept for the cascaded system [30],[31]. More than thirty years have elapsed with a multitude of publications covering the dynamic issues, but a full understanding of them still seems to be missing. Therefore, the main objective of the thesis is to show that the minor-loop gain contains information only on the stability of the interconnected system but not much information on the robustness of the stability and the interactions taken place inside the regulated

converters. The presented forbidden regions constructed by using the phase and gain margins may turn out to be useless, when the adequate load-transient response has to be guaranteed and the variety of different interfaces within the system are considered. As a consequence of this, the second objective of the thesis is to introduce techniques with which the interactions can be reduced and the design can be made more deterministic.

The thesis utilizes and extends the concept of dynamic profile introduced in [26] and the two-port networks [25] in the modeling and interaction analyses. The same consistent formalism is used throughout the publications [P1]–[P7].

The main scientific contribution of the thesis can be briefly summarized as follows:

- It is shown that minor-loop gains can be used to determine the stability of systems but not necessarily to quarantee adequate performance.

- A criterion is derived for the minor-loop gain with its sensitivity function to prevent excess peaking of various closed-loop transfer functions of a converter.

- It is shown that the inverse relation between the load-side minor-loop gain and the voltage-loop gain of the corresponding converter holds only at frequencies where the magnitude of the voltage-loop gain is very high.

- It is shown that the performance degradation of a converter due to source interactions can be accurately analyzed only with certain input admittances of the converter and not with the minor-loop gain.

- Comprehensive formulation is derived to analyze the effect of output-voltage remote sensing on converter dynamics.

- Theoretical basis for obtaining source and load invariance is established. It is shown experimentally that the theoretical findings hold also in practice.

- The concept of ideal reverse current transfer function is introduced. It is shown to be an important parameter in defining the ideality of the output-current feedforward.

2 Dynamic Modeling and Analysis Formalism

In this chapter, the formalism to uniformly characterize and analyze the voltage-input voltage-output DC-DC converters and the systems based on them is briefly introduced. The characterization process is reviewed based on the dynamic profile of a switched-mode converter and general two-port networks at open and closed loop. The interaction formalisms to analyze the effects of arbitrary source and load impedances as well as the effect of the output-voltage remote sensing on the converter dynamics are reviewed. The effects of different control methods–i.e., VM, PCM, IVFF and OCF-control–on the dynamic profile are discussed. Finally, the general system-level analysis method of cascaded systems is reviewed and discussed.

2.1 Characterizing Switched-Mode Converters

The switched-mode converters are non-linear in nature due to the rapid switching between different subcircuits within one switching cycle and due to the use of non-linear components such as diodes and MOSFETs. The dynamic modeling is usually done by applying state-space averaging technique described in [14], which is directly applicable only under direct duty-cycle or VM control in CCM. Modeling of DCM operation requires the use of different approaches as explained in detail in [17], [87]. However, the resulting average models are still non-linear and, therefore, they are typically linearized at the desired operation point by developing the proper partial derivatives yielding linear small-signal models, which describe the mappings between the input, output and state variables.

In general, a linear model can be expressed in state-space form shown in (2.1), where $\mathbf{x}(t)$ is a state-variable vector, $\mathbf{u}(t)$ is an input-variable vector and $\mathbf{y}(t)$ is an output-variable vector. The dot over the state-variable vector in the upper equation in (2.1) represents the time derivative of $\mathbf{x}(t)$. The matrixes $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ are coefficient matrixes defining the mappings between the variables at the desired operation point.

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \end{aligned} \tag{2.1}$$

The mapping from the input variables to the output variables can be solved from (2.1) by expressing it in frequency domain by means of Laplace transformation and using basic matrix algebra. That gives (2.2), where $\mathbf{G}$ represents the transfer function matrix from the input variables $\mathbf{U}(s)$ to the output variables $\mathbf{Y}(s)$. The matrix $(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B}$ in (2.2) represents the mapping from the input variables to the state variables $\mathbf{X}(s)$.

$$\mathbf{Y}(s)=\left(\mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B}+\mathbf{D}\right)\mathbf{U}(s)=\mathbf{G}\mathbf{U}(s) \tag{2.2}$$

The physical signals of the memory elements, i.e., the currents of inductors and the voltages of capacitors, are typically taken as the state variables in (2.1). The natural input variables are input voltage $\hat{u}_{\mathrm{in}}$, output current $\hat{i}_{\mathrm{o}}$ and control signal $\hat{c}$. Similarly, the natural output variables are input current $\hat{i}_{\mathrm{in}}$ and output voltage $\hat{u}_{\mathrm{o}}$ [25], [26]. At open loop (i.e., without any feedback of the output voltage), the control signal $\hat{c}$ typically represents the duty ratio $\hat{d}$ (i.e., under VMC) or control current $\hat{i}_{\mathrm{co}}$ (i.e., under PCMC). At closed loop (i.e., when the feedback from the output voltage is used to control the converter), the control signal represents the appropriate reference signal for the control system.

2.1.1 Dynamic Profile

Eq. (2.2) can be expressed as shown in (2.3). The input and output variables as well as the transfer functions are functions of the Laplace variable *s*, which is omitted here for brevity. The set of transfer-functions in (2.3) is known as the modified g-parameter set [25], [27]. The use of g-parameters is advantageous, because they can be proven to always exist for linear systems [25]. The minus sign in front of Z_{o} in (2.3) represents the true physical direction of the output current flowing out of a converter. According to the original g-parameter set [25], the direction of the current would be into the converter. Therefore, the word "modified" is used to distinguish the sets from each other.

$$\begin{bmatrix}\hat{i}_{\mathrm{in}}\\ \hat{u}_{\mathrm{o}}\end{bmatrix}=\begin{bmatrix}Y_{\mathrm{in}} & T_{\mathrm{oi}} & G_{\mathrm{ci}}\\ G_{\mathrm{io}} & -Z_{\mathrm{o}} & G_{\mathrm{co}}\end{bmatrix}\begin{bmatrix}\hat{u}_{\mathrm{in}}\\ \hat{i}_{\mathrm{o}}\\ \hat{c}\end{bmatrix} \tag{2.3}$$

The bottom row of the transfer function matrix in (2.3) describes the output dynamics. Similarly, the upper row in (2.3) describes the input dynamics. The output dynamics are determined by forward or input-to-output-voltage transfer function G_{io}, output impedance Z_{o} and control-to-output-voltage transfer function G_{co}. The transfer functions determining the input dynamics are input admittance Y_{in}, reverse or output-to-input-current transfer function T_{oi} and control-to-input-current transfer function G_{ci}. In this thesis, subscripts "-o" and "-c" are used to distinguish the open and closed-loop transfer functions: For example, the open-loop output impedance is $Z_{\mathrm{o-o}}$ and the corresponding closed-loop output impedance is $Z_{\mathrm{o-c}}$.

The voltage-output converters are intended to regulate their output voltage at constant level. Therefore, the reference signal for the feedback system is usually kept constant, i.e., $\hat{c}=0$. As a result, the closed-loop operation can be described solely by four transfer functions and, consequently, G_{ci} and G_{co} are omitted in (2.3) for the closed-loop g-parameter set. Consequently, the subscripts "-o" for the control variable related

open-loop transfer functions are also omitted for brevity. This assumption is made in publications [P1]–[P7], when presenting the transfer function sets for converters at open and closed loop.

According to the definition of the dynamic profile [26], the dynamic properties of a converter should be defined in a way that only the power-stage components and the necessary control circuitry are included in the corresponding transfer functions. Therefore, any additional components such as loads, input capacitors and the other subsystems shall be considered as external elements and not as parts of the converter and its dynamic profile. The matrix descriptions in (2.3) represent the dynamic profile of a switched-mode converter, when it is derived as follows: The transfer functions in (2.3) are derived or measured for a converter, which is supplied by an ideal voltage source and loaded with an ideal current sink [26], i.e., the internal impedance of the voltage source and the internal admittance of the current sink should be zero.

2.1.2 Two-Port Networks

The modified g-parameter set in (2.3) can be equally represented as a linear two-port network shown inside the dashed line in Fig. 2.1. Note that the two-port network is supplied by an ideal voltage source and is loaded with an ideal current sink implying that the two-port network represents the internal dynamics. The input port of the network is Norton's equivalent circuit comprising of the input admittance Y_{in} (i.e. the inverse of input impedance Z_{in}) and the current sink $T_{\mathrm{oi}}\hat{i}_{\mathrm{o}} + G_{\mathrm{ci}}\hat{c}$. Similarly, the output port is Thevenin's equivalent circuit comprising of the output impedance Z_{o} and the voltage source $G_{\mathrm{io}}\hat{u}_{\mathrm{in}} + G_{\mathrm{co}}\hat{c}$.

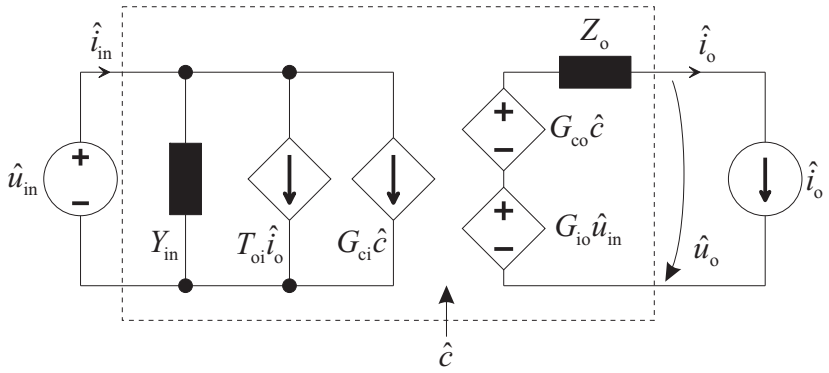


Fig. 2.1 *The two-port network representation of a converter at open and closed loop.*

2.1.3 Output-Voltage Feedback

The output-voltage feedback is necessary for good dynamic performance. It improves steady-state accuracy of the output voltage as well as the transient responses to input-voltage or output-current variations by means of a controller, which compares the measured output voltage to the reference value and changes the duty ratio accordingly to compensate the variations. Although the feedback increases the system complexity

and cost, the benefits are usually much more valuable than the disadvantages. The effect of output-voltage feedback on the dynamic profile and the modified g-parameters can be analyzed from the control block diagrams shown in Fig. 2.2 for output (a) and input (b) dynamics, respectively. In Fig. 2.2, H_v is the output-voltage sensing gain, G_{cc} is the controller transfer function and G_a is the modulator gain. The perturbed reference signal is denoted as $\hat{c}_r$ to distinguish it from the open-loop control signal $\hat{c}$. In control theory, the input voltage and output current are considered as disturbance inputs of the system [32]. The closed-loop transfer functions can be found from Fig. 2.2 by solving the mapping from the input variables of the closed-loop system (i.e. $\hat{u}_{in}$, $\hat{i}_o$, $\hat{c}_r$) to the output variables (i.e. $\hat{u}_o$, $\hat{i}_{in}$) as shown in (2.4), where $L_v = H_v G_{cc} G_a G_{co-o}$ is the output-voltage loop gain. The characteristic equation of the feedback system is $1+L_v$ and, therefore, the stability of the system can be studied by applying the Nyquist stability criterion to the voltage-loop gain L_v [32].

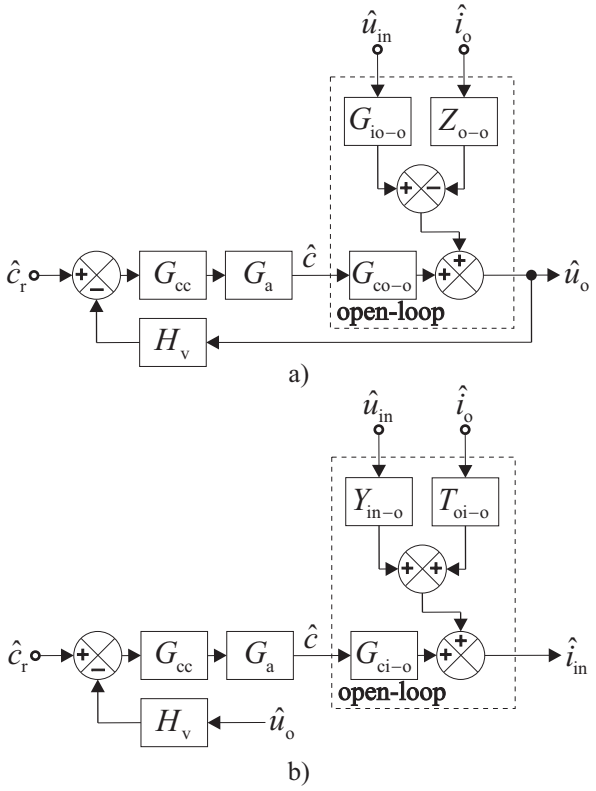


Fig. 2.2 *Control block diagrams for output (a) and input (b) dynamics.*

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y_{in-c} & T_{oi-c} & G_{ci-c} \\ G_{io-c} & -Z_{o-c} & G_{co-c} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c}_r \end{bmatrix}$$
$$= \begin{bmatrix} Y_{in-o} - \dfrac{G_{io-o}G_{ci-o}}{G_{co-o}} \dfrac{L_v}{1+L_v} & T_{oi-o} + \dfrac{Z_{o-o}G_{ci-o}}{G_{co-o}} \dfrac{L_v}{1+L_v} & \dfrac{G_{ci-o}}{H_v G_{co-o}} \dfrac{L_v}{1+L_v} \\ \dfrac{G_{io-o}}{1+L_v} & -\dfrac{Z_{o-o}}{1+L_v} & \dfrac{1}{H_v} \dfrac{L_v}{1+L_v} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c}_r \end{bmatrix} \quad (2.4)$$

2.2 Interaction Formalism

The two-port networks can be conveniently used to develop adequate formalism to analyze the load and source interactions of a converter. The formalism to analyze the load and source interactions is presented in various publications such as [P1], [P3]–[P7], [22], [27], [28] and [57]. Therefore, it is only briefly reviewed in this section.

2.2.1 Load Interactions

Fig. 2.3 shows the general two-port network of a converter (operating either at open or closed loop) and a non-ideal load (i.e. Z_L and $\hat{j}_\mathrm{o}$). The load-affected transfer functions can be found by solving the output current $\hat{i}_\mathrm{o}$ in Fig. 2.3 and substituting it in (2.3). The resulting load-affected description of the converter with the effect of load impedance is shown in (2.5), where the superscript "L" means that the corresponding transfer function includes the effect of the load impedance. The transfer function set in (2.5) describes the two-port network for the circuit inside the dashed line shown in Fig. 2.3.

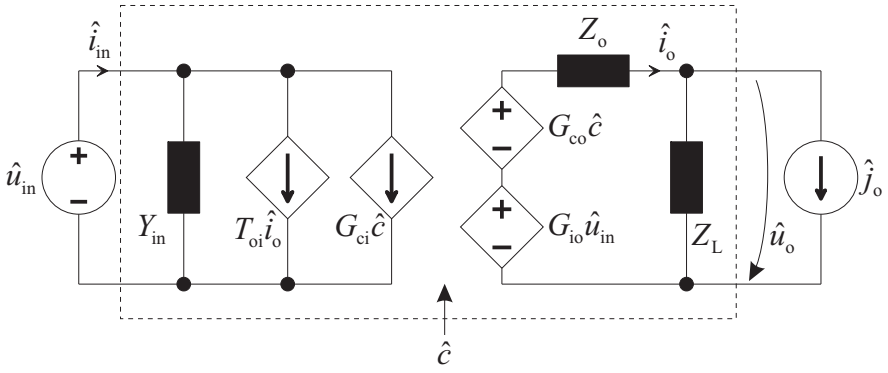


Fig. 2.3 *The general two-port network for load-interaction analysis.*

$$\begin{bmatrix}\hat{i}_\mathrm{in}\\ \hat{u}_\mathrm{o}\end{bmatrix}=\begin{bmatrix}Y_\mathrm{in}^\mathrm{L} & T_\mathrm{oi}^\mathrm{L} & G_\mathrm{ci}^\mathrm{L}\\ G_\mathrm{io}^\mathrm{L} & -Z_\mathrm{o}^\mathrm{L} & G_\mathrm{co}^\mathrm{L}\end{bmatrix}\begin{bmatrix}\hat{u}_\mathrm{in}\\ \hat{j}_\mathrm{o}\\ \hat{c}\end{bmatrix}=\begin{bmatrix}Y_\mathrm{in}+\dfrac{G_\mathrm{io}T_\mathrm{oi}}{Z_\mathrm{L}+Z_\mathrm{o}} & \dfrac{T_\mathrm{oi}}{1+\dfrac{Z_\mathrm{o}}{Z_\mathrm{L}}} & G_\mathrm{ci}+\dfrac{G_\mathrm{co}T_\mathrm{oi}}{Z_\mathrm{L}+Z_\mathrm{o}}\\ \dfrac{G_\mathrm{io}}{1+\dfrac{Z_\mathrm{o}}{Z_\mathrm{L}}} & -\dfrac{Z_\mathrm{o}}{1+\dfrac{Z_\mathrm{o}}{Z_\mathrm{L}}} & \dfrac{G_\mathrm{co}}{1+\dfrac{Z_\mathrm{o}}{Z_\mathrm{L}}}\end{bmatrix}\begin{bmatrix}\hat{u}_\mathrm{in}\\ \hat{j}_\mathrm{o}\\ \hat{c}\end{bmatrix} \quad (2.5)$$

According to (2.5), the effect of the load impedance on the output dynamics is minimal if $Z_\mathrm{o} << Z_\mathrm{L}$. However, the input dynamics are affected even if the previous condition is met. The input admittance (Y_in^L) stays intact, if G_io or T_oi can be made equal to zero. Similarly, the control-to-input-current transfer function G_ci stays intact, if $T_\mathrm{oi}=0$. The open-loop control-to-output-voltage transfer function $G_\mathrm{co-o}$ is an essential part of the voltage-loop gain L_v. Therefore, the effect of the load impedance on $G_\mathrm{co-o}^\mathrm{L}$ will also directly affect the voltage-loop gain as shown in (2.6).

$$L_{\mathrm{v}}^{\mathrm{L}} = \frac{L_{\mathrm{v}}}{1+\dfrac{Z_{\mathrm{o-o}}}{Z_{\mathrm{L}}}} \tag{2.6}$$

According to (2.6), the load impedance affects the voltage-loop gain via the open-loop output impedance $Z_{\mathrm{o-o}}$ – not via the closed-loop output impedance $Z_{\mathrm{o-c}}$. Therefore, it is important to derive the load-affected transfer function set in terms of open-loop transfer functions in order to analyze the real load effects on the converter dynamics. The other load-affected closed-loop transfer functions can be found by replacing the nominal transfer functions in (2.4) with the corresponding load-affected transfer functions.

2.2.2 Source Interactions

Fig. 2.4 shows the general two-port network of a converter with a non-ideal source (i.e. Z_{s} and u_{ins}). The effect of the source impedance on the dynamics of the converter can be found by solving the input voltage $\hat{u}_{\mathrm{in}}$ in Fig. 2.4 and substituting it in (2.3), which yields the source-affected transfer functions shown in (2.7). The superscript "S" means that the corresponding transfer function includes the effect of the source impedance Z_{s}. The special admittances $Y_{\mathrm{in-sc}}$ and $Y_{\mathrm{in-\infty}}$ are the short-circuit and ideal input admittances and are defined in (2.8). Similarly to the load interactions, the transfer function set in (2.7) describes the two-port network for the circuit inside the dashed line shown in Fig. 2.4.

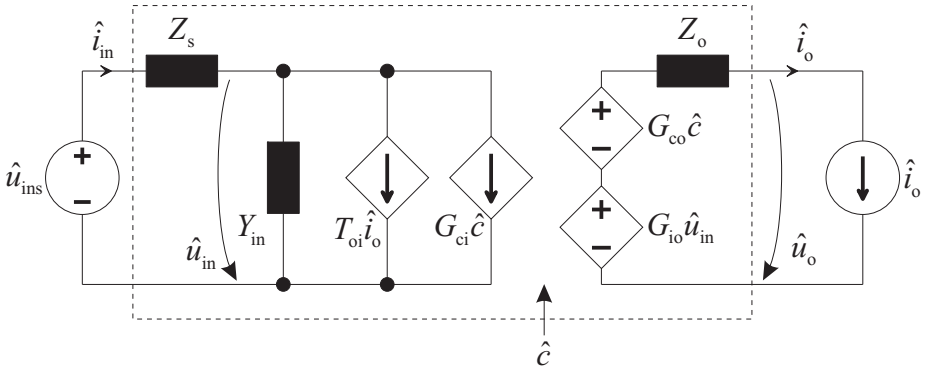


Fig. 2.4 *The general two-port network for source-interaction analysis.*

$$\begin{bmatrix}\hat{i}_{\mathrm{in}}\\ \hat{u}_{\mathrm{o}}\end{bmatrix} = \begin{bmatrix} Y_{\mathrm{in}}^{\mathrm{S}} & T_{\mathrm{oi}}^{\mathrm{S}} & G_{\mathrm{ci}}^{\mathrm{S}} \\ G_{\mathrm{io}}^{\mathrm{S}} & -Z_{\mathrm{o}}^{\mathrm{S}} & G_{\mathrm{co}}^{\mathrm{S}} \end{bmatrix} \begin{bmatrix}\hat{u}_{\mathrm{ins}}\\ \hat{i}_{\mathrm{o}}\\ \hat{c}\end{bmatrix}$$
$$= \begin{bmatrix} \dfrac{Y_{\mathrm{in}}}{1+Z_{\mathrm{s}}Y_{\mathrm{in}}} & \dfrac{T_{\mathrm{oi}}}{1+Z_{\mathrm{s}}Y_{\mathrm{in}}} & \dfrac{G_{\mathrm{ci}}}{1+Z_{\mathrm{s}}Y_{\mathrm{in}}} \\ \dfrac{G_{\mathrm{io}}}{1+Z_{\mathrm{s}}Y_{\mathrm{in}}} & -\dfrac{1+Z_{\mathrm{s}}Y_{\mathrm{in-sc}}}{1+Z_{\mathrm{s}}Y_{\mathrm{in}}}Z_{\mathrm{o}} & \dfrac{1+Z_{\mathrm{s}}Y_{\mathrm{in-\infty}}}{1+Z_{\mathrm{s}}Y_{\mathrm{in}}}G_{\mathrm{co}} \end{bmatrix} \begin{bmatrix}\hat{u}_{\mathrm{ins}}\\ \hat{i}_{\mathrm{o}}\\ \hat{c}\end{bmatrix} \tag{2.7}$$

$$Y_{\text{in-sc}} = Y_{\text{in}} + \frac{G_{\text{io}} T_{\text{oi}}}{Z_{\text{o}}}$$
$$Y_{\text{in-}\infty} = Y_{\text{in}} - \frac{G_{\text{io}} G_{\text{ci}}}{G_{\text{co}}} \tag{2.8}$$

The physical meaning of the short-circuit ($Y_{\text{in-sc}}$) and ideal ($Y_{\text{in-}\infty}$) input admittances can be derived as follows. The short-circuit input admittance represents the admittance seen at the input of a converter, when the output is dynamically short circuited, i.e., the load impedance Z_{L} is equal to zero. The ideal input admittance represents the admittance seen at the input of a converter, when the controller of the converter has infinite bandwidth and gain. Dynamically, this means that the perturbed output voltage is equal to zero, which can be obtained with the control signal shown in (2.9). When this control signal is substituted to (2.3), the input admittance is equal to the ideal input admittance shown in (2.8). The short-circuit and ideal input admittances are specific for a converter topology, but they can be shown to be the same at open and closed loop and also independent of the load [28]. Moreover, the ideal input admittance can be shown to be independent of the control method [22], [28].

$$\hat{c} = -\frac{G_{\text{io}}}{G_{\text{co}}} \hat{u}_{\text{in}} + \frac{Z_{\text{o}}}{G_{\text{co}}} \hat{i}_{\text{o}} \tag{2.9}$$

When the source-affected output impedance Z_{o}^{S} is expressed as shown in (2.7), it is actually assumed that output impedance Z_{o} is not exactly zero. If $Z_{\text{o}} = 0$, the short-circuit input admittance $Y_{\text{in-sc}}$ would be infinite according to (2.8) and, hence, the source-affected output impedance Z_{o}^{S} would not be mathematically defined, i.e., the infinite $Y_{\text{in-sc}}$ would be multiplied by the zero Z_{o}. The equation for Z_{o}^{S} shown in (2.7) is derived from the expression

$$Z_{\text{o}}^{\text{S}} = Z_{\text{o}} + \frac{G_{\text{io}} T_{\text{oi}} Z_{\text{s}}}{1 + Z_{\text{s}} Y_{\text{in}}}, \tag{2.10}$$

which gives the correct source-affected output impedance, when Z_{o} is zero as it can be theoretically for an OCF-controlled converter. However, in practice Z_{o} is not exactly zero due to the non-idealities and parasitic effects and, hence, the use of notation shown in (2.7) simplifies the source interaction analysis.

The source-affected voltage-loop gain can be represented as shown in (2.11) indicating that the effect of the source impedance is reflected via the ideal and open-loop input admittances on the loop gain.

$$L_{\text{v}}^{\text{S}} = \frac{1 + Z_{\text{s}} Y_{\text{in-}\infty}}{1 + Z_{\text{s}} Y_{\text{in-o}}} L_{\text{v}} \tag{2.11}$$

2.2.3 Output-Voltage Remote Sensing

Switched-mode converters can be equipped with remote sensing terminals [84]–[86]. These terminals are used to alternatively take the output-voltage feedback directly from the output of the converter or from the point of the load. The remote sensing – when connected into load terminals – can introduce an additional impedance network inside the feedback loop possibly deteriorating the dynamics of the converter. The general formulation presented here is published for the first time in [P3].

Fig. 2.5 shows the cascaded system consisting of a switched-mode converter and the connection-impedance block. Interface A_1 at the output of the converter represents the typical interface from which the feedback signal is taken for the feedback network. Interface A_2 represents the remote-sensing interface from which the load voltage is used as feedback signal. The connection-impedance block is represented by the general two-port network inside the dashed line.

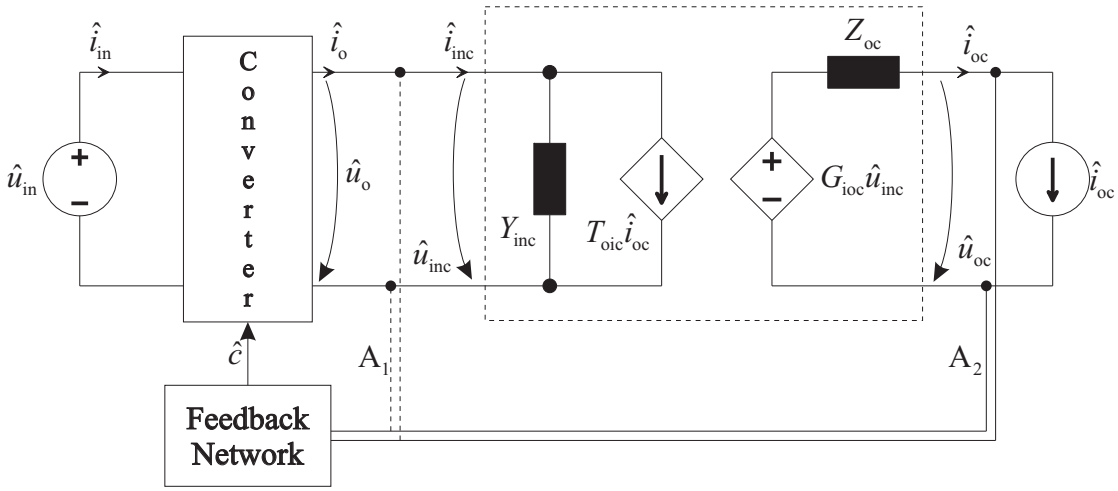


Fig. 2.5 *Cascaded system consisting of a converter and a connection-impedance block represented by the two-port network inside the dashed line.*

The transfer functions for the cascaded system shown in Fig. 2.5 are found most conveniently by first solving the transfer functions for the cascade of the open-loop converter and the connection-impedance block. The effect of the feedback can be then added as described in Section 2.1.3. The g-parameter set for the connection impedance block is defined as

$$\begin{bmatrix} \hat{i}_{inc} \\ \hat{u}_{oc} \end{bmatrix} = \begin{bmatrix} Y_{inc} & T_{oic} \\ G_{ioc} & -Z_{oc} \end{bmatrix} \begin{bmatrix} \hat{u}_{inc} \\ \hat{i}_{oc} \end{bmatrix}. \tag{2.12}$$

The transfer functions for the cascaded system can be found by solving the output current $\hat{i}_o$ and input voltage $\hat{u}_{inc}$ from Fig. 2.5, which yields

$$\begin{aligned}\hat{i}_{\mathrm{o}} &= \frac{Y_{\mathrm{inc}}G_{\mathrm{io-o}}\hat{u}_{\mathrm{in}} + Y_{\mathrm{inc}}G_{\mathrm{co-o}}\hat{c} + T_{\mathrm{oic}}\hat{i}_{\mathrm{oc}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}} \\ \hat{u}_{\mathrm{inc}} &= \frac{G_{\mathrm{io-o}}\hat{u}_{\mathrm{in}} + G_{\mathrm{co-o}}\hat{c} - Z_{\mathrm{o-o}}T_{\mathrm{oic}}\hat{i}_{\mathrm{oc}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}}\end{aligned} \tag{2.13}$$

and substituting $\hat{i}_{\mathrm{o}}$ in (2.3) and $\hat{u}_{\mathrm{inc}}$ in (2.12) with the new formulas in (2.13), when the original transfer functions in (2.3) are the open-loop transfer functions of the converter. The resulting transfer function set for the cascaded system is shown in (2.14), where the short-circuit input admittance of the connection-impedance block $Y_{\mathrm{in-sc}}^{\mathrm{c}}$ is defined in (2.15). The superscript "RS" denotes "remote sensing" although feedback is not connected yet.

$$\begin{aligned}\begin{bmatrix}\hat{i}_{\mathrm{in}} \\ \hat{u}_{\mathrm{oc}}\end{bmatrix} &= \begin{bmatrix}Y_{\mathrm{in-o}}^{\mathrm{RS}} & T_{\mathrm{oi-o}}^{\mathrm{RS}} & G_{\mathrm{ci-o}}^{\mathrm{RS}} \\ G_{\mathrm{io-o}}^{\mathrm{RS}} & -Z_{\mathrm{o-o}}^{\mathrm{RS}} & G_{\mathrm{co-o}}^{\mathrm{RS}}\end{bmatrix}\begin{bmatrix}\hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{oc}} \\ \hat{c}\end{bmatrix} \\ &= \begin{bmatrix}Y_{\mathrm{in-o}} + \dfrac{Y_{\mathrm{inc}}G_{\mathrm{io-o}}T_{\mathrm{oi-o}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}} & \dfrac{T_{\mathrm{oic}}T_{\mathrm{oi-o}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}} & G_{\mathrm{ci-o}} + \dfrac{Y_{\mathrm{inc}}G_{\mathrm{co-o}}T_{\mathrm{oi-o}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}} \\ \dfrac{G_{\mathrm{ioc}}G_{\mathrm{io-o}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}} & -\dfrac{1+Z_{\mathrm{o-o}}Y_{\mathrm{in-sc}}^{\mathrm{c}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}}Z_{\mathrm{oc}} & \dfrac{G_{\mathrm{ioc}}G_{\mathrm{co-o}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}}\end{bmatrix}\begin{bmatrix}\hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{oc}} \\ \hat{c}\end{bmatrix}\end{aligned} \tag{2.14}$$

$$Y_{\mathrm{in-sc}}^{\mathrm{c}} = Y_{\mathrm{inc}} + \frac{G_{\mathrm{ioc}}T_{\mathrm{oic}}}{Z_{\mathrm{oc}}} \tag{2.15}$$

According to (2.14), the connection-impedance block can change all the internal transfer functions of the converter profoundly, making the converter more prone to external interactions or even to be unstable. When Z_{oc} is zero, as it can theoretically be for an impedance block consisting of a pure shunt impedance (e.g., a capacitor), the short-circuit input admittance of the impedance block ($Y_{\mathrm{in-sc}}^{\mathrm{c}}$) is equal to infinity and the output impedance $Z_{\mathrm{o-o}}^{\mathrm{RS}}$ of the cascaded system needs to be computed with a different equation, i.e., $Z_{\mathrm{o-o}}^{\mathrm{RS}} = Z_{\mathrm{oc}} + G_{\mathrm{ioc}}T_{\mathrm{oic}}Z_{\mathrm{o-o}}/\left(1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}\right)$ as discussed in Section 2.2.2 in the case of source interactions. The remote-sensing-affected voltage-loop gain can be given as shown in (2.16) showing that the input-to-output transfer function of the connection-impedance block also affects the feedback loop in addition to the impedance $Z_{\mathrm{o-o}}$ and the admittance Y_{inc}.

$$L_{\mathrm{v}}^{\mathrm{RS}} = \frac{G_{\mathrm{ioc}}}{1+Z_{\mathrm{o-o}}Y_{\mathrm{inc}}}L_{\mathrm{v}} \tag{2.16}$$

2.3 Effect of Different Control Methods

The modified g-parameter sets and two-port networks considered so far have been in general form without considering by any means the effects introduced by different

control methods. These can be analyzed most conveniently by first developing the state-space model for a converter under direct duty-cycle control, because the other control methods usually change the way the duty ratio is generated and thus the dynamics associated to the perturbed duty ratio. The control methods considered here are voltage-mode, peak-current-mode, input-voltage feedforward and output-current feedforward controls.

2.3.1 Voltage-Mode Control

In VMC, the general perturbed control variable $\hat{c}$ is directly the perturbed duty ratio $\hat{d}$. The duty ratio is constructed by a pulse-width modulator by comparing a control voltage u_{co} to a constant sawtooth-ramp signal repeating at the switching frequency [19]. When the peak-to-peak amplitude of the sawtooth-ramp signal is V_m, the transfer function of the modulator can be simply presented as $G_a = \hat{d}/\hat{u}_{co} = 1/V_m$ [14]. Therefore, the dynamics of the VM-controlled converter can be characterized by the state-space averaged and linearized small-signal model of the power stage, the modulator gain G_a and the feedback network (i.e. G_{cc} and H_v), as discussed in Section 2.1.3.

2.3.2 Peak-Current-Mode Control

Different modeling techniques have been used to model the PCM-controlled converters as discussed in Chapter 1. The modeling technique presented in [63] is briefly reviewed here to illustrate the main consequences of the PCM control on the converter dynamics. In PCM control, the up slope of the inductor current or sum of many inductor currents is used in duty-ratio generation in such a way that the control current i_{co} is compared to the inductor current to establish the duty ratio at the time when the measured inductor current reaches the control current. The effect of PCM control on the small-signal dynamics can be found for a two-memory-element converter by the duty-ratio constraints shown in (2.17), where the perturbed duty ratio is expressed as a function of perturbed control current $\hat{i}_{co}$ and state and input variables [63]. In (2.17), F_m^{ss} is the duty-ratio gain, q_c and q_o are the feedback gains from the inductor current and the capacitor voltage, respectively, and q_i and q_{io} are the feedforward gains from the input voltage and the output current, respectively. The superscript "ss" refers to state space. The procedure to determine the gains shown in (2.17) is well covered in [26] and [63] and, therefore, it is not discussed here. The duty-ratio constraints can be easily modified for higher-order converters under PCMC as done for a superbuck in [P7].

$$\hat{d} = F_m^{ss}\left(\hat{i}_{co} - q_c^{ss}\hat{i}_L - q_o^{ss}\hat{u}_c - q_i^{ss}\hat{u}_{in} - q_{io}^{ss}\hat{i}_o\right) \tag{2.17}$$

The new state-space model for a converter under PCMC can be found by replacing the perturbed duty ratio in the small-signal state-space model of the converter under VMC with the expression in (2.17) and by rearranging the terms. The transfer functions in (2.3) can be solved as discussed in Section 2.1. The general control variable under PCMC is $\hat{i}_{co}$. However, the error amplifier constituting the controller works in voltage

domain (i.e., the control signal is the voltage $\hat{u}_{co}$ instead of the current $\hat{i}_{co}$) and, therefore, the modulator gain G_a becomes $1/R_{s1}$, where R_{s1} is the equivalent inductor-current sensing resistor [26].

The duty-ratio gain in (2.17) can be expressed as shown in (2.18), where M_1 and M_2 are the inductor-current up and down slopes, respectively, and M_c is the slope of the compensation ramp used to extend the duty ratio beyond 0.5 [26]. According to (2.18), the duty-ratio gain is infinite, when no compensation is used (i.e., $M_c = 0$) and the duty ratio is equal to 0.5. The compensation-ramp slope also has a special role in a PCM-controlled buck converter in reducing the source interactions and attenuating the input-voltage noise by making the input-to-output transfer functions theoretically zero [57].

$$F_m^{ss} = \frac{1}{T_s\left(M_c + \frac{D' - D}{2}\left(M_1 + M_2\right)\right)} \tag{2.18}$$

2.3.3 Input-Voltage and Output-Current-Feedforward Controls

Output-voltage feedback is necessary for good dynamic performance of a switched-mode converter. However, the feedback has its limitations in terms of sensitivity and stability, and even a well-designed feedback controller may not be fast enough to meet the transient requirements of modern-day loads [6]. Hence, feedforward from the disturbance or input variables are used to improve the system dynamics in addition to the feedback from the output variable [32].

For switched-mode converters, the input variables are input voltage and output current. Hence, the IVFF and/or OCF controls are typically applied to an open-loop converter and the feedback from the output voltage is then used to correct the inaccuracies of the feedforward controls. As a consequence, the transient performance of the converter can be substantially improved or, theoretically, even made ideal [65]. The ideality means that the variations in input voltage and output current do not affect the output-voltage regulation at all. Dynamically, this means that the perturbed output-voltage should be zero under the perturbations in input voltage and output current.

The ideal feedforward gains resulting in the ideal transient dynamics can be found by studying the control block diagrams shown in Fig. 2.6 for output (a) and input (b) dynamics. Note that the notation in Fig. 2.6 is in general form, meaning that the feedforward controls can also be applied to a closed-loop converter. In Fig. 2.6, G_o and G_i are the general feedforward gains from output current and input voltage, respectively, and G_c is the gain from the control variable $\hat{c}_r$ to the general control variable $\hat{c}$. If only the IVFF control is used, $G_o = 0$ and, similarly, if only the OCF control is used, $G_i = 0$.

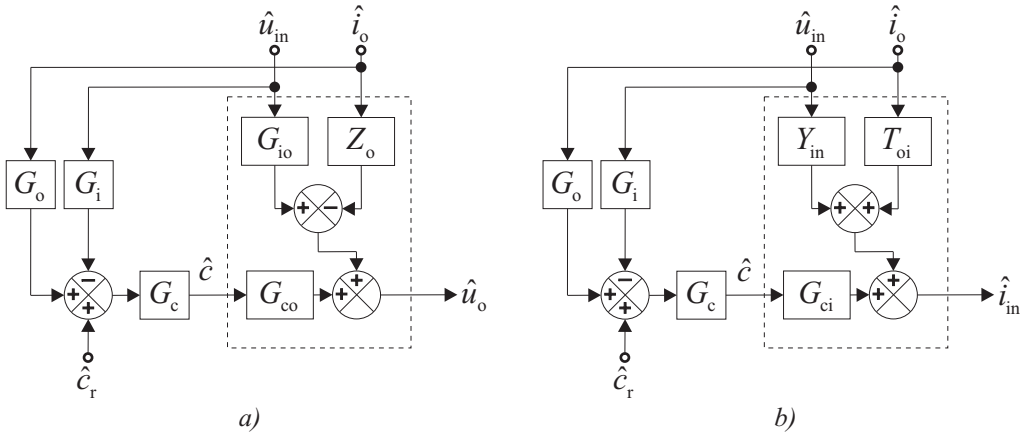


Fig. 2.6 *Control block diagrams for output (a) and input (b) dynamics to evaluate the conditions for the ideal transient performance.*

Solving the output voltage from Fig. 2.6a yields

$$\hat{u}_o = G_{io}\hat{u}_{in} - Z_o\hat{i}_o + G_{co}\hat{c} = \left(G_{io} - G_{co}G_cG_i\right)\hat{u}_{in} - \left(Z_o - G_{co}G_cG_o\right)\hat{i}_o + G_{co}G_c\hat{c}_r\,, \qquad (2.19)$$

where $G_{io} - G_{co}G_cG_i$ and $Z_o - G_{co}G_cG_o$ are the new input-to-output transfer function and output impedance of the IVFF and OCF-controlled converter, respectively. The variations in input voltage would not propagate to output voltage, if the gain G_cG_i was equal to G_{io}/G_{co}. Similarly, the variations in output current would not propagate to output voltage, if the gain G_cG_o was equal to Z_o/G_{co}. If both conditions are met, the output voltage would be changed only due to the new control variable $\hat{c}_r$, which is typically zero for converters regulating the output voltage at constant level.

It is evident that the implementation of the theoretically ideal gains (i.e., G_cG_i and G_cG_o) is not possible for non-minimum-phase converters such as boost and buck-boost without causing instability, because the right-hand-plane (RHP) zeros of the control-to-output transfer functions appear as poles in the feedforward path making the feedforward gain unstable. On the other hand, if the input-to-output transfer function and output impedance have the same zeros as the control-to-output transfer function, the needed gains would be operation-point-dependent constants making the implementation rather easy.

Solving the input current from Fig. 2.6b and replacing the gains G_cG_i and G_cG_o with the corresponding ideal gains derived above results in the input current

$$\hat{i}_{in} = \left(Y_{in} - \frac{G_{io}G_{ci}}{G_{co}}\right)\hat{u}_{in} + \left(T_{oi} + \frac{Z_oG_{ci}}{G_{co}}\right)\hat{i}_o + G_{ci}G_c\hat{c}_r = Y_{in-\infty}\hat{u}_{in} + T_{oi-\infty}\hat{i}_o + G_{ci}G_c\hat{c}_r\,, \qquad (2.20)$$

where $Y_{in-\infty}$ is the ideal input admittance discussed earlier in the case of source interactions and $T_{oi-\infty}$ – hereafter, the ideal reverse current transfer function – a new

parameter defining the reverse current transfer function from output current to input current in the case of ideal OCF control. Its existence has not been discussed in literature earlier. It can be shown that $T_{\mathrm{oi}-\infty}$ is independent of load, control method or state of the feedback, and it is specific for a given topology. Therefore, $T_{\mathrm{oi}-\infty}$ (and also $Y_{\mathrm{in}-\infty}$) can be computed based on the open-loop transfer functions of a direct-duty-cycle or VM-controlled converter.

The ideal transient performance can also be theoretically obtained with a feedback system having the magnitude and gain-crossover frequency of the voltage-loop gain infinite. Consequently, the closed-loop input-to-output and output impedances would be zero also resulting in zero perturbed output voltage, as it can be concluded from (2.4). Therefore, the closed-loop input admittance and reverse current transfer function would be equal to the corresponding ideal parameters as shown in (2.21). It is evident that the infinite magnitude and gain-crossover frequency are not possible in practice without causing instability.

$$\begin{aligned} Y_{\mathrm{in-c}} &= Y_{\mathrm{in-o}} - \frac{G_{\mathrm{io-o}}G_{\mathrm{ci-o}}}{G_{\mathrm{co-o}}}\frac{L_{\mathrm{v}}}{1+L_{\mathrm{v}}} = \frac{Y_{\mathrm{in-o}}}{1+L_{\mathrm{v}}} + \frac{Y_{\mathrm{in}-\infty}L_{\mathrm{v}}}{1+L_{\mathrm{v}}} \overset{"L_{\mathrm{v}}=\infty"}{=} Y_{\mathrm{in-o}} - \frac{G_{\mathrm{io-o}}G_{\mathrm{ci-o}}}{G_{\mathrm{co-o}}} = Y_{\mathrm{in}-\infty} \\ T_{\mathrm{oi-c}} &= T_{\mathrm{oi-o}} + \frac{Z_{\mathrm{o-o}}G_{\mathrm{ci-o}}}{G_{\mathrm{co-o}}}\frac{L_{\mathrm{v}}}{1+L_{\mathrm{v}}} = \frac{T_{\mathrm{oi-o}}}{1+L_{\mathrm{v}}} + \frac{T_{\mathrm{oi}-\infty}L_{\mathrm{v}}}{1+L_{\mathrm{v}}} \overset{"L_{\mathrm{v}}=\infty"}{=} T_{\mathrm{oi-o}} + \frac{Z_{\mathrm{o-o}}G_{\mathrm{ci-o}}}{G_{\mathrm{co-o}}} = T_{\mathrm{oi}-\infty} \end{aligned} \tag{2.21}$$

According to (2.21), the closed-loop input admittance and reverse current transfer functions for practical voltage-loop gains would track the corresponding ideal transfer functions at frequencies where the magnitude of the voltage-loop gain is much higher than unity, and the corresponding open-loop transfer functions at frequencies where the magnitude of the voltage-loop gain is much smaller than unity.

In [P6], the effect of IVFF control on a VM-controlled buck converter is analyzed. The notation used in [P6] is slightly different from the one given here. For VM-controlled converter the general control variable $\hat{c}$ is equal to the perturbed duty-ratio $\hat{d}$ and, in addition, the feedback controller operates in voltage domain. Therefore, the duty-ratio gain F_{m}, the IVFF gain q_{i} and the control voltage $\hat{u}_{\mathrm{co}}$ are used instead of G_{c}, G_{i} and $\hat{c}_{\mathrm{r}}$, respectively. Consequently, the g-parameter set describing the dynamics of a IVFF-controlled open-loop converter becomes as shown in (2.22) and the ideal condition resulting to zero input-to-output transfer function becomes $F_{\mathrm{m}}q_{\mathrm{i}} = G_{\mathrm{io-o}}/G_{\mathrm{co-o}}$. According to (2.22), the IVFF control only affects the input-to-output transfer function and input admittance leaving the output-current related transfer functions intact. Change in control-related transfer functions is due to change in the control signal from $\hat{d}$ to $\hat{u}_{\mathrm{co}}$.

$$\begin{bmatrix} \hat{i}_{\mathrm{in}} \\ \hat{u}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} Y_{\mathrm{in-o}} - F_{\mathrm{m}}q_{\mathrm{i}}G_{\mathrm{ci-o}} & T_{\mathrm{oi-o}} & F_{\mathrm{m}}G_{\mathrm{ci-o}} \\ G_{\mathrm{io-o}} - F_{\mathrm{m}}q_{\mathrm{i}}G_{\mathrm{co-o}} & -Z_{\mathrm{o-o}} & F_{\mathrm{m}}G_{\mathrm{co-o}} \end{bmatrix} \begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \\ \hat{u}_{\mathrm{co}} \end{bmatrix} \tag{2.22}$$

Similarly in [P4] and [P5], the effect of OCF control on PCM-controlled buck converter is analyzed. Therefore, $\hat{i}_{co}$ and $\hat{u}_{co}$ are used instead of $\hat{c}$ and $\hat{c}_r$, respectively, to represent the control variables. Consequently, G_c becomes equal to the modulator gain $G_a = 1/R_{s1}$, where R_{s1} is the equivalent inductor-current-sensing resistor, and G_o becomes equal to $R_{s2}H_i$, where R_{s2} is the equivalent output-current-sensing resistor and H_i is the output-current sensing gain. The resulting g-parameter set for the PCM-controlled converter with OCF (PCMC-OCF) becomes as shown in (2.23) and the ideal gain resulting in zero open-loop output impedance becomes $G_a H_i R_{s1} = Z_{o-o}/G_{co-o}$. According to (2.23), the OCF control only affects the open-loop reverse current transfer function and output impedance leaving the input-voltage related transfer functions intact. Actually, the control related transfer functions are also left intact, because multiplying the original transfer function by G_a only changes the control variable from current to voltage as also used for PCM-controlled converters in practice.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{oi-o} + R_{s2}H_i G_a G_{ci-o} & G_a G_{ci-o} \\ G_{io-o} & -\left(Z_{o-o} - R_{s2}H_i G_a G_{co-o}\right) & G_a G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{u}_{co} \end{bmatrix} \tag{2.23}$$

Another implication of the conditions for the ideal IVFF and OCF gains is that the source and load interactions would be greatly reduced. According to Section 2.2, the load interactions would be minimal, if $Z_{o-o} = 0$, i.e., the load impedance would not change the output dynamics according to the bottom row of the load-affected transfer function matrix shown in (2.5). However, the input dynamics would be affected, i.e., the open-loop input admittance Y_{in-o}^{L} and control-to-input transfer function G_{ci-o}^{L}. Similarly, if $G_{io-o} = 0$, the source interactions would be minimal on the output dynamics as can be concluded according to the bottom row of the source-affected transfer function matrix shown in (2.7), because, according to (2.8), $Y_{in-o} = Y_{in-sc} = Y_{in-\infty}$, when $G_{io-o} = 0$. In addition, the load interactions would not be reflected to the input side of a converter according Y_{in-o}^{L} in (2.5). Therefore, a converter that has the open-loop input-to-output transfer function and output impedance zero would act as a dynamic buffer within a system and prevent the interactions from propagating through the converter. Hence, the transient dynamics of the converter would be ideal and, in addition, the converter would be invariant to source or load interactions making the system analysis deterministic.

2.4 System-Level Analysis Method for Cascaded Subsystems

The load and source interactions considered so far have been derived to illustrate the effect of non-ideal load and source impedances on switched-mode converters by means of the general modified g-parameter sets and two-port networks. In this section, the same formalism is reviewed for the general subsystems connected in cascade, which is the typical situation in distributed power systems. The formalism is used to study the internal and input-output stability of cascaded subsystems, which actually form the foundation for the system-level analysis.

2.4.1 Internal and Input-Output Stability

In [33] and [88], the formalism to analyze the internal and input-output stability is derived by using the system theoretic and control engineering methods for multi-input multi-output (MIMO) systems. The same methods can also be used for the single-input single-output (SISO) systems with somewhat easier notations, i.e., each transfer function is represented by a single transfer function instead of transfer-function matrix.

Fig. 2.7 shows a SISO system consisting of two subsystems connected in cascade. The subsystems are named as source (S) and load (L) subsystems. The subsystems may be either at open or closed loop. In both cases, the control variables are constant and, therefore, the subsystems are independent of each other and the g-parameter sets compose of four transfer functions given in (2.24).

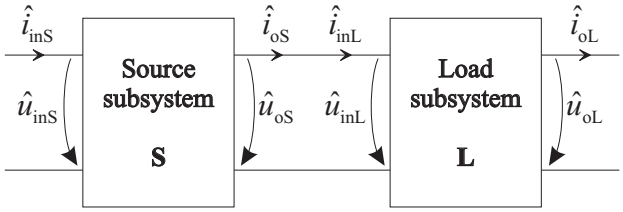


Fig. 2.7 *Cascade of two independent subsystems S and L.*

$$\begin{bmatrix} \hat{i}_{inS} \\ \hat{u}_{oS} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} \hat{u}_{inS} \\ \hat{i}_{oS} \end{bmatrix}$$
$$\begin{bmatrix} \hat{i}_{inL} \\ \hat{u}_{oL} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \begin{bmatrix} \hat{u}_{inL} \\ \hat{i}_{oL} \end{bmatrix} \tag{2.24}$$

The mapping from the system input variables (i.e. $\hat{u}_{inS}$ and $\hat{i}_{oL}$) to the system intermediate variables (i.e. $\hat{i}_x = \hat{i}_{oS} = \hat{i}_{inL}$ and $\hat{u}_x = \hat{u}_{oS} = \hat{u}_{inL}$) can be solved as shown in (2.25) by using the definitions in (2.24) in the SISO case [33]. Similarly, the mapping from the system input variables to the system output variables (i.e. $\hat{u}_{oL}$ and $\hat{i}_{inS}$) can be solved as shown in (2.26).

$$\begin{bmatrix} \hat{i}_x \\ \hat{u}_x \end{bmatrix} = \begin{bmatrix} \dfrac{S_{21}L_{11}}{1-S_{22}L_{11}} & \dfrac{L_{12}}{1-S_{22}L_{11}} \\ \dfrac{S_{21}}{1-S_{22}L_{11}} & \dfrac{S_{22}L_{12}}{1-S_{22}L_{11}} \end{bmatrix} \begin{bmatrix} \hat{u}_{inS} \\ \hat{i}_{oL} \end{bmatrix} \tag{2.25}$$

$$\begin{bmatrix} \hat{i}_{inS} \\ \hat{u}_{oL} \end{bmatrix} = \begin{bmatrix} S_{11} + \dfrac{S_{12}S_{21}L_{11}}{1-S_{22}L_{11}} & \dfrac{S_{12}L_{12}}{1-S_{22}L_{11}} \\ \dfrac{S_{21}L_{21}}{1-S_{22}L_{11}} & L_{22} + \dfrac{S_{22}L_{12}L_{21}}{1-S_{22}L_{11}} \end{bmatrix} \begin{bmatrix} \hat{u}_{inS} \\ \hat{i}_{oL} \end{bmatrix} \tag{2.26}$$

According to [33], the cascaded system is stable internally and in the input-output sense, if the transfer functions in (2.25) and (2.26) are stable. If no RHP pole-zero cancellations take place in $S_{22}L_{11}$, then it is sufficient to verify the stability of one of the transfer functions for stability to exist [33]. If the subsystems S and L are designed originally to be stable (i.e., the transfer functions in (2.24) are stable), then the internal and input-output stability can be analyzed by applying the Nyquist stability criterion to $-S_{22}L_{11}$ [28].

2.4.2 Concept of Minor-Loop Gain

Middlebrook set forth the concept of minor-loop gain in the 1970s, when analyzing the stability of a cascaded system consisting of an EMI filter and a switched-mode converter [30]. Middlebrook defined the minor-loop gain as the ratio of output impedance of the EMI filter and the closed-loop input impedance of the switched-mode converter. Later, the ratio of the output impedance of a converter and the load impedance are also used as minor-loop gain to study the load-imposed instability in publications such as [35]–[38].

When the source and load subsystems in Fig. 2.7 are an EMI filter (i.e. $S_{22} = -Z_{\mathrm{of}}$, where Z_{of} is the output impedance of the EMI filter) and a switched-mode converter (i.e. $L_{11} = Y_{\mathrm{in-c}}$), the internal and input-output stabilities can be analyzed by determining the stability of $Z_{\mathrm{of}}Y_{\mathrm{in-c}} = Z_{\mathrm{of}}/Z_{\mathrm{in-c}}$, i.e., the same minor-loop gain that Middlebrook defined in [30]. Similarly, if the source subsystem is a switched-mode converter (i.e. $S_{22} = -Z_{\mathrm{o-c}}$) and the load subsystem is a load impedance (i.e. $L_{11} = 1/Z_{\mathrm{L}}$), the internal and input-output stabilities are determined by $Z_{\mathrm{o-c}}/Z_{\mathrm{L}}$. This confirms that the minor-loop gain can be used to determine the stability of general cascaded subsystems as also stated in [28] and [33]. The generality means that the minor-loop gain can be defined at an arbitrary interface within the overall system and it will still determine the stability of the overall system perfectly. It should be noted that an interface between two dependent systems is actually not an interface, which can be used for stability analysis as briefly discussed in [89]. The subsystems are dependent of each other, when the control or reference signal for one subsystem is taken from another subsystem. E.g., when output-voltage remote sensing is used to take the feedback from the point-of-load, the converter and the impedance block inside the feedback loop form dependent subsystems.

The IVFF and OCF controls can make the converter behave as a buffer in a system and consequently make it invariant to the source and load interactions. However, such a converter can still become unstable – although originally stable – at the presence of arbitrary source impedance, if the minor-loop gain, i.e., $Z_{\mathrm{s}}Y_{\mathrm{in-c}} = Z_{\mathrm{s}}Y_{\mathrm{in-}\infty}$ does not satisfy the Nyquist stability criterion. The same implication does not hold at the load-side, because the load-side minor-loop gain $Z_{\mathrm{o-c}}/Z_{\mathrm{L}}$ would be zero, because $Z_{\mathrm{o-o}} = 0$. Therefore, the system could not become unstable due to the load interactions.

3 Theoretical and Experimental System Analysis

In this chapter, the stability and performance degradation of systems and converters are discussed based on the publications [P1], [P2] and [P3] as well as previous publications such as [30], [36], [42], [45], [53] and [55]. The existing methods to analyze stability and performance degradation are overviewed and the ambiguities in them are clarified and corrected based on the contribution of [P1] and [P2]. The effect of remote sensing on converter dynamics and system performance is discussed based on theoretical predictions and experimental measurements presented in [P3]. Many Bode diagrams are shown in this chapter. These diagrams show frequency responses of three different types, i.e., predictions, measurements or calculations. The predictions are obtained with mathematical models and measurements with a frequency response analyzer from the experimental systems or converters. The calculations are obtained computationally from measurements, e.g., to remote the effect of a load impedance.

3.1 Forbidden-Region-Based Analysis Criteria

The prevailing practical methods to analyze the stability and performance degradation of the cascaded subsystems are based on criteria stated in terms of forbidden regions in the complex plane out of which the minor-loop gain function should stay. The forbidden regions are typically defined by certain phase and gain margins of the minor-loop gain. A comprehensive summary of the existing criteria is found in [43], where also the conservativeness and simplicity of the different criteria are discussed. The conservativeness of a criterion is typically evaluated by the area in the complex plane that is considered to be forbidden. The simplicity of a criterion is evaluated by the easiness of practical measurement.

Middlebrook's famous criterion [30] defines the forbidden region as an area outside of a circle at origin having radius equal to the inverse of gain margin. Determining the violation of the forbidden region is simple, because only the relative magnitude of the voltages or currents constituting the minor-loop gain needs to be measured [43]. However, the criterion is usually considered to be too restrictive and conservative because it does not allow the impedances at an interface to overlap.

The GMPM criterion presented in [36] and [37] allows the impedances at an interface to overlap with restrictions stated in terms of phase and gain margins of the minor-loop gain. The forbidden region of the GMPM criterion can be defined as the intersection of areas which are defined as the outside of a circle centered at origin having radius equal to the inverse of a certain gain margin and as left-hand side of two sectors defined by a

certain phase margin and the negative portion of the real axis. Therefore, if the impedances at the interface are separated by the amount defined by the gain margin, there are no restrictions for the phase of the minor-loop gain. On the other hand, when the above criterion is not met, the phase difference between the impedances is not allowed to be more than $180 - PM$ or equally less than $-180 + PM$.

The ESAC criterion proposed in [42] is said to be less conservative than the other criteria and argued to be insensitive to component grouping. The forbidden region of the ESAC criterion is defined as the area left to the lines connecting the points where the phase and gain margins are defined, and two horizontal lines outside the unity circle intersecting the other lines at the points where the phase margins are defined. The benefit of ESAC criterion over GMPM criterion is that the lines defining the forbidden region outside the unity circle have constant imaginary parts. The advantage of this is explained in [42] with an example circuit showing that the GMPM criterion is always violated in a certain situation, whereas the ESAC criterion is not, although the criterions are defined by the same gain and phase margins. Common to GMPM and ESAC criteria is that both the magnitude and phase of the signals constituting the minor-loop gain needs to be measured to evaluate the violation of the criteria.

Other forbidden regions also exist, such as the opposing argument criterion introduced in [39] and the criterion proposed in [43], which is based on the opposing argument and Middlebrook's criterion. The opposing argument criterion defines the forbidden region by means of the real part of minor-loop gain, i.e., the real part is not allowed to be smaller than a certain negative value defined by the inverse of a certain gain margin. The criterion presented in [43] combines the opposing argument and Middlebrook's criteria to form a new forbidden region as follows: The opposing argument criterion is used directly for the gain margins smaller than 2 (i.e., 6 dB). For higher gain margins, the forbidden region is defined to be outside of a circle having the radius and center at real axis defined as function of the gain margin. To determine violation of the opposing argument criterion, both the magnitude and phase of the signals constituting the minor-loop gain need to be measured. The combined criterion proposed in [43] is simpler regarding to the measurement, because only magnitudes of the corresponding signals need to be measured. Actually, violation of the opposing argument criterion can also be determined by only measuring the magnitudes of the signals, when the gain margin is 2 [43].

Fig. 3.1 illustrates the differences between the Middlebrook, GMPM, ESAC and opposing argument criteria defined by means of the same gain and phase margins. According to Fig. 3.1, all the criteria prevent the minor-loop gain from encircling the critical point (-1,0), but the conservativeness of the criteria is substantially different. It should be pointed out that the stability of the system is ensured if the minor-loop gain satisfies the Nyquist stability criterion. Therefore, even the ESAC criterion can be violated and still the system can be stable.

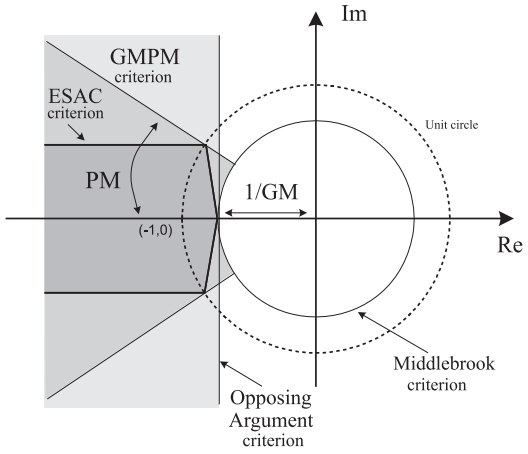


Fig. 3.1 *The typical forbidden-region criterions defined for the same phase and gain margins.*

The phase and gain margins defining the forbidden regions are typically required to be the same as for output-voltage loop gain, i.e., PM of 60 degrees and GM of 6 dB [37]. It is stated in [42] that the interpretation of the phase and gain margins changes meaning when the minor-loop gain is defined at different interfaces. Therefore, the forbidden regions as well as the phase and gain margins should actually be dependent of the interface to ensure adequate performance and robust stability of a system. The phase and gain margins are closely related to the peaking of a sensitivity function defined by the minor-loop gain.

3.2 Stability Considerations

The minor-loop gain defined at an arbitrary interface within the system can be used to study the stability of cascaded subsystems. The system is said to be stable if the minor-loop satisfies the Nyquist stability criterion, i.e., the minor-loop gain must encircle the point (-1,0) counterclockwise in a complex plane as many times as the minor-loop gain has RHP poles [32]. Usually, the individual subsystems are designed so that no RHP-poles exist and the system is therefore stable when the minor-loop gain does not encircle the critical point (-1,0).

3.2.1 Load-Imposed Instability

The minor-loop gain defined at the output of a closed-loop converter can be presented as shown in (3.1), where $Z_{\mathrm{o-c}}$ is the closed-loop output impedance of the converter, and Z_{L} is the load impedance and ϕ_{Zoc} and ϕ_{ZL} are the phases of the corresponding impedances, respectively.

$$L_{\mathrm{M-L}} = \frac{Z_{\mathrm{o-c}}}{Z_{\mathrm{L}}} = \frac{\left|Z_{\mathrm{o-c}}\right|\angle\phi_{\mathrm{Zoc}}}{\left|Z_{\mathrm{L}}\right|\angle\phi_{\mathrm{ZL}}} = \frac{\left|Z_{\mathrm{o-c}}\right|}{\left|Z_{\mathrm{L}}\right|}\angle\left(\phi_{\mathrm{Zoc}} - \phi_{\mathrm{ZL}}\right) \tag{3.1}$$

When the load-side minor-loop gain $L_{\mathrm{M-L}}$ is equal to -1 (i.e., $\left|Z_{\mathrm{o-c}}\right| = \left|Z_{\mathrm{L}}\right|$ and $\phi_{\mathrm{Zoc}} - \phi_{\mathrm{ZL}}$ = 180 degrees), the system consisting of the converter and the load is said to be

marginally stable [32]. If the magnitudes of the impedances further overlap (i.e., $|L_{M-L}|>1$), when the phase difference is 180 degrees, the minor-loop gain encircles the point (-1,0) indicating instability (providing that no RHP-poles exist in the minor-loop gain). Therefore, the Bode diagram of the closed-loop output impedance can be used to determine the safe-load profile, which ensures stability, for a given converter as discussed in [P1].

Examples of closed-loop output impedances of buck converters under VMC (solid), PCMC (dashed) and PCMC-OCF (dash-dotted) are shown in Fig. 3.2a. The converters have the same power stages, operation points and essentially the same voltage-loop gain-crossover frequencies [P1], [P4]. Examples of load impedances within distributed power systems are shown in Fig. 3.2b. The solid and dashed lines in Fig. 3.2b represent the input impedances of VM and PCM-controlled buck converters, respectively. The dotted line (LC+VMC) represents the input impedance of a subsystem consisting of an EMI filter and VM-controlled buck converter and the dash-dotted line (C) represents the impedance of a capacitor with the effect of equivalent series resistance. An example Matlab m-file to model the dynamics of a buck converter under different control methods discussed in the thesis is shown in Appendix A.

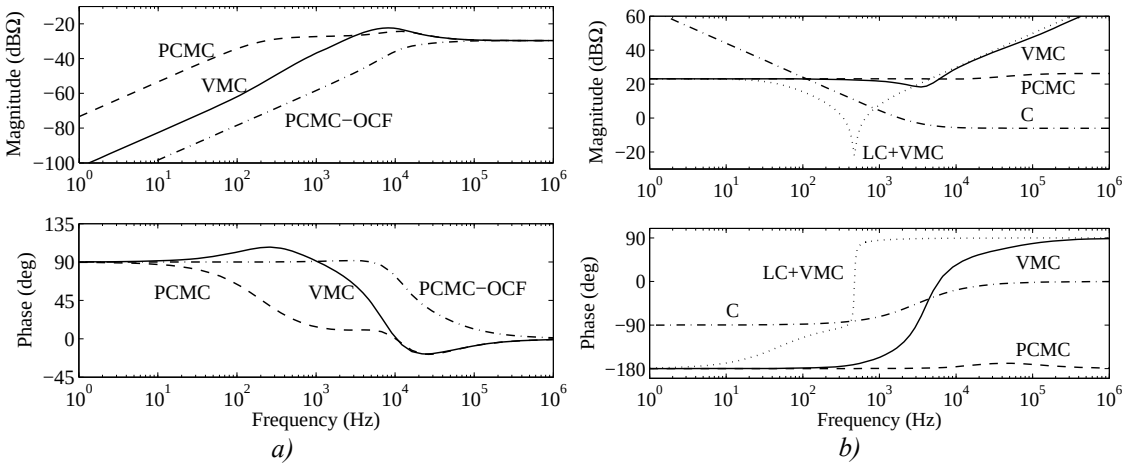


Fig. 3.2 *Examples of closed-loop output (a) and load (b) impedances within distributed systems.*

As discussed in [P1], the buck converter under VMC is most susceptible to instability due to capacitive loading (dash-dotted line in Fig. 3.2b), because of the phase behavior of the closed-loop output impedance, i.e., the phase is near or above 90 degrees at the same frequency range where the phase of the capacitive load is near -90 degrees. The PCM-controlled converter may become unstable due to the capacitive loading only at very low frequencies, where the magnitude of the closed-loop output impedance is the lowest. The PCM-controlled converter with output-current feedforward may become unstable due to the capacitive loading at the widest frequency range. However, the magnitude of the output impedance of the converter under PCMC-OCF is much lower at these frequencies making the impedance overlap less likely in practice.

3.2.2 Source-Imposed Instability

The minor-loop gain defined at the input of a converter (i.e., internal EMI filters and input capacitors are considered as parts of the source subsystem rather than parts of the converter subsystem) can be presented as shown in (3.2), where Z_s is the source impedance seen by the converter and Z_{in-c} is the closed-loop input impedance of the converter. Similarly to load-imposed instability, the system is marginally stable, if $L_{M-S} = -1$, and slight overlap of the impedances would result to an unstable system.

$$L_{M-S} = \frac{Z_s}{Z_{in-c}} = \frac{|Z_s|\angle\phi_{Zs}}{|Z_{in-c}|\angle\phi_{Zinc}} = \frac{|Z_s|}{|Z_{in-c}|}\angle(\phi_{Zs} - \phi_{Zinc}) \tag{3.2}$$

Fig. 3.3a shows examples of input impedances of VM (solid), PCM (dashed) and IVFF-controlled (dash-dotted) buck converters. The power stages, operation points and the voltage-loop gain-crossover frequencies of the converters are essentially the same. Examples of source impedances within systems are shown in Fig. 3.3b, where the solid and dashed lines represent the closed-loop output impedances of VM and PCM-controlled buck converters, respectively. The dash-dotted line represents a typical output impedance of a single-section LC filter.

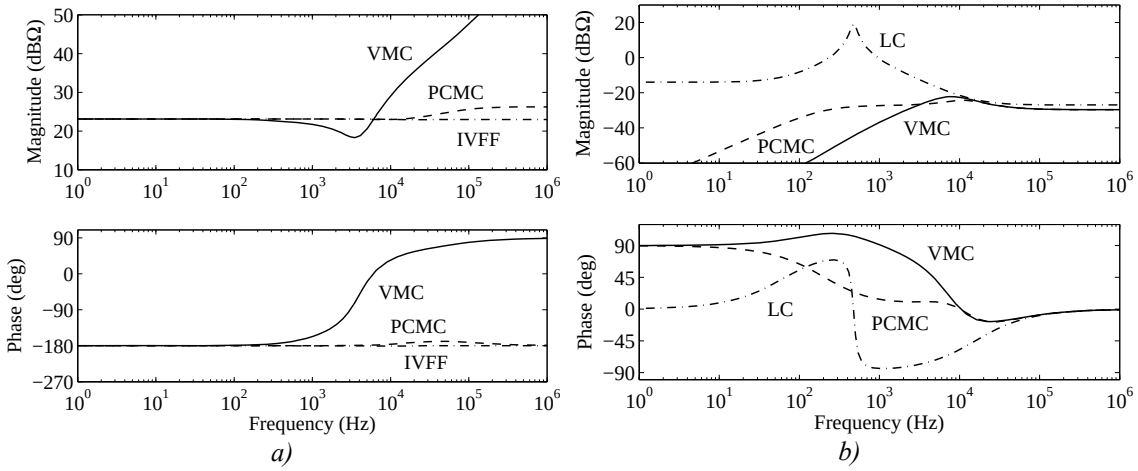


Fig. 3.3 *Examples of closed-loop input (a) and source (b) impedances within distributed systems.*

According to Fig. 3.3a, the buck converter under PCM and IVFF controls is most susceptible to source-imposed instability at the whole frequency range due to the phase behavior, i.e. the phase is close to -180 degrees. The buck converter under VMC is less sensitive due to the increased input impedance at high frequencies. According to Fig. 3.3b, the source-imposed instability occurs most likely at the vicinity of resonant frequency of the EMI filters due to the high peak of the output impedance or at the vicinity of the peak of the output impedance, i.e., at the vicinity of the voltage-loop gain-crossover frequency.

3.3 Performance Degradation

As discussed in Chapter 1, the term performance can not be explicitly defined, because criteria for it can vary from one application to another. When the individual converters, which are designed to meet the performance criteria in a laboratory environment, are interconnected to form a distributed system, it would be advantageous to have the performance of the converters unaffected. On the other hand, some performance degradation may be tolerated based on the criteria set for the subsystems, e.g., if the distribution bus does not need to be tightly regulated [8], [9]. Therefore, methods with which the performance of the system can be evaluated or predicted in practice are important for system designers.

The forbidden-region-based criteria discussed in Section 3.1 are also used to evaluate the performance degradation of converters. It should be noted that the forbidden region of Middlebrook's criterion was originally defined for the system consisting of an EMI filter and a VM-controlled converter in CCM as a practical design rule to ensure stability and possibly adequate performance of the converter. The forbidden regions of the GMPM and opposing argument criteria are, however, typically defined for the minor-loop gain at the output of a bus converter and, therefore, the performance degradation analyses are focused on the bus converter. The ESAC criterion is not defined at any specific interface and, therefore, the performance degradation analyses are not discussed in [42]. Despite the different bases for the criteria, they are used similarly to evaluate the performance degradation of cascaded systems [43].

Fig. 3.4 shows a system based on IBA, which consists of a bus converter, a POL converter with an EMI filter and a load. The POL converter is usually equipped with input capacitor C_{in} as shown in Fig. 3.4. The different interfaces, where minor-loop gains can be determined, are depicted with $\text{A}_1 - \text{A}_5$.

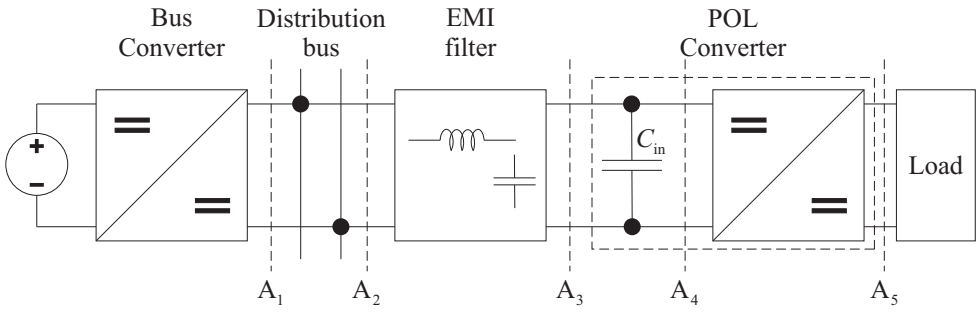


Fig. 3.4 *The different interfaces to determine minor-loop gains within a system.*

It is obvious that the performance degradation of the bus converter due to the load interactions can be most accurately analyzed by determining the minor-loop gain at the interface A_1, i.e., the interface, where the output-voltage feedback is taken for the bus converter. Similarly, interface A_5 would provide most accurate information on the load interactions of the POL converter. These interfaces are also typically available for

measurements in commercial converter modules. However, the situation is more complex for source interaction analyses of the POL converter. According to [26], EMI filters and input capacitors should be considered as parts of the source subsystem rather than parts of the converter, when analyzing the source interactions. Hence, the interface A_4 would be the key interface in source-interaction analysis of the POL converter as also implicitly defined in [30] and [55]. However, the interface is seldom available for measurement in commercial converter modules. The minor-loop gains at the physical input of the POL converter (i.e., A_3) and at the other interfaces (i.e., A_1 and A_2) may not contain at all the information of the possible source-imposed performance degradation of the POL converter as demonstrated in [P2]. In addition, the robustness of stability should be evaluated with different phase and gain margins for different interfaces as implicitly discussed in [42].

In this section, the performance-degradation of converters and the system based on them are analyzed with the minor-loop gain defined at the key interfaces shown in Fig. 3.4, i.e., A_1 and A_5 for the load-interaction and A_4 for the source-interaction analysis. The validity of the existing forbidden-region-based design rules for performance evaluation and prediction are discussed, and the vagueness of them is clarified.

3.3.1 Effect of Minor-Loop Gain Stability Margins

In control theory [32], [34], [90], the performance of a feedback system is usually addressed to transient response and disturbance rejection of the system in time and frequency domains. Typically, it is required that the sensitivity and the complementary sensitivity functions of the feedback system must stay below some predefined values for robust stability and adequate transient-performance to exist. The phase and gain margins associated with the feedback loop of the system are closely related to sensitivity and complementary sensitivity functions [90].

According to Section 2.4, the minor-loop gain defined at an interface between two general subsystems can be viewed as the system loop gain and, therefore, the system performance degradation can be evaluated by studying the sensitivity function of the minor-loop gain shown in (3.3), where L_{M} represents either the load or source-side minor-loop gain depending on which of the subsystems contains the converter of interest. Subscripts "-L" and "-S" are used to distinguish the minor-loop gains (and sensitivity functions) defined at the load or source-side of the converter, respectively. Note that the discussion presented here for the sensitivity function is general, and therefore can also be applied to voltage-loop gain analysis.

$$S_{\mathrm{M}} = \frac{1}{1 + L_{\mathrm{M}}} \tag{3.3}$$

According to Chapter 2, the load-affected closed-loop output impedance ($Z_{\mathrm{o-c}}^{\mathrm{L}}$) and input-to-output transfer function ($G_{\mathrm{io-c}}^{\mathrm{L}}$) of a converter can be expressed as shown in

(3.4). According to $Z_{\mathrm{o-c}}S_{\mathrm{M-L}}$ in the upper row in (3.4), the load-affected output impedance would be higher than the corresponding internal closed-loop output impedance, if the sensitivity function $S_{\mathrm{M-L}}$ is higher than unity at some frequency range. That indicates that the interactions have increased the impedance and, therefore, the load-transient response may be deteriorated [91]. However, the transient response may not be significantly deteriorated if the sensitivity function is higher than unity at frequencies where the voltage-loop gain L_{v} is high, as can be concluded from the last expression in the upper row in (3.4). Similar conclusions also apply for the load-affected closed-loop input-to-output transfer function as shown in the bottom row in (3.4).

$$\begin{aligned} Z_{\mathrm{o-c}}^{\mathrm{L}} &= \frac{Z_{\mathrm{o-o}}^{\mathrm{L}}}{1+L_{\mathrm{v}}^{\mathrm{L}}} = \frac{Z_{\mathrm{o-c}}}{1+L_{\mathrm{M-L}}} = Z_{\mathrm{o-c}}S_{\mathrm{M-L}} = \frac{Z_{\mathrm{o-o}}S_{\mathrm{M-L}}}{1+L_{\mathrm{v}}} \\ G_{\mathrm{io-c}}^{\mathrm{L}} &= \frac{G_{\mathrm{io-o}}^{\mathrm{L}}}{1+L_{\mathrm{v}}^{\mathrm{L}}} = \frac{G_{\mathrm{io-c}}}{1+L_{\mathrm{M-L}}} = G_{\mathrm{io-c}}S_{\mathrm{M-L}} = \frac{G_{\mathrm{io-o}}S_{\mathrm{M-L}}}{1+L_{\mathrm{v}}} \end{aligned} \tag{3.4}$$

The source-affected closed-loop input-to-output transfer function ($G_{\mathrm{io-c}}^{\mathrm{S}}$) and closed-loop output impedance ($Z_{\mathrm{o-c}}^{\mathrm{S}}$) of a converter can be expressed as shown in (3.5). The previous analysis of the load interactions also applies to the input-to-output transfer function in the case of source interactions, as shown in the upper row in (3.5). However, the effect of the source-side sensitivity function $S_{\mathrm{M-S}}$ on the source-affected closed-loop output impedance does not give the total effect of the source interactions, because the interactions may also be reflected via the short-circuit input admittance, as shown in the bottom row in (3.5).

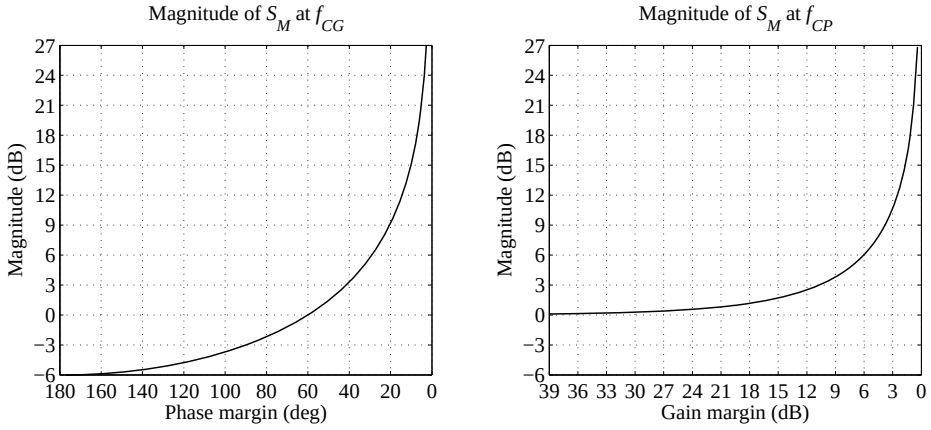
$$\begin{aligned} G_{\mathrm{io-c}}^{\mathrm{S}} &= \frac{G_{\mathrm{io-o}}^{\mathrm{S}}}{1+L_{\mathrm{v}}^{\mathrm{S}}} = \frac{G_{\mathrm{io-c}}}{1+L_{\mathrm{M-S}}} = G_{\mathrm{io-c}}S_{\mathrm{M-S}} = \frac{G_{\mathrm{io-o}}S_{\mathrm{M-S}}}{1+L_{\mathrm{v}}} \\ Z_{\mathrm{o-c}}^{\mathrm{S}} &= \frac{Z_{\mathrm{o-o}}^{\mathrm{S}}}{1+L_{\mathrm{v}}^{\mathrm{S}}} = \frac{1+Z_{\mathrm{s}}Y_{\mathrm{in-sc}}}{1+L_{\mathrm{M-S}}}Z_{\mathrm{o-c}} = \left(1+Z_{\mathrm{s}}Y_{\mathrm{in-sc}}\right)Z_{\mathrm{o-c}}S_{\mathrm{M-S}} \end{aligned} \tag{3.5}$$

The relative stability margins of the minor-loop gain are of great importance regarding the peaking of the corresponding sensitivity function S_{M}. It can be shown that the magnitude of the sensitivity function is related to the phase margin of the minor-loop gain at the gain-crossover frequency f_{CG} (i.e., the frequency, where the minor-loop gain crosses 0-dB level) as shown in (3.6) and to the gain margin at the phase-crossover frequency f_{CP} (i.e., the frequency, where the phase of the minor-loop gain is equal to 180 or -180 degrees) as shown in (3.7) [90]. Similar equations are also used in [36] to analyze the peaking of the bus impedance of a system, i.e., the load-affected output impedance of the bus converter.

$$\left|S_{\mathrm{M}}\left(f_{\mathrm{CG}}\right)\right| = \frac{1}{\sqrt{2\left(1-\cos\left(PM\right)\right)}} = \frac{1}{2\sin\left(PM/2\right)} \tag{3.6}$$

$$\left|S_{\mathrm{M}}\left(f_{\mathrm{CP}}\right)\right| = \frac{1}{1-1/GM} \tag{3.7}$$

The magnitude of the sensitivity function as a function of phase and gain margin is shown in Figs. 3.5a and 3.5b, respectively. According to Fig. 3.5, the magnitude of the sensitivity function can peak substantially due to the low phase and/or gain. Note that the magnitude of the sensitivity function and the gain margin are expressed in terms of real numbers in (3.6) and (3.7), whereas they are in dB in Fig. 3.5.



a) *b)*

Fig. 3.5 *The magnitude of the sensitivity functions as a function of the phase (a) and gain (b) margin.*

Eqs. (3.6) and (3.7) define the peaking of the sensitivity function only at gain and phase-crossover frequencies but the sensitivity function can also peak at other frequencies depending on the magnitude and phase of the minor-loop gain. In control theory [90], a more general requirement for the peak value of the sensitivity function $|S_{\mathrm{M}}|_{\max}$ is that it should be equal or lower than a certain predefined value M regardless of frequency. When the minor-loop gain in (3.3) is expressed in real and complex parts (i.e., $L_{\mathrm{M}} = \alpha + j\beta$), the inequality $|S_{\mathrm{M}}|_{\max} \le M$ can be expressed in generally as

$$(\alpha+1)^2 + \beta^2 \ge \left(\frac{1}{M}\right)^2, \tag{3.8}$$

which represents an area outside of a circle that has the radius equal to $1/M$ at the point (-1,0) in the complex plane. The implication is that, if the minor-loop gain stays out of this circle in complex plane for the whole frequency range, the peak value of the sensitivity function is always less than the value defined by M. E.g., when M is 2 (6 dB), the radius of the circle is 0.5. The corresponding peaking at the gain and phase crossover frequencies is obtained with $\mathrm{PM} \approx 29$ degrees and $\mathrm{GM} = 6$ dB, respectively. The situation is illustrated in Fig. 3.6, where the solid line represents the circle defined by (3.8), when M is 2. The forbidden regions of the GMPM (dashed line) and ESAC

(dash-dotted line) criteria for the corresponding phase and gain margins calculated above are also shown in Fig. 3.6.

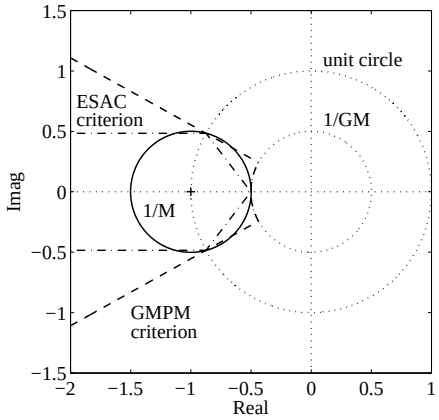


Fig. 3.6 *The sensitivity circle with a radius of 1/M at the point (-1,0) and the corresponding GMPM and ESAC criterions.*

According to Fig. 3.6, the forbidden region defined by the circle occupies much less area in complex plane than the GMPM and ESAC criterions. However, within the unit circle, the ESAC criterion is less restrictive than the criterion defined by the circle implying that the sensitivity function can peak more than expected for certain PM and GM values, when the ESAC criterion is used. On the other hand, the GMPM criterion is typically more restrictive than the criterion defined by the circle implying less peaking, when GMPM criterion is used. Both ESAC and GMPM criteria can be violated outside the unit circle without inducing excess peaking of the sensitivity function (providing that the criterion defined by the circle is not violated).

The GMPM criterion is clearly derived from the allowed peaking of the sensitivity function at phase and gain-crossover frequencies, although not explicitly shown in [36]. In addition, the opposing argument criterion [39] and the combined criterion [43] are also implicitly derived based on the allowed peaking of the complementary sensitivity function, i.e., $T_{\mathrm{M}} = L_{\mathrm{M}} / \left(1 + L_{\mathrm{M}}\right)$, which is analyzed by M-circles in control theory [90]. However, the ESAC criterion is derived solely to maintain the stability with certain phase and gain margins. According to (3.4) and (3.5), the sensitivity function S_{M} clearly has a physical meaning in the load and source interactions, while the complementary sensitivity function does not. Therefore, the usefulness of the prevailing forbidden-region-based criteria may be argued when the peaking of various closed-loop transfer functions are of concern. In [92] and [93], the sensitivity-circle-based performance analyses for output-voltage loop gains of switched-mode converters are discussed, but the analyses are not focused on minor-loop gains. In [88], the importance of the sensitivity function defined by the minor-loop gain regarding to robust stability and performance is briefly discussed.

The simplicity of measurement to determine the possible violation of the different forbidden regions is an important issue [43]. Both the voltage and current perturbation methods can be used to measure the necessary signals constituting the minor-loop gain or the criterion on which the forbidden-region-based design rules are based [40]. The original Middlebrook's criterion and the new criterion proposed in [43] only need the magnitude information of the voltage or current signals, whereas the other criteria, i.e., GMPM, ESAC and opposing argument criteria, need both the magnitude and phase information. It can be shown that only magnitude information of the necessary voltage or current signals need to be measured to evaluate violation of the sensitivity-circle-based criterion discussed above as done implicitly for the voltage perturbation method in [40]. However, the measurement of only the magnitudes of the signals constituting the sensitivity function does not provide information on the encirclement of the critical stability point in complex plane.

3.3.2 Load-Side Minor-Loop-Gain-Based Voltage-Loop Analysis

So far, the effect of the stability margins of the minor-loop-gain on different closed-loop transfer functions has been discussed with the sensitivity function. It is shown that the system performance, i.e., the transient response and noise attenuation, can be deteriorated due to the possible peaking of the sensitivity function and, consequently, also peaking of the closed-loop output impedance and input-to-output transfer function.

As discussed in Section 2.2, the load and source interactions affect the dynamics of a converter through the open-loop parameters. Especially, the voltage-loop gain of the converter is affected via the open-loop output impedance. For good dynamic performance to exist, both adequate phase and gain margins and the gain-crossover frequency of the voltage-loop gain are important. Therefore, the relation between the load-side minor-loop gain and the corresponding load-affected voltage-loop gain has been studied intensively in publications such as [20], [36] and [45]–[48]. The analyses done especially in [36] and [48] are basically correct but the conclusions the authors come to are vague and misleading. Therefore, the relation between the load-side minor-loop gain and the voltage-loop gain of the corresponding converter deserves to be analyzed and the vagueness of the previous publications corrected.

Fig. 3.7 illustrates a system consisting of a closed-loop converter and a general load subsystem. The converter is presented with the two-port and feedback networks. The load subsystem is presented as the input-port of its two-port network representation. In Fig. 3.7, $Z_{\mathrm{o-c}}$ is the internal closed-loop output impedance of the converter, when it is loaded with the ideal current sink (i.e., $Z_{\mathrm{L}} = \infty$), $L_{\mathrm{v}}^{\mathrm{L}}$ is the voltage-loop gain of the converter, when the effect of the load impedance Z_{L} is included in the model, and $Z_{\mathrm{o-c}}^{\mathrm{L}}$ is the load-affected closed-loop output impedance, i.e., the parallel combination of $Z_{\mathrm{o-c}}$ and Z_{L}, which can be expressed as shown in (3.9), where the load-side minor-loop gain $L_{\mathrm{M-L}} = Z_{\mathrm{o-c}} / Z_{\mathrm{L}}$.

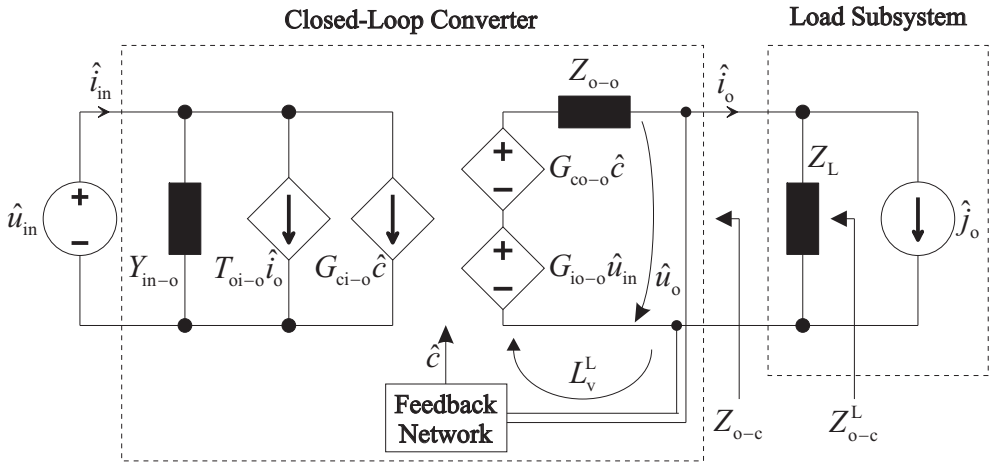


Fig. 3.7 *The two-port network of a closed-loop converter and the input-port of a general load subsystem.*

$$Z_{o-c}^{L} = \frac{Z_{o-c}}{1+L_{M-L}} = \frac{Z_{o-o}^{L}}{1+L_{v}^{L}} \tag{3.9}$$

The load-transient response of the system (i.e., the response of the output voltage $\hat{u}_o$ to the changes in $\hat{j}_o$) is characterized by the load-affected closed-loop impedance Z_{o-c}^{L} and, therefore, excess peaking due to the minor-loop gain L_{M-L} may result in deteriorated transient response as discussed in Section 3.3.1. According to Chapter 2, the load-affected closed-loop output impedance can also be expressed by the load-affected open-loop output impedance and voltage-loop gain as shown in the last expression in (3.9), where $Z_{o-o}^{L} = Z_{o-o}/(1+Z_{o-o}/Z_L)$ and the load-affected voltage-loop gain as shown in (3.10). Therefore, the possibly deteriorated load-transient response of the system can also be stated in terms of the load interactions on the open-loop output impedance and the voltage-loop gain.

$$L_{v}^{L} = \frac{L_v}{1+Z_{o-o}/Z_L} \tag{3.10}$$

There seems to be ambiquity in [36] and [48] concerning the relation between the relative stability margins of the load-side minor-loop gain and the corresponding margins of the voltage-loop gain of the loaded converter: it is stated that the stability margins of the voltage-loop gain are equal to the corresponding margins associated to the minor-loop gain. Moreover, it is stated that the minor-loop gain-crossover frequencies also determine the crossover frequencies of the voltage-loop gain. However, these assumptions are not generally true as demonstrated in [P1]. In [36], the voltage-loop gain of the loaded converter (i.e., L_v^L) is represented as a function of minor-loop gain as shown in (3.11). It can be shown that (3.11) is equal to (3.10), when the closed-loop output impedance is replaced by $Z_{o-o}/(1+L_v)$ in the minor-loop gain indicating that also (3.11) can be used to calculate the load-affected voltage-loop gain with appropriate computational tools. However, the formula of L_v^L presented in (3.10) is

much simpler than (3.11) and, therefore, it can be used more easily, e.g., with graphical analysis. The authors of [45]–[47] derive the same equation for the load-affected voltage-loop gain (i.e. (3.11)) and make the same vague conclusion as in [36].

$$L_{\mathrm{v}}^{\mathrm{L}} = \frac{L_{\mathrm{v}}}{1 + L_{\mathrm{M-L}}\left(1 + L_{\mathrm{v}}\right)} \tag{3.11}$$

The analysis made in [36] with (3.11) is divided into four different cases:

1) The closed-loop output and load impedances at the output of the converter are well separated and, hence, impedance overlap does not exist (i.e., $\left|L_{\mathrm{M-L}}\right| \ll 1$) and the load-affected voltage-loop gain $L_{\mathrm{v}}^{\mathrm{L}}$ is then equal to the internal voltage-loop gain L_{v}.
2) The overlap (i.e., $\left|L_{\mathrm{M-L}}\right| \gg 1$) occurs at frequencies well above the voltage-loop gain-crossover frequency (i.e., typically $\left|L_{\mathrm{v}}\right| \ll 1$) and, hence, the load-affected voltage-loop gain is approximately equal to $L_{\mathrm{v}}/L_{\mathrm{M-L}}$.
3) The overlap occurs at frequencies well below the voltage-loop gain-crossover frequency (i.e., typically $\left|L_{\mathrm{v}}\right| \gg 1$) and, hence, the load-affected voltage-loop gain is approximately equal to $1/L_{\mathrm{M-L}}$.
4) The overlap occurs at the vicinity of the voltage-loop gain-crossover frequency, which is simply considered to be a combination of cases 2 and 3, i.e., case 4 is equal to case 3 at frequencies below the gain crossover frequency and equal to case 2 at frequencies above the crossover.

According to [36], the load-affected voltage-loop gain $L_{\mathrm{v}}^{\mathrm{L}}$ is equal to the internal voltage-loop gain L_{v}, when the impedance overlap does not exist (i.e., the case 1). However, this is not generally true, because the voltage-loop gain can change via the open-loop output impedance although $\left|L_{\mathrm{M-L}}\right| \ll 1$ as can be concluded from (3.10). A good demonstration of this situation is found in [94]. Similarly, in case 4, it is not comprehensively discussed and analyzed when the interactions occur at the vicinity of the gain-crossover frequency, because the conclusions made for cases 2 and 3 do not hold for frequencies where the voltage-loop gain is close to unity as discussed and demonstrated in [P1].

Some of the vagueness of the conclusion concerning the load-affected voltage-loop gain made in [36] is corrected in [48] with more precise analysis. The discussed cases are the same as in [36], but the analyses are done with the magnitudes of $L_{\mathrm{M-L}}$ and the product $L_{\mathrm{M-L}}L_{\mathrm{v}}$. Despite the more accurate analyses, the case where the interactions occur at the vicinity of the gain-crossover frequency of the voltage-loop gain is discussed in the same way as in [36] (i.e., case 4 is combination of cases 2 and 3). It is clearly stated in [48], that the gain-crossover frequency and phase margins of the load-affected voltage-loop gain are determined directly by the minor-loop gain. However, based on the experimental example provided in [48], this is not evident. The load-affected voltage-

loop gain and the inverse of the minor-loop gain are shown in Fig. 5b in [48] to demonstrate the inverse relation between them. The magnitudes track each other quite well from low frequencies to second gain-crossover frequency of the minor-loop gain. However, the phase margins of the minor-loop and voltage-loop gains are roughly the same but not identical at either gain-crossover frequency of the minor-loop gain. Similarly, in Fig. 6d in [48] the gain-crossover frequency of the voltage-loop gain is reduced although the minor-loop gain is below unity at the frequency range near the crossover. The phases of the corresponding voltage and minor-loop gains are not shown, and therefore the possible change in phase margin cannot be determined.

The magnitude of the voltage-loop gain is an important factor when considering the relation between the load-affected voltage-loop and the corresponding minor-loop gain [P1]. The experimental examples provided in [36] and [48] are made so that the minor-loop gain-crossover frequencies occur at frequencies where the voltage-loop gain is relatively high or low compared to unity, and therefore the case of the voltage-loop gain being close to unity is not actually considered. The impedance interactions usually occur at the vicinity of the gain-crossover frequency of the voltage-loop gain, i.e., the frequency range, where the closed-loop output impedance is the highest. Therefore, the case in which the load-side minor-loop gain is close to unity at the vicinity of this frequency range should be analyzed carefully to determine the changes in gain-crossover frequency and the stability margins of the voltage-loop gain.

In [P1], the relation between the load-side minor-loop gain and the voltage-loop gain of a loaded converter is analyzed in a different way. The load impedance for the converter is expressed with the closed-loop output impedance and the phase and gain margins of the minor-loop gain as shown in (3.12). The corresponding load-affected voltage-loop gain was computed then with (3.10). The magnitude of the resulting load impedance is always above (or below) the magnitude of the closed-loop output impedance by the amount defined by the gain margin GM in dB. The phase difference of the closed-loop output and load impedances is always less (or more) than 180 degrees defined by the amount of PM in degrees. Consequently, the resulting minor-loop gain represents a single point in the complex plane for the whole frequency range of interest.

$$Z_{\mathrm{L}} = \left|Z_{\mathrm{L}}\right| \angle \phi_{\mathrm{ZL}} = 10^{\frac{GM_{\mathrm{dB}}}{20}} \left|Z_{\mathrm{o-c}}\right| \angle \left(\phi_{\mathrm{Zo-c}} - 180° + PM\right) \tag{3.12}$$

Fig. 3.8 shows the internal (solid) and load-affected (dashed and dash-dotted lines) voltage-loop gains of a VM-controlled buck converter, when the load impedances are calculated by (3.12) with the gain margin of 0 dB and the phase margins of 60 (1, dashed line) and -60 degrees (2, dash-dotted line). Therefore, Fig. 3.8 illustrates the relation between the 60-degree phase margin of the minor-loop gain and the corresponding load-affected voltage-loop gain at different frequencies (i.e. the magnitude of the internal voltage-loop gain varies with the frequency being high at low

frequencies and decreasing at mid frequencies and, eventually, becoming smaller than unity at high frequencies).

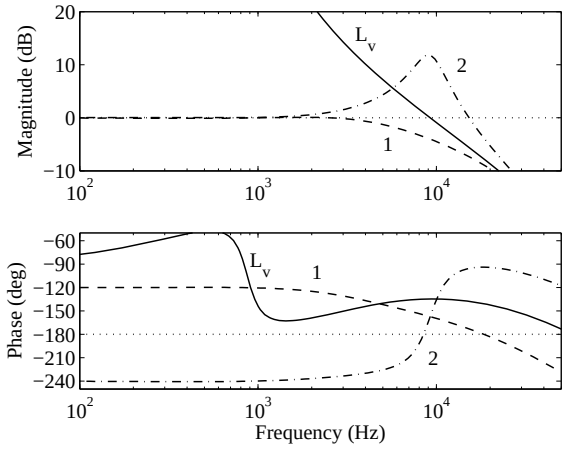


Fig. 3.8 *Predicted load-affected voltage-loop gains of a VM-controlled buck converter, when the artificial load impedance is calculated with GM = 0 dB and PM = 60 degrees (1, dashed line) and GM = 0 dB and PM = -60 degrees (2, dash-dotted line).*

According to Fig. 3.8, the inverse relation $L_v^L \approx 1/L_{M-L}$ only holds at low frequencies, where the magnitude of the internal voltage-loop gain is very high. The inverse relation diminishes rapidly when the magnitude of the voltage-loop gain is approximately below 20 dB. Therefore, the phase margin of the minor-loop gain cannot determine the phase margin of the load-affected voltage-loop gain in general, when the interactions take place at the vicinity of the gain-crossover frequency of the internal voltage-loop gain. In addition, the highest gain-crossover frequency of the load-affected voltage-loop gain can decrease (i.e., 2.5 kHz for line 1) or increase (i.e., 15.1 kHz for line 2) from the original value (i.e., 9.3 kHz for line L_v) as shown in Fig. 3.8.

Similar analysis is presented in [P1] for a PCM-controlled buck converter with the identical power stage and operation conditions. The load impedances were calculated with a gain margin of 6 dB and phase margins of 60 and 0 degrees. According to Fig. 8 in [P1], the gain-crossover frequency of the voltage-loop gain can change eventhough the impedances at the output of the converter do not even overlap (i.e. GM = 6 dB).

Experimental evidence of the situation is provided in [P1] with both VM and PCM-controlled buck converters having the same power-stage, operation point and resonant type load. The measured minor-loop gains at the output of the converters are shown in Fig. 3.9a. The minor-loop gain for the VM-controlled converter indicates slight impedance overlap at frequencies from 7.6 to 11.1 kHz, whereas the impedance overlap is not present for the PCM-controlled converter. The phase margins of the minor-loop gain for the VM-controlled converter are 132 and 155 degrees at the above gain-crossover frequencies, respectively. The internal and load-affected voltage-loop gains of the converters are shown in Fig. 3.9b. The internal voltage-loop gains are shown as

solid (PCMC) and dashed (VMC) lines and the load-affected voltage-loop gains as dotted (PCMC) and dash-dotted (VMC) lines.

The gain-crossover frequencies of both of the internal voltage-loop gains are approximately 11 kHz. According to Fig. 3.9b, the crossover frequencies are reduced approximately to 6 kHz for the both converters and the phase margins are improved (i.e., from 55 to 88 degrees for the PCM-controlled converter and from 47 to 63 degrees for the VM-controller converter). Consequently, the relation between the crossover frequencies and the phase margins of the minor-loop and voltage-loop gains are weak when the interactions occur at the vicinity of the gain-crossover frequency of the internal voltage-loop gains.

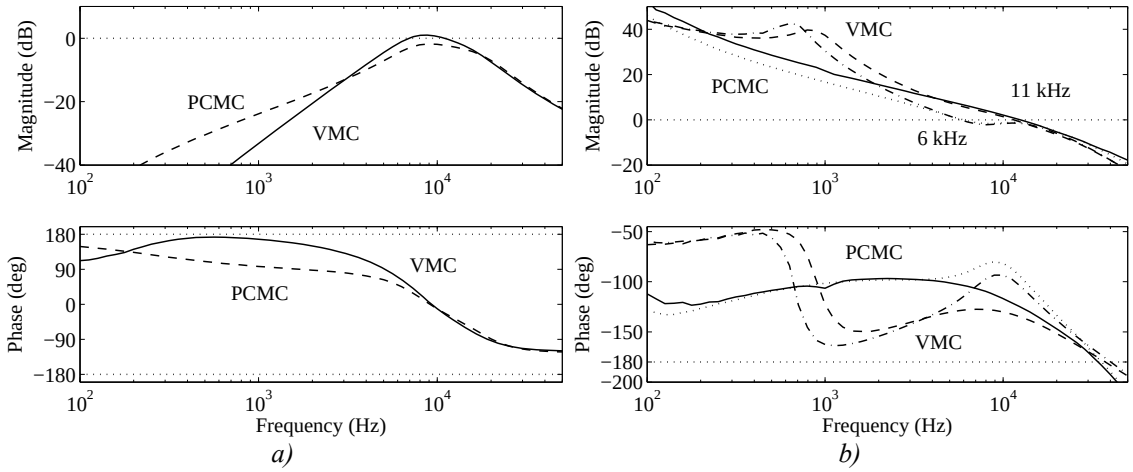


Fig. 3.9 *The measured minor-loop gains (a) and the corresponding effects on the voltage-loop gains (b): the internal voltage-loop gains (VMC: dashed line, PCMC: solid line) and load-affected voltage-loop gains (VMC: dash-dotted line, PCMC: dotted line).*

In summary, the relation between the minor-loop gain defined at the output of a converter and the corresponding load-affected voltage-loop gain can be analyzed with (3.10) and (3.11), both accurately predicting the voltage-loop gain when computational software is used. However, the graphical analysis method can be used with (3.10) more conveniently, because only the magnitudes and phases of the open-loop output and load impedances have to be considered. The inverse relation between the minor-loop gain and the voltage-loop gain only holds at the frequencies where the magnitude of the voltage-loop gain is much higher than unity and, therefore, performance degradation at the vicinity of the gain-crossover frequency of the voltage-loop gain should be considered carefully. The gain margin associated with the load-side minor-loop gain should be increased at the vicinity of the gain-crossover frequency of the voltage-loop gain, if the crossover frequency is not allowed to change much [P1]. Information of the internal properties (i.e., open-loop output impedance and voltage-loop gain) of a converter is always needed when predicting the changes of the voltage-loop gain. The load-side minor-loop gain provides useful information on the peaking of the closed-loop output impedance and input-to-output transfer function. However, the peaking may not

deteriorate the performance significantly if it occurs at the frequencies where the voltage-loop gain is high. Therefore, performance degradation can not be accurately analyzed solely by means of the load-side minor-loop gain.

3.3.3 Source-Side Minor-Loop-Gain-Based Voltage Loop and Output Impedance Analysis

The stability and performance degradation analyses of loaded converters with the minor-loop gain have received plenty of attention as discussed in the previous section. On the other hand, the stability and performance degradation of converters with the source-side minor-loop gain are not discussed as widely although the forbidden-region-based criteria are clearly utilized in source-interaction analyses [35], [43]. In [30], Middlebrook originally formulated the situation as an EMI-filter design problem by defining design rules which ensure that the performance of the converter is unaffected in the presence of an EMI filter. These rules are applicable only for basic VM-controlled converters in CCM and are presented in such a way that the relation between the source-side minor-loop gain and the source-affected voltage-loop gain cannot be recognized. However, Middlebrook also defined a practical design rule based on the minor-loop gain (i.e., it should stay inside the circle defined by the inverse of gain margin as discussed in Section 3.1), which ensures stability and adequate performance of the converter, if the gain margin is sufficiently large. In [49]–[51], Middlebrook's design rules have been modified to also be applicable for CM-controlled converters by y-parameter representation of the converter at open loop. The formulation is, however, not general and therefore not usable for all types of control methods. In [54], the input-filter design procedure is generalized by EET [56] to converters that have non-zero source impedance and an EMI filter at the input of the converters. The conditions for unaffected performance are derived based on the parameters of a converter loaded with resistive load and the parameters of the input filter, instead of considering the internal dynamics or the minor-loop gain.

In [53], an experimental method to analyze the effect of source impedance on the voltage-loop gain, closed-loop output impedance and input-to-output transfer function has been derived. The expressions are derived as a function of the source-side minor-loop gain. According to [53], the performance can be accurately predicted based on the "nominal" transfer functions, i.e., closed-loop input impedance and two different voltage-loop gains L_0 and L_∞, which are the voltage-loop gains of the converter, when the source impedance is assumed to be equal to zero and infinity, respectively. However, the authors do not explicitly define the conditions where the nominal transfer functions are obtained, e.g., what type of load has to be used or if there are additional components such as an internal EMI filter or input capacitors connected at the input.

According to Fig. 7 in [53], the analyses are done at the interface between the external source impedance and the internal input filter of the converter, which is loaded with a resistive load, and not at the true input of the converter. The experimental results

provided in [53] are obtained with a CM-controlled converter. However, the interface and the type of the load where the analysis is done are not explicitly shown. In addition, the effect of the slope of the compensation ramp is not discussed, although it significantly affects the level of possible source interactions as discussed in [57] and [63]. The use of the voltage-loop gain L_∞ is also problematic as such a voltage-loop gain does not exist in practice, because it represents the voltage-loop gain of a voltage-input converter when it is supplied by an ideal constant-current source. Therefore, it cannot be directly measured and, consequently, indirect methods have to be used as also proposed in [53]. The problem in indirect methods may be the errors induced by the measurement inaccuracies of the loop-gains and impedances, which can cumulate during the calculation process. Consequently, the analysis and experimental results obtained in [53] remains ambiguous.

In [55], the expressions for the input-to-output transfer function, voltage-loop gain and output impedance as well as input impedance of a system consisting of a converter and an input filter are derived based on EET. The analysis is done at the true input of a converter and the expressions are in general form. Therefore, they can be used with all types of converters regardless of topology and control method. Naturally, the expressions presented in [55] are the same as the expressions derived with basic circuit theory according to Chapter 2. In [55], boost converters under VMC and PCMC are used to demonstrate the typical input impedances of the converters through which the source interactions reflect (i.e. open-loop, ideal, short-circuit and closed-loop input impedances). However, the converters are loaded with resistive loads, and therefore the true internal dynamics of the converters are hidden. E.g., the phase of the open-loop input impedance of the PCM-controlled converter shown in Fig. 8 in [55] should start from -180 degrees rather than from 0 degrees as can be concluded according to appendix in [55].

The source-affected voltage-loop gain in (2.11) can also be expressed in terms of input impedances (i.e., the ideal input impedance $Z_{\text{in}-\infty} = Y_{\text{in}-\infty}^{-1}$ and the open-loop input impedance $Z_{\text{in}-\text{o}} = Y_{\text{in}-\text{o}}^{-1}$) as shown in (3.13). The resulting minor-loop gain at the interface between the source impedance and the converter can be expressed as $L_{\text{M}-\text{S}} = Z_\text{s}/Z_{\text{in}-\text{c}}$, where the closed-loop input impedance is defined in (3.14).

$$L_\text{v}^\text{S} = \frac{1+Z_\text{s}/Z_{\text{in}-\infty}}{1+Z_\text{s}/Z_{\text{in}-\text{o}}} L_\text{v} \tag{3.13}$$

$$Z_{\text{in}-\text{c}} = Y_{\text{in}-\text{c}}^{-1} = \left(\frac{1}{Z_{\text{in}-\text{o}}} - \frac{G_{\text{io}-\text{o}} G_{\text{ci}-\text{o}}}{G_{\text{co}-\text{o}}} \frac{L_\text{v}}{1+L_\text{v}} \right)^{-1} = \left(\frac{1}{Z_{\text{in}-\text{o}}} \frac{1}{1+L_\text{v}} + \frac{1}{Z_{\text{in}-\infty}} \frac{L_\text{v}}{1+L_\text{v}} \right)^{-1} \tag{3.14}$$

According to (3.13) and (3.14), the relation between the minor-loop gain and the source-affected voltage-loop gain is not as simple as for the load-side minor-loop gain and the corresponding voltage-loop gain. Solving $Z_{\text{in}-\text{o}}$ or $Z_{\text{in}-\infty}$ from (3.14) and replacing it in (3.13) with the new expression makes the analysis more complex and the relation

between the minor-loop and the source-affected voltage-loop gain cannot be directly recognized. However, at the frequencies where the magnitude of the internal voltage-loop gain is much greater than unity (i.e., $|L_v| \gg 1$), the closed-loop input impedance resembles the ideal input impedance $Z_{in-\infty}$. Consequently, the minor-loop gain is $L_{M-S} \approx Z_s/Z_{in-\infty}$ and it appears in the numerator of the term multiplying the internal voltage-loop gain. Similarly, at frequencies where $|L_v| \ll 1$, the closed-loop input impedance resembles the open-loop input impedance Z_{in-o} and the minor-loop gain (i.e., $L_{M-S} \approx Z_s/Z_{in-o}$) appears in the denominator of the term multiplying the internal voltage-loop gain. In both cases, the voltage-loop gain may also change via the open-loop or the ideal input impedance, respectively. Therefore, direct relation between the source-side minor-loop gain and the corresponding voltage-loop gain is hard to recognize and, consequently, computational software has to be used to perform more accurate analyses based on (3.13).

According to Chapter 2, the source-affected closed-loop output impedance can be expressed as shown in (3.15). The last expression in (3.15) implies that the minor-loop gain appears in the denominator of the term multiplying the internal closed-loop output impedance. In addition, there may be interactions due to the short-circuit input impedance Z_{in-sc}. According to $Z_{o-o}^S/(1+L_v^S)$ in (3.15), the closed-loop output impedance may change due to superimposed effect of the source-affected open-loop output impedance and voltage-loop gain. Consequently, the source interactions on converter dynamics are always combinations of the effects of the different impedance ratios (i.e., Z_s/Z_{in-o}, Z_s/Z_{in-sc}, $Z_s/Z_{in-\infty}$) and the effects of them all have to be considered, if accurate prediction of the source interactions is needed.

$$Z_{o-c}^S = \frac{Z_{o-o}^S}{1+L_v^S} = \frac{1+Z_s/Z_{in-sc}}{(1+Z_s/Z_{in-o})(1+L_v^S)} Z_{o-o} = \frac{1+Z_s/Z_{in-sc}}{1+Z_s/Z_{in-c}} Z_{o-c} \tag{3.15}$$

As discussed in Section 2.2.2, the source-affected closed-loop output impedance is not mathematically defined by the last expression in (3.15) for a converter that has the closed-loop output impedance equal to zero such as the buck converter with ideal OCF-control. Hence, another expression has to be used, i.e., $Z_{o-c}^S = Z_{o-c} + G_{io-c}T_{oi-c}Z_s/(1+Z_sY_{in-c})$. The last expression in (3.15) can be also derived by means of EET as done in [55], where the applicability of the expression is not, however, generally discussed.

The practical converter modules are typically equipped with input capacitors or even with internal EMI filters. Therefore, the true input of the converter where the source-interaction analyses shall be made [26] may be inaccessible for measurement. In addition, the parameter values of the input capacitors or filters may be unknown to the customer or system designer and, therefore, the calculation of the source impedance seen by the converter may not be possible. According to Chapter 2, PCM and IVFF-controlled converters can be designed so that the open-loop input-to-output transfer

function becomes equal to zero. Hence, the different input impedances defining the source interactions as well as the closed-loop input impedance becomes equal to the ideal input impedance $Z_{\text{in}-\infty}$ and, consequently, the effect of source impedance on the voltage-loop gain and the closed-loop output impedance would be cancelled according to (3.13) and (3.15). This means that the converter is invariant to the source interactions and the only issue which needs to be considered is the stability of the system by means of the source-side minor-loop gain. According to system theory [33], this can be evaluated at the physical input of the converter. However, robustness of stability can not be accurately determined without information on the inner properties of the converter [P2].

For converters which are not designed to be invariant to source interactions, some design rules can be still derived that can be utilized at the physical interface to maintain the performance of the original converter unaffected. Fig. 3.10 shows a system consisting of a source subsystem, an arbitrary impedance block (e.g., input filter) and a POL converter. A possible input capacitor is considered as part of the impedance block and, therefore, the true input of the converter is at interface A_1. The interface before the impedance block is A_2, which represents the physical input of the converter, when it has an internal input capacitor or filter.

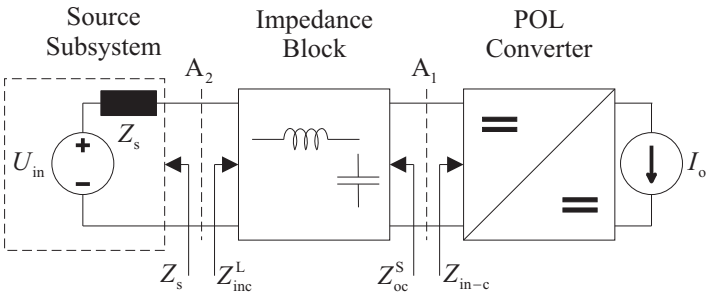


Fig. 3.10 *A system consisting of a source subsystem, an impedance block and a POL converter.*

The corresponding minor-loop gains at the interfaces A_1 and A_2 are $L_{\text{M-S1}}$ and $L_{\text{M-S2}}$, respectively, as shown in (3.16) and (3.17), where Y_{inc}, G_{ioc}, T_{oic} and Z_{oc} are the g-parameters of the impedance block and $Y^{\text{c}}_{\text{in}-\text{sc}}$ is its short-circuit input admittance. When $Z_{\text{s}}Y_{\text{inc}}$ is solved from (3.17) and substituted in (3.16) with the new expression, the minor-loop gain at the interface A_1 becomes as shown in (3.18).

$$L_{\text{M-S1}} = \frac{Z^{\text{S}}_{\text{oc}}}{Z_{\text{in}-\text{c}}} = \frac{Z_{\text{oc}}}{Z_{\text{in}-\text{c}}} \frac{1 + Z_{\text{s}}\left(Y_{\text{inc}} + \dfrac{G_{\text{ioc}}T_{\text{oic}}}{Z_{\text{oc}}}\right)}{1 + Z_{\text{s}}Y_{\text{inc}}} = \frac{Z_{\text{oc}}}{Z_{\text{in}-\text{c}}} \frac{1 + Z_{\text{s}}Y^{\text{c}}_{\text{in}-\text{sc}}}{1 + Z_{\text{s}}Y_{\text{inc}}} \tag{3.16}$$

$$L_{\mathrm{M-S2}} = \frac{Z_{\mathrm{s}}}{Z_{\mathrm{inc}}^{\mathrm{L}}} = \frac{Z_{\mathrm{s}}}{\left(Y_{\mathrm{inc}} + \dfrac{G_{\mathrm{ioc}} T_{\mathrm{oic}}}{Z_{\mathrm{in-c}} + Z_{\mathrm{oc}}} \right)^{-1}} = Z_{\mathrm{s}} \left(Y_{\mathrm{inc}} + \frac{G_{\mathrm{ioc}} T_{\mathrm{oic}}}{Z_{\mathrm{in-c}} + Z_{\mathrm{oc}}} \right) \tag{3.17}$$

$$L_{\mathrm{M-Sl}} = \frac{Z_{\mathrm{oc}}}{Z_{\mathrm{in-c}}} \frac{1 + L_{\mathrm{M-S2}} + \dfrac{Z_{\mathrm{s}} G_{\mathrm{ioc}} T_{\mathrm{oic}}}{Z_{\mathrm{in-c}} + Z_{\mathrm{oc}}} \dfrac{Z_{\mathrm{in-c}}}{Z_{\mathrm{oc}}}}{1 + L_{\mathrm{M-S2}} - \dfrac{Z_{\mathrm{s}} G_{\mathrm{ioc}} T_{\mathrm{oic}}}{Z_{\mathrm{in-c}} + Z_{\mathrm{oc}}}} \tag{3.18}$$

Even if $L_{\mathrm{M-S2}} \ll 1$ (i.e., no impedance overlap is present at interface A_2), the minor-loop gain at interface A_1 can still change due to the other terms shown in (3.18). and, hence, the performance of the converter may be deteriorated. On the other hand, if $L_{\mathrm{M-S2}} \gg 1$ (i.e., impedance overlap at interface A_2 exists) and the latter terms in the denominator and numerator of (3.18) are negligible compared to $L_{\mathrm{M-S2}}$, the minor-loop gain at interface A_1 becomes approximately equal to $Z_{\mathrm{oc}}/Z_{\mathrm{in-c}}$. This means that the impedance overlap is not present at interface A_1, if $Z_{\mathrm{oc}} < Z_{\mathrm{in-c}}$ despite the overlap at interface A_2. Any other special relation between the minor-loop gains is difficult to recognize, except the condition for a marginally stable system, i.e., when $L_{\mathrm{M-S2}} = -1$ also $L_{\mathrm{M-Sl}}$ becomes -1, which clearly confirms that the minor-loop gain can be used to determine the stability at an arbitrary interface within a system.

The voltage-loop gain and the closed-loop output impedance of the converter shown in Fig. 3.10 can be expressed as shown in (3.19) and (3.20), when the supply subsystem has non-zero source impedance. If the impedance block (e.g., an internal EMI filter) is designed appropriately to maintain the dynamics and performance of the converter adequate, when the source impedance is absent, then by having $Z_{\mathrm{s}} \ll Z_{\mathrm{in-sc}}^{\mathrm{c}}$ and $Z_{\mathrm{s}} \ll Z_{\mathrm{inc}}$ the voltage-loop gain and closed-loop output impedance stay intact in the presence of the source impedance. However, these design rules may be too restrictive to obtain in practice, although the needed impedances (i.e., $Z_{\mathrm{in-sc}}^{\mathrm{c}}$ and Z_{inc}) could be determined. Consequently, the design of a system composing of commercial converter modules remains difficult.

$$L_{\mathrm{v}}^{\mathrm{S}} = \frac{1 + Z_{\mathrm{oc}}^{\mathrm{S}} / Z_{\mathrm{in-\infty}}}{1 + Z_{\mathrm{oc}}^{\mathrm{S}} / Z_{\mathrm{in-o}}} L_{\mathrm{v}} = \frac{1 + \dfrac{Z_{\mathrm{oc}}}{Z_{\mathrm{in-\infty}}} \dfrac{1 + Z_{\mathrm{s}} / Z_{\mathrm{in-sc}}^{\mathrm{c}}}{1 + Z_{\mathrm{s}} / Z_{\mathrm{inc}}}}{1 + \dfrac{Z_{\mathrm{oc}}}{Z_{\mathrm{in-o}}} \dfrac{1 + Z_{\mathrm{s}} / Z_{\mathrm{in-sc}}^{\mathrm{c}}}{1 + Z_{\mathrm{s}} / Z_{\mathrm{inc}}}} L_{\mathrm{v}} \tag{3.19}$$

$$Z_{\mathrm{o-c}}^{\mathrm{S}} = \frac{1 + Z_{\mathrm{oc}}^{\mathrm{S}} / Z_{\mathrm{in-sc}}}{1 + Z_{\mathrm{oc}}^{\mathrm{S}} / Z_{\mathrm{in-c}}} Z_{\mathrm{o-c}} = \frac{1 + \dfrac{Z_{\mathrm{oc}}}{Z_{\mathrm{in-sc}}} \dfrac{1 + Z_{\mathrm{s}} / Z_{\mathrm{in-sc}}^{\mathrm{c}}}{1 + Z_{\mathrm{s}} / Z_{\mathrm{inc}}}}{1 + \dfrac{Z_{\mathrm{oc}}}{Z_{\mathrm{in-c}}} \dfrac{1 + Z_{\mathrm{s}} / Z_{\mathrm{in-sc}}^{\mathrm{c}}}{1 + Z_{\mathrm{s}} / Z_{\mathrm{inc}}}} Z_{\mathrm{o-c}} \tag{3.20}$$

The above theoretical analysis clearly indicates that the minor-loop gain is a weak source of information on the level of source interactions, despite the interface where it is derived. Therefore, the claimed conservatism of Middlebrook's criterion is clearly unfounded. This is also demonstrated in [P2] with the experimental system shown in Fig. 3.11 with the interface and impedance definitions. In the experimental system, a bus converter supplies two identical POL converters (the other converter is not shown in Fig. 3.11) via the main bus. The POL converters are VM-controlled buck converters operating approximately at 425 kHz. The converter of interest was loaded with a resistive load of 1.25 Ω and its input capacitor was a 35-µF ceramic capacitor with ESR of 3 mΩ. The inductance of the connection cable was approximately 60 nH. Photographs of the laboratory measurement setup and the experimental converters are shown in Appendix D in Figs. A.1 and A.2, respectively. List of equipments used in measurements are shown in Appendix D in Table A.1. The schematics of the POL converters are shown in Appendix D in Fig. A.3.

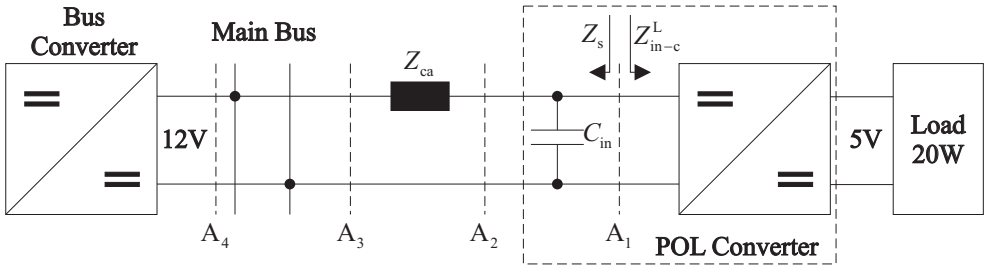
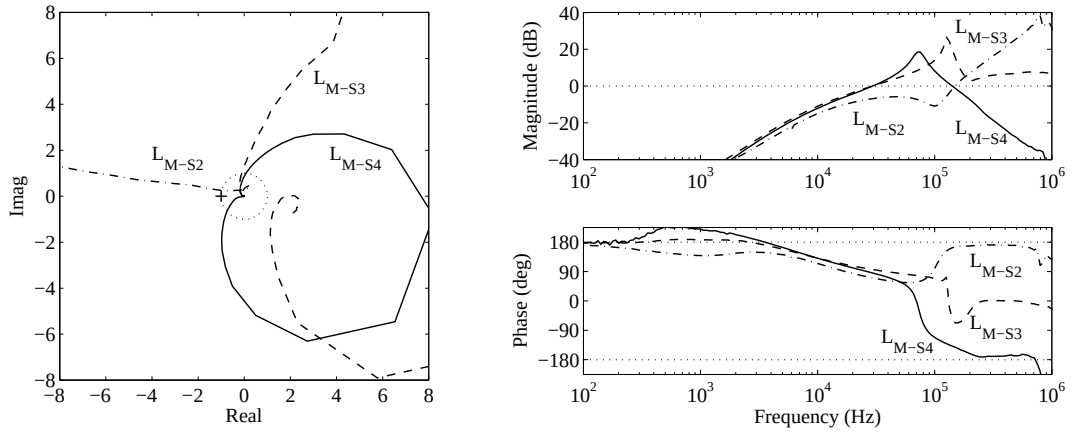


Fig. 3.11 *The experimental system used in [P2] with interface and impedance definitions.*

Three different minor-loop gains were measured at interfaces A_2, A_3 and A_4 (i.e., L_{M-S2}, L_{M-S3} and L_{M-S4}, respectively) as shown in Fig. 3.12a as Nyquist plot and in Fig. 3.12b as Bode plot. The minor-loop gain at interface A_1 could not be directly measured because the interface was physically inaccessible due to the input capacitor.



a) *b)*

Fig. 3.12 *The measured minor-loop gains of the experimental system as Nyquist (a) and Bode (b) plots.*

The minor-loop gains measured at different interfaces give different information concerning the robustness of stability and performance degradation of the POL converter as shown in Fig. 3.12. The minor-loop gain measured at the output of the bus converter (i.e., at interface A_4, L_{M-S4} in Fig. 3.12) indicates impedance overlap at the frequencies from 30 to 140 kHz with phase margins of 95 and 41 degrees at the gain-crossover frequencies. Hence, the bus converter and the system are stable although the performance of the bus converter is affected. According to L_{M-S3} measured at interface A_3, the impedance overlap exists at frequencies higher than 30 kHz. The corresponding phase margin is approximately 84 degrees also indicating stability of the system. Similarly, the minor-loop gain measured at interface A_2 indicates impedance overlap at the frequencies above the gain-crossover frequency of 140 kHz. The corresponding phase margin is approximately 15 degrees indicating that the system is stable, but with very low phase margin.

Fig. 3.13a shows the predicted input impedances of the converter and the calculated source impedance from the measurements indicating that the impedances are well separated and, therefore, the dynamics of the converter should stay intact. The measured voltage-loop gains of the converter shown in Fig. 3.13b in stand-alone operation (1, solid line) and as part of the experimental system (2, dashed line) confirm the unaffected dynamics as the impedances in Fig. 3.13a also imply.

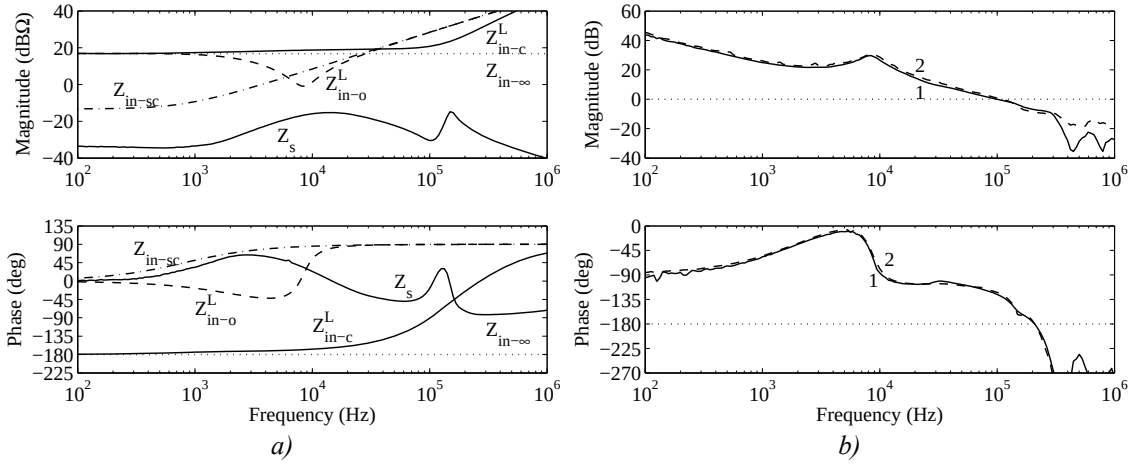


Fig. 3.13 *The predicted and calculated impedances at the interface A_1 (a) and the measured voltage-loop gains of the POL converter in stand-alone operation and as part of the experimental system (b).*

The experimental results obtained with the system used in [P2] clearly indicate that the minor-loop gain defined at an arbitrary interface within a system may not at all contain the necessary information to predict the performance degradation of POL converters as the theoretical analysis predicted. The relation between a minor-loop gain and the parameters defining the level of performance degradation is weak if the minor-loop gain is not defined at the true input of the converter, i.e., internal input filters or capacitors are considered as part of the supply system and not as part of the converter. It was also demonstrated in [P2] that if the minor-loop gain at the true input of the experimental

converter satisfies Middlebrook's criterion defined by the gain margin of 6 dB, the transient response of the converter can still be substantially deteriorated.

In [P2], the relation between the source-side minor-loop gain (i.e., at interface A_1) and the voltage-loop and closed-loop output impedance of the experimental converter were analyzed theoretically with artificial source impedances computed from the closed-loop input impedance of the converter with (3.21). The magnitude of the resulting source impedance is always below (or above) the magnitude of the closed-loop input impedance by the amount defined by GM in dB. Similarly, the phase difference between the source and closed-loop input impedances is always less (or more) than 180 degrees by the amount defined by PM. Therefore, the resulting minor-loop gain represents a single point in complex plane for the whole frequency range of interest. The source-affected voltage-loop gain and closed-loop output impedance were then calculated with (3.13) and the second expression in (3.15), respectively.

$$Z_s = |Z_s| \angle \phi_{Zs} = 10^{\frac{-GM_{dB}}{20}} |Z_{in-c}| \angle (\phi_{Zin-c} + 180° - PM) \tag{3.21}$$

Fig. 3.14a shows the predicted source-affected voltage-loop gains of the same experimental POL converter used in the system shown in Fig. 3.11 for different source impedances calculated with (3.21), when GM = 0 dB and PM = -60 degrees (1, dashed line), GM = 6 dB and PM = 0 degrees (2, dash-dotted line), GM = 12 dB and PM = 0 degrees (3, dotted line). The internal voltage-loop gain L_v is also shown in Fig. 3.14a with a solid line. The predicted source-affected closed-loop output impedances of the experimental converter are shown in Fig. 3.14b for the same gain and phase margin pairs as for the voltage-loop gain. The internal closed-loop output impedance Z_{o-c} is shown in Fig. 3.14b with a solid line.

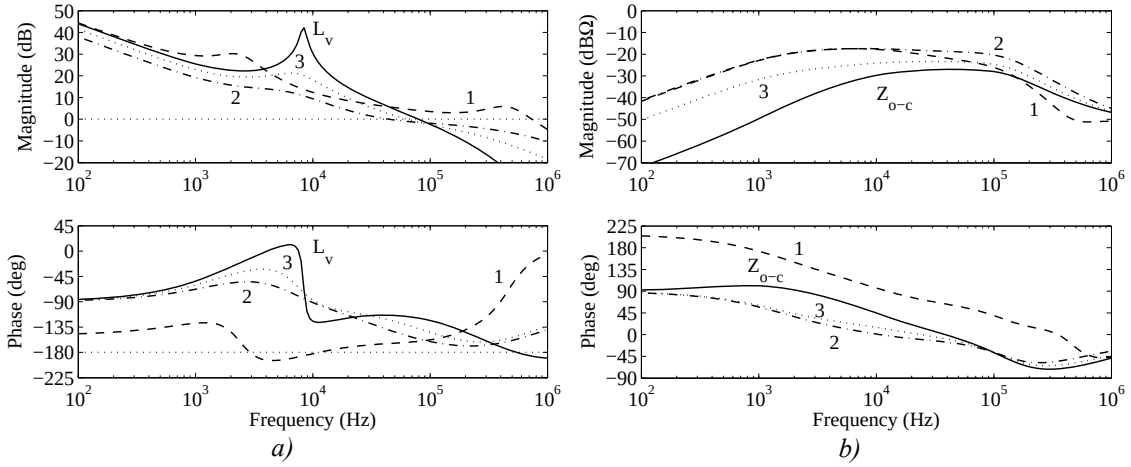


Fig. 3.14 *Predicted effect of the artificial source impedances on the voltage-loop gain (a) and closed-loop output impedance (b) for source impedances calculated with GM = 0 dB, PM = -60 degrees (1) and PM = 0 degrees, when GM = 6 dB (2) and GM = 12 dB (3).*

According to Fig. 3.14a, the voltage-loop gain is subject to both increase and decrease in magnitude depending on the value of gain and phase margins. The typical tendency is that the magnitude of the voltage-loop gain is increased above the gain-crossover frequency. Therefore, the converter can easily become unstable due to the unintentionally high gain-crossover frequency caused by the component variations or changes in operation point. At the vicinity of the converter resonant frequency (i.e., approximately 8 kHz), the magnitude of the voltage-loop gain is most susceptible to decrease. According to Fig. 3.14b, the magnitude of the closed-loop output impedance is most susceptible to increase at the whole frequency range of interest, making the converter more prone to load interactions. Similar analyses are also presented in [P2] for slightly different gain and phase margin pairs.

The safe source profile of the experimental POL converter was also discussed in [P2]. The intention of the profile is to maintain the dynamics of the converter close to the original (i.e. in stand-alone operation without the source interactions) by defining maximum allowed value for the magnitude of the source impedance based on the closed-loop input impedance. The maximum value was actually defined by the magnitude of the voltage-loop gain based on extensive analysis with different theoretical source impedances calculated with (3.21). For the experimental converter, the margin between the source and closed-loop input impedance was defined to be 6 dB at all frequencies, except for those where the internal voltage-loop gain decreases from 24 dB to -24 dB including the resonant peak, and the margin was defined to be 12 dB. As a result, the minor-loop gain stays inside a circle having radius equal to 0.5 or 0.25 (i.e., $1/\left(10^{6/20}\right)$ or $1/\left(10^{12/20}\right)$, respectively) at different frequencies depending on the magnitude of the voltage-loop gain as defined above. The derived source profile is only applicable to the experimental VM-controlled buck converter and, therefore, the profile has to be derived separately for other control methods and converter topologies.

Fig. 3.15 shows the maximum and minimum envelopes (solid lines) for the source-affected voltage-loop gains (i.e., Fig. 3.15a) and closed-loop output impedances (i.e., Fig. 3.15b) calculated for different source impedances with a magnitude between the level defined by the safe source profile and the level defined by a 60-dB margin between the source and closed-loop input impedances. The magnitude of the source impedance was increased from the lower bound to the safe source profile in 1 dB increments. The phase of the source impedance was varied between -90 and 90 degrees in 5 degree increments. The nominal voltage-loop gain and closed-loop output impedance are shown in Fig. 3.15a and 3.15b as dashed lines, respectively.

According to Fig. 3.15a, the gain-crossover frequency of the voltage-loop gain can vary between 55 and 94 kHz (the nominal crossover is 80 kHz). The corresponding minimum phase margins are 47 and 37 degrees (the nominal phase margin is 60 degrees), respectively. It should be noted that the gain-crossover frequencies and the corresponding phase margins may not occur for the same source impedance, and

therefore the actual minimum phase margins may be increased from the above values for practical source impedances. According to Fig. 3.15b, the maximum value of the closed-loop output impedance is increased by 3.5 dBΩ at the vicinity of the nominal gain-crossover frequency and the peak value is increased approximately from -27 dBΩ (at 50 kHz) to -21.6 dBΩ (at 1.3 kHz), which corresponds to 5.4 dBΩ increase, i.e., the maximum value of the output impedance is nearly doubled.

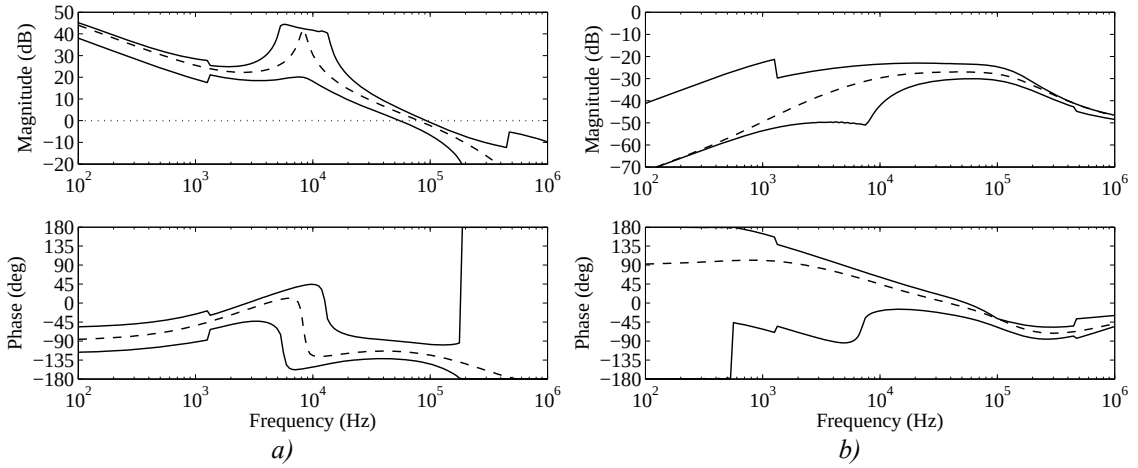


Fig. 3.15 *The predicted maximum and minimum envelopes of the source-affected voltage-loop gains (a) and closed-loop output impedances (b) for arbitrary source impedances satisfying the safe source profile of the experimental converter.*

As a summary, the source-side minor-loop gain determined at an arbitrary interface can be used to determine the stability of a system. However, it does not provide much information regarding to the robustness of stability or performance degradation of the converters, especially, if the minor-loop gain is not defined at the true input of the converter as demonstrated in [P2]. The exact effect of arbitrary source impedance on the dynamics of a converter can always be calculated by the source interaction formalism presented in Chapter 2 or the other methods presented in [30] and [49]–[55]. However, the exact calculations always require information on the inner properties of the converter of interest, i.e., the different input admittances (or impedances) $Y_{\text{in}-\text{o}}$, $Y_{\text{in}-\text{sc}}$, $Y_{\text{in}-\infty}$ and the internal voltage-loop gain. Therefore, accurate performance prediction of commercial converter modules is practically impossible, as such information is not usually available or it can not be measured without altering the feedback circuitry. The source-interaction analyses become deterministic and quite easy when the converters are designed to be invariant to source interactions. In this case, only the stability of the minor-loop gain needs to be determined. The safe source profile defined in [P2] for the experimental converter is not general and needs to be defined separately for the other type of control methods or converter topologies.

3.4 Effect of Output-Voltage Remote Sensing on Performance and Stability

The supply voltage requirements of many modern electric loads are stringent in terms of static accuracy and transient response [5], [6]. Therefore, external capacitors are usually added to the output of a converter to improve the transient response [84], [95]. To further improve the static accuracy and transient response of the load voltage, output-voltage remote sensing is typically applied. Although the application of the remote sensing is evident in many publications, the analyses are usually only focused on output dynamics, i.e., output impedance, voltage-loop gain and transient response [85], [86]. Hence, the effects of the remote sensing on input dynamics are not considered at all, although adverse effects on input dynamics may make the converter more prone to source interactions and instability. The theoretical formalism to analyze the effects of the output-voltage remote sensing on all the parameters defining the dynamics of a converter is presented in a consistent way in [P3].

According to [P3] and Section 2.2.3, the open-loop output impedance of the cascaded system consisting of an open-loop converter and the connection impedance block can be expressed as shown in (3.22). The superscript "RS" is used to distinguish the impedance from source or load-affected impedances, although the output-voltage feedback is not connected from either terminal of the system, i.e., the output of the converter or the point of load.

$$Z_{\mathrm{o-o}}^{\mathrm{RS}} = \frac{1 + Z_{\mathrm{o-o}} Y_{\mathrm{in-sc}}^{\mathrm{c}}}{1 + Z_{\mathrm{o-o}} Y_{\mathrm{inc}}} Z_{\mathrm{oc}} \tag{3.22}$$

When the feedback is taken directly from the load voltage instead of the output voltage of the converter, the closed-loop output impedance of the cascaded system can be expressed as shown in (3.23), where the new voltage-loop gain is shown in (3.24) as a function of the internal voltage-loop gain of the converter, when the feedback is taken from the output of the converter. Therefore, the closed-loop output impedance $Z_{\mathrm{o-c}}^{\mathrm{RS}}$ may contain the superimposed effects via the open-loop output impedance $Z_{\mathrm{o-o}}^{\mathrm{RS}}$ and the voltage-loop gain $L_{\mathrm{v}}^{\mathrm{RS}}$. The magnitude of the closed-loop output impedance may increase or decrease due to the impedance interactions via $Z_{\mathrm{o-o}}$ and $Z_{\mathrm{inc}} = \left(Y_{\mathrm{inc}}\right)^{-1}$ as well as $Z_{\mathrm{o-o}}$ and $Z_{\mathrm{in-sc}}^{\mathrm{c}} = \left(Y_{\mathrm{in-sc}}^{\mathrm{c}}\right)^{-1}$. The input-to-output transfer function of the connection impedance block G_{ioc} also affects the closed-loop output impedance via the voltage-loop gain.

$$Z_{\mathrm{o-c}}^{\mathrm{RS}} = \frac{Z_{\mathrm{o-o}}^{\mathrm{RS}}}{1 + L_{\mathrm{v}}^{\mathrm{RS}}} \tag{3.23}$$

$$L_{\mathrm{v}}^{\mathrm{RS}} = \frac{G_{\mathrm{ioc}}}{1 + Z_{\mathrm{o-o}} Y_{\mathrm{inc}}} L_{\mathrm{v}} \tag{3.24}$$

According to [P3] and Section 2.2.3, the open-loop input admittance of the cascaded system can be expressed as shown in (3.25) indicating that the input impedance of the connection impedance block Z_{inc} is reflected to the input side of the converter via the input-to-output and reverse current transfer functions and, therefore, possibly changing the input admittance of the converter. As discussed in Section 3.2.3, the source interactions on converter dynamics also reflect via the ideal and short-circuit input admittances. These admittances are shown in (3.26) for the cascaded system.

$$Y_{\text{in-o}}^{\text{RS}} = Y_{\text{in-o}} + \frac{G_{\text{io-o}} T_{\text{oi-o}}}{Z_{\text{o-o}} + Z_{\text{inc}}} \tag{3.25}$$

$$\begin{aligned} Y_{\text{in-}\infty}^{\text{RS}} &= Y_{\text{in-o}}^{\text{RS}} - \frac{G_{\text{io-o}}^{\text{RS}} G_{\text{ci-o}}^{\text{RS}}}{G_{\text{co-o}}^{\text{RS}}} = Y_{\text{in-}\infty} \\ Y_{\text{in-sc}}^{\text{RS}} &= Y_{\text{in-o}}^{\text{RS}} + \frac{G_{\text{io-o}}^{\text{RS}} T_{\text{oi-o}}^{\text{RS}}}{Z_{\text{o-o}}^{\text{RS}}} = Y_{\text{in-o}} + \frac{G_{\text{io-o}} T_{\text{oi-o}}}{Z_{\text{o-o}} + Z_{\text{in-sc}}^{\text{c}}} \end{aligned} \tag{3.26}$$

According to (3.26), the ideal input admittance of the cascaded system is equal to the ideal input admittance of the converter and is, therefore, left intact. The short-circuit input admittance of the cascaded system is equal to the load-affected input admittance of the converter when the load impedance is equal to the short-circuit input admittance of the impedance block. The closed-loop input admittance of the cascaded system is shown in (3.27) as a function of the ideal and open-loop input admittances and voltage-loop gain of the cascaded system, indicating that the closed-loop input admittance may contain the superimposed effects of the open-loop input admittance and voltage-loop gain. Consequently, the input dynamics of the converter may change substantially from the original dynamics when the connection impedance block is connected at the output of the converter and the output-voltage feedback is taken from the point of load.

$$Y_{\text{in-c}}^{\text{RS}} = \frac{Y_{\text{in-o}}^{\text{RS}}}{1 + L_{\text{v}}^{\text{RS}}} + \frac{Y_{\text{in-}\infty}^{\text{RS}} L_{\text{v}}^{\text{RS}}}{1 + L_{\text{v}}^{\text{RS}}} \tag{3.27}$$

In [P3], the theoretical findings were demonstrated with two VM-controlled buck converters operating approximately at 100-kHz and 430-kHz switching frequencies. The low-frequency converter was the same conventional buck converter that was also used in analyses in [P1] and in Section 3.2.2. The high-frequency converter was the synchronous buck converter also used for source interactions analyses in [P2] and Section 3.2.3. The effects of a pure connection cable (Fig. 4a in [P3]) and a T-type LCL circuit (Fig. 4b in [P3]) were analyzed on the output dynamics of the conventional and synchronous converters, respectively. It was discussed in [P3] that a pure connection cable would only change the output impedance and the short-circuit input admittance of the converter, whereas the T-type LCL-circuit would change all the parameters defining the dynamics of the resulting system making it more prone to source interactions.

Therefore, the high-frequency synchronous buck converter with the T-type LCL circuit is used here to demonstrate the possible effects of the remote sensing on converter dynamics. However, the effects on the input dynamics could not be measured due to the internal input capacitor of the converter and, therefore, only predictions are shown here. For the same reason, the affected input dynamics of the converter are not discussed in detail in [P3]. An example Matlab m-file is shown in Appendix B, which was used to evaluate the effect of the remote sensing on converter dynamics, based on the measured load impedance and predicted g-parameters of the converter and the impedance block.

The measured open and closed-loop output impedances of the high-frequency converter and the cascaded system with and without the output-voltage remote sensing are shown in Figs. 3.16a and 3.16b, respectively. The open-loop output impedance of the stand-alone converter (1, solid line) and cascaded system (2, dashed line) are shown in Fig. 3.16a. In Fig. 3.16b, the closed-loop output impedance of the stand-alone converter is shown as the solid line (1). The closed-loop output impedance of the cascaded system, when the output-voltage feedback is taken from the output of the converter, is shown as the dash-dotted line (2) in Fig. 3.16b and, similarly, when the output-voltage feedback is taken from the load terminals, the closed-loop output impedance is shown as the dashed line (3). The load impedance of the constant-current load with a 4-µF input capacitor used in the analysis is also shown in Figs. 3.16a (3, dotted line) and 3.16b (4, dotted line).

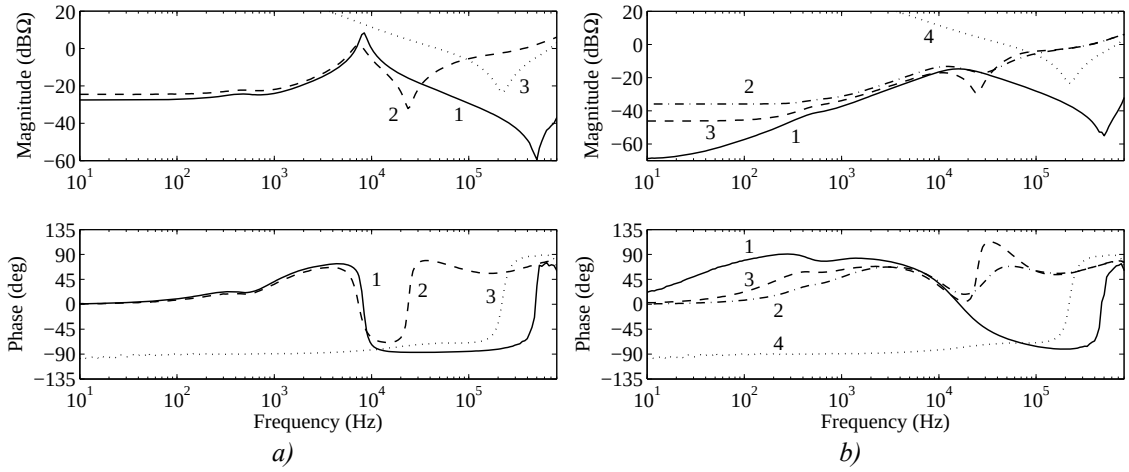


Fig. 3.16 *The different measured output impedances of the synchronous buck converter and the cascaded system at open (a) and closed (b) loop with the load impedances.*

According to Fig. 3.16a, the T-type LCL circuit increases the open-loop output impedance substantially at high frequencies making the impedance inductive (i.e., the phase is near 90 degrees and the magnitude increases approximately with 20 dB/decade slope). Similarly, the closed-loop output impedances shown in Fig. 3.16b exhibit inductive nature at high frequencies (i.e., above the voltage-loop gain-crossover frequency approximately 20 kHz). Therefore, the use of remote-sensing with the T-type

LCL circuit has made the converter sensitive to capacitive loading as can be concluded from the discussion presented in Section 3.1.

According to Fig. 3.16b, the magnitude of the closed-loop output impedance at low frequencies is substantially increased (i.e., approximately from -68 dBΩ to -36 dBΩ or correspondingly from 0.4 mΩ to 15.8 mΩ) due to the additional impedances between the converter and the load, when the remote-sensing is not used (2, dash-dotted line). When the feedback is taken from the remote-sensing interface, the magnitude of the output impedance (3, dashed line) is decreased at low frequencies (i.e., -46 dBΩ or 5 mΩ) compared to the case where remote-sensing is not used. However, the low-frequency magnitude is still higher than compared to the original closed-loop output impedance of the converter. The reason for this is that the control circuitry of the experimental converter did not have differential output-voltage measurement circuit. The output or load voltage was only measured from the high-side of the output or load terminals with respect to the ground of the converter and, therefore, the low-side trace of the connection impedance block is not included inside the feedback loop and some residual resistance is left, which is visible in the output impedance measurement in Fig. 3.16b. The problem was recognized at an early stage before the experimental analysis and, consequently, the low-side trace of the connection impedance block was made as short as possible to minimize the induced errors.

The measured voltage-loop gains of the different feedback and system configurations are shown in Fig. 3.17. The voltage-loop gain of the stand-alone converter (i.e. without remote-sensing and the T-type LCL circuit) with the constant-current load is shown as a solid line (1). The voltage-loop gain of the converter within the cascaded system without (2) and with (3) remote sensing are shown as dashed and dash-dotted lines, respectively. Actually, the voltage-loop gain of the converter without remote sensing (2, dashed line) represents the load-affected voltage-loop of the converter, when the load consists of the constant-current sink and the connection impedance block.

According to Fig. 3.17, the voltage-loop gains of the stand-alone converter (1, solid line) and the converter within the cascaded system without remote sensing (2, dashed line) are quite similar except at the vicinity of the resonant frequency of the converter (i.e., the resonant frequency is shifted to lower frequency due to the T-type LCL circuit). The magnitude of the voltage-loop gain of the converter within the cascaded system with remote sensing (3, dash-dotted line) is quite similar to the other voltage-loop gains at frequencies below the gain-crossover frequency. However, above the gain-crossover frequency the magnitude of the voltage-loop gain peaks and the phase decreases rapidly, indicating that the gain margin of the voltage-loop gain is substantially decreased.

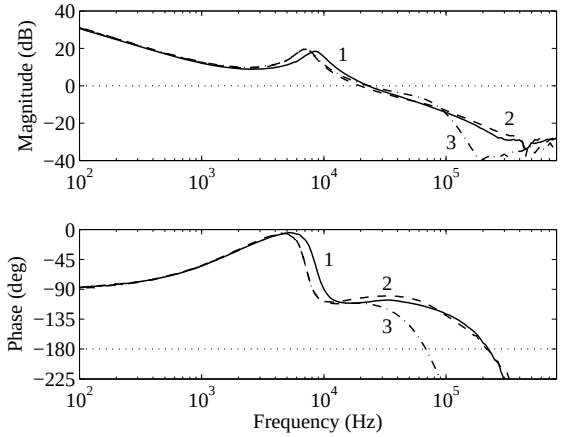


Fig. 3.17 *Measured voltage-loop gains of the stand-alone converter (1) and the converter within the cascaded system without (2) and with (3) the output-voltage remote sensing, when the converter is loaded with a constant-current-sink load.*

The gain-crossover frequencies as well as the phase and gain margins of the different voltage-loop gains shown in Fig. 3.17 are summarized in Table 3.1. According to it, the gain-crossover frequency of the converter within the cascaded system is slightly decreased from the nominal value without remote sensing (2) and stays intact, when remote-sensing is used (3). However, the use of remote sensing clearly somewhat decreases the phase margin and substantially decreases the gain margin, making the converter more prone to instability due to the component and operation point variations. Actually, the capacitor of the T-type LCL circuit had to be lossy (i.e. the ESR of the capacitor was quite high) to maintain the stability of the experimental converter. Of course, the controller of the converter could be redesigned for more robust operation at the presence of the LCL circuit and load.

Table 3.1 *The gain-crossover frequencies and the phase and gain margins of the voltage-loop gains shown in Fig. 3.17.*

Voltage-loop gain shown in Fig. 3.17	Gain-crossover frequency (kHz)	Phase margin (degrees)	Gain margin (dB)
1	23.7	71	25
2	19.8	76	22
3	23.7	67	7

The effect of remote sensing on the time domain transient response of the experimental system was also analyzed in [P3]. It was shown that when the LCL circuit was connected between the converter and load, the load-transient response of the load-voltage was deteriorated (i.e., the initial voltage dip was increased and the static voltage level was decreased). When the remote sensing was applied, the static accuracy of the load voltage was improved as the closed-loop output impedances in Fig. 3.16b imply.

However, the transient dynamics remained nearly intact. Hence, the application of the remote sensing itself does not necessarily improve the transient dynamics. Of course, the connection impedance block could be redesigned otherwise to improve the transient dynamics. However, it may not be possible to design the connection impedance block in every application and, therefore, the use of remote sensing may only improve the static accuracy of the load voltage.

Fig. 3.18a shows the predicted closed-loop input impedances of the converter within the cascaded system analyzed in [P3] without remote sensing (2, dashed line) and with it (3, dash-dotted line). The internal closed-loop input impedance of the stand-alone converter (1, solid line) and the ideal input impedance of the converter and the cascaded system ($Z_{\text{in}-\infty}$, dotted line) are also shown in Fig. 3.18a. The use of remote sensing substantially decreases the input impedance at frequency range of 30–200 kHz, compared to the input impedance of the stand-alone converter or the converter within the cascaded system, when the output-voltage feedback is taken directly from the output of the converter. In addition, the input impedance is slightly decreased at frequencies from 1 to 10 kHz for the converter within the cascaded system with and without the output-voltage remote sensing. The implication of the Fig. 3.18a is that the use of remote sensing may make the converter more prone to source interactions as the above theoretical discussion implies. Hence, the effects of the remote sensing need to be carefully analyzed on the input dynamics as well as the output dynamics.

The predicted short-circuit input impedances of the stand-alone converter ($Z_{\text{in}-\text{sc}}$, solid line) and of the converter within the cascaded system ($Z^{\text{RS}}_{\text{in}-\text{sc}}$, solid line) are shown in Fig. 3.18b indicating that the connection impedance block slightly affects the short-circuit input impedance. Especially at low frequencies, the magnitude of $Z^{\text{RS}}_{\text{in}-\text{sc}}$ is higher than the magnitude of $Z_{\text{in}-\text{sc}}$, indicating that the possible source interactions to the output impedance of the cascaded system are reduced slightly.

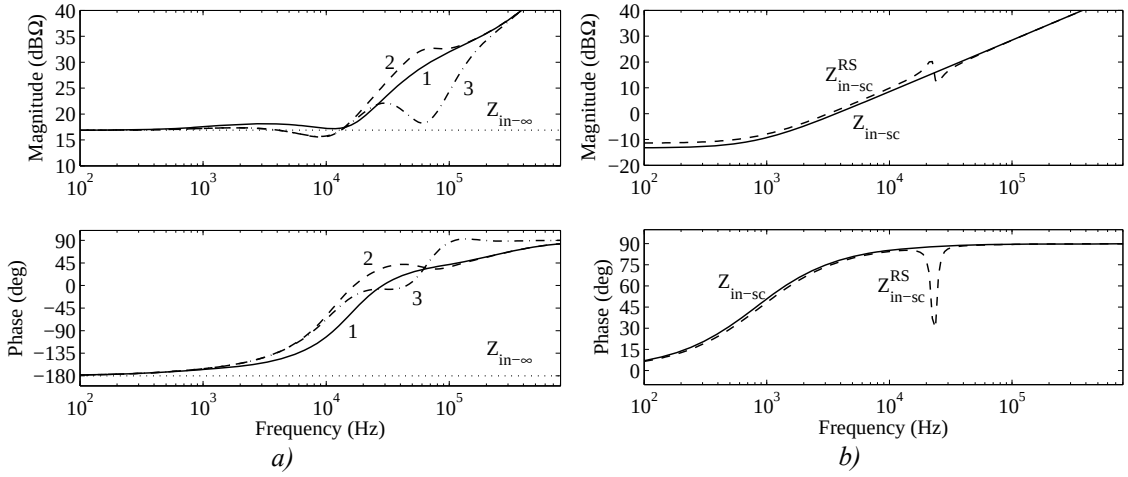


Fig. 3.18 *Predicted closed-loop (a) and short-circuit (b) input impedances for the stand-alone converter and the converter within the cascaded system without and with the output-voltage remote sensing.*

4 Application of Invariance to Reduce Interactions

As discussed in Chapter 3, the source and load interactions can affect and deteriorate the transient performance and stability of a converter. Therefore, special attention has to be paid to the design of EMI filters, converters and systems composing of them. It is not always possible or even practical to design the systems so that the impedance interactions are not present. Consequently, possible performance degradation and stability become important issues and need to be analyzed by proper methods described in Chapters 2 and 3. Accurately predicting the converter and system impedances constituting the source and load interactions may not always be possible, especially in the case of commercial converter modules due to a lack of necessary information. Therefore, the methods with which the interactions can be reduced or totally removed are of great importance. As discussed in Chapter 2, the feedforward control methods can be used to improve the converter dynamics. Even the ideal transient performance can be achieved theoretically. As a consequence of these, the load and source interactions are also reduced or totally removed. The application of these methods has to be done in the design phase of the converter and, therefore, can not be applied to commercial converter modules afterwards.

In this chapter, the practical application of such control methods that can achieve nearly ideal transient performance and also reduce the impedance interactions within systems are discussed, based on the contribution of the publications [P4]-[P7]. The control methods to be discussed are input-voltage feedforward control and PCM-control with output-current feedforward, which were applied to a basic buck converter in [P6] and in [P4], [P5], respectively. The PCM-controlled fourth-order step-down converter known as superbuck introduced in [P7] is used to demonstrate the effect of different topology on the dynamical profile and the characteristic parameters defining the level of possible interactions.

4.1 Supply Invariance of PCM and IVFF-controls in Practice

It was observed in the 70's [58], that the use of PCM-control in a buck-derived converter greatly improves the noise attenuation of the converter. Later on, the reason for this peculiar behavior is shown to be the decreased magnitude of the input-to-output transfer function due the proper value of slope of the compensation-ramp in duty-cycle generation [61], [63]. The research on input-voltage feedforward for switched-mode converters also started in the late 70's. It was noticed that the source interactions could be substantially reduced [64] and the input-to-output transfer function could be made zero [66] for certain converters under IVFF-control. Similar behavior is also observed with the buck-derived converters under boundary-conduction-mode [96] and hysteretic-

current-mode control [65]. The basis for ideal transient response of a converter using input-voltage and output-current feedforward is presented in [65] for current-mode controlled converters. The supply or input invariance is analyzed in [57] by means of simulations for the same buck converter under PCM and IVFF-controls. The practical evidence of the reduced interactions are provided for a buck converter under PCM in [97] and under IVFF-control in [73] without profound experimental frequency domain analysis. The general theoretical treatment and experimental frequency domain analyses of an IVFF-controlled buck converter are provided in [P6].

4.1.1 Input-to-Output Attenuation

The input-to-output transfer functions of a buck converter under PCM and IVFF-controls can be expressed as shown in (4.1) using the same notation as in [P5] and [P6]. In (4.1), $F_{\mathrm{m}}^{\mathrm{PCMC}}$ and $F_{\mathrm{m}}^{\mathrm{IVFF}}$ are the duty-ratio gains for PCM and IVFF-controls, respectively. Similarly, $q_{\mathrm{i}}^{\mathrm{PCMC}}$ and $q_{\mathrm{i}}^{\mathrm{IVFF}}$ are the input-voltage feedforward gains, $U_{\mathrm{E}} = U_{\mathrm{in}} + U_{\mathrm{D}} + I_{\mathrm{o}}\left(r_{\mathrm{D}} - r_{\mathrm{DS}}\right)$ and $r_{\mathrm{E}} = r_{\mathrm{L}} + Dr_{\mathrm{DS}} + D'r_{\mathrm{D}}$, where D is the steady-state duty ratio. The meaning of the other power-stage parameters in (4.1) can be deduced from Fig. 4 in [P5] and Fig. 5 in [P6].

$$
\begin{aligned}
G_{\mathrm{io-o}}^{\mathrm{PCMC}} &= \frac{\frac{1}{LC}\left(D - F_{\mathrm{m}}^{\mathrm{PCMC}} q_{\mathrm{i}}^{\mathrm{PCMC}} U_{\mathrm{E}}\right)\left(1 + sr_{\mathrm{C}}C\right)}{s^2 + s\dfrac{F_{\mathrm{m}}^{\mathrm{PCMC}} U_{\mathrm{E}} + r_{\mathrm{E}} + r_{\mathrm{C}}}{L} + \dfrac{1}{LC}} \\
G_{\mathrm{io-o}}^{\mathrm{IVFF}} &= \frac{\frac{1}{LC}\left(D - F_{\mathrm{m}}^{\mathrm{IVFF}} q_{\mathrm{i}}^{\mathrm{IVFF}} U_{\mathrm{E}}\right)\left(1 + sr_{\mathrm{C}}C\right)}{s^2 + s\dfrac{r_{\mathrm{E}} + r_{\mathrm{C}}}{L} + \dfrac{1}{LC}}
\end{aligned}
\tag{4.1}
$$

According to Section 2.3.3, the general condition for the zero open-loop input-to-output transfer function was $F_{\mathrm{m}} q_{\mathrm{i}} = G_{\mathrm{io-o}} / G_{\mathrm{co-o}}$, which reduces, according to (4.1), to $F_{\mathrm{m}} q_{\mathrm{i}} = D/U_{\mathrm{E}} \approx D/U_{\mathrm{in}}$ for both the PCM and the IVFF-controlled buck converters. The same gain (i.e., D/U_{in}) for the buck converter is found in [66], where the ideal gains are also derived for the other basic topologies (i.e., boost and buck-boost). In [67], the ideal feedforward gains that result in zero input-to-output transfer function at DC are derived for the basic topologies and also for topologies that have quadratic conversion ratios. However, the stability issue of non-minimum-phase converters to obtain the ideal gains is not discussed in either publication.

The duty-ratio and IVFF gains of the buck converter under PCM-control are shown in (4.2), where M_{c} is the slope of the artificial compensation ramp and T_{s} is the switching cycle [P5]. By having M_{c} equal to $DU_{\mathrm{E}}/(2L) \approx U_{\mathrm{o}}/(2L)$, the above condition for zero input-to-output transfer function of the PCM-controlled buck converter can be obtained [63]. A nearly similar requirement can also be derived for the PCM-controlled superbuck introduced in [P7]. However, the zero input-to-output transfer function can

be obtained only at low frequencies due to the resonant characteristics of the transfer function as discussed in [P7]. The PCM-control is implemented by controlling the peak value of the sum of the individual inductor currents flowing to output capacitor node. Therefore, the requirement for the slope of the compensation ramp becomes $M_c \approx U_o/(2L_P)$, where L_P is the inductance value of a parallel combination of the individual inductors. The expressions for the duty-ratio and IVFF gains of the PCM-controlled superbuck converter can be found in [P7].

$$\begin{aligned} F_m^{PCMC} &= \left(T_s \left(M_c + \frac{(D' - D)U_E}{2L} \right) \right)^{-1} \\ q_i^{PCMC} &= \frac{DD'T_s}{2L} \end{aligned} \tag{4.2}$$

The practical implementation of the IVFF-control method has decisive effect on the obtainable level of attenuation of the input-to-output transfer function. Different implementation approaches are discussed in [68]-[72]. Typically, the IVFF scheme for a buck converter is implemented by making the slope of the PWM ramp directly proportional to input voltage by a positive constant factor k as shown in Fig. 4 in [P6] resulting to the duty-ratio and IVFF gains: $F_m^{IVFF} = (kU_{in}T_s)^{-1}$ and $q_i^{IVFF} = kDT_s$. As a result, $F_m^{IVFF} q_i^{IVFF}$ is equal to D/U_{in} and the ideal condition for the zero input-to-output transfer function is closely met. However, it may not be possible to make the slope of the PWM ramp directly proportional to the input voltage due to the availability of such circuits. E.g., the PWM-circuit used in [73] makes the PWM-ramp slope proportional to $k(u_{in} - 3.5\text{V})$. Therefore, the implementation is not ideal and the zero input-to-output transfer function condition can not be met. Another simple method is to make the PWM-ramp signal by charging a capacitor C_x from the input voltage through a resistor R_x and discharging the capacitor during the off time of the converter. Consequently, the ramp signal is an exponential function instead of a constant ramp. In this case, the corresponding duty-ratio and IVFF gains become as shown in (4.3) meaning that the ideal condition can not be exactly met and, therefore, the resulting input-to-output transfer function would deviate from zero [P6].

$$\begin{aligned} F_m^{IVFF} &= \frac{R_x C_x e^{\frac{DT_s}{R_x C_x}}}{T_s U_{in}} \\ q_i^{IVFF} &= 1 - e^{-\frac{DT_s}{R_x C_x}} \end{aligned} \tag{4.3}$$

When the time constant $R_x C_x$ is much larger than the switching cycle T_s, the exponent function e^x can be approximated by Taylor series by $1 + x$ [98] and, consequently, $F_m^{IVFF} q_i^{IVFF} \approx D/U_{in}$ as can be deduced from (4.3). In practice, the time constant $R_x C_x$ can not be made much larger than the switching cycle due to the inner properties of the

modulator and the noise problems caused by the resulting slowly increasing ramp voltage. However, the attenuation of the input-to-output transfer function can be greatly improved compared to the converter under VMC as demonstrated in [P6], despite the imperfections of the practical implementation.

Fig. 4.1a shows the measured or calculated (solid lines) and predicted (dashed lines) internal open-loop input-to-output transfer functions of the same buck converter under VM, PCM and IVFF-controls. The power stages and operation points of the converters are the same for efficient comparison [P6]. The measured $G_{\mathrm{io-o}}$ for the PCM-controlled buck converter shown in Fig. 8 in [P6] is erroneously presented as internal or nominal measurement. Actually, it is the measured load-affected open-loop input-to-output transfer function $G_{\mathrm{io-o}}^{\mathrm{L}}$, when the load is a resistor. The PCM-controlled converter operates as a current-source at open loop and, therefore, it can not operate with constant-current load and a resistive load has to be used. The effect of the load resistor has to be removed from the measurement to get the internal or nominal transfer function. The internal input-to-output transfer function of the PCM-controlled buck converter calculated from measurements is shown in Fig. 4.1a with the corresponding prediction. Similarly, Fig. 4.1b shows the calculated (solid line) and predicted (dashed line) open-loop input-to-output transfer functions of the superbuck converter under PCMC introduced in [P7] for comparison.

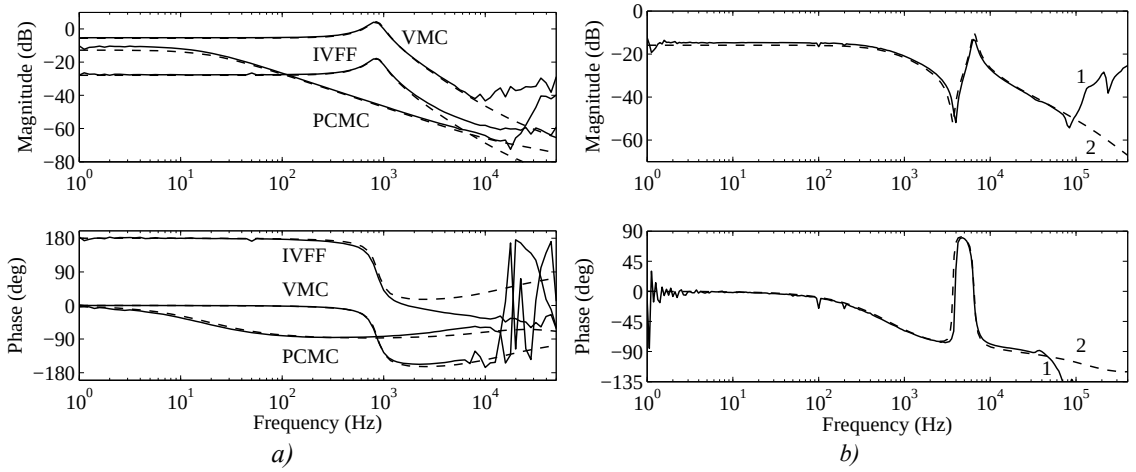


Fig. 4.1 *Measured or calculated (solid lines) and predicted (dashed lines) input-to-output transfer functions of the VM, PCM and IVFF-controlled buck converters (a) and the PCM-controlled superbuck converter (b).*

According to Fig. 4.1a, the attenuation at low frequencies is approximately -10 and -30 dB for the PCM and the IVFF-controlled converters, respectively. The attenuation is approximately -5 dB for the same buck converter under VMC. The resonant behavior typical to VM-controlled converter is present in the IVFF-controlled converter but absent in the PCM-controlled converter as expected. Therefore, at the vicinity of the resonant frequency of the converter's output filter, the input noise attenuation of the

PCM-controlled converter is better. However, the attenuation is improved more for the IVFF than the PCM-controlled converter at low frequencies. The PCM-controlled converter had to be overcompensated (i.e., the value of M_c had to be higher than the ideal value, which would result to zero input-to-output transfer function) to get the converter to work correctly without subharmonic oscillations during transients. Hence, the product $F_m^{PCMC} q_i^{PCMC}$ is approximately 60 % of the ideal value, i.e., D/U_E. Similarly, $F_m^{IVFF} q_i^{IVFF}$ for the IVFF-controlled converter is approximately 108 % of the ideal value due to the imperfections of the practical implementation. Consequently, the phase of the input-to-output transfer functions should start from 180 degrees (or equally from -180 degrees) for the IVFF-controlled converter and 0 degrees for the PCM-controlled converter as can be concluded by (4.1). The measurements and predictions shown in Fig. 4.1a confirm the above expectation.

According to Fig. 4.1b, the low-frequency input-voltage attenuation of the superbuck converter under PCMC is slightly higher in comparison to the conventional buck converter under PCMC due to more ideal compensation. The PCMC method used for the superbuck converter does not damp all the resonances in the input-to-output transfer function as shown in Fig. 4.1b. The reason for this is that the peak value of the sum current (i.e., the current flowing to output-capacitor node) is controlled instead of the individual currents. Therefore, the currents of the individual inductors can fluctuate freely within the sum, implying that resonant behavior exists at the input because the input current is equal to the current of one inductor. An examble Matlab m-file, which was used to predict the transfer functions of a superbuck converter, is shown in Appendix C. The experimental superbuck converter is shown in a photograph in Appendix D in Fig. A.2.

4.1.2 Source Interactions

As discussed in Section 2.3.3, the zero input-to-output transfer function substantially reduces the source or supply interactions by making the different input admittances (i.e., Y_{in-o}, Y_{in-sc}, $Y_{in-\infty}$ and Y_{in-c}) equal. The ideal input admittance $Y_{in-\infty}$ is independent of control method and load, but specific for a topology. Therefore, it can be expressed for a buck converter as shown in (4.4) by replacing the open-loop transfer functions with the corresponding expressions of the VM-controlled buck converter. When the zero condition for the input-to-output transfer function is met, the different input admittances are equal and can be expressed with (4.4). When the implementation of the zero condition is not exactly met, the short-circuit Y_{in-sc} and open-loop input admittances Y_{in-o} would differ from the ideal input admittance. In addition, the control method used affects the short-circuit and open-loop input admittances. The short-circuit input admittance can be expressed for the buck converters under VMC, PCMC and IVFF control as shown in (4.5).

$$Y_{in-\infty} = Y_{in-o} - \frac{G_{io-o} G_{ci-o}}{G_{co-o}} = -\frac{D I_o}{U_E} \approx -\frac{I_{in}}{U_{in}} = -D^2 \frac{I_o}{U_o} \tag{4.4}$$

$$
\begin{aligned}
Y_{\text{in-sc}}^{\text{VMC}} &= \frac{D^2}{r_{\text{E}} + sL} \\
Y_{\text{in-sc}}^{\text{PCMC}} &= \frac{D^2 - F_{\text{m}}^{\text{PCMC}}\left(q_{\text{i}}^{\text{PCMC}}\left(DU_{\text{E}} + I_{\text{o}}r_{\text{E}}\right) + DI_{\text{o}}\right) - sLF_{\text{m}}^{\text{PCMC}}q_{\text{i}}^{\text{PCMC}}I_{\text{o}}}{F_{\text{m}}^{\text{PCMC}}U_{\text{E}} + r_{\text{E}} + sL} \\
Y_{\text{in-sc}}^{\text{IVFF}} &= \frac{D^2 - F_{\text{m}}^{\text{IVFF}}q_{\text{i}}^{\text{IVFF}}\left(DU_{\text{E}} + I_{\text{o}}r_{\text{E}}\right) - sLF_{\text{m}}^{\text{IVFF}}q_{\text{i}}^{\text{IVFF}}I_{\text{o}}}{r_{\text{E}} + sL}
\end{aligned}
\tag{4.5}
$$

The short-circuit input admittances of the PCM and IVFF-controlled converters become equal to the ideal input admittance shown in (4.4), when $F_{\text{m}}q_{\text{i}}$ is equal to D/U_{E} (i.e., the zero condition for the input-to-output transfer function) in (4.5) confirming the theoretical prediction. The expressions of the corresponding open-loop input admittances can be found for PCM-controlled and IVFF-controlled buck converters in [P5] and [P6], respectively. The open-loop input admittance for the VM-controlled buck converter can be found by replacing $q_{\text{i}}^{\text{IVFF}}$ with zero in the expression of open-loop input admittance of the IVFF-controlled buck converter.

The predicted (dashed lines) and measured or calculated (solid lines) open-loop input impedances of the buck converters under VM, PCM and IVFF-controls are shown in Fig. 4.2a. The corresponding predicted short-circuit input impedances (VMC: solid line, PCMC: dashed line, IVFF: dash-dotted line) and the ideal input impedance ($Z_{\text{in}-\infty}$, dotted line) are shown in Fig. 4.2b.

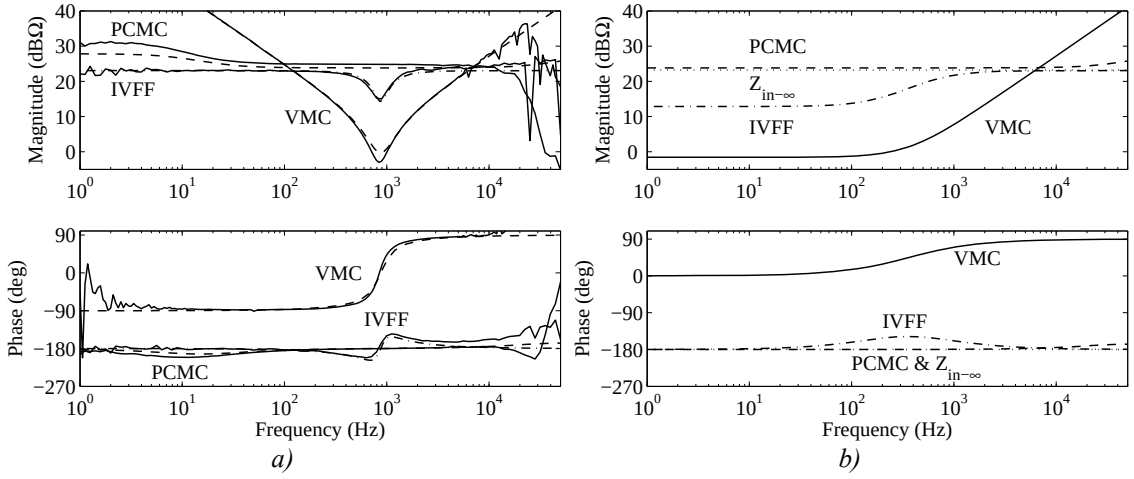


Fig. 4.2 *Predicted (dashed lines) and measured or calculated (solid lines) open-loop input impedances (a) and predicted short-circuit input impedances and the ideal input impedance (b) of the buck converters under VM, PCM and IVFF controls.*

The predictions match well with the measurements in Fig. 4.2a except at high frequencies, where the pulsating input current starts to affect the measurements. The open-loop input impedances of the PCM and IVFF-controlled converters track quite well the ideal input impedance, i.e., magnitude of 24 dBΩ and phase of -180 degrees,

except at low frequencies, where the magnitude of $Z_{\text{in-o}}$ of the PCM-controlled converter is slightly higher than the ideal input impedance. Similarly, the magnitude of $Z_{\text{in-o}}$ of the IVFF-controlled converter is slightly smaller than the ideal input impedance at the vicinity of the resonant frequency of the converter's output filter.

It is obvious that the measurement of the short-circuit input impedance is not possible in practice without changing the operation point, i.e., short-circuiting the output of the converter. Another method would be to use a very large capacitor, which has very low equivalent series resistance, in parallel with the load to nearly short-circuit the output in dynamic sense, i.e., $Z_{\text{L}} \ll Z_{\text{o-o}}$ at the frequency range of interest. Hence, the measured load-affected input impedance would be approximately equal to the short-circuit input impedance. The needed value of the capacitance would be very high (in the range of few farads) and, therefore, the short-circuit input impedances were not measured.

According to Fig. 4.2, the source interactions would be greatly reduced for the PCM-controlled converter, because the open-loop (in Fig. 4.2a) and short-circuit (in Fig. 4.2b) input impedances match quite well with the ideal input impedance $Z_{\text{in-}\infty}$ in Fig. 4.2b. Therefore, the effect of a source impedance would be nearly cancelled in the source-affected output impedance and control-to-output transfer function as can be concluded from the source-affected description of a converter in (2.7). The source interactions would also be reduced for the IVFF-controlled converter. However, the open-loop and short-circuit impedances do not follow the ideal input impedance as well as for the PCM-controlled converter.

Fig. 4.3a shows the predicted open-loop (solid line), short-circuit (dashed line) and ideal (dash-dotted line) input impedances of the PCM-controlled superbuck converter. The measured open (dashed line) and closed-loop (solid line) input impedances at the same operation point are shown in Fig. 4.3b.

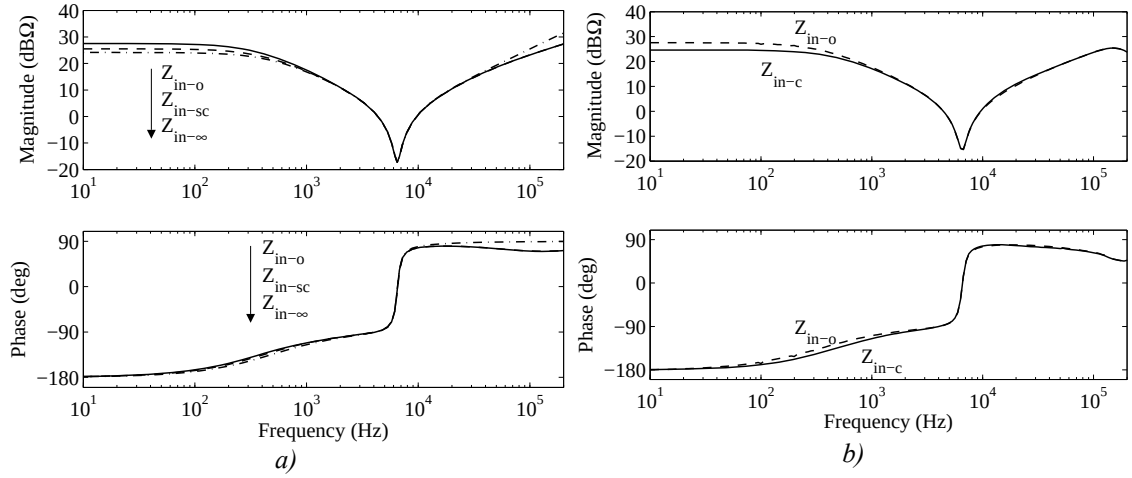


Fig. 4.3 *Predicted open-loop, short-circuit and ideal input impedances (a) and measured open and closed-loop input impedances (b) of the experimental superbuck converter.*

According to the input impedances shown in Fig. 4.3a, resonant behavior also exists in short-circuit and ideal input impedances, which represents a behavior that is totally different from what would be expected based on the characteristic behavior of the conventional buck converter. The voltage-loop gain-crossover frequency is approximately 63 kHz for the superbuck converter as shown in Fig. 13 in [P7]. Therefore, the closed-loop input impedance would follow the ideal input impedance at frequencies lower than 63 kHz (i.e., where $|L_v| \gg 1$) and the open-loop input impedance at higher frequencies (i.e., where $|L_v| \ll 1$) as can be concluded from the closed-loop input impedance shown in (3.14). This is also clearly seen by comparing Figs. 4.3a and 4.3b.

As demonstrated in [P7], the output dynamics of the PCM-controlled superbuck converter are first-order like and, hence, similar to the output dynamics of the conventional buck converter under PCMC. However, the results in Fig. 4.3 clearly indicate that the input dynamics of the superbuck converter are totally different from the conventional buck converter. Therefore, generalizing the results and design rules obtained with the conventional converters such as buck, boost, and buck-boost for other topologies with similar steady-state characteristics may lead to totally wrong conclusions due to the peculiar characteristics the higher order converters may have. It is also analyzed in [P7] that transfer functions of the superbuck converter may also have RHP-zero or zeros and possibly also poles depending on the power-stage parameters and operation conditions, which may affect the design of the converters profoundly.

4.2 Load and Supply Invariance of PCMC-OCF in Practice

As discussed in Section 2.3.3, the ideal load-transient response is achieved when the feedforward gain from the output current to the general control variable, $F_m q_o$, is equal to Z_o/G_{co}. Clearly, the implementation of the ideal gain is only possible for the minimum-phase converters such as buck. The use of output-current feedforward is most advantageous with PCMC due to increased open-loop output impedance [P5]. By using the same notation as in Chapter 2 and [P5], the ideal condition for the PCM-controlled buck converter at open loop can be stated as shown in (4.6), where G_a is the gain from the control voltage to the control current and is equal to inverse of the equivalent inductor-current-sensing resistor R_{s1}, H_i is the output-current sensing gain and R_{s2} is the equivalent output-current-sensing resistor. The ideal gain presented in (10) in [P4] is actually incorrect, but it is correct in [P5].

$$G_a H_i R_{s2} = \frac{Z_{o-o}}{G_{co-o}} = \frac{F_m^{PCMC} U_E + r_E + sL}{F_m^{PCMC} U_E} \tag{4.6}$$

According to (4.6), the ideal gain for the PCM-controlled buck converter is dependent on the operation point and power stage parameters and, therefore, practical implementation would be challenging. The ideal gain, which results in zero output impedance, derived in [75] is basically the same as in (4.6) although it is not presented

in general form. Moreover, the experimental results presented in [75] are provided with a buck-type converter and, hence, the issue of non-minimum phase converters is not discussed.

In [79], OCF-control is applied to a VM-controlled buck converter. The output current is measured directly by the current transformer. The transformer can only provide information on the output-current perturbations and, therefore, the feedforward decreased the output impedance only at high frequencies. The optimum design is based on the optimum value of the feedforward current gain by means of the integral of output-voltage squared error. The sensitivity of the different current transformer parameter values is analyzed. However, the ideal feedforward gain is not derived as a function of the transfer functions of the converter. In [81] and [82], the output-current feedforward is used to obtain resistive load-line for voltage-regulator modules supplying microprocessors.

The DC-gain of the ideal feedforward gain shown in (4.6) is close to unity and, therefore, the unity feedforward implementation (i.e., $H_\mathrm{i}=1$ and $R_\mathrm{s2}=R_\mathrm{s1}$) would provide a practical method to reduce the output impedance as demonstrated in [65] and [74]. The conclusions presented in [74] are basically correct but the statement that the output impedance of a PCM-controlled converter with unity output-current feedforward would be the same as the output impedance of the corresponding VM-controlled converter is not generally true as can be concluded based on simulations presented in [76] and experimental evidence provided in [P4] and [P5].

4.2.1 Effect of Unity Output-Current Feedforward on Output Dynamics

According to [P4] and [P5], the output-current feedforward only affects the output impedance and the control-to-output transfer function as far as the output dynamics are concerned. However, the control-to-output transfer function is actually left intact, because the gain multiplying it (i.e., $G_\mathrm{a}=\hat{i}_\mathrm{co}/\hat{u}_\mathrm{co}=1/R_\mathrm{s1}$) only changes the control signal from current to voltage domain, which is typically also used for the PCM-controlled converters due to easier practical implementation of the control circuitry.

According to [P5], when unity OCF is used (i.e., $H_\mathrm{i}=1$), the open-loop output impedance of the PCM-controlled buck converter becomes

$$Z_\mathrm{o-o}^\mathrm{PCMC\text{-}OCF}=\frac{\dfrac{1}{LC}\left(r_\mathrm{E}+\left(1-\dfrac{R_\mathrm{s2}}{R_\mathrm{s1}}\right)F_\mathrm{m}^\mathrm{PCMC}U_\mathrm{E}+sL\right)\left(1+sr_\mathrm{C}C\right)}{s^2+s\dfrac{F_\mathrm{m}^\mathrm{PCMC}U_\mathrm{E}+r_\mathrm{E}+r_\mathrm{C}}{L}+\dfrac{1}{LC}}. \tag{4.7}$$

According to the open-loop output impedance shown in (4.7), the following conclusions can be made:

- The output impedance would resemble the output impedance of the VM-controlled buck converter without the resonant behavior, when $R_{s2} = R_{s1}$.
- The output impedance would be zero at low frequencies, when $r_E + \left(1 - R_{s2}/R_{s1}\right) F_m^{PCMC} U_E = 0$, i.e., $R_{s2}/R_{s1} = 1 + r_E/\left(F_m^{PCMC} U_E\right)$, which is an operation-point-dependent constant close to unity.
- The magnitude of the output impedance would approach the output impedance of the corresponding PCM-controlled converter along the increase in the mismatch between the equivalent sensing resistors.
- The phase of the output impedance would start from 180 degrees at low frequencies, when the ratio R_{s2}/R_{s1} is higher than $1 + r_E/\left(F_m^{PCMC} U_E\right)$, indicating negative resistance behavior. Similarly, the phase would start from 0 degrees at low frequencies, when the ratio R_{s2}/R_{s1} is smaller than $1 + r_E/\left(F_m^{PCMC} U_E\right)$.

Fig. 4.4a shows the measured (solid lines) and predicted (dashed lines) open-loop output impedances of the VM-controlled buck converter and PCM-controlled buck converter without and with the OCF (i.e., $R_{s2} \approx 0.998 \cdot R_{s1}$). Fig. 4.4b shows the effect of the equivalent sensing resistors mismatch on the open-loop output impedance. The mismatch is approximately -1 %, +0 % and +2 % (the plus sign means that $R_{s2} > R_{s1}$ and the minus sign that $R_{s2} < R_{s1}$) for dashed, solid and dotted lines, respectively. A photograph of the experimental buck converter used in the analysis is shown in Appendix D in Fig. A.2 with the PCMC-OCF control circuitry.

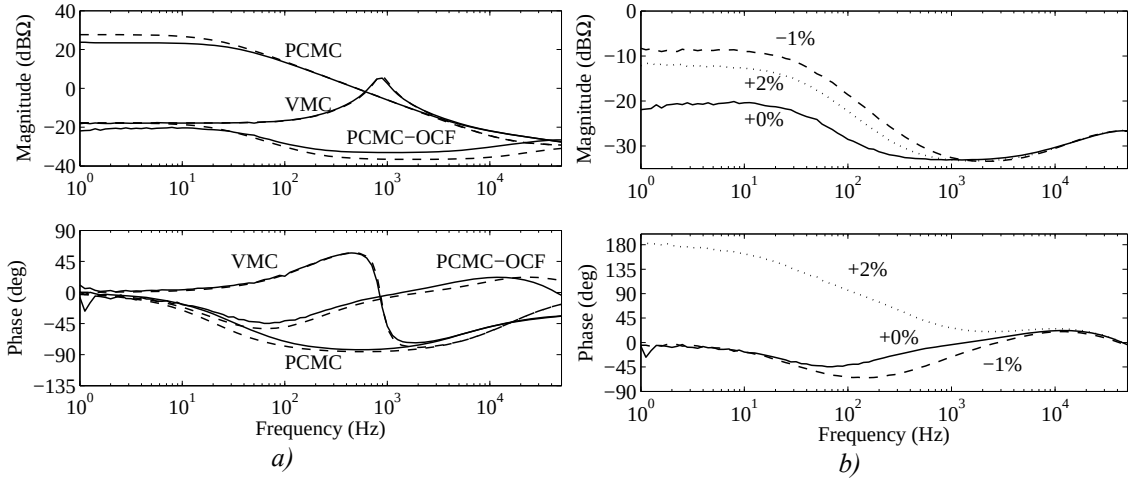


Fig. 4.4 *Measured (solid lines) and predicted (dashed lines) open-loop output impedances of a buck converter under VMC, PCMC and PCMC-OCF (a) and the measured effects of equivalent sensing resistors mismatch on the output impedance of the same converter under PCMC-OCF (b).*

The measurements agree quite well with the predictions for the VM and PCM-controlled converters as shown in Fig. 4.4a. The measured output impedance of the

converter under PCM-control with OCF is slightly higher at frequencies above 100 Hz due to the parasitic effects of the output terminals of the experimental converter. However, the OCF has significantly decreased the magnitude of the open-loop output impedance and, hence, also decreased the closed-loop output impedance, because the voltage-loop gain of the converter is left intact. The improved load transient response of the converter under PCMC-OCF is clearly seen in the Fig. 6 in [P5].

According to Fig. 4.4b, the conclusion made by (4.7) holds, i.e., the output impedance resembles the output impedance of the PCM-controlled converter along the increase in the mismatch of the equivalent sensing resistors and the negative resistance like behavior is clearly seen from the phase behavior of the dotted line, i.e., when R_{s2} is approximately 2 % than larger R_{s1}. Similar behavior also exists for the closed-loop output impedance shown in Figs. 10 and 9 in [P4] and [P5], respectively. Consequently, the load transient response exhibits overshoot as shown in Fig. 8 in [P5], when R_{s2} is 10 % larger than R_{s1}. The negative-resistance-like behavior can also make the OCF-controlled converter more prone to instability due to the capacitive loading as discussed in [P5].

The practical implementation of the OCF-control in [P4] and [P5] was conducted so that the output current was measured at low-side of the output terminal of the converter by a simple resistor, which was actually considered to be a part of the load rather than the converter. Therefore, the measurements could be compared to other measurements of the VM and PCM-controlled converters which did not have the output-current sensing resistor. In practice, the sensing resistor would affect the load voltage adversely as discussed also in [65]. If a resistor R is used to measure the output current, the output-voltage feedback should be taken at the load-side of the resistor to compensate the voltage drop. Therefore, the resistor appears in series with the open-loop output impedance resulting in the nominal closed-loop output impedance shown in (4.8).

$$Z_{o-c}^{\text{PCMC-OCF}} = \frac{Z_{o-o}^{\text{PCMC-OCF}} + R}{1 + L_v} \tag{4.8}$$

Another possibility is to use other methods to measure the output current. The method proposed in [65] and later also used in [74] only uses the current of the output capacitor measured with a current transformer. This simplifies the design of PCM-control with OCF, because the capacitor current is the difference between the inductor and load currents and, consequently, the inductor current does not need to be measured separately. Therefore, the PCM and OCF controls are provided with the same current signal. However, the method introduces additional resistance in series with the output capacitor, which can affect the output-voltage ripple adversely in some applications. In addition, if additional capacitors are connected at the output of the converter, the current of these capacitors is not used for PCM or OCF-control and, therefore, the dynamics of the converter may change adversely.

4.2.2 Effect of Unity Output-Current Feedforward on Input Dynamics

Typically, the effect of output-current feedforward is only linked to the output dynamics of a converter. However, the feedforward also affects the reverse current transfer function $T_{\mathrm{oi-o}}$ and the control-to-input transfer function G_{ci} as derived in Chapter 2 and in [P4] and [P5]. The control-to-input transfer function is virtually left intact due to the same reason as discussed in Section 4.2.1 for control-to-output transfer function and, therefore, the output-current feedforward affects only the reverse current transfer function.

When the ideal output-current feedforward gain derived in Section 2.3.3 is used, the reverse current transfer function corresponds to the ideal reverse current transfer function $T_{\mathrm{oi-\infty}}$, which for a buck converter can be expressed as shown in (4.9). For the unity OCF implementation, when the gain $H_{\mathrm{i}} = 1$, the open-loop reverse current transfer function becomes as shown in (4.10), where the coefficients *a*, *b* and *c* are defined in (4.11). It is obvious that the ratio of the equivalent sensing resistors $R_{\mathrm{s2}}/R_{\mathrm{s1}}$ affects the location of the zeros and, consequently, the shape of the reverse current transfer function significantly. According to (4.9) and (4.10), the reverse current transfer function can not be identical to $T_{\mathrm{oi-\infty}}$ when unity feedforward is used due to the different number of poles and zeros.

$$T_{\mathrm{oi-\infty}} = \frac{DU_{\mathrm{E}} + r_{\mathrm{E}} I_{\mathrm{o}} + sLI_{\mathrm{o}}}{U_{\mathrm{E}}} \tag{4.9}$$

$$T_{\mathrm{oi-o}}^{\mathrm{PCMC\text{-}OCF}} = \frac{as^2 + bs + c}{s^2 + s\dfrac{F_{\mathrm{m}}^{\mathrm{PCMC}} U_{\mathrm{E}} + r_{\mathrm{E}} + r_{\mathrm{C}}}{L} + \dfrac{1}{LC}} \tag{4.10}$$

$$\begin{aligned} a &= F_{\mathrm{m}}^{\mathrm{PCMC}} I_{\mathrm{o}} \frac{R_{\mathrm{s2}}}{R_{\mathrm{s1}}} \\ b &= \frac{1}{L}\left(\left(D - F_{\mathrm{m}}^{\mathrm{PCMC}} I_{\mathrm{o}}\right)\left(r_{\mathrm{C}} + \frac{R_{\mathrm{s2}}}{R_{\mathrm{s1}}} F_{\mathrm{m}}^{\mathrm{PCMC}} U_{\mathrm{E}}\right) + \frac{R_{\mathrm{s2}}}{R_{\mathrm{s1}}} F_{\mathrm{m}}^{\mathrm{PCMC}} I_{\mathrm{o}}\left(r_{\mathrm{E}} + r_{\mathrm{C}} + F_{\mathrm{m}}^{\mathrm{PCMC}} U_{\mathrm{E}}\right)\right) \\ c &= \frac{1}{LC}\left(D - F_{\mathrm{m}}^{\mathrm{PCMC}} I_{\mathrm{o}}\left(1 - \frac{R_{\mathrm{s2}}}{R_{\mathrm{s1}}}\right)\right) \end{aligned} \tag{4.11}$$

Fig. 4.5a shows the predicted open-loop reverse current transfer functions of the PCM-controlled buck converter with unity OCF implementation, when the ratio of the equivalent sensing resistors, $R_{\mathrm{s2}}/R_{\mathrm{s1}}$, is varied. Dash-dotted, solid and dashed lines represent the cases where R_{s2} is equal to $1.05 \cdot R_{\mathrm{s1}}$ (+5 %), $1.00 \cdot R_{\mathrm{s1}}$ (+0 %) and $0.95 \cdot R_{\mathrm{s1}}$ (-5 %), respectively. The slope of the artificial compensation ramp is the same as discussed in Section 4.1 (i.e., the product $F_{\mathrm{m}}^{\mathrm{PCMC}} q_{\mathrm{i}}^{\mathrm{PCMC}}$ is 60 % of the ideal value).

Mismatch between the equivalent sensing resistors affects the magnitude and phase of $T_{\mathrm{oi-o}}$ mainly at low frequencies as shown in Fig.4.5a.

Fig. 4.5b shows the predicted (1, dashed line) and measured (2, solid line) open-loop reverse current transfer functions of the same converter, when $R_{\mathrm{s2}} = 0.998 \cdot R_{\mathrm{s1}}$. The predicted ideal reverse current transfer function $T_{\mathrm{oi-\infty}}$ is also shown in Fig. 4.5b as the dotted line. Despite the unity feedforward implementation and a slight mismatch between the equivalent sensing resistors, $T_{\mathrm{oi-o}}$ follows the corresponding ideal transfer function quite accurately up to 10 kHz although the symbolic transfer functions presented in (4.9) and (4.10) would indicate larger differences.

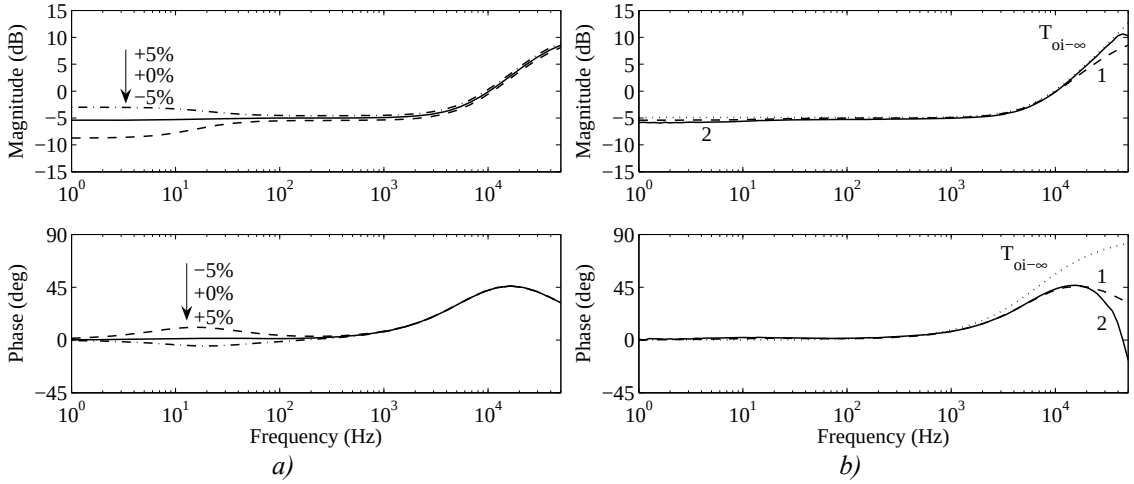


Fig. 4.5 *(a): Predicted effect of mismatch between the sensing resistors R_{s2} and R_{s1} on the open-loop reverse current transfer functions, (b): Predicted (1) and measured (2) $T_{\mathrm{oi-o}}$, when $R_{\mathrm{s2}} = 0.998 \cdot R_{\mathrm{s1}}$ with the ideal reverse current transfer function ($T_{\mathrm{oi-\infty}}$).*

According to Fig. 4.5 and Fig. 10 in [P5], the unity OCF increases the magnitude of the reverse current transfer function at high frequencies compared to the PCM-controlled converter. This may result in increased sensitivity to source interactions, because the load interactions can reflect to the source side more easily via the load-affected input admittance ($Y^{\mathrm{L}}_{\mathrm{in-o}}$) shown in the load-affected description of a converter in (2.5), if the converter is not compensated to have input-to-output transfer function close to zero.

The output-current feedforward also affects the level of source interaction reflected to the load side indirectly by changing the short-circuit input admittance, when the input-to-output transfer function is not exactly zero. The short-circuit input admittance of the PCM-controlled buck converter with unity OCF can be derived by the symbolic transfer functions presented in [P5] as shown in (4.12).

$$Y_{\text{in-sc}}^{\text{PCMC-OCF}} = \frac{D^2 - F_{\text{m}}^{\text{PCMC}}\left(q_{\text{i}}^{\text{PCMC}}\left(DU_{\text{E}} + I_{\text{o}}r_{\text{E}}\right) + DI_{\text{o}}\left(1 - \frac{R_{\text{s2}}}{R_{\text{s1}}}\right)\right) - sLF_{\text{m}}^{\text{PCMC}}q_{\text{i}}^{\text{PCMC}}I_o}{F_{\text{m}}^{\text{PCMC}}U_{\text{E}}\left(1 - \frac{R_{\text{s2}}}{R_{\text{s1}}}\right) + r_{\text{E}} + sL} \tag{4.12}$$

When the ratio of the equivalent sensing resistors is unity, the short-circuit input admittance resembles the short-circuit input admittance of the IVFF-controlled buck converter as can be concluded by comparing (4.5) to (4.12). The short-circuit input admittance becomes equal to the ideal input admittance regardless of ratio $R_{\text{s2}}/R_{\text{s1}}$, when the input-to-output transfer function is zero (i.e., $F_{\text{m}}^{\text{PCMC}}q_{\text{i}}^{\text{PCMC}} = D/U_{\text{E}}$).

The predicted short-circuit input impedances of the PCM-controlled buck converter with OCF are shown in Fig. 4.6, when R_{s2} is equal to $1.00 \cdot R_{\text{s1}}$ (+0 %, solid line), $0.95 \cdot R_{\text{s1}}$ (-5 %, dashed line) and $1.05 \cdot R_{\text{s1}}$ (+5 %, dash-dotted line). The slope of the compensation ramp is the same as in predictions shown in Fig. 4.5 and, therefore, the input-to-output transfer function is not zero and the short-circuit input impedance would differ from the ideal input impedance. The magnitude of $Z_{\text{in-sc}}$ depends highly on the ratio of the equivalent sensing resistors at low frequencies as shown in Fig. 4.6. Consequently, the unity OCF implementation has made the converter more prone to source interactions than the corresponding converter under PCMC, because the source interactions reflect to the output impedance more easily via the smaller short-circuit input impedance at low frequencies as can be concluded by comparing Figs. 4.2b and 4.6.

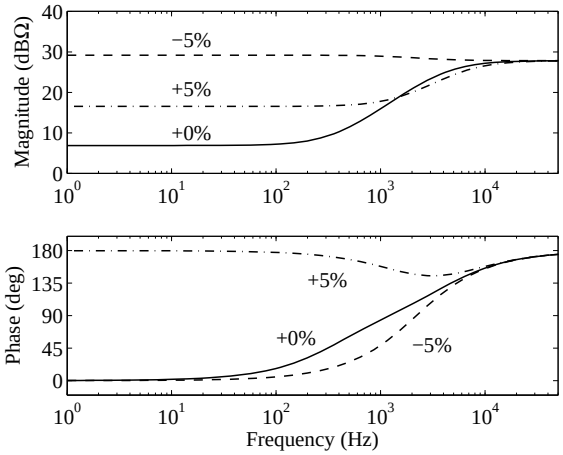


Fig. 4.6 *The predicted effect of mismatch between the equivalent sensing resistors R_{s2} and R_{s1} on the short-circuit input impedance, when $F_{\text{m}}^{\text{PCMC}}q_{\text{i}}^{\text{PCMC}}$ is 60 % of the ideal value.*

Fig. 4.7a shows the different predicted input impedances of the buck converter under PCMC and PCMC-OCF, i.e., open-loop input admittances of the both converters (1, solid line) and short-circuit input admittances of the PCM-controlled (2, dashed-line)

and PCM-controlled converter with unity OCF (3, dash-dotted line). The measured source impedance (Z_s, dotted line) represent the output impedance of single-section LC filter also used in the experimental measurements in [P4] and [P6]. Fig. 4.7b shows the measured source-affected (solid lines) and nominal (dashed lines) open-loop output impedances of the same converters.

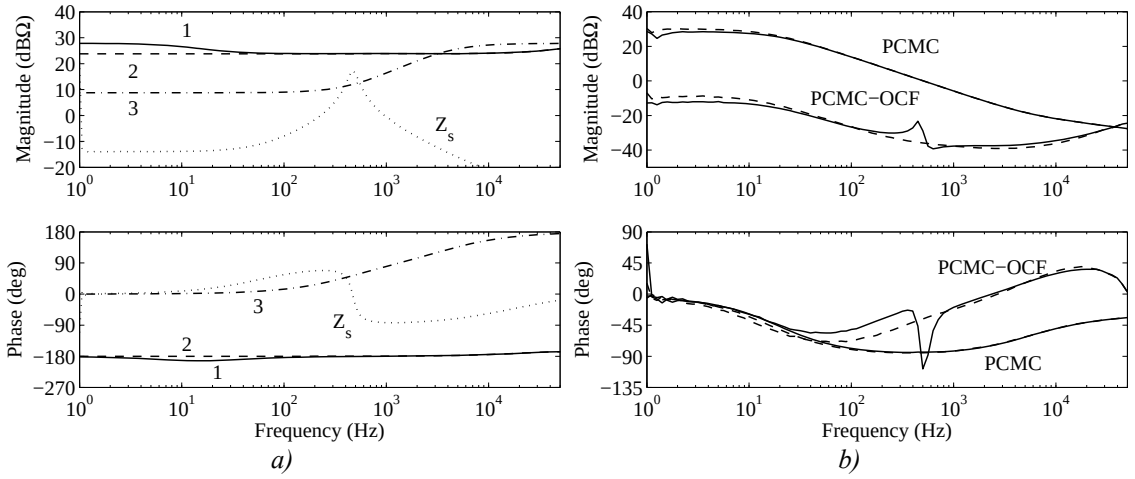


Fig. 4.7 *The different predicted input impedances of the converters under PCMC and PCMC-OCF and the source impedance seen by the converter (a), measured source-affected (solid lines) and nominal (dashed lines) open-loop output impedances of the same converters (b).*

According to Fig. 4.7a and the source-affected description of the converter in (2.7), the open-loop output impedance of the PCM-controlled converter with OCF should peak at the vicinity of 500 Hz due to the impedance overlap between the source and the short-circuit input impedances (i.e., Z_s and 3, dotted and dash-dotted lines, respectively). Fig. 4.7b confirms the predicted peaking of the output impedance. However, the source-affected open-loop output impedance of the PCM-controlled converter with OCF is significantly smaller than the corresponding impedance of the PCM-controlled converter indicating that the closed-loop output impedance would also be smaller for the converter under PCMC-OCF at the whole frequency range. The reason for this is that the source-affected voltage-loop gains are the same for the both converters as shown in Fig. 11 in [P4].

According to this section, the unity OCF implementation can actually make the PCM-controlled converter more prone to source interactions by increasing the magnitude of the reverse current transfer functions at high frequencies and by decreasing the magnitude of the short-circuit input impedance, if the inductor current feedback is not properly compensated to obtain nearly zero input-to-output transfer function. In addition, the application of the unity OCF should also be carefully considered, e.g., for a VM-controlled buck converter as used in [79], because the input-to-output transfer function of it can not be designed to be small.

5 Conclusions

This chapter provides short summaries of the publications [P1]–[P7] as well as final conlusions and remarks. The contribution of the thesis is recapitulated and future topics are also briefly discussed.

5.1 Summary of the Publications

[P1]
The stability and performance of a converter with an arbitrary load is analyzed by its closed-loop output impedance and the minor-loop gain defined at the output of the converter. System theory is used to verify that the minor-loop gain can be used to analyze internal and input-to-output stability of cascaded source and load subsystems. Hence, the closed-loop output impedance is used to define the safe load profile to avoid instability. It is shown that the stability margins of the load-side minor-loop gain do not generally match with the margins of the corresponding output-voltage loop gain of the converter. It is stated that the margins associated with the minor-loop gain should be increased at the vicinity of the voltage-loop gain-crossover frequency to avoid performance degradation of the converter, i.e., changes in stability margins and crossover frequencies. Experimental analyses are provided with VM and PCM-controlled buck converters having the same power stage and operation conditions.

[P2]
The stability and performance of a regulated converter is analyzed under source interactions. The validity of the forbidden-region-based design rules to ensure stability and performance a converter supplied by an arbitrary source subsystem is discussed. The relations between the minor-loop gain defined at the true input of a converter and the voltage-loop gain as well as closed-loop output impedance of the converter are discussed. It is shown that the forbidden-region-based design rules would ensure stability but do not necessarily provide information to maintain sufficient transient dynamics. Middlebrook's criterion is discussed to be useful, but in need of refinement to also ensure adequate transient dynamics. Hence, a safe source profile that ensures both stability and adequate performance of the experimental VM-controlled buck converter is derived. Frequency and time domain measurements are provided to support the theoretical findings.

[P3]
The effect of output-voltage remote sensing on converter dynamics is analyzed by a general and consistent formalism. Two-port representation and g-parameters are used to model the system consisting of a converter and an impedance block introduced within

the feedback loop by the application of remote sensing. The interaction formalism is derived to analyze the effect of remote sensing on all the g-parameters defining the internal open-loop dynamics of a converter. It is shown that remote sensing may change the converter dynamics profoundly and make the converter prone to instability and performance degradation due to other source and load interactions. Frequency and time domain measurements of two different VM-controlled buck converters are provided to support the theoretical discussion.

[P4]
Methods that would reduce or totally remove the source and load interactions within interconnected systems are discussed. The load and source interaction formalisms are derived by two-port representations and basic circuit theory. It is stated that a converter having zero output impedance and absolute attenuation of input-voltage noise would provide the high invariance to load and source interactions. A PCM-controlled buck converter with unity OCF is shown to have high invariance to the interactions also in practice. Frequency and time domain measurements of an experimental PCM-controlled buck converter with unity OCF are provided and compared to the measurement of the same converter under only PCM and VM controls.

[P5]
The paper provides consistent theoretical and experimental analysis of the PCM-controlled buck converter with unity OCF. The load and source interactions formalisms are derived by two-port representations and basic circuit theory. The conditions for the load and source invariance are stated. The effect of output-current feedforward on internal dynamics of a converter is analyzed with the g-parameter presentation of the converter. A PCM-controlled buck converter is modeled and its internal g-parameter set is given to evaluate the effects of the unity OCF comprehensively. The effects of imperfections in the practical implementation on the obtainable level of invariance are discussed both theoretically and experimentally. Experimental measurements in frequency and time domains are provided to compare the dynamics of the PCM-controlled converter with OCF to the dynamics of the same converter under PCM and VM controls.

[P6]
The paper provides consistent formalism to analyze the effect of IVFF control on internal dynamics of a converter. The general condition for source or input invariance is derived. An IVFF-controlled buck converter is modeled and its internal g-parameter set is given in the paper. The effect of practical implementation of the IVFF scheme is discussed and analyzed. Frequency domain measurements of the converter are provided to analyze the improved attenuation of the input-voltage noise and to compare its dynamics to the same converters under VM and PCM controls. The improved source invariance is demonstated with EMI filter interactions. Time domain measurements are

provided to show the deteriorated load-transient response of the IVFF-controlled converter due to the input-voltage-dependent maximum duty-ratio.

[P7]
A PCM-controlled fourth-order step-down converter known as superbuck operating in CCM is modeled in a consistent way by first developing the model for the corresponding VM-controlled converter. The internal dynamics of the PCM-controlled superbuck are analyzed with the symbolic transfer functions of the converter, because such models are not presented previously in literature and the dynamic features of the converter are unknown. It is shown that the converter may have similar characteristics to the conventional PCM-controlled buck converter such as first-order-like output dynamics, high input-to-output noise attenuation and insensitivity to source interactions providing that the inductor-current feedback is properly compensated. The analyses, however, show that the converter may be more susceptible to source-imposed instability, because the input dynamics are not free of resonances. The reason for this is shown to be the type of the inductor-current feedback. Frequency and time domain measurements are provided with an experimental 440-kHz converter.

5.2 Final Conclusions and Remarks

The efficient and reliable conversion of electricity from a distribution network or other sources to different DC loads with stringent requirements in terms of static accurary and transient response has necessitated the use of switched-mode converters and distributed power supply systems. Despite the many advantages of the distributed systems, they have also presented challenges for system designers in guaranteeing reliable operations, stability and performance of the systems in terms of different design issues and impedance interactions that need to be considered. The methods to model and analyze the converters and the systems composed of them have received plenty of attention during the past decades. It was noticed quite early that it is the different impedances within the systems that may compromise the stability and performance of the individual converters and systems. Consequently, a concept of minor-loop gain composing of the ratio of output and input impedances of arbitrary source and load subsystem connected in cascade has been introduced as a tool to analyze the interactions. During the past years, different forbidden-region-based design rules have been developed for the minor-loop gain to ensure stability and adequate performance of the system. The forbidden regions are usually defined based on certain gain and phase margins of the minor-loop gain so that the regions do not allow the minor-loop gain to encircle the critical point (-1,0) in the complex plane, which would result in instability according to the Nyquist stability criterion (providing that no RHP poles exist in the minor-loop gain). The different criteria are usually compared by evaluating the area they occupy in the complex plane and the simplicity of the measurement, i.e., do both the magnitude and phase of certain voltages or currents need to be measured to evaluate the violation of the forbidden region.

It is well known that the minor-loop gain defined at an arbitrary interface within a system provides information on the stability of the system. However, as discussed and analyzed in the thesis, the minor-loop gain may not at all contain the necessary information on performance degradation of converters and systems. The minor-loop gain contains the necessary information on the load-imposed performance degradation only, if it is defined at the true output of a converter, i.e., the interface from which the output-voltage feedback is taken. The load-transient response and input-to-output noise attenuation of a converter may be deteriorated due to excess peaking of the load-affected closed-loop output impedance and input-to-output transfer function. Generally, it is the peaking of the sensitivity function defined by the load-side minor-loop gain that induces the peaking on the transfer functions. According to Chapter 3, this can be avoided by a forbidden region, which is defined as a circle centered at point (-1,0). The radius of the circle can be directly determined as inverse of the allowed peaking. The criterion occupies much less area in the complex plane than the other prevailing criteria, and the violation of the criterion can be evaluated directly by only measuring the magnitudes of the signals constituting the sensitivity function. However, if the encirclement of point (-1,0) needs to be determined, both magnitude and phase information of the signals have to be measured.

The relation between the load-side minor-loop gain and load-affected voltage-loop gain of a converter has been analyzed and discussed in various publications such as [36], [47] and [48]. The analyses are based on the same equation of the load-affected voltage-loop gain, which has been derived as a function of the load-side minor-loop gain. However, the conclusions made based on the derived equation are vague in [36] and [48]: it has been stated that the load-affected voltage-loop gain is equal to the inverse of the corresponding minor-loop gain when the load interactions occur at frequencies below and near the gain-crossover frequency of the internal voltage-loop gain. Consequently, it has also been stated that the stability margins of the minor-loop gain also determine the stability margins of the voltage-loop gain. However, the inverse relation holds only at frequencies where the magnitude of the nominal voltage-loop gain is very high, i.e., typically higher than 20 dB, and diminishes rapidly when the magnitude is smaller. Therefore, the minor-loop gain can not generally determine the stability margins of the voltage-loop gain when the interactions occur at the vicinity of the gain-crossover frequency as discussed and demonstrated in Chapter 3.

When the source interactions are considered, the performance degradation can not be directly determined by the minor-loop gain defined even at the true input of a converter, i.e., additional input capacitors and internal EMI filters are considered as part of the source system rather than part of the converter. The reason for this is that the interactions reflect via the different input admittances on the converter dynamics. As discussed in Chapter 3, the peaking of the sensitivity function defined by the source-side minor-loop gain also induces peaking on the source-affected closed-loop output impedance and input-to-output transfer function of the converter. However, the output

impedance may also be affected via the interactions with the short-circuit input admittance of the converter. In addition, the source interactions reflect to the voltage-loop gain via the interactions with the open-loop and ideal input admittances of the converter. Consequently, the effect of all the input admittances (i.e., open-loop, short-circuit and ideal) need to be considered to predict the effect of source interactions on the converter dynamics. The minor-loop gains defined at other interfaces may not at all contain the correct information on source-imposed performance degradation as discussed in Chapter 3.

A common deficiency of the prevailing forbidden-region-based design criteria has been that the frequency information of the impedance interactions or overlap is lost, when the analysis results are only expressed as Nyquist plots in the complex plane. Although the possible peaking of certain closed-loop transfer functions can be determined, the frequency range where the peaking occurs is not known. E.g., if the load-side minor-loop gain implies peaking at the frequency range where the internal voltage-loop gain is high, the load-transient response of the converter may only be affected slightly and it can still be sufficient to meet the requirements. On the contrary, if the same peaking occurs at the vicinity of the voltage-loop gain-crossover frequency, the load-transient response can be affected substantially and the requirements may not be met. As discussed in Chapter 3, the gain margins associated with the load and source-side minor-loop gains should be increased at the vicinity of the gain-crossover frequencies of the internal voltage-loop gains to avoid performance degradation, i.e., the changes in stability margins and crossover frequencies. Therefore, the frequency information of the minor-loop gain is important in interaction analysis.

An accurate prediction of source and load interactions with mathematical models of converters and other subsystems can be made conveniently with the consistent interaction formalisms overviewed in Chapter 2. The formalisms are based on g-parameters and two-port representations of converters and subsystems. It is shown that the different open-loop input admittances and output impedance of a converter are the key parameters determining the effects of arbitrary source and load impedances on converter dynamics. When analyzing the interactions on commercial converter modules, such information is rarely available and the converters can be characterized only by measuring the closed-loop transfer functions. In addition, the converter modules may have internal input capacitors and additional filters and, therefore, it may not be possible to determine the impedances or the minor-loop gain at the true input and output interfaces. Consequently, accurately predicting source and load interactions becomes almost impossible without extensive laboratory experiments.

The effect of output-voltage remote sensing on the internal dynamics of a converter has been discussed and analyzed in the thesis due to the lack of comprehensive theoretical treatment in literature. The analysis formalism has been derived by the two-port representations of the converter and the impedance block connected in cascade. It has

been shown that the impedance network connected within the feedback loop may change the dynamics of a converter profoundly when remote sensing is applied. Therefore, the use of remote sensing may make the converter more prone to other source and load interactions, which can further deteriorate the transient performance or even stability of the converter.

The load and source interactions on converter dynamics can be reduced or even totally removed by proper design of the control system. As discussed in Chapter 2, the transient dynamics of a converter can be made nearly ideal with feedforward of input voltage and output current. It has been shown that the ideal feedforward gains that would result in ideal transient dynamics can be implemented only for the converters with minimum-phase control dynamics such as buck converters. It has been discussed that the ideal gains would also make the converter invariant to source and load interactions. Dynamically, this means that the open-loop input-to-output transfer function and output impedances of a converter are ideally zero. The system design would become deterministic and easy because such a converter would actually behave as a buffer within the system preventing the interactions propagating through the converter. The only issue that would need to be verified is the stability of the source-side minor-loop gain of the converter.

It has been shown and analyzed in the thesis that the PCM and IVFF-controlled buck converters would have high invariance to source interactions if the implementations of the control systems are made correctly, i.e., the inductor-current feedback is compensated properly in the PCM-controlled converter and the feedforward gain is made as close to the ideal as possible in IVFF-controlled converter. Similarly, the output-current feedforward can be used to improve the load-transient response and reduce the load interactions on output dynamics. It has been demonstrated in the thesis that the unity OCF in a PCM-controlled buck converter would provide such features although the ideal conditions can not be met exactly. However, if the inductor-current feedback of the PCM-controlled converter with unity OCF is not compensated properly, the unity OCF can actually make the converter more prone to source interactions due to the increased magnitude of the reverse current transfer function and the short-circuit input admittance.

The dynamic features of conventional second-order converters such as buck, boost and buck-boost are well treated and analyzed in literature. However, the higher-order converters are widely used, e.g., in interfacing solar arrays due to their characteristic features such as continuous currents both at the input and output. The fourth-order step-down converter known as superbuck has been modeled and analyzed under PCMC in [P7]. Similarly to the conventional buck converter, the superbuck converter can have high invariance to source interactions, but the input dynamics are not free of resonances, which makes the converter more prone to source-imposed instability. The reason for this has been shown to be the type of the current-feedback signal, which is composed of

the sum of the inductor currents flowing to the output capacitor node. Therefore, the output dynamics are similar to those of the buck converter (i.e., close to first-order) but the input dynamics are not free of resonances, because the input current is only the current of the one inductor. Consequently, the characteristic dynamics of conventional converters should not be generalized to other topologies with similar steady-state characteristics.

The main scientific contribution of the thesis can be summarized as follows:

- It is shown that the minor-loop gain provides perfect information on the stability of systems regardless at the interface where it is determined, but does not necessarily provide information on the performance degradation of the system at all. Consequently, the usefulness of prevailing forbidden-region-based design rules for performance analysis is argued.

- The peaking of sensitivity function defined by the minor-loop gain is shown to cause peaking in various closed-loop transfer functions of a converter. However, information on the inner properties of the converter is needed to evaluate the level and importance of the peaking on performance of the converter.

- It is shown that the inverse relation between the load-side minor-loop gain and the voltage-loop gain of the corresponding converter only holds at the frequencies where the magnitude of the voltage-loop gain is very high. Therefore, the margins set for the minor-loop gain should be increased at the vicinity of the gain-crossover frequency of the voltage-loop gain to ensure adequate stability margins and gain-crossover frequency.

- It is shown that the performance degradation of a converter due to source interactions can be accurately analyzed only by the open-loop, ideal and short-circuit input admittances of the converter and not by the minor-loop gain.

- Comprehensive formulation is derived to analyze the effect of output-voltage remote sensing on converter dynamics. Such formulation is not found in literature.

- Theoretical basis for obtaining source and load invariance is established. It is shown experimentally that the theoretical findings also hold in practice.

- The concept of ideal reverse current transfer function is introduced. It is shown to be an important parameter in defining the ideality of the output-current feedforward.

5.3 Future Topics

This and the recently published [26] theses together form the basis for small-signal modeling and analysis of individual converters and systems composing of them. The advantages of the dynamic profile as a tool for evaluating the suitability of a topology or a control method for a certain converter and for analyzing performance and stability of converters are currently only recognized in the academic world. Therefore, interest of the industry should be raised by organizing seminars and courses to the designers.

In the thesis, only voltage-input voltage-output converters and corresponding systems were focused on and the system-level analysis formalism was presented only for systems connected in cascade. A number of systems also exists, where the converters are voltage-input current-output converters. The converters can also be connected in parallel or series configurations. The dynamic profile of voltage-input current-output converter and its load and source interaction formalism are introduced in [26]. However, the other system configurations are not discussed comprehensively in literature. Consequently, the analyses and results presented in this thesis and in [26] should be extended to other types of system configurations to form a comprehensive set of tools for analyzing the stability and performance of all kinds of systems.

The experimental analyses were carried out by buck converters under different control methods in the thesis. In addition, the PCM-controlled superbuck converter was discussed to demonstrate its peculiar internal dynamics. There are also numerous other higher-order converters such as superboost, Ćuk and Sepic, but their internal dynamics are not comprehensively discussed in literature. Therefore, the dynamic profiles of the other basic and higher-order topologies should be derived and the applicability of the converters in different systems should be studied.

References

[1] T. G. Wilson, "The evolution of power electronics," *IEEE Trans. on Power Electronics*, vol. 15, issue 3, May 2000, pp. 439–446.

[2] R. V. White, "Emerging on-board power architectures," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, February 2003, pp. 799–804.

[3] A. Emadi, A. Khaligh, C. H. Rivetta, G. A. Williamson, "Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives," *IEEE Trans. on Vehicular Technology*, vol. 55, issue 4, July 2006, pp. 1112–1125.

[4] Y-F. Liu, "Requirements and technologies in telecom power systems," in *Proc. International Power Electronics and Motion Control Conference*, August 2000, pp. 1478–1482.

[5] A. Lidow, D. Kinzer, G. Sheridan, D. Tam, "The semiconductor roadmap for power management in the new millennium," *Proceedings of the IEEE*, vol. 89, issue 6, June 2001, pp. 803–812.

[6] Processor Power Delivery Design Guidelines For Desktop LGA775 Socket, Intel Corporation, *Voltage Regulator-Down (VRD) 11.0*, available: http://www.intel.com/design/processor/applnots/313214.htm (date: 30.1.2008)

[7] E. Lam, R. Bell, D. Ashley, "Revolutionary advances in distributed power systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, February 2003, pp. 30–36.

[8] M. P. Sayani, J. Wanes, "Analyzing and determining optimum on-board power architectures for 48V-input systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, February 2003, pp. 781–785.

[9] M. Barry, "Design issues in regulated and unregulated intermediate bus converters," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2004, pp. 1389–1394.

[10] F. C. Lee, P. Barbosa, P. Xu, J. Zhang, B. Yang, F. Canales, "Topologies and design considerations for distributed power system applications," *Proceedings of the IEEE*, vol. 89, issue 6, June 2001, pp. 939–950.

[11] L. Brush, "Distributed power architecture demand characteristics," in Proc. *IEEE Applied Power Electronics Conference and Exposition*, 2004, pp. 342–345.

[12] H. Huang, "Coordination of design issues in the intermediate bus architecture," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March 2005, pp. 169–175.

[13] R. D. Middlebrook, S. Ćuk, "A general unified approach to modeling switching-converter power stages," in *Proc. IEEE Power Electronics Specialists Conference*, 1976, pp. 18–34.

[14] R. D. Middlebrook, S. Ćuk, "A general unified approach to modeling switching-converter power stages," *International Journal of Electronics*, vol. 42, no. 6, 1977, pp. 521–550.

[15] D. Maksimović, "Computer-aided small-signal analysis based on impulse response of DC/DC switching power converters," *IEEE Trans. on Power Electronics*, vol. 15, issue 6, November 2000, pp. 1183–1191.

[16] S. Ćuk, R. D. Middlebrook, "A general unified approach to modelling switching DC-to-DC converters in discontinuous conduction mode," in *Proc. IEEE Power Electronics Specialists Conference*, 1977, pp. 36–57.

[17] J. Sun, D. M. Mitchell, M. F. Greuel, P. T. Krein, R. M. Bass, "Modeling of PWM converters in discontinuous conduction mode - a reexamination," in *Proc. IEEE Power Electronics Specialists Conference*, May 1998, pp. 615–622.

[18] D. Maksimović, A. M. Stanković, V. J. Thottuvelil, G. C. Verghese, "Modeling and simulation of power electronic converters," *Proceedings of the IEEE*, vol. 89, issue 6, June 2001, pp. 898–912.

[19] R. W. Erickson, D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed., Norwell (MA), Kluver Academic, 2001, 883 pp.

[20] B. Choi, J. Kim, B. H. Cho, S. Choi, C. M. Wildrick, "Designing control loop for DC-to-DC converters loaded with unknown AC dynamics," *IEEE Trans. on Industrial Electronics*, vol. 49, issue 4, August 2002, pp. 925–932.

[21] B. Choi, B. H. Cho, S-S. Hong, "Dynamics and control of DC-to-DC converters driving other converters downstream," *IEEE Trans. on Circuits and Systems – I: Fundamental Theory and Applications*, vol. 46, issue 10, October 1999, pp. 1240–1248.

[22] T. Suntio, I. Gadoura, "Use of unterminated two-port modeling technique in analysis of input filter interactions in telecom DPS systems," in *Proc. Annual International Telecommunications Energy Conference*, September 2002, pp. 560–565.

[23] B. H. Cho, "*Modeling and Analysis of Spacecraft Power Systems*," PhD Thesis, Virginia Polytechnic Institute and State University, 1985, 181 pp.

[24] P. G. Maranesi, V. Tavazzi, V. Varoli, "Two-port characterization of PWM voltage regulators at low frequencies," *IEEE Trans. on Industrial Electronics*, vol. 35, issue 3, August 1988, pp. 444–450.

[25] C. K. Tse, *Linear Circuit Analysis*, Addison Wesley Longman, Harlow, England, 1998, 229 pp.

[26] M. Hankaniemi, "*Dynamical Profile of Switched-Mode Converter – Fact or Fiction?*" Doctoral Thesis, Tampere University of Technology, November 2007, 131 pp.

[27] M. Hankaniemi, T. Suntio, M. Sippola, "Characterization of regulated converters to ensure stability and performance in distributed power supply systems, in *Proc. Annual International Telecommunications Energy Conference*, September 2005, pp. 533–538.

[28] T. Suntio, M. Hankaniemi, M. Karppanen, "Analysing the dynamics of regulated converters," *IEE Proc. Electric Power Applications*, vol. 153, issue 6, November 2006, pp. 905–910.

[29] T. Roinila, M. Hankaniemi, T. Suntio, M. Sippola, M. Vilkko, "Dynamical profile of a switched-mode converter – reality or imagination," in *Proc. International Telecommunications Energy Conference*, September 2007. pp. 420–427.

[30] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE Industry Applications Society Annual Meeting*, October 1976, pp. 336–382.

[31] R. D. Middlebrook, "Design techniques for preventing input-filter oscillations in switched-mode regulators," in *Proc. IEEE International Conference on Power System Technology*, May 1978, pp. A3.1–A3.16.

[32] R. C. Dorf, R. H. Bishop, *Modern Control Systems*, 9th ed., Prentice Hall, 2001, 831 pp.

[33] K. Zenger, A. Altowati, T. Suntio, "Dynamic properties of interconnected power systems – a system theoretic approach," in *Proc. IEEE Conference on Industrial Electronics and Application*, May 2006, pp. 835–840.

[34] J. B. Burl, *Linear Optimal Control: H_2 and H_∞ Methods*, Addison Wesley Longman, Inc., Menlo Park, California, USA, 1999, 462 pp.

[35] S. Schulz, B. H. Cho, F. C. Lee, "Design considerations for a distributed power system," in *Proc. IEEE Power Electronics Specialists Conference*, June 1990, pp. 611–617.

[36] C. M. Wildrick, "*Stability of Distributed Power Supply Systems*," Master of Science thesis, Virginia Polytechnic Institute and State University, 1993, 90 pp.

[37] C. M. Wildrick, F. C. Lee, B. H. Cho, B. Choi, "A method of defining the load impedance specification for a stable distributed power system," *IEEE Trans. on Power Electronics*, vol. 10, issue 3, May 1995, pp. 280–285.

[38] X. Feng, Z. Ye, K. Xing, F. C. Lee, D. Borojevic, "Impedance specification and impedance improvement for DC distributed power system," in *Proc. IEEE Power Electronics Specialists Conference*, July 1999, pp. 889–894.

[39] X. Feng, J. Liu, F. C. Lee, "Impedance specifications for stable DC distributed power systems," *IEEE Trans. on Power Electronics*, vol. 17, issue 2, March 2002, pp. 157–162.

[40] J. Liu, X. Feng, F. C. Lee, D. Borojevich, "Stability margin monitoring for DC distributed power systems via perturbation approaches," *IEEE Trans. on Power Electronics*, vol. 18, issue 6, November 2003, pp. 1254–1261.

[41] S. D. Sudhoff, S. F. Glover, "Three-dimensional stability analysis of DC power electronics based systems," in *Proc. IEEE Power Electronics Specialists Conference*, June 2000, pp. 101–106.

[42] S. D. Sudhoff, S. F. Glover, P. T. Lamm, D. H. Schmucker, D. E. Delisle, "Admittance space stability analysis of power electronic systems," *IEEE Trans. on Aerospace and Electronic Systems*, vol. 36, issue 3, July 2000, pp. 965–973.

[43] J. M. Zhang, X. G. Xie, D. Z. Jiao, Z. Qian, "Stability problems and input impedance improvement for cascaded power electronic systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2004, pp. 1018–1024.

[44] L. R. Lewis, B. H. Cho, F. C. Lee, B. A. Carpenter, "Modeling, analysis and design of distributed power systems," in *Proc. IEEE Power Electronics Specialists Conference*, 1989, pp. 152–159.

[45] P. Li, B. Lehman, "Quantative methods for DC-DC converter performance analysis in distributed power systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March 2001, pp. 778–783.

[46] P. Li, B. Lehman, "Performance prediction of distributed power systems based on small-scale prototypes," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March 2002, pp. 1161–1167.

[47] P. Li, B. Lehman, "Performance prediction of DC-DC converters with impedances as loads," *IEEE Trans. on Power Electronics*, vol. 19, issue 1, January 2004, pp. 201–209.

[48] D. Lee, B. Choi, J. Sun, B. H. Cho, "Interpretation and prediction of loop gain characteristics for switching power converters loaded with general load subsystems," in *Proc. IEEE Power Electronics Specialists Conference*, June 2005, pp. 1024–1029.

[49] S. Y. Erich, W. M. Polivka, "Input filter design criteria for current-programmed regulators," *IEEE Trans. on Power Electronics*, vol. 7, issue 1, January 1992, pp. 143–151.

[50] R. M. Tedder, "An alternate analysis of the current programmed model leads to simplified input filter design criteria," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, February 1992, pp. 756–763.

[51] C. R. Kohut, "Input filter design criteria for switching regulators using current-mode programming," *IEEE Trans. on Power Electronics*, vol. 7, issue 3, July 1992, pp. 469–479.

[52] T. Suntio, I. Gadoura, K. Zenger, "Input filter interactions in peak-current-mode-controlled buck converter operating in CICM," *IEEE Trans. on Industrial Electronics*, vol. 49, issue 1, February 2002, pp. 76–86.

[53] P. Li, B. Lehman, "Accurate loop gain prediction for DC-DC converter due to the impact of source/input filter," *IEEE Trans. on Power Electronics*, vol. 20, issue 4, July 2005, pp. 754–761.

[54] M. Florez-Lizarraga, A. F. Witulski, "Input filter design for multiple-module DC power systems," *IEEE Trans. on Power Electronics*, vol. 11, issue 3, May 1996, pp. 472–479.

[55] B. Choi, D. Kim, D. Lee, S. Choi, J. Sun, "Analysis of input filter interactions in switching power converters," *IEEE Trans. on Power Electronics*, vol. 22, issue 2, March 2007, pp. 452–460.

[56] R. D. Middlebrook, "Null double injection and the extra element theorem," *IEEE Trans. on Education*, vol. 32, issue 3, August 1989, pp. 196–180.

[57] T. Suntio, K. Kostov, T. Tepsa, J. Kyyrä, "Using input invariance as a method to facilitate system design in DPS applications," *Journal of Circuits, Systems, and Computers*, vol. 13, issue 4, 2004, pp. 707–723.

[58] C. W. Deisch, "Simple switching control method changes power converter into a current source," in *Proc. IEEE Power Electronics Specialists Conference*, 1978, pp. 300–306.

[59] S-P. Hsu, A. Brown, L. Rensink, R. D. Middlebrook, "Modelling and analysis of switching DC-to-DC converters in constant-frequency current-programmed mode," in *Proc. IEEE Power Electronics Specialists Conference*, 1979, pp. 284–301.

[60] R. B. Ridley, "A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM," in *Proc. IEEE Power Electronics Specialists Conference*, June 1990, pp. 382–389.

[61] R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. on Power Electronics*, vol. 6, issue 2, April 1991, pp. 271–280.

[62] B. Johansson, "A comparison and an improvement of two continuous-time models for current-mode control," in *Proc. Annual International Telecommunications Energy Conference*, September 2002, pp. 552–559.

[63] T. Suntio, M. Hankaniemi, T. Roinila "Dynamical modeling of peak-current-mode controlled converter in continuous conduction mode," *Journal of Simulation Modelling Practice and Theory*, vol. 15, issue 10, November 2007, pp. 1320–1337.

[64] S. S. Kelkar, F. C. Lee, "A novel feedforward compensation canceling input filter-regulator interaction," *IEEE Trans. on Aerospace and Electronic Systems*, vol. AES-19, issue 2, March 1983, pp. 258–268.

[65] R. Redl, N. O. Sokal, "Near-optimum dynamic regulation of DC-DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. on Power Electronics*, vol. PE-1, issue 3, July 1986, pp. 181–191.

[66] D. V. Otto, "Reduction of switching regulator audiosusceptibility to zero," *Electronics Letters*, vol. 22, issue 8, April 1986, pp. 441–442.

[67] L. Calderone, L. Pinola, V. Varoli, "Optimal feed-forward compensation for PWM DC/DC converters with 'linear' and 'quadratic' conversion ratio," *IEEE Trans. on Power Electronics*, vol. 7, issue 2, April 1992, pp. 349–355.

[68] R. J. King, "Feedforward control laws for the buck converter," in *Proc. IEEE Workshop on Computers in Power Electronics*, August 1994, pp. 192–197.

[69] B. Arbetter, D. Maksimović, "Feed-forward pulse-width modulators for switching power converters," in *Proc. IEEE Power Electronics Specialists Conference*, June 1995, pp. 601–607.

[70] D. Maksimović, B. Arbetter, "Feedforward pulse-width modulator for boost DC-DC power converters," *Electronics Letters*, vol. 31, issue 7, March 1995, pp. 513–514.

[71] M. K. Kazimierczuk, A. Massarini, "Feedforward control of DC-DC PWM boost converter," *IEEE Trans. on Circuits and Systems – I: Fundamental Theory and Applications*, vol. 44, issue 2, February 1997, pp. 143–148.

[72] M. K. Kazimierczuk, L. A. Starman, "Dynamic performance of PWM DC-DC boost converter with input voltage feedforward control," *IEEE Trans. on Circuits and Systems – I: Fundamental Theory and Applications*, vol. 46, issue 12, December 1999, pp. 1473–1481.

[73] J-P. Sjöroos, T. Suntio, J. Kyyrä, K. Kostov, "Dynamic performance of buck converter with input voltage feedforward control," in *Proc. European Conference on Power Electronics and Applications*, September 2005, 9 pp.

[74] G. K. Schoneman, D. M. Mitchell, "Output impedance considerations for switching regulators with current-injected control," *IEEE Trans. on Power Electronics*, vol. 4, issue 1, January 1989. pp. 25–35.

[75] L. D. Varga, N. A. Losic, "Synthesis of zero-impedance converter," *IEEE Trans. on Power Electronics*, vol. 7, issue 1, January 1992, pp. 152–170.

[76] M. Hankaniemi, T. Suntio, S. Ruotsalainen, "Load invariant buck converter – analysis and implementation," in *Proc. European Power Electronics and Application Conference*, 2005, CD-ROM publication, paper no. 367, 10 pp.

[77] S. Hiti, D. Borojević, "Robust nonlinear control for boost converter," in *Proc. Power Electronics Specialists Conference*, 1993, pp. 191–196.

[78] S. Hiti, D. Borojević, "Robust nonlinear control for boost converter," *IEEE Trans. on Power Electronics*, vol. 10, issue 6, 1995, pp. 651–658.

[79] S. Kanemaru, T. Hamada, T. Nabeshima, T. Sato, T. Nakano, "Analysis and optimum design of a buck-type DC-to-DC converter employing load current feedforward," in *Proc. IEEE Power Electronics Specialists Conference*, 1998, pp. 309–314.

[80] B. Johansson, "Analysis of DC-DC converters with current-mode control and resistive load when using load current measurements for control," in *Proc. IEEE Power Electronics Specialists Conference*, 2002, pp. 165–172.

[81] X. Zhang, G. Yao, A. Q. Huang, "A novel VRM control with direct load current feedback," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2004, pp. 267–271.

[82] A. V. Peterchev, S. R. Sanders, "Load-line regulation with estimated load-current feedforward: application to microprocessor voltage regulators," *IEEE Trans. on Power Electronics*, vol. 21, no. 6, November 2006, pp. 1704–1717.

[83] E. Figueres, J. M. Benavent, G. Garcerá, M. Pascual, "A control circuit with load-current injection for single-phase power-factor-correction rectifiers," *IEEE Trans. on Industrial Electronics*, vol. 54, issue 3, June 2007, pp. 1272–1281.

[84] A. F. Rozman, K. J. Fellhoelter, "Circuit considerations for fast, sensitive, low-voltage loads, in a distributed power system," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March 1995, pp. 34–42.

[85] C. Gezgin, W. C. Bowman, V. J. Thottuvelil, "A stability assessment tool for DC-DC converters," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March 2002, pp. 367–373.

[86] C. Gezgin, "A transient prediction and stability analysis tool for DC-DC converters," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2003, pp. 1014–1020.

[87] T. Suntio, "Unified average and small-signal modeling of direct-on-time control," *IEEE Trans. on Industrial Electronics*, vol. 53, issue 1, February 2006, pp 287–295.

[88] K. Zenger, A. Altowati, T. Suntio, "Stability and performance analysis of regulated converter systems," in *Proc. Annual Conference on IEEE Industrial Electronics*, November 2006, pp. 1975–1980.

[89] Y. Panov, M. Jovanović, "Practical issues of input/output impedance measurements in switching power supplies and application of measured data to stability analysis," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March 2005, pp. 1339–1345.

[90] S. Skogestad, I. Postlethwaite, *Multivariable feedback control: Analysis and Design*, John Wiley & Sons Ltd, West Sussex, England, 1996, 559 pp.

[91] B. Choi, "Step load response of a current-mode-controlled DC-to-DC converter," *IEEE Trans. on Aerospace and Electronic Systems*, vol. 33, issue 4, October 1997, pp. 1115–1121.

[92] A. Balestrino, A. Landi, L. Sani, "Closed loop tests for performance evaluations of controlled DC-DC switching converters," in *Proc. IEEE International Symbosium on Industrial Electronics*, May 2004, pp. 519–524.

[93] A. Balestrino, D. Carsanimi, A. Landi, L. Sani, "Circle-based criteria for performance evaluation of controlled DC-DC switching converters," *IEEE Trans. on Industrial Electronics*, vol. 53, issue 6, December 2006, pp. 1862–1869.

[94] M. Hankaniemi, T. Suntio, M. Karppanen, "Load and supply interactions in VMC-buck converter operating in CCM and DCM," in *Proc. IEEE Power Electronics Specialists Conference*, June 2006, pp. 2768–2773.

[95] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Trans. on Advanced Packaging*, vol. 22, issue 3, August 1999, pp. 284–291.

[96] J. Chen, R. Erickson, D. Maksimović, "Averaged switch modeling of boundary conduction mode DC-to-DC converters," in Proc. *Annual Conference of IEEE Industrial Electronics Society*, December 2001, pp. 844–849.

[97] M. Hankaniemi, M. Karppanen, T. Suntio, "EMI filter interactions in a buck converter," in *Proc. International Power Electronics and Motion Control Conference*, August 2006, pp. 54–59.

[98] P. T. Krein, *Elements of Power Electronics*, 1st ed. Oxford University Press, 1998, 766 pp.

Appendices

Appendix A

```
%=========================================================================%
% Nominal small-signal models for a buck converter under VM, PCM,         %
% PCMC-OCF and IVFF controls                                              %
% Copyright Matti Karppanen                                               %
% Tampere University of Technology                                        %
% Department of Electrical Energy Engineering                             %
% 2008                                                                    %
%=========================================================================%

s = tf('s');      % Laplace variable 's'

% Converter parameters
L = 105e-6;       % Inductor value
r_L = 60e-6;      % ESR of the inductor
C = 316e-6;       % Capacitor value
r_c = 33e-3;      % ESR of the capacitor
u_d = 0.3;        % Diode forward voltage drop
r_d = 55e-3;      % Diode on-time resistance
r_ds = 0.4;       % Switch on-time resistance

% Operation point parameters
Uin = 50;         % Input voltage
Uo = 10;          % Output voltage
Io = 2.5;         % Nominal output current
f_s = 100e3;      % Swithing frequency
Ts = 1/f_s;       % Swithing period
Io = Io;          % Average current of inductor
D = (Uo+r_L*Io+r_d*Io+u_d)/(Uin-r_ds*Io+r_d*Io+u_d); % Duty ratio
Iin = D*Io;       % Average input current

% Additional parameters
UE = Uin+u_d+(r_d-r_ds)*Io;
rE = r_L+D*r_ds+(1-D)*r_d;

%-------------------------------------------------------------------------%
% Nominal open-loop g-parameters for VMC
det_vmc = s^2+s*(rE+r_c)/L+1/(L*C);                % Determinant
Yin_o_vmc = (D^2*s/L)/det_vmc;                     % Input admittance
Tji_o_vmc = (D*(1+s*r_c*C)/(L*C))/det_vmc;         % Output-to-input TF
Gio_o_vmc = (D*(1+s*r_c*C)/(L*C))/det_vmc;         % Input-to-output TF
Zo_o_vmc = (((rE+s*L)*(1+s*r_c*C))/(L*C))/det_vmc;  % Output impedance
Gci_vmc = (D*UE*s/L)/det_vmc+Io;                   % Control-to-input TF
Gco_vmc = ((UE*(1+s*r_c*C))/(L*C))/det_vmc;        % Control-to-output TF

% Special input admittances
Yin_sc_vmc = (D^2)/(rE+s*L);        % Short-circuit input admittance
Yin_inf_vmc = tf(-(D*Io)/UE);       % Ideal input admittance

% Controller component values and transfer function for VMC
R1_vmc = 7.87e3;
R2_vmc = 3e3;
R3_vmc = 1.15e3;
C1_vmc = 47e-9;
C2_vmc = 470e-12;
C3_vmc = 11e-9;
Gcc_vmc = 1/(R2_vmc*(C1_vmc+C2_vmc)) ...
   *((1+s*(R1_vmc*C1_vmc))*(1+s*((R2_vmc+R3_vmc)*C3_vmc))) ...
   /(s*(1+s*(R3_vmc*C3_vmc))*(1+s*(R1_vmc*C1_vmc*C2_vmc/(C1_vmc+C2_vmc))));

% Nominal closed-loop g-parameters for VMC
Vm = 3;                % Peak-to-peak amplitude of the PWM-ramp voltage
Ga_vmc=1/Vm;                        % Modulator gain
L_vmc=Ga_vmc*Gco_vmc*Gcc_vmc;       % Voltage-loop gain

Yin_c_vmc=Yin_o_vmc-L_vmc/(1+L_vmc)*Gci_vmc*Gio_o_vmc/Gco_vmc;
Tji_c_vmc=Tji_o_vmc+L_vmc/(1+L_vmc)*Gci_vmc*Zo_o_vmc/Gco_vmc;
Gio_c_vmc=Gio_o_vmc/(1+L_vmc);
Zo_c_vmc=Zo_o_vmc/(1+L_vmc);
```

```
%-------------------------------------------------------------------------%
% Duty-ratio constrains
Mc = 8e4;         % Slope of the compensation ramp in A/s
qi_pcm = (D*(1-D)*Ts)/(2*L);              % Input-voltage feedforward gain
Fm_pcm = 1/(Ts*(Mc+(UE*(1-D-D))/(2*L)));  % Duty-ratio gain

% Nominal open-loop g-parameters for PCMC
det_pcm = s^2+s*(rE+r_c+Fm_pcm*UE)/L+1/(L*C);
Yin_o_pcm =(((D-Fm_pcm*UE*qi_pcm)*(D-Fm_pcm*Io)*s)/L)/det_pcm ...
    - Fm_pcm*Io*qi_pcm;
Tji_o_pcm =(((D-Fm_pcm*Io)*(1+s*r_c*C))/(L*C))/det_pcm;
Gio_o_pcm =(((D-Fm_pcm*UE*qi_pcm)*(1+s*r_c*C))/(L*C))/det_pcm;
Zo_o_pcm =(((rE+Fm_pcm*UE+s*L)*(1+s*r_c*C))/(L*C))/det_pcm;
Gci_pcm =((Fm_pcm*UE*(D-Fm_pcm*Io)*s)/L)/det_pcm + Fm_pcm*Io;
Gco_pcm =((Fm_pcm*UE*(1+s*r_c*C))/(L*C))/det_pcm;

% Special input admittances
Yin_sc_pcm = (D^2-Fm_pcm*(qi_pcm*(D*UE+Io*rE)+D*Io) ...
    -s*L*Fm_pcm*qi_pcm*Io) ...
    /(Fm_pcm*UE+rE+s*L);           % Short-circuit input admittance
Yin_inf_pcm = tf(-(D*Io)/UE);      % Ideal input admittance

% Controller component values and transfer function for PCMC and PCMC-OCF
R1_pcm = 33e3;
R2_pcm = 20e3;
C1_pcm = 22e-9;
C2_pcm = 470e-12;
Gcc_pcm = 1/(R2_pcm*(C1_pcm+C2_pcm))* ...
   (1+s*(R1_pcm*C1_pcm))/(s*(1+s*(R1_pcm*C1_pcm*C2_pcm/(C1_pcm+C2_pcm))));

% Nominal closed-loop g-parameters for PCMC
R_s1 = 7.5/100;         % Equivalent inductor-current sensing resistor
Ga = 1/R_s1;                          % Modulator gain
L_pcm = Ga*Gco_pcm*Gcc_pcm;           % Voltage-loop gain

Yin_c_pcm = Yin_o_pcm-L_pcm/(1+L_pcm)*Gci_pcm*Gio_o_pcm/Gco_pcm;
Tji_c_pcm = Tji_o_pcm+L_pcm/(1+L_pcm)*Gci_pcm*Zo_o_pcm/Gco_pcm;
Gio_c_pcm = Gio_o_pcm/(1+L_pcm);
Zo_c_pcm = Zo_o_pcm/(1+L_pcm);

%-------------------------------------------------------------------------%
% OCF parameters
R_s2 = 1.0*R_s1;        % Equivalent output-current sensing resistor

% Nominal open-loop g-parameters for PCMC-OCF
det_ocf = s^2+s*(rE+r_c+Fm_pcm*UE)/L+1/(L*C);
Yin_o_ocf = (((D-Fm_pcm*UE*qi_pcm)*(D-Fm_pcm*Io)*s)/L)/det_ocf ...
    - Fm_pcm*Io*qi_pcm;
Tji_o_ocf = (((D-Fm_pcm*Io)*(1+s*C*(r_c+(R_s2/R_s1)*Fm_pcm*UE)))/(L*C)) ...
    /det_ocf + R_s2/R_s1*Fm_pcm*Io;
Gio_o_ocf = (((D-Fm_pcm*UE*qi_pcm)*(1+s*r_c*C))/(L*C))/det_ocf;
Zo_o_ocf = ((rE+(1-R_s2/R_s1)*Fm_pcm*UE+s*L)*(1+s*r_c*C)/(L*C))/det_ocf;
Gci_ocf = ((1/R_s1*Fm_pcm*UE*(D-Fm_pcm*Io)*s)/L)/det_ocf ...
    + 1/R_s1*Fm_pcm*Io;
Gco_ocf = ((1/R_s1*Fm_pcm*UE*(1+s*r_c*C))/(L*C))/det_ocf;

% Special input admittances
Yin_sc_pcm = (D^2-Fm_pcm*(qi_pcm*(UE*D+Io*rE)+D*Io*(1-R_s2/R_s1)) ...
    -s*L*Fm_pcm*qi_pcm*Io) ...
    /(Fm_pcm*UE*(1-R_s2/R_s1)+rE+s*L);  % Short-circuit input admittance
Yin_inf_ocf = tf(-(D*Io)/UE);          % Ideal input admittance

% Nominal closed-loop g-parameters for PCMC-OCF
L_ocf = Gco_ocf*Gcc_pcm;
Yin_c_ocf = Yin_o_ocf-L_ocf/(1+L_ocf)*Gci_ocf*Gio_o_ocf/Gco_ocf;
Tji_c_ocf = Tji_o_ocf+L_ocf/(1+L_ocf)*Gci_ocf*Zo_o_ocf/Gco_ocf;
Gio_c_ocf = Gio_o_ocf/(1+L_ocf);
Zo_c_ocf = Zo_o_ocf/(1+L_ocf);

%-------------------------------------------------------------------------%
%IVFF parameters
C_x=1e-9;
R_x=36.5e3;
qi_ivff = 1 - exp(-(D*Ts/(R_x*C_x)));          % IVFF gain
Fm_ivff = R_x*C_x*exp(D*Ts/(R_x*C_x))/(Ts*Uin); % Duty-ratio gain
```

```
% Nominal open-loop g-parameters for IVFF
det_ivff = s^2+s*(rE+r_c)/L+1/(L*C);
Yin_o_ivff = ((D*s*(D-qi_ivff*Fm_ivff*UE))/L)/det_ivff-qi_ivff*Fm_ivff*Io;
Tji_o_ivff = (D*(1+s*r_c*C)/(L*C))/det_ivff;
Gio_o_ivff = (((D-qi_ivff*Fm_ivff*UE)*(1+s*r_c*C))/(L*C))/det_ivff;
Zo_o_ivff = (((rE+s*L)*(1+s*r_c*C))/(L*C))/det_ivff;
Gci_ivff = Fm_ivff*((D*UE*s/L)/det_ivff+Io);
Gco_ivff = Fm_ivff*((UE*(1+s*r_c*C))/(L*C))/det_ivff;

% Controller component values and transfer function for IVFF
R1_ivff = 13e3;
R2_ivff = 1.4e3;
R3_ivff = 154;
C1_ivff = 27e-9;
C2_ivff = 800e-12;
C3_ivff = 47e-9;
Gcc_ivff = 1/(R2_ivff*(C1_ivff+C2_ivff)) ...
   *((1+s*(R1_ivff*C1_ivff))*(1+s*((R2_ivff+R3_ivff)*C3_ivff))) ...
   /(s*(1+s*(R3_ivff*C3_ivff)) ...
   *(1+s*(R1_ivff*C1_ivff*C2_ivff/(C1_ivff+C2_ivff))));

% Nominal closed-loop g-parameters for IVFF
L_ivff = Gco_ivff*Gcc_ivff;         % Voltage-loop gain
Yin_c_ivff = Yin_o_ivff-L_ivff/(1+L_ivff)*Gci_ivff*Gio_o_ivff/Gco_ivff;
Tji_c_ivff = Tji_o_ivff+L_ivff/(1+L_ivff)*Gci_ivff*Zo_o_ivff/Gco_ivff;
Gio_c_ivff = Gio_o_ivff/(1+L_ivff);
Zo_c_ivff = Zo_o_ivff/(1+L_ivff);

%%%
```

Appendix B

```
%=========================================================================%
% M-file to evaluate the effect of output-voltage remote sensing and the %
% load on converter g-parameters                                          %
% Copyright Matti Karppanen                                               %
% Tampere University of Technology                                        %
% Department of Electrical Energy Engineering                             %
% 2008                                                                    %
%=========================================================================%

% Converting the data of the measured load impedance (ZL_measured)
% to frequency and complex vectors f and M_ZL
f = transpose(ZL_measured(:,1));            % frequency data to vector f
mag = 10.^(transpose(ZL_measured(:,2))/20); % magnitude in real numbers
phase = pi/180*transpose(ZL_measured(:,3)); % phase in radians
M_ZL = mag.*(cos(phase)+j*sin(phase));      % resulting complex vector

% Open and closed-loop g-parameters of the converter specified by another
% m-file converted to complex vectors by means of a function tf2cmplx as
% follows:
% function [cmplx_tf] = tf2cmplx(tf,f)
% [mag2,phase2] = bode(tf,2*pi*f);  % TF to magnitude and phase
% mag = mag2(:,:);                  % mag as real numbers
% phase = phase2(:,:);              % phase as degrees
% phase_rad = pi/180*phase;         % phase as radians
% cmplx_tf = mag.*(cos(phase_rad)+j*sin(phase_rad));

P_Yino = tf2cmplx(Yin_o,f);     % Open-loop input admittance
P_Toio = tf2cmplx(Toi_o,f);     % Open-loop output-to-input TF
P_Gci = tf2cmplx(Gci,f);        % Control-to-input TF
P_Gioo = tf2cmplx(Gio_o,f);     % Input-to-output TF
P_Zoo = tf2cmplx(Zo_o,f);       % Open-loop output impedance
P_Gco = tf2cmplx(Gco,f);        % Control-to-output TF
P_Lv = tf2cmplx(Lv,f);          % Voltage-loop gain
P_Yinc = tf2cmplx(Yin_c,f);     % Closed-loop input admittance
P_Toic = tf2cmplx(Toi_c,f);     % Closed-loop output-to-input TF
P_Gioc = tf2cmplx(Gio_c,f);     % Closed-loop input-to-output TF
P_Zoc = tf2cmplx(Zo_c,f);       % Closed-loop output impedance

% G-parameters of the connection impedance block speficied by
% another m-file converted to complex vectors
P_Yin_CIB = tf2cmplx(Yin_CIB,f);        % Input admittance
P_Toi_CIB = tf2cmplx(Toi_CIB,f);        % Output-to-input TF
P_Gio_CIB = tf2cmplx(Gio_CIB,f);        % Input-to-output TF
P_Zo_CIB = tf2cmplx(Zo_CIB,f);          % Output impedance
P_Yinsc_CIB = tf2cmplx(Yinsc_CIB,f);    % Short-circuit input admittance

%-------------------------------------------------------------------------%
% Cascaded system consisting of the converter at open-loop and the
% connection impedance block
C_Yin_CSo = P_Yino+(P_Gioo.*P_Toio.*P_Yin_CIB)./(1+P_Zoo.*P_Yin_CIB);
C_Toi_CSo = (P_Toio.*P_Toi_CIB)./(1+P_Zoo.*P_Yin_CIB);
C_Gci_CSo = P_Gci+(P_Gco.*P_Toio.*P_Yin_CIB)./(1+P_Zoo.*P_Yin_CIB);
C_Gio_CSo = (P_Gioo.*P_Gio_CIB)./(1+P_Zoo.*P_Yin_CIB);
C_Zo_CSo = (1+P_Zoo.*P_Yinsc_CIB)./(1+P_Zoo.*P_Yin_CIB).*P_Zo_CIB;
C_Gco_CSo = (P_Gco.*P_Gio_CIB)./(1+P_Zoo.*P_Yin_CIB);

% Load-affected TFs (Load impedance for the system is M_ZL)
C_Yin_CSo_L = C_Yin_CSo+(C_Gio_CSo.*C_Toi_CSo)./(M_ZL+C_Zo_CSo);
C_Toi_CSo_L = C_Toi_CSo./(1+C_Zo_CSo./M_ZL);
C_Gci_CSo_L = C_Gci_CSo+(C_Gco_CSo.*C_Toi_CSo)./(M_ZL+C_Zo_CSo);
C_Gio_CSo_L = C_Gio_CSo./(1+C_Zo_CSo./M_ZL);
C_Zo_CSo_L = C_Zo_CSo./(1+C_Zo_CSo./M_ZL);
C_Gco_CSo_L = C_Gco_CSo./(1+C_Zo_CSo./M_ZL);

%-------------------------------------------------------------------------%
% Cascaded system consisting of the converter at closed-loop and the
% connection impedance block
C_Yin_CSc = P_Yinc+(P_Gioc.*P_Toic.*P_Yin_CIB)./(1+P_Zoc.*P_Yin_CIB);
C_Toi_CSc = (P_Toic.*P_Toi_CIB)./(1+P_Zoc.*P_Yin_CIB);
C_Gio_CSc = (P_Gioc.*P_Gio_CIB)./(1+P_Zoc.*P_Yin_CIB);
C_Zo_CSc = (1+P_Zoc.*P_Yinsc_CIB)./(1+P_Zoc.*P_Yin_CIB).*P_Zo_CIB;

% Load-affected TFs (Load impedance for the system is M_ZL)
C_Yin_CSc_L = C_Yin_CSc+(C_Gio_CSc.*C_Toi_CSc)./(M_ZL+C_Zo_CSc);
```

```
C_Toi_CSc_L = C_Toi_CSc./(1+C_Zo_CSc./M_ZL);
C_Gio_CSc_L = C_Gio_CSc./(1+C_Zo_CSc./M_ZL);
C_Zo_CSc_L = C_Zo_CSc./(1+C_Zo_CSc./M_ZL);

%-------------------------------------------------------------------------%
% Cascaded system consisting of the converter at closed-loop and the
% connection impedance block with the effect of the load

% Loaf-affected g-parameters of the connection impedance block
C_Yin_CIB_L = P_Yin_CIB+(P_Gio_CIB.*P_Toi_CIB)./(M_ZL+P_Zo_CIB);
C_Toi_CIB_L = P_Toi_CIB./(1+P_Zo_CIB./M_ZL);
C_Gio_CIB_L = P_Gio_CIB./(1+P_Zo_CIB./M_ZL);
C_Zo_CIB_L = P_Zoi_CIB./(1+P_Zo_CIB./M_ZL);

% Transfer functions of the cascaded system
C_Yin_CS = P_Yinc+(P_Gioc.*P_Toic.*C_Yin_CIB_L)./(1+P_Zoc.*C_Yin_CIB_L);
C_Toi_CS = (P_Toic.*C_Toi_CIB_L)./(1+P_Zoc.*C_Yin_CIB_L);
C_Gio_CS = (P_Gioc.*C_Gio_CIB_L)./(1+P_Zoc.*C_Yin_CIB_L);
C_Zo_CS = (1+P_Zoc.*C_Yinsc_CIB_L)./(1+P_Zoc.*C_Yin_CIB_L).*C_Zo_CIB_L;
C_Lv_L = P_Lv./(1+P_Zoo.*C_Yin_CIB_L);

%-------------------------------------------------------------------------%
% Cascaded system consisting of the converter with output-voltage remote
% sensing applied over the connection impedance block and the load

% Remote-sensing affected closed-loop TFs
C_Lv_RS = (P_Gio_CIB.*P_Lv)./(1+P_Zoo.*C_Yin_CIB);
C_Yinc_RS = C_Yin_CSo-(C_Gio_CSo.*C_Gci_CSo)./(C_Gco_CSo) ...
    .*(C_Lv_RS./(C_Lv_RS));
C_Toic_RS = C_Toi_CSo+(C_Zo_CSo.*C_Gci_CSo)./(C_Gco_CSo) ...
    .*(C_Lv_RS./(C_Lv_RS));
C_Gioc_RS = C_Gio_CSo./(1+C_Lv_RS);
C_Zoc_RS = C_Zo_CSo./(1+C_Lv_RS);

% Load-affected TFs (Load impedance for the system is M_ZL)
C_Lv_RS_L = C_Lv_RS./(1+C_Zo_CSo./M_ZL);
C_Yinc_RS_L = C_Yinc_RS+(C_Gioc_RS.*C_Toic_RS)./(M_ZL+C_Zoc_RS);
C_Toic_RS_L = C_Toic_RS./(1+C_Zoc_RS./M_ZL);
C_Gioc_RS_L = C_Gioc_RS./(1+C_Zoc_RS./M_ZL);
C_Zoc_RS_L = C_Zoc_RS./(1+C_Zoc_RS./M_ZL);

%%%
```

Appendix C

```
%=========================================================================%
% Nominal small-signal model for a PCM-controlled superbuck converter    %
% Copyright Matti Karppanen                                               %
% Tampere University of Technology                                        %
% Department of Electrical Energy Engineering                             %
% 2008                                                                    %
%=========================================================================%

% Power stage component values
L1 = 15e-6;             % Inductor 1 value
rL1 = 80e-3;            % ESR of the inductor L1
L2 = 15e-6;             % Inductor 2 value
rL2 = 55e-3;            % ESR of the inductor L2
C1 = 20e-6;             % Capacitor 1 value
rC1 = 100e-3;           % ESR of the capacitor C1
C2 = 25e-6;             % Capacitor 2 value
rC2 = 10e-3;            % ESR of the capacitor C2
UD = 0.3;               % Diode forward voltage drop
rD = 50e-3;             % Diode on-time resistance
rDS = 0.25;             % Switch on-time resistance

% Operation point parameters
Uin = 15;               % Input voltage
Uo = 10;                % Output voltage
Io = 2.5;               % Output current
Fs = 440e3;             % Switching frequency
Ts = 1/Fs;              % Switching period

%=========================================================================%
% Duty-ratio calculation
co2 = (rL1+rL2-rC1)*Io;
co1 = -Uin-UD+(rC1+rDS-rD-2*rL2)*Io;
co0 = Uo+UD+(rL2+rD)*Io;

% solution for: co2*D^2 + co1*D + co0 = 0
if ( ( co1 == 0 ) && ( co2 == 0 ) ) % 0th order solution
    dussym_co = solve('co0=0','x');
elseif ( co2 == 0 )         % 1st order solution
    dussym_co = solve('x*co1+co0=0','x');
else                        % 2nd order solution
    dussym_co = solve('x^2*co2+x*co1+co0=0','x');
end
dus = eval(dussym_co);      % Duty ratios
ind=zeros(1,length(dus));

% Determines if the duty ratio is out of range
for index=1:length(dus)
    if ( (real(dus(index)) < 1) && (real(dus(index)) > 0) ...
            && (imag(dus(index)) == 0) )
        ind(index)=1;
    end
end
% Chooses the duty ratio if only one solution found
if ( (sum(ind) == 1) )
    for index2=1:length(ind)
        if (ind(index2)==1)
            D=real(dus(index2));    % Duty ratio
            Dp=1-D;                 % Complementary duty ratio
        end
    end
% More than 1 or none correct duty-ratios
else
    error('incorrect duty-ratio!')
    return
end

%=========================================================================%
% Other steady-state values
UC1 = Uin-(D*rL1-Dp*rL2)*Io;    % Average voltage of capacitor C1
UC2 = Uo;                       % Average voltage of capacitor C1
IL1 = D*Io;                     % Average current of capacitor L1
IL2 = Dp*Io;                    % Average current of capacitor L1
Iin = IL1;                      % Average input current
```

```
% Additional parameters for the model
Lp = L1*L2/(L1+L2);             % Parallel combination of L1 and L2
R1 = rL1+rC2+D*rDS+Dp*(rD+rC1);
R2 = rC2+D*rDS+Dp*rD;
R3 = rL2+rC2+D*(rDS+rC1)+Dp*rD;
U1 = Uin+UD+(rD-rDS+D*rC1-D*rL1+Dp*rL2)*Io;
U2 = Uin+UD+(rD-rDS-Dp*rC1-D*rL1+Dp*rL2)*Io;

% Duty-ratio constrains
qL1 = 1+( (D*Dp*Ts)/2 )*( (rC1+rD-rDS)/L1+(rD-rDS)/L2 );
qL2 = 1+( (D*Dp*Ts)/2 )*( (rD-rDS)/L1+(rD-rDS-rC1)/L2 );
qC1 = D*Dp*Ts*(L1+L2)/(2*L1*L2);
M12 = ( U1/L1 + U2/L2 );
Mc = 8.35e5;                % Slope of the compensation ramp in A/s
Dmax = 0.5+Mc/M12;          % Mode limit
Fm = 1/(Ts*Mc+(((Dp-D)*Ts)/2)*(M12) );  % Duty-ratio gain

%=========================================================================%
% PCM state-space matrixes
Aa = ...
[-(R1+Fm*qL1*U1)/L1,-(R2+Fm*qL2*U1)/L1,-(Dp+Fm*qC1*U1)/L1,-1/L1;
 -(R2+Fm*qL1*U2)/L2,-(R3+Fm*qL2*U2)/L2,(D-Fm*qC1*U2)/L2,-1/L2;
 (Dp+Fm*qL1*(IL1+IL2))/C1,-(D-Fm*qL2*(IL1+IL2))/C1,(Fm*qC1*(IL1+IL2))/C1,0;
 1/C2,1/C2,0,0];
Be = ...
[1/L1,rC2/L1,(Fm*U1)/L1;
 0,rC2/L2,(Fm*U2)/L2;
 0,0,-(Fm*(IL1+IL2))/C1;
 0,-1/C2,0];
Ce = ...
[1,0,0,0;
 rC2,rC2,0,1];
De = ...
[0,0,0;
 0,-rC2,0];

SYSss = ss(Aa,Be,Ce,De);    % Open-loop state-space model
TFS = tf(SYSss);            % Open-loop transfer-function matrix

Yino = TFS(1,1);            % Open-loop input admittance
Toio = TFS(1,2);            % Open-loop output-to-input TF
Gci = TFS(1,3);             % Open-loop control-to-input TF
Gioo = TFS(2,1);            % Open-loop input-to-output TF
Zoo = -TFS(2,2);            % Open-loop output impedance
Gco = TFS(2,3);             % Open-loop control-to-output TF

Yin_inf = minreal(Yino-(Gioo*Gci)/Gco); % ideal input admittance
Yin_sc = minreal(Yino+(Gioo*Toio)/Zoo); % short-circuit input admittance

%=========================================================================%
Rs = 10/100;                % Equivalent inductor-current sensing resistor
Ga = 1/Rs;                  % Modulator gain

% Controller parameter values and transfer function
R1c = 3.3e3;
R2c = 3.9e3;
R3c = 16e3;
C1c = 68e-9;
C2c = 220e-12;
C3c = 100e-12;
Z1 = 1/(R1c*C1c);
Z2 = 1/((R2c+R3c)*C3c);
P1 = 1/(R3c*C3c);
P2 = 1/((R1c*C1c*C2c)/(C1c+C2c));
K = 1/(R2c*(C1c+C2c));
s = tf('s');                % Laplace variable 's'
Gcc = K*((1+s/Z1)*(1+s/Z2))/(s*(1+s/P1)*(1+s/P2)); % Controller TF

% Nominal closed-loop g-parameters
Lv = Gcc*Ga*Gco;            % Voltage-loop gain
Yinc = Yino-((Gioo*Gci)/Gco)*(Lv/(1+Lv));
Toic = Toio+((Zoo*Gci)/Gco)*(Lv/(1+Lv));
Gioc = Gioo/(1+Lv);
Zoc = Zoo/(1+Lv);

%%%
```

Appendix D

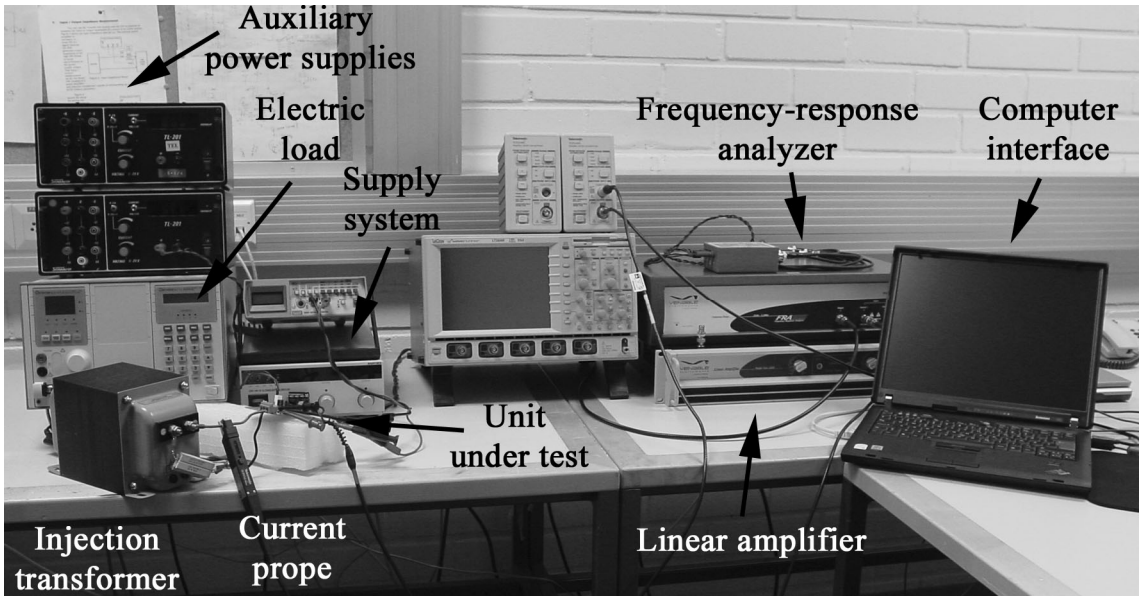


Fig. A.1 *Laboratory measurement setup.*

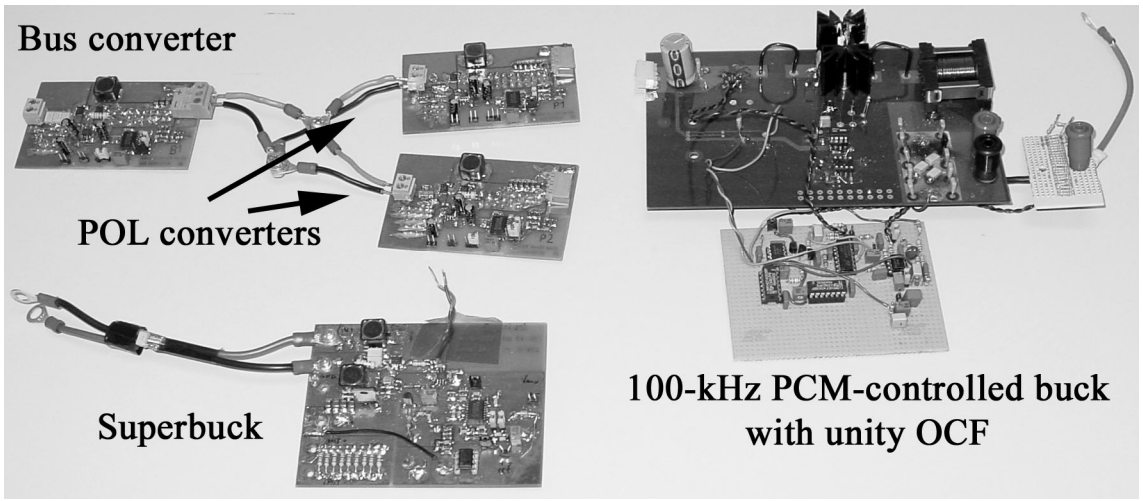
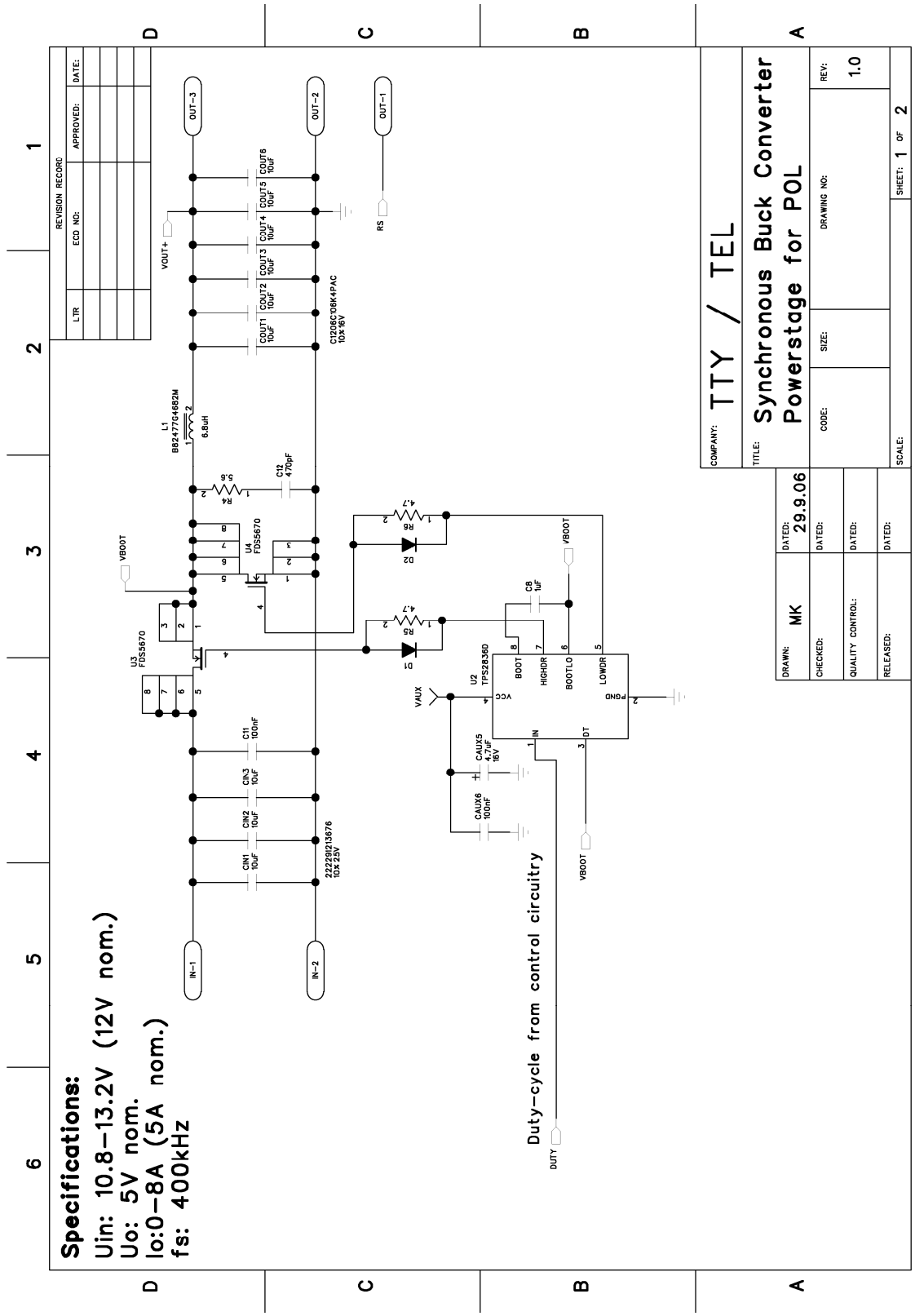


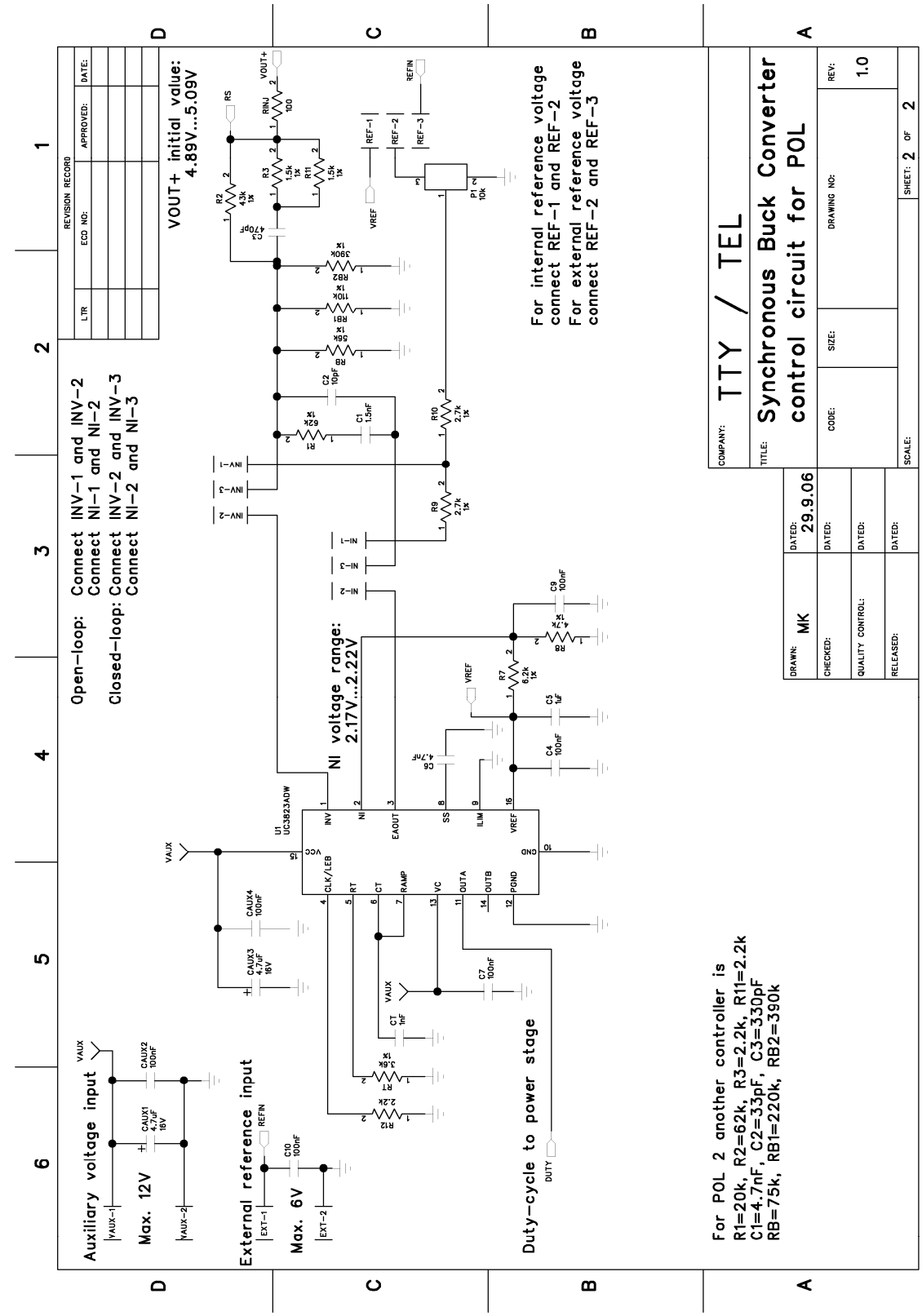
Fig. A.2 *The experimental converters.*

Table A.1 *Manufacturers and models of the equipments used in the thesis.*

Equipment	Manufacturer	Model
Frequency response analyzer	Venable Instruments	3120
Linear amplifier	Venable Instruments	VLA 1000
Electric load	Chroma	Main frame: 6312 Load unit: 63103
Supply system	Xantrex	XHR 100-10
Current probe	Tektronix	Amplifier: TCPA300 Probe: TCP312


Specifications:
Uin: 10.8–13.2V (12V nom.)
Uo: 5V nom.
Io:0–8A (5A nom.)
fs: 400kHz
Duty–cycle from control circuitry
COMPANY: TTY / TEL
TITLE: Synchronous Buck Converter Powerstage for POL
DRAWN: MK
DATED: 29.9.06
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SHEET: 1 OF 2
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
IN–1
IN–2
OUT–1
OUT–2
OUT–3
VOUT+
RS
VBOOT
VAUX
DUTY
L1
B82477G4682M
6.8uH
C12
470pF
R4
5.6
U4
FDS5670
U3
FDS3670
D1
D2
R5
4.7
C8
1uF
U2
TPS2836D
BOOT
HIGHDR
BOOTLO
LOWDR
VCC
GND
IN
DT
CAUX5
4.7uF
16V
CAUX6
100nF
C11
100nF
CIN3
10uF
CIN2
10uF
CIN1
10uF
2222892136
10x 25V
COUT1
10uF
COUT2
10uF
COUT3
10uF
COUT4
10uF
COUT5
10uF
COUT6
10uF
C1206C106K4PAC
10x 16V

a)



b)

Fig. A.3 *Example schematic of a synchronous buck converter: Power stage and gate drive (a), PWM and control circuit (b).*

Publications