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GHz RANGE CMOS LNA

Master of Science Thesis

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ABSTRACT

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This thesis work presents 7GHz CMOS Common Gate LNA, Layout design and a scaled down version of the same topology with BJT, operating frequency of 5MHz. Schematic was designed in OrCAD Capture CIS, gain and linearity results were taken. PCB LNA was modified to operate at the target frequency of 5MHz. Its linearity, gain measurements and practical results were taken by using oscilloscope and spectrum analyzers. These measurements results were then compared with the results taken previously in OrCAD Capture CIS design environment. Both the measurement results were taken by giving different input powers. The goal was to check the behavior of LNA and to see the effects of different components on its gain and linearity. Also the task was to find out for what range of input power it remains linear and stable.

Another part of this thesis work is GHz range Complementary Metal Oxide Semiconductor (CMOS) LNA and then followed by the design layout for the circuit. Schematic for GHz range LNA was designed using Cadence Virtuoso 45nm technology, and operational frequency target was 7GHz. The design followed mainly the same methodology as it was for the MHz range LNA, but here in CMOS technology the higher operational frequency was selected. Common gate stage was designed to operate at targeted frequency, and since common gate has low input and high output impedance, buffer stage is needed for output matching. White's Cascode buffer stage was introduced for output impedance matching. Different parameters results are needed to be achieved for LNA design before stepping forward into Layout design. Such as Scattering parameters, Noise Figure, Stability, transient analysis, Linearity, 1dB compression point and IP3 measurement.

Next part of thesis work consists of Layout design of 7GHz CMOS LNA. A Layout was carefully designed by taking care of allocation of metal layers to avoid extra sheet resistances, and paths were capable of withstanding enough current density. Its parasitic extracted results were compared with the results obtained from the schematic design. Clear difference was noticed during comparison between important parameters, such as gain and operational frequency.

PREFACE

This Master thesis ”GHz Range CMOS LNA” is performed to fulfill the requirements for M.Sc. in Electrical Engineering. It was performed at RFIC Laboratory, Faculty of Computing and Electrical Engineering, Tampere University of Technology, under the supervision of Prof. Nikolay T. Tchamov.

Upon successful completion of my thesis work, I am profoundly grateful to Prof. Nikolay T. Tchamov for providing an interesting topic, supervising and examining my research work. I would also like to thank my immediate supervisor Jani Järvenhaara, who guided me effectively with great advices and for his kind help under different circumstances. It was a fascinating experience to work under their supervision. I would also like to thank Aneeb Sohail and Ilari Nevalainen for their support and important suggestions throughout my working tenure.

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Tampere, 15.10.2018

Amad Khattak

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LIST OF ABBREVIATIONS

CB	Common Base
CG	Common Gate
LNA	Low-Noise Amplifier
L	Inductance
C	Capacitance
IP3	Third-order intercept point
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
NF	Noise Figure
CS	Common Source
NMOS	N-type metal oxide semiconductor
PMOS	P-type metal oxide semiconductor
K	K-factor or Stern Factor
DBm	Power level in decibels referenced to 1mW level
R	Resistance
RF	Radio Frequency
GPDK	Generic Process Design Kit
DRC	Design Rule Check
LVS	Layout Versus Schematic
LO	Local Oscillator

1. INTRODUCTION TO LOW NOISE AMPLIFIER

A low noise figure RF preamplifier, Low Noise Amplifier (LNA) is generally the first significant active block of the radio receiver after antenna or duplexer, and its noise performance characterize the noise figure of the whole receiver [1] [2] [3]. It is an electronics amplifier that is used to amplify the signal, which is received through antenna, where the signal is very weak and should be amplified with minimum addition of noise. Therefore, LNAs are described mainly by the noise they add to the input signal, which means, lowering the NF, the better it is [4]. Addition of high noise value might result in losing the important information, by being corrupted or even losing it completely. LNA has to meet number of parameters, such as noise figure (NF), high gain, input and output matching, low power consumption, stability at the frequency of interest and linearity [5].

Different aspects of performances of an amplifier are necessary to kept in mind. Other than linearity, noise, maximum voltage swing, gain, speed, power dissipation, supply voltage, input and output impedances regulates the circuit interaction with the previous and successive stages. All these different parameters trade-off with each other, which makes the design a multidimensional task. Figure1 below shows these multidimensional problems in the design of high quality amplifiers, needs insight knowledge and experience to come to an acceptable compromise(s) between important trade-off [6].

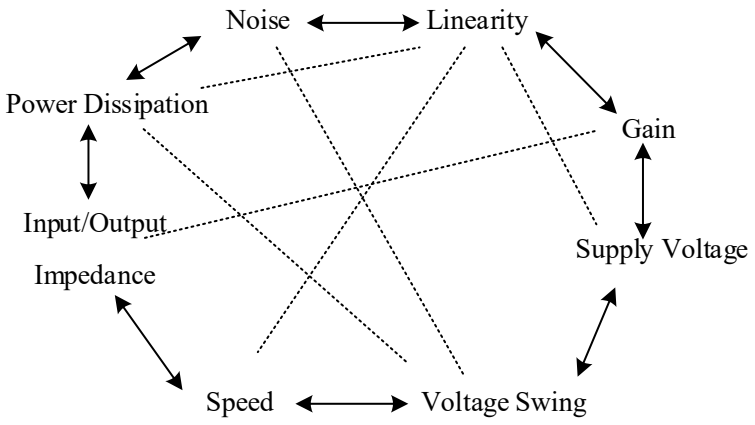

Figure 1: Analog design octagon

Low noise amplifier is one of the crucial building block of commonly used super-heterodyne receiver. After signal is received at antenna, the bandpass filter minimizes the chances of addition of interfering signals into the wanted signal, and that's how the amplifier can be saved from overloading by those interfering high power signals. LNA amplifier comes next, which basic function is to amplify that received signal, which is weak, and to reduce the noise power added to that signal. In next step, the LNA output is fed to the mixer, and its use for the downconversion of received signal from higher to a lower frequency signal. Local oscillator (LO), is set same with the level of frequency which is closer to RF input and mixer output will be comparatively low, and can be filtered out through IF band-pass filter. The following IF amplifier with high gain, boost the power level of this filtered signal, so the baseband information can be reclaimed with minimum distortion [7].

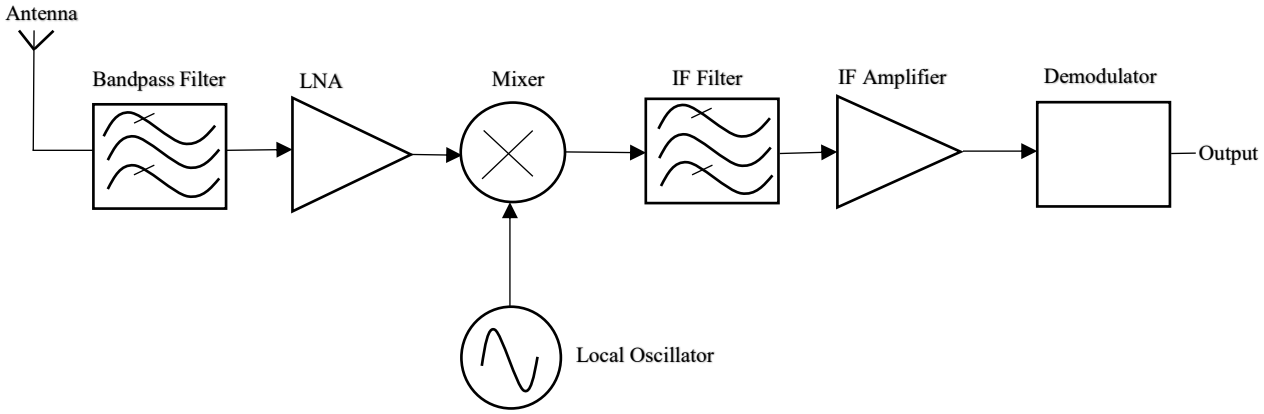

Figure 2: Block diagram of Super-Heterodyne receiver

1.1 Important Parameters

1.1.1 Noise Figure

Noise could be the decisive aspect in evaluating the system performance, it is all the time playing its crucial role in any microwave of electronic system [8]. Noise Figure (NF) tells about how much any specific block is adding noise to the signal, which is going through receiver. The noise figure of LNA combines with that of receiver, which as a result effects the performance metrics of the overall wireless communication system [9] [10] [11] [12]. Usually receivers have total noise figure of 6 to 8dB, which is combination of different blocks. For LNA noise contribution, it adds between 2 to 3dB, but this value depends on performance of all the stages in system [13].

$$NF = \frac{\overline{V_{n,out}^2}}{A_0^2} \cdot \frac{1}{4kTR_S} \tag{1.1}$$

$$= 1 + \frac{\overline{V_{n,in}^2}}{4kTR_S} \tag{1.2}$$

$\overline{V_{n,out}^2}$ comprise of both source impedance noise and LNA noise, $A_{0=} \mid \alpha \mid A_v$ is gain from V_{in} to V_{out}, k is Boltzmann's constant and T is absolute temperature, and R_S is also constant in this case as source impedance is 50Ω [13].

To know about how much noise is present in the circuit, the noise figure (NF) can be quantified as,

$$NF = \frac{SNR_{IN}}{SNR_{OUT}} \tag{1.3}$$

Signal-to-noise ratio (SNR) is defined as the signal power divided by noise power. For noiseless circuit, the output SNR is equal to input SNR or NF is $0dB$. In decibels we can express NF as,

$$NF_{dB} = 10\log\frac{SNR_{IN}}{SNR_{OUT}} \tag{1.4}$$

Noise figure for n cascaded RF stages is given by Friis equation,

$$F_{CASCADED} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \cdots + \frac{F_n-1}{G_1 \ldots G_{n-1}} \tag{1.5}$$

F_n is the noise factor and G_n is the gain, of the nth stage. Now it can be understood that the first stage of cascaded system is setting the noise figure.

1.1.2 Gain

LNA gain should be high enough that it reduce the noise addition of following stages, especially, of downconversion mixer(s). In present-day RF design, LNA directly runs the downconversion mixer(s) without impedance matching among them [13].

The output voltage divide by input voltage gives the voltage gain (eq. 1.3). But RF gain is for the most part power gain (eq. 1.4). When input and output of two-port are both conjugate matched, the voltage gain and power gain are both equal (eq. 1.5)

$$A_V = V_{OUT}/V_{IN} \tag{1.6}$$

Power Gain

$$A_p = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}^2/Z_L}{V_{IN}^2/Z_{IN}} \tag{1.7}$$

Voltage Gain $A_V(dB) = 20\log\left[\frac{V_{OUT}}{V_{IN}}\right] = 10log\left[\frac{V_{OUT}^2/Z_L}{V_{IN}^2/Z_{IN}}\right] = 10log\left[\frac{V_{OUT}^2}{V_{IN}^2}\right] = G(dB)$ (1.8)

Only if $Z_L = Z_{IN}$

1.1.3 Linearity

A system, which proves these two statements true, is considered linear: 1) Input and Output frequencies remains identical. 2) Frequency experience only magnitude and phase change. If a system does not meet these requirements, it is considered to be a non-linear system. In most applications, adding to collective gain through receiver chain, the following stages such as the baseband amplifiers or filters contribute to restrain the total input IP3 (third order intercept point) or P1dB (1dB compression point) [13]. These two are the merits, which are usually used to present the non-linearity in RF devices. Therefore, we design and develop LNAs with less worry for its linearity [13].

1.1.4 1dB Compression Point

The input signal value that results in the drop of gain of DUT by 1dB, is called 1dB Compression Point. On a log-log scale, as a function of input value, the output value drops below its ideal value by 1 dB at 1-dB compression point. A memoryless two port network with less non-linearity, we can give the system equation as power series.

$$y(t) = \alpha_1 v_1^1 + \alpha_2 v_1^2 + \alpha_3 v_1^3 \ldots. \tag{1.9}$$

If a signal $Acos\omega t$ is given into to the system, we get:

$$y(t) = \alpha_1 Acos\omega t + \alpha_2 A^2 cos^2\omega t + \alpha_3 A^3 cos^3\omega t \tag{1.10}$$

Further it leads to the next equation [13],

$$y(t) = \frac{\alpha_2 A^2}{2} + \left[\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right] cos\omega t + \frac{\alpha_2 A^2}{2} cos2\omega t + \frac{\alpha_3 A^3}{4} cos3\omega t \tag{1.11}$$

1-dB compression point, also represented by P1dB, is most of the time in between range of -20 to -25dBm at the input of receiver [13].

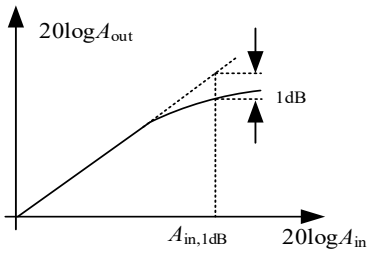

Figure 3: Definition of 1-dB compression point

1.1.5 Third Order Intercept Point

If an input signal of amplifier have several frequency components, its output resulted signal will be of new frequency components, and they are called intermodulation frequencies. For the small input signals, its resulted signal of intermodulation frequencies will be also small, the signal detection at output will be less effected. But when input signal is increased, signal with intermodulation frequencies increases significantly. A point where the third order intermodulation signal amplitude becomes equal to that of linear gain output amplitude, that output signal level is third order intercept point [14].

For better understanding, if we have two signals $Asin\omega_1 t$ and $Asin\omega_2 t$ at the input of a system at equation 1.6. The mixed output product of those input signals, and the frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are third order terms. Equations 1.9 and 1.10 are given for third order term

$$2\omega_1 - \omega_2 : \frac{3\alpha_3 A^3}{4}\cos(2\omega_1 - \omega_2)\, t \tag{1.12}$$

$$2\omega_2 - \omega_1 : \frac{3\alpha_3 A^3}{4}\cos(2\omega_2 - \omega_1)\, t \tag{1.13}$$

The equation above tells that third order terms are proportional to cube of the fundamental term, so they increases three times quicker as compare to fundamental term. Figure below shows the illustration on log-log scale. And third order and fundamental tones at the output of mixing device are shown in figure given below [13].

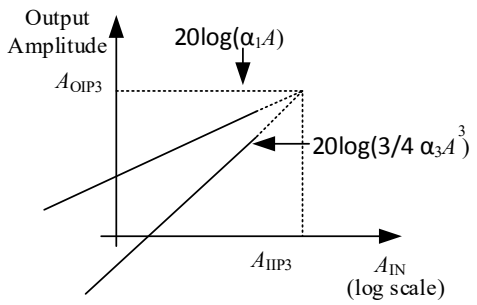

Figure 4: Definition of IP_3 (for voltage quantaties)

Third order products are important, because they may be located closer to the signal band of interest/data, which makes it impractical to filter them out using any filters.

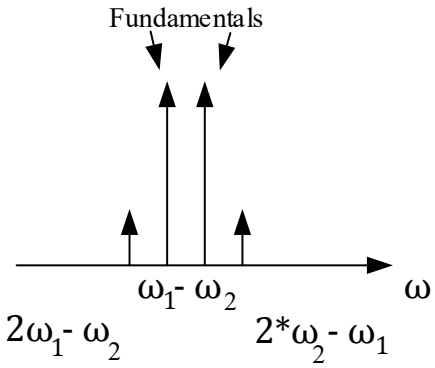

Figure 5: Fundamental and third order tones at output of mixing device

1.1.6 Scattering Parameters

Commonly known as S-Parameters, are established on common properties, for example as reflection and gain. Since they are easy to measure at higher frequencies, and conventional microwave design works on transfer of power from one phase to the following phase. Thus microwave theory models devices, systems, and circuits by specifications that can be achieved through measurement of power quantity. In figure below, at the input port, V1+ and V2-, denotes the incident and reflected waves respectively. V2+ and V2- denotes incident and reflected waves at the output ports respectively.

Equation below defines S-Parameters.

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \quad (1.14)$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \quad (1.15)$$

$S_{11} = \frac{V_1^-}{V_1^+}$, when $V_2^+$is zero and port 2 terminated accordingly

$S_{21} = \frac{V_2^-}{V_1^+}$, when V_2^+ is zero and port 2 terminated accordingly

$S_{22} = \frac{V_2^-}{V_2^+}$, when V_1^+ is zero and port 1 terminated accordingly

$S_{12} = \frac{V_1^-}{V_2^+}$, when V_1^+ is zero and port 1 terminated accordingly

S11 shows the reflection coefficient observed at port1 and S22 shows the reflection coefficient observed at port2. S21 shows gain from port 1 to 2, and S12 shows the gain from port 2 to 1.

2. BACKGROUND

2.1 System Consideration

One of the first effort to consider Ge-transistors RF amplifier, was published at ISSCC by Saunders in 1966 [15]. It was a four stage amplifier with 12 dB gain in C-band and 8dB noise figure (NF). One of the earliest publications with special attention on C-band bipolar transistor amplifier in GaAz technology was published in 1970 by [16]. Main target was radar receiver applications, with NF of 2 dB and gain of 14 dB. Early solid state design amplifiers were consisted of a single transistors, with some passive components for better matching. In 1972 [17], by It achieved a NF of 3 dB and gain of 11.5 dB at 4 GHz, and at 6GHz it achieved 4.2 dB of NF and 8 dB of gain.

Later in 80's and early 90's, BiCMOS and III-V compound technologies lead the RF LNA market. NF of 2 dB was easily achievable with silicon, which is tolerable within wireless communication standards, such as GSM and DECT. For all that, the 0.1-µm T-gate InAIAs-InGaAs-InP HEMT developed in III-V compound technologies amid the same era exhibit exceptional performance, for example NF of 3.2 dB and gain with 17.5 dB was achieved with LNA for frequency ranging from 91 to 96 GHz [18].

Advancement in technology scaling, the tuning frequency (f_T) of the transistors have increased from few GHz to hundreds of GHZ for present deep submicron processes. RF CMOS is not only the backbone for systems-on-a-chip (SoCs) designed into mobile handsets, but also mm-wave and sub-THz frequency circuits in CMOS have become practical as well. Lately, LNAs for multimode, multiband and software-defined radio architecture [19] [20] [21] set up by CMOS technology are under further development [4].

2.2 LNA Topologies

Table1 shows number of LNA topologies, some of them will be discussed in this chapter [13].

Table 1: Overview of LNA topologies

Common-Source Stage with	Common Gate Stage with	Broadband Topologies
▪ Inductive Load ▪ Resistive Feedback ▪ Cascode, Inductive Load, Inductive Degenration	▪ Inductive Load ▪ Feedback ▪ Feedforward ▪ Cascode and Inductive Load	▪ Noise-Cancelling LNAs ▪ Reactance-Cancelling LNAs

2.3 Common-Source Stage with Resistive Load

Transconductance characteristic of MOSFET converts gate-source voltage (Vgs) alteration to a small-signal drain current, which passing through a resistor and generates output voltage. Figure5(a) showing common-source (CS) circuit execute such operation. Its input impedance is very high at lower frequencies [6].

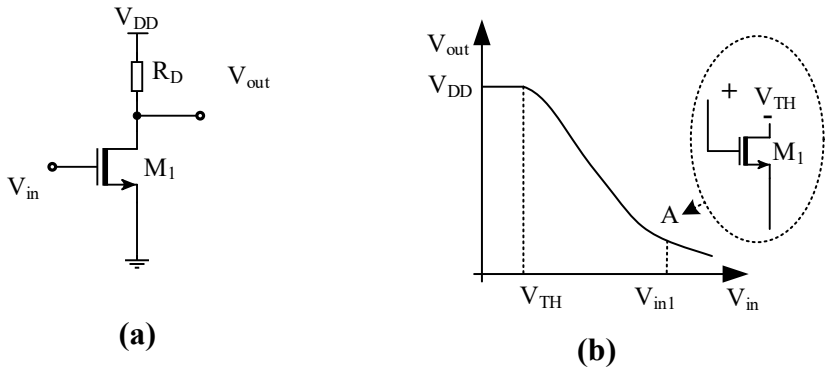

Figure 6: (a) Common-source stage (b) I/O characteristic

When input voltage goes high, M1 stays off and Vout = VDD [Fig 3.3 (b) page 49]. As Vin reaches Vth, M1 turns on and is in now in saturation region, we have [6]

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in-} V_{TH})^2 \quad (2.1)$$

Increase in Vin, Vout drops further, but the transistors still operates in saturation. When Vin exceeds Vout by Vth, at this point.

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in-} V_{TH})^2 \quad (2.2)$$

From above equations, Vout can be calculated. When Vin>Vin1, M1 is in triode:

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2 (V_{in-} V_{TH}) V_{out} - V_{out}^2] \quad (2.3)$$

We have an equation from small signal model

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} \quad (2.4)$$

$$= -g_m R_D \quad (2.5)$$

Which tells us about what will happen when a circuit experience large signal swing, If the gain changes significantly with the signal swing, then it will start operating in large signal mode. This

dependency of circuit gain on signal level goes towards nonlinearity, and that is undesirable outcome. To minimize the nonlinearity, magnitude of Av should be increased by increasing W/L, or decreasing Id in equation given below [6].

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} \frac{V_{RD}}{\sqrt{I_D}}} \tag{2.6}$$

Increasing $\frac{W}{L}$ or V_{RD} or decreasing I_D, magnitude of A_v can be increased, if other parameters are constant. The circuit needs trade-offs between some of its parameters, such as voltage swings, bandwidth and gain. Above that, low supple voltage makes further tightening in trade-off [6].

2.4 CS Stage with Diode-Connected Load

When gate and drain of MOSFET are shorted, it operate as small signal resistor as in Figure6 (a) and (b) given below [6].

Figure 7: (a) Diode-connected NMOS (b) Diode-connected PMOS

This configuration shows a small signal performance similar to two terminal resistors, the transistor is in saturation all the time as the drain and gate have the identical potential.

2.5 CS Stage with Inductive Load

As CS stage with resistive load does not provide good matching, and also the output node time constant may constrain working at higher frequencies. To avoid the trade-off between the supply voltage and voltage gain, and also to operate at higher frequency, common source stage can integrate and inductive load. This topology works with low supply voltages, as the inductor preserve a smaller dc voltage drop in comparison with resistor. Also, inductor resonates with the capacitance at the output node, and allowing higher operating frequency than the resistive-load [13].

It also provide possibility to get Re{Zin} = 50 Ω at the frequency of interest, but the negative capacitance in fig 5.11 (b) [13] increasing the negative input resistance at other frequencies, which

may possibly cause instability. The effect of feedback capacitance can be neutralized for some frequencies by using parallel resonance [13]. Since feedback capacitance (Cf) is small in relation, feedback inductor (Lf) must assume a higher value, and hence introducing noticeable parasitic capacitances at the input and output and in result lowering the performance. That is why this topology is not very popular in modern RF design [13].

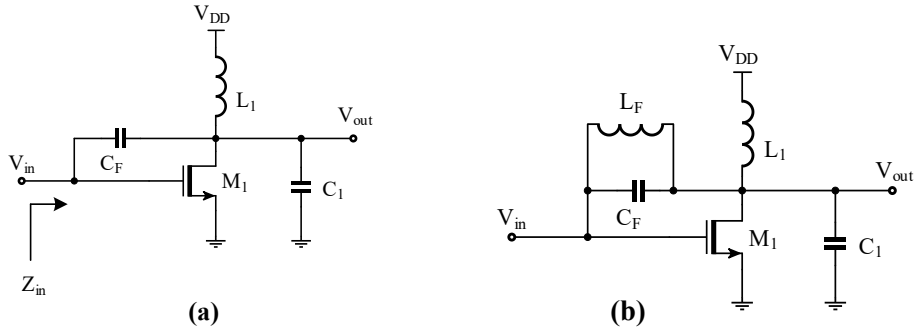

Figure 8: Input impedance in presence of C_F, (b) Neutralization of C_F by L_F

2.6 Source Follower

If an amplifier has to achieve high voltage gain using limited supply voltage, the load impedance must have to be as large as possible. But if this amplifier stage has to drive a low impedance load, then a buffer stage must have to be used after the amplifier to drive that low impedance load without losing the signal level. Source follower, also known as common drain stage, can act as voltage buffer. Figure9 (a) shows the source follower receive the signal at gate and drives the load at source, and letting source to "follow" gate voltage [6].

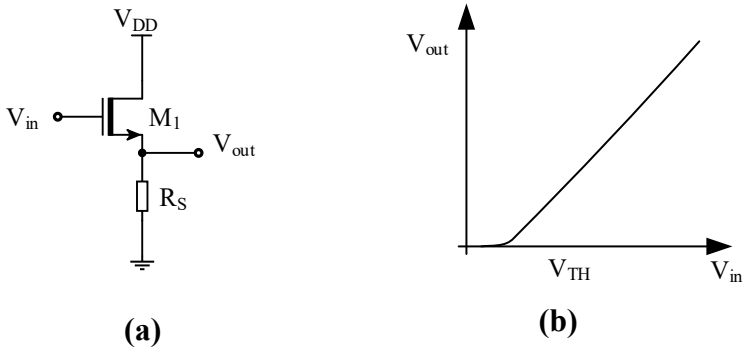

Figure 9: (a) Source follower (b) its I/O characteristic

High input impedance and moderate output impedance are the properties of source follower, but by having two undesirable properties: voltage headroom limitation and nonlinearity. Voltage headroom limitation is because of shifting the dc level of signal V_{gs}, and hence consuming voltage

headroom and confining the voltage swing. Nonlinearity drawback at input-output occurs, even if source follower is biased by ideal current source, because of the nonlinear reliance of V_{th} on the source potential.

In source follower, as the drain is connected to the power supply or bypassed to ground, no AC signal present there. At the source, it has full negative feedback, the whole device gain is moving to make the output equal to input. Source follower is the most predictable and stable with high input impedance. Its output impedance is low, and is a very good setup for the unity gain buffer.

2.7 Common Gate Stage

An important property, which makes common-gate an interesting option for LNA designer, is its low input impedance [13]. In common-gate topology, the input signal is applied to the source terminal, a capacitive coupling common gate LNA is shown in figure10**.** The LNA shown below sense the input at source terminal and gives output at drain [6].

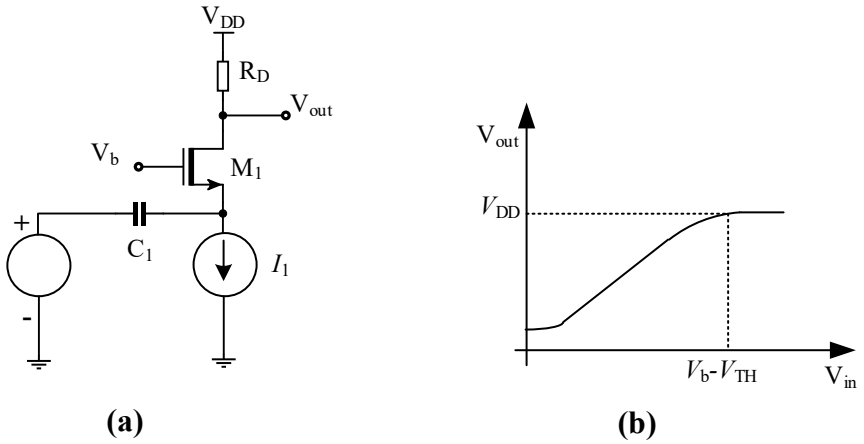

Figure 10: (a) Common-gate stage with capacitive coupling, (b) CG input-output characteristic

For large signal analysis, when M1 is in saturation, the output voltage is expressed as

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{b-}V_{in} - V_{TH})^2 R_D \tag{2.7}$$

For small signal gain,

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right)R_D \tag{2.8}$$

As $\partial V_{TH}/\partial V_{in} = \partial V_{TH}/\partial V_{SB} = \eta$, we get

$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta) \tag{2.9}$$

$$= g_m(1+\eta)R_D \tag{2.10}$$

The input impedance of common-gate is important too. The body effect increases the corresponding transconductance of the stage. And it also decreases input impedance of CG stage. The comparably lower input impedance of CG stage becomes advantageous in some applications.

In submicron CMOS technology the channel length modulation has compelling influence over common gate stage. Input impedance of common gate is very low when channel length modulation is ignored and very high when they are taken in consideration. Many techniques are used to deal with low input impedance problem, with current technology the problem is high input impedance. To solve this problem, transistor channel length can be increased, hence reducing channel length modulation and increasing the obtainable $g_m r_O$. As device width also increases correspondingly to keep the transconductance value, gate to source capacitance also increases well enough, hence input return loss is degraded [13].

From the figure 11(a) below, the drain-source current of M_1 equals $-g_m V_X$ when body effect is not considered. Positive feedback through r_O increases the input impedance, as shown in the figure below 11 (a). Current going through r_O is given as, $I_X - g_m V_X$, and resulting a $r_O(I_X - g_m V_X)$ voltage drop across it. The current $I_X$also pass through the output tank and giving voltage $I_X R_1$ at resonance frequency. By combining both of them voltage drop at r_O and $I_X R_1$, we get

$$V_X = r_O(I_X - g_m V_X) + I_X R_1 \tag{2.11}$$

Which is,

$$\frac{V_X}{I_X} = \frac{R_1 + r_O}{1 + g_m r_O} \tag{2.12}$$

If $g_m r_O \gg 1$, it tells that the drain impedance is divided by $g_m r_O$ when seen at the source. Because of the low intrinsic gain, it is specifically important in short-channel devices.

For output impedance of common-gate, the equation and circuit (figure 11 (b)) is given as,

$$R_{out} = \{[1 + g_m r_O]R_S + r_O\} || R_D \tag{2.14}$$

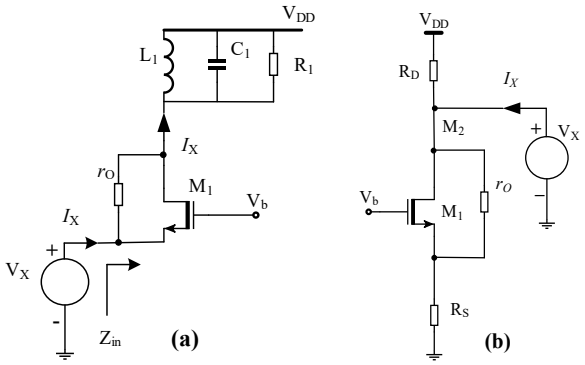

Figure 11: (a) Input Impedance of common-gate stage in considering r_O (b) Calculation of output resistance of common-gate stage

2.7.1 Noise in CG Stage

MOS transistors create mainly two different types of noises, thermal and flicker noise. Thermal noise majorly is produced in the channel and ohmic sections of MOS. It is generated by the gate resistance, and the gate resistance is dependent on geometry of MOS. During operating in saturation, the long channel MOS devices noise can represented by modelling it by current source connected between drain and source terminals figure12. Thermal noise produced in channel can be controlled by the transconductance of the device. It can be done by reducing the effect of gate resistance through proper layout or for example mutli-finger gate design. Flicker noise on other hand is the noise generated by the interface between gate oxide and silicon substrate. It is difficult to predict flicker noise as compare to thermal noise.

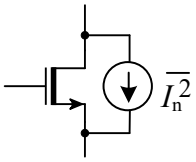

Figure 12: Thermal noise of MOSFET

Here, $\overline{I_n^2} = 4kT\gamma g_m$

Common gate configuration is given in figure13 (a) and its thermal noise model is given in figure13 (b). Thermal noise of R_D and M_1 is represented by current sources, channel length modulation is neglected. To calculate input referred noise voltage and noise current, we have noise models in figure14 (a) and (c), and figure14 (b) and (d) shows the configurations respectively. For input referred noise voltage the input is short to ground, and for input referred current noise the input is left open. Increasing transconductance helps in reducing the input referred noise voltage. For the input noise voltage we have equation 2.16 [6].

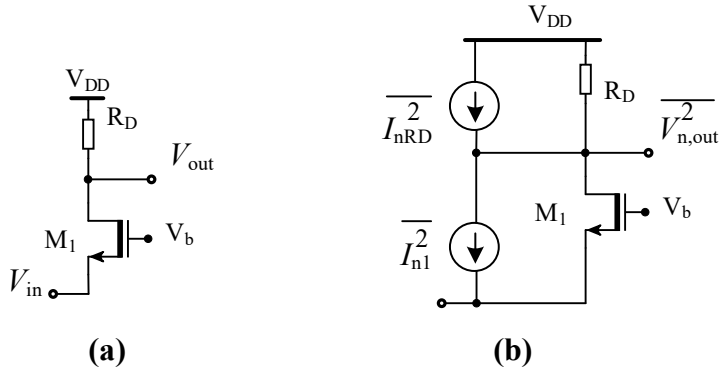

Figure 13: (a) Common Gate Stage (b) Circuit with noise sources included

$$\left(4kT\frac{2}{3}g_m + \frac{4kT}{R_D}\right)R_D^2 = \overline{V_{n,in}^2}(g_m + g_{mb})^2 R_D^2 \qquad (2.15)$$

$$\overline{V_{n,in}^2} = \frac{4kT(2gm/3+ 1/R_D)}{(g_m+ g_{mb})^2} \tag{2.16}$$

After equating the output noise of circuit in figure 14 (c) and (d), results in the input referred noise current. If summation of currents I_{n1} and I_{D1}equals zero at the source of M_1, then as a result I_{n1} create equal and opposite current in M_1, resulting in no noise at output. The output noise voltage become equal to $4kTR_D$, which becomes:

$$\overline{I_{n,in}^2}R_D^2 = 4kTR_D \tag{2.17}$$

$$\overline{I_{n,in}^2} = \frac{4kT}{R_D} \tag{2.18}$$

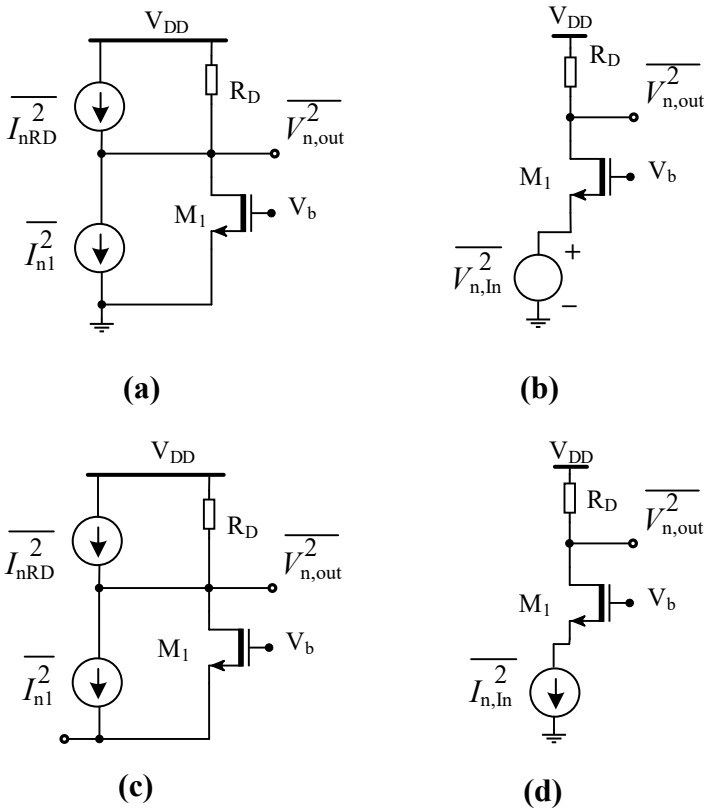

Figure 14: Input-referred noise calculation of Common Gate stage

Common gate topologies suffers from the noise current generated by referring the load to the input, this drawback comes in because these circuits does not provide any current gain. Beside thermal noise, it is important to consider flicker noise $(1/f)$ to get overall noise per unit bandwidth. Flicker noise values varies a lot depending on the oxide-silicon among different CMOS technology (eq 2.19). For convenience, it can be roughly taken into account as voltage source in series with gate. Below given equation (2.19) also tells about the minimizing of flicker noise, which is to increase WL (device area). K is process dependent constant, on the order of $10^{-25}V^2F$, and C_{ox} is gate oxide capacitance per unit area [6].

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.19}$$

2.7.2 Cascode Stage

A cascade of common-source stage and common-gate stage is called cascode topology. It provide several useful properties. Figure15 given below shows basic schematic, M1 generating small signal drain current equal to Vin. M2 providing route the current towards Rd. The gate of M2 is retained at fixed DC voltage, to keep both the transistors in saturation for all the time, and M2 act as CG amplifier [6].

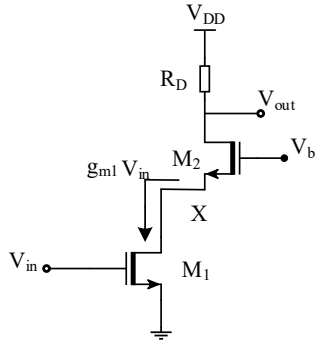

Figure 15: Cascode stage

One of the important properties of cascode topology is its high output impedance, and to find out Rout, the circuit should be viewed as CS stage with degeneration resistor equals r_{o1}.

$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1} + r_{o2} \tag{2.20}$$

If $g_m r_o \gg 1$, we get $R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$.

M1 output impedance increased by M2, by factor $(g_{m2} + g_{mb2})r_{o2}$. High output impedance can be achieved by increasing cascading more devices, but as the required extra added voltage headroom make it less desirable configuration.

Voltage gain can be written as $G_m R_{out}$, hence G_m is usually driven by transconductance of transistor. So the figure12 have to make tradeoff between device capacitances and bias current, and to increase voltage gain, its desirable by maximizing Rout.

2.7.3 Folded Cascode

Cascode structure main usage is to convert input voltage to current and apply that to a CG stage, but both, input and cascode device should of different type, as shown in figure 16(a). The figures16 (b) and 16(c) are called folded cascode, because small signal current is folded up (fig16b) or down (fig16c). For comparable performance, the bias current in these cases must be higher than in

figure15. For achieving higher voltage gain, the load of folded cascode can be used as cascode by itself.

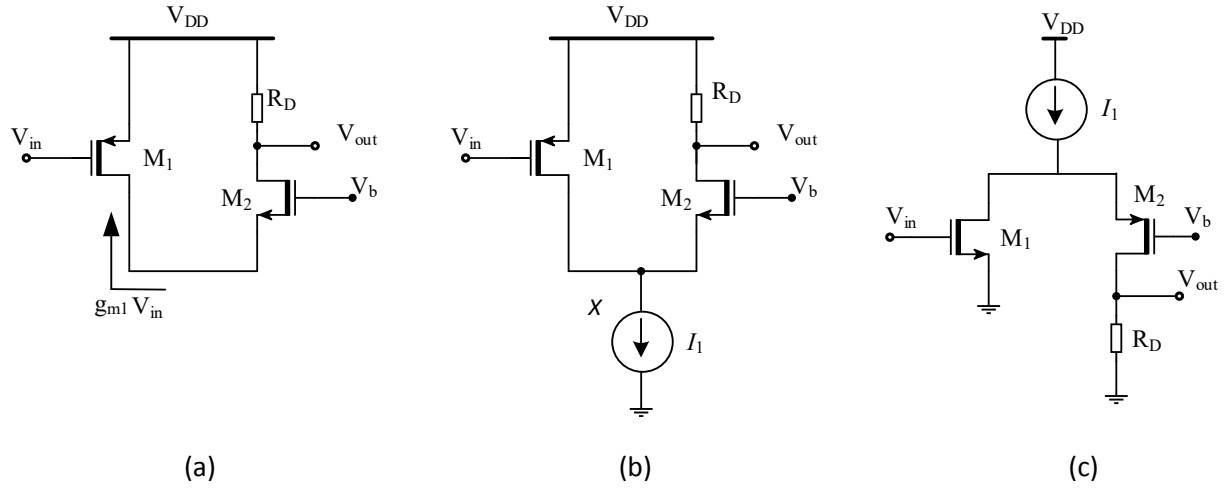

Figure 16: (a) Simple folded cascode, (b) folded cascode with proper biasing, (c) folded cascode with NMOS input.

2.8 Current Mirror

Current mirror is usually used in amplifier stages for bias currents and active loads. The simple work principle of current mirror is a basic relationship between two same size transistors, having equal V_{GS} for MOS and V_{BE} for a BJT and same drain current or collector current respectively, at the same temperature. It is a circuit block that is responsible to copy the current flowing out or into, of an input terminal, by replicating output terminal current. Due to its relative high output resistance, the output current stays constant, regardless of loading. Other characteristic of current mirror is its lower input resistance, that keeps helps in keeping constant input current regardless of drive conditions.

Figure 17 shows the simple n-channel current mirror. Current i_{in} is supposed to be characterized by current source and i_{out} is output current or mirrored current. As $V_{DS1} = V_{GS2}$, transistor $M_1$is in saturation. If it is assumed that $v_{DS2} \geq v_{GS2} - V_{T2}$, this let us use the equation in saturation region of MOS. Further, as the current mirror components are processed in same integrated circuit, so all the physical parameters like K' and V_T are equal for both devices. In this scenario, we get the general ratio of i_{out} to i_{in} is

$$\frac{i_{out}}{i_{in}} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right) \tag{2.21}$$

Assuming, $v_{DS2} = v_{DS1}$, the ratio i_{out}/i_{in} becomes more simplified (ideal situation). As a result, i_{out}/i_{in} is function of aspect ratios, which a designer can control.

$$\frac{i_{out}}{i_{in}} = \left(\frac{L_1 W_2}{W_1 L_2}\right) \tag{2.22}$$

Three effects makes current mirror different from ideal situation of above given equation. They are, channel length modulation, non-perfect geometrical matching and the threshold offset between two transistors [22].

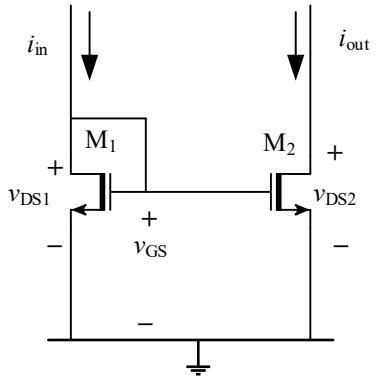

Figure 17: n-channel current mirror

3. SCALED DOWN (7GHz to 5MHz) IN FREQUENCY BJT LNA DESIGN

3.1 Introduction

Research purpose was to design a common base (CB) bipolar junction transistor (BJT) low noise amplifier (LNA) in OrCAD Capture CIS Lite for a target frequency of 5MHz and then modify the printed circuit board (PCB) LNA with exactly same values of components and parameters, to the same operating frequency as was in PSpice designed LNA and compare both results.

The existing PCB LNA, schematic figure18 given below, is consisted of three inductors slots, which are mainly responsible for frequency selections. Variable capacitors were used for fine-tuning in frequency selection. Jumpers were used accordingly to get specific desired parameters results, there functionality can be understood from Table2.

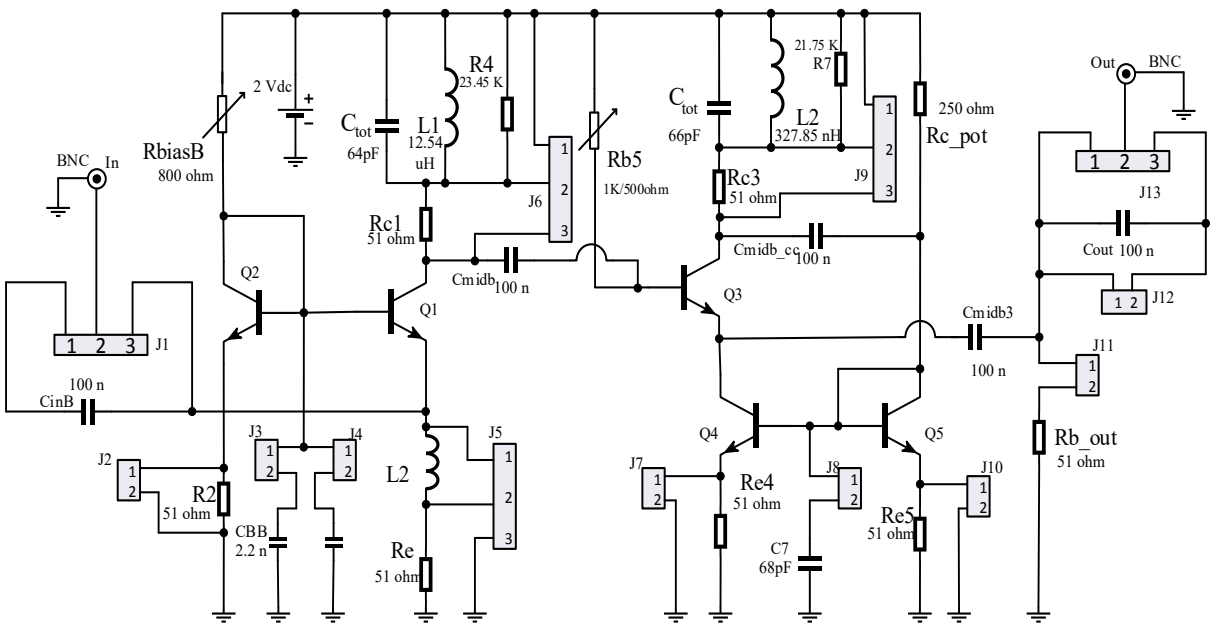

Figure 18: Schematic of PCB LNA with jumpers

Table 2: Different components connections depending on jumpers positions

Jumper	Position	Connection
J1	1-2	CinB – OFF
J2	Open	R2 –ON
J3	Close	C2 -ON
J4	Open	C4 – OFF
J5	1-2	L2 Short
J6	2-3	Rc1 Short
J7	Close	Re4 Short
J8	Close	C7 Short
J9	2 – 3	Rc3 – Short
J10	Close	Re5 Short
J11	Open	Rb_out OFF
J12	Close	Cout – Short
J13	2 – 3	Output White's Casecode

3.2 Pspice version LNA

Common base LNA, schematic shown in Figure 19 below, was designed in OrCAD Capture CIS Lite with the exactly same values as they are modified within PCB LNA. This LNA was divided mainly in two different blocks, the common base block with LC tank and white's cascade.

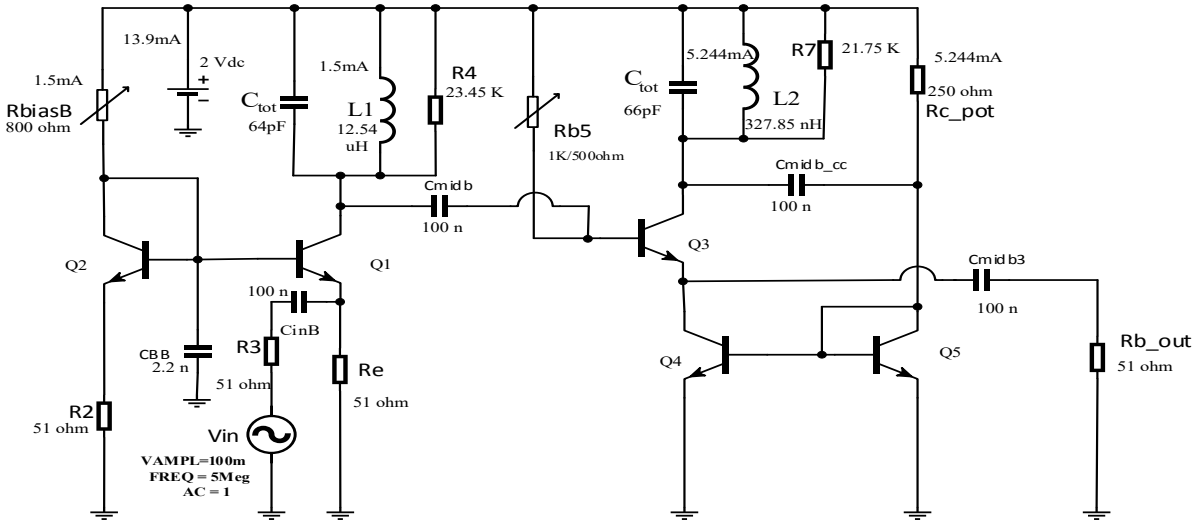

Figure 19: Modified and simplified schematic of LNA

3.3 Bandwidth and Selectivity of Tuned Circuit

Parallel tuning circuit has been used in BJT LNA, and some brief work principle of this tuning circuit will be explained here. At resonance, parallel tank has maximum impedance and minimum current, and hence the applied voltage to output will be maximum at this resonance frequency. For all other frequencies around the resonance, the impedance goes down and therefore the applied voltage to output also goes down.

The Bandwidth (BW) is a range of frequencies that passes to the output with 50% (or greater) power level. Those frequencies above 50% power level corresponds to 70.7% on the impedance axis of frequency response curve. The reason which make bandwidth a significant property is, that it defines the selectivity of tuned circuit and selectivity of RF amplifier. Selectivity is the capability of circuit to select the desired signal and reject unwanted signal [23].

Selectivity and Bandwidth are inversely proportional characteristics of parallel LC tank circuit, a circuit with small bandwidth is good in selectivity and vice versa.

$$\text{Selectivity} \propto 1 / \text{Bandwidth} \tag{3.1}$$

Both selectivity and bandwidth, are mostly determined by Q of the circuit.

$$\text{Bandwidth} = \frac{f_R}{Q} \tag{3.2}$$

The Q factor shows the quality of parallel tank circuit, and is ratio between reactance to resistance of tuned circuit.

$$\text{Q} = \frac{X}{R} \tag{3.3}$$

Or otherwise, can be written as

$$\text{Q} = \frac{X_L}{R_W} \tag{3.4}$$

X_L = Coil's reactance at resonance

R_W = Resistance of winding

The bandwidth and selectivity of tuned circuit can hence be controlled by increasing or decreasing the resistance of tuned circuit [23]. In this research work, to analyze the bandwidth we can use the

above given equations. Q factor plays an important role in bandwidth and selectivity. According to equation (3.2), higher Q factor value gives better selectivity and narrower bandwidth. Q factor value itself is dependent on resistance 'R', equation (3.3), higher resistance value means lower Q factor. So if 'R' value is increased, it decreases Q factor, which results in higher bandwidth.

3.4 Real coil model and LC tank

Capacitance and inductance determines the oscillation frequency, as both of them control the rate of change of energy back and forth within tank circuit [23]. In this research work, first of all, LC tank was tuned into desired oscillating frequency by finding right values of inductor L_1 and capacitor C_{tot}. Resonance frequency can be found by a formula given below, if any one of those component value is known [23].

$$F_r = \frac{1}{2\pi} \frac{1}{\sqrt{L_1 \times C_1}} \tag{3.5}$$

In this research, first selected inductor was analyzed to study its behavior outside circuit. Then LC tank circuit was analyzed for its oscillating frequency, separate circuit was designed to study what changes comes when inductor is compared with capacitor, as shown in figure20.

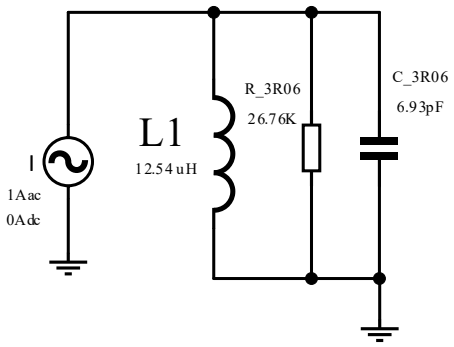

Figure 20: Real coil model with its capacitance and resistance values

Figure20 shows the real coil model with its resistance and capacitance values were considered same as they are given *'Inductors list'* available in the laboratory. Inductor of 12.54 uH was selected for the 5MHz frequency, and it has 26.76KΩ of resistance and 6.93pF of capacitance.

In inductor study, it was noticed that inductor with smaller value has higher resonance frequency. Figure21 shows that more inductance value is increased, the more resonance frequency comes towards the lower frequency side. In figure18 it can also be seen, that at resonance frequency the

inductor has the highest impedance value. Finally, after having results from different inductors, the inductor with closest to the target frequency was selected.

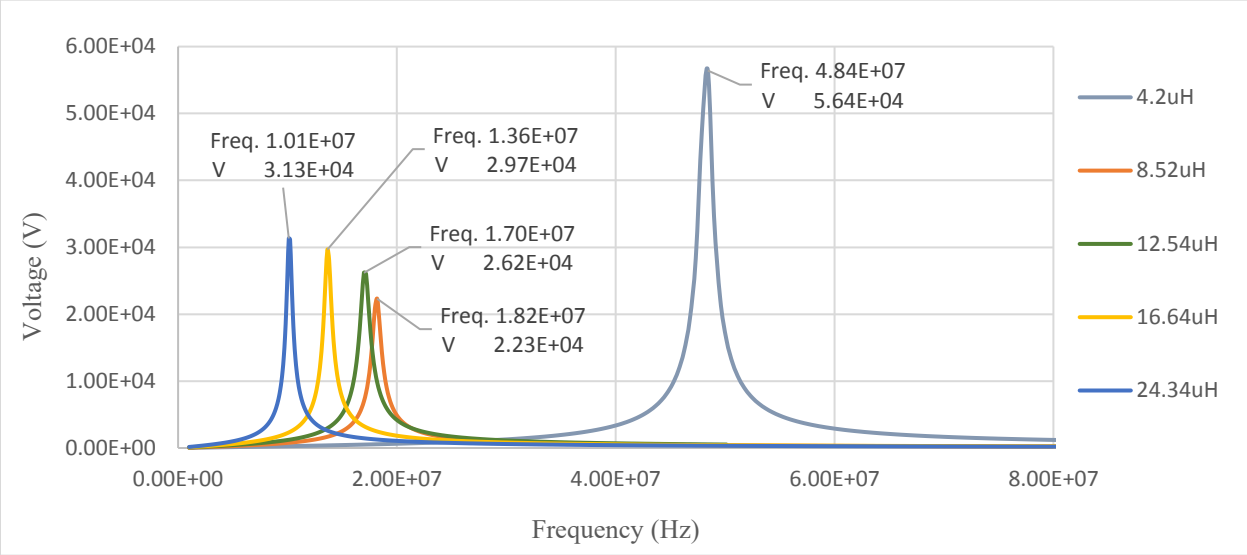

Figure 21: Real coil model results showing oscillating frequency of different values Inductors

Next step was to analyze the selected inductor within tank circuit with all resistances and capacitances given in the 'inductor list'. Same method was used, as it was in real coil model analysis to study frequency and gain response. Figure22 given below shows the schematic designed in PSpice.

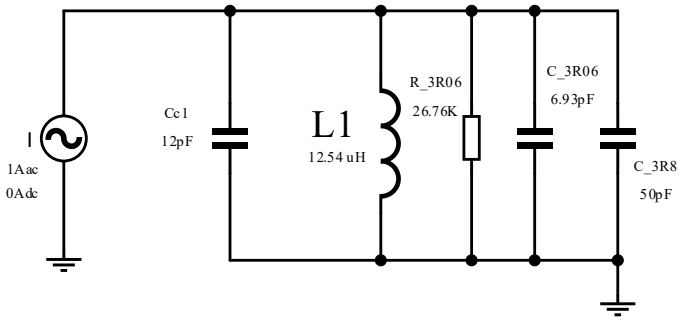

Figure 22: Coil model within tank circuit and series resistance R

Tank circuit was designed with all parameters same as they are in PCB LNA, 12pF of constant capacitance was considered with additional 50pF of variable capacitor was also added. Current source was used to study the behavior of tank circuit impedance.

Important thing to notice was that resonance frequency significantly comes down to 5.4 MHz, which is the same as it was calculated by using equation (3.5). By adding inductor and capacitor values, we get:

$$F_r = \frac{1}{2_{\pi}} \frac{1}{\sqrt{12.54uH \times 68.93nF}}$$

$$F_r = 5.4\ MHz$$

This equation gives us good comparison of the inductor and capacitor values selection for the target frequency, as we can see in the graph given below.

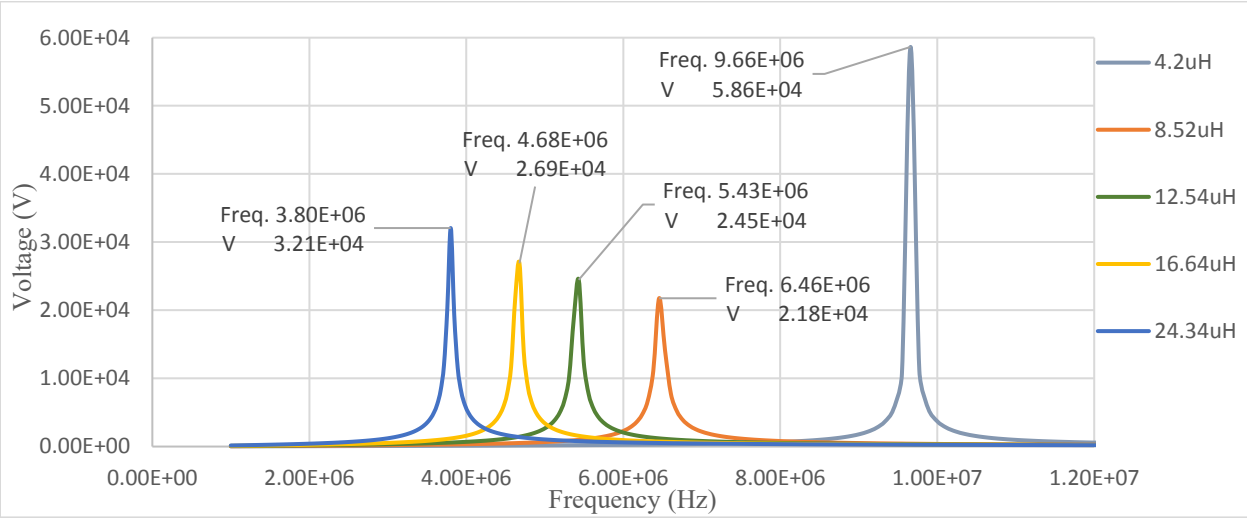

Figure 23: Showing effect of Cc1 and tuning capacitance on different values Inductors.

Inductor study was done to find the resonance frequency, which can be seen in figure21 and 23, showing high impedance at the resonance frequency. Other thing to notice is the effect of impedance on tank circuit, by changing capacitor values, we can tune the frequency accordingly. For example, in figure21 it can be noticed that the resonance frequency for 12.54uH inductor is at 17MHz. After including the capacitances, the frequency comes down to the 5.4MHz, it can be seen in figure 23.

Figure24 shows a good comparison of real coil model and inductor within tank circuit. Clear resonance frequency shift can be seen in between both of these cases.

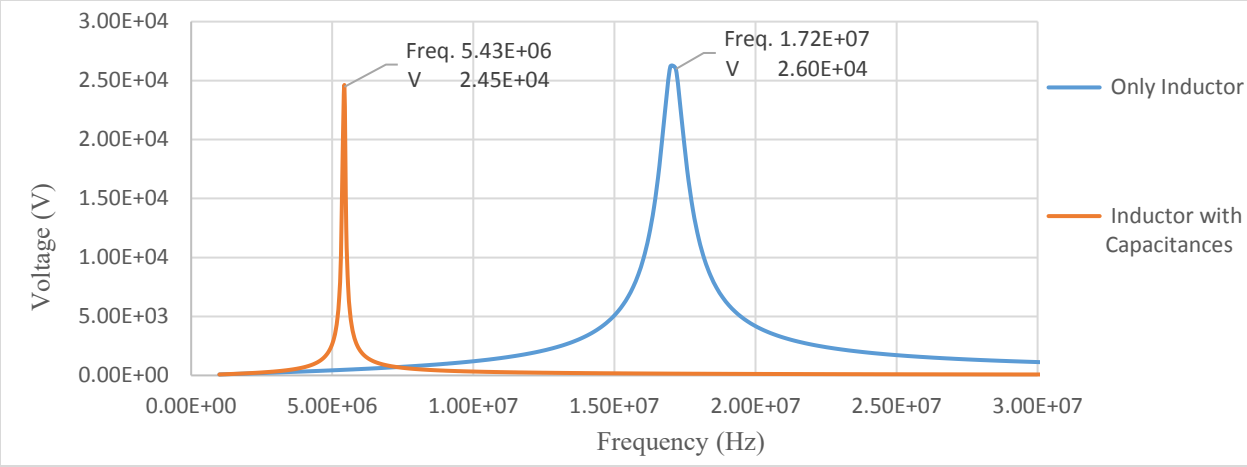

Figure 24: Comparison of Inductor measured within tank circuit and outside tank circuit separately, for the effect on center frequency.

3.5 Biasing and Common Base Stage

For the common base stage, the potentiometer RbiasB was set for a value of 800Ω, and 1.5mA current flows through it and transistor Q2 is used as diode, which controls biasing voltage of Q1. Next stage is common-base amplifier, whose output impedance is higher, and hence white's casecode buffer is used to bring down the output impedance of the whole LNA. Current mirror was used within white's cascade stage where transistor Q5 and Q4 are connected together working as current mirror, and hence setting a reference current.

Inductor with closest resonance frequency to the target frequency was selected. In figure25, it can be seen that its resonance frequency is now at 5MHz, which was desired frequency. It was due to the fact that the whole LNA circuit adding up further resistance and capacitance when inductor was used within the LNA circuit.

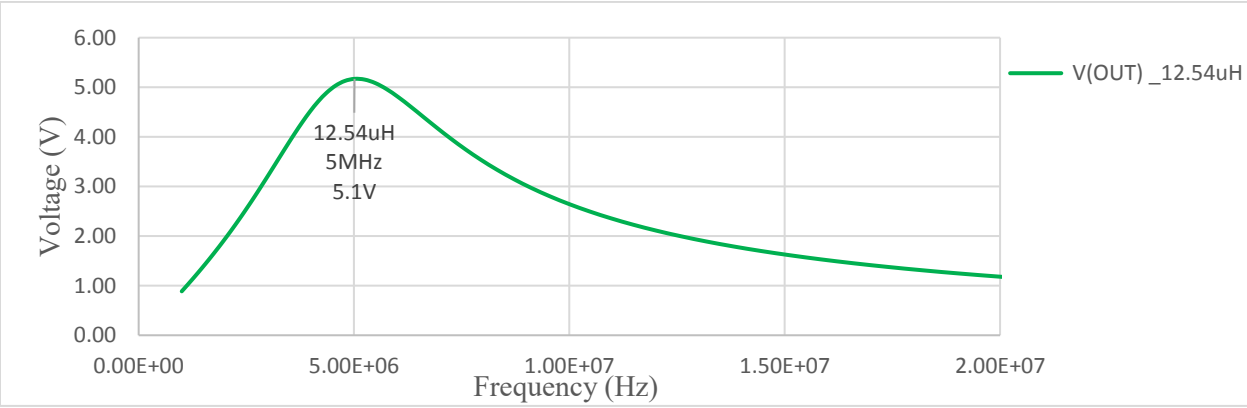

Figure 25: Inductor (L2) with 12.54uH value within LNA circuit

Table3 showing the inductors used in schematic with capacitance and resistances, with detail information according to the "List of ***HWD Ltd. PCB Inductors***" (see Appendix A).

Table 3: List of inductors used for measurements

No	L_p nH	R_p kΩ	C_p pF
24	4200	59.07	2.59
32	8520	22.50	9.03
35	12540	26.76	6.93
37	16640	29.85	8.13
40	24340	32.10	10.06

Common base topology has low input impedance and higher output impedance [24]. To tackle this issue while using this topology in our LNA, White's stage has been used to lower down the output impedance, as White's cascode has high input impedance and low output impedance [25]. Current mirror transistors M4 and M5 brings stable current reference point. Current mirror's reference current can be controlled through Rc_pot, and feedback capacitor Cmidb_cc brought linearity to the output.

The output voltage from common base is attenuated at buffer stage, as it has been shown in figure26. The common base output voltage is slightly higher than the whole LNA output voltage, which is taken after buffer stage. This occur because the output voltage gain of White's cascode is less than unity.

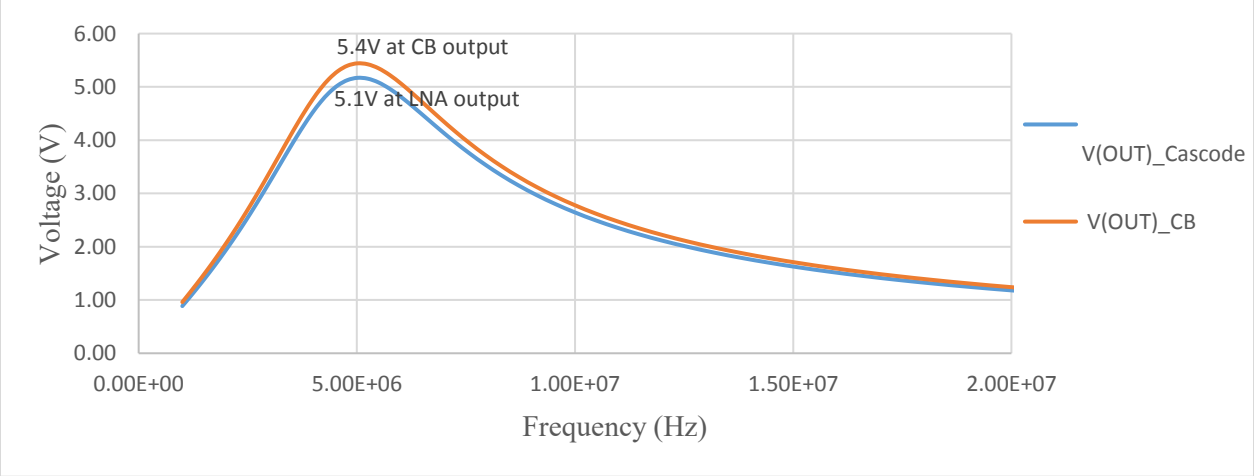

Figure 26: Attenuation effect of emitter follower on the common base output signal

3.6 Effect of different Rb5 values on Gain and Linearity

Higher value of Rb5 yields into higher voltage at base of transistor Q3, which in turn gives higher voltage at emitter, from where the output is taken. And for the lower value of Rb5, lower voltage at base terminal yields into lower voltage at emitter of Q3. Hence from Figure27 below we can see the difference in output voltage for both the values of Rb5.

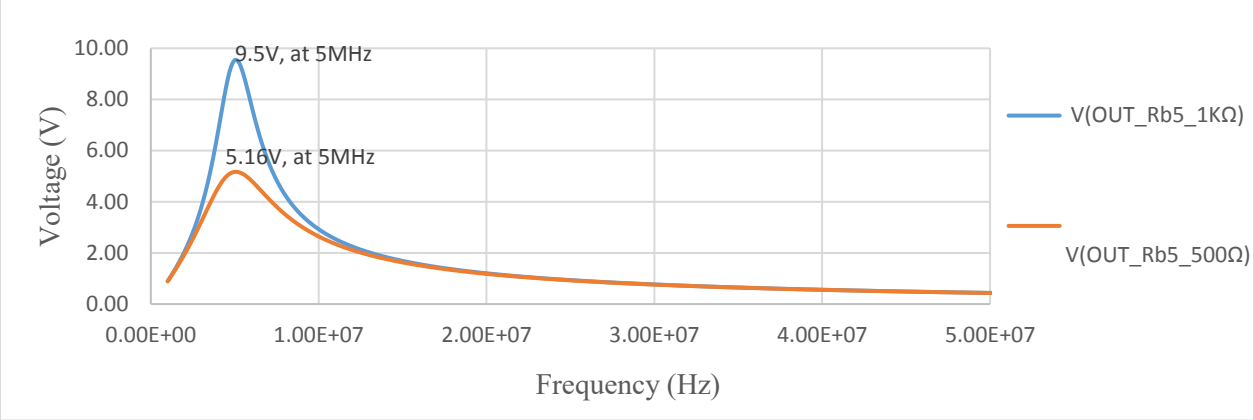

Figure 27: Effect of higher Rb5 resistance value on the output

Two separate values of Rb5 were used to understand its effect on the linearity. Figure28 shows that the higher value of 1KΩ resistor results into linearity for smaller range of inputs. For smaller values it is quite linear (from -30dBm till -22dBm), but as the input goes higher till -18dBm (79.6mV), the output gets distorted.

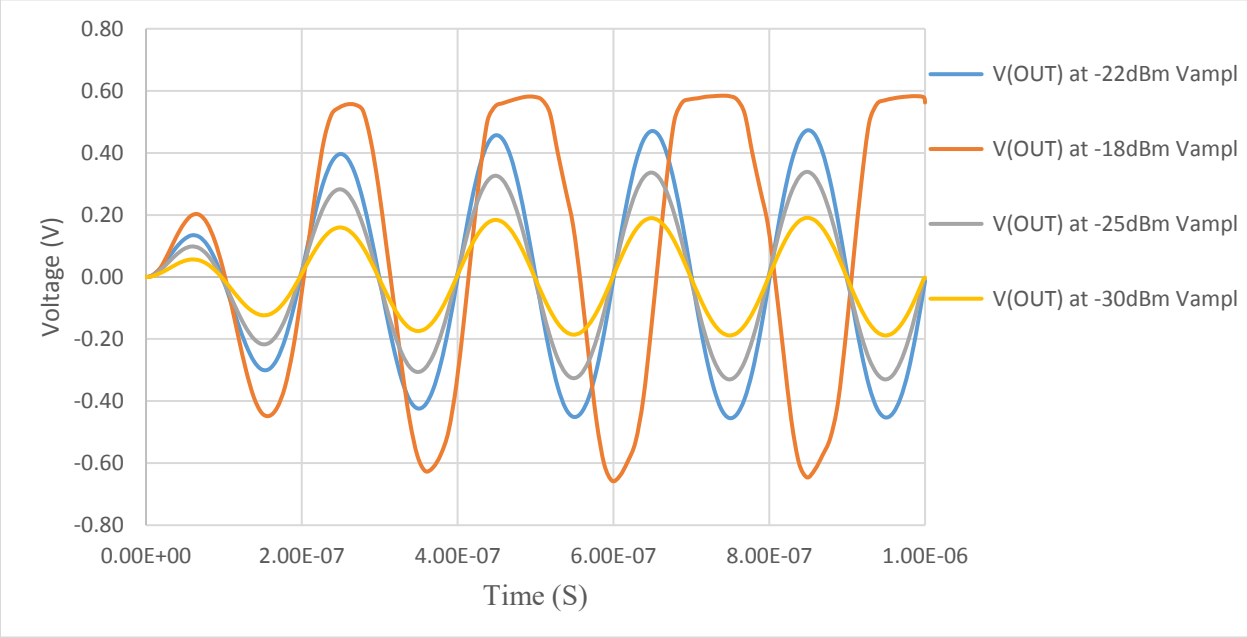

Figure 28: Effect of higher Rb5 value on the linearity of LNA output

Next, smaller Rb5 value was selected, and as from the figure29 we can see that LNA behave quite linear for the broader and higher input values (from -30dBm till -18dBm) as compare to the LNA with 1KΩ Rb5. The output gets distorted at -12dBm (158mV) for 500ΩRb5.

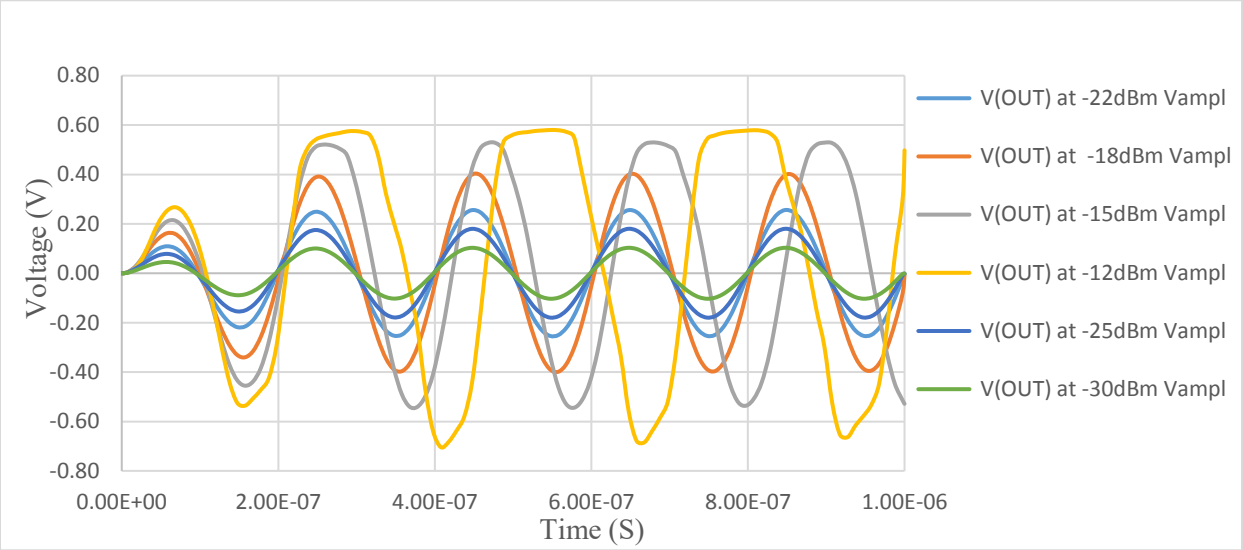

Figure 29: Effect of lower Rb5 value on the linearity of LNA output

3.7 Practical Measurements

Practical measurements were done to compare the results with simulator's results for linearity and gain, oscilloscope and spectrum analyzer were used. First of all PCB LNA was adjusted with different components, its values and jumpers. Inductor was available in lab (see Appendix A). For this LNA, inductor with new label 12R5 was used, which has parallel inductance value of 12.540uH, parallel resistance of 26.76K and parallel capacitance of 6.93pF. Jumper "J3" was connected to activate capacitor CBB 2.2nF. Jumper J5 was connected on pin 1 and 2 to bypass L2, and to make a path through resistor Re to the ground, with L2 circuit was consuming too much current out of battery source and it does not have significant effect. Jumper J9 was connected to bypass RC3, RC3 was bypassed because it was creating noise in the signal. Figure30 shows the practical measurement setup. LNA was consuming 12mA current from the power supply, with 2.78V applied voltage.

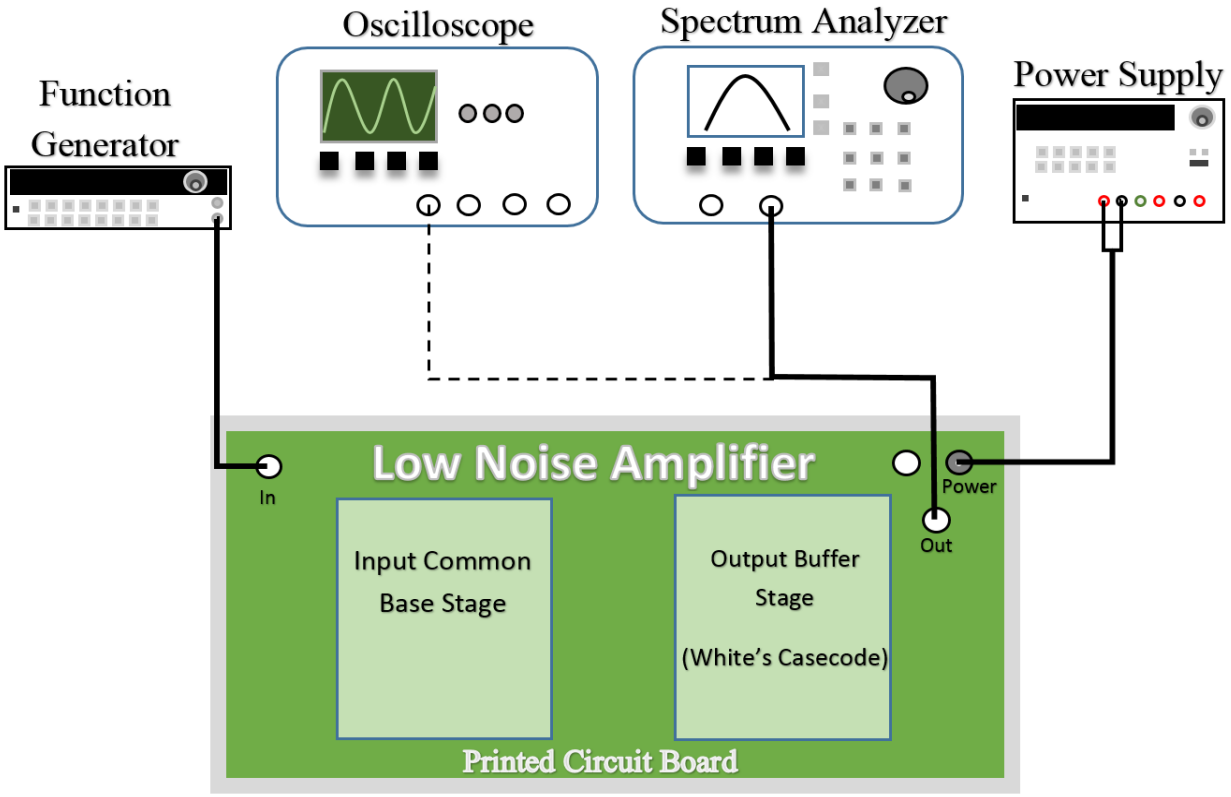

Figure 30: Practical measurement setup

3.8 Linearity and Gain

Measurements were done by modifying Rb5 with two different values, below results pictures tells us about the Rb5 effects on linearity and gain. These measurements also tells us about how gain and linearity are related to one another, and a tradeoff should be made between both of these properties according to the desired application.

The PCB LNA was first measured with RbiasB 500Ω, and applying -22dBm voltage. Stepwise it was measured for different input voltages, and the LNA was quite linear till -15dBm. At the higher input voltage -12dBm, the signal get distorted, but overall the LNA was quite linear for inputs from -22dBm till -15dBm. The overall gain of this LNA was ~20dB (Voltage gain). Results can be seen in figure31-35, for different values of input power values. Equation used for calculating gain was,

$$L_v = 20log_{10}\frac{V}{V_0}\,dB \qquad (3.6)$$

Vin = Input Voltage

V_o = Output Voltage (peak to peak)

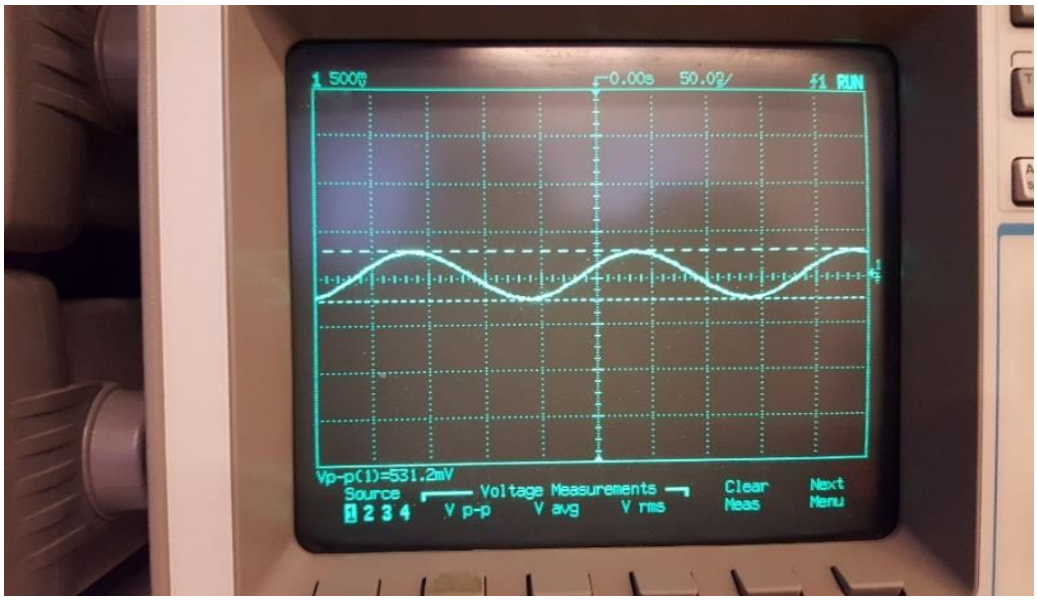

*Figure 31: BJT LNA Oscilloscope measurement for (**Vin** = 50.2mV (-22dBm), **V_o** = 531.3mV, **Gain** = 20.5dBm, **Freq.** = 5MHz)*

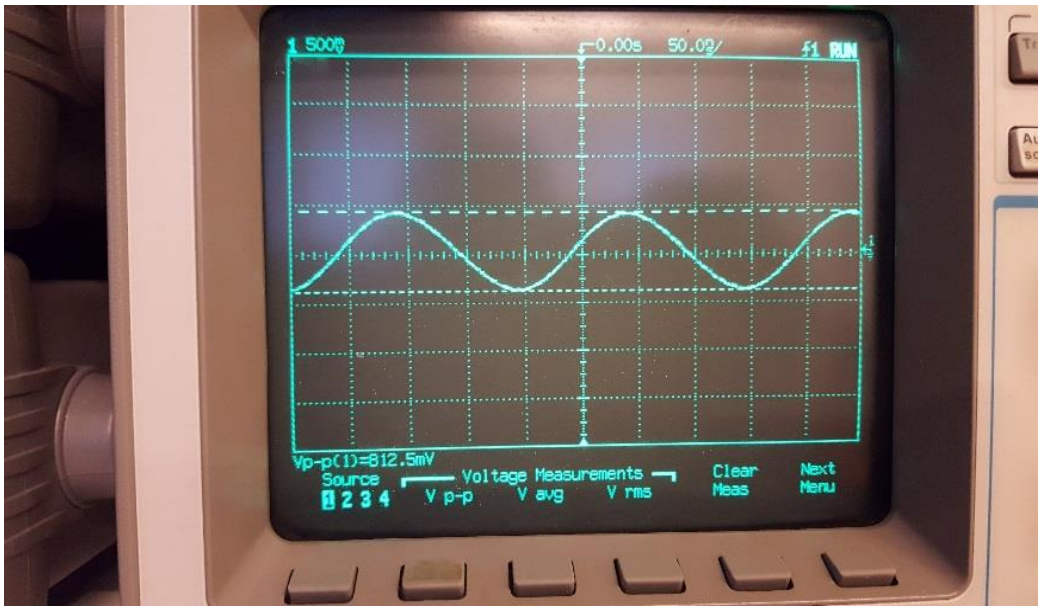

*Figure 32: BJT LNA Oscilloscope measurement for **Vin** = 79.6mV (-18dBm), **V_o** = 812.5 mV, **Gain** = 20.2dBm, **Freq.** = 5MHz*

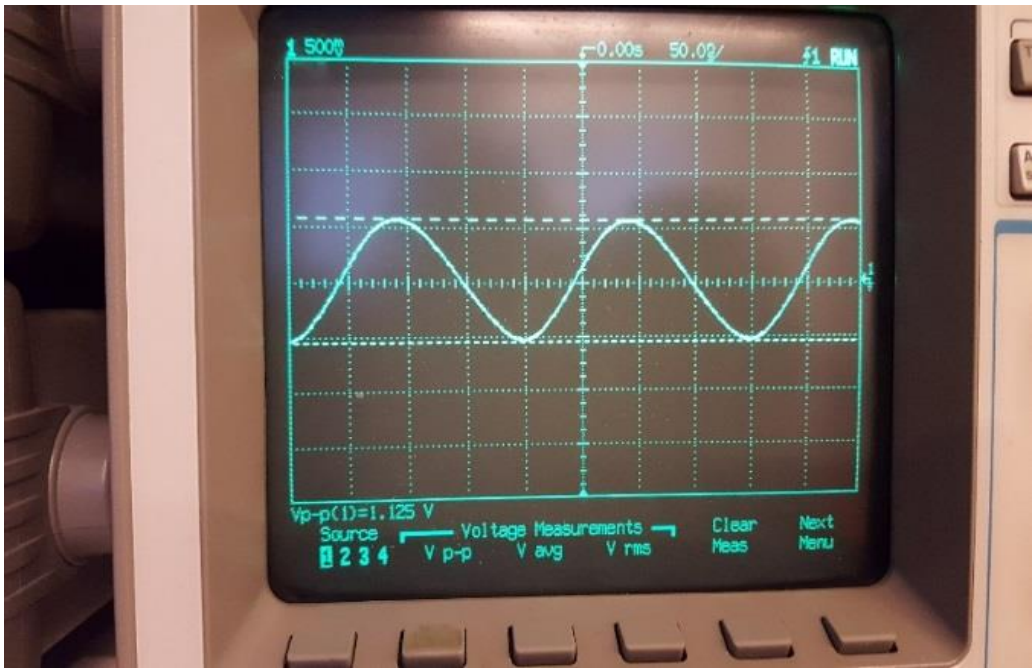

*Figure 33: BJT LNA Oscilloscope measurement for **Vin** = 112.45 mV (-15dBm), $\boldsymbol{V_o}$= 1.125 V, **Gain** = 20.0dBm, **Freq.** = 5MHz*

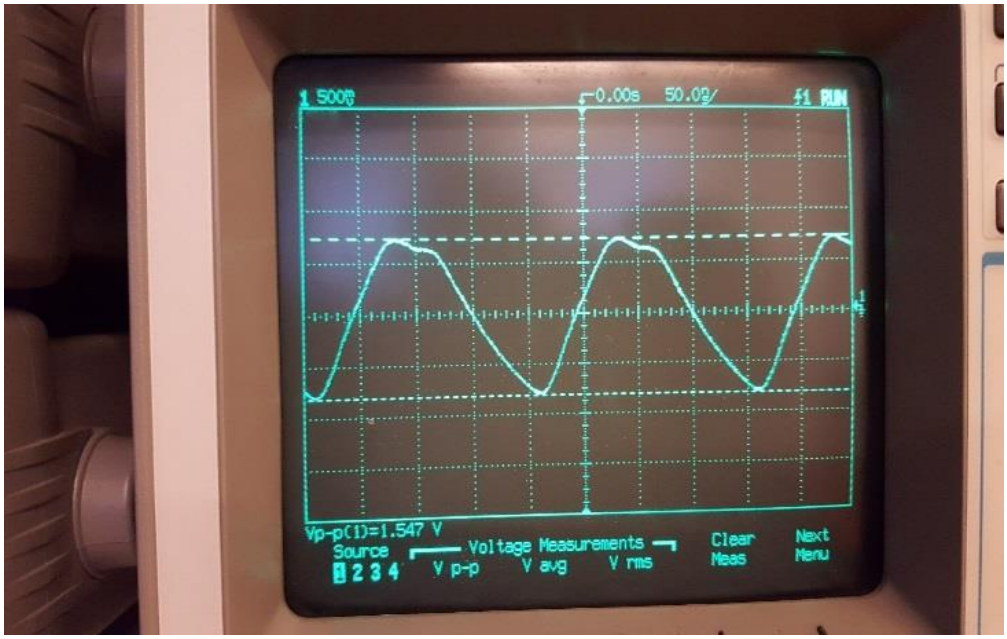

*Figure 34: BJT LNA Oscilloscope measurement for **Vin** = 158.8 mV (-12dBm), $\boldsymbol{V_o}$= 1.547 V, **Gain** = 19.7dBm, **Freq.** = 5MHz*

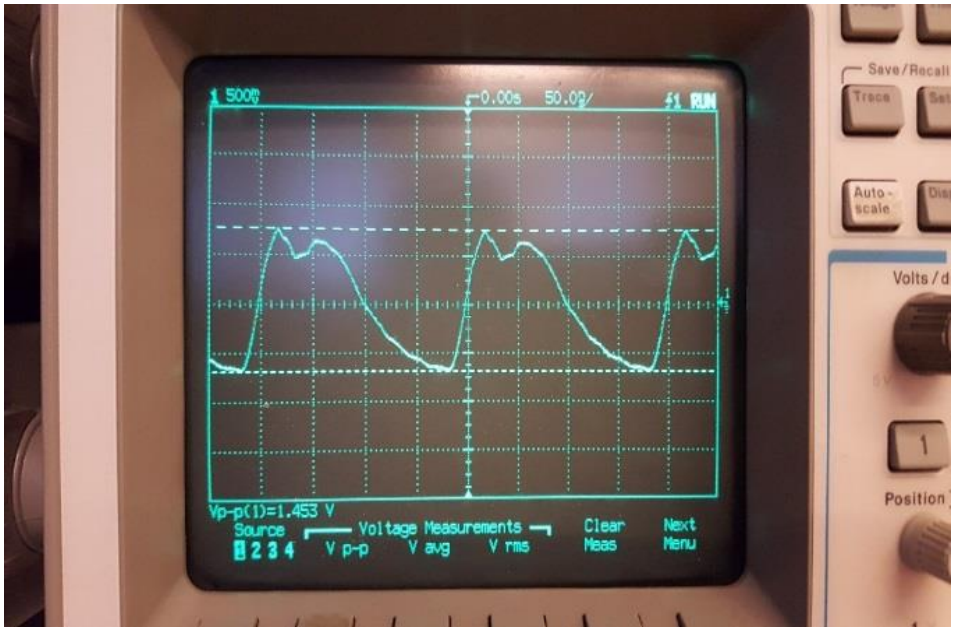

*Figure 35: BJT LNA Oscilloscope measurement for **Vin** = 199.97 mV (-10dBm), $\boldsymbol{V_o}$= 1.453 V, **Gain** = 17.2dBm, **Freq.** = 5MHz*

Next step was to check the effects of higher value of Rb5, and this time the resistance was increased for 1KΩ. The result was quite clear, it increased the gain, but the linearity range for input voltages get narrower. The LNA loses its linearity quite soon as the input voltage gets on the higher side, but the gain goes up to 24.84dB (voltage gain). Figure 36, 37 and 38 shows the measurement results from oscilloscope for different input power values.

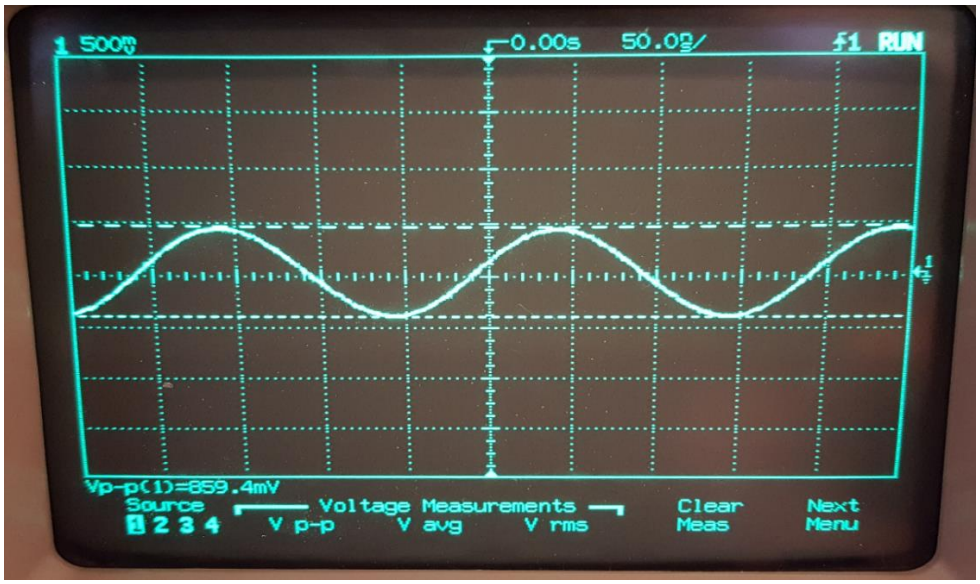

*Figure 36: BJT LNA Oscilloscope measurement for **Vin** = 50.2 mV (-22dBm), $\boldsymbol{V_o}$= 859.4 V, **Gain** = 24.6dBm, **Freq.** = 5MHz*

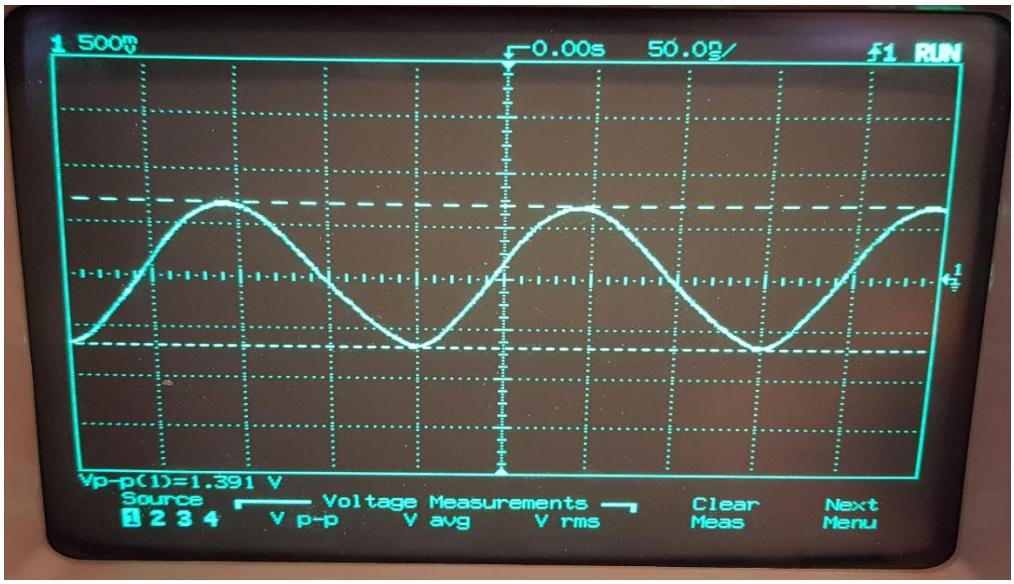

*Figure 37: BJT LNA Oscilloscope measurement for **Vin** = 79.6mV (-18dBm), V_o = 1.391 V, **Gain** = 24.8dBm, **Freq.** = 5MHz*

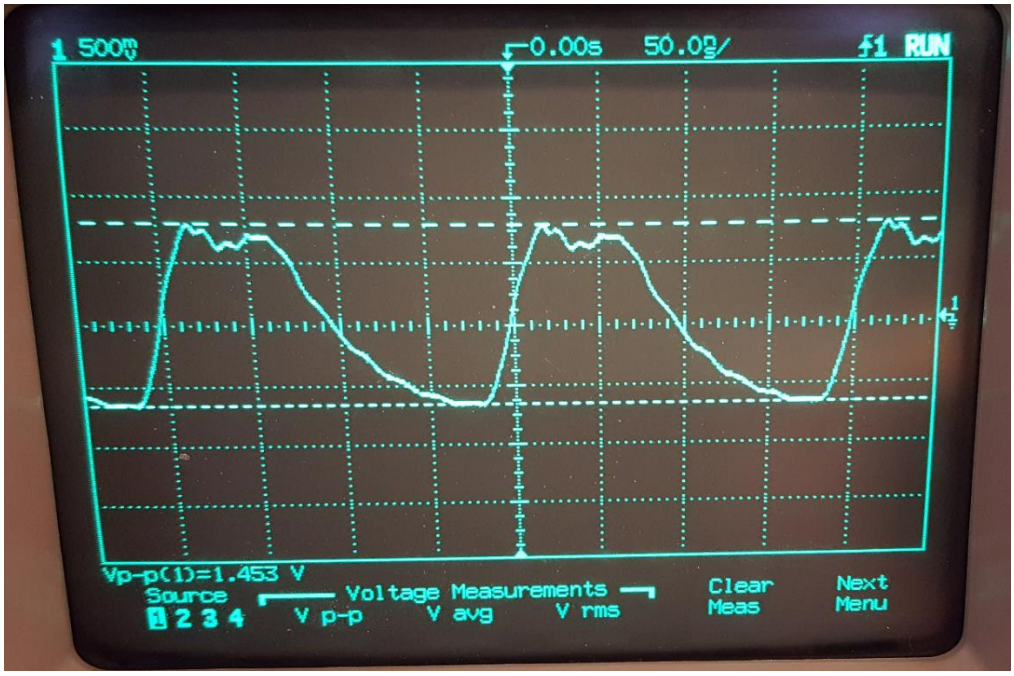

*Figure 38: BJT LNA Oscilloscope measurement for **Vin** = 112.45mV (-15dBm), V_o = 1.453 V, **Gain** = 22.2dBm, **Freq.** = 5MHz*

Furthermore, spectrum analyzer measurements were done to analyze the gain in frequency domain, and to see if the results are within the 5MHz target frequency. Figure39 shows the spectrum analyzer measurement result for the gain at 5MHz frequency with source amplitude of -30dBm.

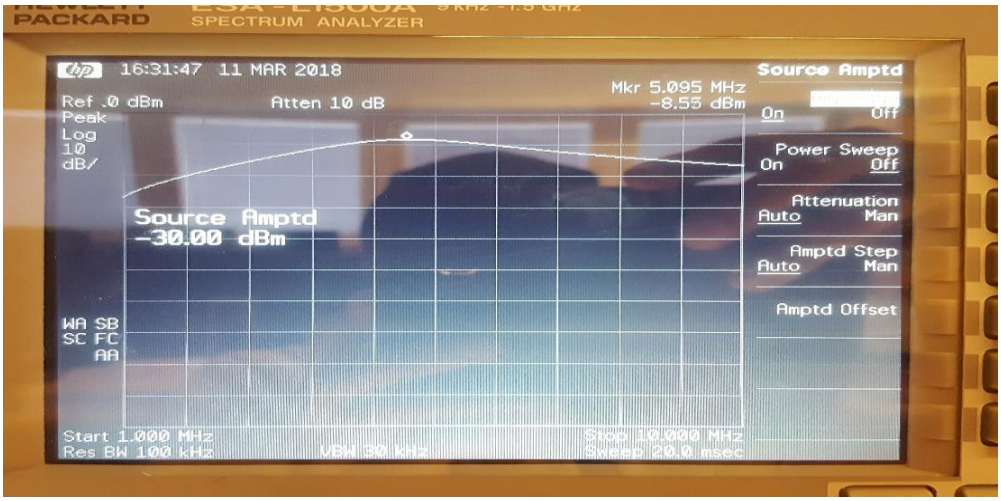

Figure 39: Spectrum Analyzer result for -30dBm Source Amplitude, ***Gain*** *= ~22dB, at* ***5MHz*** *Frequency*

3.9 Conclusion

This LNA study concludes that higher output impedance of common base topology can be minimized by proper selection of circuit, white's casecode in this case. By selecting proper inductor and capacitance values, oscillating frequency can be determined. Furthermore, the effect of different components over the linearity and gain, tradeoff can be done and a circuit can be designed according to the requirements. Higher gain can lead to linearity over narrower range of RF input signal, mostly linear on the lower side of the signal power (figure 36, 37 and 38). And to get a linearity over broader range (figure 31-35), a tradeoff should be made between linearity and gain. Biasing resistor Rb5 plays crucial role in determining either of the specification, higher Rb5 value yields a higher gain but lower linearity range and vice versa.

4. 7GHz CMOS LOW NOISE AMPLIFIER

Chapter three presents the schematic design explanation and results obtained from 7GHz CMOS LNA. It was designed in Cadence Virtuoso, 45nm CMOS Technology. The project target was to design a GHz range CMOS LNA with an upgraded higher range of operating frequency, using the same topology and technique as it was used in BJT MHz range LNA. For CMOS LNA common-gate topology was implemented to design the targeted operating frequency LNA and to achieve adequate important parametric results, such as low noise figure, higher gain, low power consumption, input output matching, stability etc.

4.1 Circuit Design

The power supply voltage was 1.1V and current consumption was kept as minimum as possible. Firstly, appropriate transistor, inductors and capacitors were selected for the common gate stage. Common gate stage was tuned to7GHz, a desired center frequency. It was followed by the White's cascode stage, which was designed to lower down the output impedance of common gate stage. Biasing stage independent of supply voltage was designed to set less sensitive or stable current reference point for the common base stage. Voltage supply and ground pad, Input output pads were designed and were taken into consideration. Below given figure40 is the schematic of 7GHz common gate LNA.

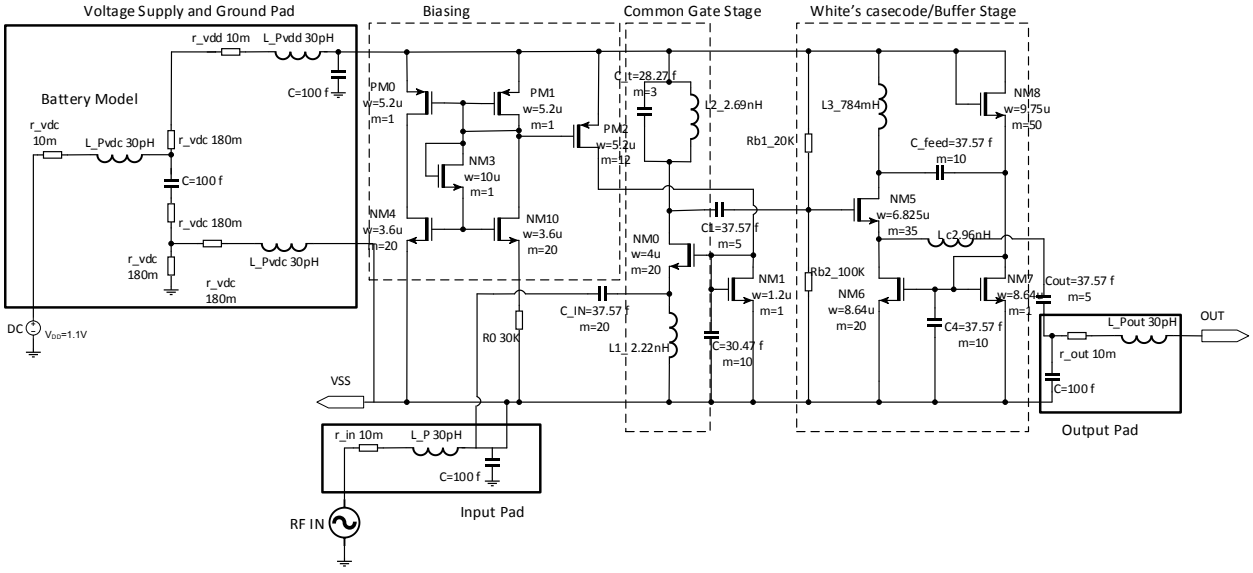

Figure 40: Schematic of 7GHz CMOS LNA

Inductors used in this LNA were designed to get the operating frequency with Q-factor above 8. Capacitors (mimcap) and transistors were taken from gpdk045 library. Below table 4 shows the designed inductor values and their Quality factor values.

Table 4: Inductor list with inductance and Q-factor values

Inductor name	InductanceValue	Quality_factor
L1	2.694nH	8.187
L2	2.221nH	8.927
L3	0.784nH	8.993
L4	2.963nH	8.279

4.2 Common Gate and LC tank

Common gate topology is selected for this LNA design, widely used in wireless communications. Some of other commonly used topologies are common source and other cascode topologies. Those commonly preferred topologies, are heavily dependent on the common source stage developed gain, which in turn suffer from Miller's effect. To decrease this Miller's effect, a second layer of common gate is used [25] which in turn may give benefit of increasing gain (higher load impedance) but decreases the voltage headroom. Due to the reason of common gate not suffering from Miller effect, it gives an opportunity to get the acceptable reverse isolation by using a single transistor stage [26].

For this thesis work, the common gate topology is used for the input matching and amplification. Common gate topology higher output impedance issue was addressed by using modified White's casecode as the next stage, which has high input impedance, low and stable output impedance [25]. Both the stages were connected through DC blocking capacitor C1 (figure40). Input was fed to the LNA through the input capacitor C_IN, which is 37.57 fF (with multiplier = 20). It has the 20 multiplier value selected, because the input impedance of CG and the source impedance are small and C_IN has to form suitable time constant with both of them to transfer the RF-Input's at desired frequency. The inductor L1 is basically used as load of the common gate stage, but by using inductor, better performance and results can be achieved. It helps in better gain, low voltage supply requirement and better frequency selectivity.

Common gate stage is followed by the modified White's cascode, which is modified by using inductor L3 at the drain of transistor NM5.This inductor's (L3) loading effect makes the circuit operation more closer like a ideal follower by boosting up the amplification in local loop. It starts behaving approximately 100% negative feedback, which in response results in much low output impedance, making the circuit a better output stage [25]. Capacitor C4 helped in slightly curbing the noise and capacitors C_feed, Cout and C1, all of them were used for DC blocking. Voltage

divider resistors Rb1 and Rb2 were used to set the DC bias voltage at the gate of NM5, while current is set with current mirror. Two different results were compare, one while input was controlled with Rb1 and Rb2, and also while using only Rb1. Both results tells that using both of the resistor gives more stability while using only Rb1 gives a slightly higher output.

Figure 44(b) was the initial schematic diagram of common-gate circuit, it was designed without cascoded stage, just to get better understanding of operating frequency and effects of tank circuits components, input capacitor C_IN, LC tank circuit, L1 and most importantly the effect of different parameters of transistor NM0. It's an easy approach for the better practical understanding of common-gate stage of the LNA. After getting understanding of effects of different components, a high-input impedance modified White's cascode stage was introduced as second stage. Figure 45 shows the common-gate stage with modified White's cascode stage.

4.3 Inductor Design

Inductors used in this project were designed and tested separately, to get the desired inductance and operating frequency. The target was to get the operating frequency as closer to the highest Q-factor value and far away from self-resonance frequency. Q-factor value target was selected to have value range of between 8 and 10. All the inductor used in this LNA circuit has met the target Q-factor value of above 8.

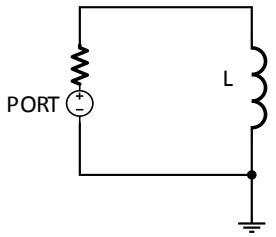

Figure 41: Inductor study circuit

After achieving the targeted Q-factor value, simple circuit (figure41) was designed to check the inductor's behavior at 7GHz and to confirm its Q-factor value**.** Figure42 shows the inductor's behavior and its self-resonance frequency (SRF), and it can be seen that the inductors used in LNA circuit are operating within the inductance range. It is always better to use an inductor operating far below the self-resonance frequency. For this LNA, one of the target was to avoid using any inductor above 3nH, so this was the best available option in this case. Following equation was used to get the inductance,

$$Z_L = j\omega L \tag{4.1}$$

$(Z = j\omega L)$, $(\omega = 2\pi f)$

For inductor, quality factor is expressed as,

$$Q = \frac{\omega L}{R} = \frac{X_L}{R} \tag{4.2}$$

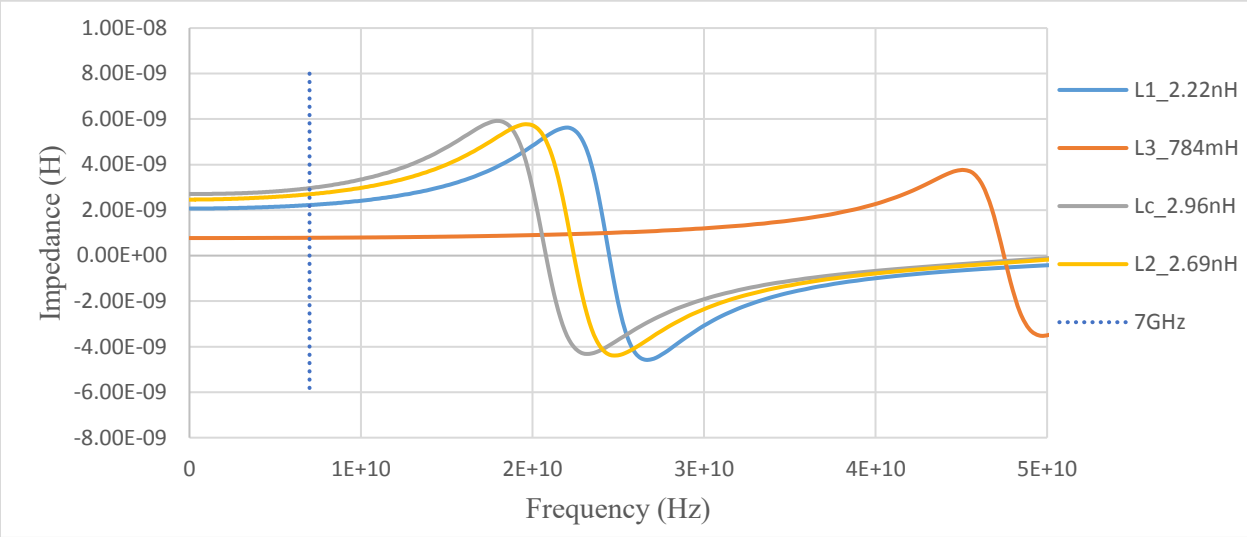

Figure 42: Inductors behavior at 7GHz frequency

In the below given figure, it shows the Q-factor values (table4) of inductors used in LNA circuit at 7GHz. In virtuoso (R) Visualization & Analysis XL calculator, by a command given below

```
imag(ZM("/PORT4"))/real(ZM("/PORT4"))
```

`imag(ZM("/PORT4"))` = Imaginary part of Inductor's impedance

`real(ZM("/PORT4"))` = Real part of Inductor's impedance

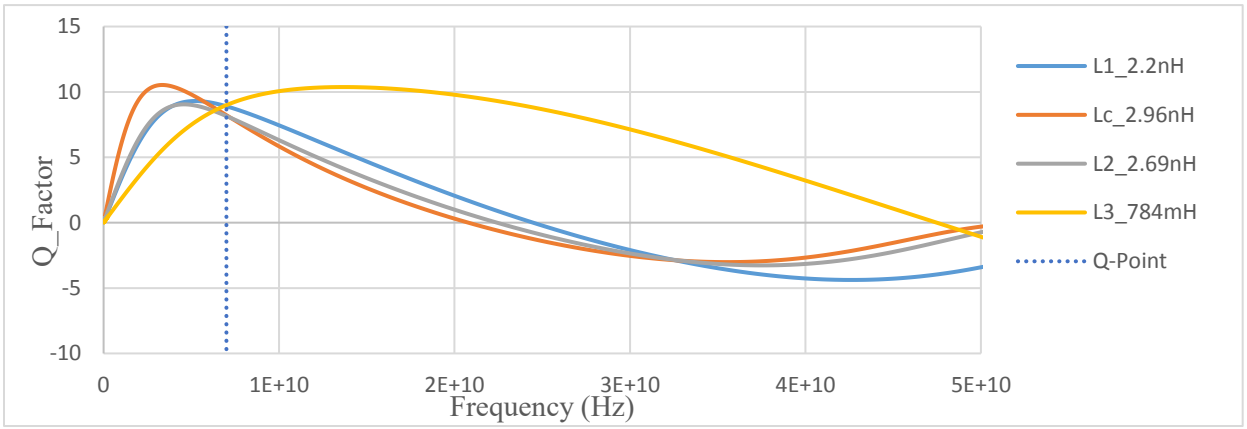

Figure 43: Inductors Q-Point at 7GHz frequency

4.4 Biasing

Common-gate stage was biased through supply-independent biasing circuit Figure 44(a), it was designed for circuit to bias itself, and output current should be independent of V_{DD}. To achieve independent current, the current between PM0-NM4 and PM1-NM10 must be the copy of each other, and PM0 and PM1 copy the output biasing current and hence defining the reference current. Resistor R_S is used specifically to define the currents, and transistor NM3 was added to handle the "start up" (zero current indefinite loop when supply is turned ON) issue. Diode-connected transistor NM3 helps in to take the circuit out of zero current indefinite loop while supply is ON, by providing a current path from V_{DD} through PM1 and NM4 to the ground at start-up condition [6].

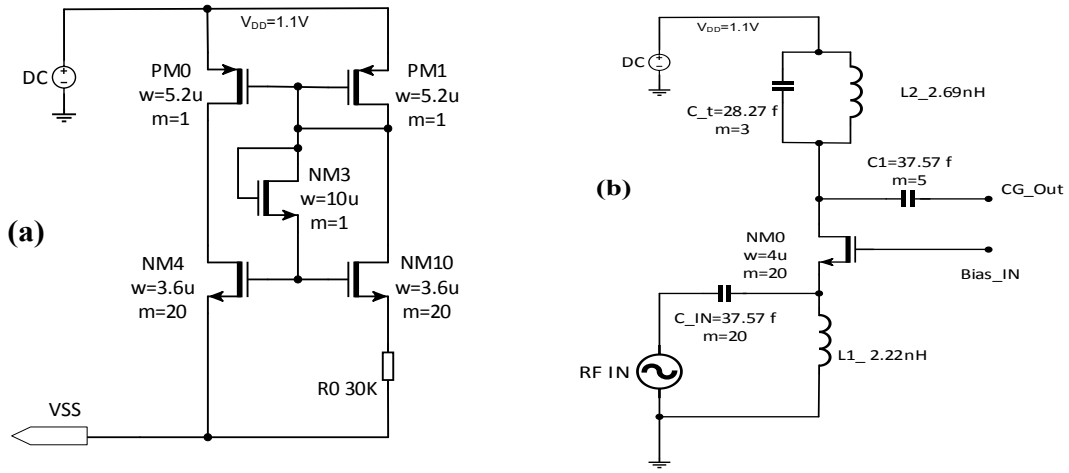

Figure 44: (a) Biasing stage and (b) Common Gate stage

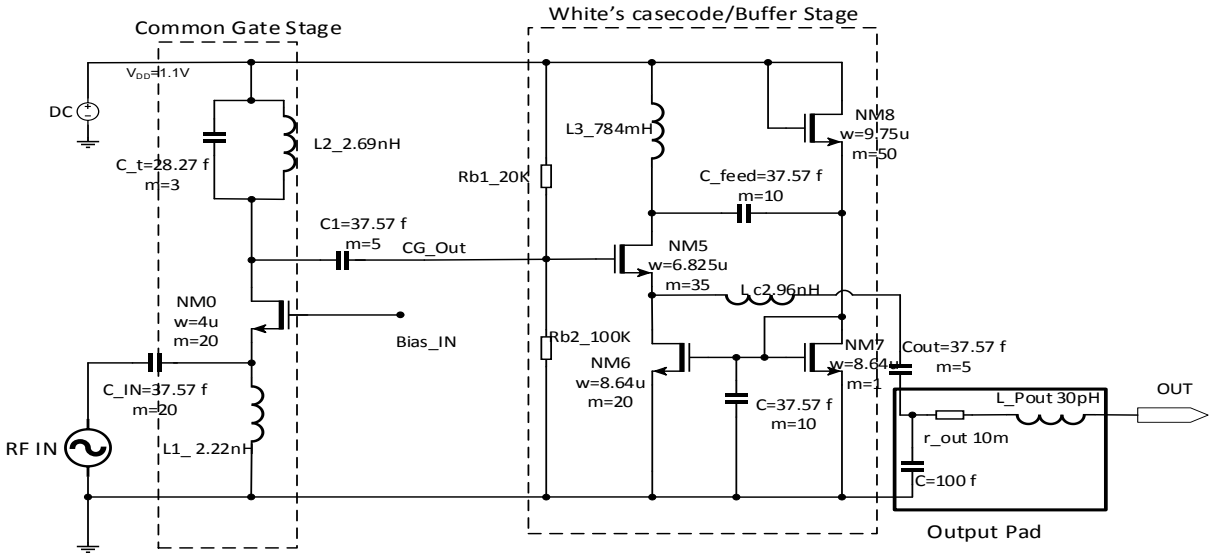

Figure 45: Common gate stage with White's casecode stage

4.5 Pad Models and Testbench

The LNA chip Input, output, VDD, voltage supply and ground pads were designed for the schematic design. Pads are used for the protection of integrated circuit from damages of unexpected and unwanted high voltages, which may occur due to faults on other parts of the circuitry or electrostatic discharges. Since pads are physically made up of metals, and are used in between the chip/LNA and the other parts of circuitry, they present additional capacitances, resistances and inductances. In these models, all those additional effects were considered and kept in schematic design.

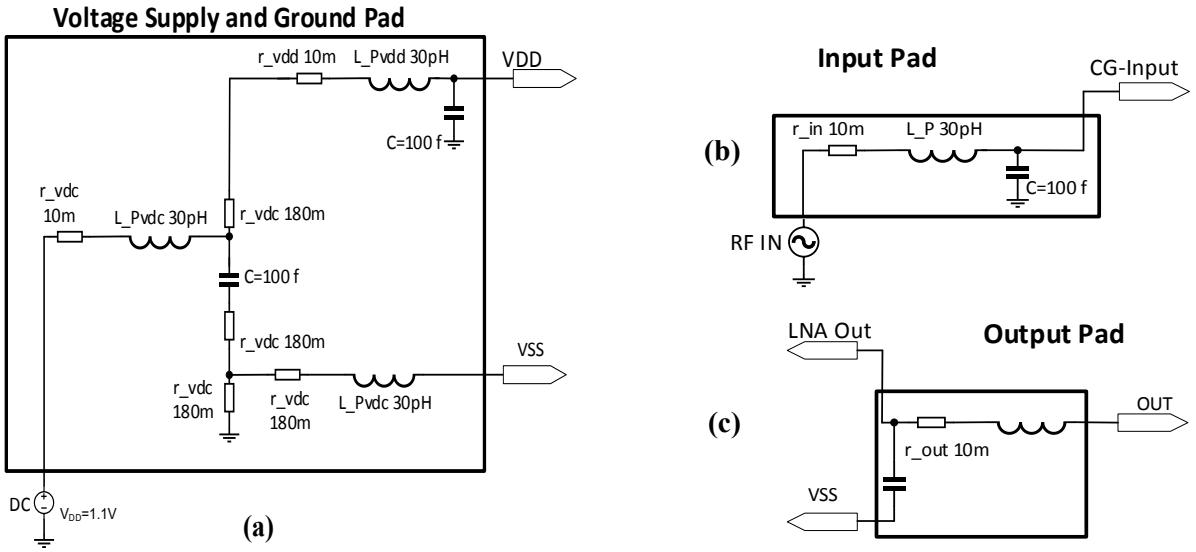

Figure 46: (a) VDD Pad and Battery model (b) Input Pad model (c) Output Pad model

Testbench was designed for simulating LNA parameters. To make it as amplifier measurement using network analyzer, its input and output are terminated by a resistive ports. Further, I/O, VDD, voltage supply and ground pads were connected to the main LNA cellview schematic.

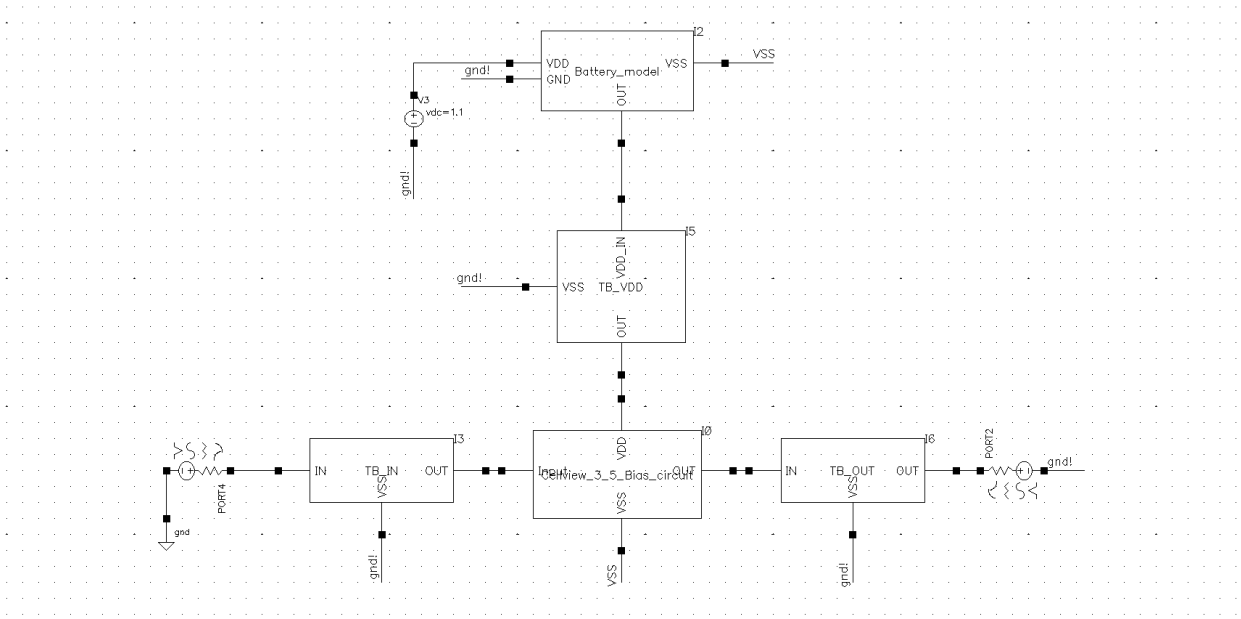

Figure 47: LNA testbench for measurements

4.6 Parameters Results

4.6.1 Scattering Parameters

Scattering parameters, also known as the S-parameters, tells about the performance of an LNA. It shows the gain $|S_{21}|$, the reverse isolation $|S_{12}|$, input-output matching which is characterized by input and output return loss $|S_{11}|$ and $|S_{22}|$.

In this presented LNA, gain $|S_{21}|$ of ~14dB is achieved at the 7GHz frequency. For input-output matching, the input return loss of -16.3dB and output return loss of -16.7dB were achieved. And for the reverse isolation of -27.1dB was achieved at the target frequency. Figure48 shows the results obtained from the cadence virtuoso, and the dotted line shows the target frequency point of 7GHz.

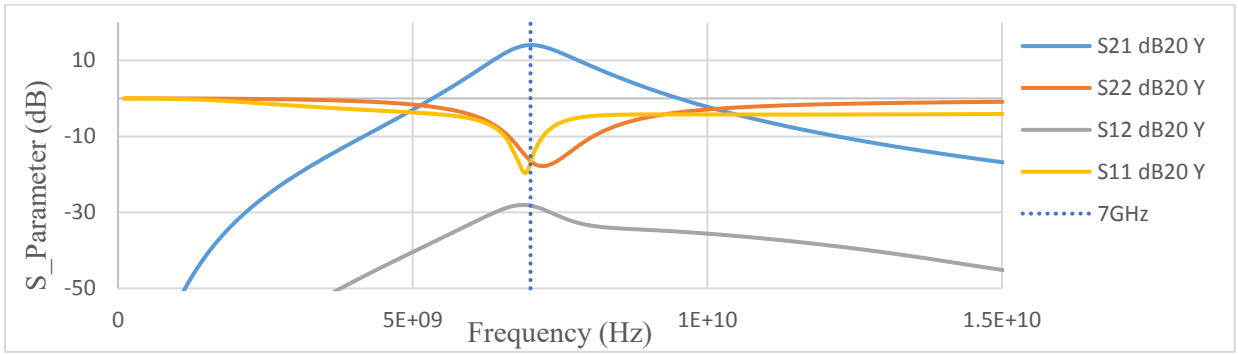

Figure 48: S-Parameters, $|S_{21}|$, $|S_{22}|$, $|S_{12}|$, $|S_{11}|$ at 7GHz frequency

4.6.2 Noise Figure

The noise figure of a system is defined as the noise factor in dB.

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{4.3}$$

SNR = Signal to Noise Ratio

$$NF = 10log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{4.4}$$

Noise factor of an LNA can simply be defined as the noise added by the LNA itself to the RF signal, and noise figure (NF) is the expression of noise factor in decibels. Lower the noise figure, the better it is. For this LNA, target value of not more than 3dB was selected at frequency of 7GHz. The main noise contributor in this LNA was NM0 (CG main transistor), and the second major noise contributor were the series resistors of inductor (L2_2.69nH), complete noise summary is given in Appendix B. However, NM0 total width value was adjusted to help in decreasing the noise figure. Figure49 shows that noise figure of 2.76dB is achieved. The vertical line shows the noise figure value at the 7GHz frequency.

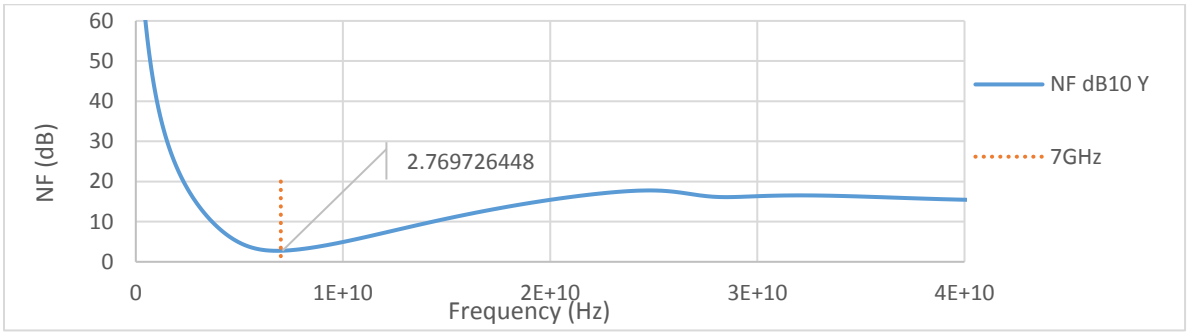

Figure 49: Noise Figure at 7GHz

4.6.3 Stability

The circuit may behave unstable for some of the sources and load impedances combinations, because of feedback paths from output to input, and starts oscillating with voltage variations at maybe higher or lower frequencies. To find out the stability of circuit over longer range of frequencies, a Stern stability factor is used to check the stability.

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}|\,|S_{12}|} \tag{4.5}$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$

And, if $K > 1$ and $\Delta < 1$, the circuit is unconditionally stable. Another factor B1f (Alternative stability factor) is also needed to be greater than 0 for stability.

Figure50 shows the stability factor for the longer range of frequency, and it can be seen a cross-section small line at the 7GHz point, that the K value is well above 1. Hence LNA is unconditionally stable. The marking line show 7GHz frequency point.

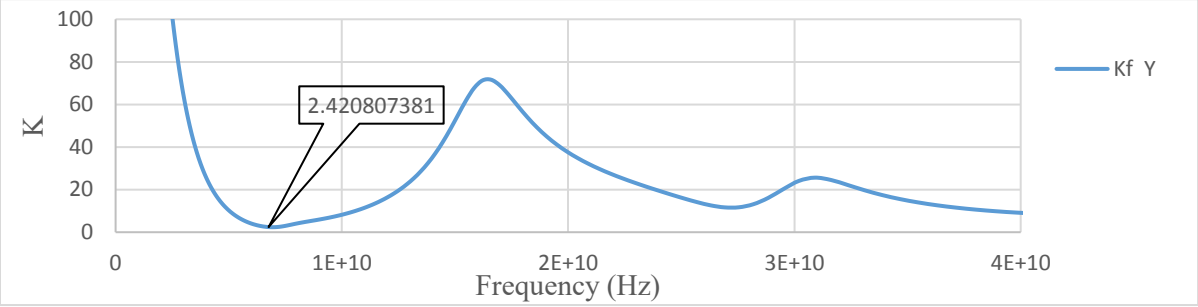

Figure 50: K-factor values 2.4 at 7GHz, and stays greater than 1 for much higher frequencies

Figure51 shows the alternative stability factor (B1f) plot. For the stability, B1f greater than 0 is required. The figure given below is showing B1f = 0.99 at 7GHz.

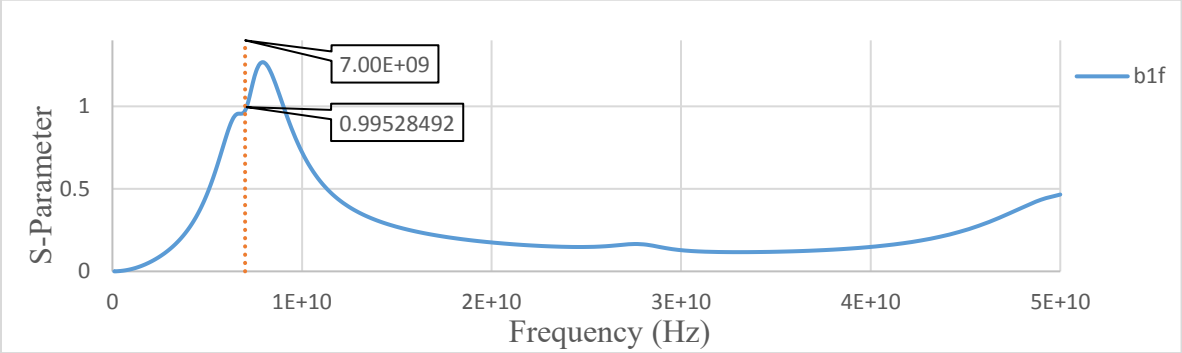

Figure 51: B1f (Alternative stability factor)>0 at 7GHz

4.6.4 Transient Analysis

Transient analysis results shows (figure52) that LNA has operating frequency 7GHz, and there are no glitches/irregularities within the output oscillation. Figure53 shows the transient current analysis, which shows the current drawn from the power source (vdc = 1.1 V).

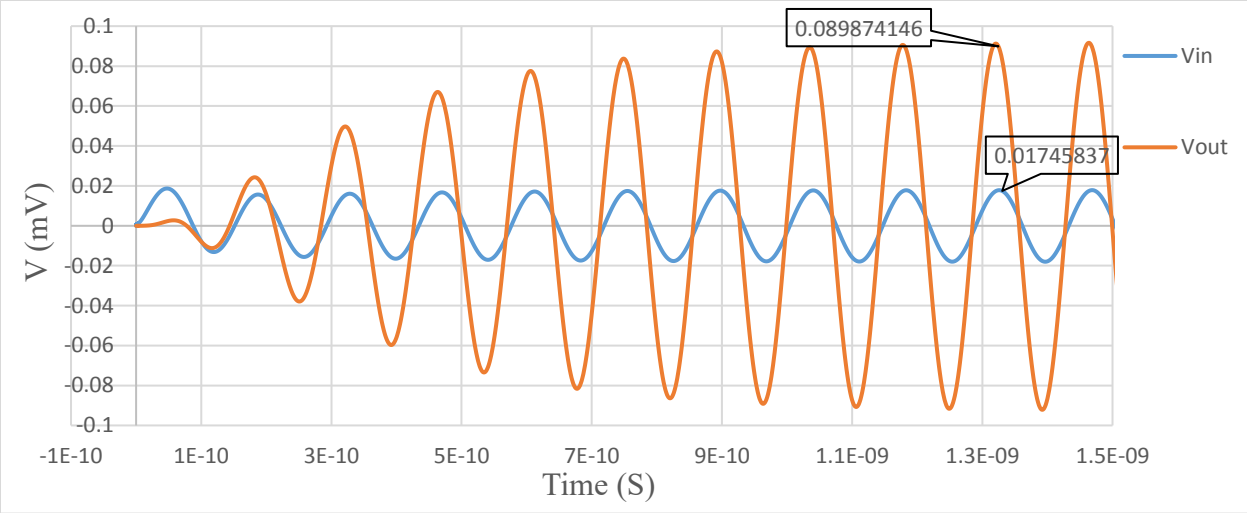

Figure 52: Transient analysis (voltage)

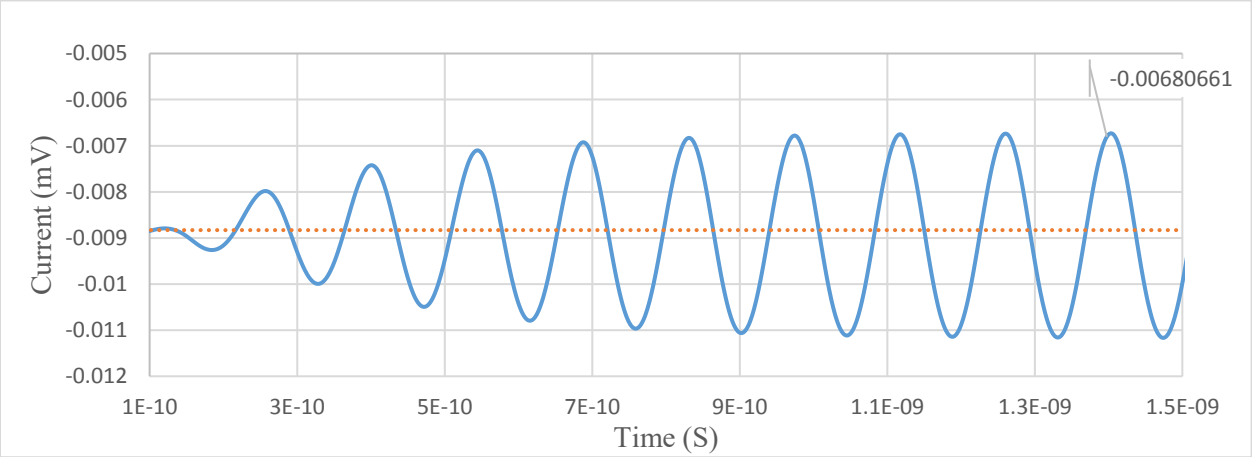

Figure 53: Transient (current)

4.6.5 1-dB Compression and IP3 Measurements

1-dB compression point measurements were done to find out the compression point where the gain linearity get distorted and with output doesn't increase in response to the input power. It is an important parameter to know where the 1-dB compression starts, so that input can be limited to that level and to stop happening any distortion. The results shows that gain at -40dBm input power is -26-(-40) = 14 dBm, which is fairly good match for small signal gain. 1-dB compression occurs at -13.77 dBm input power.

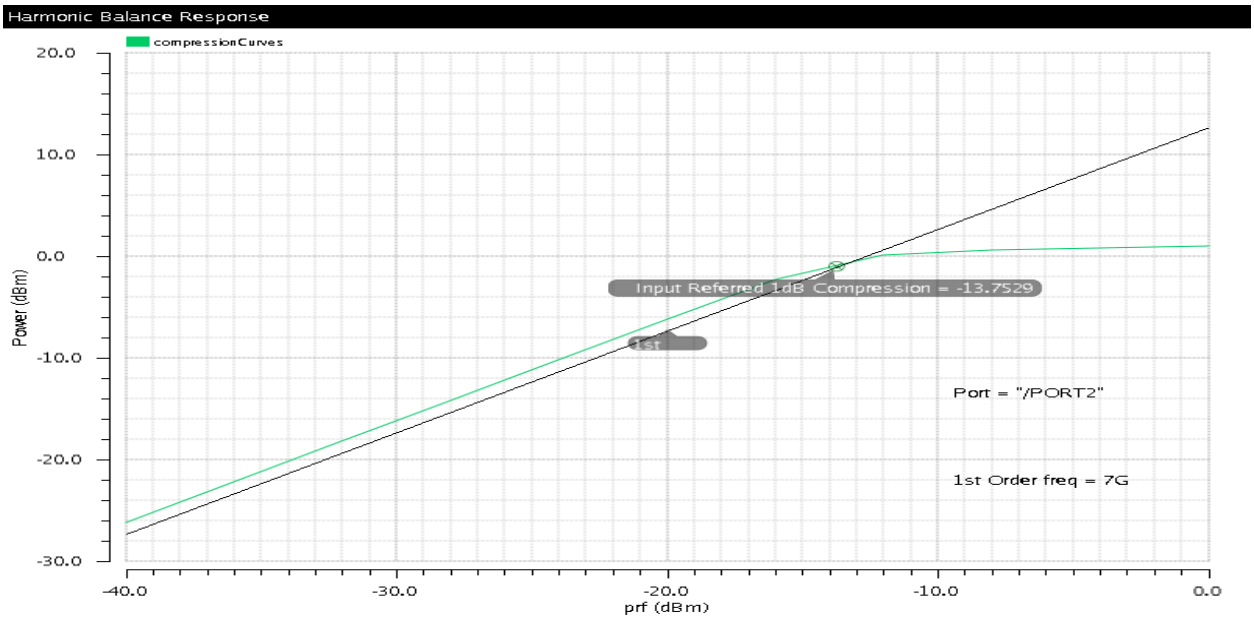

Figure 54: 1dB-Compression Curve

Another important parameter is IP3, explained in Background chapter at 1.1.5. It is an important to have IP3 point, to find about the linearity of an LNA. Figure 55 showing1st and 3rd order harmonic, and the spacing between two tones is 20 MHz.

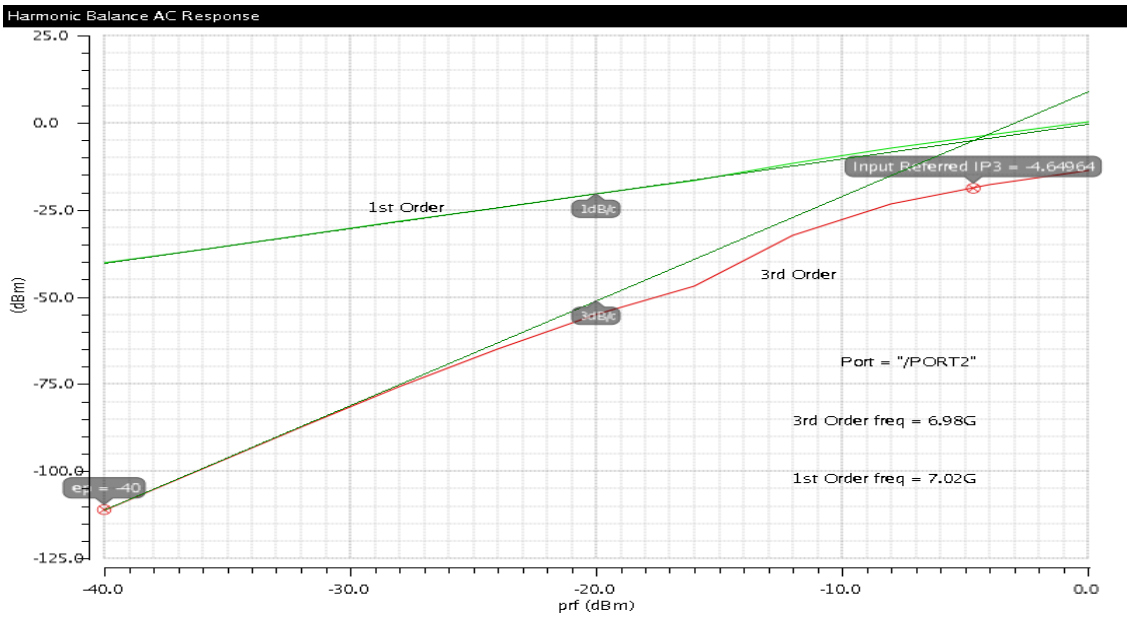

Figure 55: IP3 measurement intersection point between 1st and 3rd order harmonic

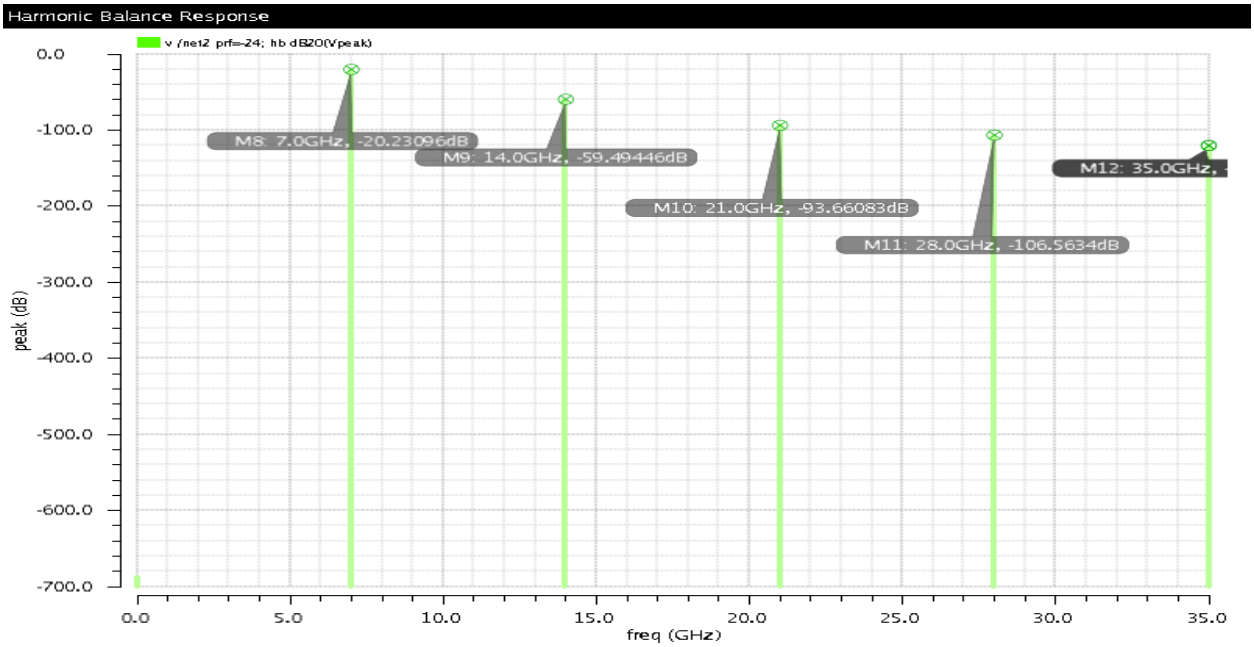

Figure 56: Nonlinear response of LNA for -24dBm input power

For different input voltage values, output response was checked to find out the effects on LNA output. It was found that for lower side of power values, the response was well linear till -16dB, a slight change in phase occur at -12dB, and then clear phase shift start happening at -8dB and further higher values. After -12dB input value, the gain stops further getting higher for higher input values (figure 57 and 58).

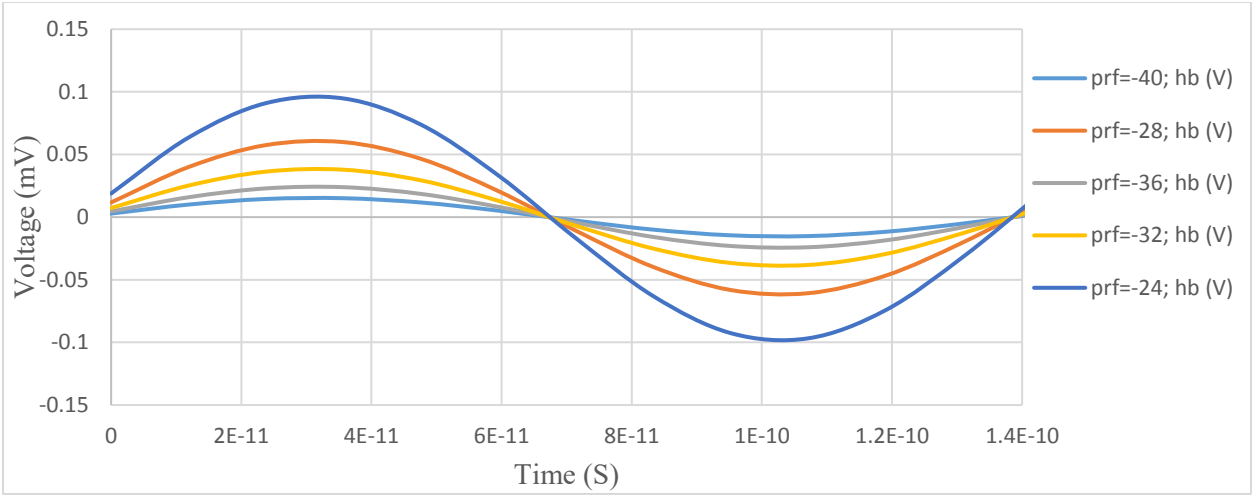

Figure 57: Output response for different input voltages

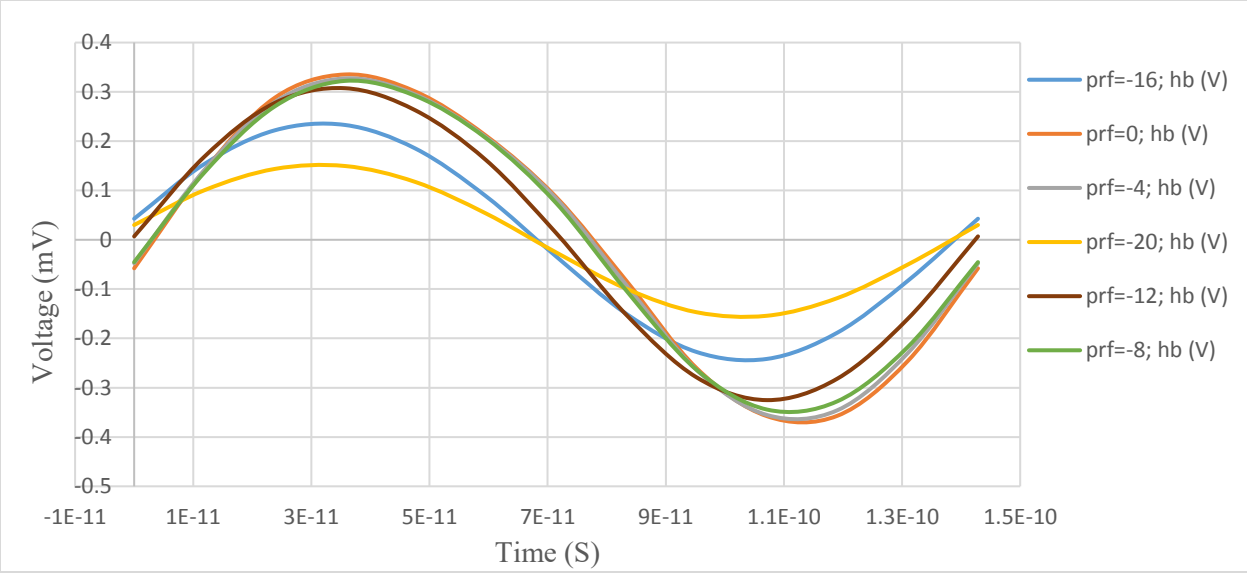

Figure 58: Output voltage response for higher input values

4.7 Design Specifications and Results

While designing the LNA, there is always a tradeoff between different parameters such as gain, linearity, noise figure and power dissipation. It depends on the practical usage of an LNA, for using in desired application, tradeoff should be made either for getting higher gain, linearity, stability etc. Therefore these parameter are very important to be kept as priority.

Specification comparison between target results and achieved results (schematic) are in the table-5 for presented LNA are as following:

Table 5: Comparison between target results and achieved (schematic) results

	Target	***Schematic Results***
Operating Frequency	7GHz	7GHz
Voltage	1.1 V	1.1 V
Gain	>12 dB	~14 dB
Power	< 9 mW	9.5 mW
NF	< 3 dB	2.7 dB
Stability	100MHz – 100GHz	100MHz – 100GHz

5. LAYOUT AND PARASITIC EXTRACTION RESULTS COMPARISON

In this chapter layout design and comparison between parasitic extraction results and schematic design results are presented. After getting desired results in electrical design, next step was to go to layout design and then parasitic extraction.

5.1 Layout Process

During the process of layout design, the generated layout has gone through design rule check (DRC), layout versus schematic (LVS) and lastly parasitic extraction before going to simulations with extracted parasitic. The best method was followed to check the layout by every few changes or modification in the design.

For better clarity and avoiding any complexity, the design was divided in three different circuits layout, which after every stage was DRC clean and LVS matched were connected together to form the whole LNA. After connecting all three stages (as in Figure59: Biasing, Common-Gate & White's Cascode), the whole LNA was again checked for DRC and LVS matching. It was next followed by the QRC, through which parasitic resistances and capacitances were extracted.

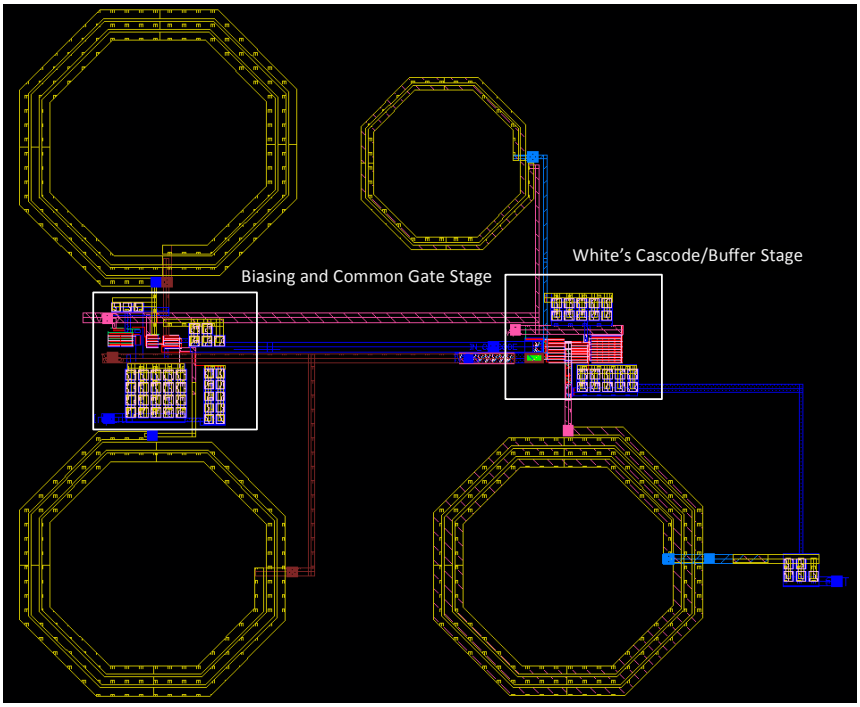

Figure 59: LNA Layout final version after DRC, LVS and QRC

In designing layout, important aspects were considered, to use higher metal layers for critical paths. Metal layer 10 was dedicated for RF input path, metal layer 8 was dedicated to VDD and metal layer 9 is dedicated for VSS. The reason behind this dedication was because of lower sheet resistance of higher layers and also higher current densities [27]. Inductors were placed carefully far from one another to avoid any coupling effect, because they are the critical components. Inductors are the biggest and critical components, so metal 11 was used for their design, as it has lowest sheet resistance. All the components except PMOS, were encircled by P-tap guard ring for shielding against electric field lines which are radiated within the LNA circuit and also providing convenience for grounding [28]. PMOS were encircled by N-tap guard ring, which is connected to VDD.

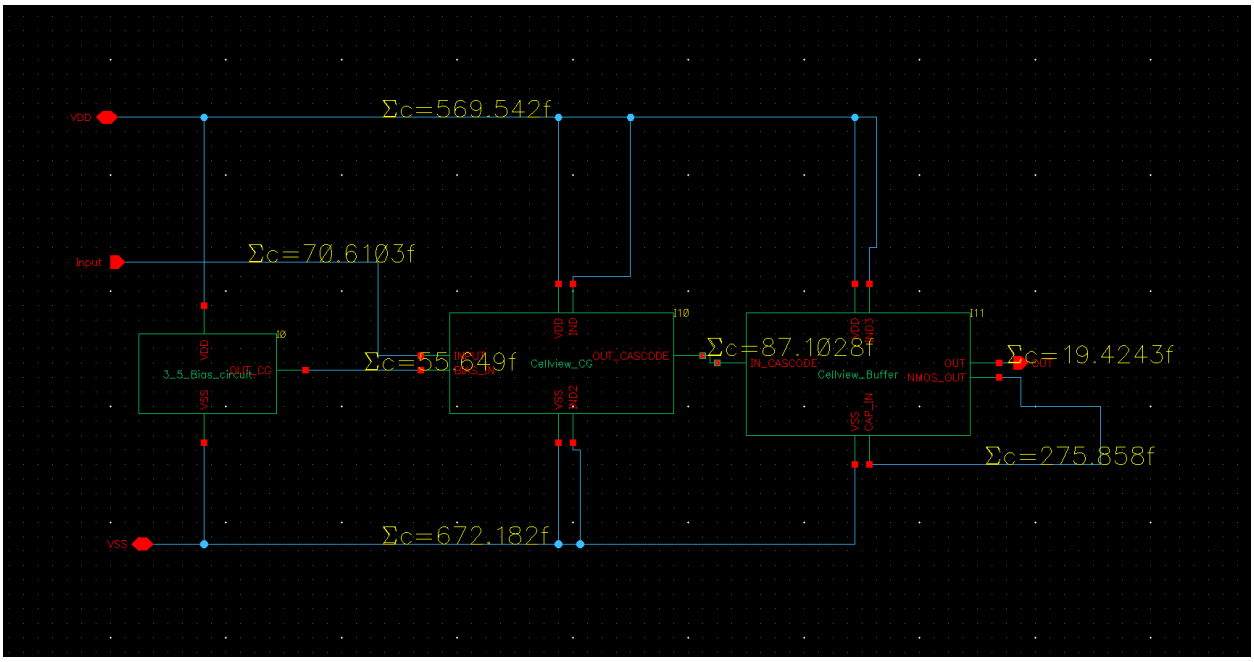

Figure 60: Schematic of LNA all three stages with parasitic capacitances value

5.2 Results Comparison

From the figure60 above it can be seen that good enough amount of parasitic capacitance is added into the initial LNA design. As we have a resonance frequency equation (3.5) discussed earlier, which tells us about the impact of capacitance on the resonant frequency of LNA.

$$F_r = \frac{1}{2_\pi} \frac{1}{\sqrt{L_1 \times C_1}}$$

According to this equation, the resonance frequency should become lower by the increase in capacitance in form of parasitic capacitance. To prove that condition, the extracted version of LNA different parameters were checked, and it was found that the LNA's operating frequency came down from 7GHz to 6GHz. Operating frequency was brought down by those parasitic capacitances. Different parametric results are shown to make a comparison between the LNA results before parasitic extraction and after parasitic extractions. It was also found that those parasitic extraction not only added capacitance, but also resistance to the LNA, which in altogether has also affected the gain of LNA.

Figures given below show both the cases, blue lines shows the simple LNA results, and the orange line with (P) at the start of legend shows the results for LNA after parasitic extraction. The vertical dotted line shows the operating frequency.

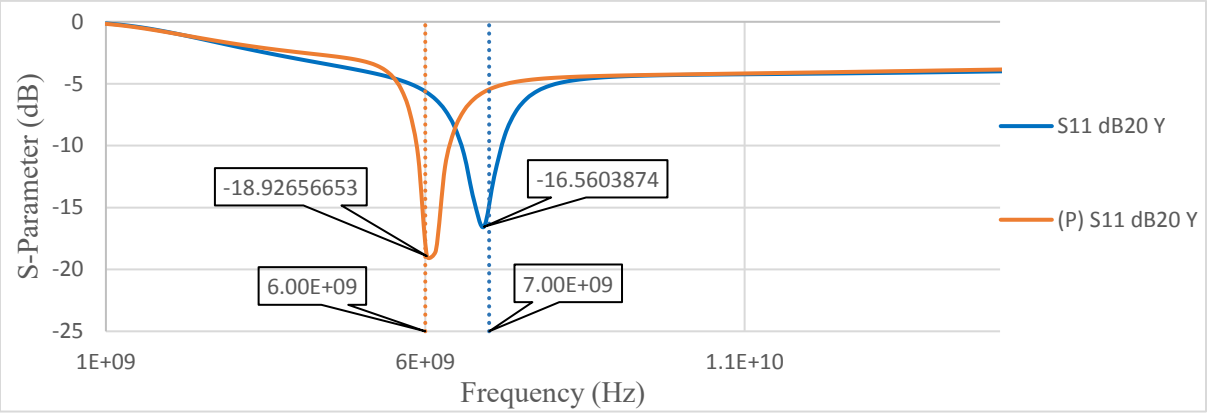

Figure 61: The reflection coefficient S_{11}, at 7GHz for simple LNA and 6GHz for parasitic extracted LNA

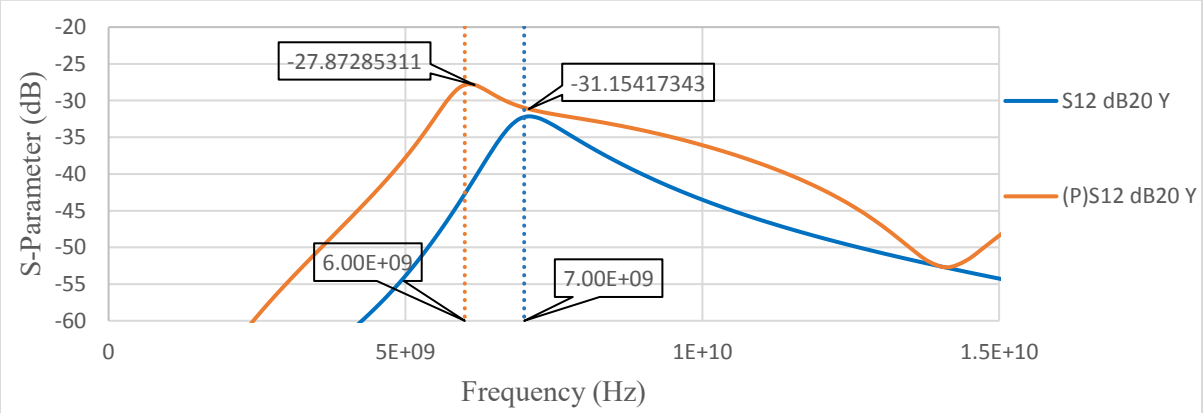

Figure 62: The reverse transmission coefficient S_{12} measurement

S11 shows the reflection coefficient observed at port1 and S22 shows the reflection coefficient observed at port2. S21 shows gain from port 1 to 2, and S12 shows the gain from port 2 to 1.

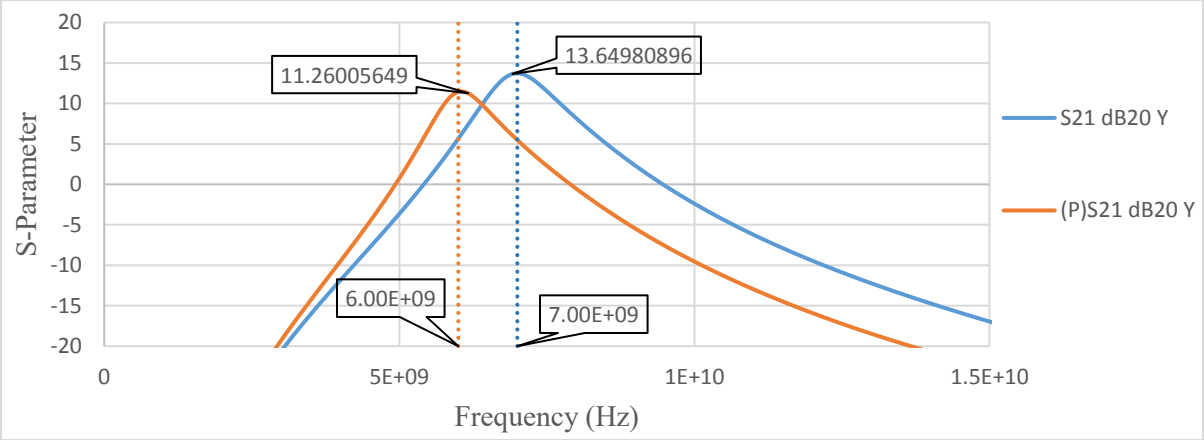

Figure 63: The forward gain or simply gain S_{21}, shows decrease in operating frequency after parasitic extraction and also loss in gain

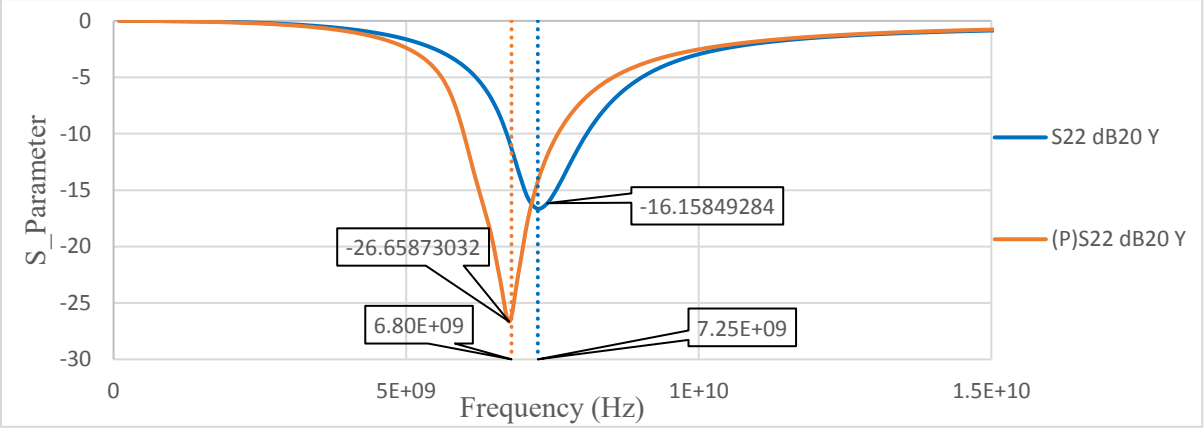

Figure 64: The reverse reflection coefficient S_{22}

For some other parameters, the values did not changed enough and remained almost the same. However, the frequency of operation get changed from 7GHz to 6GHz. It can be seen the figures 65 and 66, for NF and Stability factor. NF at 6GHz was (2.9dB) after parasitic extraction, and the stability factor stayed K>1 (3.24 at 6GHz) till the higher frequencies all the way. Figure 67 show alternative stability factor (b1f) > 0. Blue line shows LNA results without parasitic extraction and orange line shows the results with parasitic extractions.

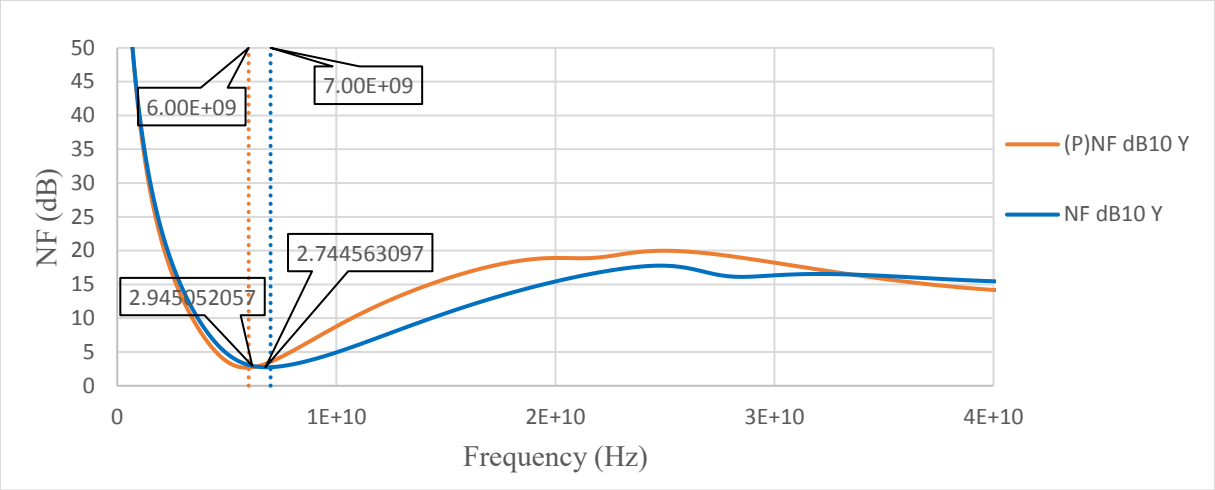

Figure 65: Noise figure for LNA with and without parasitic extraction

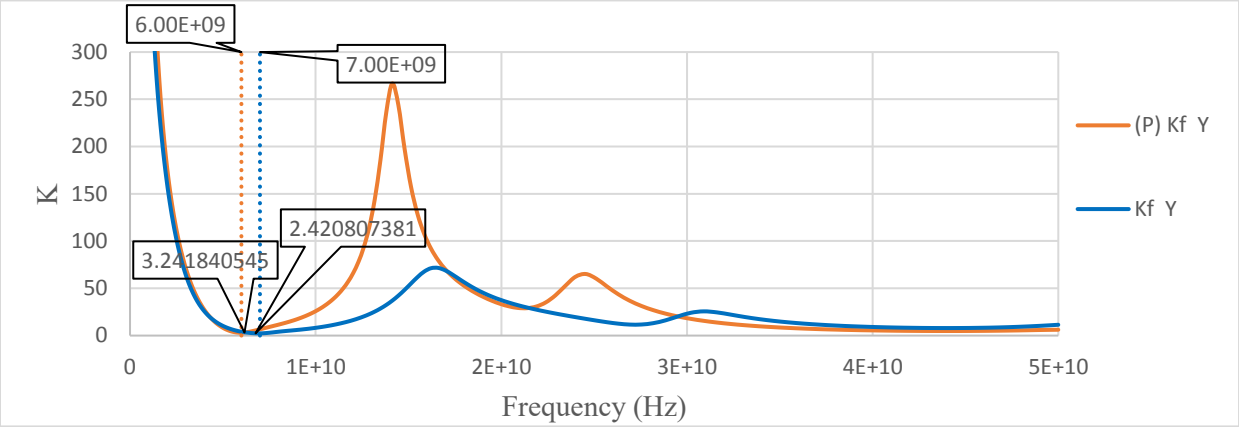

Figure 66: K-Stability measurements

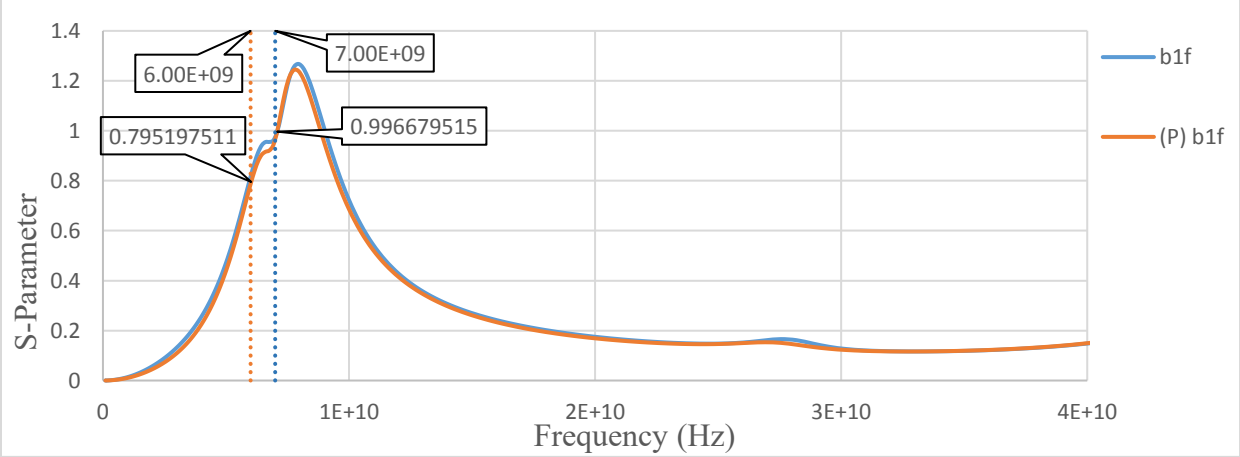

Figure 67: B1f (Alternative stability factor)>0 at 6GHz comparison between

After parasitic extraction the gain goes down and also frequency of operation become lower, the compression point also shifts, previously compression occurred at approximately -13dBm input power and now it occurs at -8.2 dBm input power.

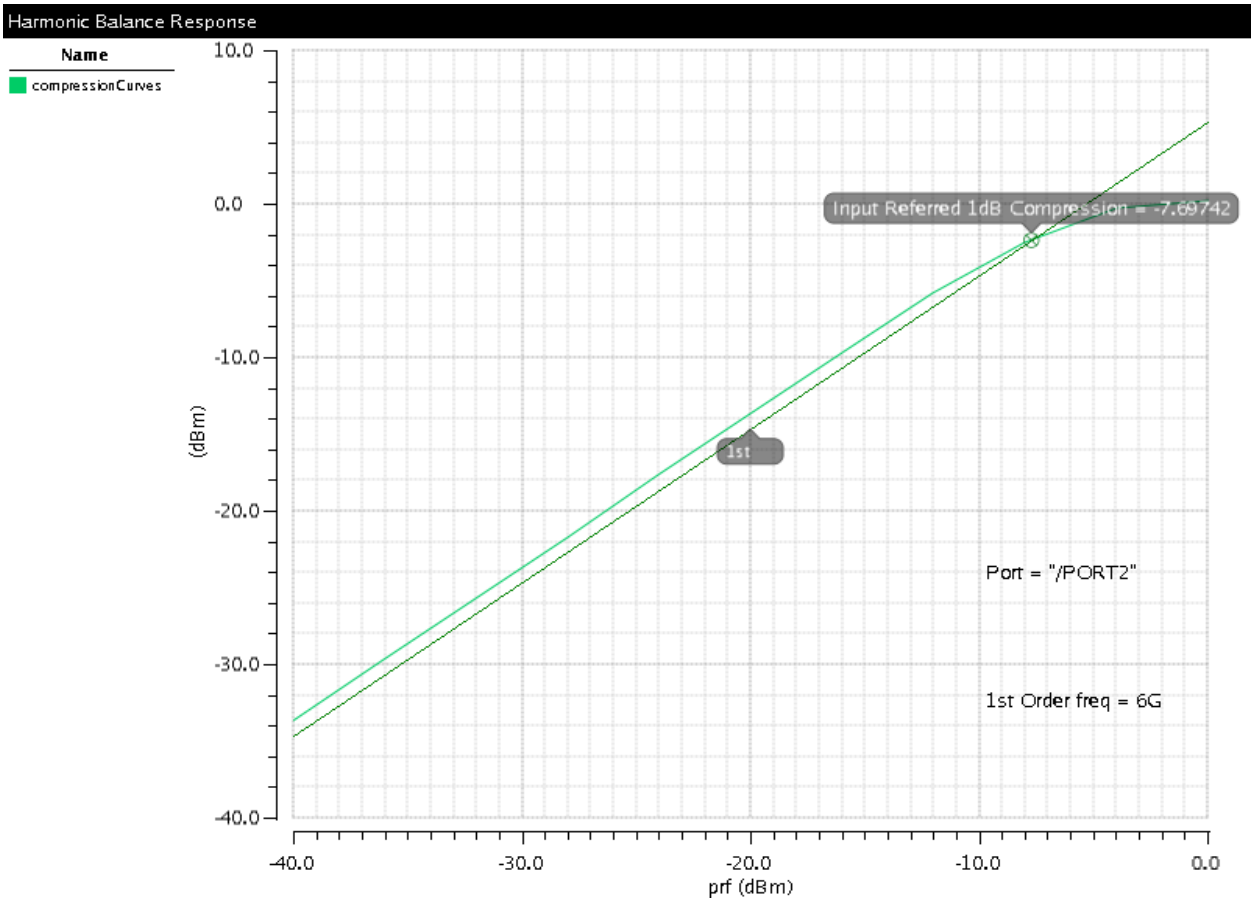

Figure68: 1dB-Compression point after parasitic extraction

Specification comparison between target results and achieved results (schematic) are in the table for presented LNA are as following:

Table 6: Comparison between schematic results and after extraction results

	Schematic	***Extracted***
Operating Frequency	7GHz	6GHz
Voltage	1.1 V	1.1 V
Gain	~14 dB	~11 dB
Power	9.5 mW	10.7 mW
NF	2.7 dB	2.9 dB
Stability	100MHz – 100GHz	100MHz – 100GHz

6. CONCLUSIONS

This thesis work is done with purpose to investigate the not very commonly used common-gate topology to design a 7GHz LNA. Same topology was used to design a scaled down version of 7GHz LNA, and its frequency of operation was 5MHz. Common emitter and other topologies are frequently preferred for research and production purposes, although they are heavily prone to the Miller effect. Common gate topology is a good alternative option, its higher output impedance can be matched to 50Ω easily by using White's cascode stage at output.

For BJT LNA, the purpose was to study different components effect on the LNA's several parameters. It was learned through practical measurements that LC tank is the major source of selecting operating frequency, by selecting proper inductor and then for the fine tuning we need to modify the capacitor in LC tank. Resistor Rb5 has an important role in a tradeoff between gain and linearity. For using higher value Rb5 (1KΩ), we can get higher gain (~24dBm), but the linearity for input power will decrease and the LNA become non-linear soon on higher input power side (starts distorting at -15dBm). On other hand, using lower value Rb5 (500Ω), we can get good amount of linearity for broader range of input power (-22dBm till -15dBm), with lesser gain (~20dBm). So, we can adjust all and select the values according to the desired practical usage. Schematic designed in Cadence Pspice and practical setup, shows the similar behavior throughout the measurements. It was drawing 13mA current from a 2Vdc power supply in the schematic, and in practical measurements, it was consuming 12mA current from power supply with 2V applied voltage.

The 7GHz CMOS LNA was designed with same topology, and a White's cascode stage was used to match the CG LNA output impedance to 50Ω standard. This LNA uses ~9.0mW of power with 1.1V input voltage. It was noticed that compression point comes soon in CG topology, as compare to CE topology. Besides that, there was no significant difference or lacking found in CG topology, and it is very suitable to be considered for future research purposes, while being used with White's cascode, which takes away the prominent issue of its output matching. Current consumption is higher in this presented LNA, and for the future work it can be minimized by using higher Q-factor value. Inductors used in this design were have Q-factor above 8, but increasing Q-factor helps in minimizing the current consumption. Increasing number of metal layers used for winding can help to get higher Q-factor value.

After the results comparison, it was noticed that the operating frequency gets lower from initial LNA operating frequency 7GHz to 6GHz for the parasitic added LNA. From the parasitic extraction it can be seen that some extra capacitance is added to the schematic. This parasitic capacitance was taken into account by using the netlist generated by QRC during layout

simulations, but are not exactly added to the schematic. In order to achieve the target frequency of 7GHz, the schematic LNA should be modified by decreasing the capacitance in tank circuit, to get the higher operating frequency according to how much it has dropped after parasitic extraction. Make those changes within the layout and follow the process again to get parasitic extracted LNA and compare the results again, and this process should be followed until the target operating frequency is achieved. Furthermore for the future work, the stability can checked and verified through Time-Varying Root-Locus (TVRL) technique. As it is successfully implemented, and proved to be more numerically precise [29] [30].

References

[1] S. M. B. G. C. Toumazou, Trade-offs in Analog Circuit Design: The Designer's Companion, Part 1, Springer, 2004.

[2] J. Rogers and C. P. (141-194), Radio Frequency Integrated Circuit Design, Artech House Inc, 2003.

[3] "A 3-10GHz low-power CMOS low-noise amplifiers-theory, design and applications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 50, no. 1, pp. 288-301, 2002.

[4] J. R. Long, "IEEE RFIC Journal," *General LNA Design Considerations,* no. 4, 2014.

[5] M. Marenk, "2.45 GHz SOI CMOS Low Noise Amplifier," Tampere University of Technology, Tampere, Finland, 1999.

[6] B. Razavi, Design of Analog CMOS Integrated Circuits, Los Angeles: McGraw Hill, 2001.

[7] K. S. Khandelwal and A. K. Kureshi, "Robust Design Challenges in Low Noise Amplifier," *International Journal of Innovative Research in Science, Engineering and Technology,* vol. 3, no. 4, pp. 343-349, 2014.

[8] C. Poole and I. Darwazeh, Microwave Active CIrcuit Analysis and Design (pp. 476-489), Elsevier Science, 2015.

[9] W. Aman, G. A. S. Sidhu, T. Jabeen, F. Gao and a. S. Jin, "Enhancing physical layer security in dual-hop multiuser transmission," in *Wireless Communications and Networking Conference (WCNC), 2016 IEEE*, Doha, Qatar, 2016.

[10] A. Mahmood, W. Aman, M. O. Iqbal, M. M. U. Rahman and a. Q. H. Abbasi, "Channel Impulse Response-based Distributed Physical Layer Authentication," in *Vehicular Technology Conference (VTC Spring), 2017 IEEE 85th*, Sydney, Australia, 2017.

[11] W. Aman, G. A. S. Sidhu, H. M. Furqan and a. Z. Ali, "Enhancing physcial laye security in AF relay-assisted multicarrier wireless transmission," *Transactions on Emerging Telecommunications Technologies,* vol. 29, no. 6, pp. 1-14, 2018.

[12] W. Aman, M. M. U. Rahman and a. J. Qadir, "Impersonation Detection in AWGN-Limited Underwater Acoustic Sensor Networks," pp. 1-10, 2018.

[13] B. Razavi, RF Microelectronics, Pearson Education Internationl, 2011.

[14] T. Hui and W. Wei, "Modelling and Simulation of the Nonlinear Response of Reciever Amplifiers," in *3rd Asia-Pacific Conference on Antennas and Propagation*, Harbin, China, 2014.

[15] T. E. Saunders and a. P. D. Stark, "An Integrated 4-GHz Balanced Transistors Amplifier," in *International Solid-State Circuits Conference*, New Jersey, 1966.

[16] J. Collard and A. Gobat, "High-dynamic-range low-noise microwave amplifier," *Electronics Letters,* vol. 6, no. 7, pp. 202-203, 1970.

[17] D. Ch'en, "A new low-noise bipolar C-band transistor," *1972 International Electron Devices Meeting,* vol. 18, pp. 36-36, 1972.

[18] K. H. G. Duh, P. C. Chao, S. M. J. Liu, P. Ho, M. Y. Kao and J. M. Ballingall, "A Super Low-Noise 0.1um T-Gate InAlAs-InGaAs_InP HEMT," *IEEE Microwave and Guided Wave Letters,* vol. 1, no. 5, pp. 114-116, 1991.

[19] J. Craninckx, M. Liu, D. Hausoie, V. Giannini, T. Kim, J. Lee, M. Libois, D. Debaillie, C. Soens, M. Ingels, J. V. Driessche, L. V. d. Perre and P. Vanbekbergen, "A Fully Reconfigurable Software-Defined Radio Transceiver in 0.13um CMOS," in *Digest of Technical Papers of the International Solid-State Circuits Conference*, 2007.

[20] M. Brandolini, P. Rossi, D. Manstretta and F. Svelto, "Toward multistandard mobile terminals-fully integrated recievers requirements and architecture," *IEE Transactions on Microwave Theory and Techniques,* vol. 53, no. 3, pp. 1026-1038, 2005.

[21] M. M. Rahman, H. E. Baidoo-Williams, R. Mudumbai and S. Gupta, "Fully wireless implementation od distributed beamforming on a software-defined radio platform," in *Proceedings of the 11th international conference on Information Processing in Sensor Networks (pp. 305-316)*, Beijing, China, 2012.

[22] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, New York: Oxford University Press, 2012.

[23] N. P. Cook, Practical Electronics, Ohio: Prentice Hall, 2002.

[24] A. R. Hambley, Electronics, Michigan: Prentice Hall, 2000.

[25] N. Tchamov and P. Jarske, "Low Noise Amplifier". Finland Patent 5,933,057, 3 August 1999.

[26] J. Kaukovuori, M. Kaltiokallio and J. Ryynänen, "Analysis and design of common-gate low-noise amplifier for wideband applications," *International Journal of Circuit Theory and Applications,* vol. 37, no. 2, pp. 257-281, 2007.

[27] "GPDK 45nm Mixed Signal GPDK spec," Cadence, 2014.

[28] R. C. Li, RF circuit design (pp. 352-355), John Wiley & Sons, Incorporated, 2012.

[29] A. Sohail, N. Tchamov and J. Järvenhaara, "VCO Start-up and Stability Analysis usin Time-Varying Root Locus," Tampere University Of Technology, Tampere, Finland, 2015.

[30] A. Sohail, S. Jain and N. T. Tchamov, "QVCO frequency stability analysis using time varying root locus," *IEICE Electronics Express,* vol. 13, no. 13, pp. 1-6, 2016.

Appendix A: List of HWD Ltd. PCB Inductors

LIST

of HWD Ltd. PCB Inductors*

No	Current Label	New Label	L_p nH	R_p kΩ	$C_p \sim C_s$ pF	R_s mΩ	L_s nH	f_0 MHz	R_{dc} mΩ	Part No
1.	**R271**	**R159**	158,87	90,91	3,98	90,91	158,87	200,138	53	**317a**
2.	**R191**	**R170**	170,34	48,95	2,89	44,39	170,33	227,41	35,5	**219**
3.	**R228**	**R180**	180,04	15,25	4,93	129,35	179.99	168,79	72	**415a**
4.	**R256**	**R226**	226,02	15,02	4,47	132,67	225,92	158,346	78	**513a**
5.	**R179**	**R243**	242,95	71,47	3,50	71,47	242,95	172,42	58,3	**317**
6.	**R385**	**R245**	245,23	18,292	3,932	76,65	245,15	161,75	59	**317b**
7.	**R351**	**R328**	327,85	21,75	4,07	91,05	327,75	136,419	75,5	**415b**
8.	**R390**	**R352**	351,99	47,29	2,96	83,04	351,96	155,01	77,5	**415**
9.	**R399**	**R373**	372,84	22,05	4,14	106,99	372,72	127,977	87	**513b**
10.	**R431**	**R409**	409,50	65,67	2,84	91,77	409,48	148,547	78	**513**
11.	**R566**	**R564**	564,17	38,72	2,63	175,6	564,02	130,7	172,6	**6/31**
12.	**R805**	**R793**	793,1	218	2,35	218	793,1	117,529	210,7	**7/31**
13.	**1R10**	**1R11**	1110	50,78	2,63	315,18	1110	92,98	262,5	**8/31**
14.	**1R37**	**1R39**	1390	52,98	2,61	413,20	1390	83,59	364	**9/24**
15.	**1R77**	**1R71**	1710	51,96	2,87	463,42	1710	72,02	414	**10/24**
16.	**1R86**	**1R79**	1790	27,3	5,89	323,41	1790	49,09	314	**2x6/31**
17.	**2R05**	**1R98**	1980	50,10	3,25	588,12	1980	62,047	536	**11/20**
18.	**2R52**	**2R49**	2490	56,05	2,80	631,52	2490	60,74	586	**12/20**
19.	**2R72**	**2R57**	2570	24,99	7,05	471,87	2570	37,22	382,5	**2x7/31**
20.	**3R06**	**3R06**	3060	61,73	2,59	780,03	3060	56,98	738	**13/20**
21.	**3R18**	**3R09**	3090	51,78	2,60	1020	3090	55,78	986	**14/12**
22.	**3R82**	**3R55**	3550	26,37	8,64	355,48	3550	28,828	475	**2x8/31**
23.	**3R73**	**3R67**	3670	62,72	2,57	1210	3670	51,22	1,161	**15/12**
24.	**4R32**	**4R20**	4200	59,07	2,59	1270	4200	48,05	1,219	**16/12**
25.	**4R80**	**4R38**	4380	27,98	8,35	740,82	4380	26,47	659	**2x9/24**
26.	**4R98**	**4R84**	4837	65,96	2,608	1485	4834	45,08	1,460	**17/12**
27.	**5R69**	**5R64**	5640	84,94	2,57	1550	5630	41,40	1,513	**18/12**
28.	**6R32**	**5R97**	5970	19,02	9,01	847,06	5960	21,857	762,5	**2x10/24**
29.	**6R49**	**6R22**	6220	89,90	2,57	2220	6210	38,839	1,758	**19/12**
30.	**7R33**	**6R88**	6880	89,22	2,72	1910	6880	36,436	1,852	**20/12**
31.	**7R26**	**6R94**	6940	21,73	8,05	1060	6920	21,39	994	**2x11/20**
32.	**9R14**	**8R52**	8520	22,50	9,03	1190	8490	18,045	1,088	**2x12/20**
33.	**11R38**	**10R2**	10240	23,45	10,14	1580	10210	15,546	1,400	**2x13/20**
34.	**11R24**	**10R8**	10750	25,64	6,35	1980	10700	19,235	1,904	**2x14/20**
35.	**13R39**	**12R5**	12540	26,76	6,93	2610	12490	16,928	2,207	**2x15/12**
36.	**15R85**	**14R4**	14410	28,45	7,58	2510	14,370	15,219	2,362	**2x16/12**
37.	**18R66**	**16R6**	16640	29,85	8,13	2860	16570	13,68	2,784	**2x17/12**
38.	**21R87**	**19R1**	19070	30,57	8,76	3030	18990	12,30	2,947	**2x18/12**
39.	**25R54**	**21R8**	21830	30,38	9,26	3550	21730	11,29	3,464	**2x19/12**
40.	**29R84**	**24R3**	24340	32,10	10,06	3760	24250	10,155	3,636	**2x20/12**

Appendix B: List of Noise Contributing Components

Device	Param	Noise Contribution	% Of Total
/PORT4	rn	4.66099e-18	50.28
/IO/NM0	fn	1.5473e-18	16.69
/IO/NM0	id	9.22455e-19	9.95
/IO/I3/rs1	rn	2.05342e-19	2.21
/IO/I3/rs2	rn	1.99652e-19	2.15
/PORT2	rn	1.77815e-19	1.92
/IO/I3/rsbp2	rn	1.74133e-19	1.88
/IO/I15/rs2	rn	1.62202e-19	1.75
/IO/I15/rs1	rn	1.49147e-19	1.61
/IO/NM5	id	1.31153e-19	1.41
/IO/PM2	id	1.25575e-19	1.35
/IO/I3/rsbt1	rn	9.18967e-20	0.99
/IO/I15/rsbp1	rn	9.10646e-20	0.98
/IO/NM6	id	7.02505e-20	0.76
/IO/NM1	id	6.52805e-20	0.70
/IO/I15/rsbt1	rn	4.86437e-20	0.52
/IO/I3/rs22	rn	3.91727e-20	0.42
/IO/I3/rs11	rn	3.82476e-20	0.41
/IO/NM5	fn	3.71385e-20	0.40
/IO/I35/rsbp2	rn	3.67851e-20	0.40
/IO/I15/rs22	rn	3.44998e-20	0.37
/IO/I15/rs11	rn	2.87587e-20	0.31
/IO/I35/rsbt1	rn	2.28202e-20	0.25
/IO/I35/rs2	rn	1.84258e-20	0.20
/IO/I35/rs1	rn	1.8369e-20	0.20
IO.NM0.xrg.r1	thermal_noise	1.76496e-20	0.19
/IO/NM6	fn	1.60722e-20	0.17
IO.R1.R0.r4	thermal_noise	1.42483e-20	0.15
IO.R1.R0.r3	thermal_noise	1.42381e-20	0.15
IO.R1.R0.r2	thermal_noise	1.42309e-20	0.15

Spot Noise Summary (in V^2/Hz) at 7G Hz Sorted By Noise Contributors
Total Summarized Noise = 9.27069e-18
No input referred noise available
The above noise summary info is for sp_noise data

PORT4 and PORT2 are not the parts of main LNA circuit, so they are not considered as noise contributor.