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30 GHz RF-DAC BASED I/Q MODULATOR

Master of Science Thesis

ABSTRACT

For massive MIMO systems, large number of antennas and transmitter chains are considered. This huge and complex circuitry consume lot of power. For saving the power, the modulator and DAC can be integrated in to one. Therefore, by taking in to account of power consumption, the 30 GHz RF-DAC based I/Q modulator has been investigated. The thesis work summarizes the circuit design and simulation of digital I/Q modulator based on RF-DAC which is implemented by combining digital to analog converter and mixer in to one circuit block. The analog blocks are completely removed that saves chip area and power consumption. Since large portion of analog circuitry is removed, so it gives high efficiency and output power.

In this thesis, the research work is to design 4-bit RF-DAC based I/Q modulator in 130nm SiGe, BiCMOS process at 30 GHz. The I/Q modulator consist of several blocks: differential branch line coupler, Wilkinson power combiner, 50-100 and 100-50 Ω input and output BALUN circuit.

The circuit is designed for the four bits' digital input. The problem of glitches arises as the output shifts from one level to next. In order to overcome this problem, the concept of thermometer coding logic has been used. So for the four binary bits, the thermometer coder gives 15 outputs. Thus, 15 conversion cells are designed and arranged in parallel in two quadrant RF-DACs I/Q modulator.

PREFACE

The thesis work has been carried out in the Department of Microtechnology and Nanoscience, Microwave Electronics; GHz Centre at Chalmers University of Technology, Gothenburg, Sweden.

First of all, I would like to say thanks to my supervisors Dr. Mustafa Ozen and Prof. Christian Fager for their profound guidance throughout my thesis. It's been a great privilege to work under these wonderful supervisors. I would like to thank my thesis Examiner Prof. Jukka Vanhala for allowing me to work on my thesis in exchange program. I wish to thank my friend Andreas Johansson for helping me a lot in various issues. Special thanks to Vidisha Naik and Aditya Premi for encouraging me.

Last but not least my parents and my whole family for their moral and mental support throughout my Masters study.

Tampere, 20.6.2016

Salman Ahmad

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LIST OF SYMBOLS AND ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
BALUN	Balanced Unbalanced
DAC	Digital to Analog Converter
DC	Direct Current
DNL	Differential Non-linearity
DSP	Digital Signal Processing
I_{BB}	In-phase Base Band signal
Q_{BB}	Quadrature Base Band signal
IC	Integrated Circuit
INL	Integral Non-Linearity
LO	Local Oscillator
LTE	Long Term Evolution
Q	Quadrature
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RF-DAC	Radio Frequency Digital to Analog Converter
RX	Receiver
SFDR	Spurious Free Dynamic Range
SNDR	Signal-to- (Noise + Distortion)
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion
TX	Transmitter

.

1. INTRODUCTION

1.1 Motivation

There are lot of design challenges in conventional transmitter and receiver which usually contains complex analog baseband components that requires large chip area and power consumption. The research in the field of wireless communication has been shifted towards the digital domain since digital designs offer more flexibility and enables a higher level of integration.

A conventional up-conversion transmitter has separate digital to analog converter (DAC) and quadrature modulator. A DAC is used to convert digital signals to continuous analog time-domain signals. The analog signal is then up-converted by the mixer. A conventional up-converter IQ modulator is shown in Figure 1-1.
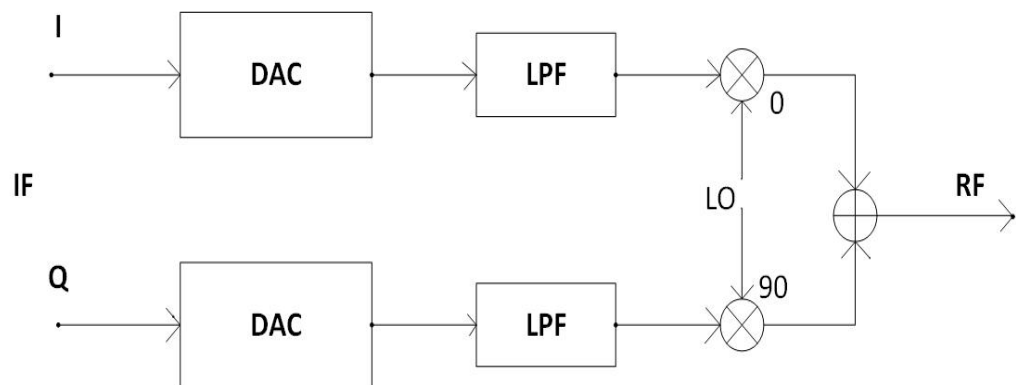
Figure 1- 1 Conventional DAC based transmitter

To solve the problem of power consumption, the modulator and DAC are integrated in to one. This architecture is known as Radio Frequency Digital to Analog Converter (RF-DAC). The RF-DAC based I/Q modulator is shown in Figure 1-2.
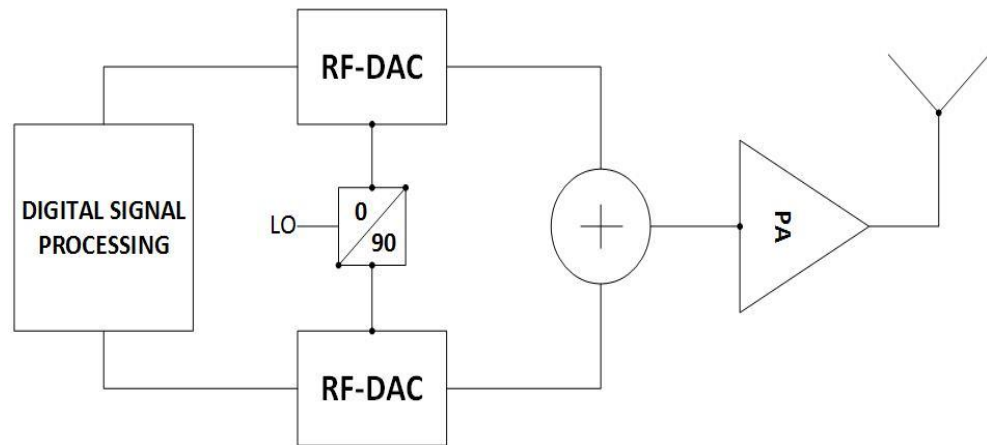
Figure 1- 2 RF-DAC based transmitter architecture

The idea of RF-DAC was first introduced by Luschas *et al*. that fulfills the criteria of high output power, high efficiency and high speed [1]. Basically RF-DAC is a combination of digital to analog converter and mixer in to one block, omitting the requirement of separate DAC and mixer. The digital input data is directly applied to the RF-DAC. Thus, for the implementation of the 4 bit I/Q modulator, the RF-DAC conversion cells are arranged in parallel for both the I and Q quadrant. Their output is summed together at the RF port.

There are several advantages of using the digital transmitter because it is easy to integrate and to implement on the chip.

1.2 Objective of thesis

The main objective of the thesis is to design a modulator for the millimeter wave application which gives high power, high efficiency. A 30 GHz RF-DAC based I/Q modulator has been implemented in 130 nm BiCMOS technology. Since the DAC and modulator has been integrated in to one functional block, it gives high efficiency and output power.

1.3 Organization of thesis

The outline of thesis is described as follows:

- **Chapter 1- Introduction:** Introduction to thesis
- **Chapter 2- Digital to Analog Converter:** the basic introduction of digital to analog converter is described. The dynamic and static performance requirements are discussed in detail as well as the architectures of converter.
- **Chapter 3- Quadrature Modulator:** The concept of I/Q modulator, characteristic of I/Q modulation and types of mixer are discussed that are pre-requisite of RF-DAC.

- **Chapter 4- Concept and Fundamentals of RF-DAC:** The history and background of RF-DAC is presented. Different architectures of RF-DAC have been compared on the basis of implementation and performance has been evaluated.
- **Chapter 5- Components of Proposed I/Q Modulator:** The basic components of implemented I/Q modulator have been described.
- **Chapter 6- Circuit Implementation and Simulations:** the complete circuit implementation and simulations are shown step by step.

2. DIGITAL TO ANALOG CONVERTER

A digital to analog converter is used to convert the digital signal to continuous analog signal. The DAC is the boundary between the digital and analog signals that connects the abstract world to real world. Signals can be easily restored and can be transmitted in the form of digital domain. The converter is briefly explained in the following points.

2.1 Concept of DAC

The basic concept of DAC is to take binary data as input and outputs analog continuous signal that is voltage or current. Below diagram is the possible representation of the converter [2].
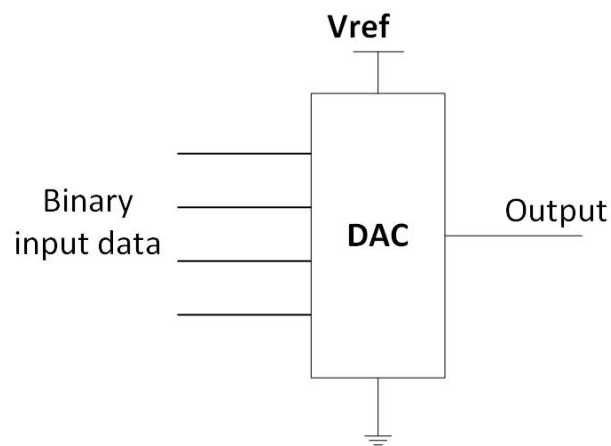
Figure 2- 1 Digital to Analog Converter

A digital to analog converter reconstructs the continuous time varying signal from the available sampled data and it introduces the quantization noise during the conversion.
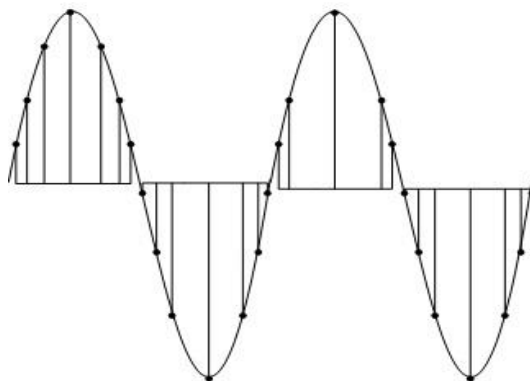
Figure 2- 2 Reconstruction of signal from sampled data

2.2 Current steering DAC

Current steering mode DAC converter is illustrated in Figure 2-3. The basic principle of this converter is, the input digital bits controls the two current steering branches comprising of transistor switches that drives out the current. Here, N-bit digital control words are fed to the switch pair that steers the current of the current source to one of the two output loads connected.

The topology of the converter is described as follows: The current source steering branches are controlled by the digital words. Depending on the input code, the branches drives out the current to the load or to the ground. The advantage of this architecture is that it is easy to implement and it provides good efficiency [3].
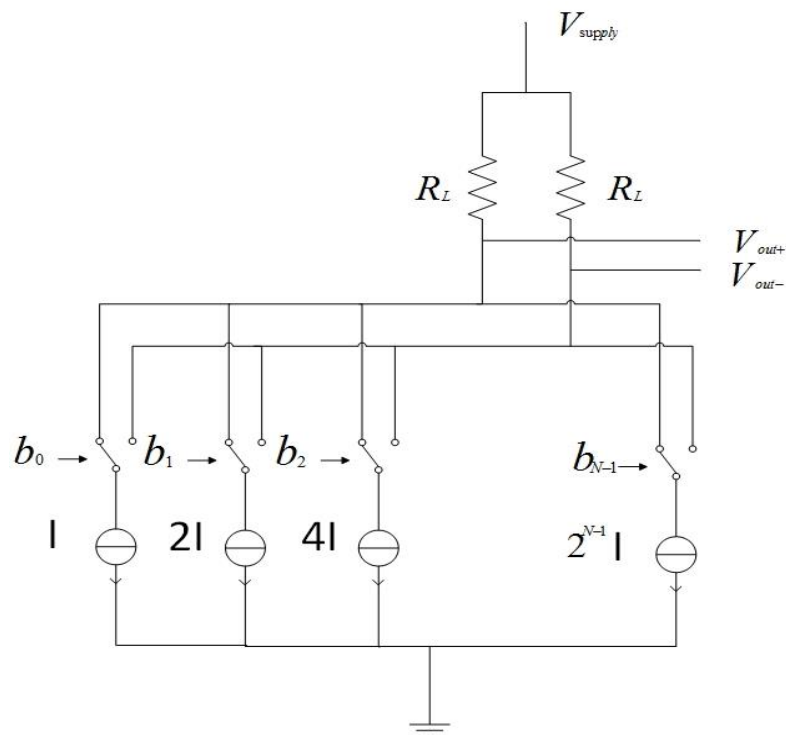
Figure 2- 3 Current steering DAC

2.3 Performance

The performance measure of DAC is categorized as static and dynamic performance.

2.3.1 Static performance

The static performance of DAC accounts the deviation of the output response than the ideal straight curve. It includes DNL (Differential Non-Linearity), INL (Integral Non-Linearity), offset and gain errors [4].

Differential Non-Linearity

DNL represents the deviation of the two adjacent output values from the ideal value of 1 LSB. To achieve the monotonicity of output values in accordance with the input values, the DNL must be greater than -1 LSB. The differential nonlinearity DNL and INL are illustrated in the Figure 2-4. The height at the digital code 001 is in accordance with the ideal curve, i.e., DNL is zero. Whereas the height at the 011 digital code words became half of the ideal curve, therefore,

$$DNL_3 = 0.5 \text{ LSB} \tag{2.1}$$

Integral Non-Linearity

INL represents the maximum deviation from the ideal characteristics curve. In the given Figure2-4 the straight line represents the ideal transfer curve [3].
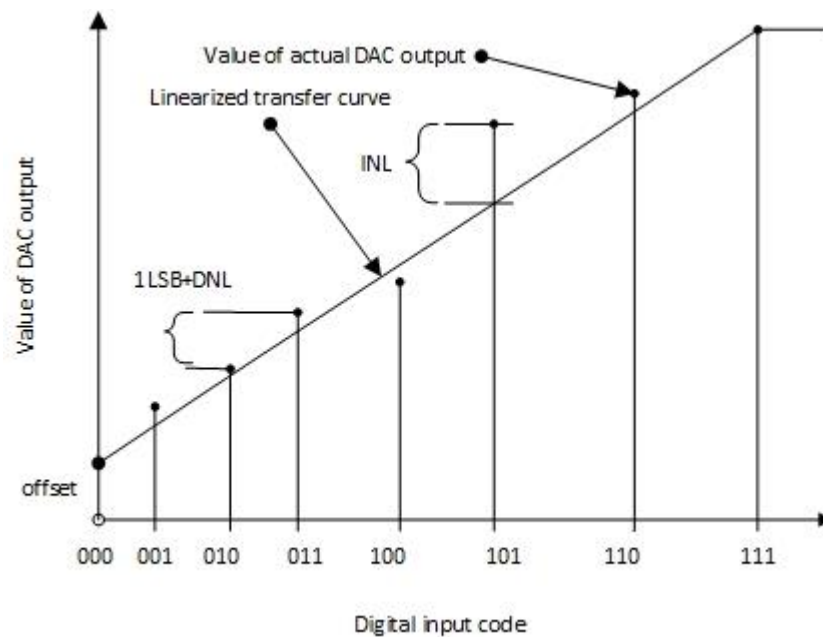
Figure 2- 4 *DNL and INL of digital to analog converter*

2.3.2 Dynamic performance

The dynamic performance describes the behavior of DAC when the transition or shifting between input level occurs. The most important dynamic performance metrics are SNR, total harmonic distortion, Spurious-free Dynamic Range (SFDR), Signal to noise and distortion ratio (SNDR) and glitches [5] [6]. The performance metrics are illustrated in Figure 2-5.

Spurious-free Dynamic Range

It is the ratio of the fundamental tone to the second harmonic component or the largest power component in the frequency domain spectrum. SFDR and unwanted noise are inversely proportional to each other.

Total Harmonic Distortion

THD is defined as ratio of the total power at the harmonics and the signal power.

Signal to Noise Ratio

SNR is the ratio of the fundamental tone to the noise floor in the Nyquist region. It is expressed in decibels.

Signal to (noise + distortion) ratio

SNDR is the ratio of fundamental tone to the Nyquist region plus the total harmonics.

Glitches

This performance metric is important for the behavior of the DAC. A glitch generates when the transition takes place. This occurs due to the charge injection in the switch transistor during the shifting of one output level to other level, as a result it displays a wrong code at the output. Let's take an example, if the code changes from 01111 to 10000, for a while it displays 11111 at the output and it creates error [7].
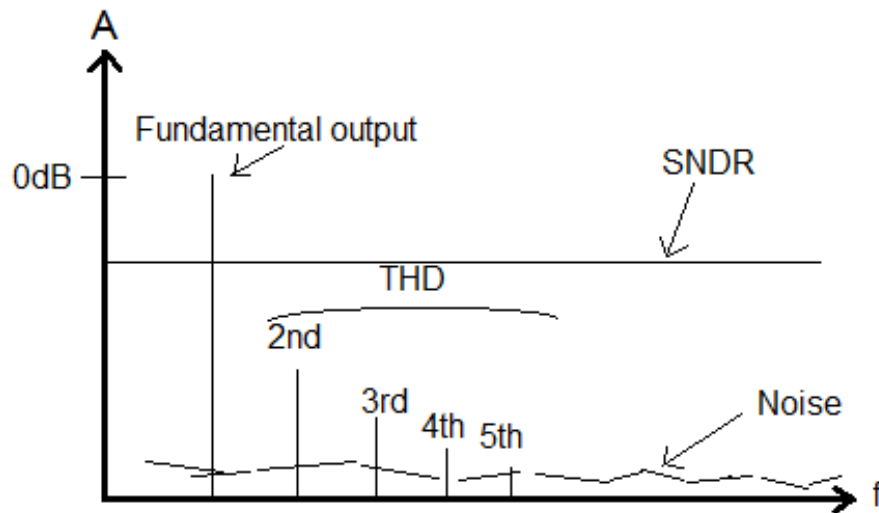
Figure 2- 5 *Dynamic performance metrics*

2.4 Architectures of DAC

Generally, there are three types of architectures namely, binary, thermometer and segmented architectures. There are other types of available architectures, but in this section only the basic architectures are described.

2.4.1 Binary weighted architecture

Binary weighted architecture uses binary input data directly. The number of binary weighted current source responds to the corresponding bits applied at the input. There are three ways to implement the binary architecture: resistor, charge redistribution and current mode. The advantages of this architecture are, easy to implement, less number of switches required therefore less chip area is required for integration and gives high power. But the problem is, there is large gap between the least significant bit and the most significant bit and the matching is not guaranteed between them, therefore, it creates DNL and INL errors. If the switching of the current sources is not synchronized properly, glitches generates between the transition of two level at the output [6].
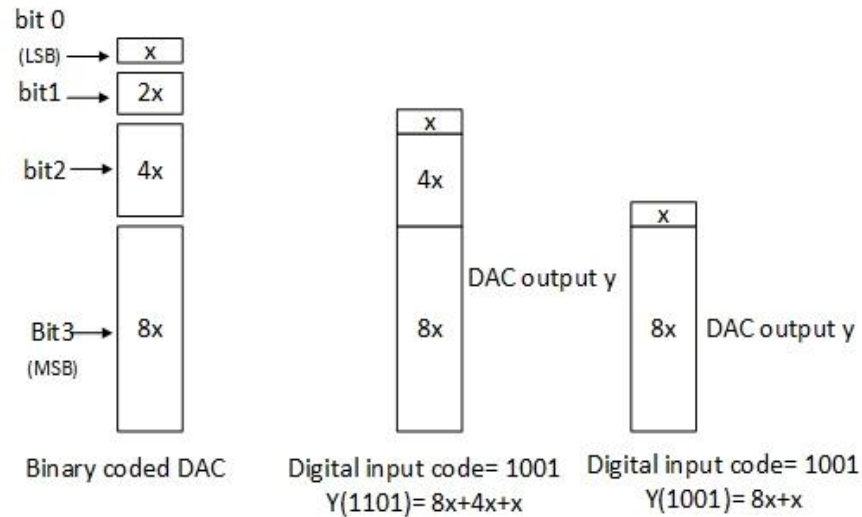
Figure 2- 6 *An example of 4 bit DAC*

A 4bit binary coded D/A converter is shown in the Figure 2-6. When a digital code 1101 is applied to DAC it outputs:

$$y(1101) = 8x + 4x + x \qquad (2.2)$$

When the digital input is 1001,

$$y(1001) = 8x + x \qquad (2.3)$$

Here, there is large gap between the MSB and LSB.

2.4.2 Thermometer based architecture

In the binary weighted architecture, the problem DNL and INL arises as the number of bits' increases. To overcome these problems, a thermometer based DAC is developed. In this architecture, a thermometer coder is used that gives $2^N - 1$ digital thermometer bits to represent 2^N digital input bits. The cost of this architecture is higher in comparison to binary weighted architecture. This architecture requires lots of switches, power and large area on the chip. Thermometer coding is therefore typically not preferred if number of bits larger than ten. [4].

There are several advantages of thermometer architecture such as having low DNL, improved monotonicity and reduced glitches problem.

Table 1 *Thermometer code representations for 3-bit binary values*

Decimal	Binary	Thermometer Code
d_0	$b_2 b_1 b_0$	$s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1$
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

By comparing binary weighted DAC and thermometer weighted DAC, it is found that using the thermometer architecture, will not increase the size of analog circuit portion. This is because, in thermometer weighted architecture, the total resistance is same as the resistance used in the binary weighted DAC. Hence, all the conversion cells and switches are equal in sizes and all the switches draw equal amount of currents. A binary to thermometer based DAC is shown in Figure 2-7.
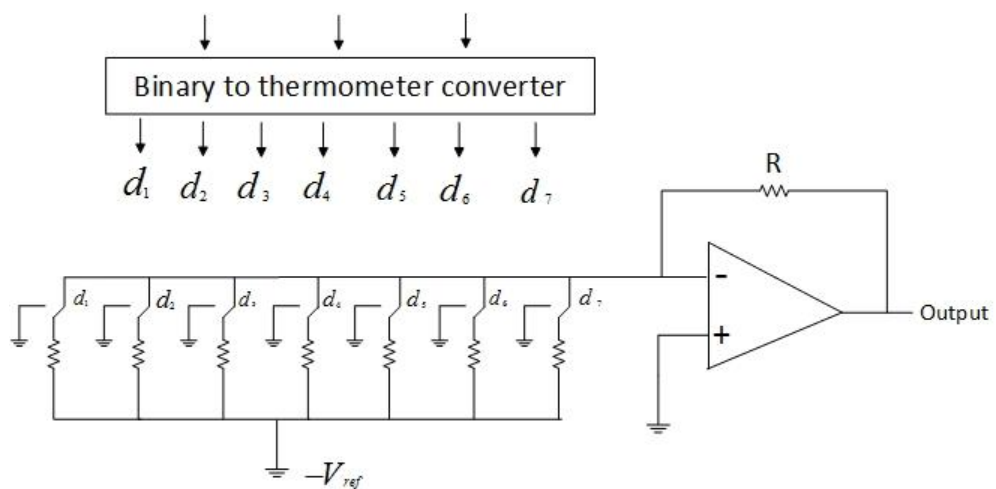
Figure 2- 7 *A 3-bit thermometer- based digital to analog converter*

2.4.3 Segmented architecture

Segmented architecture describes the DAC in such a way, that some part of the input is implemented in the binary and some part is implemented in thermometer coding. This means the MSBs are implemented in thermometer elements and other LSBs are represented in binary elements. In this way, a DAC of large number of bits can be implemented.

As an example, in the Figure 2-8, a 5-bit DAC is represented, 3-bit are implemented as thermometer coding and remaining 2-bit are implemented in binary coding.
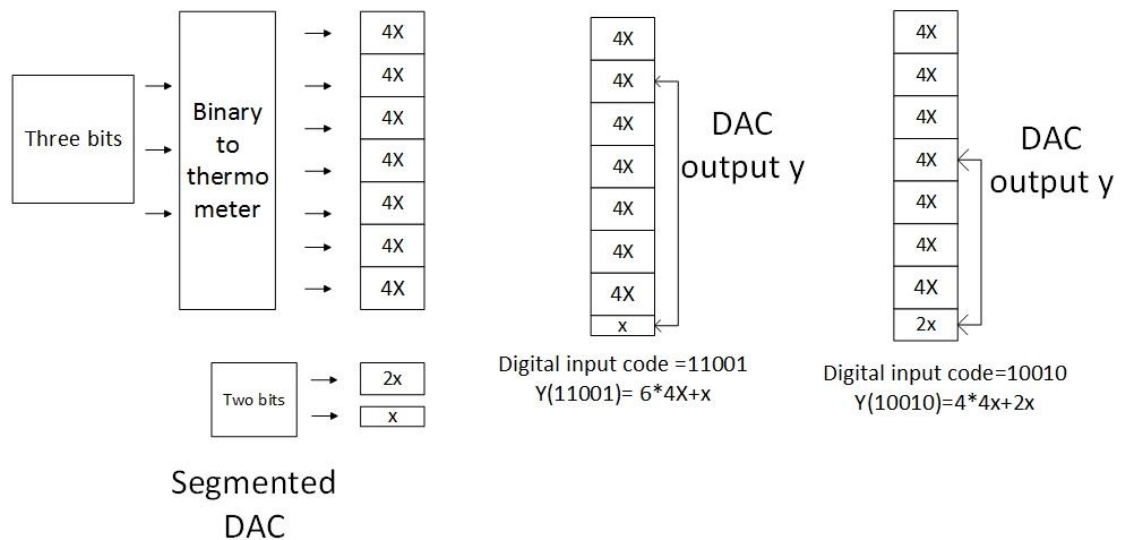
Figure 2- 8 A 5 bit segmented DAC

2.4.4 DAC realization

Based on implementation, the DACs can be classified in to three categories: resistive ladder, switched-capacitor and current steering DAC. Current steering DAC is already explained in section 2.2, remaining types are described in this section.

Resistor based digital to analog converter

This architecture is also called as R-2R ladder binary weighted DAC converter, shown in Figure2.8. This architecture is easy to implement. Generally, two different resistors are used that reduces the complexity of the converter. The characteristic of this architecture is, it can be used to implement the binary weighted elements using two different resistors that provides more accuracy and better matching.

Switched capacitor digital to analog converter

This architecture is also called as redistribution DAC. In this architecture capacitors are used to store the charge unlike the resistor used in R-2R ladder architecture. These capacitors are responsible for the conversion of digital bits to analog signal. It is shown in Figure 2.9 that when the capacitors are connected to the reference voltage, the feedback to the op-amp circuits is connected and the output voltage is the fraction of the reference voltage. If it is connected to the ground, both inverting and non-inverting inputs of op-amp are at zero potential, therefore there is zero voltage at the output. The disadvantage of this architecture is same as R-2R ladder, its accuracy depends on the matching of capacitors.
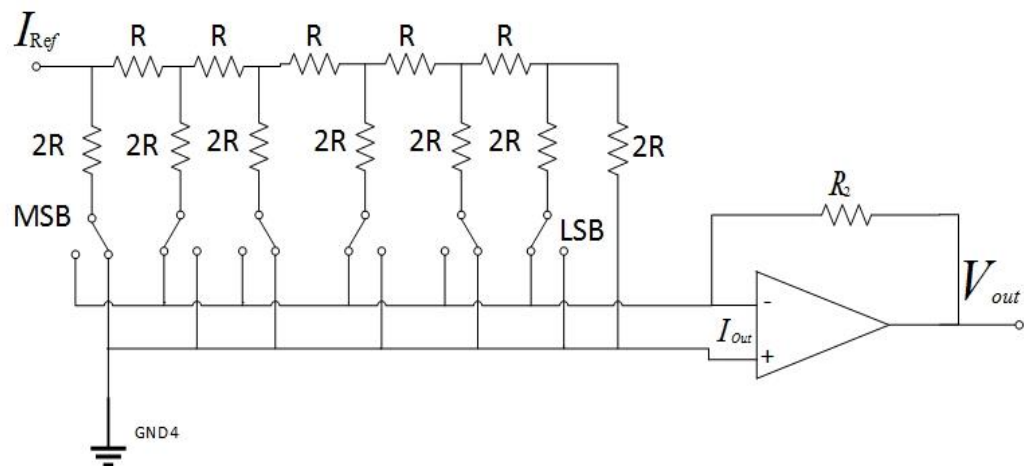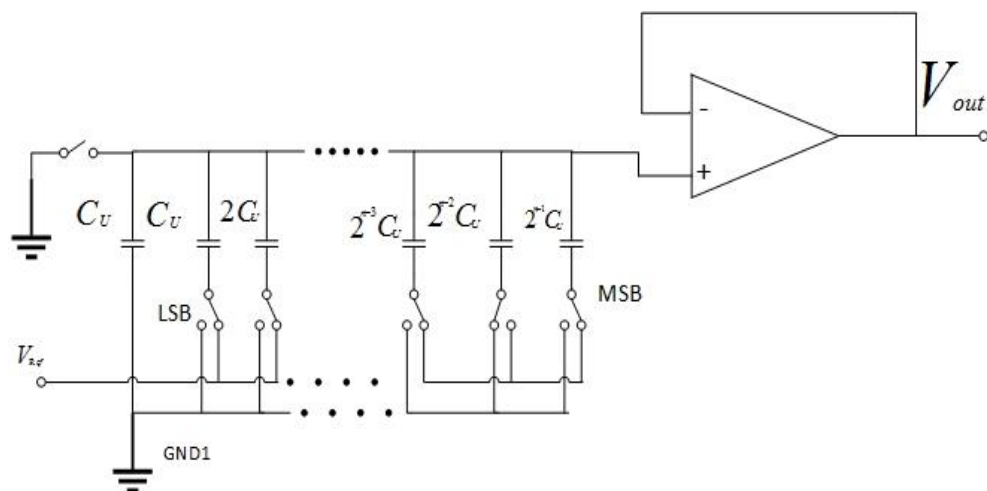
Figure 2- 9 R-2R ladder

Figure 2- 10 Switched capacitor

3. QUADRATURE MODULATOR

In this chapter, the concept and theory of IQ modulation is briefly described.

3.1 Concept of IQ modulation

Amplitude and phase of an RF signal can be modulated to convey the message signal:

$$y = A(t)\cos(w_0 t + \varphi(t)) \tag{2.4}$$

The two components are orthogonal to each other. By varying the amplitude of I and Q components, the phase of the signals changes automatically without changing the phase directly [8]. The I/Q modulator is shown in Fig.3.1. The cross circles are representing the mixers which are used to up-convert or down convert the signals. The converted signals are combined by the combiner at the output.

A carrier signal is applied to the circuit that splits in to two parts. Both parts of carrier signal are 90 degrees separated to each other. One part is modulated by the I signal and other part is modulated by Q signal. The two modulated signals are combined at the output.
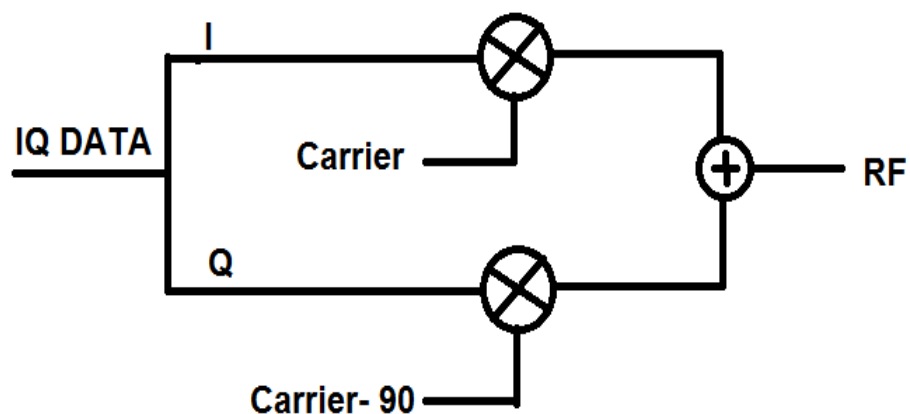

Figure 3- 1 I/Q Modulator

The signal at the output of modulator is given as:

$$cos(\alpha + \beta) = cos(\alpha)cos(\beta) - sin(\alpha)sin(\beta) \tag{2.5}$$

Multiply equation 2.6 by A and put $2\pi f_c t$ in place of α and φ in place of β.

$$Acos(2\pi f_c t + \varphi) = Acos(2\pi f_c t)cos(\varphi) - Asin(2\pi f_c t)sin(\varphi) \qquad (2.6)$$

Now,

$$I = Acos(\varphi) \qquad (2.7)$$

$$Q = Asin(\varphi) \qquad (2.8)$$

$$Acos(2\pi f_c t + \varphi) = Icos(2\pi f_c t) - Qsin(2\pi f_c t) \qquad (2.9)$$

Where, I is the amplitude of in-phase component and Q is the amplitude of quadrature component. The phase and amplitude of modulating carrier signal can be controlled by simply manipulating the amplitudes I and Q signals.

Two commonly used digital modulation communication techniques are quadrature-phase-shift-keying (QPSK) and quadrature-amplitude modulation (QAM). In QPSK modulation, the signal that changes among the states are 90-degree phase separated. In QPSK modulator, two bits are transferred at a time [9]. So there are four states since $2^2 = 4$. The constellation diagram of QPSK is shown in Figure 3.2.
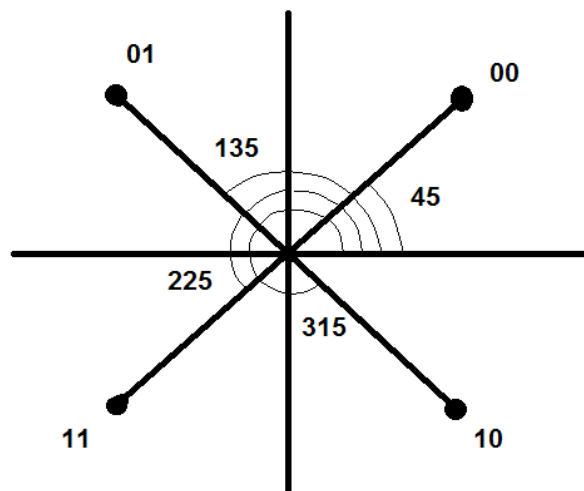

Figure 3- 2 Constellation diagram of QPSK

In 16-QAM techniques, there are four values of I and Q. QAM modulation provides a higher spectral efficiency than QPSK since four bits are transmitted per symbol [10]. The constellation diagram of 16-QAM is shown in Figure 3.3.
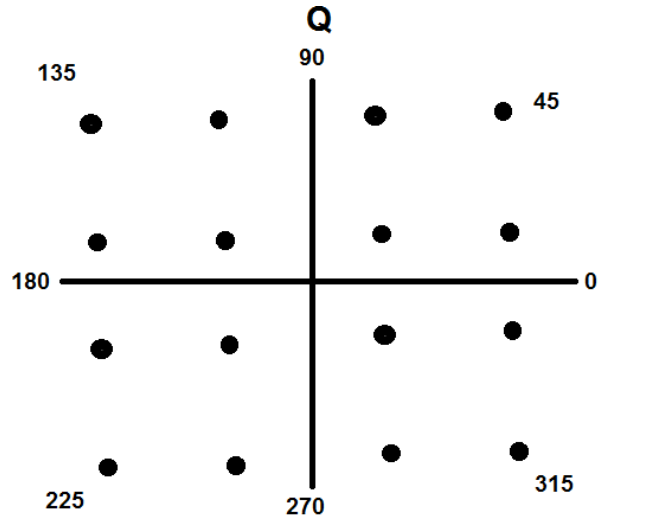
Figure 3- 3 *Constellation diagram of 16-QAM*

3.2 IQ Modulator Non-idealities

Practically, the IQ modulator is not perfectly ideal. In practice, non-idealities of mixers, 90° phase-shifter degrades the performance of IQ modulators. In the next sections, these non-idealities will be described and the error metrics will be introduced.

3.2.1 Non-idealities

Due to the mismatches in the amplitude and phase of I and Q signals, the output of the I/Q modulator changes and creates the unwanted components in the output.

In reality, the output equation (2.10) is represented as:

$$A\cos(2\pi f_c t + \varphi) = L\{g_I * I\cos(2\pi f_c t) - g_Q * Q\sin(2\pi f_c t + \theta)\} \quad (2.10)$$

where g_I and g_Q are the functions of I and Q, θ is the phase error, L is the non-linearity of the modulator [11]. The final equation when expanded, contains three different errors: DC offset, LO leakage and unwanted signal.

The LO leakage can be represented in the equation (2.12)

$$LO_{LEAKAGE} = 10\log\left(\frac{P_{LO}}{P_{SIGNAL}}\right) \quad (2.11)$$

where P_{LO} is local oscillator power and P_{SIGNAL} is RF signal power.

3.2.2 EVM

The concept of EVM (Error Vector Magnitude) is described as follows. When the signal is transmitted by the transmitter or received by the receiver, it has ideally well placed constellation points at their respective position. But practically it's not possible to achieve the perfectly placed constellation points. This is because of the error which arises from the phase inaccuracies between the I and Q components, amplitude mismatch, LO leakage and various distortions present in the transmitter. As a result, the constellation points shift from their ideal positions to some other unusual location by the imperfections. EVM is defined as the root mean square of reference power and error vector power relation [12, 13]. The relation is shown in the equation (2.13).

$$EVM(dB) = 10\log_{10}\left(\frac{P_{error}}{P_{reference}}\right) \qquad (2.12)$$

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} \times 100\% \qquad (2.13)$$

$$P_{error} = actual\ value - reference\ value \qquad (2.14)$$

Where, P_{error} is error vector power and $P_{reference}$ is reference signal power.
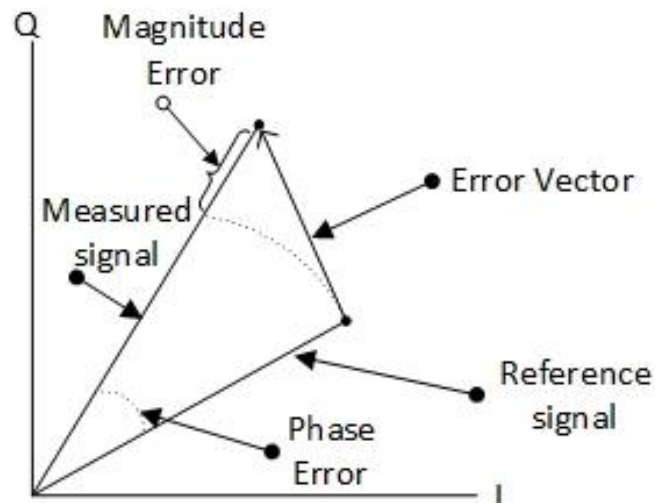
The EVM is shown in the figure 3.4.

Figure 3- 4 Error Vector Magnitude

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3.2.3 Distortion

The transmitter suffers from amplitude mismatches, 90° phase inaccuracy between t I and Q components and non- linearity of the power amplifier that leads to the distortion. The distortion of the transmitter is expressed by the ACPR (Adjacent Channel Power Ratio) that is used to measure the power in the adjacent channel. It is the ratio of power in the adjacent channels to the rms power in the main channel.

$$ACPR = \frac{Power\ in\ the\ adjacent\ channels}{rms\ power\ in\ the\ trasmitter\ channel} \tag{2.15}$$

It is an important metric which is used to measure the power spectral re-growth of the transmitter, since power amplifier is the last part of the transmitter and it introduces non-linearity in the system. It is also called as ACLR (Adjacent Channel Leakage Ratio).

3.3 Mixer Figure of Merit

The mixer specification is described as following.

Conversion gain

Conversion gain is the measure of power gain or voltage gain from IF to RF or RF to IF ports. The conversion gain of the mixer can be maximized by having a proper conjugate matching at IF, RF and LO ports. Active mixers give conversion gain whereas, passive mixer gives conversion loss [14, 15].

$$V_{conversion\ gain} = \frac{V_{rms}\ (at\ IF\ signal)}{V_{rms}\ (at\ RF\ signal)}$$

$$P_{conversion\ gain} = \frac{P_{RF}\ (at\ load)}{P_{RF(rms)}\ (at\ source)}$$

Linearity

The linearity of mixer is measured by 1dB compression point P_{1dB} and third order inter-cept point at the input, IIP3. Generally, passive mixers exhibit high linearity.

Noise figure

Noise figure of mixer is represented by SNR ratio between the IF and RF output and it is also calculated from the following expression:

$$N_0 = KT\Delta f(G_1 + G_2) + N_a \tag{2.16}$$

Where, G_1 and G_2 are the conversion gains, $N_i = KT\Delta f$ is the input noise power and N_a is the total noise power.

Isolation

Isolation is defined as the measure of amount of power leaks or feedthroughs from one port to another port. If isolation of mixer is not proper then it will introduce EVM, DNL and INL errors at the output. Isolation differs from topology to topology.

- LO to RF leakage causes self-mixing.
- RF to LO feedthrough allows interferer to in RF signal to interact with the LO.
- LO to IF feedthrough produce desensitization.
- RF to IF feedthrough.

4. CONCEPT AND FUNDAMENTALS OF RF-DAC

4.1 Background

The RF-DAC is a combination of mixer and DAC into one structure. It generates modulated RF signal directly from digital base-band data.

Advantages of RF-DAC

The RF-DAC has several advantages over conventional D/A converter.

- The main advantage of RF-DAC is that the mixer and DACs are integrated into one circuit. This enables reduced chip area and a lower power consumption.
- All the transistor of RF-DAC work as switches without any linearity constraints. Since the linearity of RF-DAC is mainly determined by the resolution of the converter.
- As the digital signal is directly applied to the switches therefore it is immune to the DC-offsets in the baseband signal [16].

4.2 Basic architectures of RF-DAC

The RF-DAC was first introduced by Luschas *et al*. shown in Figure 4-1 [1].
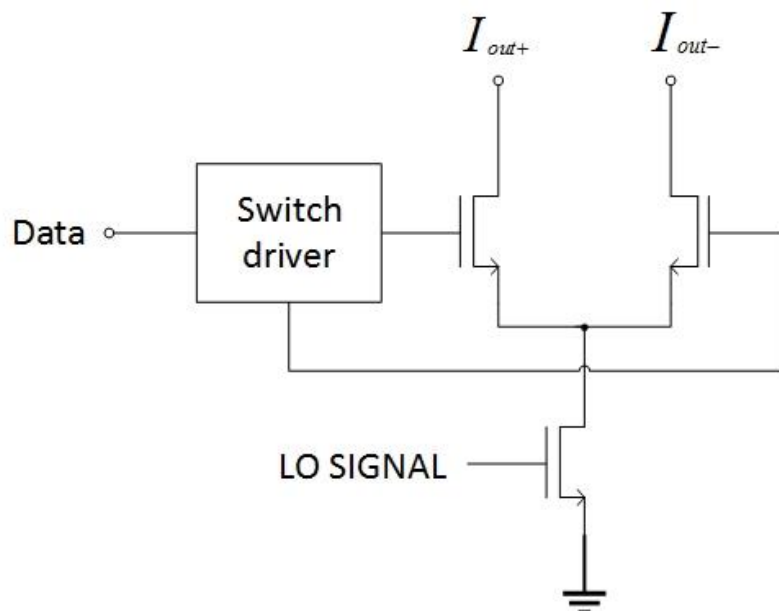

Figure 4- 1 *RF-DAC implemented by Luschas et. al.*

Here in the Figure 4-1 LO signal is applied to the tail current source and data signal is applied to the differential transistor pair. This architecture is same like single conversion mixer but LO and data signals are interchanged.

The disadvantage of this architecture is, it introduces unwanted signals at other frequencies than f_{LO}, usually at DC. The phase of data signals and LO signal must be synchronized with each other to avoid the glitches.

The problem of unwanted signal appearing at the DC in the Luschas *et al.* architecture [1] is overcame by the double balanced architecture of RF-DAC developed by the Eloranta *et al.* [17]. By having the double balanced in nature, the architecture removes the components at DC and the even order harmonics. It is closely related to the double balanced Gilbert cell but the position of LO and data signals are interchanged. In this architecture, the data signal is applied to the differential quad transistor preceded by the LO signal applied to differential transistor pair.
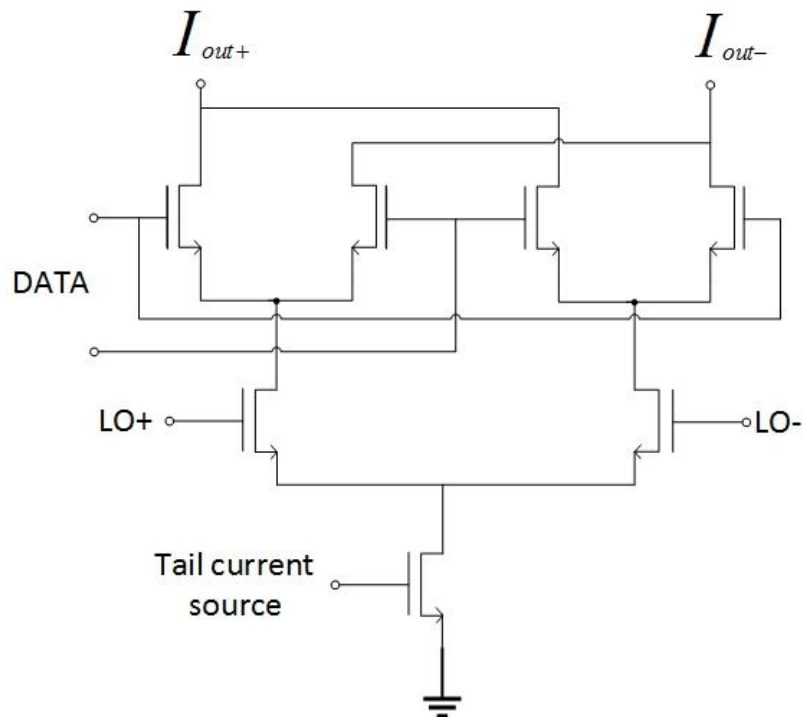

Figure 4- 2 RF-DAC by Eloranta et. al.

The combined output is obtained by summing the output of all the conversion cells. Ideally the linearity of signal is defined by the resolution of the converter.

5. COMPONENTS OF I/Q MODULATOR

5.1 Double balanced Gilbert cell

Double balanced Gilbert mixer is the most popular topology that is being used in the up conversion or down conversion of frequency circuits. It provides the perfect isolation between LO-IF, IF-LO and RF-LO. Basically, it consists of two cross coupled differential transistor and one transconductance stage that increases gain of signal.
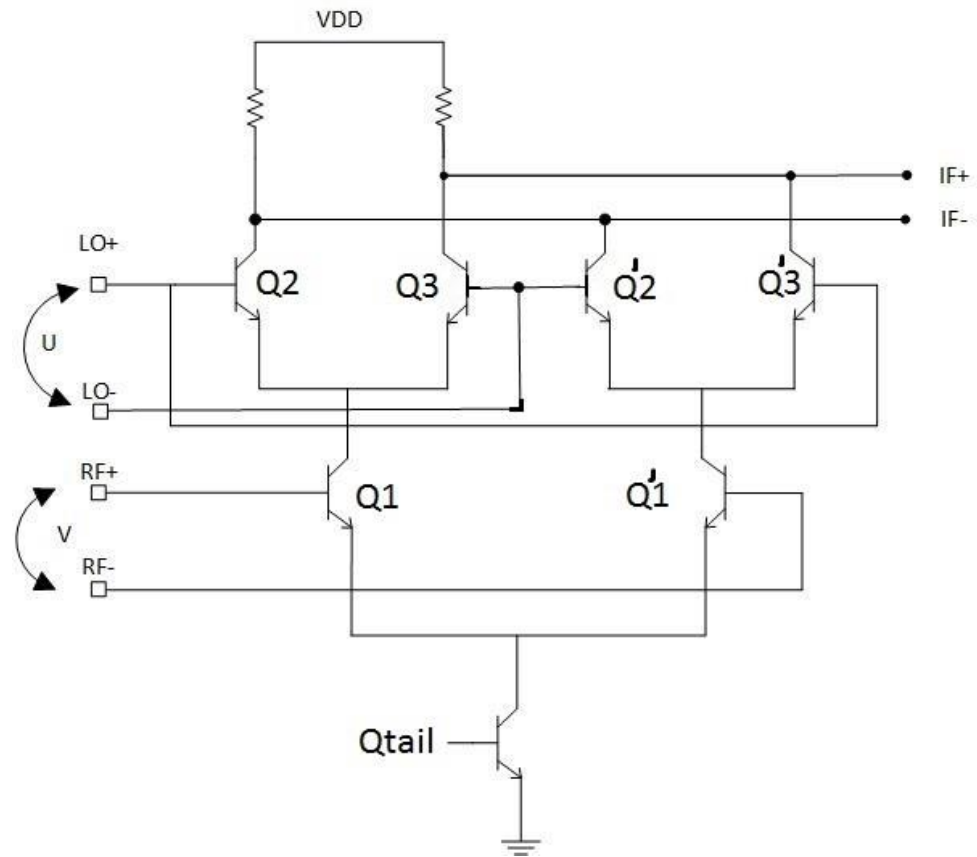

Figure 5- 1 *Double balanced Gilbert cell*

According to simple exponential relation between collector current and base- emitter voltage, the differential current between the transistor Q_2 and Q_3 can be figure out and in the same way the current between Q_2' and Q_3' can be figure out [15].

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \text{ and } V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \qquad (2.17)$$

Let's suppose U is the voltage difference between Q_2 and Q_3 and we know,

$I_{Q1} = I_{Q2} + I_{Q3}$. The difference of the current can be derived as follows,

$$\Delta I = I_{Q2} - I_{Q3} = I_S \left[\exp\left(\frac{V_{BE2}}{V_T}\right) - \exp\left(\frac{V_{BE3}}{V_T}\right) \right]$$
$$= I_S \exp\left(\frac{V_{BE3}}{V_T}\right) \left[\exp\left(\frac{U}{V_T}\right) - 1 \right] \qquad (2.18)$$

$$I_{Q1} = I_{Q2} + I_{Q3} = I_S \left[\exp\left(\frac{V_{BE2}}{V_T}\right) + \exp\left(\frac{V_{BE3}}{V_T}\right) \right]$$
$$= I_S \exp\left(\frac{V_{BE3}}{V_T}\right) \left[\exp\left(\frac{U}{V_T}\right) - 1 \right] \qquad (2.19)$$

From equation (2.21) and (2.22),

$$\Delta I = I_{Q2} - I_{Q3} = I_{Q1} \tanh\left(\frac{U}{2V_T}\right) \qquad (2.20)$$

Similarly

$$\Delta I = I_{Q'2} - I_{Q'3} = I_{Q'1} \tanh\left(\frac{U}{2V_T}\right) \qquad (2.21)$$

And

$$\Delta I_{IF} = I_{Q2} - I_{Q3} - I_{Q'2} - I_{Q'3} = (I_{Q1} - I_{Q'1}) \times \tanh\left(\frac{U}{2V_T}\right) \qquad (2.22)$$

The same expression for the transconductance transistor pair,

$$(I_{Q1} - I_{Q'1}) \times \tanh\left(\frac{V}{2V_T}\right) \qquad (2.23)$$

Now, for the current at IF, the expression can be obtained by putting equation (2.25) in to (2.24)

$$v_{IF} = -R_L I_{TAIL} \tanh\left(\frac{V}{2V_T}\right) \tanh\left(\frac{U}{2V_T}\right) \qquad (2.24)$$

For small amplitudes,

$$v_{IF} = -R_L I_{TAIL} V U \qquad (2.25)$$

As seen from (2.28), the output of a Gilbert cell is multiplication of the two inputs.

5.2   Quadrature (90°) hybrid coupler

Quadrature hybrid couplers are four terminal device illustrated in Figure 5-1. The incident power signal splits in to two at output ports. Here, the power is incident on port 1 and splits equally at port 2 and 3 and are 90 degrees out of phase. All the reflections are sent to the isolated port 4, therefore no reflected power go back to input. The signals at the output port are attenuated by 3 dB, it means 50% of power is lost. In addition to splitting, they can also combine power signal if the isolation between the port is high enough.

Here, the hybrid coupler illustrated in Figure 5-1 is realized by the lumped elements which are ideal capacitors and inductors (lossless). Realization of coupler by lumped elements provides wider bandwidth, low insertion loss and is very suitable for MMIC applications.
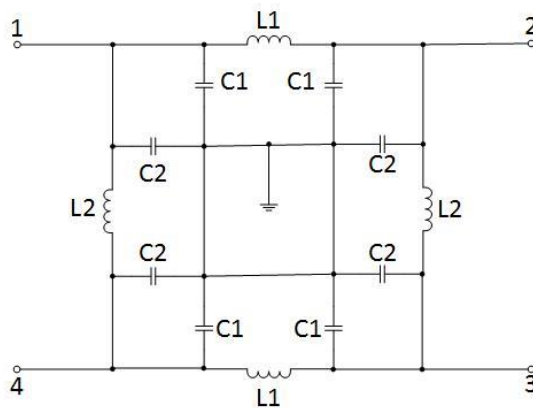
Figure 5- 2 Quadrature hybrid coupler

An example of distributed elements coupler is shown in Figure 5-3. The coupler has two transmission lines i.e. vertical and horizontal, both transmission lines has quarter wave-length.
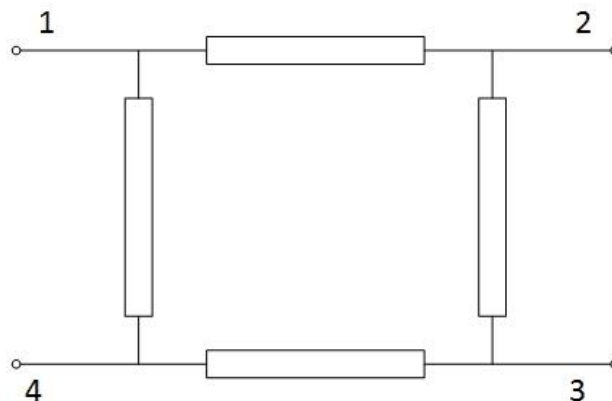
Figure 5- 3 Branch line coupler

The impedance of vertical and horizontal transmission lines is $Z = Z_0$ and $Z = \frac{Z_0}{\sqrt{2}}$ respectively, whereas Z_0 is characteristic impedance. It is preferred to realize transmission lines with lumped component to save area in MMIC realizations. For the MMICs, the hybrid coupler is realized with lumped elements using π or T equivalent network. In the lumped element configuration, each transmission line is represented by the equivalent π network. The values of lumped elements can be calculated by using the ABCD matrix.

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{bmatrix} \cos\theta & jZ_r \sin\theta \\ j\frac{1}{Z_r}\sin\theta & \cos\theta \end{bmatrix} \tag{2.26}$$

When $\theta = 90°$, the values of lumped element can be calculated as following;

$$L_1 = \frac{Z_r}{\omega_0}, L_2 = \frac{Z_p}{\omega_0}, C_1 = \frac{1}{Z_r\omega_0}, C_2 = \frac{1}{Z_p\omega_0}$$

Where, Z_r represents the impedance of horizontal transmission line and Z_p represents the impedance of vertical transmission line.

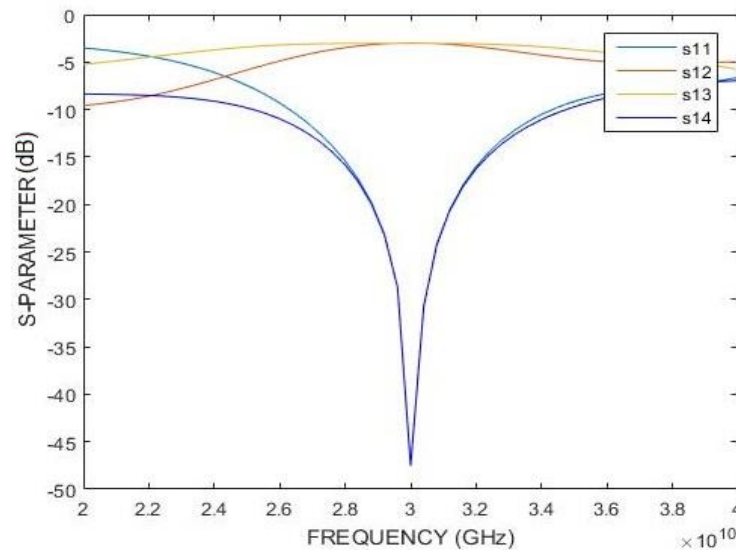The s-parameter measurements are given in the Figure 5-2.

Figure 5- 4 *S-parameter of hybrid coupler*

The magnitude of s12 and s13 are very close to -3dB, -2.993dB respectively. The phase difference between s12 and s13 is also 90 degrees.

5.3   Wilkinson power combiner/divider

Wilkinson power combiner is a three port network that is lossless when the outputs are completely matched. The Wilkinson circuit is used for both combining and splitting signals. The output is the sum of the in-phase input signals. The Wilkinson combiner has good isolation between the ports.
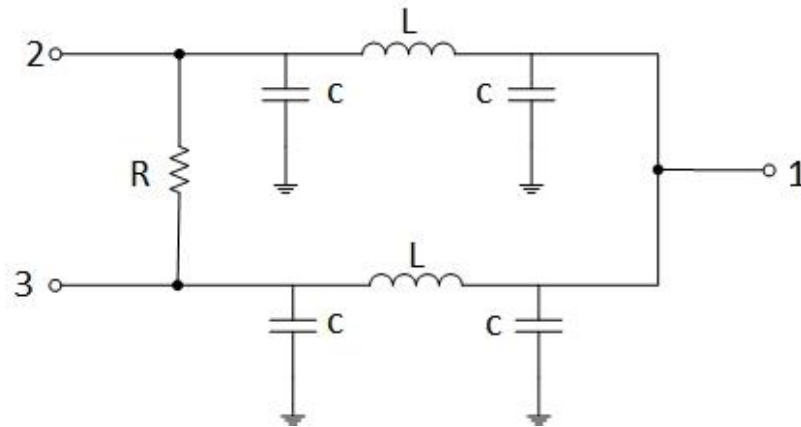

Figure 5- 5 *Wilkinson power combiner*

The characteristic impedance of π network in the branches of combiner is $\sqrt{2}Z_0$, and the isolator resistor is $2Z_0$. The two transmission line is realized by using the lumped elements. Lumped elements are easy to integrate and gives wider bandwidth. Since the input signals are 90 degrees out of phase in an IQ modulator, half of the power is wasted in the isolation resistor.

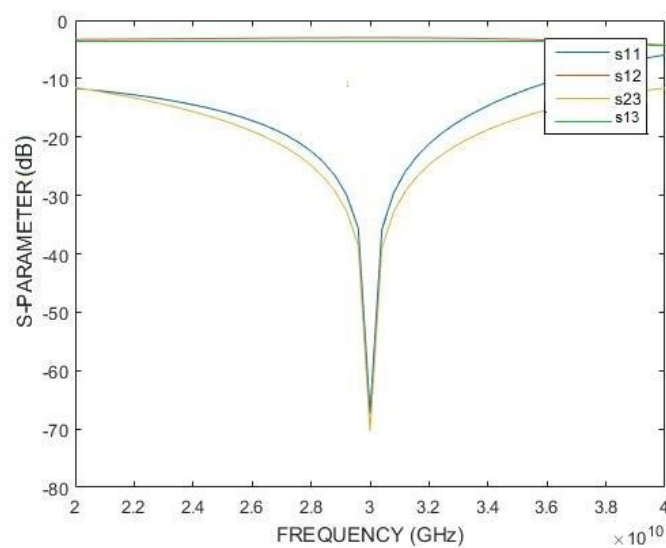The s-parameter simulation of three port device is shown in Figure 5-4.

Figure 5- 6 *S-parameter of Wilkinson power combiner*

For equal split, Wilkinson should half the power to each of the output port. Therefore, s12 and s13 are equal to -3dB. The ideal component simulation is very close to the theory giving s12=s13= -3.01dB.

5.4 BALUN

BALUN is an electronic device that converts single-ended signals to differential signals, vice versa. Baluns are widely used in for instance mixer and push-pull amplifier designs. Basically, baluns are used to generate 180-degree phase shift signals at the output.

Baluns can be classified in to two categories; active and passive baluns. Passive baluns are further classified in to two; lumped element balun and distributed baluns. L-C Balun is shown in the given Figure 5-5. In the proposed I/Q RF-DAC circuit, two baluns are used one at the input and other at output.
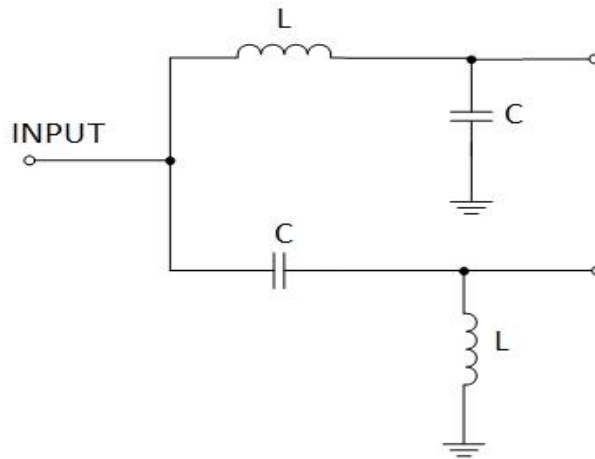

Figure 5- 7 BALUN

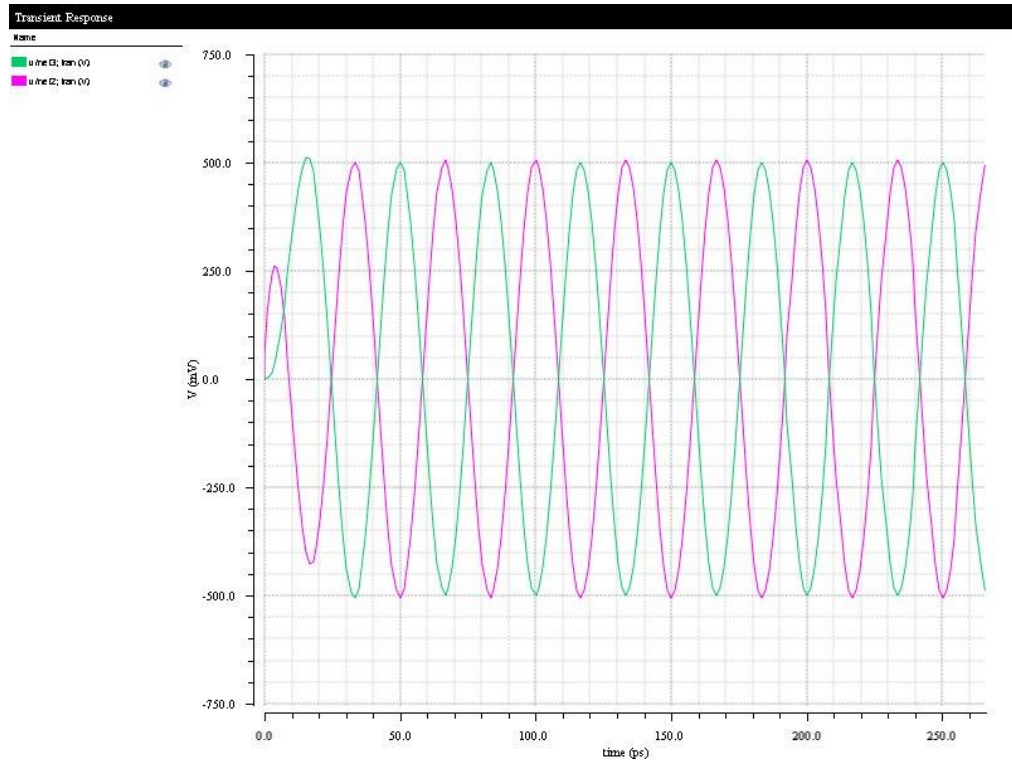The phase difference between the two outputs of BALUN is 180 degrees to each other given in the Figure 5-6.

***Figure 5- 8* 180^0** *phase difference between two outputs*

6. CIRCUIT DESIGN AND SIMULATIONS

In this chapter the complete implementation of the four bit 30 GHz RF-DAC based I/Q modulator is described. As this thesis is more concerned towards the RF domain, only the analog/RF part of circuit is implemented. The circuit is implemented in Cadence environment and 130 nm BiCMOS technology is used. The complete block diagram is given in the Figure 6-1. There are four sub-circuits: input and output BALUN, differential branch line coupler, 15 conversion cell stacked in to one box for the two quadrant RF-DACs I/Q vector modulator combined and a differential Wilkinson power combiner.

The main function of differential branch line coupler is to feed differential signal to I and Q quadrant. The BALUN has a single-ended input impedance of 50 Ω and a differential output impedance of 100 Ω. Differential branch line coupler, BALUN and Wilkinson combiner has already been described in detail in Chapter 5.
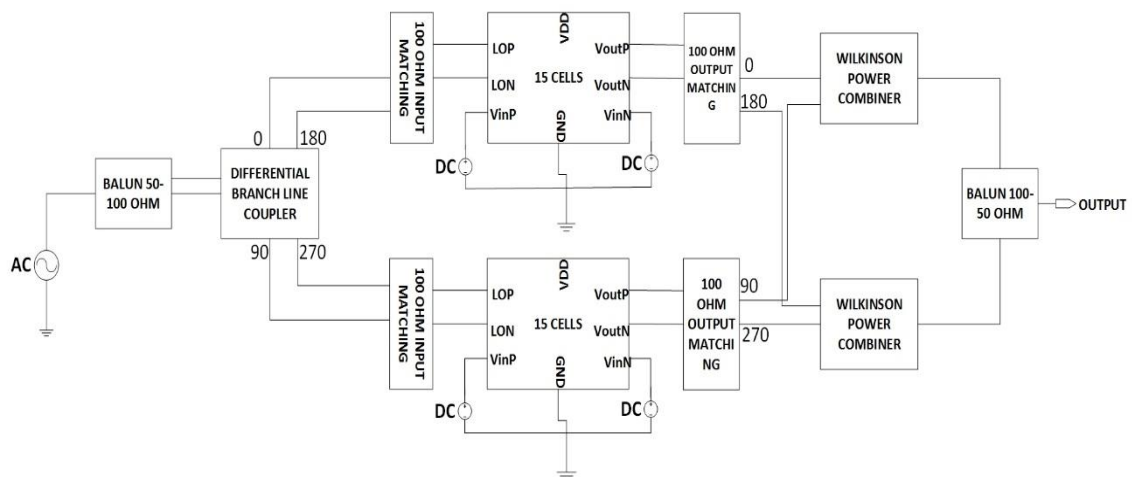

Figure 6- 1 Block diagram of I/Q modulator

In order to remove the glitches while switching the output from one level to another level, the circuit is designed for Thermometer coding logic. The proposed I/Q modulator is designed for four bits; therefore, it gives 15 output levels. Thus, 15 such RF- DAC conversion cells are designed and arranged in parallel.

For the simplicity, the circuit is described below in detail step by step. The different building blocks are added step by step and simulations are performed. The circuit starts from RF-DAC unit cell, arrangement of these 15 cells in parallel. Arranging of two quadrant RF-DACs that form the I/Q modulator with combined Wilkinson power combiner. The complete I/Q modulator by combining input and output BALUN is illustrated in Figure 6-1. In section 6.7, the 15 bits are turned ON from 1 to 15 in the increasing order and the effect on power added efficiency and output power is observed.

6.1 RF-DAC unit cell

The RF-DAC unit conversion cell is shown in Figure 6-2. The RF-DAC consists of several parallel unit cells. The output is controlled by switching the unit cells on or off according to the applied digital input.
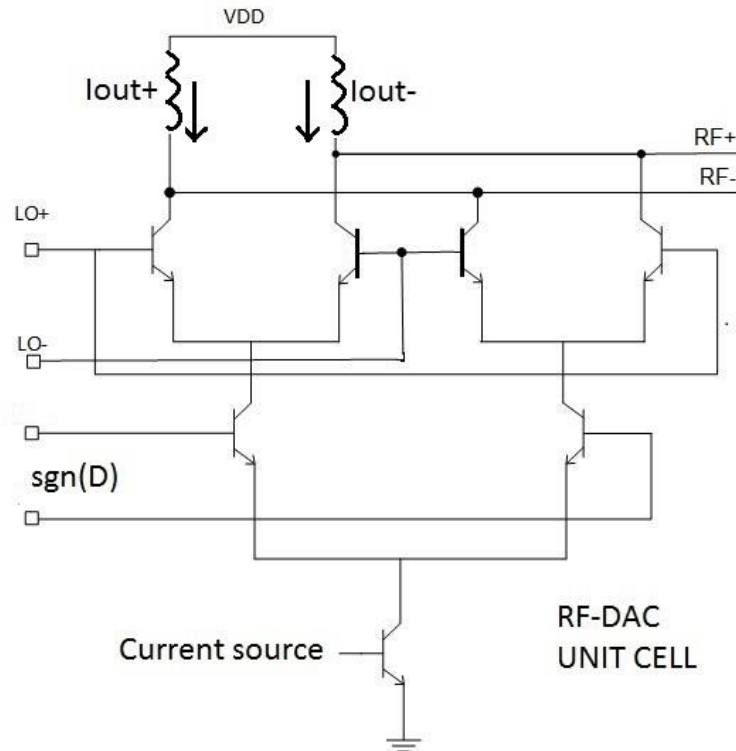

Figure 6- 2 RF-DAC unit cell

In the given Figure 6-2, the differential local oscillator signal of 30 GHz is applied to the two differential pair of the transistor. These quad transistors are preceded by one differential pair where the digital bits are applied. Since the digital circuitry is omitted, differential DC voltage of 100 mV is applied. All the transistors are working as high speed switches except tail current source, so all the transistors are biased in the active region.

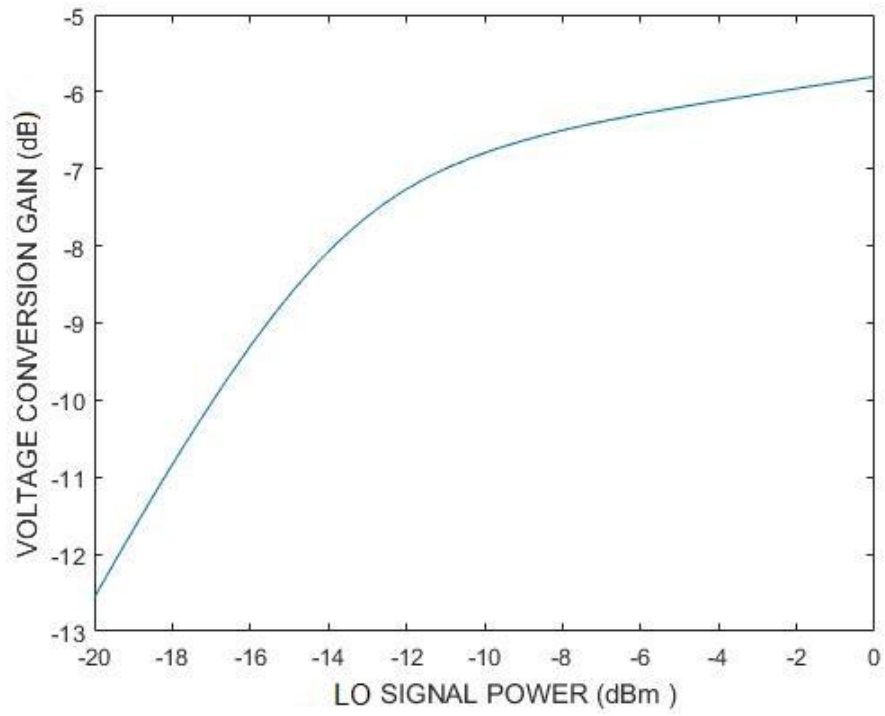Simulations of voltage conversion gain and output power is illustrated in Figure 6-3, 6-4.
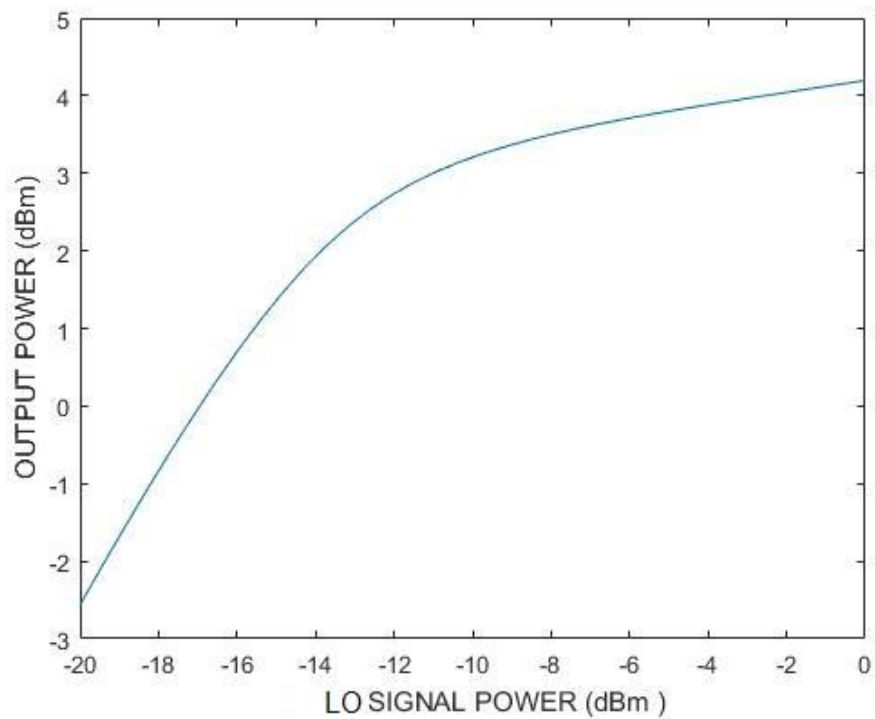
Figure 6- 3 *Voltage conversion gain*

Figure 6- 4 *Output power vs input power*

6.2 Arrangement of cells

A thermometer coder is used that gives $2^N - 1$ digital thermometer bits to represent N digital input bits. So for four bits it generates 15 outputs, therefore 15 conversion cells are used. The arrangement of cells is illustrated in Figure 6-5. All the cells are organized in parallel and their output is summed at the RF port.
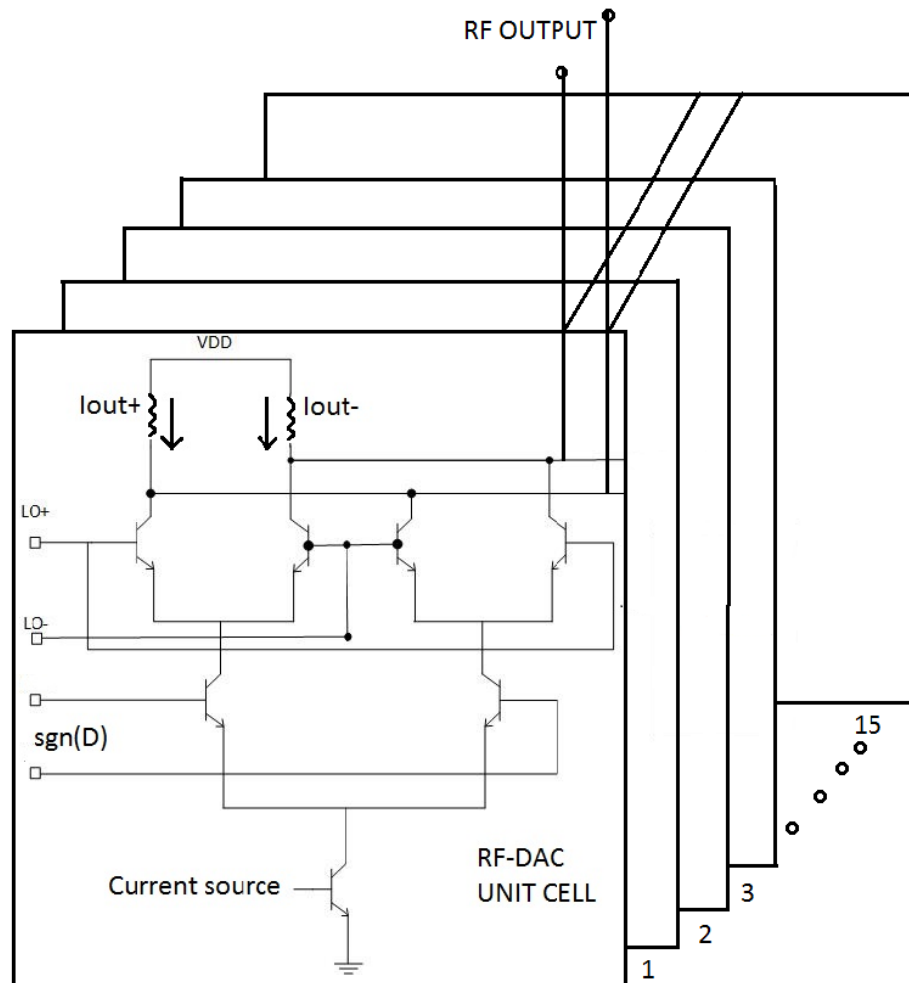

Figure 6- 5 Arrangement of 15 RF-DAC cells in parallel

The schematic of test bench for all the 15 cells arranged in parallel is illustrated in Figure 6-6. The LOP and LON are the 30 GHz differential local oscillator signal that are 180 degrees out of phase. The differential output is collected at terminal VoutP and VoutN. VinP and VinN are differential DC voltage. Hence from now this test bench circuit is used for further stages of circuit.
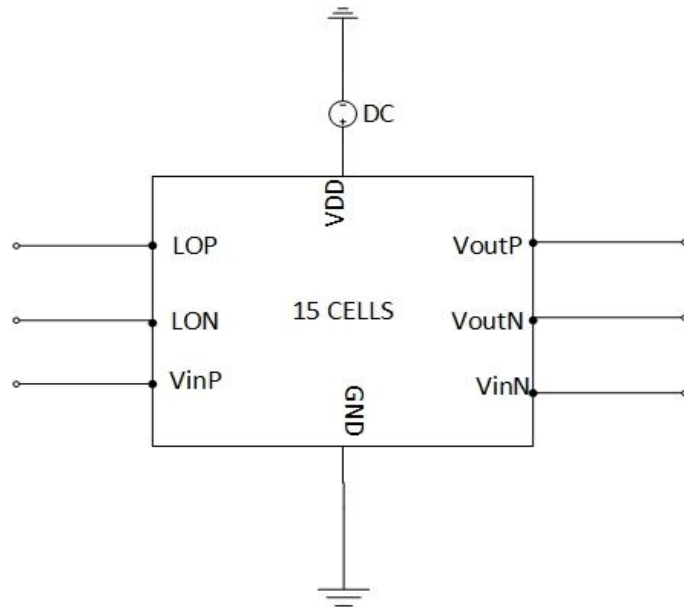
Figure 6- 6 Test bench of 15 RF-DAC unit cells

6.3 Input and output matching

The LO input port and RF output port are matched to differential 100 Ω. The basic idea behind the matching is the load pull analysis of one RF-DAC unit cell to get the optimum impedance at which maximum performance is achieved. So the optimum impedance for the 15 cells arranged in parallel is the optimum impedance of one RF-DAC unit cell divided by 15. The output load is matched to 100 Ω load (RL=100 Ω) and in the same way the input is 100 Ω conjugate matched. In the given Figure 6-7, the differential 100 matching is shown at output and input by using the lumped elements.
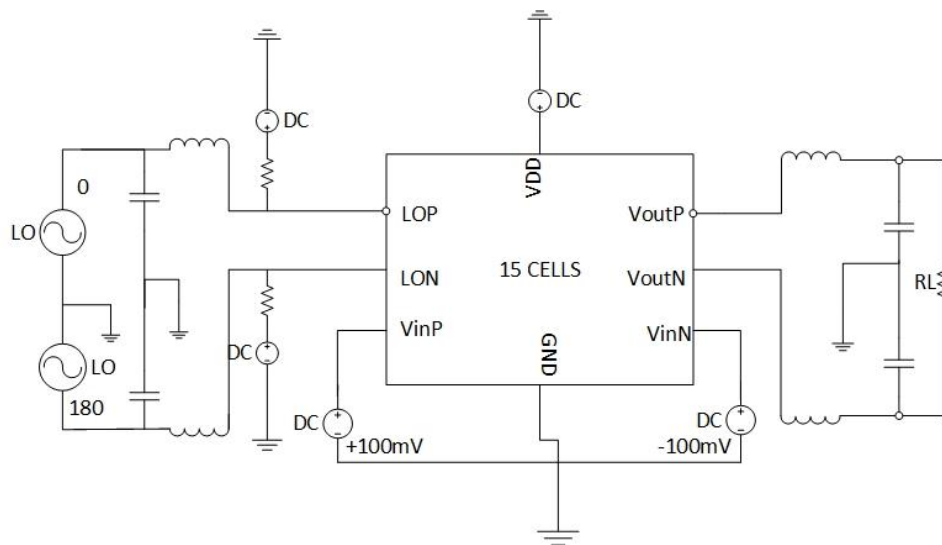

Figure 6- 7 100 Ohm differential input and output conjugate matching

6.4 IQ RF-DAC arrangement

The combination of two RF-DACs in parallel makes the I/Q vector modulator. The in phase and quadrature part combined with Wilkinson power combiner is illustrated in Figure 6-8.
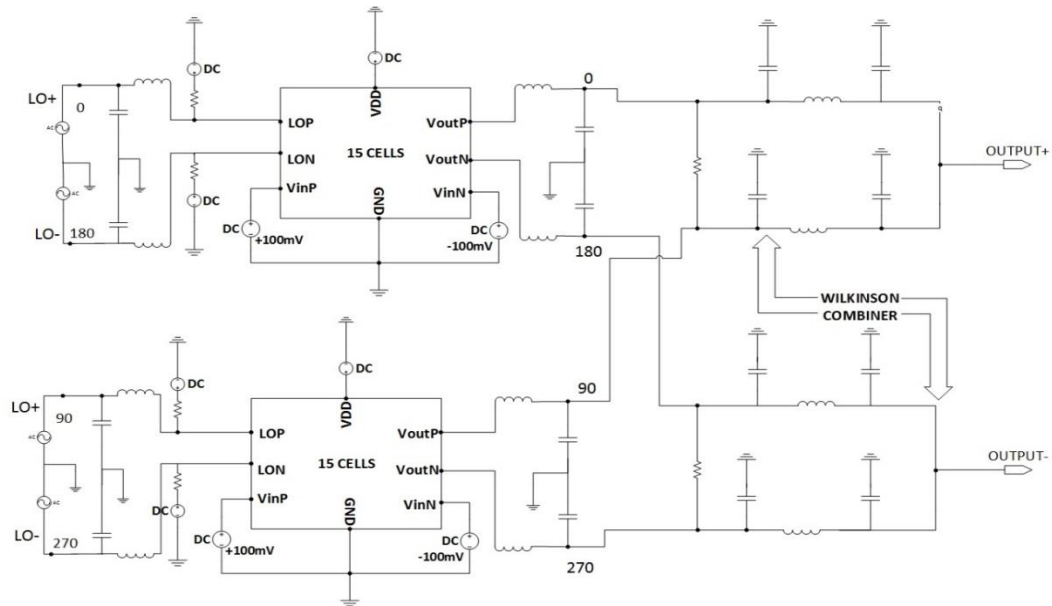

Figure 6- 8 Combination of test bench in I and Q part with Wilkinson power combiner

6.5 Combining of Differential branch line coupler

At this stage, the differential branch line coupler is added to the circuit illustrated in Figure 6-10. Differential branch line coupler is basically constructed by using two-single ended branch line couplers. Signals in port 2 and port 3 are 90 degrees out of phase. Port 4 is the isolated port which is terminated with 100 Ω.
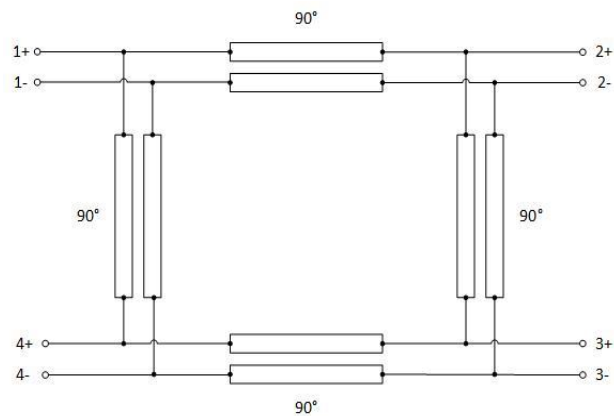
Differential branch line coupler is shown in Figure 6-9.

Figure 6- 9 Differential branch line coupler

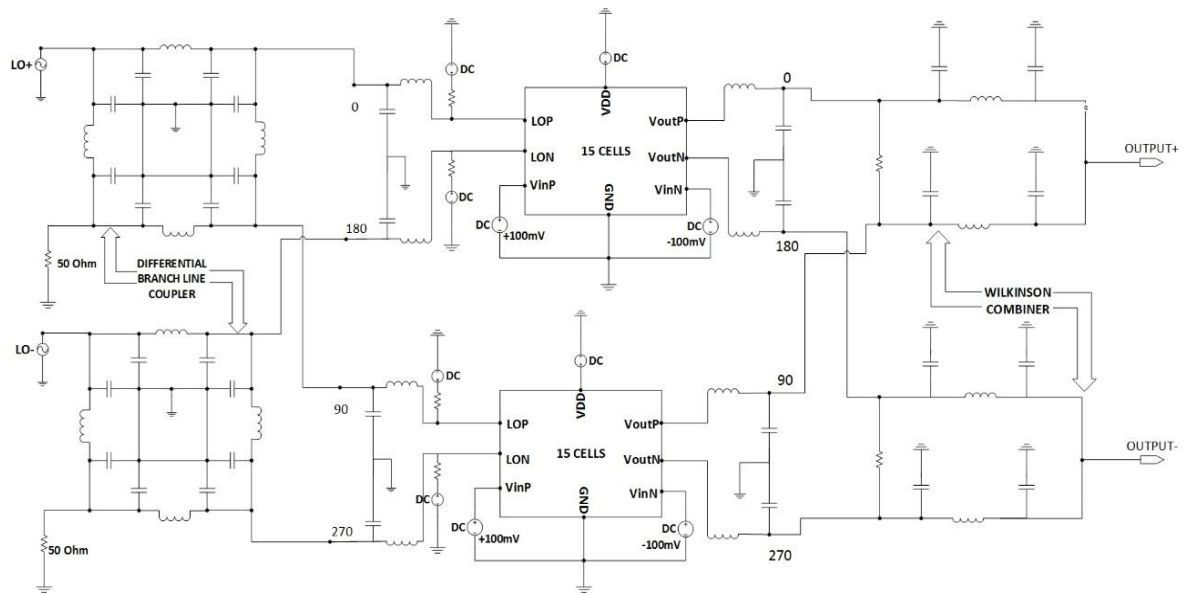Port 4 is isolated, port 2 and 3 are 90 phase difference signal and are 100 Ω matched.

Figure 6- 10 *Addition of differential branch line coupler*
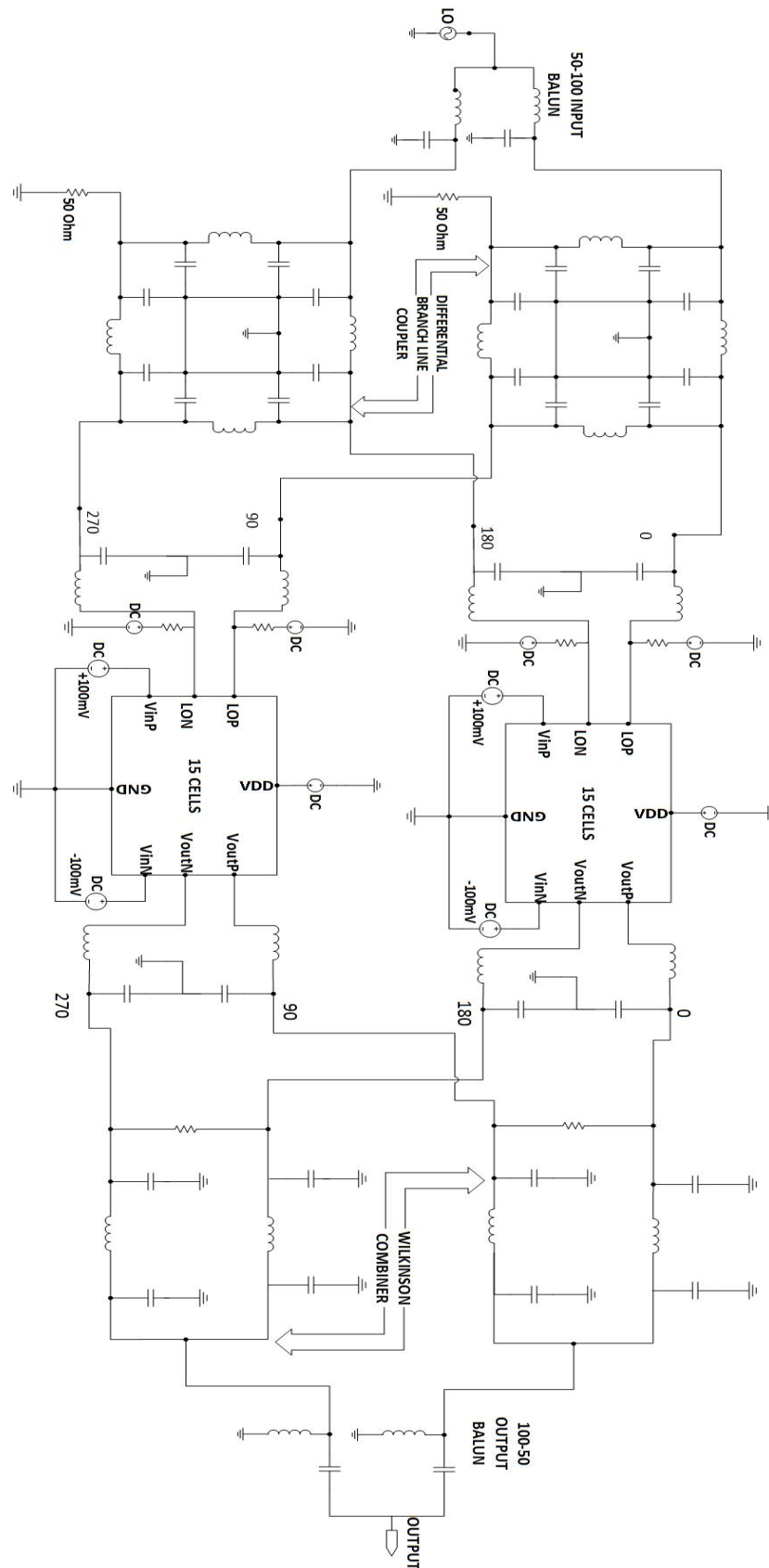
6.6 Complete IQ modulator

Figure 6- 11 A 4-bit RF-DAC based I/Q modulator

The complete circuit of I/Q modulator is illustrated in Figure 6-11. At this stage balun circuit is added to both input and output. Several simulations have been performed which are shown in the given figures.

6.6.1 Simulations

PAE

The horizontal axis represents the LO input power and vertical axis represents PAE (Power Added Efficiency). In the given Figure 6-12, around at 5 dBm input power, the efficiency began to saturate. At 5 dBm input signal power, the observed efficiency is 23%.
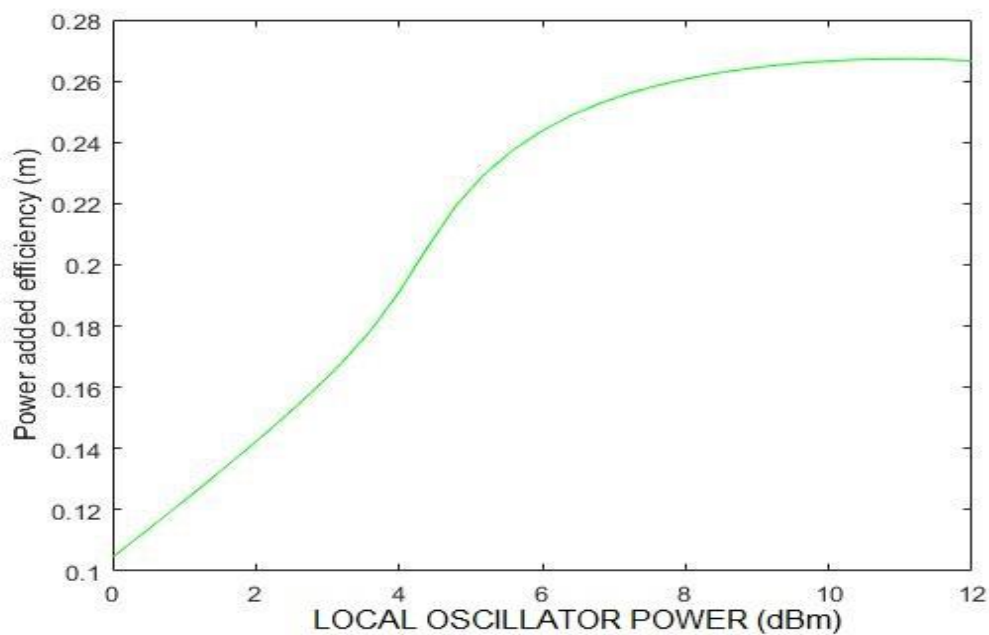

Figure 6- 12 *Power added efficiency vs input power*

The individual RF-DACs have two times higher efficiency but 3 dB power is lost in the isolator resistor of Wilkinson power combiner.

Gain

In the given Figure 6-13, observed gain is 18-dB at 5 dBm input signal power. The formula of the gain is shown in equation 2.30.

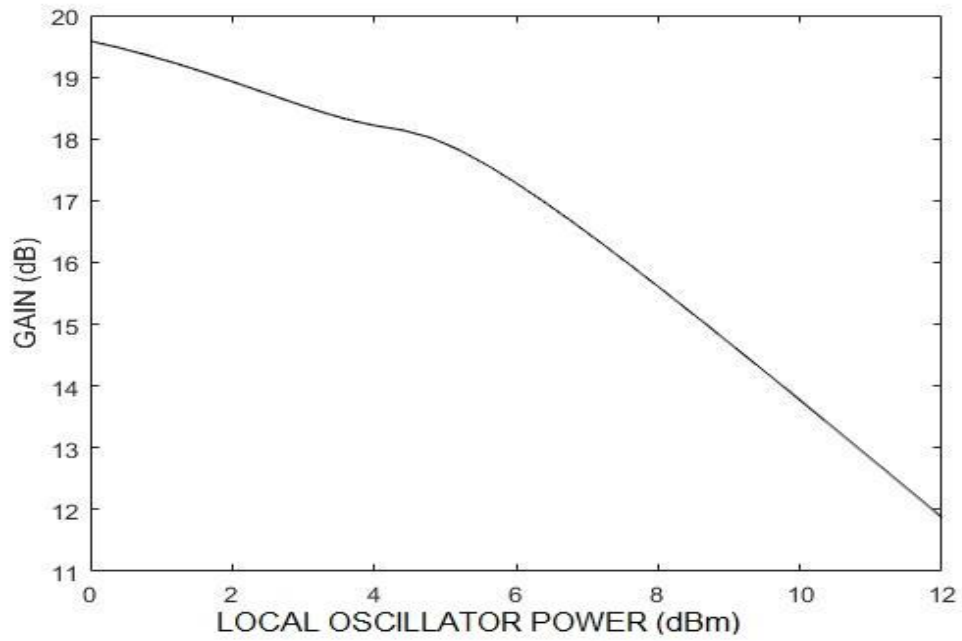$$Gain = db10\left(\frac{Output\ power}{Input\ power}\right) \tag{2.27}$$

Figure 6- 13 *Gain vs input power*

Output power

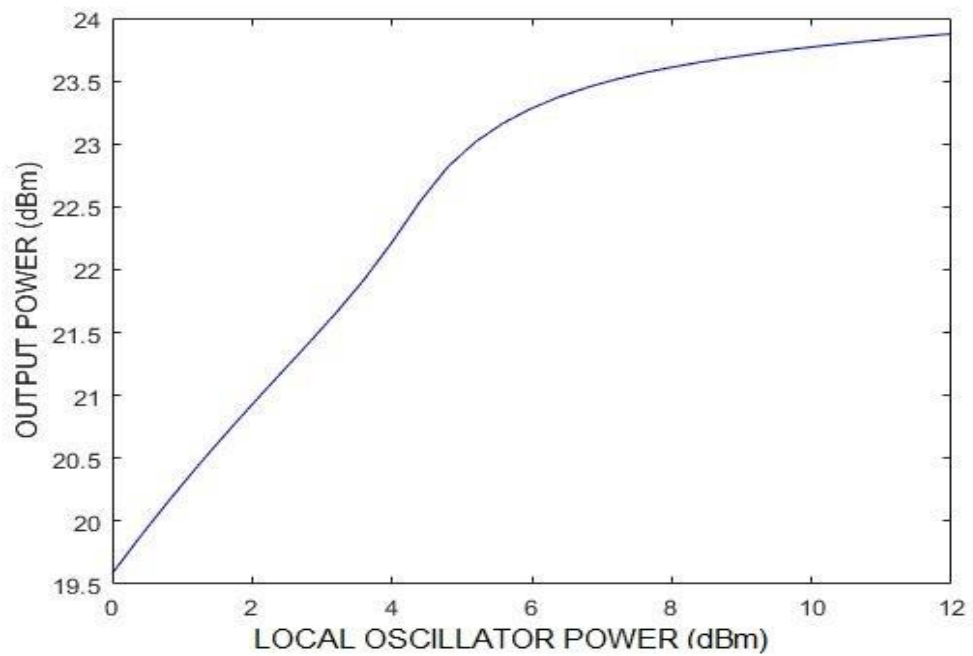In the given Figure 6-14, the total output power was estimated around 23 dBm at 5 dBm input signal power.

Figure 6- 14 *Output power vs LO input power*

DC Power consumption

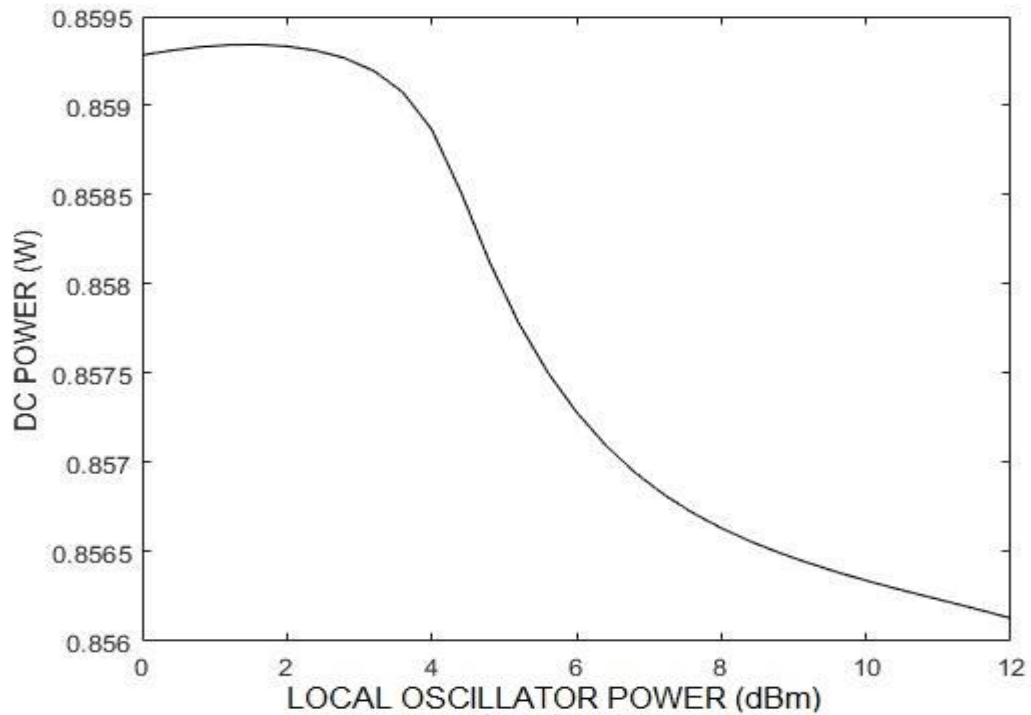In the given Figure 6-15, the power consumption is 859-mW at 5 dBm input signal power.

Figure 6- 15 DC power consumption

Bandwidth

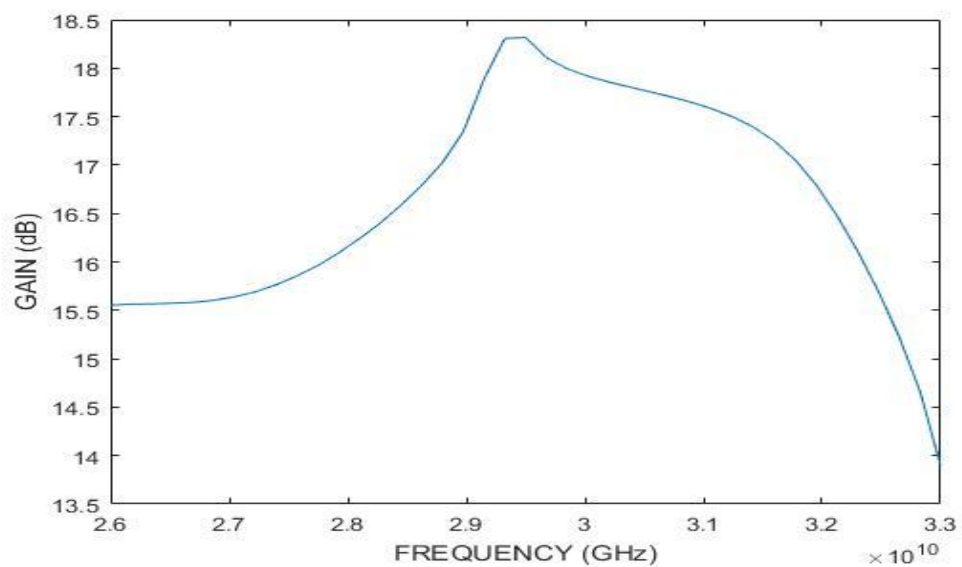The bandwidth of circuit is around 6 GHz.

Figure 6- 16 Gain bandwidth of circuit

6.7 Performance versus number of ON bits

In the given Figure 6-17, the arrangement of RF-DAC of 15 cells in both I and Q part is shown. The idea of this arrangement is to observe the effect on PAE (Power Added Efficiency), output power and relation of PAE vs output power as the number of bits turned ON from 1 to 15 bits.
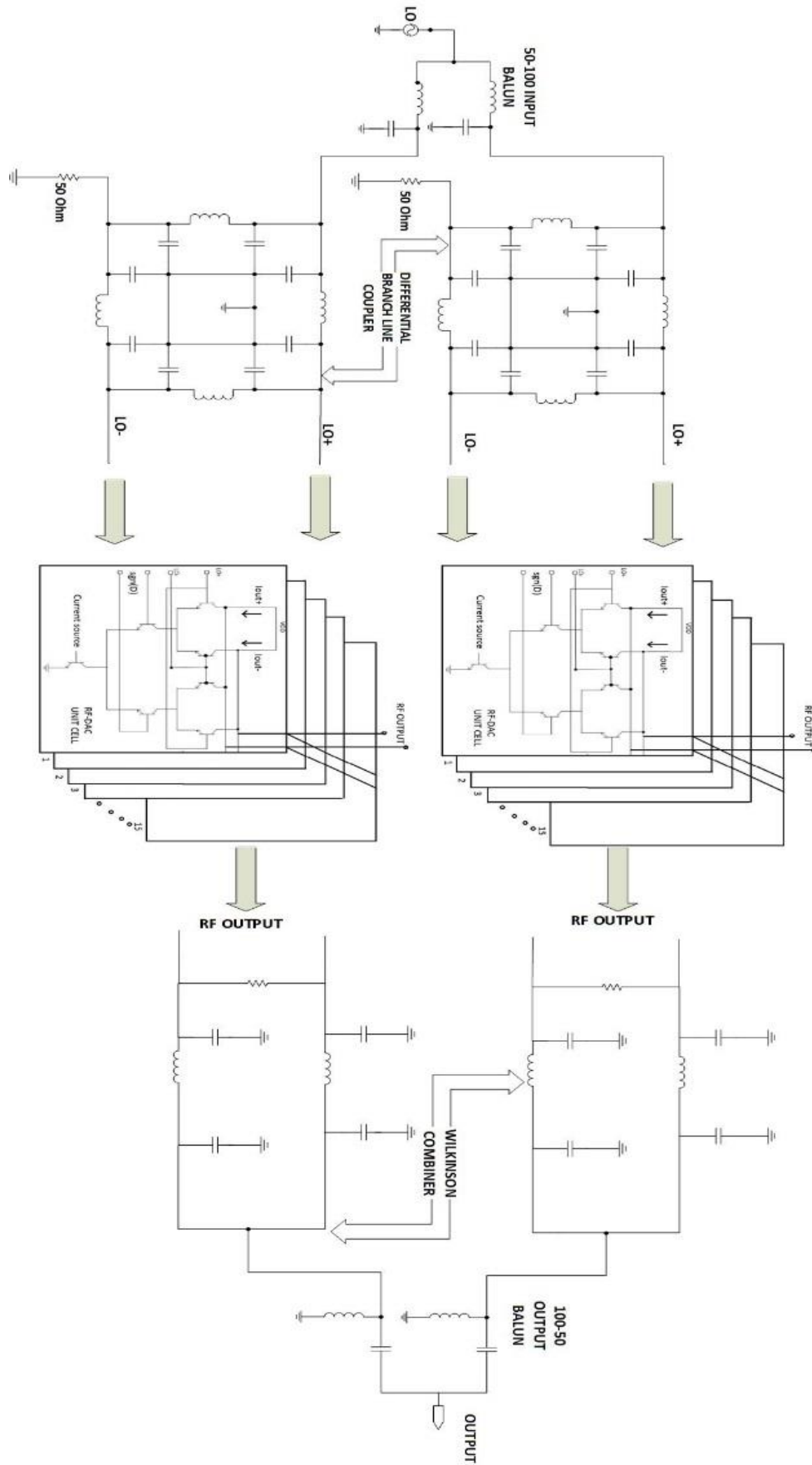
Figure 6- 17 *Number of ON bits from 1 to 15*

PAE vs number of bits

In the given Figure 6-18, the horizontal axis represents the number of bits from 1 to 15 and vertical axis represents PAE. It appears like an exponential curve and at 15 bits when all the RF-DAC cells are ON gives 23 %.

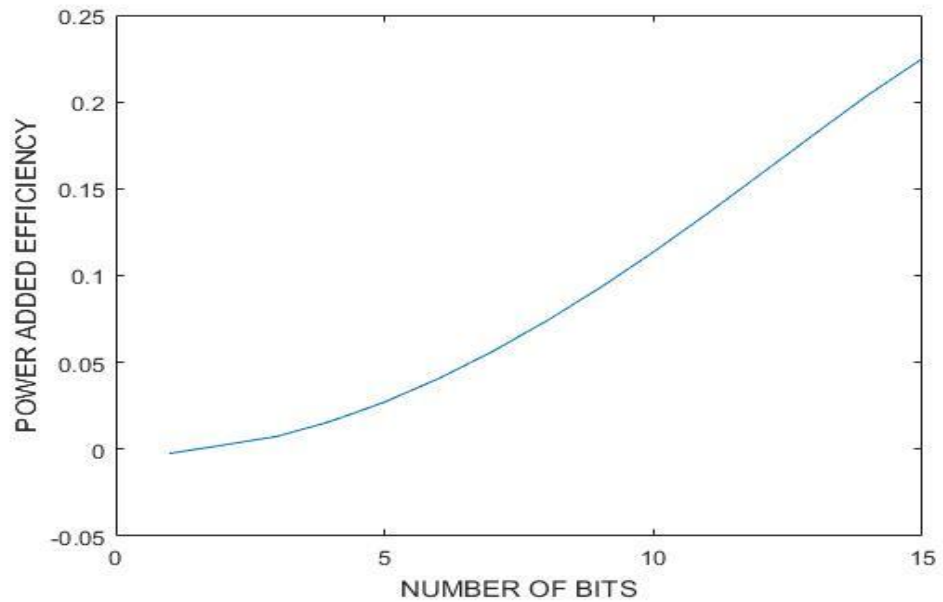***Figure 6- 18*** *Power added efficiency vs number of bits*

6.7.1 Output power vs number of bits

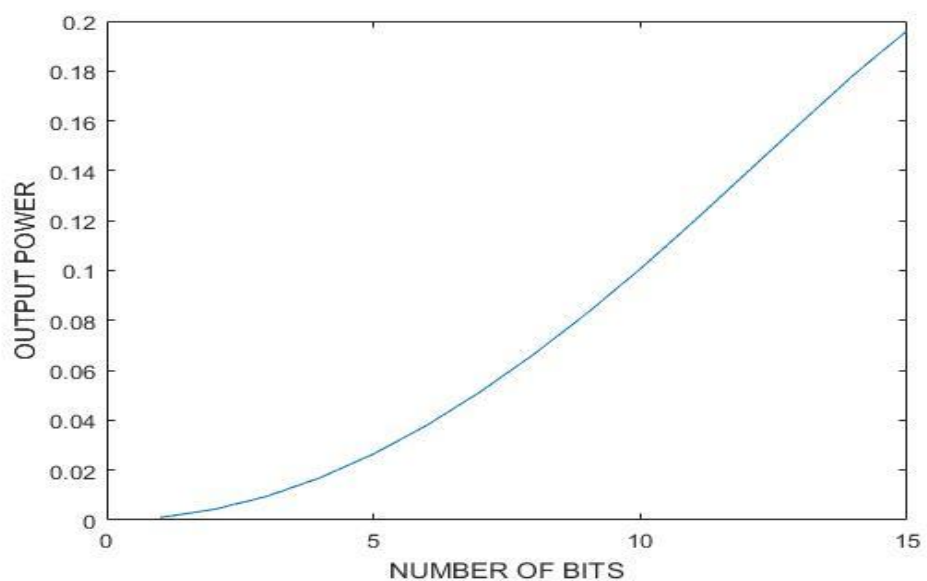The same curve for output power illustrated in Figure 6-19.

Figure 6- 19 *Output power vs number of bits*

6.7.2 PAE vs Output power

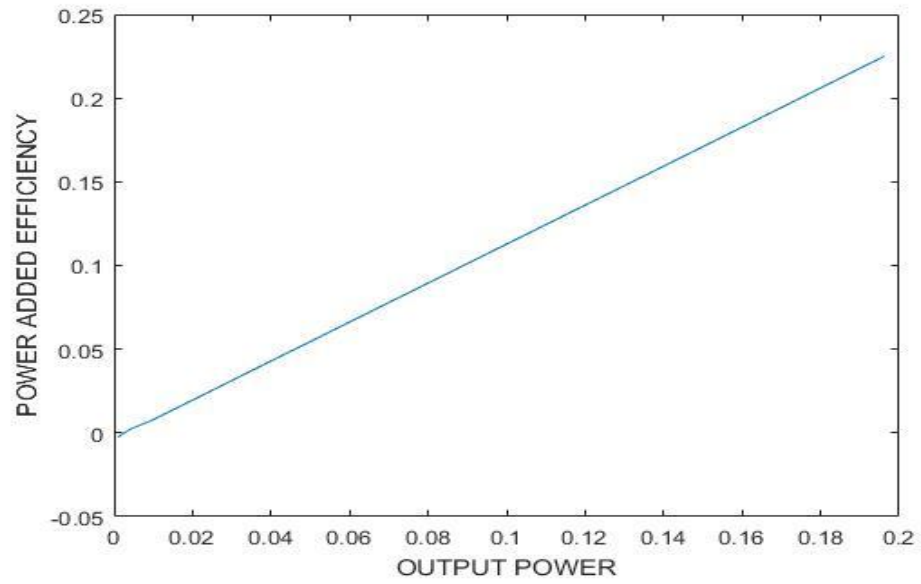In the given Figure 6-20, the graph shows linearly straight curve as it was anticipated.

Figure 6- 20 *Power added efficiency vs output power*

7. CONCLUSION

The goal of thesis was to design and simulate the "30 GHz RF-DAC BASED I/Q MOD-ULATOR" that has been completed successfully. For the implementation of the circuit, a RF-DAC, Wilkinson power combiner, differential branch line coupler and balun has been designed. The complete circuit have an output power of 23 dBm, efficiency of 23% and 18 dB gain.

The thesis reports the designing of modulator circuit with reasonably low power consumption, high efficiency and good gain. Due to time limits the layout of circuit was not made. The project can be continued by making the layout, fabricating the circuit and taking measurements of hardware in the next stage.

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