TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

CUMHUR KUSDEMIR

HIGH-SPEED ASYMMETRIC SELF-OSCILLATING DC-DC CONVERTER OF SINGLE LITHIUM BATTERY CELL VOLTAGE

Master of Science thesis

Examiner: Prof. Nikolay T. Tchamov,
Prof. Teuvo Suntio
Examiner and topic approved by the
Faculty Council of the Faculty of
Computing and Electrical Engineering
on 9 December 2015

ABSTRACT

CUMHUR KUSDEMIR: High-Speed Asymmetric Self-Oscillating DC-DC Converter of Single Lithium Battery Cell Voltage
Tampere University of Technology
Master of Science thesis, 51 pages, 0 Appendix pages
April 2016
Master's Degree Programme in Electrical Engineering
Major: Smart Grids
Examiner: Prof. Nikolay T. Tchamov, Prof. Teuvo Suntio
Keywords: Self-Oscillating DC DC Converter, Resonant Converter, Buck Converter, Resonant Gate Drive, Dead-Time Latch

Lately, there has been a dramatically increase in demand for power electronics having reduced size, weight, and cost as well as improved dynamic performance. The dimension of a power electronic circuit mainly depends on passive components (inductor, capacitor). Increasing the switching frequency does not only leads to decrease in dimensions and weight but also provides faster transient response.

The proposed converter is a buck (step-down) converter, with no external controller. By the feedback system it has, it provides constant duty ratio of around 50%. The defined ranges for the converter is 3.5 MHz, 3.5V-24V input voltage and 2V-12V output voltage. The lowest values for efficiency is defined as 70%.

Since in the market, all high speed converters are on silicon, it makes them expensive to manufacture. Hence, in this converter, we are using real components from the market and later on will be assembled on a PCB. It will decrease the efficiency but the prices of manufacturing is dramatically reduced. Most important is taking parasitics into account which can kill the circuit otherwise. The proposed circuit topology with suitable gate drives is a new thing, and from business point of view, it is easy and cheap.

Switching point is primary side of the transformer, hands over the sending power to the output load, and secondary side of the transformer provides inductive feedback. Thanks to inductive feedback, it provides fast response and adaptive dead-time to eliminate dead-time losses. Two different kind of gate drive circuitries are integrated to converter switches: resonant gate drive and dead-time latch circuitries. They are

applied to switches which are responsible for the major part of the power losses. The overlapping time with main NMOS and PMOS switch is removed, and soft switching is observed at gate drives. Hence, around 4% efficiency increase is realized overall.

Cascaded MOSFETs are introduced in order to make it available for also high voltage applications. Main NMOS and PMOS transistors work complimentary, meaning that once NMOS in ON, PMOS is OFF and vice versa. When PMOS is ON, current flows from battery to load, pulls the switching point (Vx) to battery voltage. When NMOS is ON, current flows from load to ground over the NMOS and pulls down Vx to ground. After Vx point, by using a proper filtering technique, flat DC voltage is obtained at the output.

Using 3.8 V input voltage with 10 Ω load, at the output 2.2 V is achieved with 27 mV voltage ripple. Efficiency is increased to 74% with 3.5 MHz switching frequency by the help of resonant gate drive and dead-time latch circuits. All parasitics are included and deeply studied with simulations conducted in LTSpice.

PREFACE

This thesis work has been conducted at RFIC Laboratory, Departments of Electronics and Communications Engineering of Tampere University of Technology.

I would like to thank to my supervisors Prof. Nikolay T. Tchamov and Prof. Teuvo Suntio for providing me this thesis subject and for the support throughout the thesis. Likewise, I would like to thank to Jani Järvenhaara for sharing his experiences and his recommendations in critical points and my colleague and friend Stanislav Babaev for continuous help till the end and his invaluable friendship.

I would also thank to my friends who helped me to learn and share a life. Especially to my two brothers, in every trouble I have faced, I know I have people I can count on Anil Sirri Baslamisli and Ismailcan Ersahin. You have been my family that we have explored the life and grown up together.

The one who has been there for me for ages, the whom I want to have it there forever, Begum Gokce Sagmaner. The life I had, changed for sweeter at the moment I saw you first time. I would like to send you my heartfelt gratitudes for your warm love ever presented in our hearts. May you be my home forever.

Finally, for their infinite love, patience and support, I could not thank to my mother, father and brother enough for the things they have done for me. I never managed that much without you. Thus, I would like to dedicate this thesis for them.

Tampere, 13.04.2016

Cumhur Kusdemir

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND SYMBOLS

AC	Alternative Current, page 32
BCM	Boundary Conduction Mode, page 4
CCM	Continuous Conduction Mode, page 4
CMC	Current-Mode Control, page 10
dB	Decibel, page 29
DC-DC	Direct Current to Direct Current, page 2
DCM	Discontinuous Conduction Mode, page 4
DSP	Digital Signal Processing, page 8
EMI	Electromagnetic Interference, page 8
ESR	Equivalent Series Resistance, page 31
GND	Ground, page 19
MLCC	Multi-Layer Chip Capacitor, page 31
MOSFET	Metal Oxide Semiconductor Field Effect Transistor, page 14
NMOS	N-Type Metal Oxide Semiconductor Field Effect Transistor, page 14
PCB	Printed Circuit Board, page 2
PMOS	P-Type Metal Oxide Semiconductor Field Effect Transistor, page 14
PWM	Pulse Width Modulation, page 2
Q	Quality Factor, page 26
VMC	Voltage-Mode Control, page 9
ZCS	Zero-Current Switching, page 11
ZVS	Zero-Voltage Switching, page 11

D	Duty Ratio, page 5
I_L	Inductor Current, page 5
V_L	Inductor Voltage, page 5

1. INTRODUCTION

Recently, in order to fulfill the energy provision of the systems, converters with higher efficiency and smaller sized are needed. To obtain reduced size passive components, which are mainly responsible for converter sizes, the switching frequency of the converter should be increased. High speed does not only result in smaller passives but also faster transient response. However, having faster circuit brings some drawbacks as well. It reduces the overall efficiency of the converter and increases the output voltage ripple. It has some limitations because of the parasitic capacitances that appears at high frequencies, lead to power losses while charging and discharging. Figure 1.1 illustrates the relation between a circuit speed and passive component sizes. For the output voltage ripple smaller than 100 mV, 100 MHz switching frequency is able to cut down the sizes of passives to tens of nanometers [11].

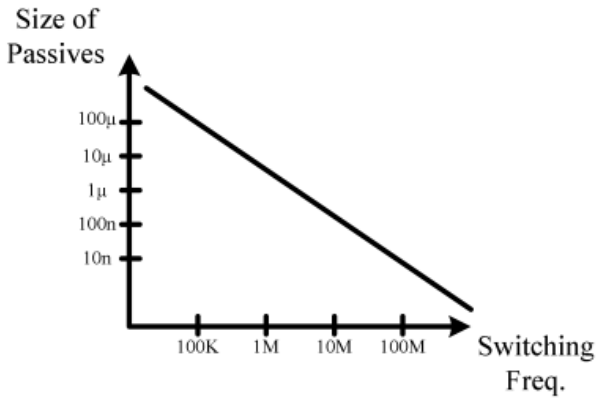

Figure 1.1 *The relationship between switching frequency and passive components.*

Converter power losses have to be cleared up, and lessened. It is crucial to understand how each component contributes to the total power loss.

Self-Oscillating converters are well known for higher speed since the resonant technology they have, makes them to operate at high switching frequencies with higher

efficiency and optimized converter size. In fact, they are resonant converters where the feedback signal is obtained from its resonant load. They can be a solution for switching losses due to their resonant behaviors and prevent the switching surge problems in PWM converters. Despite of their advantages, limitation of applicable upper voltage level, current stress on the switches and poor voltage regulation at the output are the main downsides of resonant converters.

This thesis describes how a self-oscillating dc/dc converter works and what kind of components it consists of. The objective of this thesis is to optimize a buck converter in terms of speed and efficiency. Then the same converter can be used in many appliances which have different output powers and input voltage levels.

The thesis proposes a new technique for Self-Oscillating DC DC Converters, with higher efficiency, variable input voltage levels, output load ranges and suitable for PCB applications by all parasitic taken into account. It includes resonant gate drive and dead-time latch circuitry, so that energy losses can be avoided which occur due to input capacitances of switches and short circuit path from power supply to ground. They help us to apply zero-voltage switching and dead-time method in order to prevent switching losses. Hence, the cost to be paid for higher speed is eliminated by the help of these two circuit topologies.

The reason of employing a lithium battery cell as power source is that they are most convenient ones for supplying power because of their high energy storage density and smaller internal resistances.

The rest of the thesis is organized as follows: Theoretical background 2 , Methodology 3, Experimental Setup and Results 4 and Conclusion 5. Some background information about converters, control techniques and gate switching methods are studied in the next chapter to give brief idea about the work. In methodology chapter, how the model has been developed and what kind of components it has are given. It is supported with some initial theory and discussions. In the fourth chapter, firstly component selection is discussed by using datasheets, frequency analysis and equations. How each converter part is designed and, parasitic is approached are studied. Also, overall design and model of the components are given in a table. The effect of major parameters to overall speed, efficiency and output voltage ripple is highlighted. The results are discussed with waveforms and tables. Finally, the thesis is summed up with the last chapter.

2. THEORETICAL BACKGROUND

This chapter provides the basic knowledge for switching mode dc-dc converters, control techniques and gate drive methods concepts that will be used throughout the thesis.

2.1 Switched Mode DC-DC Converters

In very basic concept, there are two kind of DC/DC Converters which are linear and switched mode. The difference between them is that, a linear mode reduces the voltage by using a resistive drop component to adjust the output voltage where a switched mode uses storage elements which are releases and stores energy periodically to regulate output voltage. Therefore, linear mode DC/DC converters output voltage must be smaller than input voltage, since they are only available for step down function [22]. Switched Mode DC/DC Converters are more common thanks to their higher efficiency and better voltage regulation features.

Achieving energy transfer is the main target of DC/DC Converters [8]. Such transfers can happen between:
A DC Voltage source and a DC Current source: Allows output voltage regulation to a level lower than input voltage.
A DC Current source and a DC Voltage source: Allows output voltage regulation to a level greater than input voltage.
A DC Voltage source and another DC Voltage source: Allows output voltage regulation to a level lower or greater than input voltage, energy transfer occurs by the help of an internal inductance.

Later on in this chapter, all three type of the converter will be studied.

Figure 2.1 depicts the working diagram for a switched mode converter. Firstly, battery voltage is filtered by input side capacitors. The filtered signal goes into

the converter as unregulated. After the converter stage, the signal is regulated to a constant DC voltage value. Finally, it feeds the load as desired.

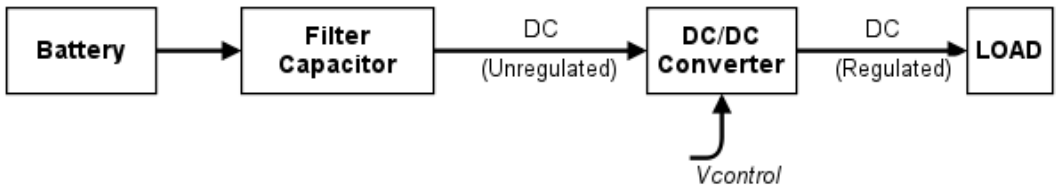

Figure 2.1 *Block Diagram of a Switched Mode DC/DC Converter*

First of all, some basic terminology will be described to help with the understanding of the basic terms.

Duty Cycle: It is the ratio between ON time to the time in one period.

Output Voltage Ripple: Fluctuations in output voltage waveform.

Continuous Conduction Mode (CCM): It means the inductor current never falls down to zero and never stays there. It continuously rises and falls.

Boundary Conduction Mode (BCM): The inductor current rises immediately, after reaches to zero value.

Discontinuous Conduction Mode (DCM): The inductor current falls down to zero and spends considerable amount of time there.

Noise: Random fluctuations in the signal due to parasitic. A filtering technique is needed if it makes the circuit unstable.

Difference between conduction modes are given in Figure 2.2 in order to illustrate. The graph on top is an example waveform of *CCM*, the one in the middle is for *BCM* and the below one is for *DCM*.

2.1.1 Buck (Step-Down) Converter

It is a type of converter which drops down the input voltage and increases the input current at the output, hence input to output power ratio is one, ideally. Usually,

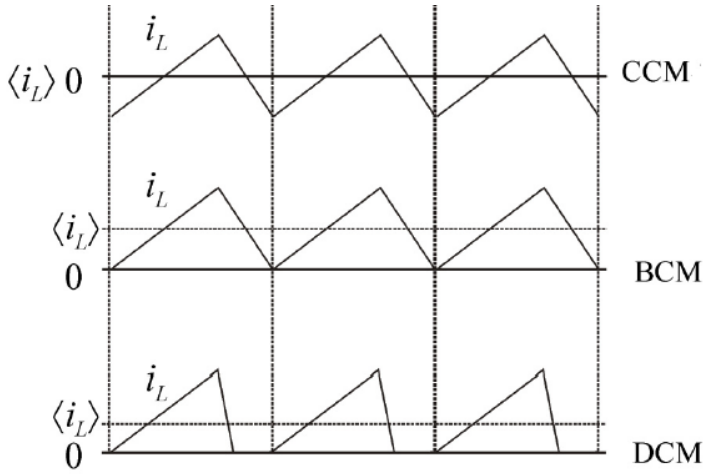

Figure 2.2 *Inductor Current Waveform for Different Conduction Modes*

a buck converter consists of two switches (any pair of switching devices), a storage element (inductor or capacitor), filtering components and a load.

Figure 2.3 contains schematic of a buck converter and output voltage, inductor current waveforms. The principle is such that; when T is ON, diode switch is OFF. During ON time, input current charges the inductor, feeds the load and output voltage equals to input voltage. After T is OFF, inductor discharges through the diode and output voltage becomes zero. By averaging the output voltage waveform of the converter:

$$V_{out} = \frac{V_{in} * t_1 + 0 * (T - t_1)}{T} \quad \& \quad D = \frac{t_1}{T} \tag{2.1}$$

$$\text{Results in;} \quad V_{out} = DV_{in} \tag{2.2}$$

Since the maximum value for D is one, input voltage will be always greater than the output voltage. Moreover, since the law of conservation of energy, in ideal conditions, output power is equal to input power:

$$V_{in}I_{in} = V_{out}I_{out} \tag{2.3}$$

Bearing in mind that Equation 2.2, the relationship between input and output current is given by:

$$I_{in} = DI_{out} \tag{2.4}$$

During ON time, V_L equals to $V_{in} - V_{out}$ and I_L rises, during OFF time, equals to

$-V_{out}$ and I_L decreases. In steady-state, the overall change in inductor current over one period is zero [13]. Hence, the equation below is derived and used for inductor selection:

$$V_L = I\frac{dI_L}{dt} \tag{2.5}$$

$$\Delta I_{Lon} = \int_0^{t_{on}} \frac{V_L}{L}dt = \frac{V_{in} - Vout}{L}t_{on} \quad \& \quad \Delta I_{Loff} = \int_{t_{on}}^{T} \frac{V_L}{L}dt = \frac{-Vout}{L}t_{off} \tag{2.6}$$

$$\frac{V_{in} - Vout}{L}t_{on} + \frac{-Vout}{L}t_{off} = 0 \tag{2.7}$$

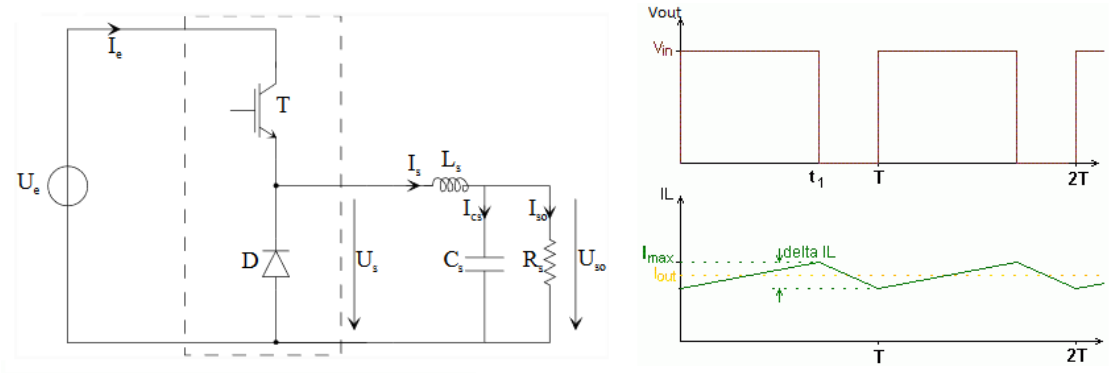

Figure 2.3 *Buck Converter Schematic (Left), Corresponding Waveforms (Right) (Source:* `http://cas.web.cern.ch/cas/Warrington/PDF/Cours20CERN20Barrade202.pdf/` *)*

In our circuit, same equations are employed, and it works in continuous conduction mode all the time.

2.1.2 Boost (Step-Up) Converter

It is a type of converter which steps up the input voltage and decreases the input current at the output, hence input to output power ratio is one, ideally. Usually, a boost converter consists of with the same components as in a buck converter.

Figure 2.4 contains schematic of a boost converter and inductor voltage, current waveforms. The principle is such that; when T is ON, diode switch is OFF. During ON time, input current charges the inductor flows through the switch, V_L equals to

V_{in} and inductor current starts to rise. After T is OFF, inductor discharges through the load, V_L equals to $V_{in} - V_{out}$. Since the voltage over one period in steady-state on an inductor is zero, following equation is used in calculations:

$$V_{in}t_{on} = (V_{in} - V_{out})t_{off} \quad \& \quad D = \frac{t_{on}}{T} \tag{2.8}$$

$$V_{out} = \frac{V_{in}}{1 - D} \tag{2.9}$$

Also, considering Equation 2.2, in ideal conditions, output and input current relation is given by:

$$I_{out} = I_{in}(1 - D) \tag{2.10}$$

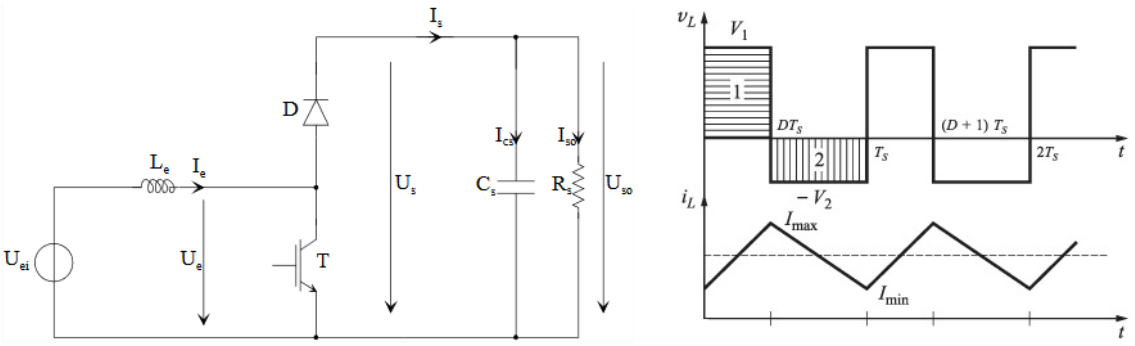

Figure 2.4 *Boost Converter Schematic (Left), Corresponding Waveforms (Right) (Source:* `http://cas.web.cern.ch/cas/Warrington/PDF/Cours20CERN20Barrade202.pdf/` *)*

2.1.3 Buck-Boost Converter

This converter can be realized as either step up or step down converter, as to applications. By changing the switch control signal, in other words changing the duty cycle, output voltage can be higher or smaller than the input voltage. Components are the same as the ones used in previous topologies.

Figure 2.5 includes schematic of a buck-boost converter and inductor voltage, current waveforms. The principle is such that; when T is ON, diode switch is OFF. During ON time, input current charges the inductor flows through the switch, V_L equals to V_{in} and inductor current starts to rise. After T is OFF, inductor discharges through the load, V_L equals to $-V_{out}$. Since the same voltage on an inductor over

one period rule applies in this topology as well, the following equations are derived:

$$V_{in}t_{on} = (-V_{out})t_{off} \quad \& \quad D = \frac{t_{on}}{T} \tag{2.11}$$

$$V_{out} = V_{in}\frac{D}{1-D} \tag{2.12}$$

Anew, keeping in mind Equation 2.2, in ideal conditions, output and input current relation is given by:

$$I_{out} = I_{in}\frac{1-D}{D} \tag{2.13}$$

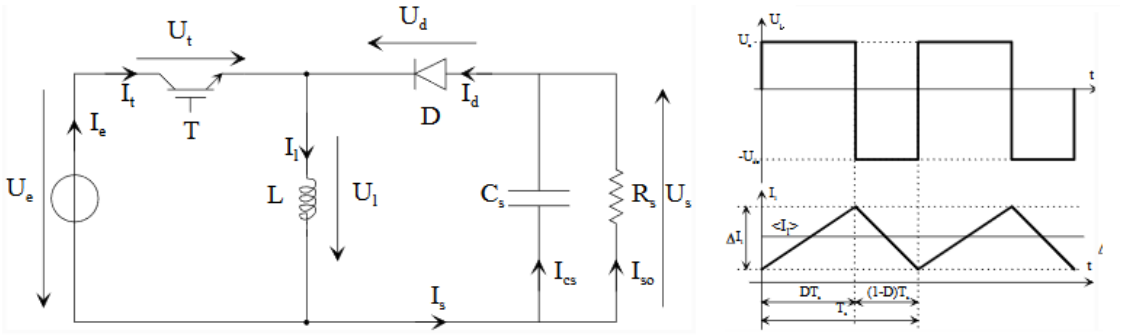

Figure 2.5 *Buck Boost Converter Schematic (Left), Corresponding Waveforms (Right) (Source:* `http://cas.web.cern.ch/cas/Warrington/PDF/Cours20CERN20Barrade202.pdf/` *)*

2.2 Control Techniques

Switched Mode DC/DC Converters consist of two different stages: power and control stage. In order to regulate output voltage, either an external DSP board, or self-control methods are employed. Self-control method is studied in Chapter 3. Brief information on external control techniques will be given in this section.

Control stage handles the operation of the circuit by observing and interfering the output voltage, or the feedback source. Control and power stage are connected over a feedback component. Without a controller, stability and precision of the power supply would be doubtful and PWM techniques are the most common in regulation.The reason of employing PWM signal with constant frequency is to limit electromagnetic interference (EMI) produces by power supply [21]. There are mainly two methods which can generate PWM signal: Voltage Mode and Current Mode Control.

2.2.1 Voltage-Mode Control

It basically compares the output voltage with a reference voltage. The reference voltage and the output voltage are connected to a single loop controller for comparison. The difference between the reference and measured voltage forms the control voltage. After that, the switching duty ratio is generated by comparing the control voltage with a constant frequency waveform. The obtained duty ratio is utilized to produce average voltage over the main inductor. Finally, this creates the desired voltage at the output. In Figure 2.6, the control schematic is presented.

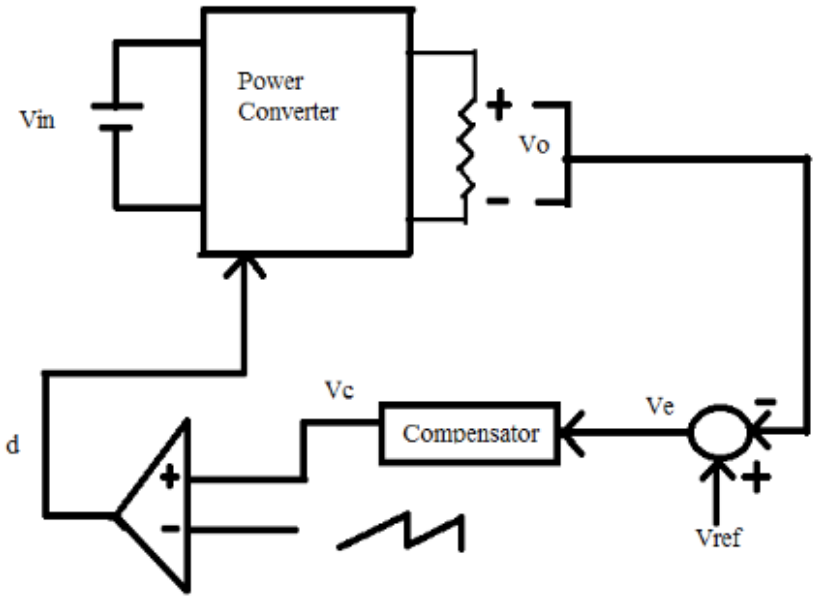

Figure 2.6 *Voltage mode control of power converter (Source: http://www.isca.in/IJES/Archive/v2/i8/4.ISCA-RJEngS-2013-099.pdf)*

Design of a single feedback loop is easier than other control loops. Having decent noise margin in stable modulation process as a result of using large-amplitude ramp waveform is one of the advantages of VMC [21]. Another advantage is acquiring good cross-regulation for multiple-output supplies due to a low-impedance power output. [38] lists the drawbacks of VMC as such: i. Poor main switch reliability and stability. ii. Once more than one converters connected in parallel to one load, reliability, stability and performance even decrease more. iii. It is hard to keep main transformer to operate in the center of its linear region. iv. The response takes couple of cycles since it is a slow system.

2.2.2 Current-Mode Control

Unlike VMC, current-mode control has two, current and voltage, control loops as seen in Figure 2.7. It does not only observers the inductor voltage but also its current. In order to control the duty cycle, the inductor current is employed. The output voltage is compared with the reference, and control signal is generated. After that, the control signal is compared with the inductor current, and duty cycle for switch drive is generated.

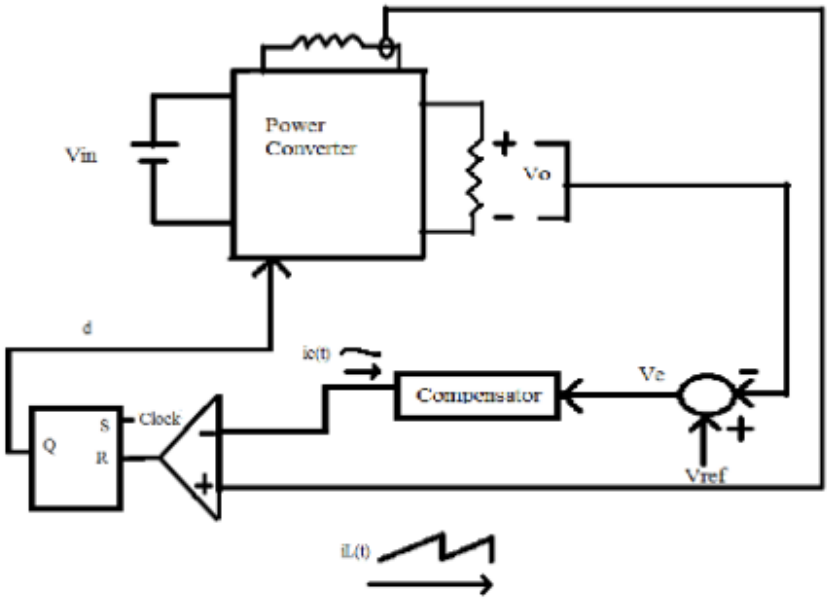

Figure 2.7 *Current mode control of power converter (Source: http://www.isca.in/IJES/Archive/v2/i8/4.ISCA-RJEngS-2013-099.pdf)*

[38] lists the advantages of CMC: i. Improved transient response, since order of the converter is reduced to first at the beginning. ii. Decent line regulation. iii. Better performance than VMC when converters are parallel. iv. More secured main switch.

As disadvantages: i. When the duty ratio is bigger than 0.5, it becomes very unstable. ii. Sub-harmonic oscillations appear with CMC.

2.3 Gate Switching Methods

The main disadvantage of PWM converters are their switching losses and low efficiencies at high frequencies [9], which make them inconvenient for higher speed. The main advantage of resonant self-oscillating converters is their reduced switching loss, by employing zero-current switching (ZCS) and zero-voltage switching (ZVS). These mechanisms are described in detail in following sections. Before that, the definitions of hard and soft switching terms are given.

Hard Switching: It takes place when voltage and current of a transistor overlaps, while switching it ON and OFF. The overlap leads to a short circuit path and results in power loss, which can be reduced by increasing the di/dt and dv/dt [18]. Fast changing of di/dt and dv/dt would produce EMI, hence the change in them should be revised. Figure 2.8 illustrates hard switching waveform.

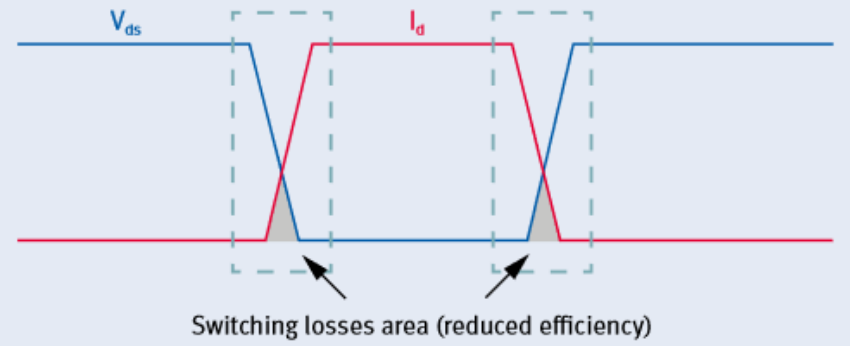

Figure 2.8 *Hard Switching waveforms*
(Source: `http://www.infineon.com`)

Soft Switching: It means adjusting voltage or current to zero before switching ON or OFF. The advantage is reducing in power loss, in other words not short circuit path. Moreover, having flat switching waveforms decreases EMI [18]. Zero-voltage and zero-current switching methods are applied for soft switching. Figure 2.9, depicts soft switching waveform.

Zero-Voltage Switching (ZVS): ZVS technique includes soft switching so that conduction and switching losses are minimized. Ideally, switching from ON to OFF or vice versa happens when transistor current is zero, so no power dissipation occurs. However, in real life, the transistor output capacitance discharges, and spends too much energy, when the switch is pulsed. Using ZVS technique, this loss is avoidable

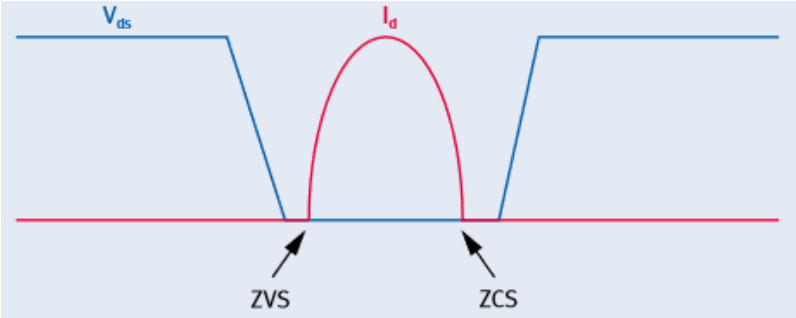

Figure 2.9 *Soft Switching waveforms*
(Source: http://www.infineon.com)

since it deceives the capacitance to discharge before switching ON the transistor [4], [43]. It important to recall that, ZVS only eliminates turn ON losses. Advantages come with ZVS are such: i. Lossless switching periods. ii. Decrease in EMI at switching. iii. Discharging of output capacitance does not cause energy losses. iv. High efficiency at any switching frequency.

Zero-Current Switching (ZCS): Switching OFF of transistors happens at zero current. Switching at zero current phase outs losses caused by current tailings and stray inductances [37]. Employing together with ZCS and ZVS would cut off most of the switching losses occur in ON and OFF transition and energy losses due to discharging of output capacitance. Resonant circuitries should be applied to use these techniques, and some times snubber circuits are needed. Figure 2.10 illustrates the losses arise when ZVS and ZCS are not utilized.

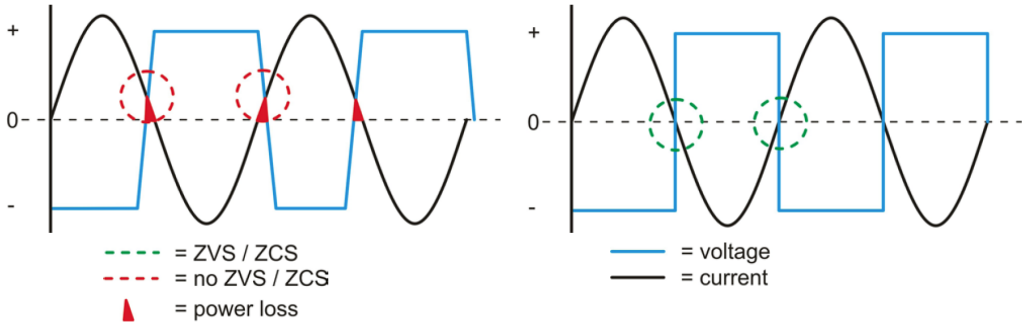

Figure 2.10 *ZVS-ZCS losses*
(Source: http://www.kitguru.net/components/power-supplies/zardon/be-quiet-dark-power-pro-11-550w-review/4/)

3. METHODOLOGY

This chapter will give the further explanation of the Self-Oscillating DC/DC Converter, by going into design details and theory. Component Selection, gate driving, feedback system and its parts, speed factors and efficiency are described and presented by graphs.

3.1 Initial Model

The initial topology of the converter is given in Figure 3.1. This is the most basic form of the converter. The final topology of the converter is built based on this model, which will be discussed in detail in Section 3.3.

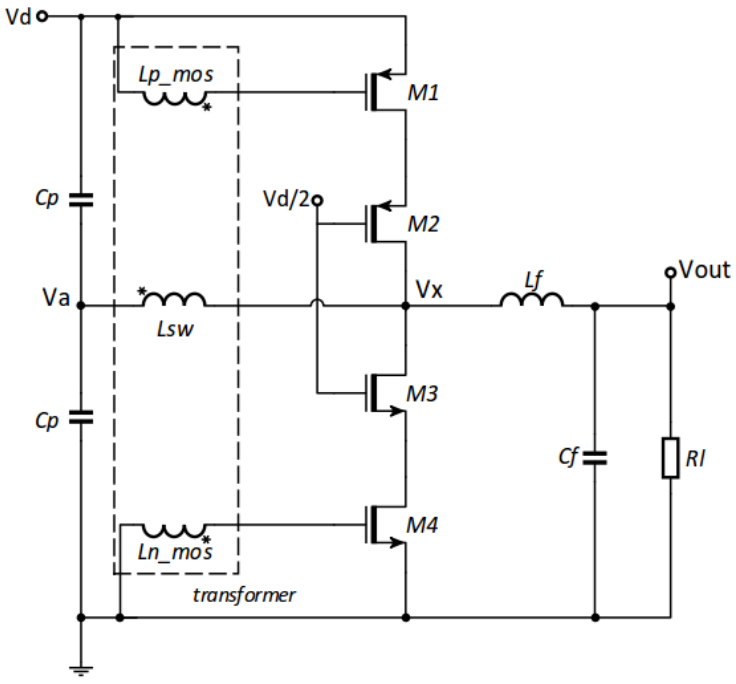

Figure 3.1 *Initial model of SODCDC*

The reason of using cascading transistor is to handle not only low voltage applications but also high voltage applications.

The operation principle of the circuit is such that, *M1* and $M4$ MOSFETs are working complimentary. $M1$ & $M2$ are PMOSs, $M3$ & $M4$ are NMOSs. Lp_mos and Ln_mos have the same polarity, contrast to Lsw. Cp capacitors are high enough to provide Vd/2 to Va point. Initially, Vx is zero and therefore Lsw has Vd/2 voltage on it. Then this value is transferred to $M1$ & $M4$ gates, which makes $M1$ ON and $M4$ OFF, enables the current flows through $M1$ & $M2$. Now, Vx has Vd voltage on it and Lsw has -Vd/2. This voltage value switches OFF M1 transistor and ON $M4$ transistor. It enables the current flow from Vx to the ground through $M3$ & $M4$ and makes Vx value zero again. Hence, Vx becomes the center of oscillation. By utilizing the filter elements after oscillation point, a flat shaped output voltage waveform can be obtained. As a result, a basic buck converter with 50% duty cycle is constructed. The relation of output and input voltage as happens in a buck converter is given by:

$$V_{out} = \frac{1}{2} V_{in} \tag{3.1}$$

In Equation 3.1, the duty cycle is assumed as 50%, as it mostly happens in Self-Oscillating DC-DC Converters.

However, even if it is possible to achieve the target frequency with this topology, there are some challenges. The main challenge is to accomplish coupled inductor & transformer design. At high frequencies, the losses increase for transformers [12] and hence it is hard to implement it on a PCB. Other challenges are such as; conduction and dead-time losses due to inadequate control. These challenges and way to overcome them are explained in details in further chapters. Therefore, this initial design needs some development in order to have more efficient and decent control system

3.2 Secondary Model

The model in Figure 3.2, now has improvements on it and works better way than the previous one. $L1$ inductor is employed as not only switching but also filter inductor. The transistor pairs, such as $M5$ & $M6$ form inverter stages. Moreover,

using two inverter stages consecutively, makes them a buffer stage. Thanks to this stage, at the gate drive, square waveforms are obtained. Buffers are mostly used for drive circuits[24]. The benefit of having these stages is to obtain reduced gate drive losses, which will be explained in detail later.

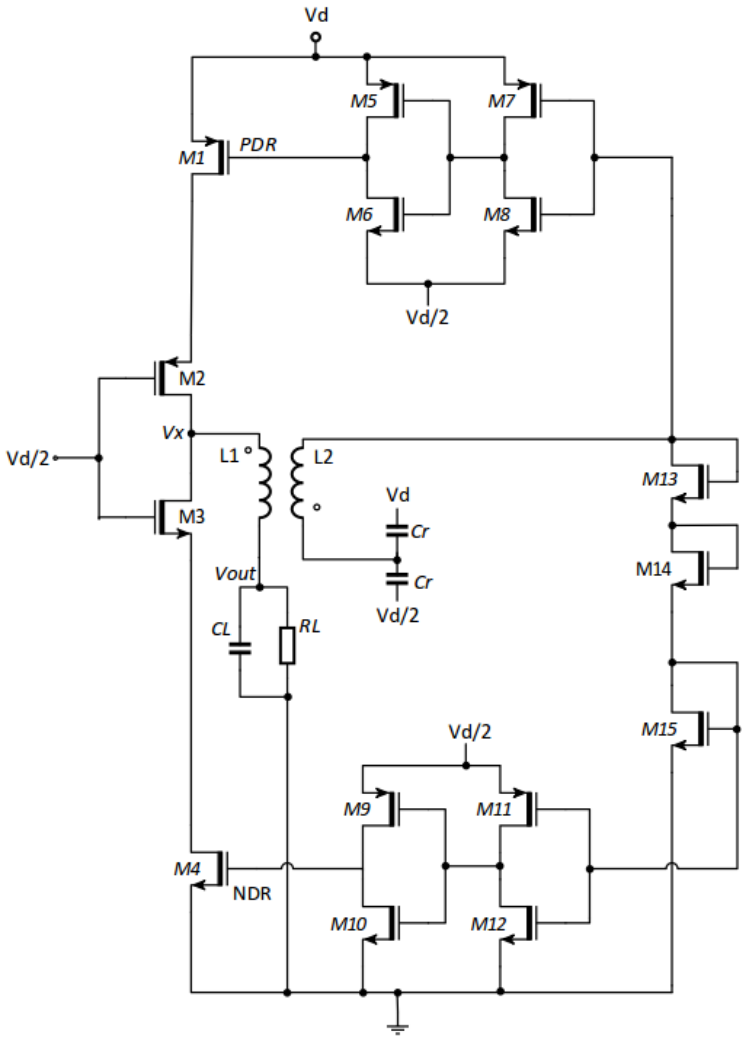

Figure 3.2 *Secondary model of SODCDC*

The level shifter circuit is formed by $M13$, $M14$ and $M15$. Since the NMOS side of the circuit is driven by the voltage level of Vd/2 to ground, dropping the feedback voltage for NMOS side is a must. By using three NMOS transistor, the voltage level is reduced certain amount because of their threshold voltages.

Nevertheless, this circuit has some amount of losses that are not acceptable, so more

improvements are needed. The final version of the circuit is presented in the next section with all the details and sub circuits.

3.3 Final Model

In the final model Figure 3.3, we have additional 4 MOSFETS *(M16, M17, M18, M19)* and additional filter inductor at the output stage. Moreover, resonant gate driver and dead time latch structures are introduced. These are studied in (Subsection 3.3.4)

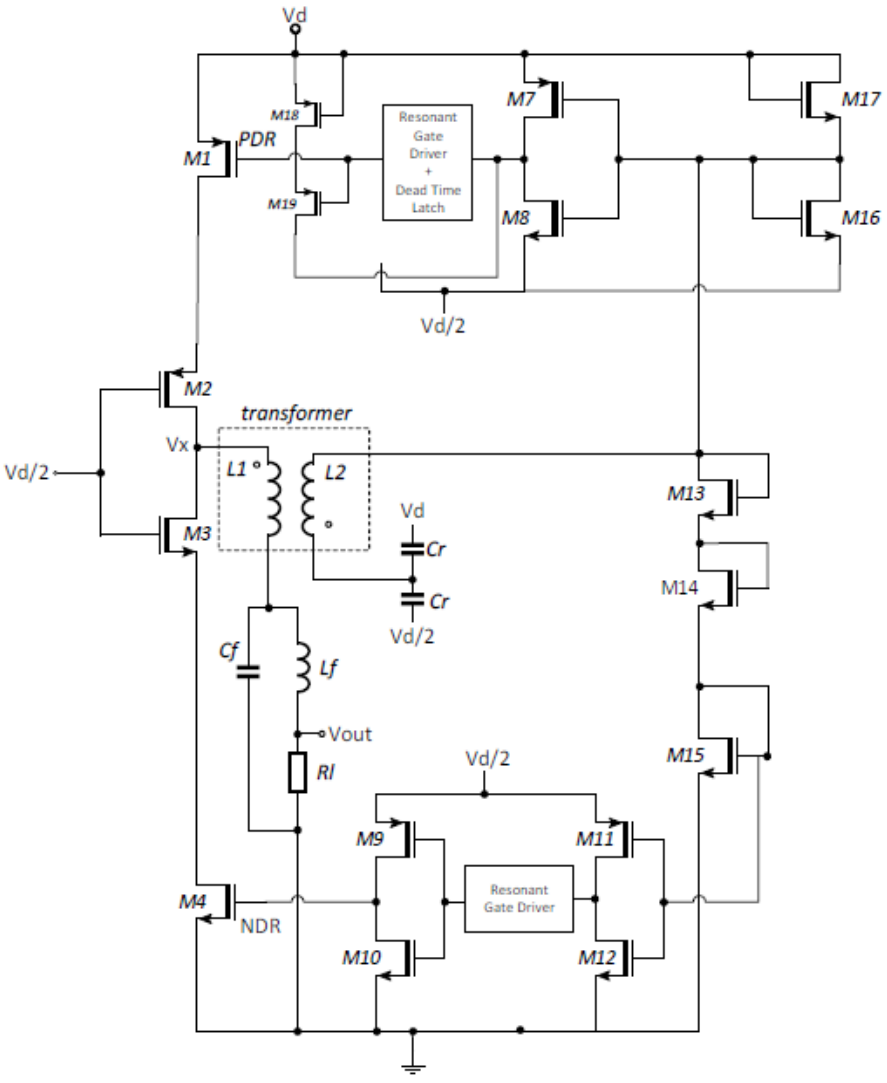

Figure 3.3 *Final model of SO-DC/DC*

To divide the circuit into two stages, *M1, M2, M3* and $M4$ transistors form the power stage, and the rest forms the feedback circuitry (duty cycle detector and pulse shaper).

$M16$ & $M17$ transistors are employed as diodes to supply enough voltage to the connection point at the secondary side of the transformer [3]. Moreover Cr capacitor pairs are used for that purpose as well, by dividing the voltage between Vd and Vd/2.

$M18$ & $M19$ transistors offers a small feedback function to p-channel driver. This function is not necessary in n-channel driver in order to have correct start-up [3]. The asymmetric term in the title of thesis comes from this local feedback difference.

In order to prevent turning ON both MOSFETs at the same time, dead time latch and resonant gate drive techniques are employed. By this way, conduction losses are decreased considerable amount.

The factors affecting the speed of the converter are inductance and magnetic characteristic of the transformer, internal parasitic capacitances of switching MOSFETs, hence, the current at the output and the input battery voltage.

In the following subsections, the divisions of the main circuitry will be discussed.

3.3.1 Feedback System

Simply, the high power stage of the circuit and low power stage of the circuit, feedback circuitry, is separated by using coupled inductor feedback system. Thanks to inductive feedback, we do not need more level shifters to drive transistors in the power stage. Moreover, it provides fast response and adjustable dead-time between drive signals in order to bypass conduction losses [2]. Moreover, inductor is a passive storage element, which is used normally to store energy. However, in steady-state conditions, average voltage on an inductor equals to zero over one switching period. The formula below Equation 3.2 expresses that statement.

$$\frac{1}{Ts}\int_{0}^{Ts} Vl * dt = 0 \tag{3.2}$$

The name of the rule is called as $InductorVolt - SecondBalance$. It can be assumed as voltage on an ideal inductor equals to zero, which results in zero power

consumption.

After the feedback inductor, the signal is solidified by $M16$ & $M17$ and Cr capacitors. This signal goes through two paths; one way is to NMOS side through the level shifter and the buffer, other way is to PMOS side through the buffer and the local feedback.

3.3.2 Buffers and Inverters

Figure 3.4 illustrates the schematic of an inverter made of two transistor pairs. The transistor at the top is a p-channel MOSFET and the one at the below is an n-channel MOSFET. It is actually a basic switching circuit, when the voltage at the input is high output voltage is zero and vice-versa. When the input voltage

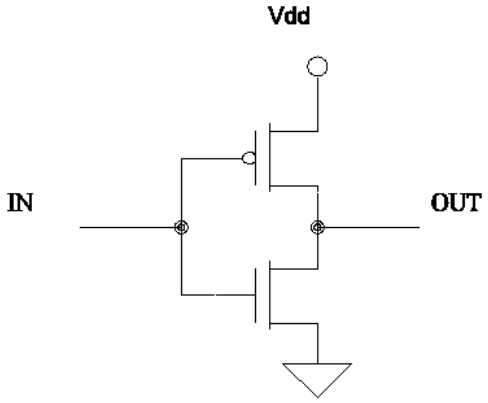

Figure 3.4 *Schematic view of an inverter*

is smaller than the threshold value of the NMOS, the NMOS turns OFF and the PMOS turns ON. Then the current goes from Vdd to output capacitor and the output voltage equals to the supply voltage. When the input voltage is bigger than then the threshold voltage of the NMOS, the NMOS turns ON and the PMOS turns OFF. Then the current flows from the output capacitor to ground through the NMOS, and the output voltage becomes zero.

In Figure 3.5, when input voltage rises, output starts to fall. t_f and t_r mean fall and rise times, respectively. These terms refer to charging and discharging time of the capacitor. Depend on the time constant of a capacitor, these times may take shorter or longer times

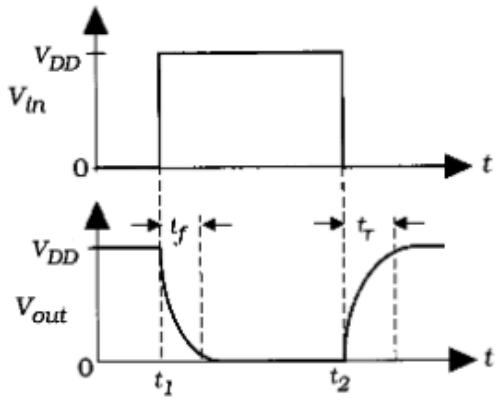

Figure 3.5 *Input vs Output Voltage waveform of a MOSFET Inverter*

Figure 3.6 presents two inverter stages in series, forming a buffer stage. Buffer circuit is a connection of back to back two MOSFET inverters. The output of the one feeds the input of another, as a result two inversion function eliminates each other. In other words, no inversion is observed at the output. The reason of using buffer stage in a circuit is to strengthen or boost the input signal. The output would be the same as input signal as logic level but the signal is railed between Vdd and Gnd. Another reason is to delay the signal for a short time. However, this may be considered as a drawback for some applications.

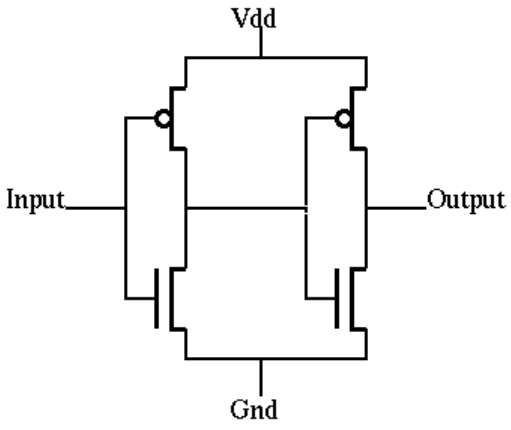

Figure 3.6 *Schematic of a MOSFET Buffer*

In the Figure 3.7, it is shown that how the buffer straightens the input signal, and results in a better square wave form. the waveform on the top is input and the other one is the output voltage of a buffer circuit. As it can be easily concluded, the input

signal is boosted and now at the output, a superior square wave is obtained.

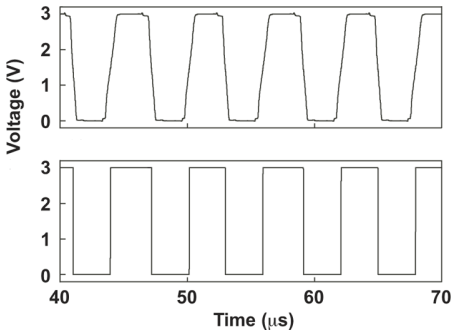

Figure 3.7 *Input (upper) and output (lower) voltage waveforms of a buffer circuit*

3.3.3 Level Shifter

Since biasing voltages of NMOS and PMOS are different, we need a level shifter to drive the main NMOS transistor. Level shifters are widely used in power management units and in many related applications, when different voltage levels are needed. Each transistor, reduces the voltage as its own threshold voltage. In the circuit, there are two MOSFET's in series, which means the voltage value after them is decreased by two threshold voltage. Gate and drain voltages are the same, therefore the following equation gives the source voltage:

$$V_d - V_{th} = V_s \tag{3.3}$$

This configuration is formed by $M13$, $M14$ and $M15$ transistors. There are two main drawbacks in the setup. The first one is power consumption. Since all transistors behave like a resistor when they are ON, continuously, they consume some amount of power depend on the current passes through. The second drawback is the timing delay. To turn on and off a transistor, the capacitors inside of them are charged, or discharged first. The time heavily depends on the internal capacitances of a transistor.

3.3.4 Gate Drives

When dealing with very high frequencies, conventional hard-switching techniques for transistor gates are not applicable, since they introduce some losses which are not acceptable from the efficiency point of view [32]. The power consumption when using hard switching can be calculated by the formula given by:

$$P_{loss} = Q_{gs} * V_{gs} * f \tag{3.4}$$

V_{gs} denotes, gate-to-source voltage, f frequency and Q_{gs} gate-source charge. In our circuit, we have two main switches and this power loss would be huge if hard-switching is employed.

In order to turn a MOSFET on, the gate needs some amount of charge. Once the gate voltage reaches the certain level, the MOSFET operates in linear or in saturation region. The below formulas are the working conditions for an NMOS transistor.

$$\text{For cut-off region:} V_{gs} < V_t \tag{3.5}$$

$$\text{For linear region:} V_{gs} > V_t \quad \& \quad V_{ds} \leq V_{gs} - V_t \tag{3.6}$$

$$\text{For saturation region:} V_{gs} > V_t \quad \& \quad V_{ds} > V_{gs} - V_t \tag{3.7}$$

If the function of the transistor is a switch, then drive circuit should have large transient current capability. By that way, the time that the MOSFET in linear region becomes very short, and therefore the switching losses are reduced [19].

The Gates of the main MOSFET?s are driven by the signals come out from two pulse-shaping circuits, which are working in-phase. The crucial part is, overlapping these two MOSFET drive signals in order to prevent that main NMOS and PMOS are ON at the same time. We can avoid dead-time losses mostly by applying Resonant Gate Drive and Dead-Time Latch Techniques.

Resonant Gate Drive Technique

This technique provides recovering of energy at charging and discharging stages of internal transistor capacitors [10]. It is basically a LC circuit that oscillates and charges or discharges gate capacitances of a transistor. [10] offers a circuit to be

used as this technique. Figure 3.8, represents the structure. Diodes are clamping diodes, used for recovering the energy.

Operation of the circuitry is such that: Firstly, M_{DR1} turns ON, and voltage at the mutual point of the transistors becomes V_{DD}. The voltage on the gate of the main switch starts to rise with the inductor current. After that the voltage after the inductor clamped to V_{DD} by the help of D_{DR1}. At this time period, current flows between M_{DR1}, D_{DR1} and L_R. After M_{DR1} turns OFF, recovering the energy process and current starts to flow from $VDD - D_{DR1} - L_R$ and body diode of M_{DR2}. The inductor current declines linearly. The Inductor value arranged carefully so that it does not behave as a current source.

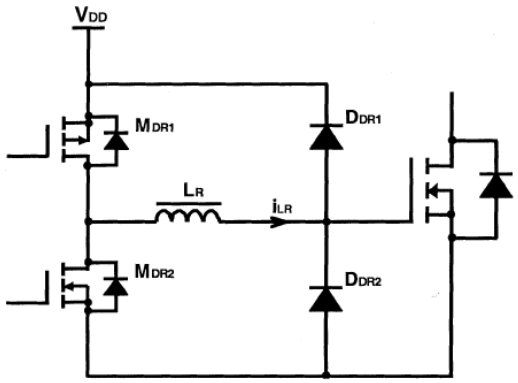

Figure 3.8 *Resonant Gate Drive Circuit*

This circuit is utilized at the gate of NMOS side buffer and main PMOS Gate. The reason is that; they are the circuit components that are responsible for energy losses.

Dead Time Latch

In order to restrain dead time losses due to the short circuit path between power supply and ground, the dead time is required [20]. The dead time between PMOS and NMOS gate drives is achieved by utilizing a latch circuitry to main PMOS gate, since it dissipates more energy than the main NMOS.

Figure 3.9, represents the dead time latch circuit. Output signal of the latch drives the main PMOS, and input signal comes from the resonant gate drive circuitry after the PMOS side inverter. Feedback is taken from the signal after the main PMOS.

The main NMOS should be switched OFF first, then the PMOS can be ON with a lag. Q2 postpones switching the PMOS ON for a short time to make sure that the main NMOS is turned OFF. Internal capacitance of the transistor in the circuitry plays the main role for the length of dead time. Other transistors in the circuitry work as an inverter, since one inverter from the buffer stage is removed in the PMOS side.

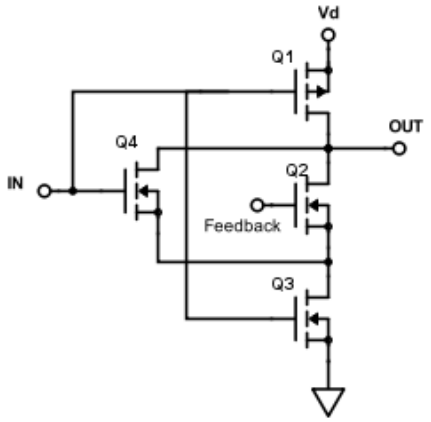

Figure 3.9 *Dead-Time Latch Circuit*

3.3.5 Output Filter

The waveform signal at Vx switching point is a square waveform, where the desired waveform at the output is DC voltage. To obtain DC voltage at the output, a filtering circuit is needed between output and switching point.

Output filters mainly consist of inductors and capacitors. Main duties are to reduce noise and ripple at the output. In reality, there are no ideal capacitors. They include a resistor and an inductor series to the capacitor as one can see on Figure 3.10. Attenuation performance also depends on the resistance not only the capacitance. In addition, maximum operating frequency depends on inductance value [16]. The impedance of a capacitor is given by;

$$X_c = \frac{1}{2 * pi * f * C} \tag{3.8}$$

Figure 3.10 *Model of a Capacitor*

In reality, there are no ideal inductors. They include a resistor in series and a capacitor in parallel as can be seen from Figure 3.11. The internal resistance decreases the efficiency because of the losses. The capacitor appears at high frequencies and it affects maximum frequency range negatively [16]. The impedance of an inductor is given by;

$$X_l = 2 * pi * f * L \tag{3.9}$$

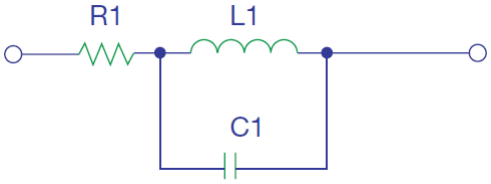

Figure 3.11 *Model of an Inductor*

In the proposed circuit, we use an LCL Filter as can be seen on Figure 3.12. Also in digital applications, this filter is known as Butterworth Filter. The main reason of employing this filter is that they have indeed smooth frequency response. In other words, the ripple at the output is small [23]. Moreover, output response becomes oscillatory [14].

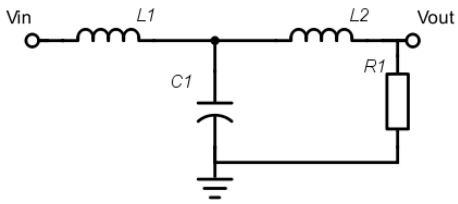

Figure 3.12 *LCL Filter*

Vin point in Figure 3.12, is the switching point Vx in our circuit. $L1$ is the

primary side of the transformer and $L2$ and $C1$ are filter inductor and capacitor, respectively. The maximum output current of the circuit should be smaller than the current ratings of the inductors. Furthermore, the voltage rating of the capacitor should be as high as possible in order to avoid circuit malfunctions.

Determining the components values needs trial & error method mostly, which will be analyzed in further chapters. The required ripple factors are also taken into account for component selection. Figure 3.13 depicts the waveform after and before filtering process. As it can be clearly understood, when voltage ripple of Vin is around 5V, the output voltage ripple is around 35mV.

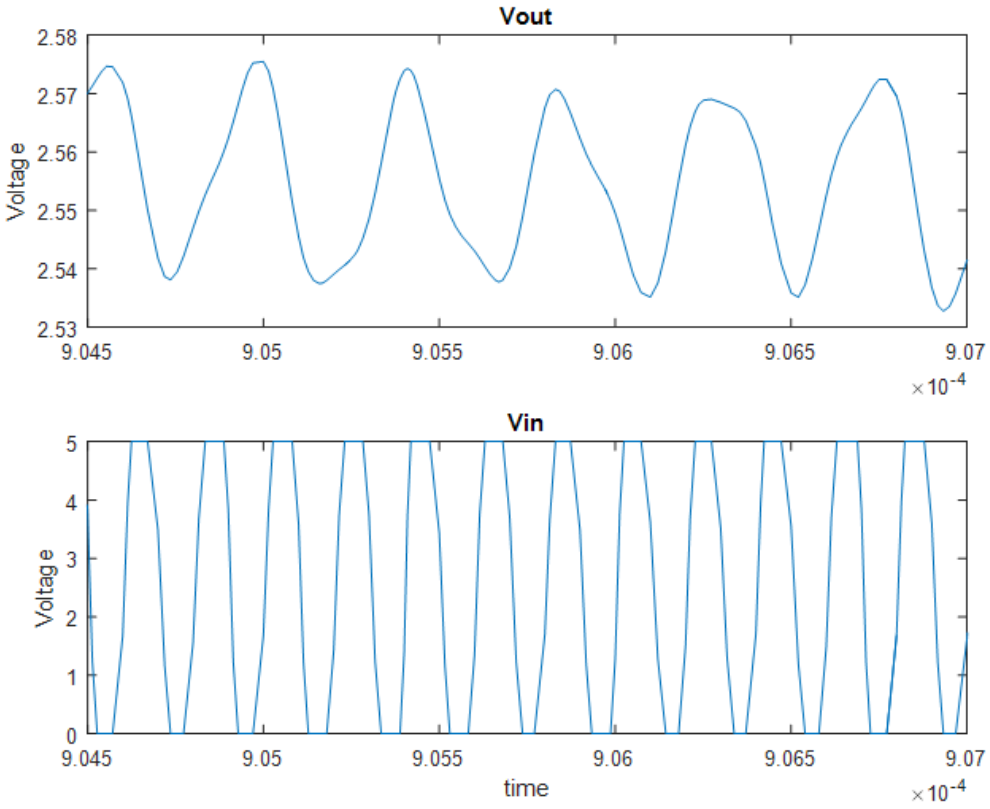

Figure 3.13 *Output and Input voltage waveforms after filtering*

3.3.6 Transformer

In the proposed circuit, the transformer is employed as an insulator, which separates basically power and feedback stages. It is important to isolate high and low

voltage sides in order to reduce power losses in the feedback stage. The transformer transfers small amount of current to secondary side. The primary winding of the transformer is used as an switching inductor, where power calculations happens, while the secondary winding of the transformer is used as an inductive feedback.

Oscillation frequency is mostly related to transformer inductances. Since basic inductors are storage elements, certain amount of time is needed in order to charge and discharge them. The energy is stored in the windings. The charging time of an inductor is the time for applied current to reach its maximum value. After that the current stays at steady-state unless there are some changes to input. This time from zero current to steady-state depend on two variables which are inductance and resistance value. Figure 3.14 shows a demonstration circuit for inductor circuit. Once S1 turns ON, current starts flowing through the inductor and charging process begins. The time constant of an inductor is L/R. The formula below describes the changing of the current with respects to time is given by:

$$i = \frac{E}{R} * (1 - e^{\frac{-Rt}{L}}) \tag{3.10}$$

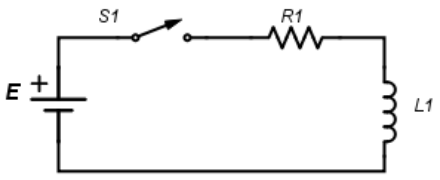

Figure 3.14 *Inductor charging circuit*

Also Figure 3.15 shows the graph representation of Equation 3.10. It is obvious that, the smaller L/R ratio, the faster the circuit. Discharging process is also the same. Hence, small L/R ratio is needed to speed up the circuit.

The other factors that need to be careful about transformer are the saturation concept and Q factor. Q factor stands for quality factor, which describes reactive elements like inductors and capacitors. We have applied this concept to the transformer in order to see the effective frequency range of it. The equation for the

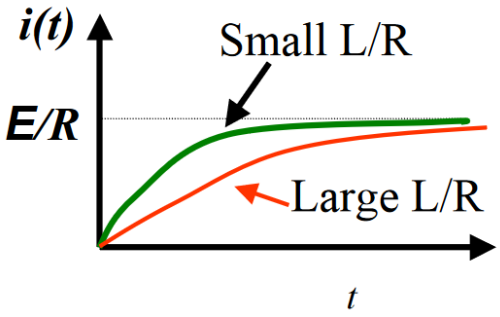

Figure 3.15 *Current vs Time in RL circuit*

general definition of the quality factor is given by:

$$Q = 2 * \pi * f * \frac{StoredEnergy}{PowerLoss} \tag{3.11}$$

Hence, quality factor equals to the ratio of stored energy while oscillating to the energy dissipated. Another equation alternative to Equation 3.11 for the quality factor is that the ratio of imaginary part of the impedance to real part of the impedance.

$$Q = \frac{Im(Z)}{Re(z)} \tag{3.12}$$

Method of checking Q factor is by using two-port equivalent circuit of the transformer and then short circuiting the output port [5]. After running the circuit in frequency domain, Q factor can be calculated easily by dividing imaginary impedance to real impedance.

The saturation of core means decreasing the inductance value of an inductor. The maximum saturation current of a core can be estimated by using the formula given by;

$$I_{max} = \frac{B_{max} * l_g}{n * \mu_0} \tag{3.13}$$

B_{max} is the maximum core flux density, l_g is air gap length, μ_0 is permeability of air and n is the turn ratio. If the saturation flux density B_{max} is bigger, it leads the inductance value to decrease dramatically, which eventually becomes short circuit [36].

4. EXPERIMENTAL SETUP AND RESULTS

In this chapter, experimental setup and results are discussed in detail. Firstly, selection of components is examined in Section 4.1. Secondly, design implementation is explained in Section 4.2. Finally, measurements result is presented by figures and graphs in Section 4.3.

4.1 Component Selection

In order to meet the goals of high efficiency, high speed converter, modeling and selecting components need paying attention. Package inductances, gate capacitances and internal resistances cannot be ignored since they become significant in very high speed ranges [31]. All of them are selected by examining their datasheets and frequency responses. Input voltage range is set to 3.8 V. In the following subsections, selection of transistors (Subsection 4.1.1), capacitors (Subsection 4.1.2), filter inductor (Subsection 4.1.3)and transformer (Subsection 4.1.4) are explained.

4.1.1 MOSFETs

Recently, in the market, the low R_{ds} ,on value MOSFETs are available but the trade-off is increased gate capacitance. At low frequencies, this capacitance is insignificant, however at high frequency level, it becomes powerful. Figure 4.1 presents parasitic components that a discrete MOSFET includes. R_g is the gate resistance and R_{oss} is the drain to source resistance. C_{gd} and C_{gs} together forms the gate capacitance. L_g, L_d and L_s represent inductances that occur in metalization or packaging.

Moreover, in MOSFET datasheets, capacitance values are denoted as C_{iss}, C_oss and C_{rss}. The corresponding equation for them is given by:

$$C_{iss} = C_{gs} + C_{gd} \quad , C_{oss} = C_{gd} + C_{ds} \quad , C_{rss} = C_{gd} \tag{4.1}$$

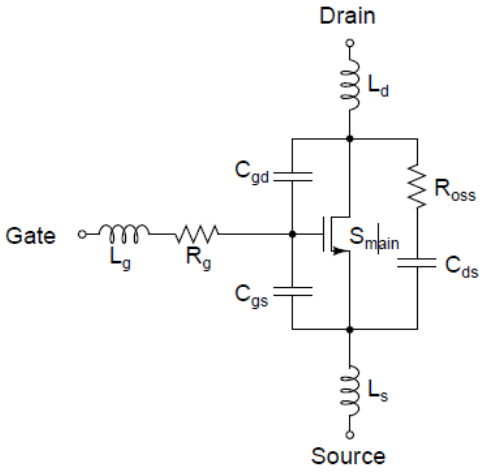

Figure 4.1 *Parasitics of a discrete MOSFET*

The list of used MOSFETs is given in Table 4.1. The V_{ds}, R_{ds}, C_{iss} values are presented when the junction temperature is 25^oC

Table 4.1 *Selected MOSFETs*

Component	Model Name	V_{ds}	R_{ds}	C_{iss}
M1, M2, M7, M11	Si1315DL[40]	8 V	0.28 Ω	112 pF
M3, M4, M8, M12	SiB312DK[39]	20 V	0.18 ω	95 pF
M9, Q2	Si1553CDLP[41]	20 V	0.7 ω	43 pF
M10, Q3, Q4	Si1553CDLN[41]	20 V	0.3 ω	38 pF
M13, M14, M15, M16, M17, Q1	Us6m1_n[34]	30 V	0.25 ω	70 pF
M18, M19	Vt6m1_p[35]	20 V	NA	15pF

After carefully analyzing the datasheets, a test bench for frequency response analysis is built in LTSPICE to carry out simulation on them. Figure 4.2 shows the test bench for an NMOS transistor.

This bench is employed to evaluate the performance of a transistor. F_t is a figure of merit for transistor performance [15]. F_t is specified as the unity gain frequency of a transistor's short circuit current gain. In order to calculate short circuit current gain, the drain is connected to a power supply. Then, current gain of the MOSFET is needed. Basically, dividing the drain current to the gate current will give the result. Since, in normal operating conditions, current flows from drain to source, and only leakage current goes through the gate. If the ratio of the drain current and gate current equals to one, it means that transistor does not work anymore. In dB

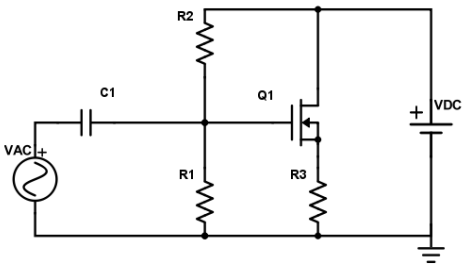

Figure 4.2 *Test bench for frequency response analysis*

scale, one equals to zero. Hence, by looking for the point where the curve intercepts 0 dB, operating frequency range of the transistor can be analyzed.

In Figure 4.3, the frequency responses of the chosen transistors are given. As can be easily noticed, none of them intercepts zero at our target frequency, which is 3.5 MHz. All transistors work until around 1 GHz range. However, since these are not ideal, better to consider their last operating point is around 100 MHz.

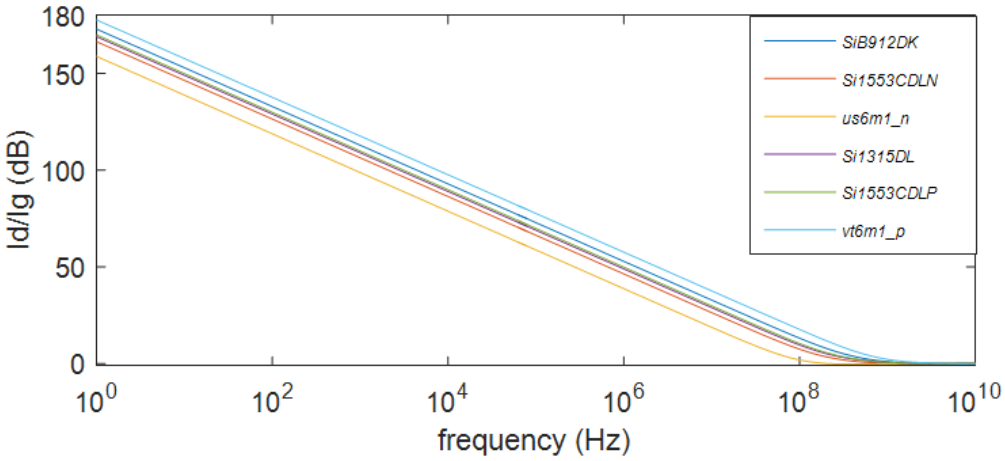

Figure 4.3 *Frequency response of the MOSFETs*

According to [33] there is also a way to calculate the maximum operating frequency by hand. The equations for this calculation are given by:

$$f_t = \frac{gm}{2 * \pi * C_{gs}} \tag{4.2}$$

$$f_{max} = \sqrt{\frac{f_t}{8 * \pi * R_g * C_{gd}}} \tag{4.3}$$

gm stands for transconductance and R_g for gate resistance, which can be easily found in datasheets. Moreover, to verify our MOSFETs, some hand calculations are carried out. Table 4.2 represents f_t and f_{max} values for chosen transistors. To sum up, all transistor models are convenient to be employed in high frequency applications.

Table 4.2 *MOSFET Frequency ranges*

Model Name	F_t	f_{max}
Si1315DL[40]	6.6 Ghz	970 MHz
SiB312DK[39]	5.6 GHz	2.8 GHz
Si1553CDLP[41]	3.8 GHz	1.2 GHz
Si1553CDLN[41]	7.4 GHz	1.8 GHz
Us6m1_n[34]	2.74 GHz	953 MHz
Vt6m1_p[35]	1.4 GHz	1.9 GHz

4.1.2 Capacitors

When selecting a capacitor, voltage rating, size, cost and dynamic response should be taken into account. Especially, for filtering purpose, dynamic load response and ripple effect is important. In order to obtained improved transient response and accomplished energy storage, low-ESR capacitors are more beneficial. On the other hand, low overall impedance at the output may hurt the dynamic response of the converter [7]. Hence, it is good to think both sides of low-ESR capacitors when making a selection.

Ceramic Capacitors, known as multi-layer chip capacitors (MLCC), are the most common capacitors. They generally used in high-frequency low-loss applications [25]. They are capable of handling high frequency and high level of electrical noise.

In our converter, C_r capacitors are employed as voltage divider. Since they are identical, the voltage across them is the same. The lower end voltage is $Vd/2$ upper end voltage is Vd, therefore the mid voltage is $3Vd/4$. At the filtering part, we utilize 3 parallel capacitors instead of one single capacitor. The overall capacitance value of the 3 parallel capacitor is the same as we use only one capacitor. The

reason for that is keeping the capacitance value the same but reducing the overall impedance. The other reason is to diminish the stress over the capacitors, the same amount now can be divided into 3 capacitors.

Table 4.3 shows the selected ceramic capacitors, their capacitance values and voltage capabilities.

Table 4.3 *Selected Capacitors*

Component	Model Name	Capacitance	Rated voltage
C_r	GRM155R71H122KA01 [27]	1.2 nF	50 Vdc
C_{f1}	GRM155R71H821KA01 [29]	0.82 nF	50 Vdc
C_{f2}	GRM155R71H391KA01 [28]	0.39 nF	50 Vdc
C_{f3}	GRM155B11E102KA01 [26]	1 nF	50 Vdc

Overall filter capacitance value is around $2.21nF$ and with very low-ESR value. Another test bench is set up for measuring their frequency responses. Figure 4.4 represents the test bench for capacitors. Basically it is an AC analysis ,a current source feeds the capacitor. Frequency is sweeping from 1 Hz to 10 GHz. The resulting waveform is in Figure 4.5.

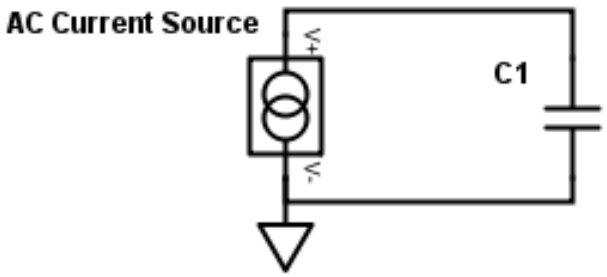

Figure 4.4 *Test bench for capacitor frequency analysis*

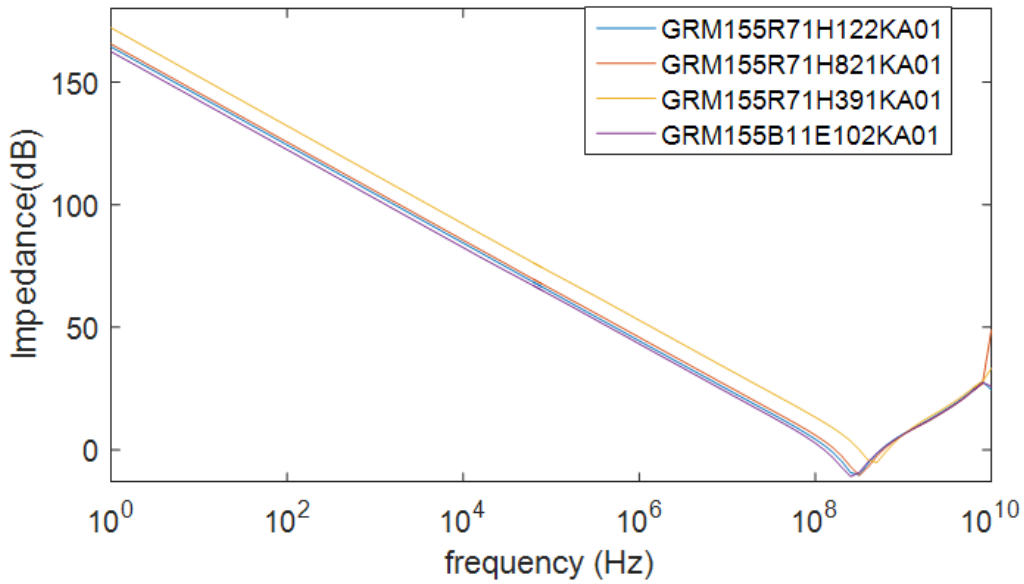

Figure 4.5 *Frequency response of the Capacitors*

From Figure 4.5, it can be interpreted that their resonance frequency is around 100 MHz, which means that they work perfect, lossless, at that frequency level. At our frequency level, 3.5 MHz, they have some *ESR* value, but this value will be insignificant when three filter capacitors are connected in parallel.

4.1.3 Filter Inductor

There are couple of crucial factors when choosing a filter inductance. Maximum current at the output of the converter should be small or equal to the rated current of the inductor. Otherwise the inductor will saturate, which results in reduction of the inductance value. The certain level of cutback in inductance will increase the ripple amount. The value of the inductor should be chosen carefully. Dynamic load response may go negative in case of huge inductance [16]. It should be less than mili-Henry range. The greater the inductance, the slower dynamic response. In case picking up a large inductance, it should be compensated by using large capacitors. Table 4.4 shows the selected filter inductance. It includes inductance value, internal resistance and nominal current. Obviously internal resistance is really small, therefore, its conduction losses are limited.

Similar test bench is set up for measuring its frequency response. Figure 4.6 repre-

Table 4.4 *Filter Inductor*

Component	Model Name	Inductance	Internal Resistance	Rated Current
L_f	HL-8113 [17]	60 μH	5 mΩ	20 A

sents the test bench for the filter inductance. It is an AC analysis; a voltage source feeds the inductor. Frequency is sweeping from 1 Hz to 10 GHz. The resulting waveform is in Figure 4.7.

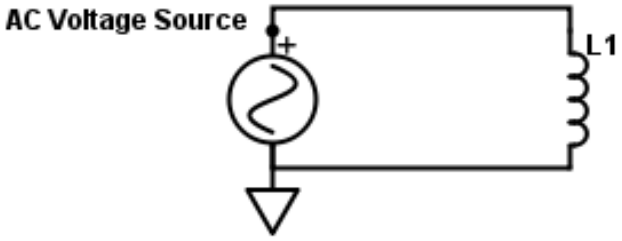

Figure 4.6 *Test bench for the inductor frequency analysis*

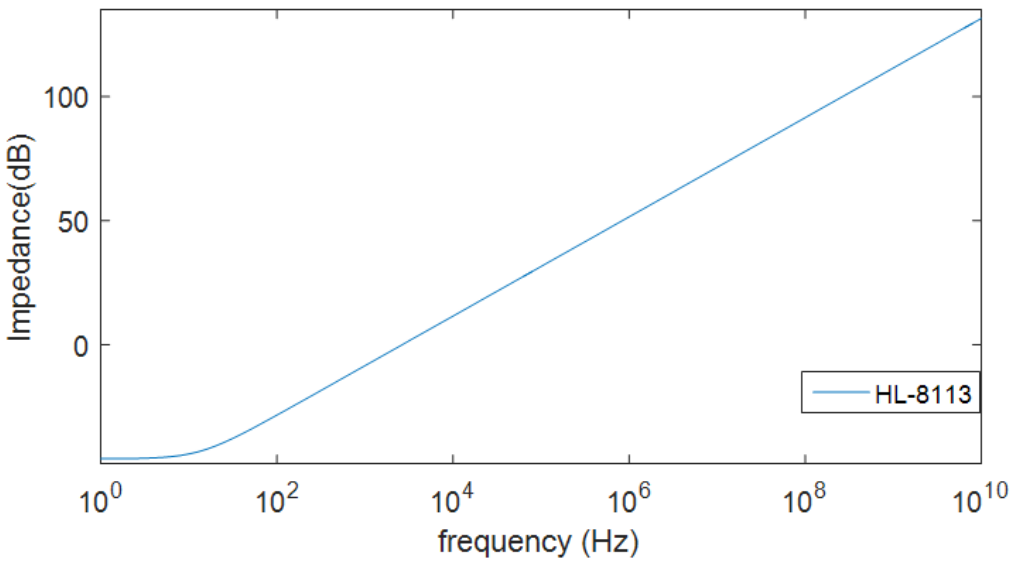

Figure 4.7 *Frequency response of the Filter Inductor*

Clearly its resonant frequency is around *100 kHz*, and after that range it operates as an inductor.

4.1.4 Transformer

The use of transformer is explained already in Subsection 3.3.6. Now, the selection procedure will be discussed. For high frequency ranges, it is a demanding work to build a transformer and model it. In addition, finding a suitable transformer and its model in the market challenging. Since inductance is one of the important component that defines the speed of the converter, the model should be chosen carefully. Table 4.5, shows some the specifications of the selected transformer.

Table 4.5 *Transformer*

Component	Transfomer
Model Name	750312547 [42]
Primary Inductance	1 μH
Primary Resistance	30 mΩ
Secondary Resistance	48 mΩ
Turn Ratio	1 : 2.4

Moreover, a test bench is constructed and measured it quality factor and frequency range. Figure 4.8 includes demonstration transformer test bench.

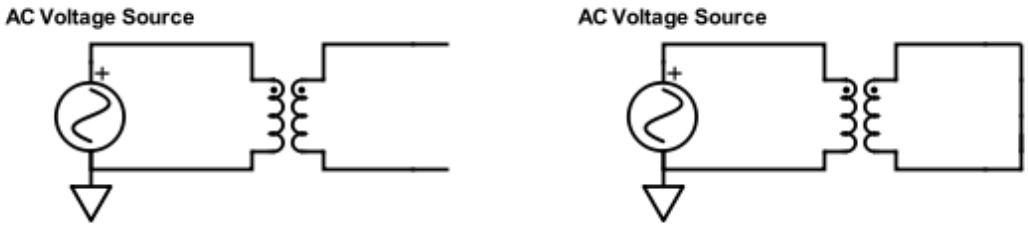

Figure 4.8 *Test bench for transformer*

The one at the right in Figure X, for open circuit test, the left one is for short circuit test. Figure 4.9 shows the calculation result of the Equation 3.12 for Q factor.

The peak point in the waveform in Figure 4.9 for open circuit analysis is 13.8 and for short circuit is 1.95, therefore the best frequency point for the transformer is around 500 kHz. Operating this transformer beyond that point only will cause more power losses, because of the increase in the resistance, whereas it does not affect its operation.

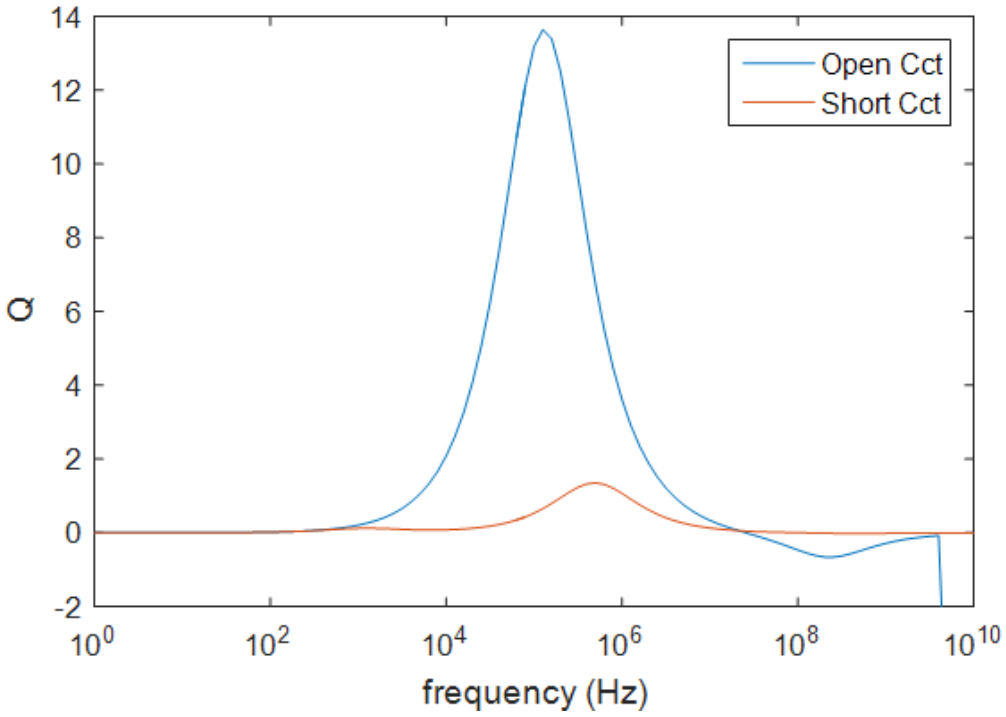

Figure 4.9 *Q Factor of the transformer*

4.2 Circuit Design

This section describes how the circuit implemented in LTSPICE. In order to prevent problems in passing to implementation on a PCB, the realistic model of the components is used. Moreover, trace, battery and contact parasitics are taken into account. In the subsections battery modeling (Subsection 4.2.1), gate drive circuitry (Subsection 4.2.2), parasitics (Subsection 4.2.3) and overall design (Subsection 4.2.4) of the circuit will be studied.

4.2.1 Battery Modeling

In the circuit two different voltage value is employed *Vd* and *Vd/2*. Batteries and solar cells are considered as non-ideal voltage sources, which means they include internal resistance [30]. In general, they comprise only internal inductance and resistance. To demonstrate the effect of internal resistance, the circuit in Figure 4.10 is built and the waveforms in Figure 4.11 is obtained as a result.

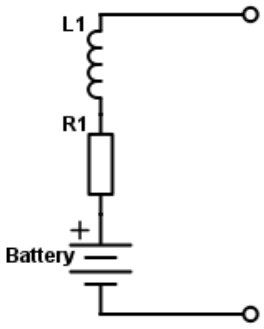

Figure 4.10 *Realistic Battery Model*

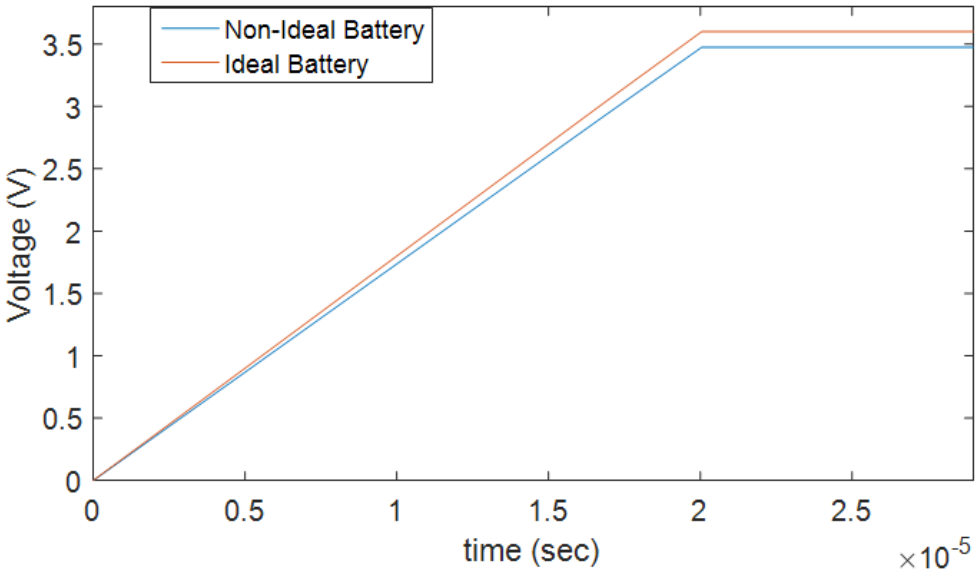

Figure 4.11 *Output voltage of a battery, ideal model (red) and realistic model (blue)*

As it can be clearly seen, with realistic model, it has voltage drop due to internal resistance and some time delay due to internal inductance.

In order to provide *Vd/2* voltage to the circuit, a voltage divider capacitor pair is utilized rather than a separate voltage source. By this way the setup cost is reduced. Because of the fact that, using voltage divider resistors would cause power losses,

voltage divider capacitors are preferred instead. Two capacitors are connected in series and total voltage on them is *Vd*. *Vd/2* is received from their connection point, since they are identical. Two ceramic capacitors, *8.2 nF*, are used for that purpose. Figure 4.12 shows together with divider circuit and the voltage at the midpoint.

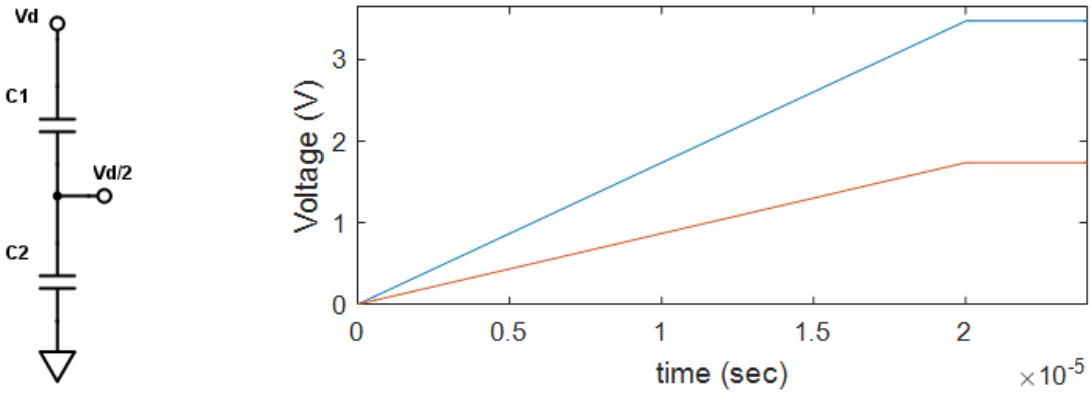

Figure 4.12 *Capacitor Divider (Left), Midpoint voltage (Right)*

Since capacitors needs time to charge and discharge *Vd/2* lags *Vd*. As an advantage, they consume insignificant amount of power, on the contrast power consumption of the resistors cannot be ignored.

4.2.2 Gate Drive Circuitry

At first, the components which consumes most power is investigated. After seeing that the main PMOS and NMOS side inverter dissipates considerable amount, some gate drive techniques are applied to that parts of the converter.To the main PMOS gate, last inverter stage of the buffer is removed, and resonant gate drive and dead-time latch circuitry are built together, instead. Moreover, between inverter stages in the NMOS side, a resonant gate drive is constructed. Explanation of these techniques are already studied in (Subsection 3.3.4).

Inductor value should be small in resonant gate drive in order not to behave as a current source. However making it too small may cause it to act as a short circuit. The desired amount of delay is adjusted by looking at the gate drive signals. With considering certain margins, these circuits are integrated into the converter.

4.2.3 Parasitics

In electrical circuits, parasitics are inevitable, meaning that they are formed by any electrical component. Especially at high frequencies they arise, and unsettle the circuit. They are mostly in form of parasitic capacitance, resistance and inductance. In order to avoid inaccuracy and instability, parasitics need to be estimated.

To form an parasitic inductor, an alteration in the current flow on a conductor is adequate [1]. Parasitic capacitance occurred due to the closeness of two conductive plate. Non ideality on a trance or copper wire causes parasitic resistance. In the design for the simulation, most of the parasitics estimated by using components real models.

A small amount of resistance and inductance is added to grounding path, since in reality ideal ground does not exist. Moreover, since there is no such a thing as ideal conductor in real life, leakage resistance for paths and trances are also considered.

At the input side, to reduce non-idealites rails to ground method is applied. It means, using parallel capacitors from source voltage to ground [6]. It draws the AC signal, occurred due to parasitics, to the ground and supply DC signal to the rest of the circuit.

4.2.4 Overall Design

After carefully considering all components and parasitics the final schematic of the circuit is in Figure 4.13. As clearly seen from it, supply voltages are designed, all parasitics are included, and ground path is modelled deliberately.Table 4.6 is the list components, which are utilized in the simulations.

In Figure 4.13 all sub circuits are interconnected via labels. In the coming section, waveforms of these parts will be presented.

Table 4.6 *Component List*

Component	Value/Model	Component	Value/Model
Rs1	180 mΩ	Ls1	25 nH
R2, R3, R7	10 mΩ	L1	215 nH
R4, R5, R6	5 mΩ	L2, L3	100 pH
R8	3 mΩ	L4	$MPZ1005S300CT000\_s$
RL	10 Ω	L5	60 uH / HL-8113
M1, M2, M7, M11	Si1315DL	L6	10 pH
M3, M4, M8, M12	SiB912DK	C3	GRM155D80E475ME47
M13, M14, M15, M16, M17, Q1	Us6m1_n	C4	2 pF
M9, Q2	Si1553CDLP	C5	GRM152D70E104KE19
M10, Q3, Q4	Si1553CDLN	C6	C0603X7R1E101K030BA
M18, M19	Vt6m1_p	C7	GRM155R71E222KA01
C1	GRM155R71H821KA01	C9, C10	GRM155R71E822KA01
C2, C8	GRM155R71H821KA01	C9, C10	GRM155R71E822KA01
D1, D2, D3, D4	1N914	L7, L8	180, 210 nH
Transformer	75031257_Würth	C12	GRM155B11E102KA01

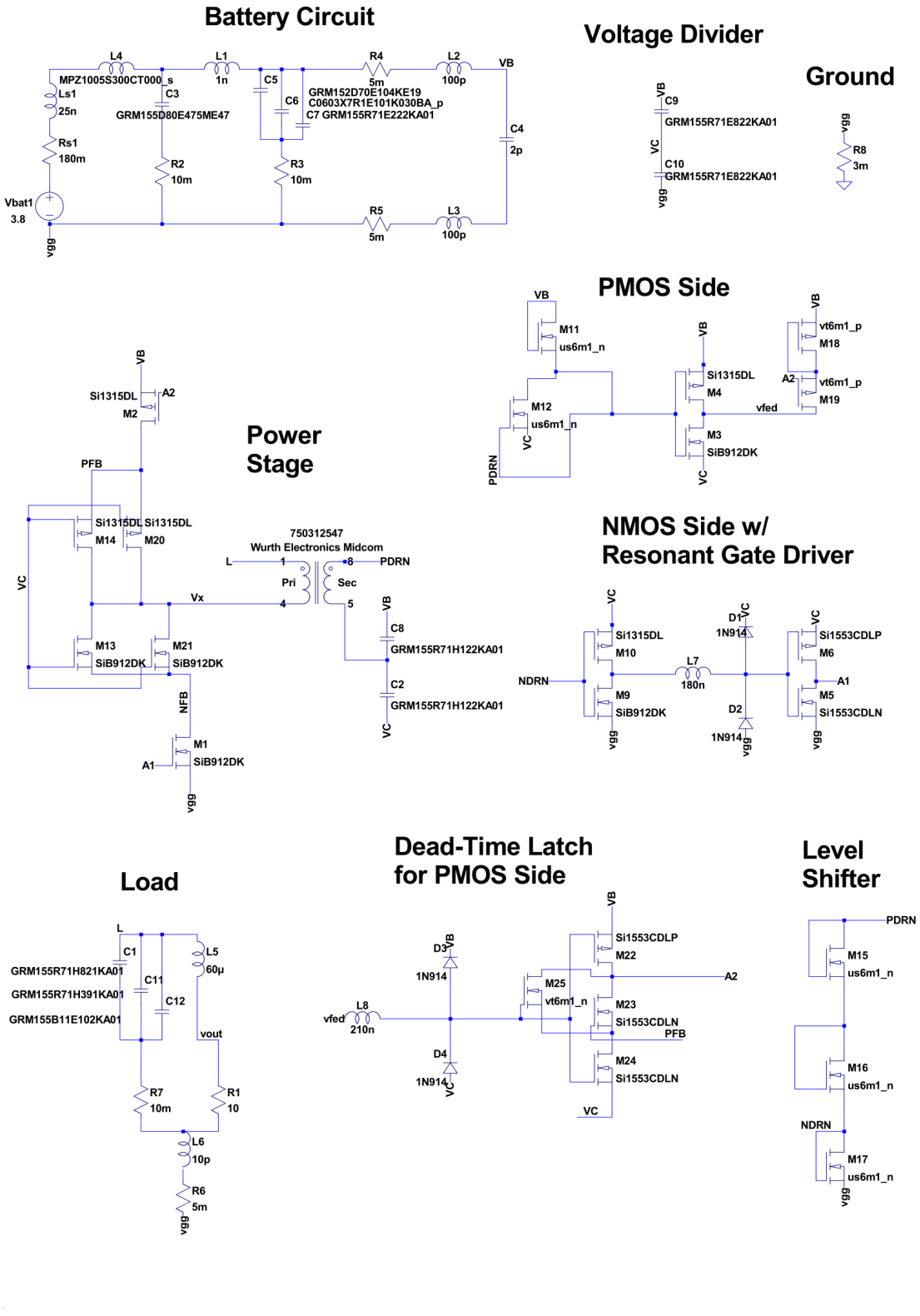

Figure 4.13 *Overall Converter Circuit*

4.3 Results and Measurements

All corresponding waveforms are given in below subsections separately. How change in some parameters affects the circuit function in terms of speed and power loss is examined in detail. Finally, how much power is consumed by each component is presented by a graph explicitly.

4.3.1 Battery Circuitry

In Figure 4.13, a detailed battery circuitry is shown. The supply point *VB* powers the converter. *VC* supplies half of the powering signal. Battery voltage is *3.8 V* and the voltage at the *VB* point is reduced due to the trace losses and internal resistance. Transient time for the *VB* signal is *22 μsec*, for *VC* is *23 μsec*, on the contrast for battery is *20 μsec*. Figure 4.14 includes voltage waveforms when *3.8 V* is applied. In the figure VB and VC point voltages can be clearly seen.

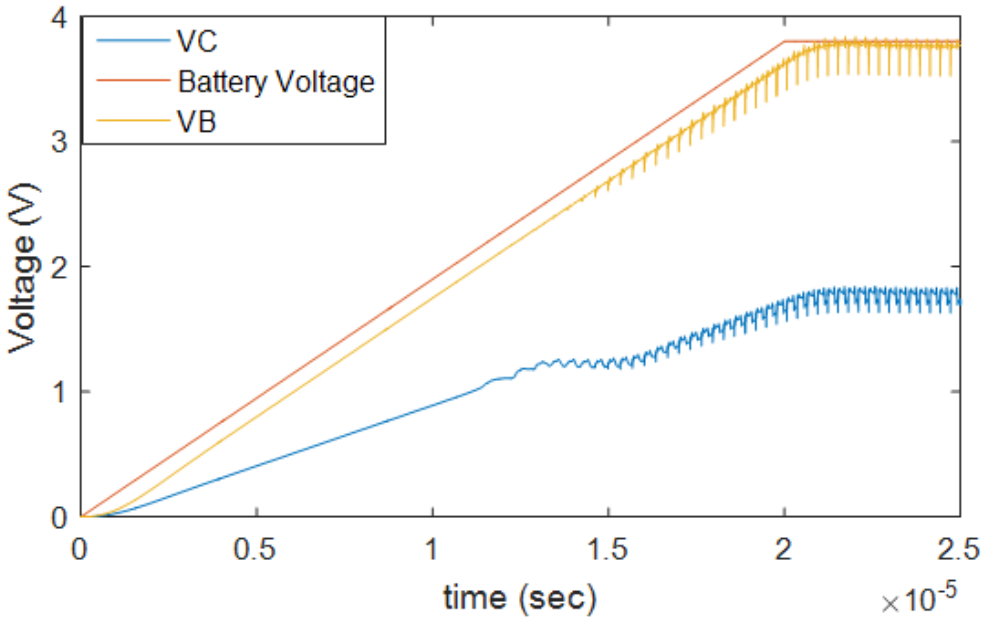

Figure 4.14 *Battery Circuit Waveforms*

4.3.2 Power Stage and Switching Point

(Subsection 4.3.2) The effect of changing input voltage, and load to Vx switching point is presented in Figure 4.15. The duty cycle and speed is highlighted in Table 4.7.

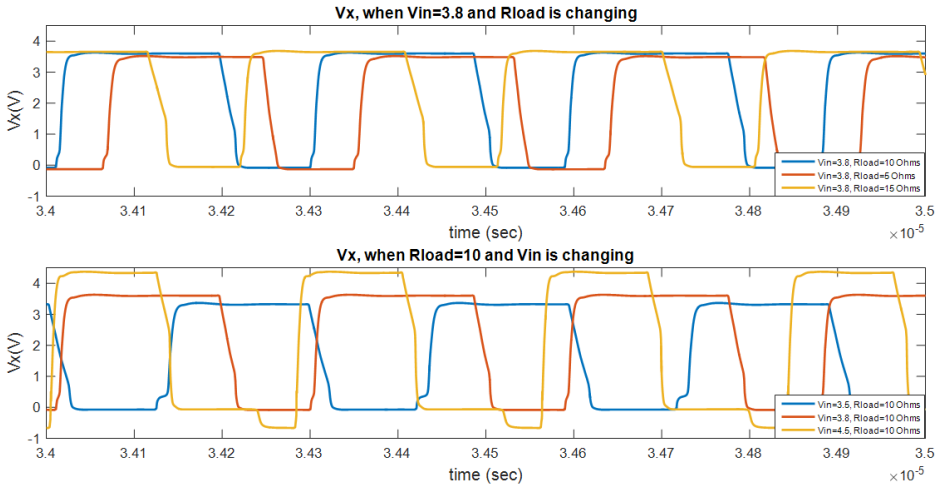

Figure 4.15 *Switching Point Voltage Waveforms under different conditions*

Table 4.7 *Duty Cycle and Speed of the Circuit*

Vin (V)	R_{Load} (Ω)	Duty Cycle (%)	Speed (MHz)
3.5	10	46	3.35
3.8	**5**	**57**	**3.5**
3.8	**10**	**55**	**3.46**
3.8	15	53	3.41
4.5	10	48	3.63

Increase in duty cycle means increased output power as its average would be higher than the others. The results from Table 4.7 and Figure 4.15, shows that increase in the input voltage makes the circuit faster whereas decreases the output power. Increasing the load slows down the circuit, on the contrast increases the output power. Evidently, having $Vin = 3.8V$ and $R_{load} = 5\Omega$ seems the best option. However holding small load at the output may produce instability. Hence it is better option to have 10Ω load at the output in case of any instability occurrences.

4.3.3 Feedback Circuitry

The changes in the signal after transferred to feedback circuitry is shown in Figure 4.16,Figure 4.17, Figure 4.18 and Figure 4.19. Figure 4.16 shows the signal on the secondary of transformer and it shows that the average current on it is zero. This signal then goes to the PMOS side buffer and the level shifter for NMOS side buffer. Figure 4.17 depicts the waveform for after and before level shifter block. After level shifter signal will be shaped by NMOS side buffer later. The shaped signal is shown in Figure 4.18 along with the process.Figure 4.19 presents the signal goes to the main PMOS, and how it grows as a perfect pulse shape by the help of PMOS side buffer.

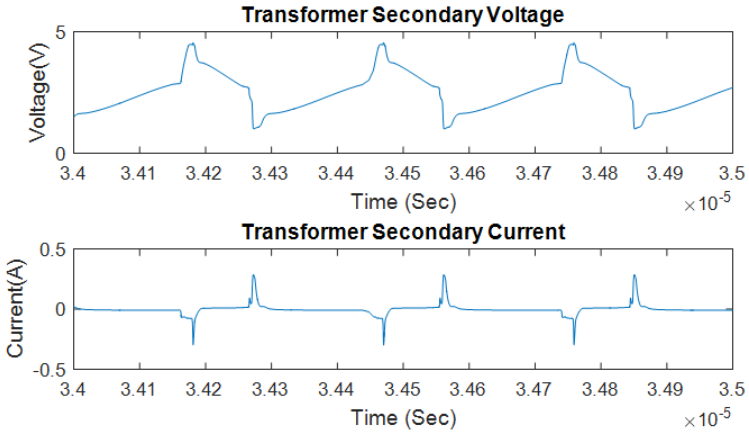

Figure 4.16 *Transformer Secondary Voltage and Current*

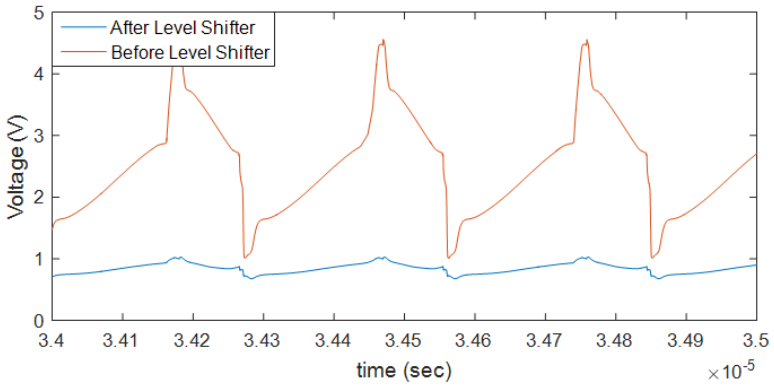

Figure 4.17 *Level Shifter*

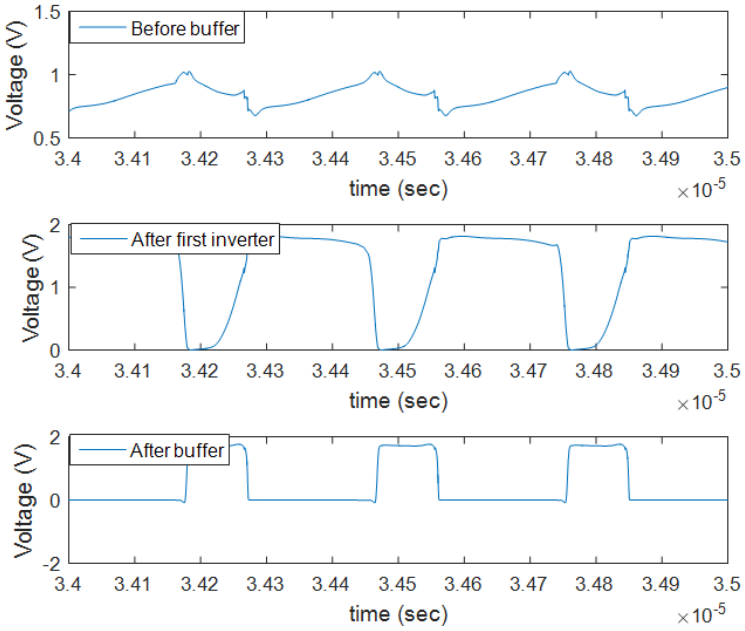

Figure 4.18 *NMOS Buffer operation*

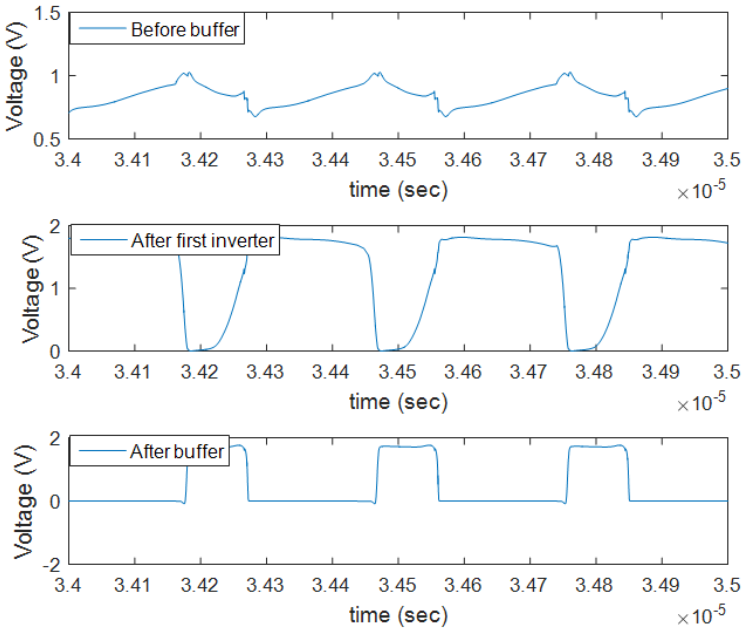

Figure 4.19 *PMOS Buffer operation*

Figure 4.20 shows the comparison of PMOS and NMOS gate drives. It is important to have them not overlapping any of the edges in order not to consume energy as conduction loss. The left-hand edge looks ideal however, right-hand edge is slightly problematic. For such a short time, the main PMOS and NMOS are switched ON at the same time, which results in short circuit connection between power supply and ground. The flow of current in that time period causes conduction losses. In order to avoid, PMOS should be turned off before NMOS is ON. In order to do that, gate drive techniques are introduced to the converter. As described before, resonant gate drive circuit integrated to the NMOS buffer stage, between inverters. For the PMOS stage, second inverter is replaced with the dead time latch circuitry and the resonant gate drive circuit is connected between them. The result is shown in Figure 4.21. As comparison to Figure 4.20, now, both edges have enough margins and delays so that, the transistors are not switched ON at the same time. The dead-time is *5 ns* now between falling edges.

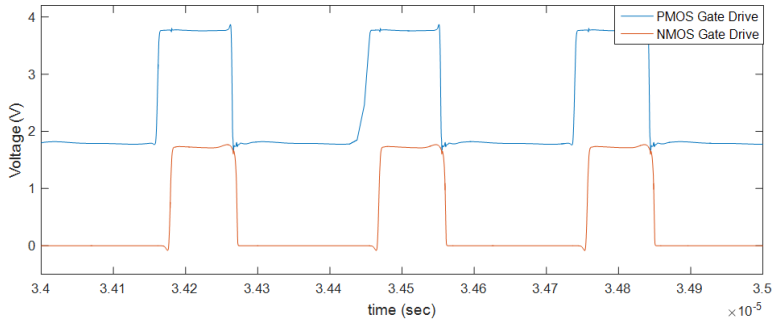

Figure 4.20 *Main PMOS and NMOS gate signals without any drive circuitry*

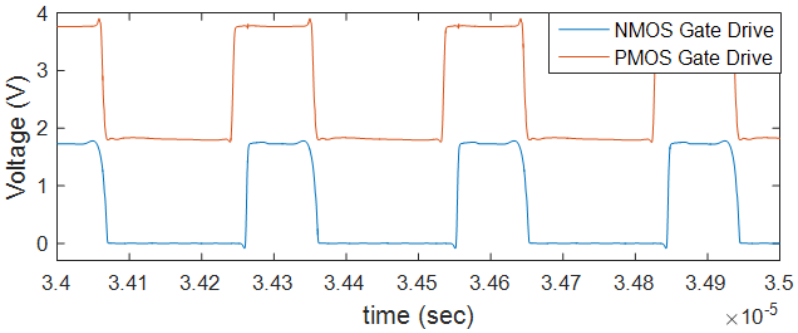

Figure 4.21 *Main PMOS and NMOS gate signals with drive circuitry*

4.3.4 Load Analysis

Below, effect of changing load and input voltage to efficiency and ripple voltage is presented by Figure 4.22, Figure 4.23 and Table 4.8.

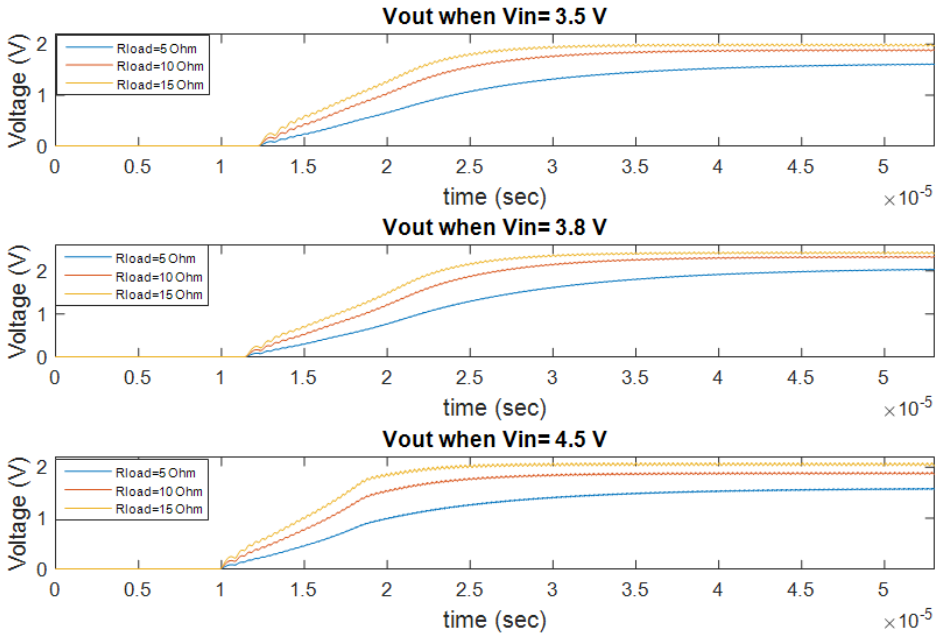

Figure 4.22 *Output voltage with different parameters*

Table 4.8 *Comparison of different V_{in}, R_{Load} pairs*

V_{in} (V)	R_{Load} (Ω)	P_{out} (mW)	P_{in} (mW)	η(%)	V_{out} (V)	V_{ripple} (mV)
3.5	5	526	918	58	1.63	13
3.5	10	352.94	614.22	57.4	1.88	26
3.5	15	261	501	52.1	1.97	41
3.8	**5**	**812**	**1092**	**74.4**	**2**	**12**
3.8	**10**	**518**	**700**	**74**	**2.25**	**27**
3.8	15	390	587	66.5	2.41	40
4.5	5	504	1026	49	1.59	15
4.5	10	354	819	43	1.88	37
4.5	15	283	731	39	2.1	54

From the given information, regardless of the input voltage level, increasing load decreases output and input powers and hence efficiency, increases output voltage and

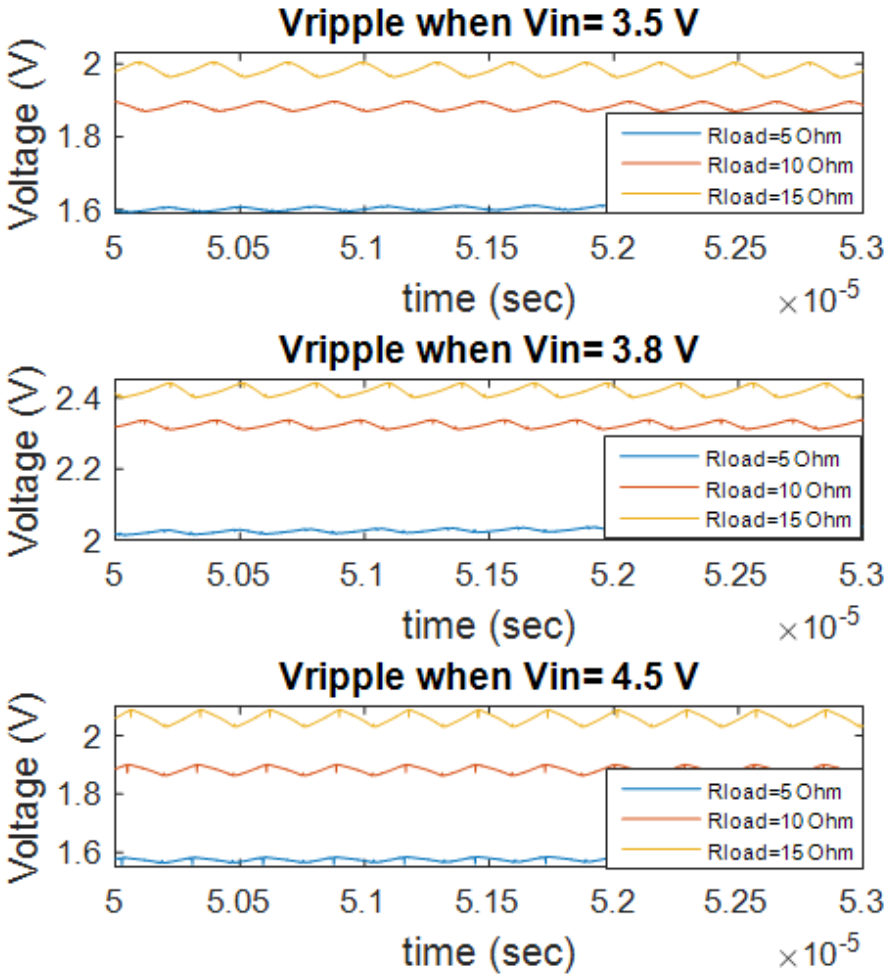

Figure 4.23 *Output voltage ripple with different parameters*

ripple of it. For the input voltage it is not convenient to make a linear estimation since there seems like employing rather than *3.8 V* hurts the efficiency and ripple.

A user can freely choose a pair of input voltage and load, depending on the priorities such as efficiency, speed or voltage regulation. The best voltage value, however seems like *3.8 V* and load value is *5* Ω. As it is mentioned before in (4.3.2), having *5* Ω load at the output can make the system unstable, since it may be not adequate for stability. Therefore, choosing *10* Ω load at the output would be better in terms of stability issue.

4.3.5 Power Losses

When $V_{in} = 3.8V$, $R_{Load} = 10\ \Omega$, the losses are analyzed in the converter. The bar chart in Figure 4.24, depicts the elements cause loss in the circuit. The data is taken when gate drive techniques (Resonant Gate Drive and Dead-Time Latch) are employed.

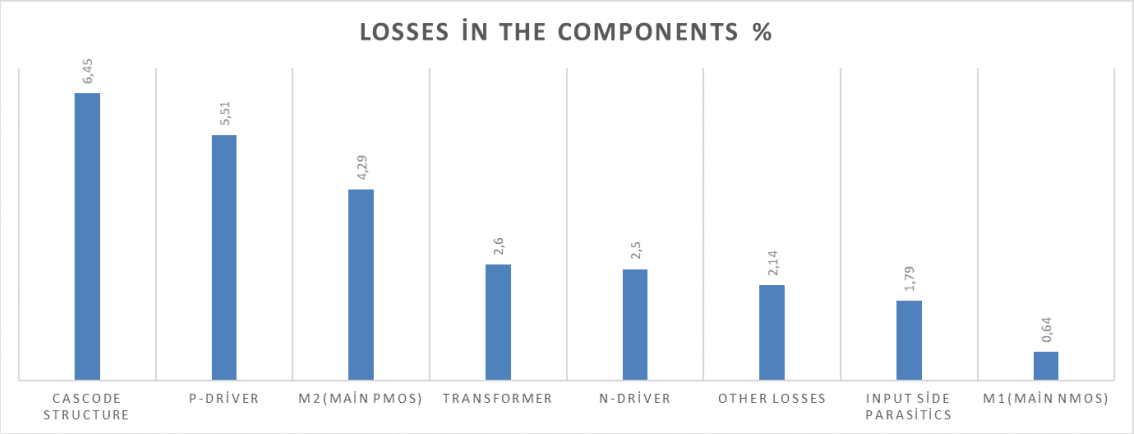

Figure 4.24 *Losses in the converter*

As can be clearly seen, cascade structure, PMOS side, and the main PMOS are the components which are responsible for the major power consumption. Further precautions might be taken in the future and the circuit could work with even higher efficiency. The gate driver circuits can be improved to allow more convenient gate drive. On the contrast, the losses caused by parasitic of elements are inevitable, as they appear at high frequencies. Previously, in the simulations without any gate drive circuitries, the efficiency is around *70 %* . Now, by the help of resonant gate drive and dead-time latch techniques, efficiency steps up to *74 %*.

5. CONCLUSIONS

This thesis developed a self-oscillating dc/dc converter topology suitable for high frequency applications on a PCB with higher efficiency by the help of resonant gate drive and dead-time latch circuitry. The design presents a fast, fixed duty ratio and highly efficiency converter cell, which is controlled by using an inductive feedback. This approach has some advantages of separating the power stage circuit from the control, enabling high efficiency at light load, as illustrated in the simulation results. The high switching frequency of the converter provides us to utilize small passive energy storage elements. Moreover, reduced weight, size, and cost are the other benefits of the converter.

Power stage of Self Oscillating DC/DC converter is implemented by a buck converter consists of four MOSFET switches (two PMOS and two NMOS). Reason of using cascading MOSFET structure is to enable them to be used with voltages higher than their breakdown. The primary side of the transformer is employed as switching inductor, in which power calculations take place. Finally, the switched signal is filtered with a filter and feeds the resistive load.

Feedback and control side consist of different blocks which help to maintain decent signal waveforms at the gates of main switches. The feedback signal comes from the secondary side of the transformer. Inductive feedback features fast response. This signal feeds buffer stages of the gates. For NMOS side this signal needs to minimized. A level shifter is employed for that purpose. After the signal is shifted down, it is flattened and squared by the buffer stage and it feeds the main NMOS gate. For PMOS side, the feedback signal goes directly to the buffers and feeds the main PMOS gate.

Resonant gate drive and dead-time latch circuits are integrated in the feedback stage of the converter. Resonant gate drive circuit, basically an LC circuit, recovers the energy dissipated for charging and discharging transistor capacitances. Dead-time latch circuitry adjusts the time to prevent conduction loss between power supply and

ground due turning ON of both switches. Since the main PMOS switch consumes considerable amount of power, a latch circuitry inserted to its gate. By that way, it postpones switching it ON just for a short time to ensure that the main NMOS switch is OFF. Resonant gate drive circuitries are accommodated to PMOS side before the latch and to NMOS side in the buffer. All component limits and working conditions are analyzed by simulations, data sheets and calculations. Parasitics are carefully studied and located into the design in order to make it available for PCB implementation.

Experiments are conducted in LTSpice software. The real life parameters of the components are used in simulations in order not to face with unexpected results on the PCB. Different input voltage and load pairs are utilized in the simulations. The best results are achieved with input voltage of 3.8 V and load value of 10 Ω. The observed results are having 74% efficiency with 3.5 MHz and 2.2 V output voltage. Output voltage ripple is limited to 27 mV. Before applying gate drive techniques (resonant gate drive and dead-time latch), the efficiency was 70.1%. After setting up these two circuitries efficiency is amended by 4% in overall.

The first target in the near future is implementing the converter on a PCB. As future work, instead of normal transformer, coupled inductor can be employed as it will reduce core losses and increase the speed of the converter further. Higher input voltage level can be applied and as a result higher power level can be reached, if all parameters are arranged properly.

BIBLIOGRAPHY

[1] "Parasitic inductance," http://www.capacitorguide.com/parasitic-inductance/.

[2] R. Akbar, "High speed fully monolithic self triggered dc-dc buck converter," Master's thesis, Tampere University of Technology, Finland, 2013.

[3] R. Akbar, I. Filanovsky, J. Jarvenhaara, and N. Tchamov, "An asymmetric vhf self-oscillating dc-dc converter with integrated transformer," *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1–4, Aug. 2015.

[4] B. Andreycak, *Zero Voltage Switching Resonant Power Conversion*, Texas Instruments. [Online]. Available: http://www.ti.com/lit/an/slua159/slua159.pdf

[5] Y. Aoki, "Q-factor definition and evaluation for spiral inductors fabricated using wafer-level csp technology," *IEEE Transactions on Microwave Theory and Techniques (Volume:53 , Issue: 10)*, pp. 3178–3184, Oct. 2005.

[6] J. Ardizzoni, "A practical guide to high-speed printed-circuit-board layout," *Analog Dialogue*, Sept. 2005.

[7] J. Arrigo, "Input and output capacitor selection."

[8] P. Barrade, "Switched mode converters," http://cas.web.cern.ch/cas/Warrington/PDF/Cours%20CERN%20Barrade%202.pdf.

[9] P. Callemeyn and M. Steyaert, "Monolithic integration of a class de inverter for on-chip resonant dc-dc converters," *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, pp. 325–328, Sept. 2012.

[10] Y. Chen, F. C. Lee, L. Amoroso, and H. Wu, "A resonant mosfet gate driver with efficient energy recovery," *IEEE Transactions on Power Electronics (Volume:19 , Issue: 2)*, pp. 470–477, March 2004.

[11] C. H. Chia, P. S. Lei, R. C. H. Chang, and T. Y. Kao, "A high-speed dc-dc converter with high efficiency at wide loading range," in *Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference*. IEEE, 2013, pp. 925–928.

[12] "Lecture 34 high frequency transformer," http://www.engr.colostate.edu/ECE562/98lectures/l34.pdf, Colorado State University.

[13] "Lecture 9 buck boost converter design," http://www.engr.colostate.edu/ECE562/98lectures/l09.pdf, Colorado State University.

[14] P. A. Dahono, "A control method for dc-dc converter that has an lcl output filter based on new virtual capacitor and resistor concepts," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual.* IEEE, 2004, pp. 36–42.

[15] J. del Alamo, "Course materials for 6.720j integrated microelectronic devices," May 2007.

[16] *Output Filter Design Note 011*, Ericsson. [Online]. Available: http://www.jbkj.com.cn/Ericsson/pdf/andn/dn011_r2a_0904.pdf

[17] Hurricane, "Hl8113," http://www.hurricaneelectronics.com/filterInductor.php.

[18] Infineon, "Coolmos benefits," http://www.infineon.com/dgdl/Infineon+-+Product+Brochure+-+PowerMOSFETs+-+CoolMOS%E2%84%A2+-+Benefits+in+hard+and+soft+switching+SMPS+topologies.pdf?fileId=db3a3043338c8ac80133aca62ba63047.

[19] *Application Note AN-937*, International Rectifier. [Online]. Available: http://www.infineon.com/dgdl/an-937.pdf?fileId=5546d462533600a40153559ea1481181

[20] J. Jarvenhaara, H. Herzog, S. Sipila, J. Tian, I. M. Filanovsky, and N. T. Tchamov, "High speed dc-dc dead time architecture," *IEICE Electronics Express*, Sept. 2015.

[21] S. Keeping, "Voltage- and current-mode control for pwm signal generation in dc-to-dc switching regulators," *ArticleLibrary by Digi-Key Electronics*, Oct. 2001.

[22] ——, "Understanding the advantages and disadvantages of linear regulators," *ArticleLibrary by Digi-Key Electronics*, May 2008.

[23] V. Kim, *How to Design 10 kHz filter (Using Butterworth filter design) Application notes*, Michigan State University. [Online]. Available: http://www.egr.msu.edu/classes/ece480/capstone/fall11/group02/web/Documents/How%20to%20Design%2010%20kHz%20filter-Vadim.pdf

[24] A. K. Maini, Ed., *Digital Electronics: Principles, Devices and Applications*. John Wiley Sons, Inc., 2007.

[25] Murata, "Basics of capacitors," http://www.murata.com/en-sg/products/emiconfun/capacitor/2011/09/14/en-20110914-p1.

[26] ——, "Grm155b11e102ka01," http://datasheet.octopart.com/GRM155B11E102KA01D-Murata-datasheet-14400354.pdf, 2008.

[27] ——, "Grm155r71h122ka01," http://psearch.en.murata.com/capacitor/product/GRM155R71H122KA01%23.pdf, 2013.

[28] ——, "Grm155r71h391ka01," http://psearch.en.murata.com/capacitor/product/GRM155R71H391KA01%23.pdf, 2013.

[29] ——, "Grm155r71h821ka01," http://psearch.en.murata.com/capacitor/product/GRM155R71H821KA01%23.pdf, 2013.

[30] "Simulating a non-ideal voltage source," http://eecs.oregonstate.edu/education/docs/tutorials/Simulating%20a%20non-ideal%20voltage%20source.pdf, Oregon State University.

[31] R. C. N. Pilawa-Podgurski, "Design and evaluation of a very high frequency dc/dc converter," Master's thesis, Massachusetts Institute of Technology, USA, 2007.

[32] R. C. N. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very high frequency resonant boost converters," *IEEE Transactions on Power Electronics*, pp. 1654–1665, June 2009.

[33] J. Prasad, "High frequency characterization of transistors."

[34] ROHM, "Us6m1." [Online]. Available: http://datasheet.octopart.com/US6M1TR-Rohm-datasheet-12557909.pdf

[35] ——, "Vt6m1," 2009. [Online]. Available: http://rohmfs.rohm.com/en/products/databook/datasheet/discrete/transistor/mosfet/vt6m1.pdf

[36] *Magnetic Core Characteristics Section 2*, Texas Instruments. [Online]. Available: http://www.ti.com/lit/ml/slup124/slup124.pdf

[37] "Soft switching in resonant converters," http://ecee.colorado.edu/~ecen5817/lectures/L5_ECEN5817_notes.pdf, University of Colorado Boulder.

[38] S. Verma, S. K. Singh, and A. Rao, "Overview of control techniques for dc-dc converters," *Research Journal of Engineering Sciences*, pp. 18–21, Aug. 2013.

[39] VISHAY, "Sib912dk," 2008. [Online]. Available: http://www.vishay.com/docs/68883/sib912dk.pdf

[40] ——, "Si1315dl," 2010. [Online]. Available: http://www.vishay.com/docs/67193/si1315dl.pdf

[41] ——, "Si1553cdl," 2014. [Online]. Available: http://www.vishay.com/docs/67693/si1553cdl.pdf

[42] WurthElectronic, "750312547 transformer," http://katalog.we-online.de/ctm/datasheet/750312547.pdf, 2012.

[43] P. Zuk and S. Havanur, *System Application Note AN847*, Vishay. [Online]. Available: http://www.vishay.com/docs/90936/an847.pdf