TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

ISMAILCAN ERSAHIN

HIGH-SPEED RESONANT DC/DC CONVERTER OF A SINGLE LITHIUM BATTERY CELL VOLTAGE

Master of Science thesis

Examiner: Prof. Nikolay T. Tchamov
and Prof. Teuvo Suntio
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ABSTRACT

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The objectives of power supplies have been to reduce the size,volume and cost whilst increasing efficiency, speed and reliability. These are considered to be the main challenges of the future power supplies.

The proposed discrete resonant self-oscillating DC/DC converter operable at high speed with high efficiency comprises cascoded power stage, automatic dead time circuitry and a transformer. Primary side of the transformer delivers power to the load and secondary side of the transformer provides inductive feedback to drive switching transistors. Driving stage composed of duty cycle detector and pulse shaping circuit. Since there is no external control, proposed topology offers fast response, adaptive dead-time and increased reliability in terms of EMI considerations. Switching losses caused by high frequency operation is reduced by ensuring ZVS operation which is performed by optimizing dead-time driving signals. Efficiency of the converter is further enhanced by adding automatic dead-time latch circuitry by 1.3%. SPICE simulations of the proposed converter is conducted by employing real SPICE models of the components and the likelihood of parasitic components that can emerge with high frequency in PCB is taken into account and they are modeled thoroughly based on practical requirements. Hence, PCB implementation is applicable. As the converter designed for discrete implementation, it makes proposed topology to be cost effective since most of the high speed converter are designed for silicon process.

Proposed discrete resonant self oscillating DC/DC converter operates at 3.4 MHz with 72.3% efficiency and drives 10Ω resistive load. Supply voltage is 4 V and generated average output voltage is 2.34 V± 30mW with 58.5% duty ratio.

PREFACE

This thesis has been conducted at RFIC Laboratory, Departments of Electronics and Communications Engineering of Tampere University of Technology.

I would like to thank to my supervisors Prof. Nikolay T. Tchamov and Prof. Teuvo Suntio for providing me this thesis subject and opportunity to be a part of RFIC Research Team. In a same manner, I also would like to thank Jani Järvenhaara for sharing his deep knowledge and his assistance and my colleague Stanislav Babaev for his friendship and his valuable helps during the thesis work as well.

When I first came here in Finland 2 years ago, I was quite far from Finnish culture and lifestyle until I met with Saara Repo. She unconditionally helped me to adapt to Finland and brought different perspectives to my life. I would like to express my deepest gratitude to her as she all the time supported and believed in me.

I am very elated that I got the opportunity to know my beloved friends Anil Sirri Baslamisli, Begum Gokce Sagmaner and Cumhur Kusdemir 7 years ago in Cyprus. You became my family and offered me your precious love and the best friendship. We have grown up and managed to overcome any challenges we came across on the way altogether. That is what makes us a family with full of valuable memories that will never fade away. After all, I want to appreciate your endless support, love and friendship.

Finally, I would want to thank my family. You are the reason that I managed to motivate myself and come to this far. You always inspired me and took the trouble to help me unconditionally. For that reason, I would like to dedicate my thesis to you.

Tampere, 13.04.2016

Ismailcan Ersahin

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LIST OF ABBREVIATIONS AND SYMBOLS

DC/DC	Direct Current to Direct Current
MOSFET	Metal Oxide Silicon Field Effect Transistor
CMOS	Complementary Metal Oxide Silicon
NMOS	Negative Channel Metal Oxide Silicon
PMOS	Positive Channel Metal Oxide Silicon
PCB	Printed Circuit Board
ZVS	Zero Voltage Switching
DTHL	Dead Time High to Low
DTLH	Dead Time Low to High
D	Duty Ratio
D'	Complementary Duty Ratio
PWM	Pulse Width Modulation
EMI	Electro Magnetic Interference
ESR	Equivalent Series Resistance

1. INTRODUCTION

Recently, the objective of power electronics circuits has been to diminish the size of storage elements, weight and energy cost while increasing the efficiency and reliability. The trend of miniaturizing is additionally pushed by the energy awareness which result in need of high efficient power supplies. The size of storage elements usually dominates over other parts like switching devices and control circuits which constraint power density of the converter. Similarly, achievable transient performance of the converter heavily depend on energy stored in the passive elements such as capacitors and inductors. This is due to the fact that as the component values and energy stored decrease, operating frequency of the switched mode power supplies tends to increase proportionally. Therefore, there is a motivation to operate switching mode power supplies at high frequencies if the practical constraints like efficiency can be addressed [23]. That is to say, high switching frequencies enable to achieve high efficient switched mode power supplies, however, the rate of high frequency is limited because with high frequencies average power dissipation of the semiconductor devices increase. Hence, highly efficient and fast switching semiconductors are needed. Nonetheless, parasitic inductances, capacitances and resistances of printed circuit boards and packages become even more visible at higher frequencies and this also affects the dynamic behavior of fast switching transistors beside their effect to the efficiency. Therefore, realizing the requirements for electromagnetic compatibility and robustness becomes difficult with use of high efficient semiconductors[9]. Moreover, as the frequency increases intrinsic capacitances of MOSFET come into play and effective impedance started to be seen causing dynamic losses in the converter. Among the switching power supplies, the resonant self-oscillating DC/DC buck converters are considered to be a good choice in order to achieve the objectives mentioned above [11]. In parallel with that, through implementing Zero-Voltage-Switching (ZVS) technique, it is also possible to mitigate the switching losses. ZVS technique requires adjustment of dead-time between driving signals for appropriate switching instant which helps to prevent losses due to short circuit paths.

Battery-powered devices has been utilized widely by means of recent developments in electronic industry. A battery powered DC/DC power converter system is illustrated in Figure 1.1 However, batteries, like Li-ion, supplies variable output voltage, while many electronic devices operates at fixed power supply. Direct utilization of batteries as an input can cause instabilities in performance of the connected device. Thus, there is vulnerable need to employ a converter between the battery and input of the device which is capable of converting variable output voltage to fixed input voltage.

DC/DC buck converter has good output voltage regulation characteristics and high efficiency. It is the main component of the power management units and supplies smooth and constant output voltage. Nevertheless, maximum battery voltage that can be applied to the converter is limited owing to MOSFET gate-oxide breakdown voltage constraint in standard CMOS process. In order to achieve high voltage conversion ratio, cascaded transistor structure can be applicable. Cascaded structure allows converter to operate at input voltage higher than maximum transistor allowed gate-oxide breakdown voltage[2]. Operating the converter at high speed introduces numerous challenges that paves the way to traditional converter topologies become impractical. Traditional switched mode converters usually with external gate drive control operates at 100 kHz-1MHz range [3]. This thesis proposes new high-speed discreet resonant self-oscillating converter topology with no external gate drive control and demonstrates its feasibility at 3.4MHz with 72.3 % efficiency rate.

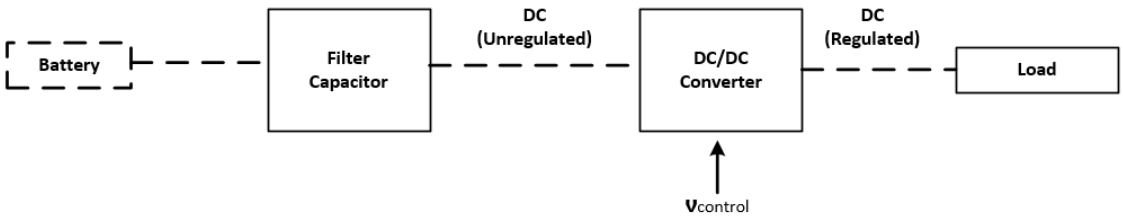

Figure 1.1 *A DC/DC Converter System*

2. THEORETICAL BACKGROUND

This chapter provides the basic knowledge for DC/DC converter concept that will be used throughout the thesis.

Direct-Current-to-Direct-Current (DC/DC) converters are widely used in regulated switched mode supplies and virtually become a part of every electronic circuits. Such converters need to supply adequate regulated output voltage or current to the specific applications. The power source that delivers the electrical energy to DC/DC converter can be a rechargeable battery such as Li-ion batteries. Many portable electronic devices has been powered by rechargeable batteries which have low self-discharging, small memory effect and high energy density. Such batteries nominally provides voltage in the range of 3.6-3.8V. However, the different circuits in electronics devices which utilize single battery often demand various range of supply voltages. See Figure 2.1. Thereby, DC/DC converters must be placed in the device so that they will convert one single battery voltage to different level input voltages. DC/DC converters are designed depending on the requirements with respect to varied output power, voltage conversion ratio, power conversion efficiency, power density, and size [16].

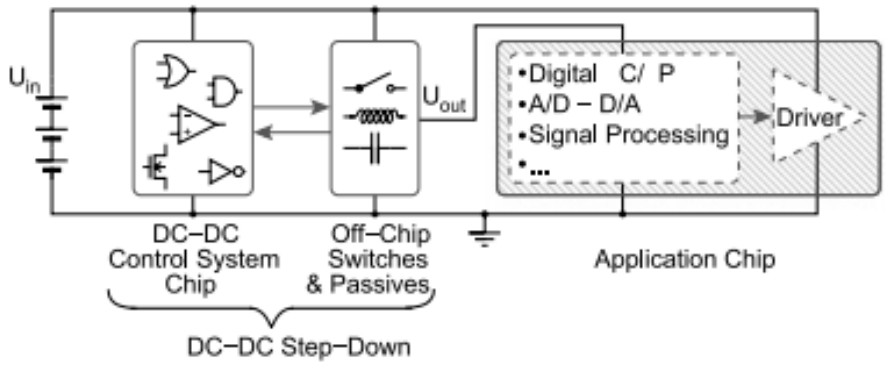

Figure 2.1 *The block diagram of battery-powered application utilizing DC/DC Buck (step-down) converter.*

DC/DC converters can be examined under two different topologies which are linear dc power supplies and switching mode dc power supplies. Traditionally, linear dc power supplies has been utilized. However, advances in the semiconductor technology paved the way to design switching dc power supplies which are more efficient and smaller size compared to linear dc power supplies. In this thesis, switching mode DC/DC Buck converters will be mainly analyzed in terms of background information. Through, the basics of buck converter, resonant self-oscillating converters will be discussed in order to grasp thoroughly the concept of resonant self-oscillating DC/DC converters which are the primary concern of this thesis. In order to appreciate and comprehend the advantages of switched mode dc power supplies, it is essential to first revise the linear dc power supplies.

2.1 Linear DC Power Supplies

Linear dc power supplies are considered to be the most basic converters. Through a resistor divider, input power simply delivered to the output stage in the expense of large power dissipation over the resistor. In that case, in terms of efficiency such supplies poorly converts the voltage level. In parallel with that, their ability of power conversion is limited due to nature of these supplies. In general, conversion ratio of linear dc power supplies changes only between zero and one[16]

One the positive side, linear dc power supplies are quite easy to build and implement and as well as cost less for small power ratings (<25W)[15]. Besides, EMI considerations is less in this type of supplies and circuit does not comprise large inductance and capacitance which dominate the space. In contrast, power conversion efficiency is quite poor usually in the range of 30-60 % [15]. Therefore, switched mode dc power supplies are developed with much higher efficiency rates. Power stage of a linear dc power supply is shown in Figure 2.2

2.2 Switched Mode DC Power Supplies

Switched mode DC power supply can be defined as a converter which transfers power from a source to a load efficiently while changing voltage and current characteristics of the source. This conversion is achieved by incorporating a switch (usually MOSFET transistor) in the circuitry. As opposed to Linear DC power supplies, transistor in the switched mode dc power supplies operate in switched mode instead of linear

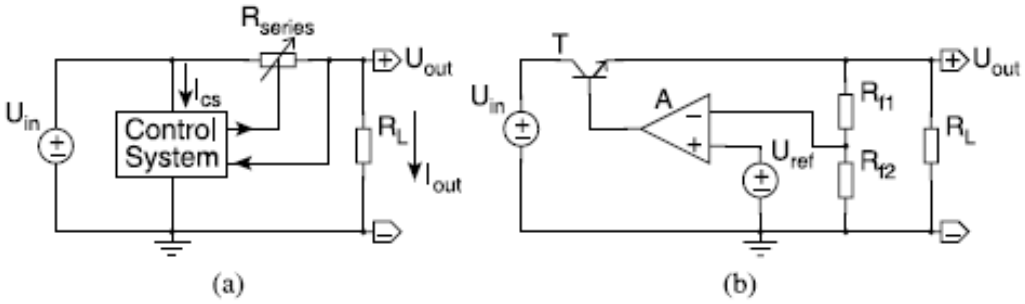

Figure 2.2 *(a) Basic linear dc power supply. (b) Simple implementation with feedback circuitry which adjust the voltage at the gate of the transistor so that transistor behaves like variable resistor.*

(active mode). In switched mode, switch is either completely on or off [15]. During the on state current conducts and voltage drop over the transistor is small while during the off state transistor blocks the voltage and no current flows through the transistor which means that transistor is acting like an ideal switch causing power loss in the converter to reduce significantly. Hence, much higher efficiency, smaller size, low power dissipation, relatively low cost, high voltage and current ratings and higher voltage conversion ratio are the main factors from which the switched mode dc converters emerged. In linear dc-dc converters, as explained above, voltage regulation is achieved continuously dissipating power in the transistor which behaves as a varying resistor. That is, output voltage is regulated based on ohmic losses. On the contrary, voltage regulation is performed by changing the ratio between on and off time of the switch. To illustrate this conversion concept, a basic DC/DC converter is depicted in Figure 2.3 . The average value of output voltage depends on durations of on and off times in Figure 2.4

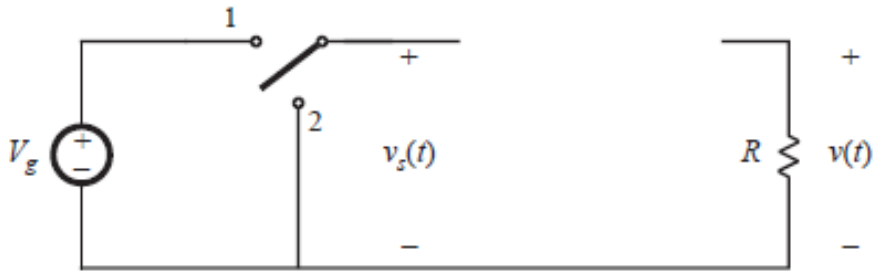

Figure 2.3 *Basic Switched mode DC/DC Converter*

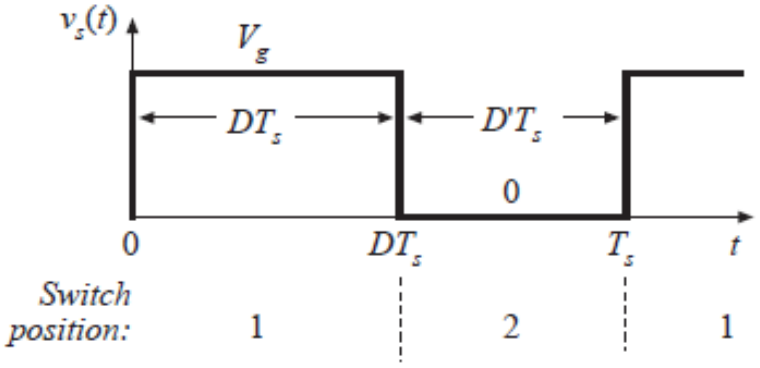

Figure 2.4 *Average Output Voltage Waveform*

By simply adjusting the durations of on and off times, average value of Vo is subject to vary. This method is called pulse with modulation switching (PWM). In addition to this, the on-time duration of the whole switching time is defined as duty ratio (D) that changes between zero and one [15]. Complementary duty ratio (D') indicates off time duration in a switching period (Ts). Average value of the output can be expressed as follows[15]:

$$Vo = \frac{D \times \mathrm{Ts}}{Ts} \times \mathrm{Vg} \tag{2.1}$$

Switched Mode DC/DC converters can basically be examined through two different topologies. As mentioned, switched mode DC/DC converters are utilized in order to convert unregulated output voltage to controlled and desired voltage level. If the regulated output voltage is less then the input voltage this type of converter is called *Buck Converter* and if the output voltage level is higher than the input voltage level then the converter is called *Boost Converter*.

In this thesis, discussion will be mainly maintained through buck (step-down) converter basics, since the proposed topology resembles buck type of converter.

2.2.1 Buck (Step Down) Converter

As its name suggests, buck converter simply steps down its dc input voltage level to a lower average dc output voltage value[15]. It is one of the most basic type converter in the class of switched mode dc to dc converters. Due to their high efficiency and

good output regulation characteristics it is vastly used in many portable electronics applications. In Figure 2.5, power stage of a buck converter is illustrated. Buck converter comprises two switches, output filtering elements(LC low pass filter) and a load. Load can be either resistive or a current source. However, it is assumed that load is resistive in this case. It is further assumed that input voltage is constant, switches are ideal. Based on these conditions instantaneous output voltage waveform Vx is depicted in Figure 2.6

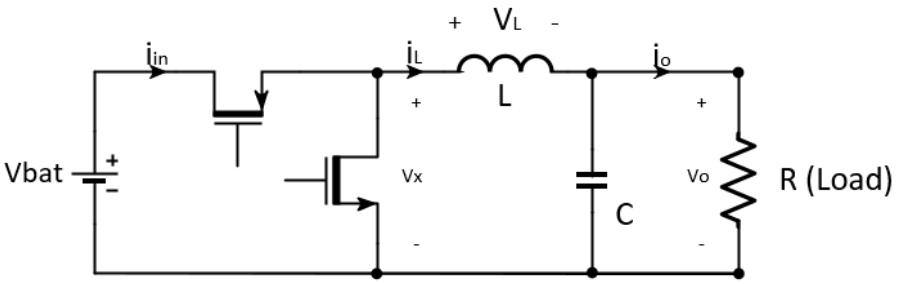

Figure 2.5 *Buck Converter Power Stage*

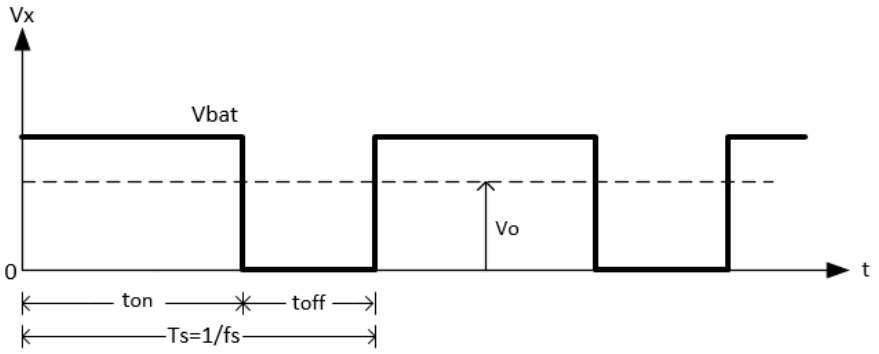

Figure 2.6 *Instantaneous Output Voltage Waveform*

Instantaneous output voltage Vx is a function of switch position. Meaning that, dc component of the output voltage is determined by the switch[8] According to the waveform presented in Figure 2.6average output voltage can be computed with respect to duty ratio (D) over one switching period as follows:

$$Vo = \frac{1}{Ts}\int_{0}^{Ts} vo(t)\,\mathrm{d}t = \frac{1}{Ts}\left(\int_{0}^{ton} Vbat\,\mathrm{d}t + \int_{ton}^{Ts} 0\,\mathrm{d}t\right) = \frac{ton}{Ts}\mathrm{Vbat} = D\mathrm{Vbat} \qquad (2.2)$$

Operation principle of the buck converter can be explained better with respect to inductor voltage and current. When the main switch is on and complementary switch is off (on-state), dc source delivers energy to the inductor and to the output. During the off state, when main switch is off but complementary switch is on, energy stored in the inductor in the form of magnetic field is transferred to the load via inductor current that flows through the complementary switch. In the on state, voltage over inductor is *Vbat-Vo* and inductor current increases, on the other hand, during the off state inductor voltage equals to *-Vo* and current decreases. This behavior repeats in every switching cycle in steady-state operation and it is demonstrated in Figure 2.7 .

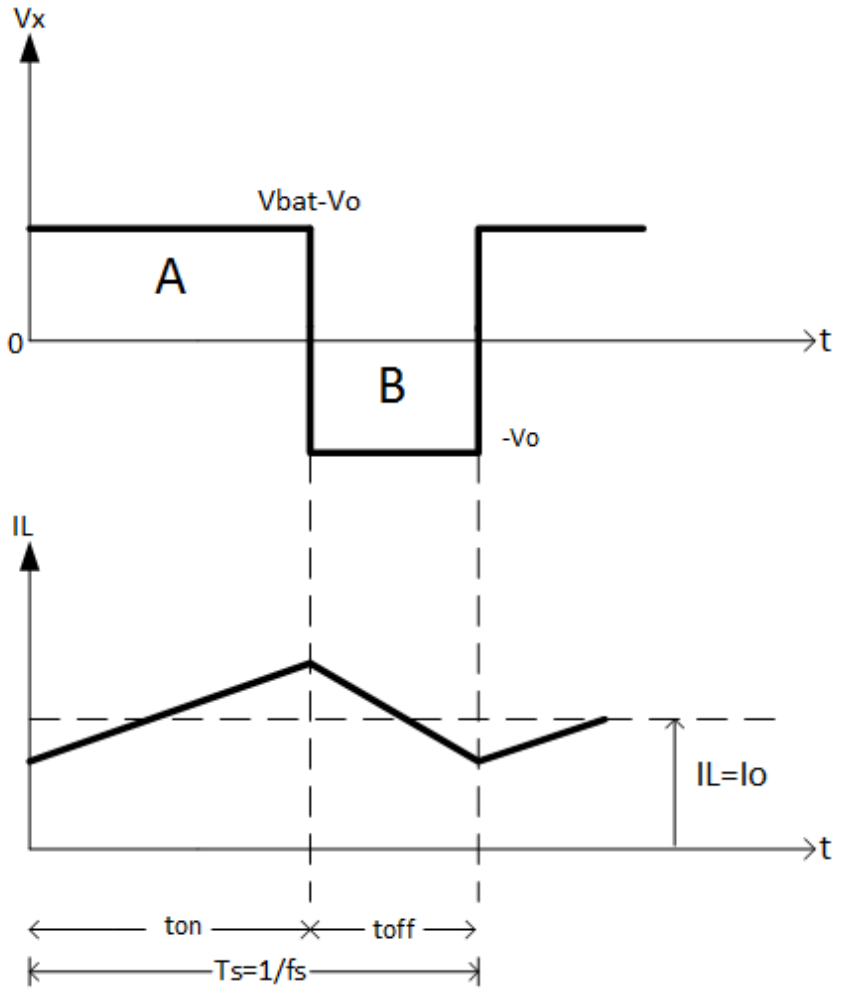

Figure 2.7 *Inducutor Voltage and Current During Switching States*

Furthermore, it can be recalled that in steady-state fundamentally inductor voltage over one period is zero. Based on this, output and the input voltage relationship can be expressed by the following Equation where *Ts=ton+toff* and VL is the inductor voltage.

$$\int_0^{Ts} VL\,\mathrm{d}t = \int_0^{ton} VL\,\mathrm{d}t + \int_{ton}^{Ts} VL\,\mathrm{d}t = 0 \tag{2.3}$$

Aforementioned Equation further implies that

$$(Vbat - Vo)ton = Vo(Ts - ton) \tag{2.4}$$

and equation 2.4 simplifies to

$$\frac{Vo}{Vbat} = \frac{ton}{Ts} = D\ (Duty\ Ratio) \tag{2.5}$$

It is clear that average output voltage value depends on the duty ratio regardless of the other circuit parameters. Moreover,the gates of the MOSFET switches are driven with the pulse signals according to desired duty ratio. Control of the gate drives are usually achieved by PWM (Pulse Width Modulation) technique as mentioned in *section 2.2*. Appropriate PWM control signals are generated based on the feedback circuitry. See Figure 2.5

In Figure 2.6, it can be seen that output voltage (before filtering stage) swings between zero and Vbat which is a drawback of the buck converter and not acceptable for many practical works. However, this can be resolve by employing low pass filter consisting of an inductor and capacitor at the output stage. In order to reduce the ripple in the output voltage, very large capacitor is selected. Thus, instantaneous output voltage approaches to be almost constant which is desired by many applications.The formulas for the calculation of output voltage ripple ΔVo and inductor current ripple ΔIL are provided below. Additionally, corner frequency of the filter must be less then the switching frequency of the converter. In that way, it is also possible to eliminate switching ripples that might be seen at the output[15]. What is more, series resistance of the filter capacitance should be less than the load resistance [2]in order to make sure that AC component of the inductor current flows

through capacitor and DC component flows through the load.

$$\Delta IL = \frac{Vo}{L}(1 - D)Ts \tag{2.6}$$

$$\Delta Vo = \frac{1}{C}\frac{1}{2}\frac{\Delta IL}{2}\frac{Ts}{2} \tag{2.7}$$

Another down side of the buck converter is that even the load is resistive, there is always stray inductance shows up at the output and inductive energy formed by that stray inductance needs to be dissipated in the circuit otherwise MOSFET which is used as a switch will be destroyed. To cope with this issue, a second switch (NMOS) is introduced as a complementary switch to the main switch (PMOS) that will absorb the inductive energy.
Theoretical analysis of the buck converter is simplified here by neglecting parasitic elements that exist in the inductor, capacitor and switches. Such parasitics cause losses in the converter. Effects of the parasitics will be discussed in the following chapter. However, it should be noted that for low frequency applications like in the vicinity of several hundred kilohertz despite the parasitics, it is possible to achieve very high efficiency approaching to 100 % .Yet, efficiency issue emerges when the operation frequency goes high.[8]

2.2.2 High Speed Buck Converter Efficiency

Ideally, it is assumed that switches have no parasitic components. However, in practice transistor switches are modeled as resistors which indicates that there are static losses exist in the MOSFET switches. It is further claimed that CMOS inverters where NMOS and PMOS operate in a complementary manner, have no static losses. But in fact, when there is no dead time introduced between switching times of the complementary switches, short circuit losses tend to occur. That is to say, a path from supply voltage to ground will be formed at an instance when both switches are not synchronized properly.

The efficiency characteristic of the buck converter,however,changes dramatically when the switching frequency is increased [12]. Consequently, beside the static losses, dynamic losses come into play. Meaning that, parasitic capacitances of the

MOSFET transistor Cgs, Cgd and Cdb causes dynamic losses. This loss can be expressed with the following formula:

$$Pdyn = C \times Vbat^2 \times fsw \tag{2.8}$$

where C is the capacitance, Vbat is the supply voltage and f is the switching frequency. It is obvious that dynamic losses increase dramatically when the high frequency operation is performed. Hence, efficiency of the converter will decrease substantially. The dynamic power is dissipated in each course of cycle by charging or discharging of the parasitic capacitors such as Cox,Cgd,Cgs,Cdb capacitances of the MOSFETs.

The total power loss of a buck converter is a combination of conduction losses which emerge from the resistive parasitic impedances and dynamic switching losses caused by capacitive parasitic impedances. In Figure 2.8,parasitic model of the buck converter circuit is demonstrated.

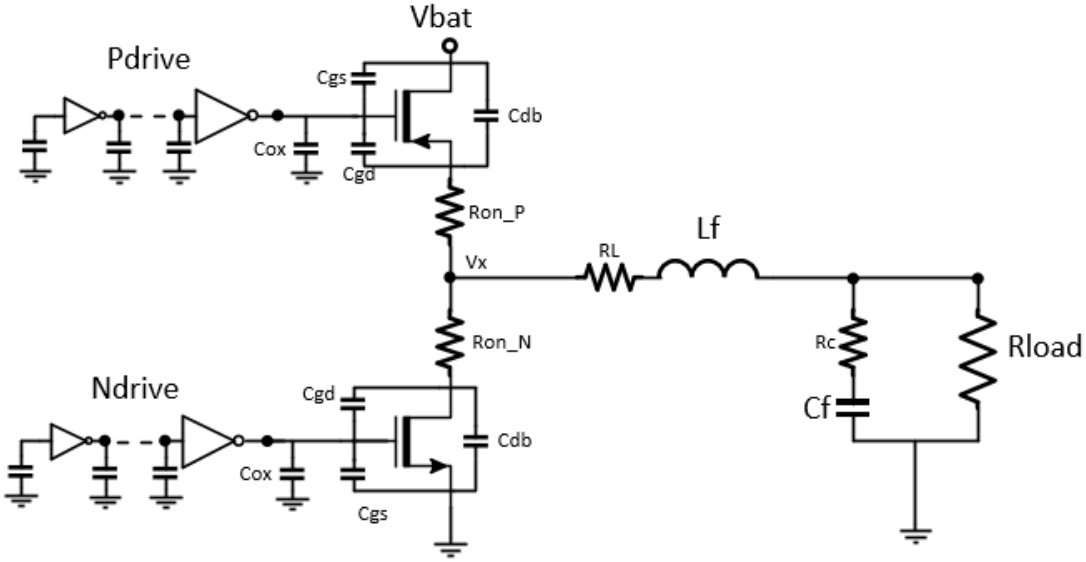

Figure 2.8 *Buck Converter Parasitic Circuit Model*

Apart from the MOSFET related losses, filter inductor and capacitor are of great concern. Some part of the total power dissipation is led by the series resistance and stray inductance and capacitance of the filtering elements. Filter inductor power loss is formulated by the following expressions[12]:

$$Ptotal, inductor = b \times (\frac{Io^2}{\Delta i fs} + \frac{\Delta i}{3fs} + \frac{CLVbat^2}{RL\Delta i}) \tag{2.9}$$

$$b = \frac{(Vbat - Vo) \times D \times RL}{2} \tag{2.10}$$

where CL is the stray capacitance and RL is the series resistance of the filtering inductor. Additionally, Δi is the inductor ripple current and Io is the output current. Similarly, filtering capacitor suffers from the series resistance sticked to the actual capacitance. This causes static losses at the filtering stage. If the filtering capacitance is implemented gate oxide capacitance of a MOSFET then this power loss can be dictated with the following formula [12].

$$Ptotal, inductor = d \times fs \times \Delta i \tag{2.11}$$

$$d = \frac{8 \times Rcap \times Lcap \times Co \times \Delta Vo}{3} \tag{2.12}$$

where Rcap is the series resistance of the MOSFET with $1um$ width, Co is the gate oxide capacitance per um^2 and Lcap is the channel length of the MOSFET.

Lastly, it is crucial to mention short circuit losses in the converter once again which is caused by the instantaneous path formed between Vbat and the ground. This path is formed owing to the incorrect adjustment between the gate pulse signal. This type of loss is depicted in below Figure 2.9

Whenever PMOS transistor is ON complementary NMOS transistor must be OFF or vice versa in order to avoid short circuit losses. However, as can be seen in the Figure,, there is some small time interval when PMOS is ON and NMOS is still ON as well. To be able to prevent such loss, dead time ought to be introduced between the driving signals.

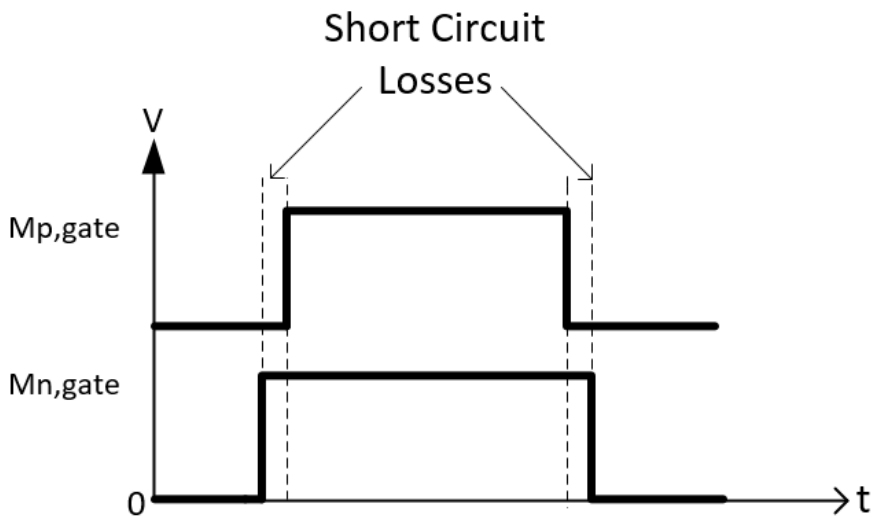

Figure 2.9 *Short Circuit Losses*

Finally, efficiency of a buck converter is given as follows[12]:

$$\eta = \frac{Pload}{Pload + Pbuck} \times 100 \tag{2.13}$$

where the Pload is the average power that the load dissipate and Pbuck is the total power consumed internally.

2.3 Passive Component Behavior at High Frequency

Usually passive components like inductors and capacitor are presented in an ideal sense in the circuit analysis. They are treated as purely inductive or capacitive component and often effects of wires, leads and connectors are omitted. However, in practice, it happens so that every passive components in fact exhibits capacitive and inductive behaviors beside its own characteristics even above any frequency larger than zero. As it is the case, performance of the circuit designed might deviates from what is expected in ideal sense. Impedance, capacitance or inductance values of the passive elements might greatly change due to non-ideal behavior especially at high frequencies. In this section, parasitic models of the capacitor and inductor are examined in order to comprehend the sources of non-ideal behaviors of the circuit passive elements in practice.

2.4 High Frequency Behavior of Capacitor

In capacitors, wires leads are connected to each parallel plates having an area A and separated from each other via dielectric material. At high frequencies, except from the ideal bulk capacitance, other parasitic resistances or inductances or capacitances might become relevant. In Figure 2.10 adapted from[19], parasitics model of a capacitor that is soldered on PCB is demonstrated. In this model, the inductor Ls is emerged due to the leads of the capacitor itself and dominates the inductance most of the time. Due to finite conductivity of the plates and lead cause resistive losses in the capacitor. This resistance is also known as ESR (effective series resistance) and modeled as Rs. In addition to this, large resistance caused by the dielectric material between the plates is also added as shunt resistance to the bulk capacitance in the parasitic model. Furthermore, shunt capacitances Cp in the model represents the capacitance occurred due to solder path to ground plane in PCB.

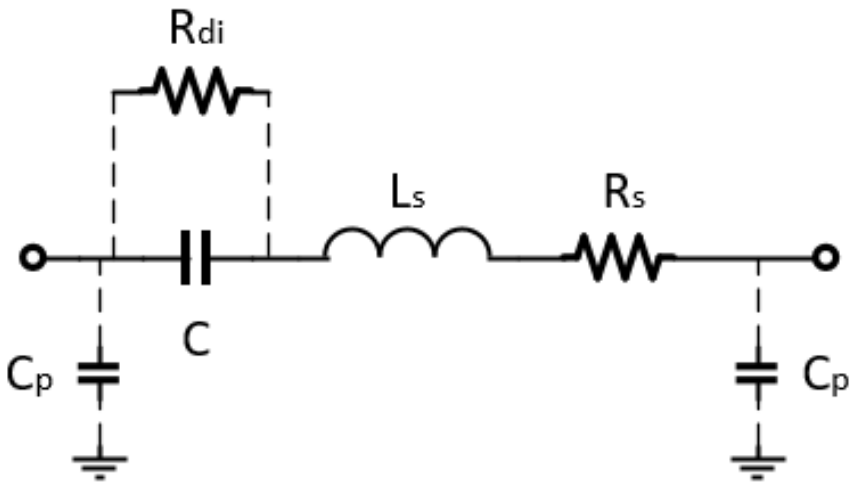

Figure 2.10 *The lumped parasitic model of the real soldered capacitor*

In Figure 2.11 adapted from [19], high frequency impedance characteristic of a capacitor is showed. In addition to its ideal behavior, at a certain frequency (in this case at 1 GHz), self-resonant occurs. It means that after this point, capacitor no longer behaves as am ideal capacitor. This is inevitable because as AC current flows through a capacitor, a magnetic field is generated by the capacitor itself and paves way to an inductance in the structure[19].

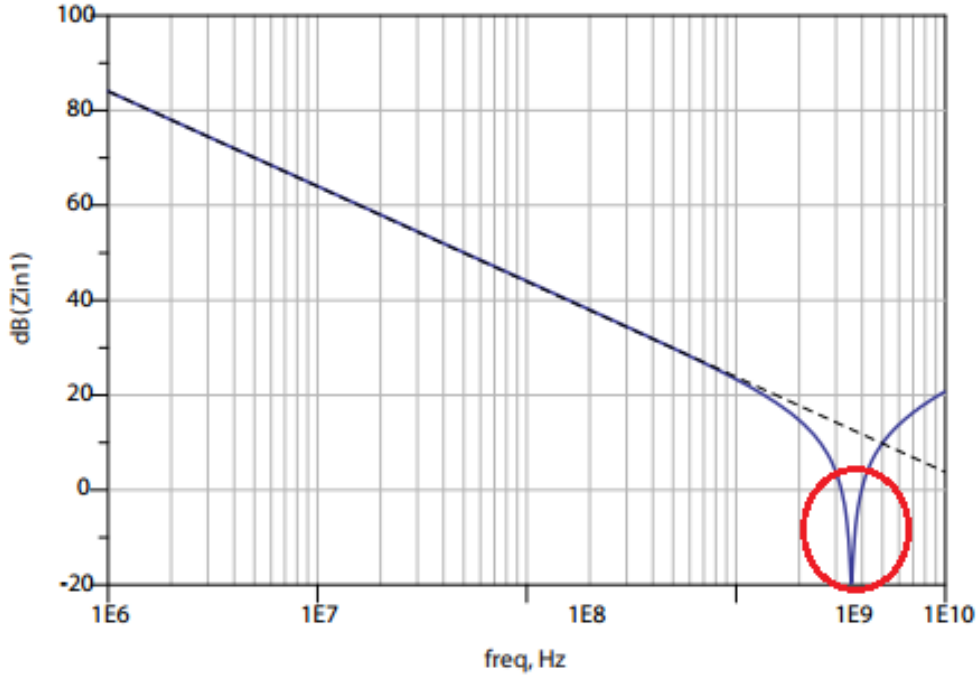

Figure 2.11 *Impedance of a capacitor in magnitude (dashed line represents the ideal behavior)[19]*

The demonstrated parasitic model for the capacitor can be further simplified as shown in Figure 2.12. Based on circuit theory capacitor is reactive and its impedance is expressed by:

$$Xc = \frac{1}{2\pi fC} \tag{2.14}$$

The impedance of the capacitor is tend to decrease as the frequency increase by given formula ideally. However, if the simplified parasitic circuit is investigated equivalent impedance of overall capacitor model can be written as follows:

$$Zeq = \frac{1}{jwC} + jwL + Rplates = Rplates + j(\frac{-1}{wC} + wL) \tag{2.15}$$

Thus, it is clear that mathematically impedance of the overall capacitor model will change as the frequency changes when compared to ideal case. It is crucial to note

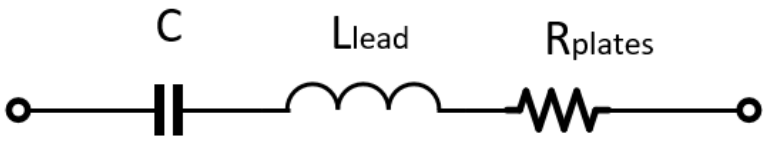

Figure 2.12 *Simplified Parasitic Model of a Capacitor*

that as the frequency increases, equivalent impedance that is dominated by the capacitance decreases linearly until the point where it reaches its minimum. See Equation 2.15. This point called as $self - resonance$ and at this point impedance is pure real and this point can be given as :

$$jwL = \frac{1}{jwC} \tag{2.16}$$

The frequency at which self resonance occurs is given by:

$$fsr = \frac{1}{2 \times \pi\sqrt{L \times C}} \tag{2.17}$$

It should be remarked that as the frequency further increases beyond the self resonance, impedance starts to increase and to be dominated by the inductive term. What is more, as the frequency even increases to infinity then lead inductor will behave like an open circuit. Hence, maximum operation frequency of the capacitor is limited by the lead inductance. A table that shows the various capacitors and their operable frequency range is given below.[13]

Table 2.1 *Various Capacitor Types and Operable Freqencies*

Capacitor Type	**Approximate Operation Frequency**
Tantalum electroytic	1-1000 Hz
Large value aliminum electrolytic	1-1000 Hz
Ceramic	10 kHz-1 GHz
Mica	10 kHz-1 GHz

2.5 High Frequency Behavior of Inductor

Similarly, inductors are also non-ideal passive elements like capacitors as their behavior changes as the the frequency changes and it is possible to model it with its

parasitic components. Inductor is made of coil of insulated wire. Meaning that, between the windings there are parasitic capacitances exist. These tiny parasitic capacitances emerge whenever individual winding is placed close to one another.(as they are insulated and there is a small potential differences exist between the wires due to resistance and inductance). Therefore, it would be wise to reduce the distance between the windings so that the parasitic capacitances will decrease. This type of parasitic capacitance is modeled as parallel to bulk inductance. Additionally, the wire resistance is modeled as series to the bulk inductance. In PCB, solder path to ground plane forms an additional parasitic capacitance which is also depicted in the model. The parasitic model of an real soldered inductor is resented in Figure 2.13

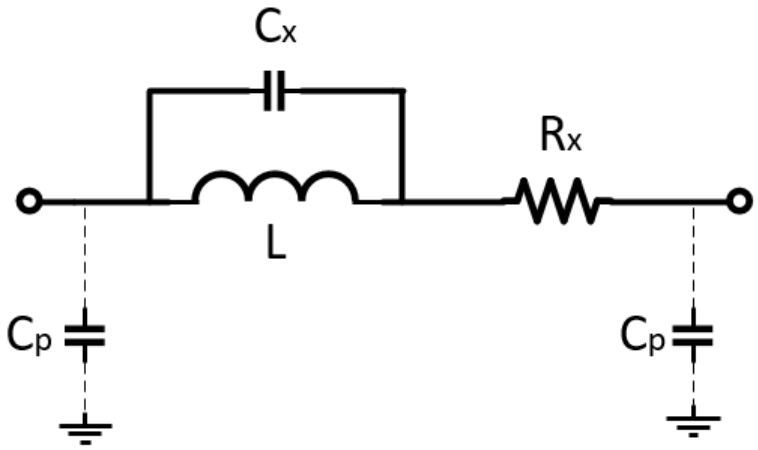

Figure 2.13 *Lumped parasitic model of real soldered inductor*

Equivalent impedance of the parasitic model can be expressed by omitting Cp as:

$$\frac{1}{Ztotal} = \frac{1}{Z1} + \frac{1}{Z2} \tag{2.18}$$

where

$$\frac{1}{Z1} = \frac{1}{jwCx} \tag{2.19}$$

and

$$\frac{1}{Z2} = jwL + Rx \tag{2.20}$$

then finally,

$$Ztotal = \frac{jwL + Rx}{w^2LCx + jwCxRx} \tag{2.21}$$

The high frequency behavior of the impedance of the inductor parasitic model can be analyzed over the different frequency ranges by examining 2.21[13]. Such as,

At very low frequencies it is obvious that total impedance is dominated by series wire resistance Rx.

As frequency start increasing, inductor begins to dominate the impedance near the frequency :

$$w = Rx/L \tag{2.22}$$

As frequency increases further, impedance of the capacitance decreases until its value equals to impedance of the inductor. This point called $self - resonance$ and occurs at :

$$fsr = \frac{1}{2 \times \pi\sqrt{L \times Cx}} \tag{2.23}$$

Total impedance is maximum at this point and beyond the self resonance parasitic capacitor dominates the impedance and total impedance start to diminish. Hence, inductor no longer behaves as an inductor as it is expected to behave in ideal world. In Figure 2.14 adapted from [13],this examined behavior can be seen clearly.

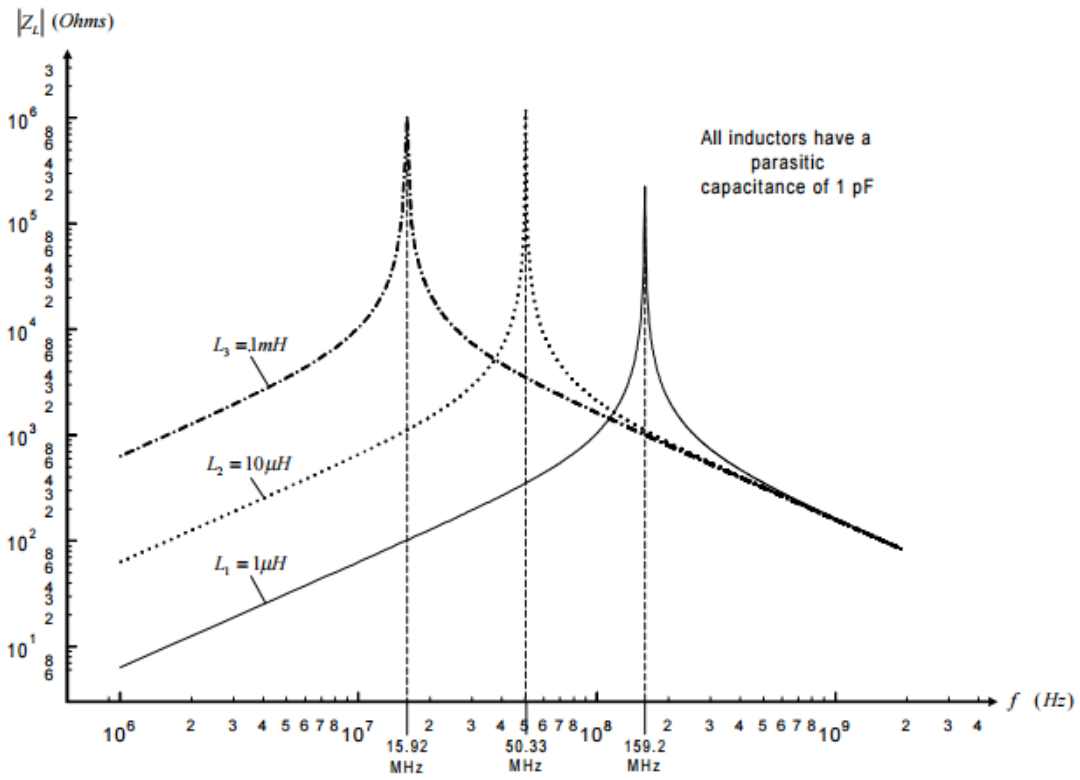

Figure 2.14 *Frequency dependent impedance behavior of various inductors[13]*

3. METHODOLOGY

This chapter discusses the design procedure of proposed converter.

3.1 Resonant Self-Oscillating DC/DC Converter

Resonant Self-oscillating converter is defined in[11] as follows: Self-oscillating converter is a resonant converter in which commutation control signal is attained from inductive feedback of its resonant load. Its fundamental operating principle is same with the traditional DC/DC Buck converter. Nonetheless, high frequency operation beside high efficiency require some modifications in the convenient topology.
There are many advantages of self oscillating converters, such as high power density, reliability and low cost. In addition to these, as noted in[7] the most prominent feature of the self oscillating control is that it compensates the tolerances in the components so that the converter will be driven much closer to resonant frequency while maintaining the zero voltage switching (ZVS). Likewise, in this type of topology, one of the main characteristics of the circuit is that switching frequency is independent from the load. Furthermore, converter is capable of operating at high frequency without any external control which might need FPGAs and micro controllers. Since there is no external driver circuit, reliability of the circuit increases whilst system cost decreases.
In Figure 3.1, block diagram of proposed resonant self-oscillating converter is depicted. The power stage of the converter comprises cascoded transistors, transformer, duty cycle detector and pulse shaping circuit. Instead of traditional filtering coil, a transformer is placed. While primary side of the transformer delivers power to the load, secondary side provides positive feedback to the duty cycle detector. Then, through the pulse shaping circuit gates of PMOS and NMOS transistors are driven. Pulse shaping circuit is needed as the feedback signal waveform obtained from the secondary of the transformer is sinusoidal. Besides, creation of automatic dead-time which enables the converter to achieve ZVS operation is also performed by means of pulse shaping circuit.

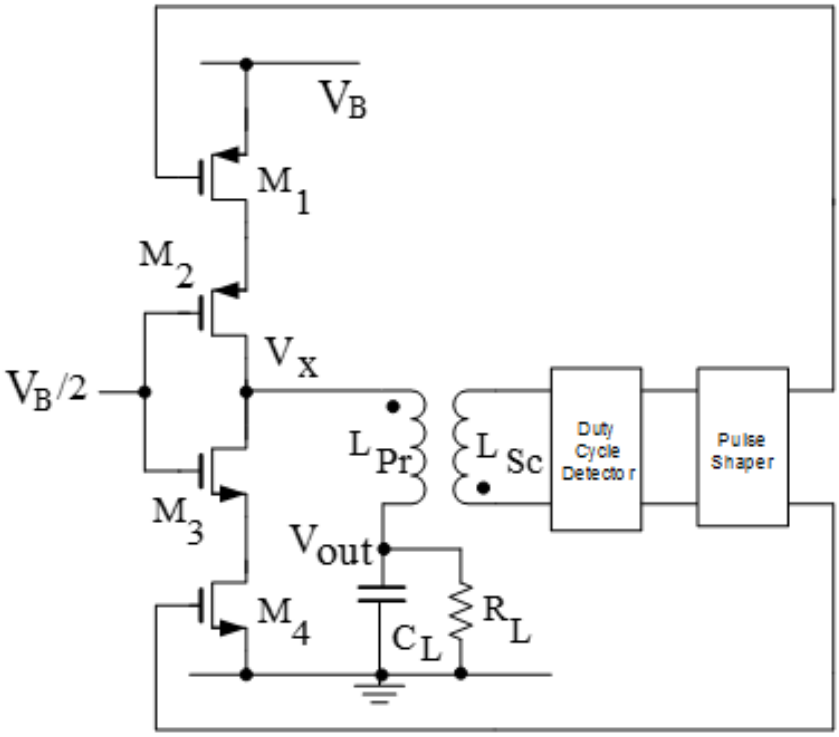

Figure 3.1 *Resonant Self-Oscillating DC/DC Converter Block Diagram*

3.1.1 Operation Principle

The operation principle of the proposed converter can be explained by examining the Figure 3.2. In the Figure, there are NMOS and PMOS complementary switches which are driven by the self oscillating manner which indeed makes the difference from the traditional methods. Transistors M2 and M3 are employed as cascoded transistors so that the converter can operate high supply voltages since the maximum voltage that can apply to the low voltage transistors are constrained in CMOS technology. Moreover, primary side inductor Lpr, three parallel capacitors CL and Lf are the filtering elements. On top of that, CL and the primary side inductor resembles the resonant load and resonates near the operating frequency which means that operation frequency of the resonant self oscillating converter is mainly determined by the transformer primary side inductor and load capacitor CL. Secondary side of the transformer is in the role of inductive feedback provider. Capacitive divider consists of two large high frequency compatible Cr capacitors are the AC

ground [2] or voltage reference in the duty cycle detector circuit. Transistors M5 and M6 are the active divider in the form of diodes in the same circuitry. CMOS buffers in both high and low side are responsible for the shaping the sinusoidal gate signal with inherent regenerative characteristics of the multi stage CMOS inverters. On top of that both driver causes time delay of the driving signal. For instance, between the time voltage at the Vx node increases and M1 PMOS transistor switched on is delayed so that the switching losses are reduced. Feedback signal for the low side NMOS M4 is delivered through a level shifter because the swing voltage for the low side buffer is between ground and Vbat/2. M14 and M15 are the utilized for the local feedback for the high side driver. This local feedback forces the high side driver as a Schmitt Trigger.

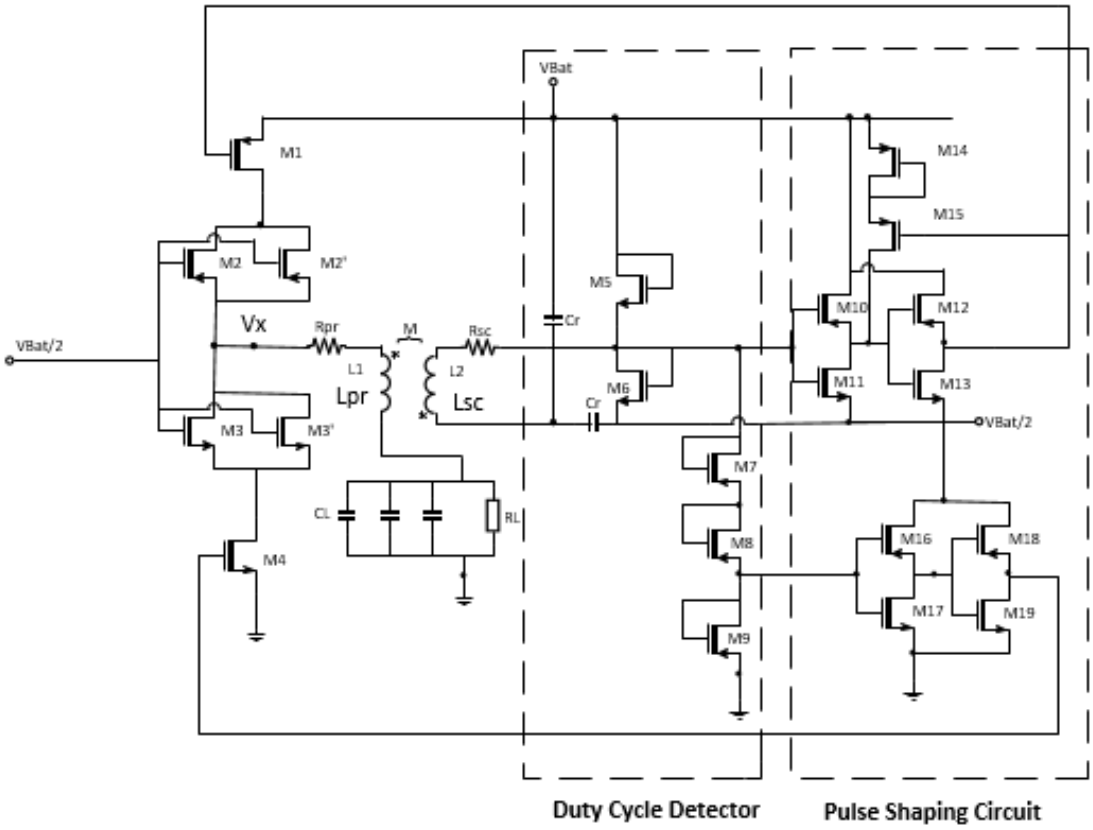

Figure 3.2 *Resonant Self-Oscillating DC/DC Converter Power Stage*

As mentioned earlier, operating principle is quite similar to buck converter. As the

name implies, self oscillating converter starts to oscillate on its own. Initially, say time $t1$, Vx node is zero. This zero voltage is transferred to the input of the PMOS driver side via transformer and through the driver, M1 is switched ON. Therefore, Vx node starts to charge to Vbat level since M1 passes VBat to Vx node with a time delay. At the time $t2$, VBat voltage at the Vx node is delivered to low side NMOS driver by means of the transformer and M4 NMOS transistor is forced to switched ON while M1 is switched OFF already. Then Vx node is pulled down to ground through M4. In that way, Vx node is switched ON and OFF periodically. That is to say, Vx node is either charged to Vbat or is pulled to zero. Resonant load CL and the transformer primary side inductor resonate over the course of the cycle.

One of the main drawback of this topology is that the duty cycle is somehow fixed to around 50%. Therefore, voltage regulation is constrained by the constant duty ratio. However, duty ratio and operation frequency are totally independent from the load changes. If external disturbance is introduced to the circuit then the circuit has a tendency to keep the duty cycle around the original ratio. Thus, the name *duty cycle detector* represents this feature.

Apart from this proposed topology, some-state-of art-Self-Oscillating DC/DC Converters are reported and tabulated in Table 3.1.

Table 3.1 *Self Oscillating DC/DC Converter Examples from Literature*

Features	**[11]**	**[21]**	**[24]**	**[5]**	**[1]**
Vin	24V	48V	24V	48V	1.1V
Vout	180V	5V	3-20V	12V	7V
Efficiency	80%	75%	93%	86%	25%
Operation Frequency	510kHz	>1MHz	200kHz	100kHz	1MHz
Output Power	50 W	20W	4W	100W	1mW
Converter Type	Boost	Buck	Buck	Buck	Boost
Discreet/Integrated	Discrete	Discrete	Discrete	Discrete	Discrete
Year Published	2012	2000	2012	2005	2012

3.2 Design Process and SPICE Simulations

Design process comprises discreet component selections. Regarding that, some analysis are performed in order to understand and determine the suitability of the components. For instance, fT (unity gain frequency) analysis is done to understand the

high frequency compatibility of the PMOS and NMOS transistors. Furthermore, transformer Q factor analysis is important as the transformer is the core part of the topology. Capacitor and inductor behaviors are subject to change whenever converter operates at much higher frequencies.

3.2.1 Transistor Selection

Understanding the data obtained from the datasheets of the components are not straightforward always. It may further require to employ SPICE model of the component provided by the manufacturer in the simulation. By that way, compatibility of the transistor, for example, can be inspected. Nonetheless, compatibility of a transistor can be examined through several aspects. As reported in [20],temperature, voltage ratings, on-resistance, power dissipation, current ratings, intrinsic capacitances and high frequency operable characteristic can be counted as the main criteria. However, for the proposed topology, what is crucial to inspect are particularly high frequency behavior, voltage and current characteristic and intrinsic capacitances with respect to dynamic losses of a MOSFET transistors. Breakdown voltage of the MOSFET namely VDS (Drain to Source Voltage) is the primary characteristic. It is the maximum allowed voltage that the MOSFET can withstand. After the breakdown voltage MOSFET is useless. The maximum VDS rating can be defined as the DC Voltage level plus spikes and ripples in the circuit. In Figure 3.3, current-voltage (I-V) characteristics of the main NMOS MOSFET M4 (SIB912DK) is examined using LTSPICE IV simulation tool [22].It can be understood from the Figure that voltage across its drain to source cannot be more than 21.5 V otherwise this MOSFET is no longer reliable. Similarly, same voltage stress evaluation is performed for other main complementary switching PMOS transistor Si1315DL. The datasheet of the Si1315DL PMOS transisor points out that breakdown voltage is 8V. As can be clearly seen from the SPICE simulation of this real model of Si1315DL PMOS transistor in Figure,, in practice it breaks down at 9.5 V source the drain voltage. Thus, whenever these two main transistors are employed in the design in a complementary manner, supply voltage for the converter is limited to 9.5 voltage. Therefore, transistor ought to be selected according to supply voltage design specifications. Nonetheless, for the proposed resonant-self oscillating converter supply voltage is aimed as 4V and these two switching transistors are met the requirements. But, it also means that proposed circuit can operate up to 9.5 V as the transistors can stand that much high voltage stress.

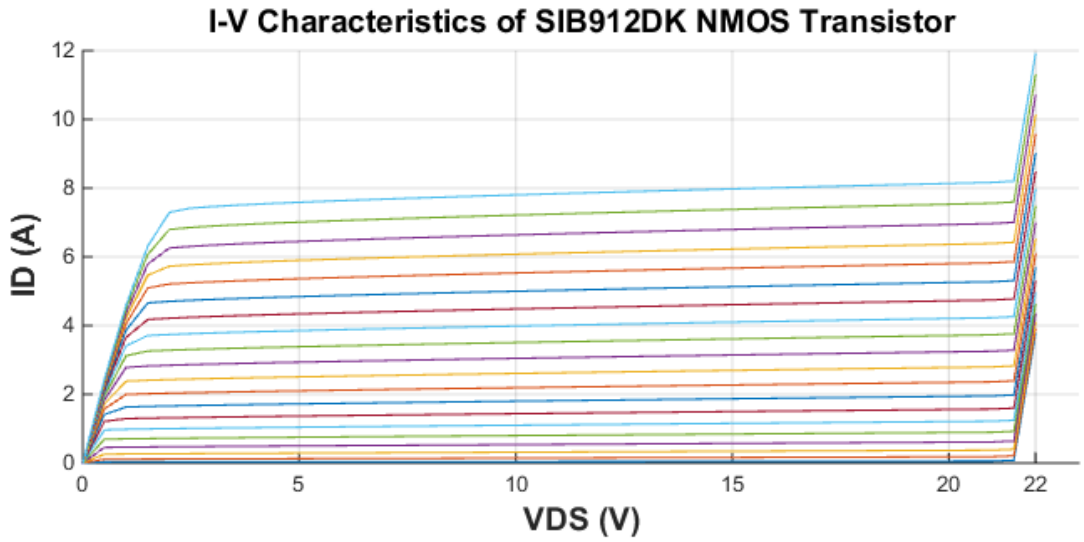

Figure 3.3 *I-V Characteristic of SIB912DK NMOS Transistor*

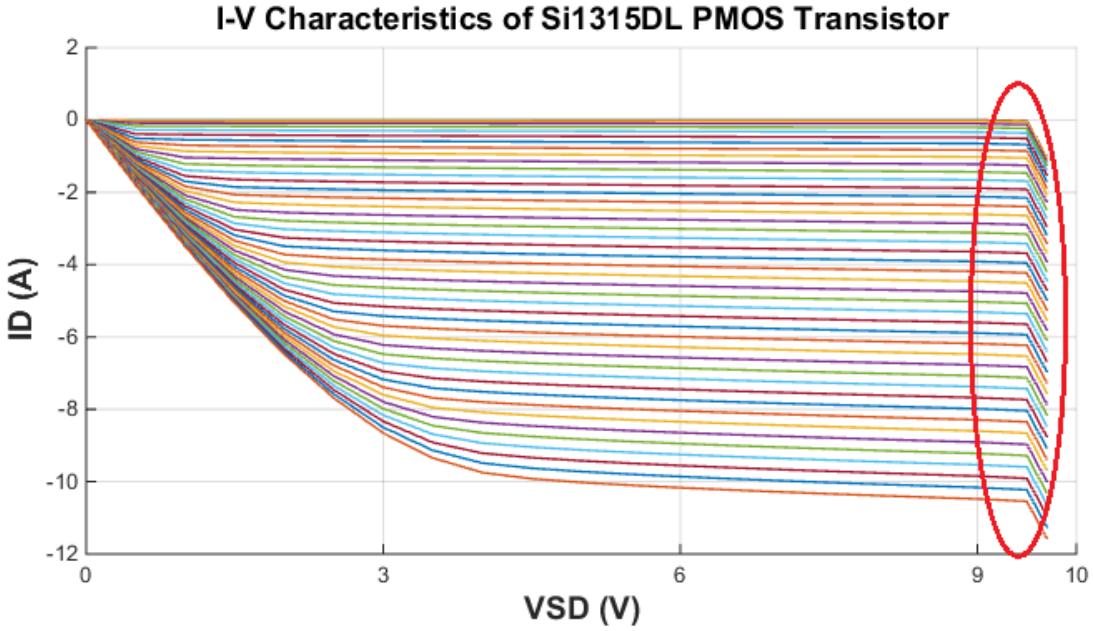

Figure 3.4 *I-V Characteristic of Si1315DL PMOS Transistor*

Size of the transistors are another substantial part of the transistor selection in terms of balancing performance of a single CMOS inverter in both PMOS and NMOS driver stage. In general, carrier mobility of the NMOS is usually 2-3 times bigger than that of PMOS[6]. In order to obtain the balance in the performance, width of the PMOS transistor must be 2 to 3 times larger.In parallel with that, current ratings of the discreet MOSFET transistors are considered as a base to achieve this ratio since current rating of the transistor is directly proportional to its width. What is more, largest transistors are determined as M1 (main PMOS), M4 (main NMOS), M2 and M3 (cascode transistors) in order to switch ON and OFF faster with the expense of larger energy dissipation.

fT Point Analysis of Discreet MOSFET Transistors

Unity Gain (β) corresponds to a point at which current gain becomes unity.[sedra simith] fT point analysis is used as an indicator to evaluate the high frequency performance of the transistor. In MOSFET transistor case, the ratio of drain current to gate current (Id/Ig) ought to be examined. If the fT point where the defined current gain drops to 1, is at a lower frequency than the converter operating frequency then this means that transistor can handle specified operation frequency.

Ideally, it is known that gate resistance of the MOSFET is infinite meaning that there is no current flowign through the gate.However, as the frequency starts increasing, intrinsic or adjunct capacitances of the MOSFET which are Cgs, Cgd and Cgb comes into play. Hence, an effective impedance at the gate of the transistor will begin to be seen. Then, AC current starts flowing into the MOSFETs gate. Since now there is a current flow, current to current gain starts decreasing (because now drain current is divided by a finite amount of current flowing in the gate) until the point where Cgd (gate to drain capacitance) is completely shorted. When that happens, it means that fT point is reached. It further means that MOSFET transistor is absolutely useless because input and output are shorted. As a result, fT analysis can be exploited to understand the high frequency behavior of the a MOSFET transistor.

In Figure 3.5, test bench of an fT analysis is demonstrated. AC analysis is applied to NMOS discreet transistor by means of the SPICE tool so that the current gain behavior is observed with the frequency sweep. The resulting waveform of current gain is also shown in below Figure. As can be understood form the Figure 3.5,,

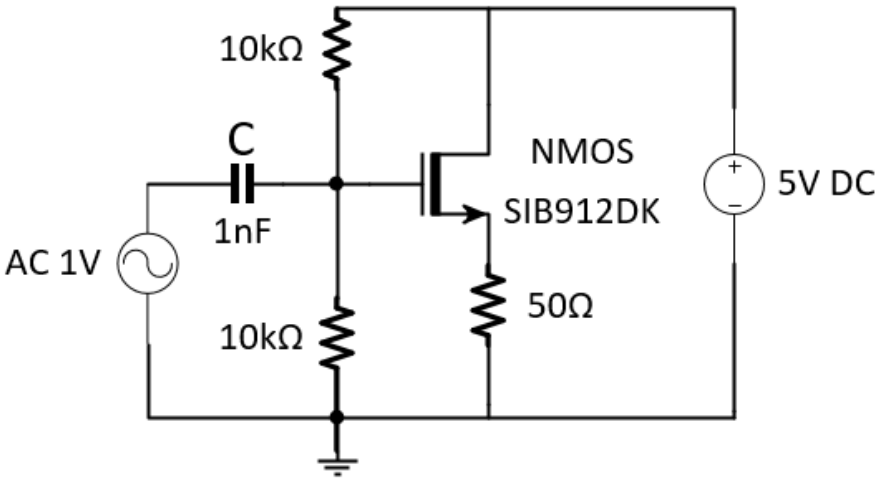

Figure 3.5 *fT analysis test bench of SIB912DK NMOS Transistor*

the ratio of drain current to gate current starts to decrease as the frequency rises. Eventually, around 4 GHz frequency, ft point where the gain is 0 dB (unity gain) is reached. As a result, it indicates that SIB912DK NMOS transistor which is employed as the main switching NMOS transistor is suitable for the proposed circuit.

Having observed that selected discreet NMOS is compatible with the operation frequency specification, complementary switching PMOS transistor SPICE model is also investigated with respect to high frequency operation requirements. Same fT analysis test bench with small modification in pull down resistor is applied to discreet Si1315DL , PMOS switching transistor.See Figure 3.7. Resulting waveform from the test is presented in Figure 3.8. Likewise, discreet NMOS transistor, complementary Si1315DL discreet PMOS transistor passed the test as well. Unity gain, fT point is detected around 1-2Ghz It appears that, it is still operable even in the vicinity of several GHz. But, after this range inspected transistor cannot be utilized.Nevertheless, it is still useful in the proposed circuit operation frequency range.

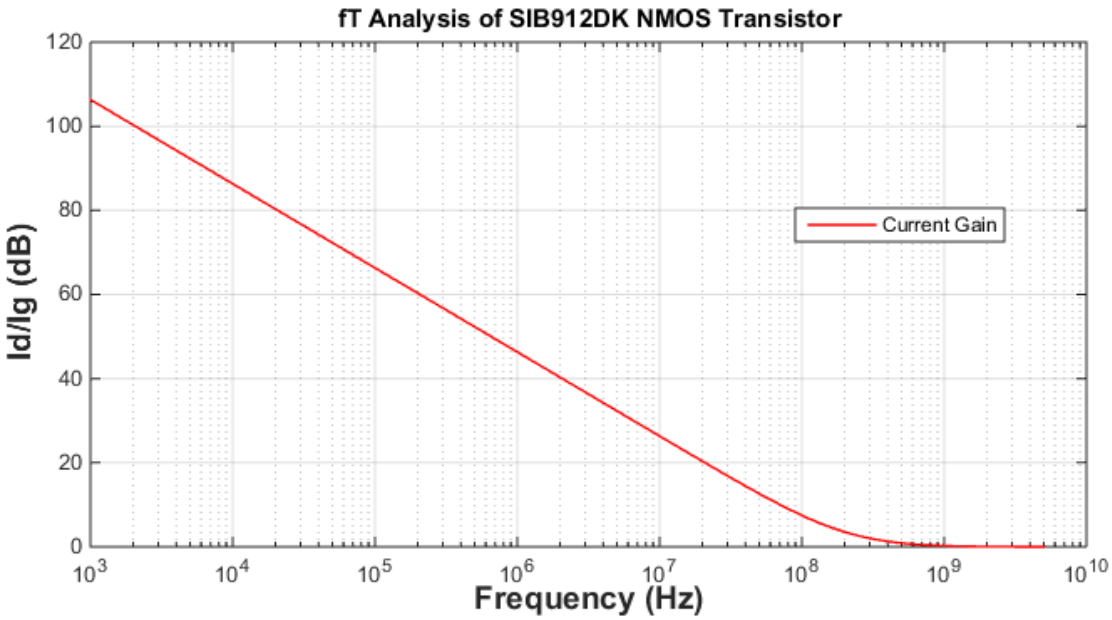

Figure 3.6 *fT analysis waveform of SIB912DK NMOS Transistor*

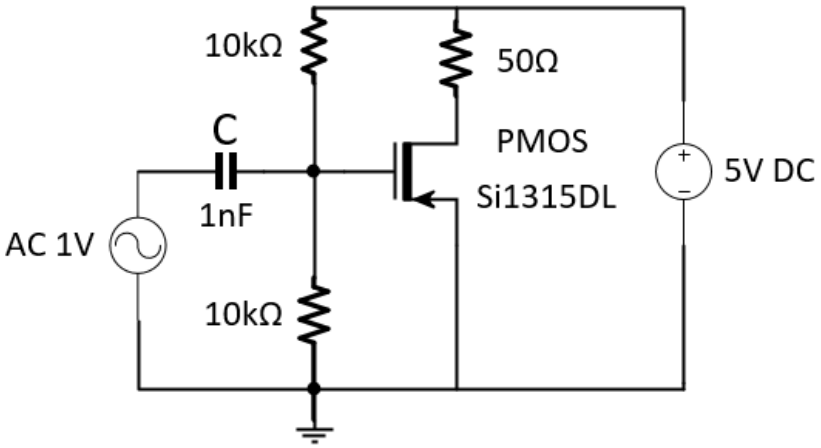

Figure 3.7 *fT analysis test bench of Si1315DL PMOS Transistor*

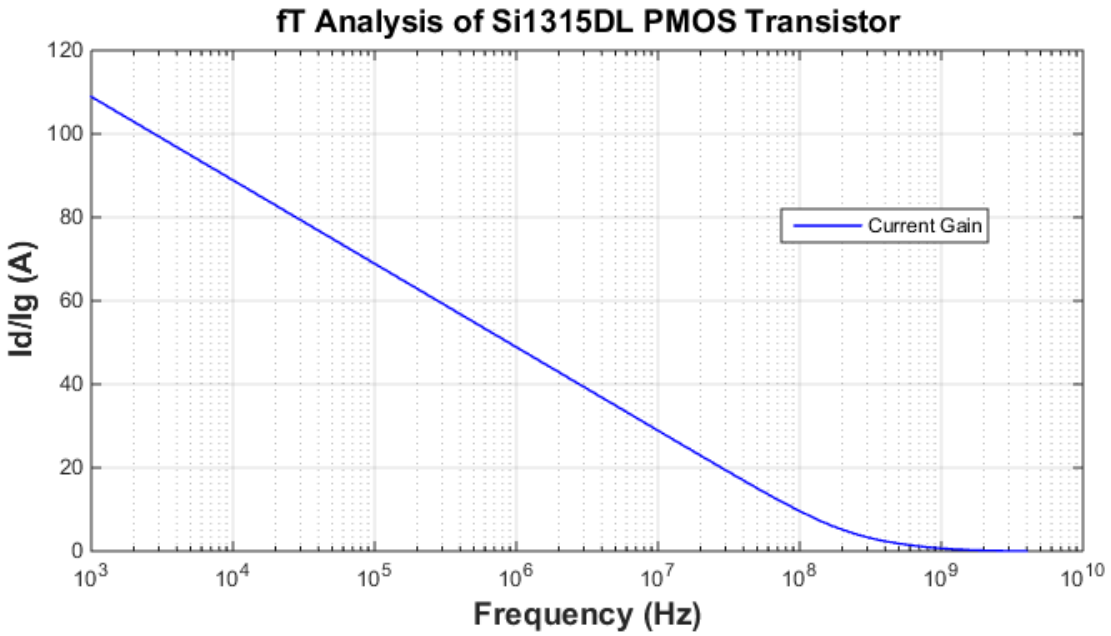

Figure 3.8 *fT analysis of Si1315DL PMOS Transistor*

3.2.2 Transformer Selection and Quality-Factor Analysis

Efficiency considerations of a transformer become more substantial as high frequencies are achieved. Quality Factor is basically a measure of efficiency in an inductor. Ideally, an inductor,as the core part of a transformer, has no resistance and therefore no losses. However, in practice, due to the windings consisting of metal wires in the coil, naturally there is a series resistance with the inductor. As a consequence, it causes losses in the inductor in the form of heat and a loss in inductive quality. Hence, Quality Factor (Q)can be defined as the ratio of its inductive impedance (imaginary part) to its resistive impedance (real part) which is dimensionless at a given frequency .The higher the Q factor, the lower the loss of passive device[18]. In other words, the higher the Q factor, the closer ideal and lossless behavior of an inductor,therefore,a transformer. As a result, Q factor can be exploited to gain an insight about the characteristic of a transformer. In addition, it can be noticed from the Figure 3.1 that primary side of the transformer is employed as a filtering inductor at the same time in the proposed converter.

Quality of an inductor is given in the following formula[4]:

$$Q = \frac{imag(Zind)}{real(Zind)} \tag{3.1}$$

Q factor test benches for short and open circuit tests are provided in Figure 3.9 and Figure 3.10 [2]. Open circuit and short circuit tests are applied to 750312547 Würth Electronics Midcom off-chip transformer SPICE model.

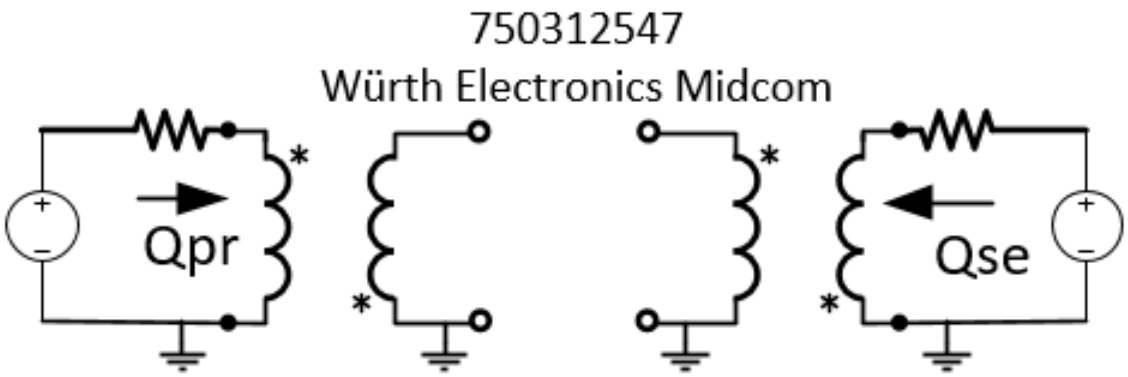

Figure 3.9 *Q-factor Open-Circuit Test Bench*

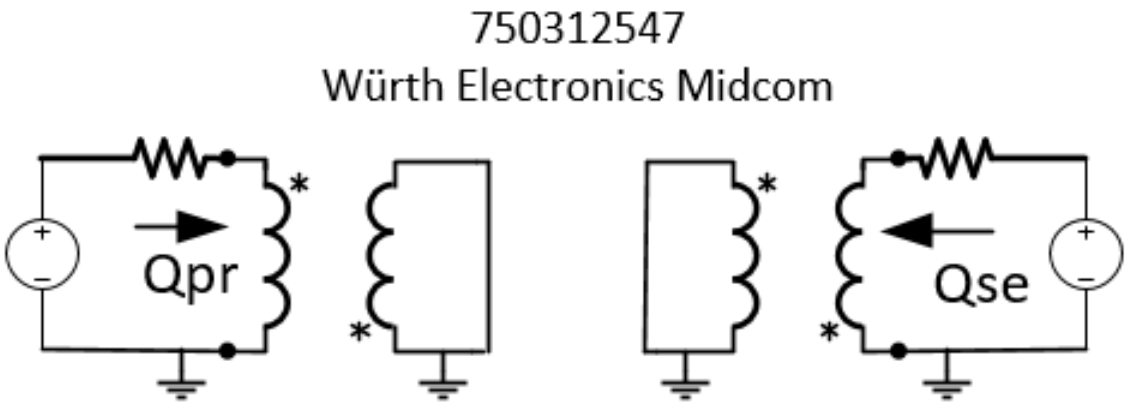

Figure 3.10 *Q-factor Short-Circuit Test Bench*

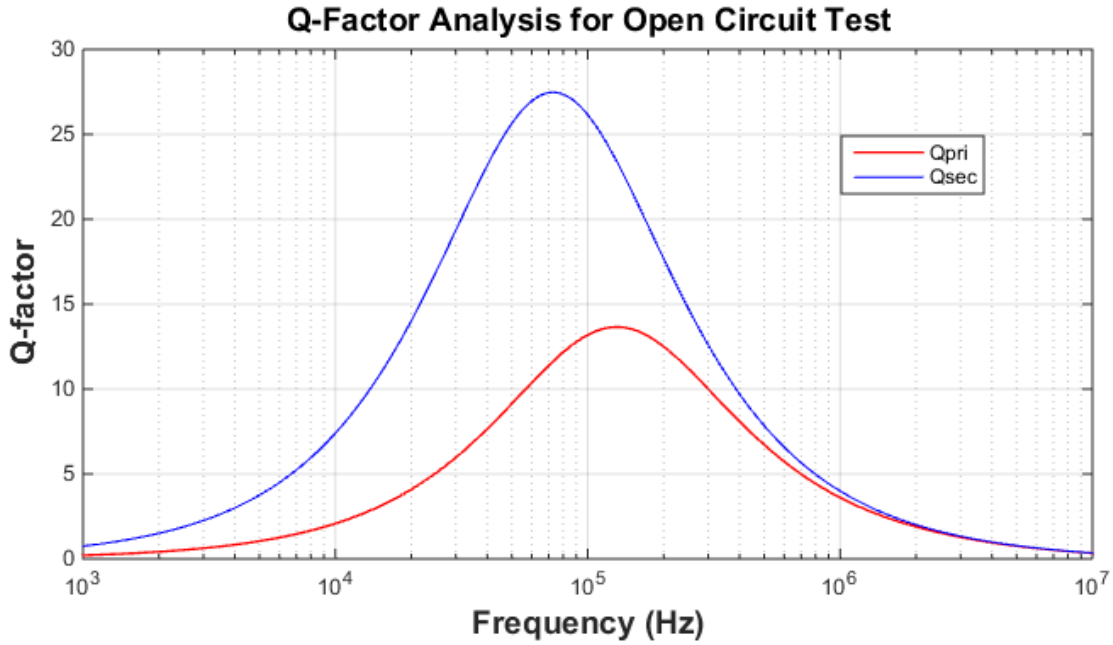

Figure 3.11 *Q-factor Open-Circuit Test Result*

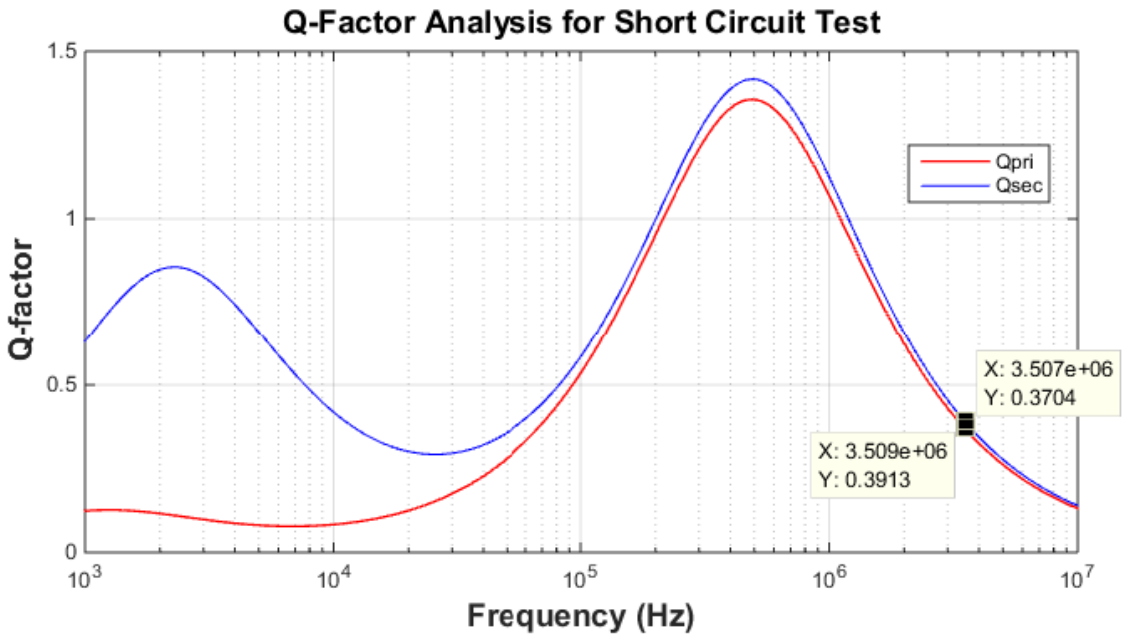

Figure 3.12 *Q-factor Short-Circuit Test Result*

Resulting waveform for the open circuit test in depicted in Figure 3.11.Open circuit test is done such that Q factor for the primary side is measured while secondary is open circuited and for the secondary side measurement primary side is open circuited. According to provided waveform, Q factor for both primary and secondary side is 1.135 at 3.4 MHz operation frequency. Similarly for the short circuit test, same procedure is followed but each terminal is short circuited respectively. By inspecting the Figure 3.12, Q factor for the primary side is 0.371 and for the secondary side, it is measured as 0.392 again at 3.4 MHz frequency. Based on the presented simulation measurement results one can infer that the evaluated transformer may not be the best choice in terms of the efficiency performance within the existing market. Nonetheless,it is still compatible with the aimed operation frequency and fairly good for desired efficiency level.

Some important transformer parameters for the discreet design of the proposed converter is tabulated in Table 3.2 [14].

Table 3.2 *750312547 Würth Electronics Midcom Transformer Parameters*

Parameters	**Primary Side**	**Secondary Side**
DC Resistance	0.03Ω	0.48 Ω
Inductance	1uH	1uH
Leakage Inductance	35nH typ.	not specified
Turns Ratio	2.4	1

3.2.3 Capacitor Selection Considerations

High frequency behavior analysis of the capacitors are one of the key concepts when high frequency ranges are concerned. Capacitors have many parasitics which are only relevant at high frequencies as mentioned in Chapter 2. Whenever high frequencies are applied, behavior of the capacitor changes. After a certain frequency, they start to act as an inductor. In other words, as the AC current flows through the capacitor, it creates a magnetic field. This causes an inductance in the capacitor structure resulting a notable self resonance of a capacitor in addition to its ideal behavior. Hence, low impedance characteristic at the desired operation frequency is a critical indicator while choosing a capacitor. Why it is desirable to have lower impedance at higher frequencies is that if the capacitor has even a few nH range inductance, then narrow, high amplitude spikes will be generated which is dictated by di/dt of the parasitic inductor[17].

Based on this discussion, high frequency behavior of the discreet capacitors in the proposed circuit (capacitors in Duty Cycle Detector and output filtering capacitors) are inspected through their SPICE models. Testing capacitors are picked to be a chip monolithic ceramic capacitors which are mostly considered to offer lowest impedance at 500 kHz and beyond. Test bench of the analysis is demonstrated in Figure 3.13

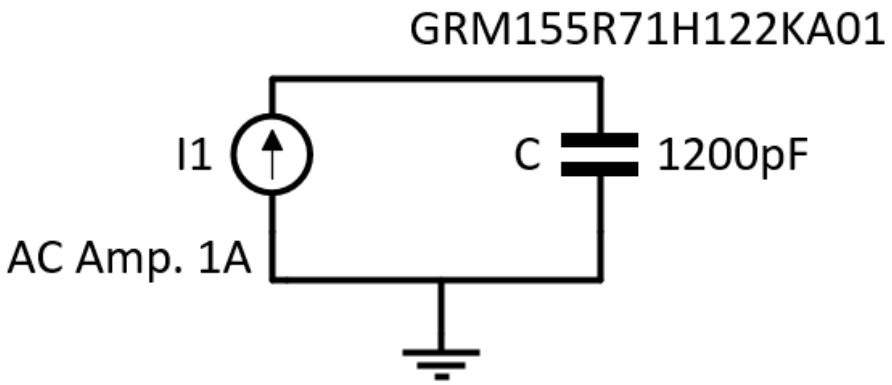

Figure 3.13 *High Frequency Analysis Test Bench*

Impedance characteristic of the testing capacitor which is employed in duty cycle detector stage as AC ground is simulated and result is depicted in Figure 3.14. According to the Figure, at the desired operating point that is 3.4 MHz, capacitor tends to keep its capacitive characteristics which is desirable for the proposed topology.

Similarly, for the filtering capacitor chip monolithic ceramic capacitor is utilized. As remarked in[17], at high frequencies, most of the capacitors approach an inductive line of about 1nH to 5nH. Smaller units in parallel will reduce the effective inductance. Therefore, at the filtering stage, instead of one single capacitor, three capacitors are connected in parallel satisfying the same capacitor value as single one does in order to diminish effective impedance. Hence, efficiency is increased slightly.

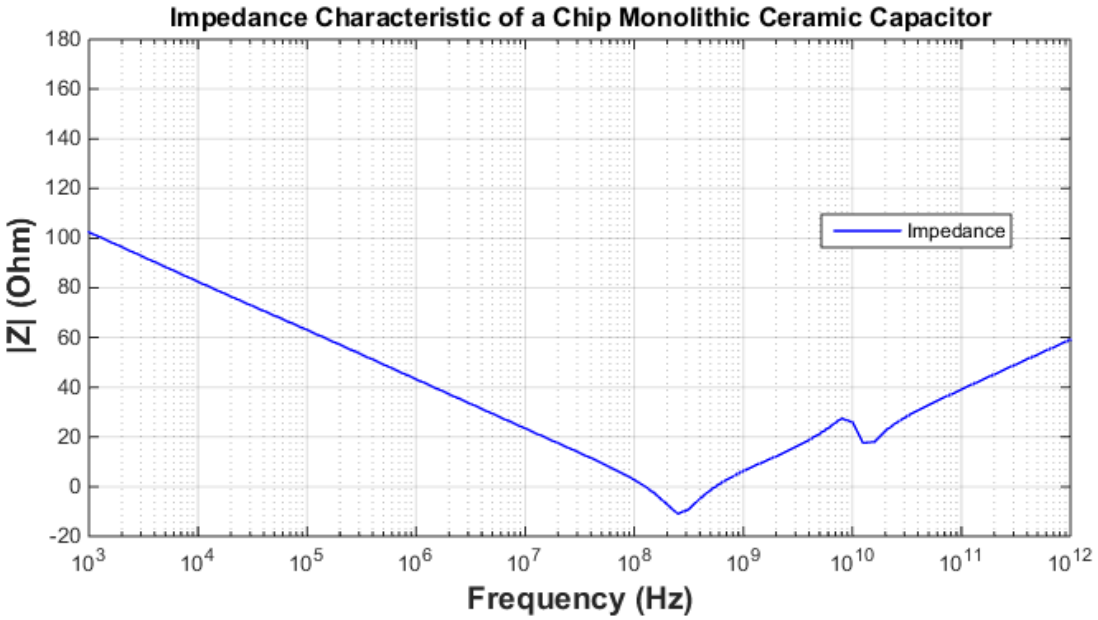

Figure 3.14 *Impedance Characteristic of a Chip Monolithic Ceramic Capacitor*

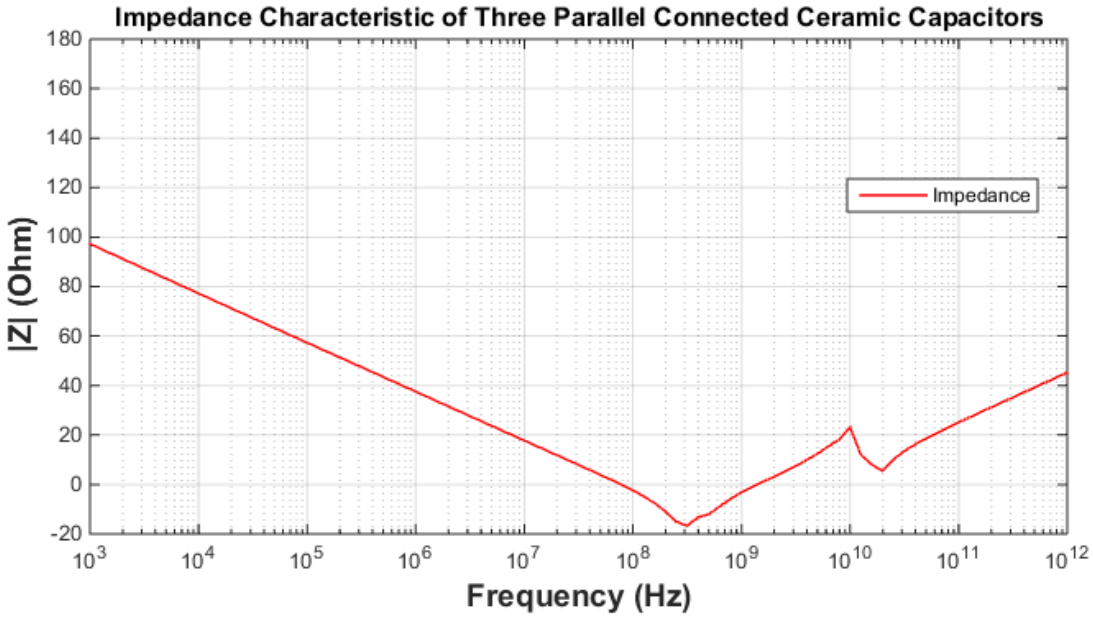

Figure 3.15 *Impedance Characteristic of Three Parallel Connected Filtering Capacitors*

In Figure 3.15 frequency depended behavior of three parallel capacitors are simulated and demonstrated. As seen by the above Figure, equivalent filtering capacitor is compatible with the target operation frequency since self-resonant frequency is far beyond 3.4 MHz.

3.2.4 Printed Circuit Board Parasitic Model

Resonant Self-Oscillating Converter is designed for PCB implementation. Therefore, possible parasitics that can exist in practice are taken into consideration. Printed Circuit Board (PCB) parasitics takes the form of undesired resistance, capacitance and inductance embedded in the PCB. Especially with the high frequencies, parasitics becomes more visible and affect the overall efficiency significantly.

As stated in [19], when a component is soldered between two microstrip traces in a board, inductance and capacitance of the component will be affected by the place of the component relative to the ground plane. Similarly, when a component is soldered to a ground plane, via path will create an inductance. There is both resistance and inductance exist associated with the via to ground plane. Moreover, plane layers of the PCB exhibit parasitic capacitance due to the fact that positive voltage plane and ground plane are parallel to each other.

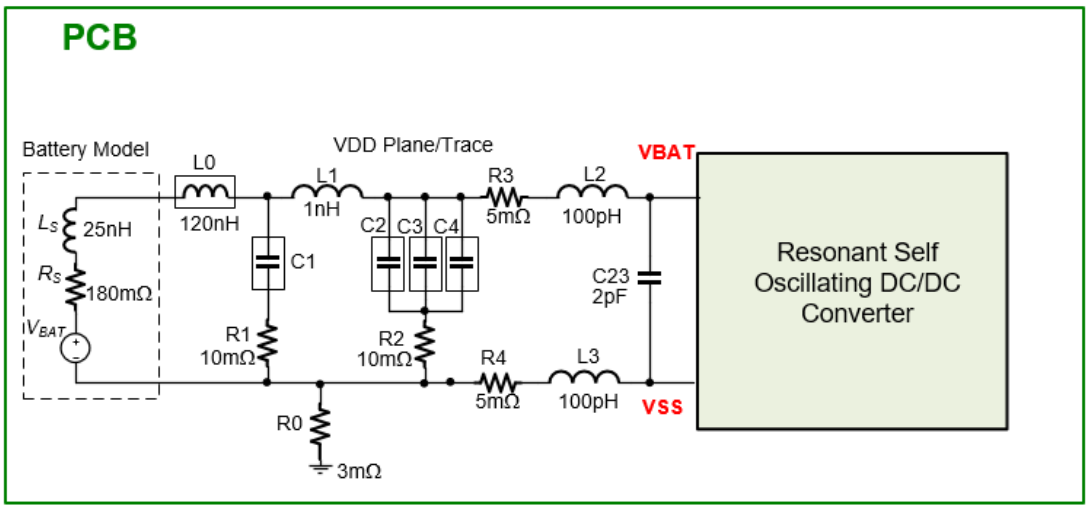

Figure 3.16 *Input Side PCB Parasitics*

Ideally a short circuit must have a zero impedance. However, there is a finite resistance and inductance under self resonant frequency according to measurements[19]. It is even impractical to consider the ground plane as pure ground. When it is measured at high frequencies, one can realize that ground is no longer zero since it contains inductive and resistive parasitic elements.

Bearing all these in mind, both input side and output side PCB parasitics are modeled in order to increase the accuracy of the simulation. Input side PCB parasitics and output side PCB parasitics are depicted in Figure 3.16 and in Figure 3.17 respectively.

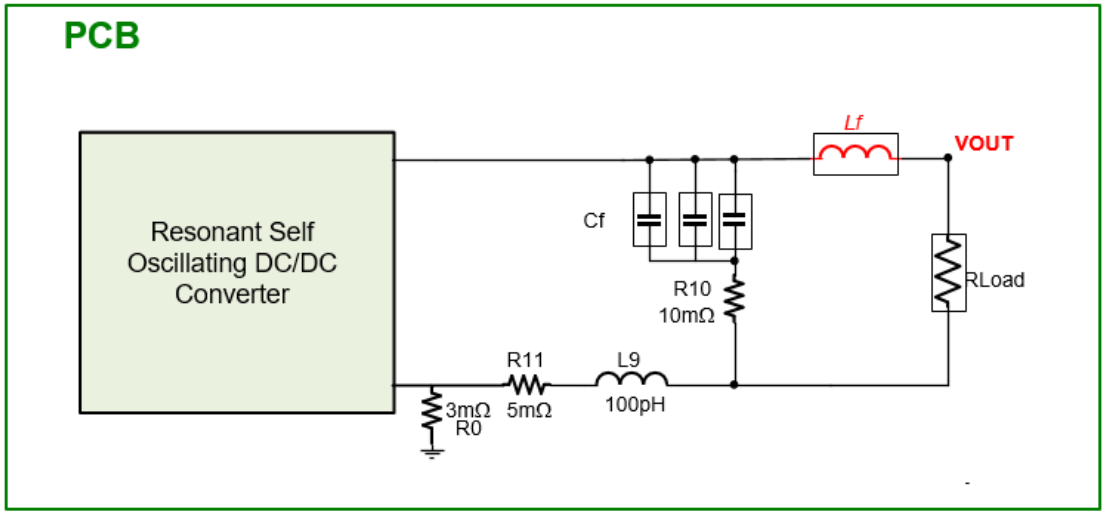

Figure 3.17 *Output Side PCB Parasitics*

A table which indicates purpose of some of the input and output side PCB parasitics are also presented below.

Table 3.3 *Description of PCB Parasitics*

Parasitic Elements	Value	Purpose
R0	3m Ω	Ground Plane
R1, R2, R10	10m Ω	Via+Trace Resistance
R3, R4, R11	5m Ω	Trace Parasitics
L2, L3, L9	100pH	Trace Parasitics
L1	1nH	VDD Plane
C23	2pF	PCB Parasitic

3.3 Selected Components and SPICE Simulation Circuit

As the discreet component selection process is thoroughly explained, list of selected components such as transistors and passive elements is tabulated and provided below. The lists comprise the most important components, their manufacturers and the purposes in the circuit. In Table 3.4 , list of transistors that are utilized are tabulated.

Table 3.4 *List of Transistors Employed*

Component Name	Manufacturer	Purpose
SiB912DK	**Vishay Semiconductors**	Main Switching N-type MOSFET
Si1315DL	**Vishay Semiconductors**	Main Switching P-type MOSFET
Si1553CDLP	**Vishay Semiconductors**	CMOS pair P-type MOSFET
Si1553CDLN	**Vishay Semiconductors**	CMOS pair N-type MOSFET
US6M1N	**Rohm Semiconductors**	Level Shifter NMOS Transistor
VT6M1P	**Rohm Semiconductors**	Diode PMOS Transistor
VT6M1N	**Rohm Semiconductors**	Dead-Time Latch NMOS Transistor

In Table 3.5, list of the important passive elements used in the components are tabulated in a same manner with their manufacturers and purposes in the circuit.

Table 3.5 *List of Passive Components Employed*

Component Name	Manufacturer	Purpose
750312547	**Wurth Electronics Midcom**	High-Speed Transformer
GRM155R71H122KA01	**Murata Electronics**	Voltage Clamp Cap.
GRM155B11E102KA01	**Murata Electronics**	Output Filter Cap.
GRM155R71H821KA01	**Murata Electronics**	Output Filter Cap.
GRM155R71H391KA01	**Murata Electronics**	Output Filter Cap.
GRM155B11E103KA01	**Murata Electronics**	Voltage Clamp Cap.
GRM152B31A104KE19	**Murata Electronics**	Input Filter Cap.
GRM155B11E222KA01	**Murata Electronics**	Input Filter Cap.
GRM033R71E121KA01	**Murata Electronics**	Input Filter Cap.
HL-8113	**Hurricane Electronics**	Output Filter Inductor

As mentioned before, SPICE simulations with the real SPICE models of the components are carried out by means of LTSPICE IV simulation tool. The proposed converter circuit is depicted in Figure 3.18.

As can be seen in the above configuration, on the upper left side battery that is used as input voltage source is modeled with its parasitic components. In order to obtain

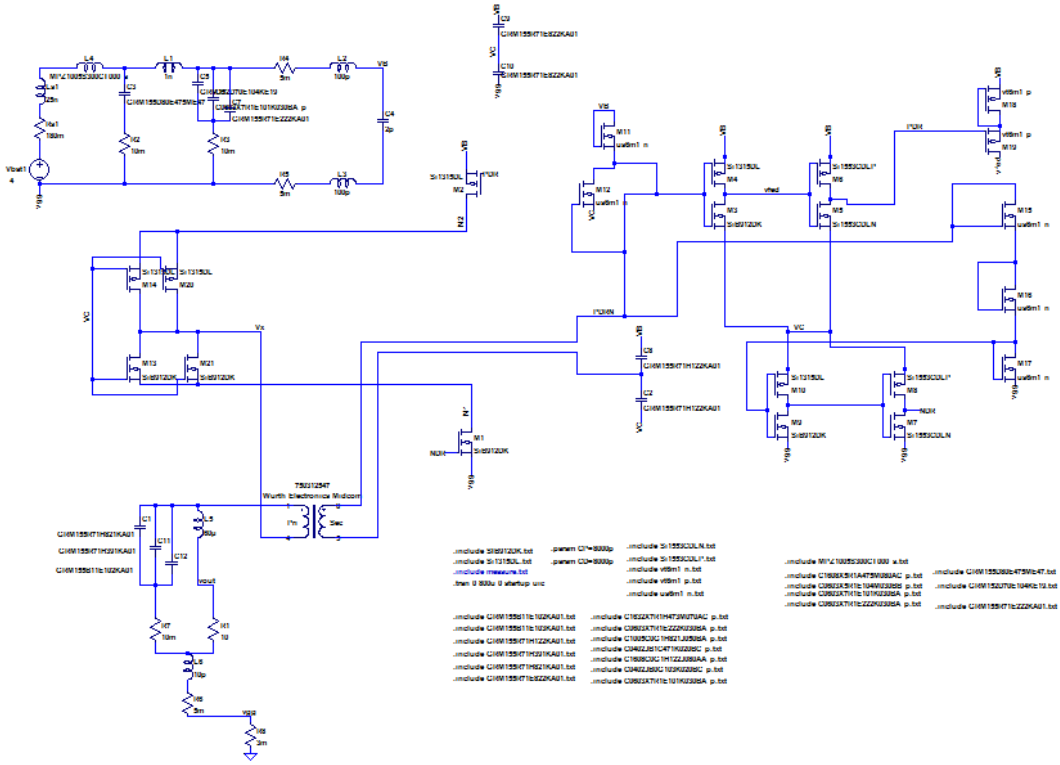

Figure 3.18 *Resonant Self-Oscillating DC/DC converter SPICE Simulation Circuit*

Vbat/2 voltage, Vbat voltage is clamped by voltage divider capacitors. On the right hand side, pulse shaping circuit composed of level shifter and CMOS buffers both in low and upper side. Finally on the low side, high speed transformer and output stage of the circuit again with their parasitic components are located.

4. SPICE SIMULATION RESULTS

Resonant Self Oscillating Converter is simulated by means of LTSPICE IV SPICE simulation tool. Simulation is conducted for $4V$ supply voltage (battery model) and 10 Ohm resistive load. Real SPICE models of the all components are obtained from the manufacturers' web sites so that the fully accurate simulation results are targeted. In addition to this, simulation setup is prepared such that the PCB implementation of the proposed converter will be applicable. For instance, beside the real SPICE models, possible PCB parasitics which is a serious problem for a converter operating high frequencies are taken into account and modeled in the simulation circuitry. Operation principle of the resonant self oscillating circuit is meticulously described in 3.1 and power stage of the proposed converter is provided in Figure 3.2. In this chapter, waveform analysis of the results are performed and the effect of automatic dead-time enhancement is depicted. Additionally, efficiency of the converter is evaluated in terms of losses in each component in the circuit.

4.1 Waveform Analysis

NMOS and PMOS gate drive signals are presented in Figure 4.1 Positive feedback signals provided by the transformer are in the the form of sinusoidal signals. Through the inverter stages both in NMOS and PMOS side such sinusoidal driving signals are transformed to square shape signals which is better for the efficiency of the converter[2]. Pulse shaping is performed by means of the regenerative property of the cascaded CMOS inverter stages. That is to say, inherently, CMOS inverter stages have an ability to restore the proper logic value despite of the non-ideal input levels. Thereby, cascaded CMOS inverter buffer is employed in order to exploit this property and therefore, shape the sinusoidal feedback signals and acquire proper square waves. Furthermore, by means of the driver stages automatic dead-time which is necessary for the zero voltage switching (ZVS) operation is introduced. Whenever the converter operates in ZVS, short-circuit losses can be prevented. In

Figure provided below, obtained high-to-low dead-time is measured as 0.226 us. However, as can be seen, there is no dead time for low-to-high transition which still causes short circuit losses. This problem is solved by automatic dead time enhancement circuitry which is explained in 5.

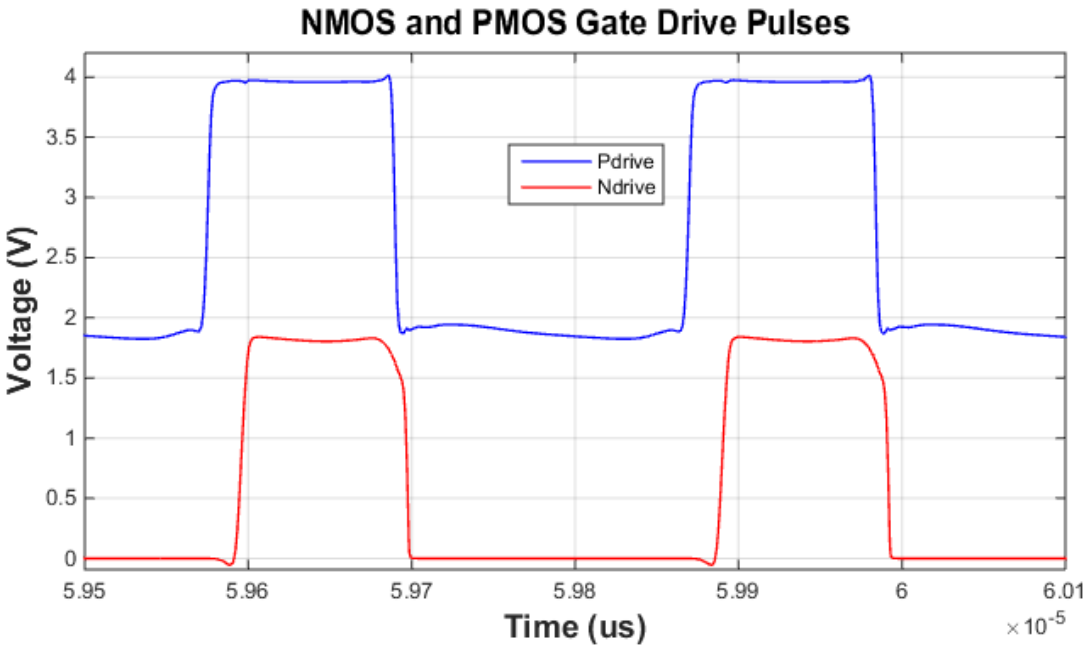

Figure 4.1 *Gate Drive Pulses*

Switching node Vx voltage and transformer primary side current Ix is shown in Figures 4.2 , and 4.3. Ix either charges the intrinsic capacitances of the MOSFETs connected to Vx node to $VBat$ or discharges them to the ground. Switching frequency at the node Vx is measured as **3.4 MHz**.

Along with that, the transformer primary side current Ix, resonates with the output filtering capacitances at a frequency which is very close to the operating frequency of the proposed converter. This resonant frequency is calculated as follows:

$$fr = \frac{1}{2 \times \Pi\sqrt{L \times C}} \tag{4.1}$$

Given that transformer primary side inductance is **L=1uH** and equivalent output filtering capacitance is **2.2nF**, resonant frequency is calculated as **3.39 MHz**. It clearly indicates that this resonant behavior is helping the converter to sustain its

self oscillating function. Thereby, it justifies the name *resonant self- oscillating DC/DC converter.*

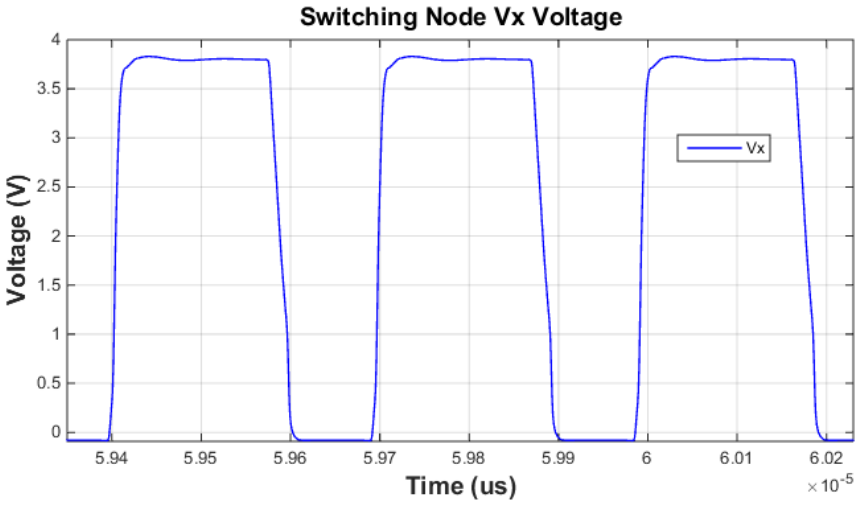

Figure 4.2 *Switching Node Vx Voltage*

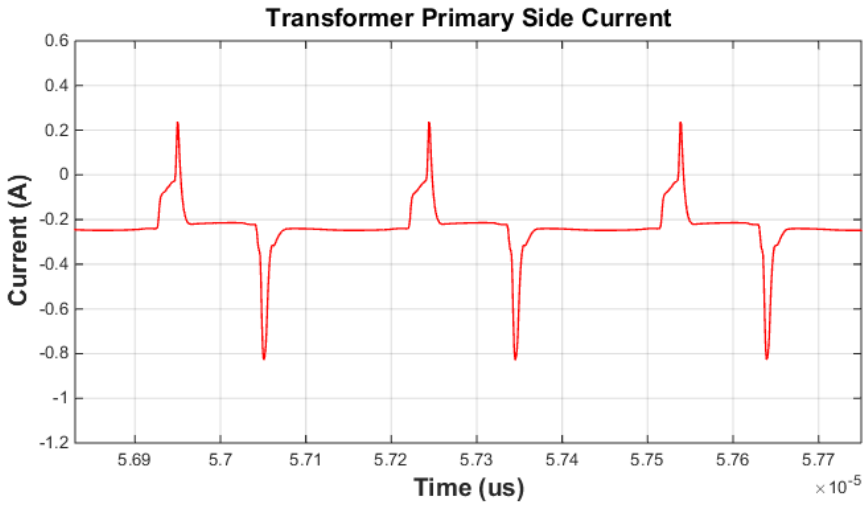

Figure 4.3 *Transformer Primary Side Current Ix*

Output voltage waveform are depicted in Figure 4.4. Average output voltage is properly smoothed by the LC filter and its value is measured as **2.34 V** which means that the duty ratio (D) is for the proposed circuit is 58.5% or 0.585. Voltage ripple is quite small and measured as **30mW**.

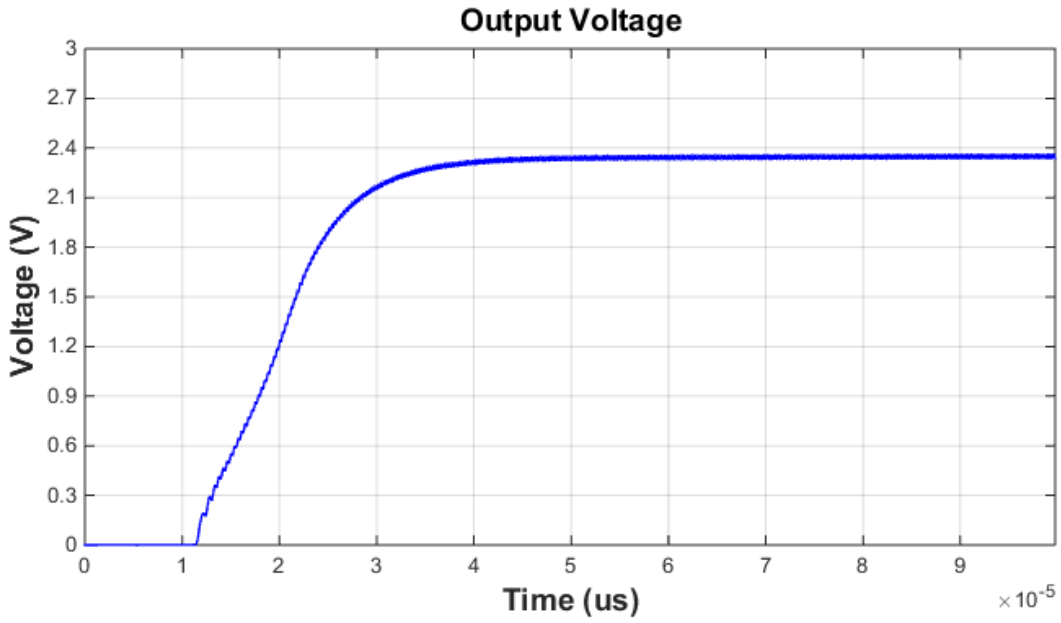

Figure 4.4 *Output Voltage*

Two level of input voltages $Vbat$ and $Vbat/2$ is showed and the effect of PCB parasitics can be noticed clearly. See Figure 4.5 In addition, as mentioned before, feedback signal provided by the secondary side of the transformer is not in the form of pulse but mostly a sinusoidal signal. Thanks to regenerative property of the cascaded CMOS inverter stages which are used as a driver circuit, this sinusoidal signal is transform into almost perfect square waves. This property can be seen in Figure 4.6.

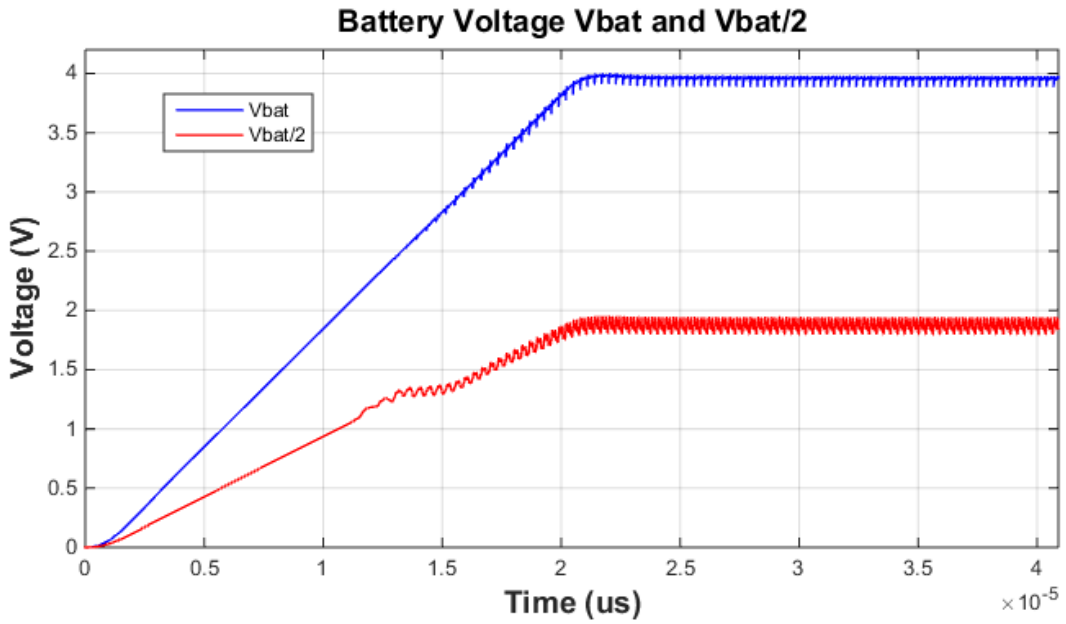

Figure 4.5 *Simulated Battery Voltages*

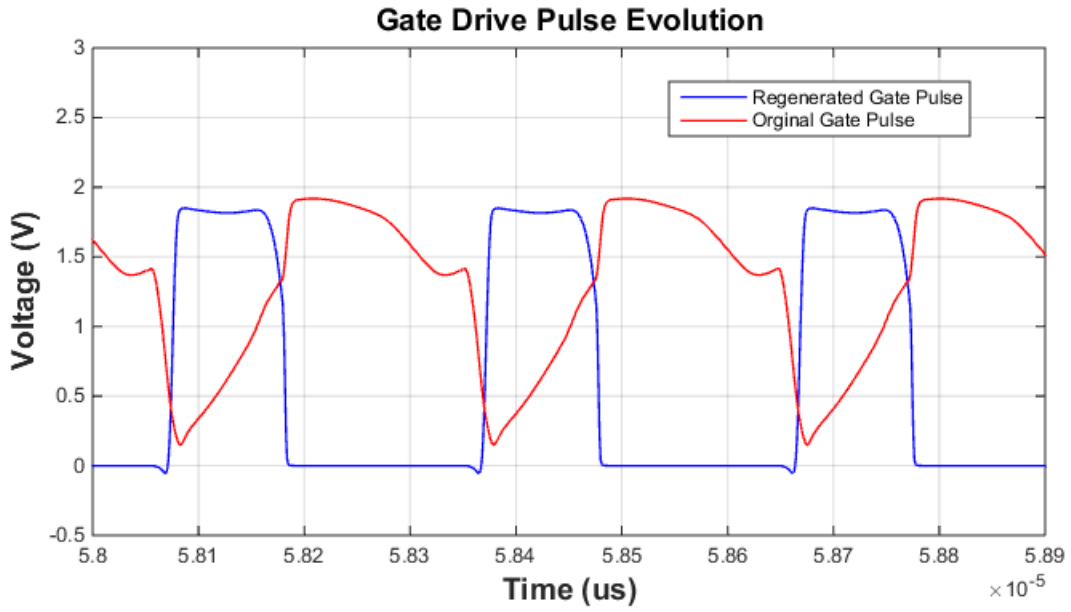

Figure 4.6 *Regenerated Feedback Signal*

4.2 Efficiency Analysis

The efficiency of the proposed converter is **71%**. Input power delivered by the battery is **781.22 mW** and output power is **549.62 mW**. The loss contribution of the all components in the circuit is examined and demonstrated in Figure„. According to this analysis, it is found that the cascode structure consumes the largest amount of power. Type of losses that causes efficiency to mitigate are MOSFET static and dynamic losses, transformer i^2R losses and magnetic losses and lastly the losses due to the parasitics in the PCB which particularly contributes at high frequencies. Along with that, since during low-to-high transition of the Vx signal there is no dead-time between gate pulses which introduces short circuit losses in the circuitry and degrades the efficiency.

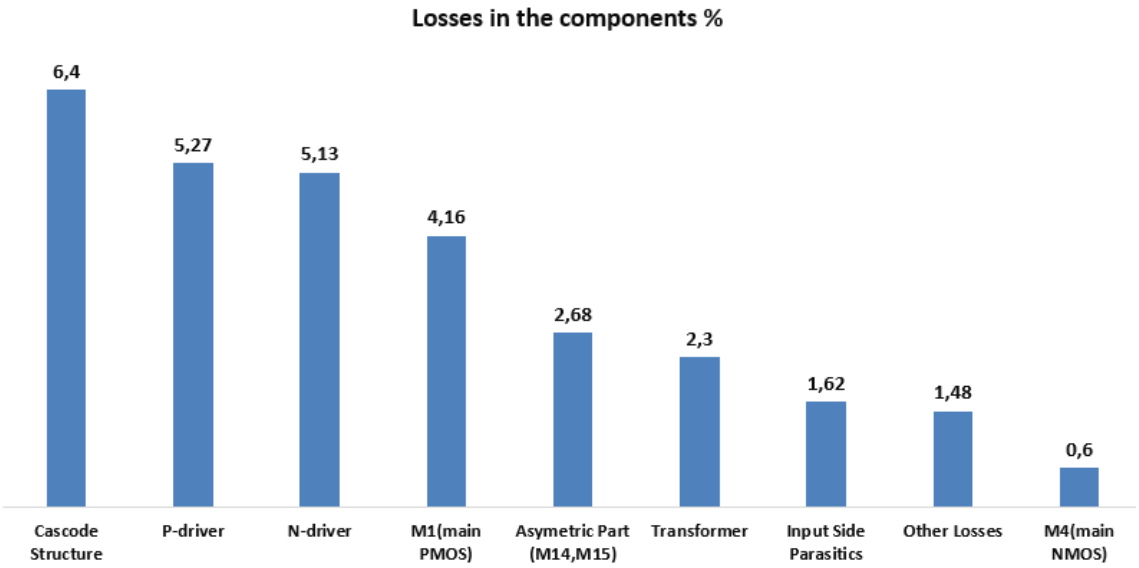

Figure 4.7 *Loss Contribution of the Components*

Finally, achieved converter specifications are presented in Table 4.1 and in Table 4.2. The results are obtained in the existence of possible PCB parasitics and employing real SPICE models of the transistors, transformer and other passive elements. What is more, as remarked before deficiency is one of the major concern of this proposed converter,therefore, the achieved efficiency is slightly increased by implementing additional automatic dead-time latch circuitry. Operation principle and implementation is studied in the upcoming chapter.

Table 4.1 *Achieved Circuit Specifications*

Supply Voltage(V)	Load (Ω)	fs (MHz)	Duty Cycle (%)	Efficiency (%)
4V	**10**	**3.4**	**58.5**	**71.0**

Table 4.2 *Achieved Output and Power Specifications*

Vout(V)	Iout (mA)	Input Power (mW)	Output Power(mW)
2.34±30 mV	**234**	**781.22**	**549,62**

5. AUTOMATIC DEAD-TIME ENHANCEMENT

In order to improve the efficiency of the resonant self oscillating converter further, high speed dead-time architecture is added to the original circuit structure. Formerly, automatic dead-time is obtained for high-to-low transition (DTHL) of Vx signal. However, for the low-to-high transition (DTLH) of Vx signal, dead time was zero. Meaning that, there are still short circuit losses exist. Thus, automatic dead time control is necessary to prevent short circuit path formed due to the incorrect dead time during the low-to-high transition of Vx signal. In Figure 5.1, dead time latch circuity is depicted for low-to-high transition (DTLH).

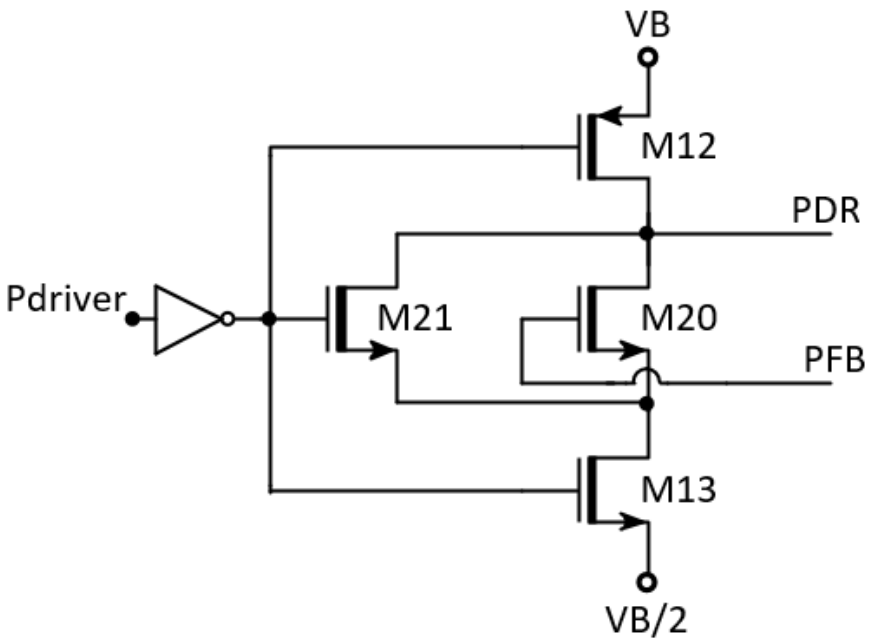

Figure 5.1 *Dead-Time Control Circuitry for DTLH*

The dead-time between driving signals is adjusted for DTLH utilizing a latch circuitry [10] formed of M12, M20 and M13. In order to obtain a dead time for DTLH, main PMOS switching transistor must switch ON with a delay after the main NMOS

switching transistor switch OFF. See Figure 5.2.

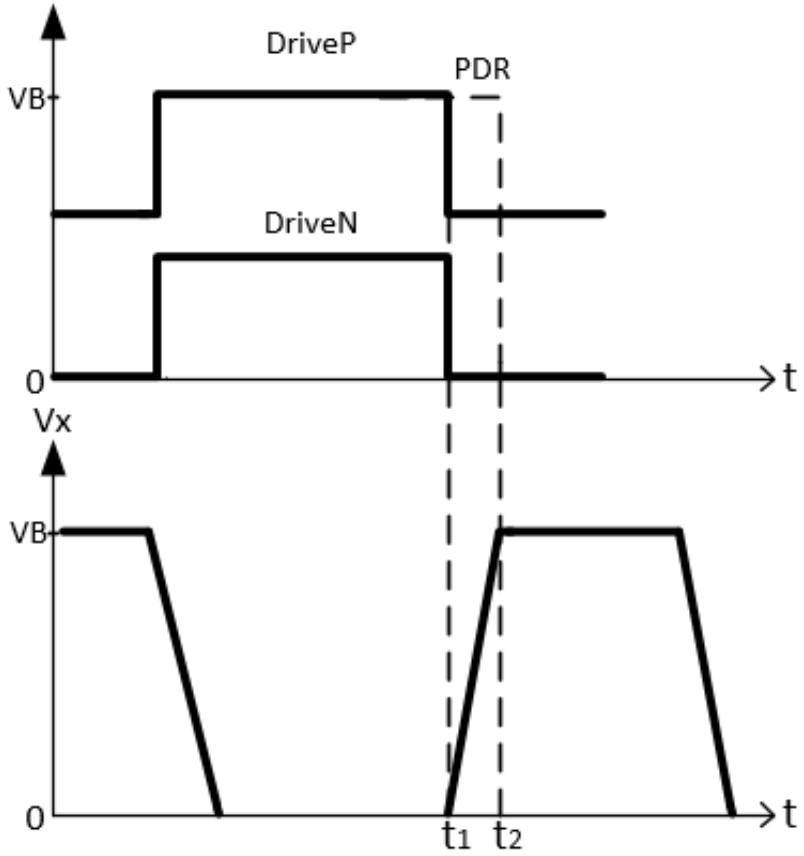

Figure 5.2 *Time Diagram for DTLH*

Function of the M20 transistor is to delay the main PMOS switching transistor to turn ON. This function of the M20 transistor can be explained as follows: at the time t1, M13 is ON and PFB node where all the capacitances are connected is equal to VB/2+|VTP| (VTP is the PMOS threshold voltage) by the pass transistor logic. As transistor M20 stays in OFF state, main PMOS switching transistor will not turn ON so that time delay will occur and dead time will be created. But dead time duration is limited by the charging time of the capacitances connected to PFB node. Meaning that, as the capacitances are charged by the reverse inductor current, PFB node voltage will increase and will be larger than VB/2. Therefore, M20 will turn ON and enables main PMOS switch to turn ON. As can be understood, duration of the dead time depends on the charging time of the capacitances connected to PFB node by the transformer primary side inductor current. Because, as long as PFB node voltage is smaller than VB/2 voltage main PMOS switching transistor will not

be turned ON by M20 so that the dead time will be obtained. What is more, purpose of the transistor M21 is to help with the correct start up of the circuit. It provides small initial current to the gate of the main PMOS switching transistor until the inductor current reaches sufficient reverse current [10]. Size of the transistor is quite small compared to M20. Furthermore, enhanced dead-time (DTLH) is presented in the results chapter. The overall resonant self oscillating converter circuit with automatic dead time enhancement structure is also depicted in Figure 5.3

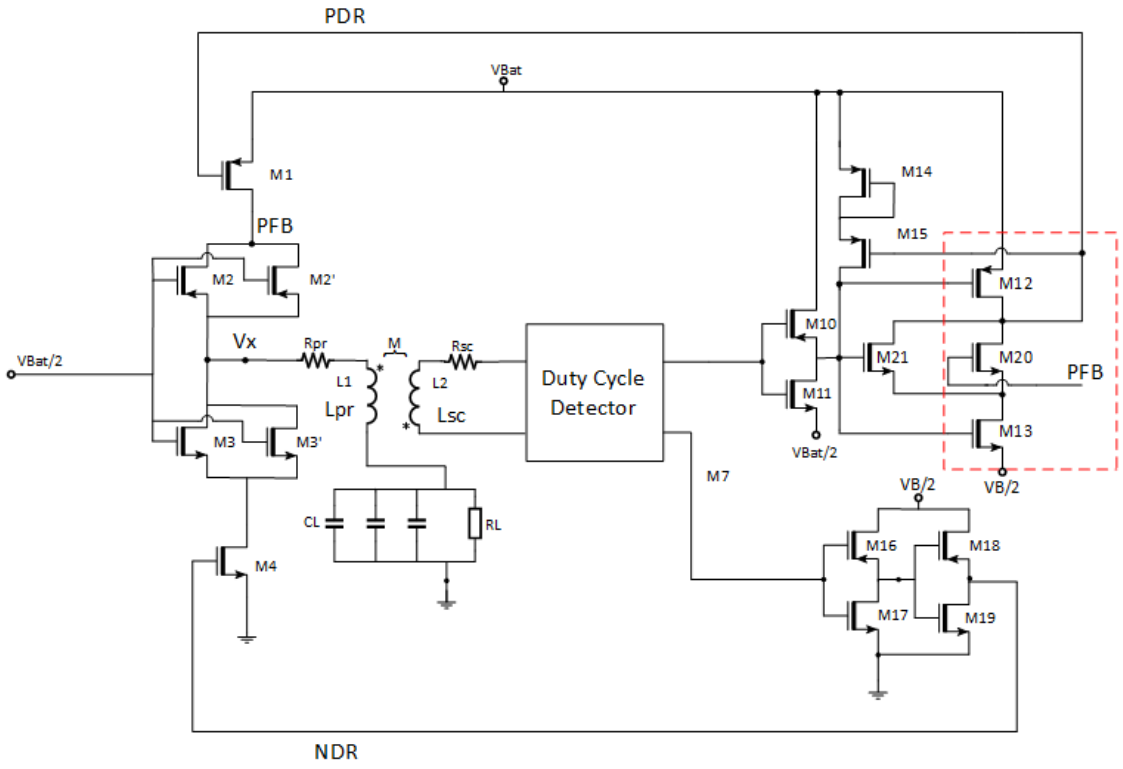

Figure 5.3 *Resonant Self Oscillating Converter with Automatic Dead Time Enhancement*

It is should be noted that dead-time circuitry placed next to the first CMOS inverter stage by removing second stage inverter.

5.1 Automatic Dead-Time Enhancement Results

Efficiency is slightly increased by automatic dead-time latch circuitry. Prior to dead time enhancement, falling edge of the gates drive pulses are almost synchronized

meaning that there is a time interval exist where both NMOS and PMOS switching MOSFETS are both switched on. This paves way to a path between supply voltage to ground causing short circuit losses. By means of the enhancement, low-to-high transition dead-time (DTLH) is achieved and measured as **2.35 ns**. In Figure 5.5, improved gate drive pulses are presented. The difference at the falling edge of the pulses are quite obvious when compared to the gate pulses demonstrated in Figure 5.4. When the dead-time is created in the falling edge of the pulses, it further improved the overall efficiency by **1.3%**. Hence, the efficiency of the proposed converter is reached to **72.3%**. Besides, switching node Vx voltage and tranformer primary side current are also presented in Figure 5.6 and Figure 5.7

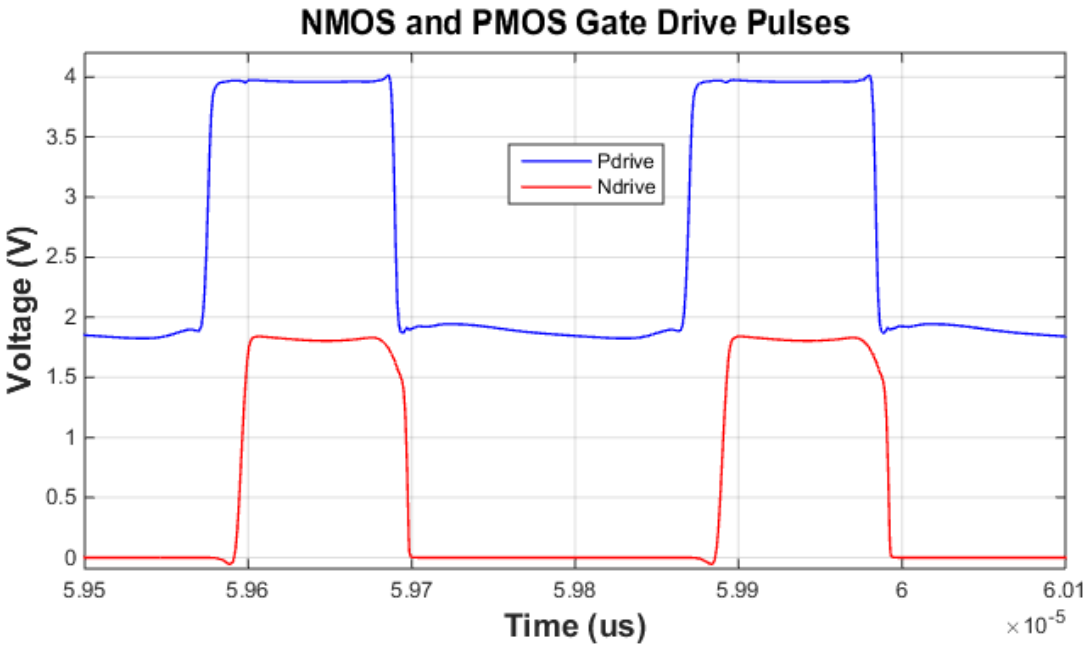

Figure 5.4 *Gate Drive Pulses without Dead-Time Enhancement*

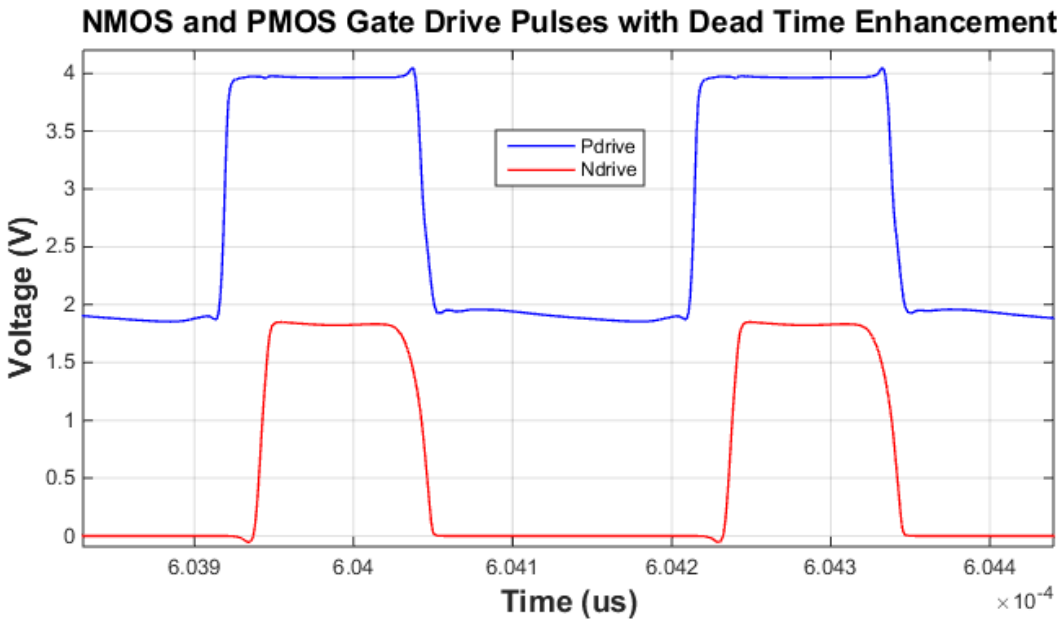

Figure 5.5 *Gate Drives with Automatic Dead-Time Enhancement*

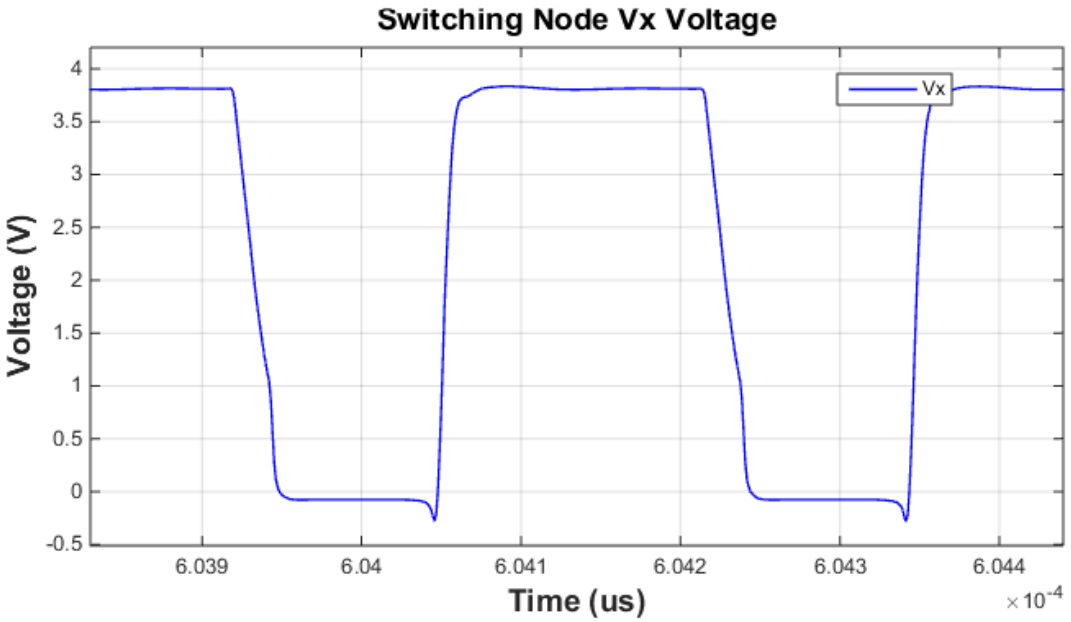

Figure 5.6 *Switching Node Vx Voltage After Dead-Time Enhancement*

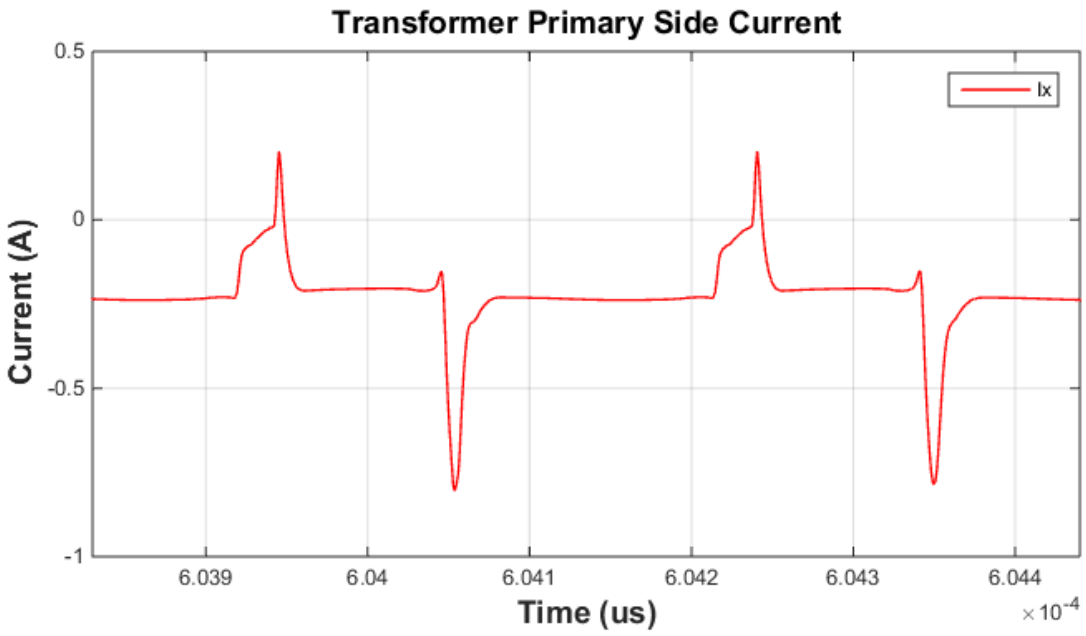

Figure 5.7 *Transformer Primary Side Current After Dead-Time Enhancement*

As can be seen form the above Figures, whenever inductor current reverses, it charges the node PFB where all the parasitic capacitances are connected. Therefore, charging time of the capacitances basically delays main PMOS switch to turn ON resulting a dead time in the falling edge which can be seen clearly in Figure 5.5.

After adding the automatic dead-time enhancement, achieved circuit specifications are tabulated in Table 5.1 and Table 5.2.

Table 5.1 *Achieved Circuit Specifications After Dead-Time Enhancement*

Supply Voltage(V)	Load (Ω)	fs (MHz)	Duty Cycle (%)	Efficiency (%)
4V	**10**	**3.4**	**58.5**	**72.3**

Table 5.2 *Achieved Output and Power Specifications After Dead-Time Enhancement*

Vout(V)	Iout (mA)	Input Power (mW)	Output Power(mW)
2.34±30 mV	**234**	**773.23**	**566.38**

6. CONCLUSION AND DISCUSSION

In this thesis, a method for driving switched mode resonant DC/DC converter in a self-oscillating manner has been presented. The proposed converter topology composes of cascoded transistors, a transformer, duty cycle detector and pulse shaping circuit. Unlike the convenient complex control techniques, commutation control signals are attained by means of an inductive feedback. Fundamental operation principle of the proposed converter is same with traditional buck (step-down) converter, however, high frequency operation required some modifications in the convenient topology. For instance, transformer in the proposed topology provides feedback signal to driver stage and delivers power to the load. As the feedback signal is inductive, its response its faster therefore it enables proposed converter to operate much higher frequencies as opposed to convenient topologies. Generally, as the operation frequencies increases, efficiency of the converter mitigates significantly especially due to switching losses in the semiconductor devices and high frequency parasitic components. Nevertheless, by means of inductive feedback it is possible obtain adaptive dead time between the gates pulses which helps to also achieve zero voltage switching (ZVS). Hence, short circuit losses are diminished and efficiency of the proposed converter is increased substantially. What is more, dead time between the gate pulses for DTLH transition enhanced and optimized with the additional dead time latch circuitry and efficiency is further improved by **1.3%**.

Owing to transformer primary side inductor and load capacitor, circuit has a resonant behavior that helps converter to sustain its self-oscillating function. Resonant frequency of this resonant load is quite close to operation frequency of the proposed converter, therefore, it justifies the name resonant self-oscillating converter. In other words, the operation frequency is mainly determined by the transformer primary side inductor and load capacitor. In connection with this, it is also understood that operation frequency is independent from the load.

SPICE simulations of the proposed converter is conducted with real SPICE models of the components which are obtained from the manufacturers' website so that the high simulation accuracy is aimed. On top of that, the compatibility of the components such as MOSFETs, transformer and other passive elements for the target frequency are meticulously investigated as presented in this thesis. Since all the component SPICE models are real, it is possible to implement this proposed circuit in printed circuit board (PCB). Furthermore, possible parasitic components that will be visible at high frequencies are modeled both at the input side and output side of the converter. Particularly, battery that is employed as supply voltage source is modeled with the parasitic elements so that the simulations are performed in a much more realistic manner. Thus, proposed converter circuit is coherent for practical implementation on PCB. Regarding this, high speed converters are mostly designed for integrated circuits where the silicon process is involved. In this case, cost of the converter increases with the silicon area. However, when the proposed converter is implemented as off chip (discreet) converter, the cost of the converter decreases dramatically. Hence, from business point of view, proposed converter is advantageous. PCB implementation and necessary technical improvements will be direction of the future work.

While the proposed topology offers high power density, reliability and low cost, it also has some downsides as well. To illustrate, the duty cycle is fixed to around 50-60%, therefore, voltage regulation is constrained by the constant duty ratio. Besides, effects of parasitic components especially at high frequencies comes into play and degrades overall efficiency of the converter. However, high frequency behavior of the all components in the circuit are inspected rather carefully and selected by the manufacturer accordingly so that the adverse effects to circuit efficiency are tried to be mitigated. Last, drawback is that as the operation frequency is mainly determined by transformer passive element, it would be difficult to find a discreet transformer which is suitable for much more high frequencies, if the much higher operation frequencies are desired. The best solution in case of absence of such discreet transformers in the market, is to a designing a transformer based on the circuit speed specification. An air core transformer design would be beneficial in terms of circuit efficiency since air core transformer does not exhibit undesired characteristics of ferromagnetic material such as eddy current and hysteresis. Such losses become significantly important when high frequencies are aimed.

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