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VCO STRAT-UP AND STABILITY ANALYSIS USING TIME-VARYING ROOT LOCUS

Master of Science thesis

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ABSTRACT

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The oscillator circuit is one of the key components of the communication systems. It is necessary for an oscillator to provide the proper oscillations in order to confirm the stable operation of a communication circuit. There are many different analysis methods of analyzing the start-up and frequency stability of a system, but mostly it fails to analyze properly due to the parasitics involved. Somehow if any of them manages to compute the analysis it would be very complex, difficult and time consuming.

The time varying root locus (TVRL) approach can be utilized to analyze the start-up and frequency behavior of different oscillator designs. It is a theoretical based technique that can provide further insights into a circuit designer for oscillator operation. To analyze the start-up behavior, a semi-symbolic TVRL approach can be used with the help of the numerical QZ (Generalized Schur Decomposition) algorithm. By finding the time varying roots of polynomials, TVRL can help to estimate the undesired operating points. A symbolic TVRL analysis is capable of computing the system roots during an oscillation with the help of Muller algorithm.

Different numerical and the CAD (Computer Aided Design) tool are involved to implement this theoretical approach. Cadence 45nm CMOS General Process Design Kit (GPDK) helps to design the required schematic and SpectreRF simulator computes the time varying periodic solutions. Maple script can form an admittance matrix which is later used in MATALB to compute the final TVRL trajectories of dominant poles. The corresponding results are then analyzed to detect the failure mechanism which is responsible for relaxation oscillations.

In this thesis, an active inductor quadrature voltage controlled oscillator and five stage ring oscillator circuits are proposed to analyze thoroughly with the help of TVRL approach. The above mentioned techniques along with some extra computations have been implemented to verify whether the proposed circuits can overcome the relaxation oscillations and can produce the proper sinusoidal waveforms or there is a need to devise some modifications.

PREFACE

The Master thesis “VCO start-up and stability analysis using time-varying root locus” is performed to fulfill the requirements for M.Sc. in Electrical Engineering. The work was done at RFIC Laboratory, Department of Electronics and Communication Engineering, Tampere University of Technology (TUT) under the supervision of Prof. Nikolay T. Tchamov.

During my working tenure I have got a lot of moral and intellectual help from my supervisor and the colleagues in our work group. Especially I would like to thanks Prof. Nikolay T. Tchamov for allowing me to work in his research group. I would also like to thank my immediate advisors Jani Järvenhara, Sanjeev Jain and Rahman Akbar for their kind help for ambiguities and issues under different circumstances.

Finally I would like to pay special thanks to my elders, friends, Muhammad Rizwan and Fatima Syed, who helped me to stay motivated and well-focused during my whole study period.

Tampere, April 2016

Aneeb Sohail

CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

LC	Inductor Capacitor
CAD	Computer Aided Design
VCO	Voltage Controlled Oscillator
LHP	Left Half Plane
RHP	Right Half Plane
GPDK	Generic Process Design Kit
QZ	Generalized Schur Decomposition
LO	Local Oscillator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SBG	Simplification Before Generation
SDG	Simplification During Generation
SAG	Simplification After Generation
IC	Integrated Circuit
MNA	Modified Nodal Analysis
MOR	Model Order Reduction
CMOS	Complementary Metal Oxide Semiconductor

1. INTRODUCTION

The pole-zero analysis of a network transfer function in a feedback system reveals that an unwanted phenomenon prevails during its operation [10], [23]. It is commonly known as relaxation oscillations. It is the failure mechanism which is not really easy to detect with the help of transient simulations while generating the sinusoidal oscillations [14]. If somehow a transient simulation method is devised which can detect this problem efficiently, it would be very complex, difficult and time consuming. So further enhancements, in large swing voltage oscillator requires some simple and less time consuming analysis structure in order to detect the problem accurately.

A time varying methodology mentioned in [4], depends upon impulse sensitivity functions involves some considerable simulations or some analytical derivations based on circuit design [24]. A theory demonstrated in [9], called the perturbation projection vector. Another topology depends upon fundamental large signal physical aspect is developed in [7]. A root locus strategy is used to analyze the oscillator star-up conditions [10], hence further used for the oscillators having multiple frequency oscillations [25]. Usually these types of oscillators have high-order resonance tanks. The root-locus methodology is used to compute the instability analysis of delta sigma modulators [28]. Along with this it is also used to analyze different parameters of multivibrators such as switching time [27] and sinusoidal operations [26]. So the same time varying technique has been modified to analyze the start-up and stability of different VCO structures.

In this thesis, the steady-state analysis of a large signal voltage controlled and a ring oscillator has been conducted with the help of the semi-symbolic CAD algorithm [14]. To compute the start-up behavior of oscillators a semi-symbolic TVRL analysis is utilized with the help of the numerical QZ algorithm [1]. To compute deflating the subspaces of matrix pairs and compute the generalized eigenvalues QZ algorithm is widely used. There are three major factors with makes it a successful algorithm [22].

a) The reduction of the matrix pair into Hessenberg-triangular form.
b) To preserve Hessenberg-triangular form, implicit shift QZ iteration is implemented.
c) To split up the calculations of generalized Schur form, a deflation process is applied.

To reveal some important information about some unwanted operating points of nonlinear circuits, the periodic time varying roots of the characteristic polynomial has been determined [17]. The roots for the single oscillation period are computed by using

TVRL analysis along with Muller Algorithm. The steady state time domain periodic solutions computed through SpetreRF simulator and their trajectories of relevant roots have been analyzed [21].

The TVRL structure has been implemented in such a way that first the schematic of desired circuitry has been inserted into a CAD tool which can compute the different analysis with respect to that circuit. Such as DC operating points, transient analysis, pole-zero computation and pss analysis. Another computing tool is used to create an admittance matrix to implement the QZ algorithm. Finally, all computed results are cumulated with the help of MATLAB and presented in the graphical form. Later on the obtained results will help to reveal the operating conditions for proposed circuitry.

The background research which includes the basic theory about oscillators and basicity of some analysis techniques such as semi symbolic analysis and periodic steady state analysis have been described in Chapter 2. Chapter 3 will reveal a concise description about TVRL analysis for specific circuit design and how it being implemented. In Chapter 4 the start-up and frequency analysis of Quadrature voltage controlled oscillator has been discussed in detail. The analysis of ring oscillator is depicted in Chapter 5. In end, the last chapter concludes the thesis.

2. BACKGROUND

2.1 Oscillator history and design aspects

The first oscillator design was made by using electromagnetic coupling technique among inputs and outputs (vacuum tubes). With the help of close coupling along with output and enough energy is produced for input circuitry in order to provide proper oscillations. Eventually, the oscillation frequency equalizes to the resonant frequency of LC (inductor capacitor) oscillator. It also prevails some of the little parasitics.

Generally, oscillator is an electronic circuit that uses DC supply as an input and produces a periodic waveform as an output. The resulted waveform can be a square, sinusoidal, triangular or sawtooth wave depending upon its construction and requirement. Fig. 1 shows the basic concept of oscillator. It can be noticed that oscillators are widely used to design transmitters and receivers. The main purpose to use an oscillator is to drive the mixer by providing periodic signals.

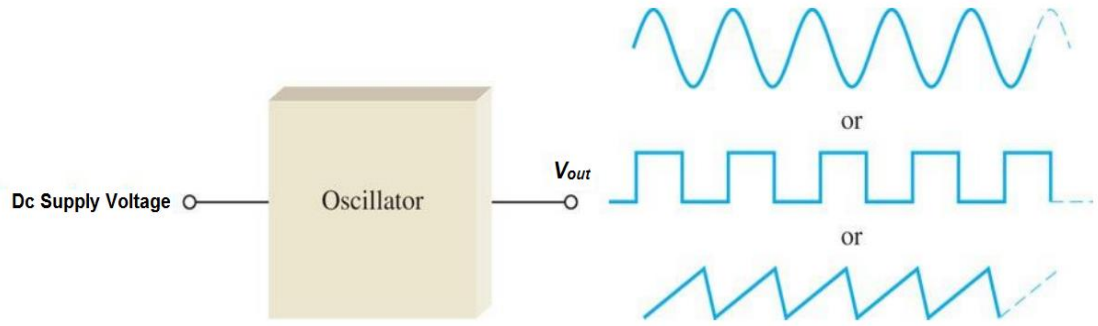

Figure 1: *Basic concept of oscillator with possible output waveform.*

Usually there are two types of oscillator circuits:

1. Feedback Oscillators:

   An oscillator circuit that provides some fractions of output signal along with input keeping the phase to its original value. The main idea behind this is to reinforce the output swing. Final design includes a feedback circuitry and a gain amplifier as shown in Fig. 2.

2. Relaxation Oscillators:

Second kind of oscillator is the relaxation oscillator, so this topology uses RC circuit to produce a typical non-sinusoidal waveform such as triangular or square waves. Fig. 3 shows a basic relaxation oscillator.

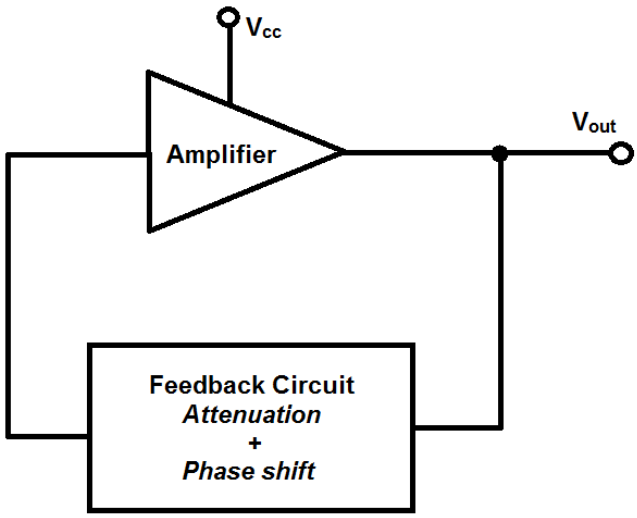

Figure 2: *Basic feedback Oscillator.*

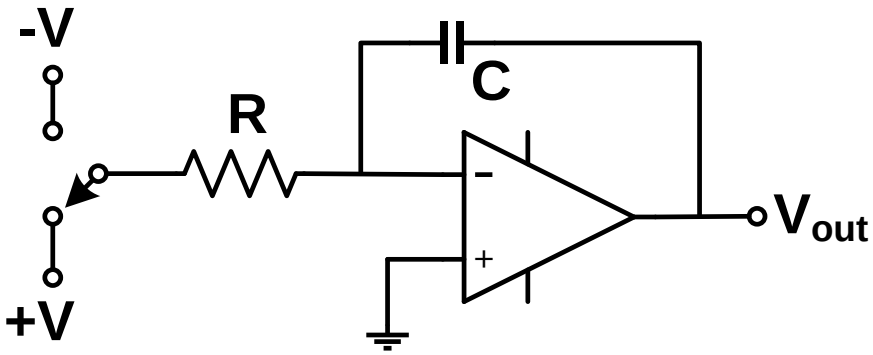

Figure 3: *Basic relaxation oscillator.*

Oscillator operation and design

To design an efficient oscillator for RF circuits it must satisfy some specifications and parameters that must be taken care to fulfill the requirement [15].

Frequency: While designing a RF oscillator it must be taking into account that its operating frequency must be able to variate according to requirements.

Output Voltage: As it already discussed earlier that the main functionality of RF oscillators is to drive dividers and mixers, so an oscillator must be capable of producing such big output swings to satisfy the proper switching of MOS transistors.

Drive capability: An oscillator must be efficient enough to drive capacitance with maximum load in order to control the "frequency synthesizer" efficiently.

Phase noise: It is a major phenomenon occurs in oscillators when its output diverts from an impulse and broadened to create a noise. It directly affects the tuning range and power dissipation of the oscillator.

Square wave output: In an optimum oscillator the output waveform must be a square wave but practically it is very difficult for a local oscillator to generate accurate square wave due to harmonic attenuation. This attenuation occurs because of the circuit itself and resonant load buffer.

Smoother supply: For an efficient LO (Local Oscillator) the supply voltage must be constant because it can heavily affect the operating frequency of oscillator. This happens due to a phenomenon called flicker noise of voltage regulator which can change the oscillation frequency. Fig. 6 shows the effect of flicker noise [15].

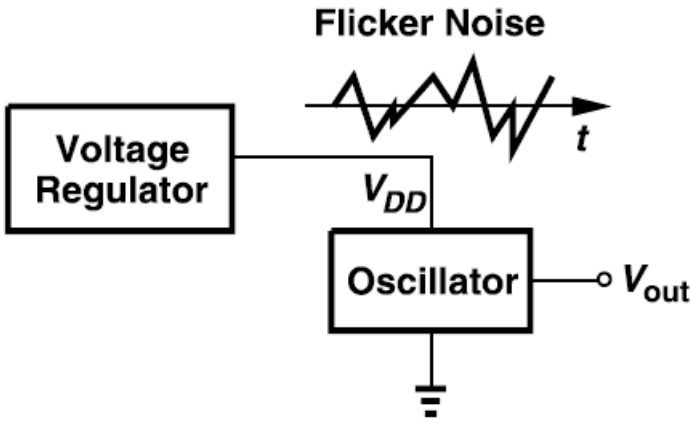

Figure 4: *Flicker noise on an oscillator.*

Power Dissipation: It is very crucial for an oscillator to consume low power because it directly affects the tuning range and phase noise. Therefore some of the techniques have been introduced, which lessens the phase noise in respect to applied power.

Voltage controlled oscillator

As discussed earlier, for the proper operation of an oscillator it is necessary to setup its frequency in a certain range. To accomplish this we prefer to tune the frequency range of an oscillator by using an electronic circuit, so Voltage Controlled Oscillators (VCOs)

have been introduced. Fig. 5 below shows the basic concept of its working principle [15].

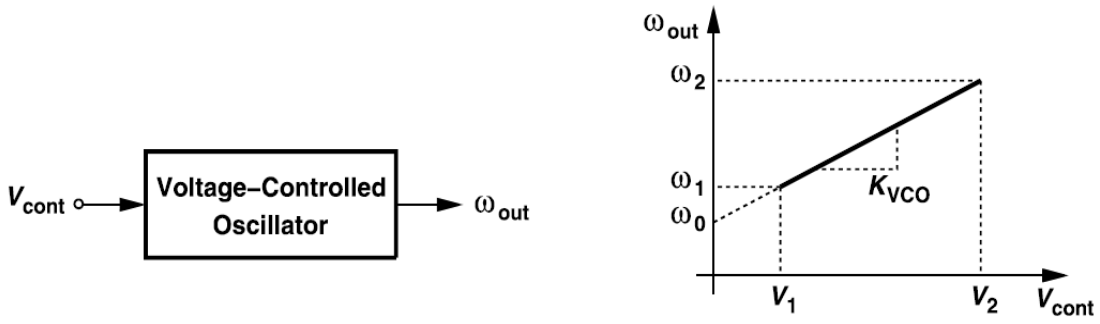

Figure 5: *Characteristics of a VCO.*

When control voltage, V_{cont}, changes from V_1 to V_2, the resultant frequency goes from ω_1 to ω_2. Hence the output slope can be denoted as K_{VCO} and commonly known as the gain of VCO. The gain can be expressed as rad/V/Hz [15].

$$\omega_{out} = K_{VCO}V_{cont} + \omega_0 \qquad (2.1)$$

In this equation, ω_0 represents the point of interception of K_{VCO} slope at Y-axis.

To change LC oscillator frequency, it is necessary to change the resonance frequency of LC tank. For this purpose we design our circuit to change the capacitance through varactor because it is not possible to electronically change inductance. Fig. 6 shows the circuit diagram of basic VCO devised by Razavi in his book. According to this circuit M_{V1} and M_{V2} are parallaly attached to tanks. Source/drain are connected to V_{cont} and the gates are connected to the *X* and *Y* terminals of Oscillator nodes. On operation the capacitance of M_{V1} and M_{V2} will reduce as V_{cont} will reach from zero to V_{DD} and the gate source voltage will remain positive. The circuit will show the same nature to the existence of even large voltage swings across M_{V1} and M_{V2} and at *X, Y* nodes. As the value of V_{cont} increases to V_{DD} the *average* voltage across varactor reduces to zero, hence establishes a monotonic reduction in their capacitance. The expression for oscillation frequency will be:

$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_1+C_{var})}} \qquad (2.2)$$

In this expression, C_{var} represents the average varactor capacitance and C_1 is introduced to increase the tuning range else the varactor frequency can change widely. Perhaps C_1 replaces the need for important capacitances like: (1) the gate, source and drain capacitances of M_1 and M_2, (2) inductor parasitic capacitance, (3) the capacitance of transceiver design circuitry attached ahead.

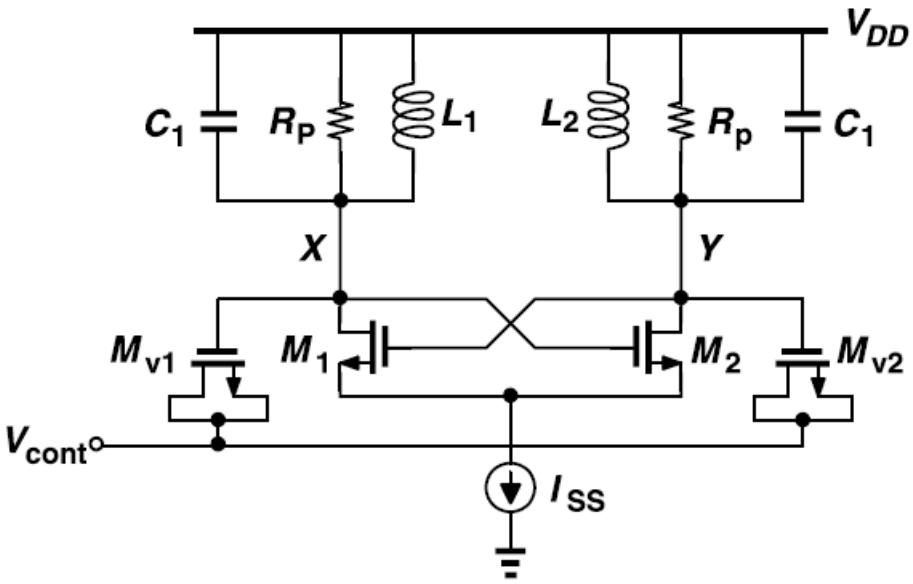

Figure 6: *VCO using MOS varactor.*

Although cross coupled voltage control oscillator is one of the prosperous topologies still they experience a problem of small tuning range. The three factors which influence the change in varactor capacitance are already discussed earlier; hence C_{var} turns out as a small capacitance in front of total capacitance. So if the total change in average varactor capacitance is about 20% of the total capacitance then VCO tuning range will be about ±5% around center frequency. Due to this reason the overall *Q* of varactor is reduced with the help of resistive loss.

2.2 Steady state and start-up conditions

Fig. 7 shows a common feedback oscillator circuit which is a two-port network with the combination of a feedback linear and forward nonlinear circuit. For steady state analyses of forward feedback oscillator, let us consider a *Barkhausen criterion* equation [18].

$$T(V_{in}, \omega) = A(V_{in}, j\omega)\beta(j\omega) = 1 \qquad (2.3)$$

Hence the equation represents unity complex loop gain. Where the feedback and forward transfer functions are represented by β and A respectively.

It is a methodology where the periodic steady state (pss) analysis is computed with the help of either time domain (shooting) or frequency domain (harmonic balance) computational strategies. It is independent of the time constraints of circuit. By using pss analysis, the circuit operating points can also be found which is later useful to compute TVRL analysis. Usually harmonic balance is used to analyze the circuits with frequency dependent such as S-parameter, delay and transmission line and linear circuitry. On the other hand shooting is used for nonlinear circuits with sharp rising and falling signals.

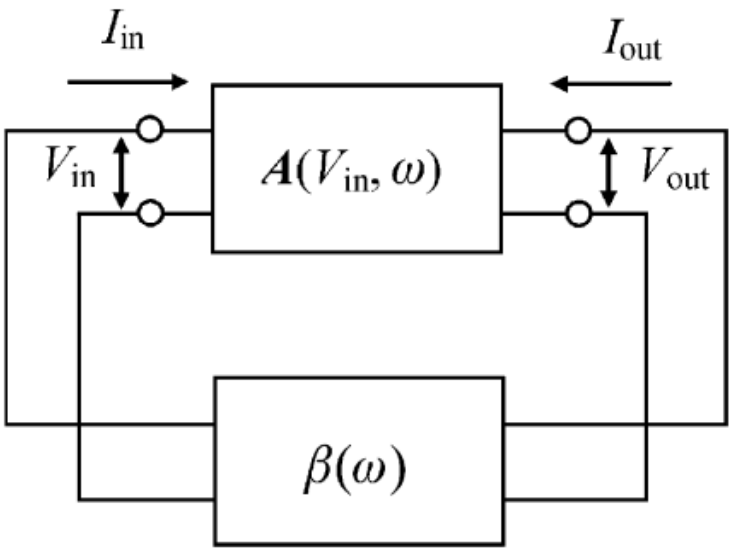

Figure 7: *Parallel feedback oscillator.*

For both of the autonomous circuits (non-driven) such as oscillators and non-autonomous circuits (driven) such as mixers filters and amplifiers, the pss analysis is equally suitable. In the case of oscillators (autonomous circuits) two nodes *p* and *n* are specified in the parameters, hence the pss can determine the circuit type; else pss takes it as a non-autonomous circuit. So for driven circuits pss requires an integer multiple of signal period as a *period* and the fundamental frequency related to the circuit. But for non-driven circuit exact oscillation period is unknown so the user can provide estimated oscillation period and the pss simulation calculates it automatically with the help of periodic solution waveforms [20].

It is a time-domain, iterative methodology. In shooting method the initial conditions for startup are estimated and later on the simulation computes the exact initial condition which helps to conclude the steady state solution. In this method after a period if the final stage results an initial stage of non-linear function, then some iterations become mandatory. Usually during simulation of non-linear behavior of circuit, approximately five iterations are required within the shooting interval.

Nowadays shooting engine yields more accurate results for nonlinear circuits with the help of a new Fourier integral approach (computes Fourier analysis) is introduced by *Cadence.* With this approach shooting method can easily meet the efficiency of Harmonic balance [21].

There are total two phases involved in pss analysis [21]:

1. Initial transient phase

   It provides the basic structure for required steady state solution so the circuit can be directed to a particular solution rather than the undesired one. Initial transit analysis also wipes out the large and fast decaying

modes of a circuit to yield the convergence. During this phase, the simulation starts with initial time usually 0 and continues through the onset of periodicity. It represents the minimum time when all sources are periodic. Then the oscillation stabilization time is maintained. The third step of 1st phase represents the period of both driven and non-driven circuits.

2. Shooting phase

   Then the periodic steady state simulation enters the second phase where the circuit is solved iteratively with the help of Newton method of finding the final pss solution. The circuit simulates with repetition and adjusts the initial condition to compute pss solution. To find out initial condition accurately the initial state of circuit must match with the final state. Then the maximum mismatch is found out with the help of transient analysis and if the convergence benchmark is not met then the initial condition estimation is done again to improve accuracy. The process goes on until simulation converges. Frequency domain response can also be computed later if needed.

The harmonic balance or shooting must be started at proper time interval to attain the maximum conveyance. Because starting at bad interval can slow the analysis and stop the convergence. It is least favorable to start harmonic balance or shooting while the circuit is showing extreme non-linear behavior. To simulate pss analysis of an oscillator linear or transient initialization is used to initially guess the oscillation frequency and steady state solution. To start oscillator it is necessary to kick off with initial conditions else some impulse stimulus can be provided. For the initial conditions parameters of components related to oscillator resonator are needed and if stimulus is used then it should be strongly coupled to an oscillator mode of circuit.

One of the first phase noise estimation methods was devised by D.B Leeson in 1966, in which he derived an equation to approximate the phase noise of an oscillator depending upon its critical specifications such as noise contribution (F), signal power (P_s), and Q-Factor of resonator [3]. Hence the most common derived expression of the oscillator phase noise $\mathcal{L}$ according to the Lessons model is [4].

$$\mathcal{L}\{\Delta\omega\} = 10\log_{10}\left(\frac{2F.kT}{P_s}.\left(\frac{\omega_o}{2Q.\Delta\omega}\right)^2\right) \qquad (2.4)$$

Where F denotes noise factor, k is Boltzmann constant, T is absolute temperature, ω_o is oscillation frequency, Q is effective quality factor of resonator tank, and $\Delta\omega$ can be expressed as offset from the carrier [5].

Another method depends upon impulse noise injection during various oscillations is known as impulse-sensitivity function [4]. It can be determined in both ways either ana-

lytically or numerically using three different approaches, but the numerical approach is considered as the best suitable approach as it has more accuracy then rest and computed by using Dirac impulse during the particular instants of time [1]. It can also be said that this approach lies between both CAD and design oriented topologies as it relies upon the circuit simulations therefore it utilizes much time in comparison to other techniques. Mostly impulse-sensitivity function method is used to differentiate the noise performance of Colpitts and cross coupled oscillators. The numerical approach also lessens the implementation of ISF due to less information on noise structure in oscillator.

Emad Hegazi and his research group also derived a popular topology to analyze the phase noise of an oscillator is known as mechanistic physical model. It is categorized as design oriented topology because it only provided the understanding about a circuit but not the accurate numerical analysis. This method utilizes some parameters to design the circuit and determines the phase noise of an oscillator by devising some basic expressions. Mechanistic physical model is a large signal time varying methodology. It is capable of dealing with the results that are not visible by simple linear analysis. The core cause for the success of this method is the disintegration of certain noises into amplitude and phase modulation. So this method can detect different fundamental noises in LC oscillator [7].

PPV (Perturbation projection vector) is a numerical methodology to analysis the phase noise of an oscillator. It is purely a CAD oriented methodology formulated on Floquent theory. It was originally developed by Franz Kärtner [8], but readily embraced after the further modifications done by Demir [9], such as decreasing the computational processing time and driving simple and easy analyzing methods. This method works in way that during every period it creates a cyclic limit, hence noise perturbations at specific time tends to change the position of its operating points to its neighbors of cyclic limit [1].

2.3 Symbolic Analysis

To gain the information regarding analog circuits analytically a systematic methodology is used known as symbolic analysis. In mid of 19^{th} century electronic computer came into introduction and the need for symbolic analysis rose when they were used for circuit analysis. The first computer programs were designed to compute different network equations with the help of matrices and to develop some basic CAD designs. Among them the most common development was the nodal analysis which is still applicable in the present world analysis in the form of *Spice.*

By the time various methods were introduced to solve the complex circuit problems but out of them these three are the most popular techniques which can efficiently reduce the final symbolic expression [19].

1. Simplification Before the Generation (SBG)

   As depicted by name the simplification is done while modeling the circuit with the help of matrices and graphical representation in form of circuit equations. The main target behind this method is to attain the simple symbolic results by using easy to solve matrices and graphs or circuit model. This methodology can be applied to the expanded network functions as mentioned in [19].

$$H(s,x) = \frac{\sum_{j=1}^{m} s^j f_j(x)}{\sum_{i=1}^{n} s^i g_i(x)} \qquad (2.5)$$

   The SBG technique cannot properly govern the accumulation error. Hence huge pole/zero displacement, magnitude and phase error can be resulted.

2. Simplification During Generation (SDG)

   This type of simplification can be done while processing the solution of circuit equation. The main target in this technique is to create only the important part of symbolic expression. Eventually, the final results are somehow compromised as symbolic terms are not used. It can be applied directly on equitant circuit, graph or matrix in the form of network equation. SDG helps to simplify the resulting equations and models the circuit response efficiently with the error margin limiting to specific frequency range.

3. Simplification After Generation (SAG)

   Simplification after generation needs older circuit analysis and equation results therefore it is directly implied on symbolic solutions.

In present analysis techniques there are two types of approaches which are commonly followed: one includes approximation, and the other one uses hierarchical decompositions. In approximation, least important symbolic terms are removed from the computation depending upon the model parameters and frequency [19]. The hierarchical method creates the symbolic terms in nested form [19]. To attain transfer function a sequence expression concept is followed. Mentioned below are the three different approaches to implement the above algorithms under discussion.

2.4 Matrix based approach

This approach uses nodal admittance matrix method to create the circuit equation and applied through SBG method.

$$\boldsymbol{YV} = \boldsymbol{I} \qquad (2.6)$$

For this technique, a row and column operation is implemented to minimize the non-zero elements and amount of symbols in the circuit, hence the dimensions of matrix are minimized with no non zero element keeping the determinant value constant. During the analysis, approximations can only be done to a certain range of frequency and to analyze with high frequency range capacitors should be included to admittance matrix. The error produced in determinants due to denominator and numerator can be handled but it cannot handle the errors due to network transfer function.

Forming admittance matrix

An admittance matrix of any circuit design can be formed with the help of Kirchhoff's circuit laws. It is mostly applicable when a complex circuit is needed to optimized, usually it requires computer simulations. To create an admittance matrix with the help of nodal analysis let us consider a basic electronic circuit shown in Fig. 8, which includes some passive components along with a power source [6].

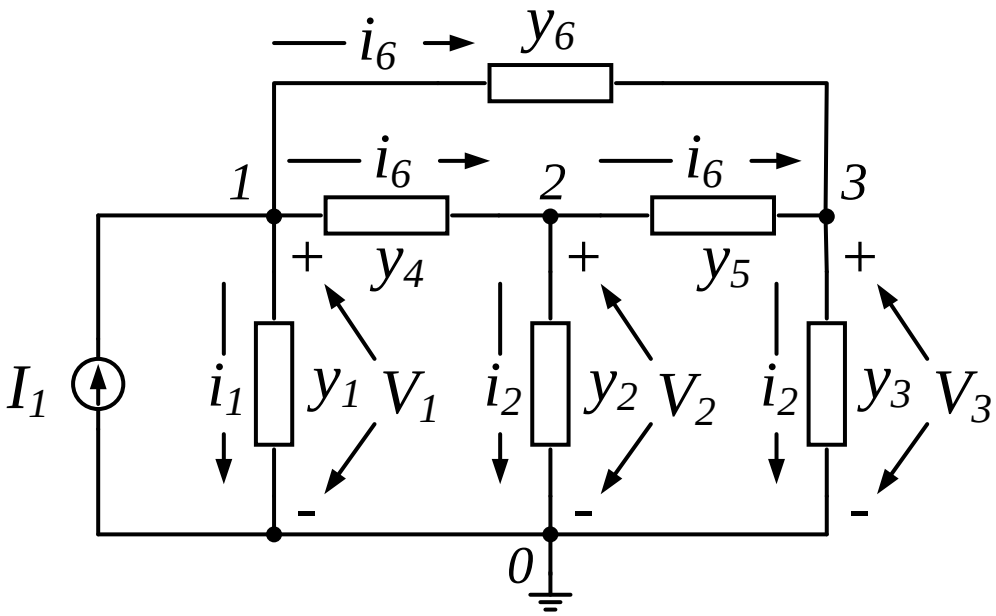

Figure 8: *Basic circuit design to create an admittance matrix.*

First of all select a reference node and then write down the KCL equations corresponding to the unknown node voltages in the whole circuit. For above mention circuit there are total three nodes, hence the equations will be.

$$\text{Node 1:} \quad V_1(y_1 + y_4 + y_6) - V_2 y_4 - V_3 y_6 = I_1$$

$$\text{Node 2:} \quad -V_1 y_4 + V_2(y_4 + y_2 + y_5) - V_3 y_5 = 0$$

$$\text{Node 3:}\quad -V_1 y_6 - V_2 y_5 + V_3(y_6 + y_5 + y_3) = 0$$

Once the equations are created, they can be inserted into the matrix as shown in equation 2.6, mentioned in the previous section. In that *Y* represents the admittance matrix. *V* represents the voltages vector between each node and the reference node. *I* represent the independent current source vector in the circuit. Now the final matrix would have each node equation in one row corresponding to the number of node in another matrix. If, the total numbers of nodes in a circuit are *M* then the size of *Y* matrix will be *M*M*. The size of remaining *V* and *I* matrices will be *M*1*. Hence the admittance matrix for above equation will be.

$$\begin{bmatrix} y_1 + y_4 + y_6 & -y_4 & -y_6 \\ -y_4 & y_4 + y_2 + y_5 & -y_5 \\ -y_6 & -y_5 & y_6 + y_5 + y_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_1 \\ 0 \\ 0 \end{bmatrix} \qquad (2.7)$$

The placement of components in the *Y* matrix will be in such a way that each of the cell y_{ii} connected diagonally will have the sum of all branches attached to node i. As we know the matrix will be symmetrical so the remaining non diagonal elements ($y_{ij} = y_{ji}$) will be the sum of all admittances connected between the nodes i and j, with a negative sign. The resultant matrix will be in such a way that all diagonal points will be positive else all are negative. Fig. 9 explains the formation of admittance matrix discussed above.

The designed circuit can also have a controlled power source along with an independent one as shown in Fig. 10, and then the equation for admittance matrix can be written as.

$$\boldsymbol{Y_p V = I_1 + I_2} \qquad (2.8)$$

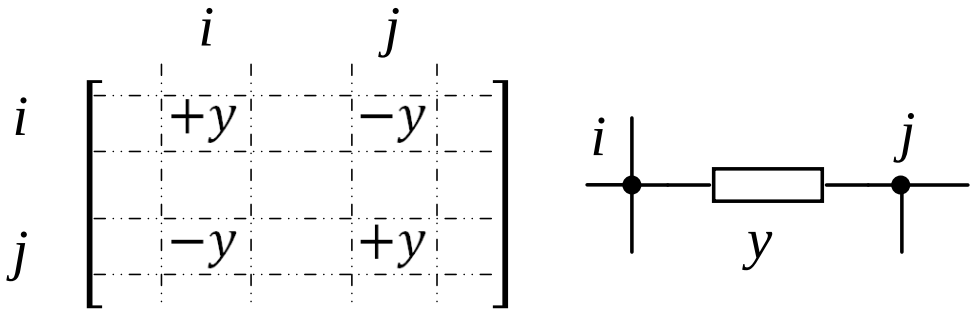

Figure 9: *Formation of admittance matrix.*

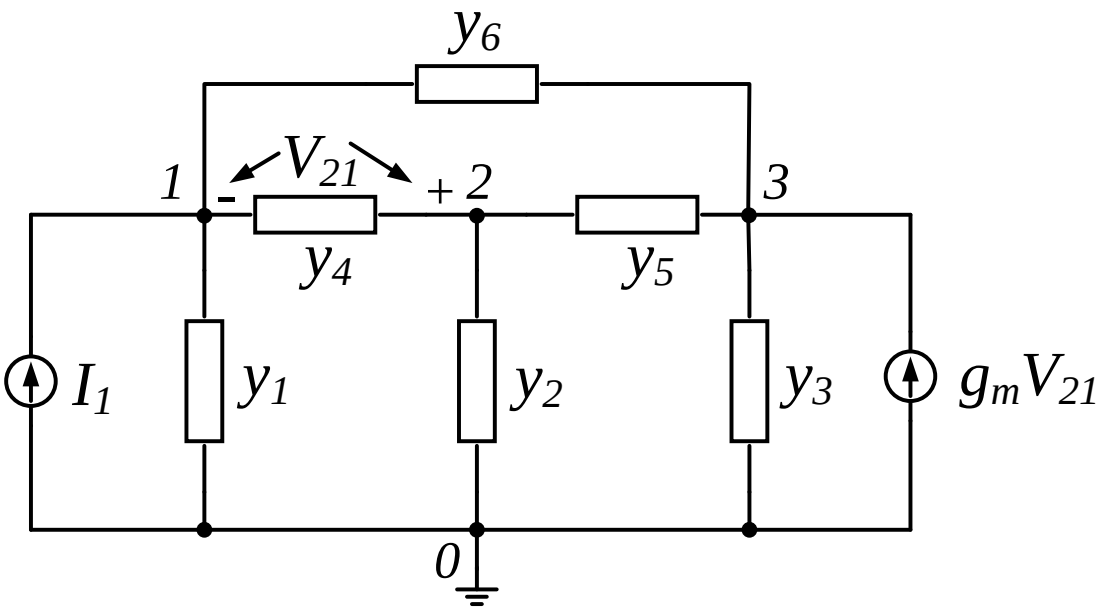

Figure 10: *Circuit with controlled current source.*

Where I_1 represents the vector with independent current source and I_2 represents the vector of controlled current source. On the other hand transconductance (gm) is also added in added in *Y* matrix. It is added in four places y_{ip}, y_{iq}, y_{jp}, y_{jq} in a way that i and j are the nodes where controlled source is connected and, p and q are the nodes connected to the controlling voltage. The sign will depend upon the polarity of controlled voltage and current direction. Fig. 11 shows the formation of admittance matrix along with controlled sources.

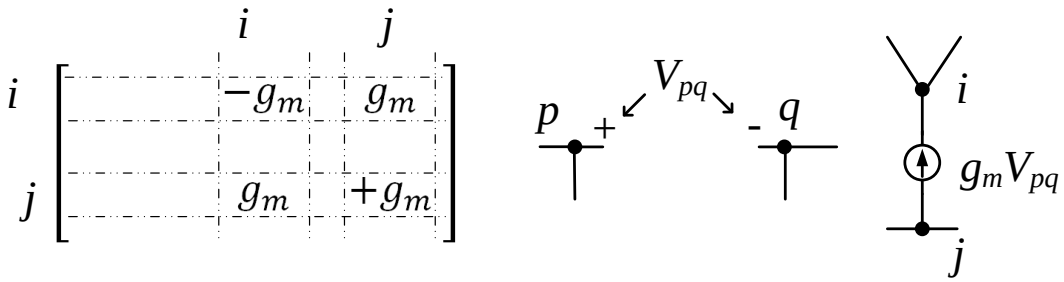

Figure 11: *Formation of admittance matrix with controlled sources.*

2.5 Graph based approach

There are two basic graphical approaches to implement SBG. Usually the first technique the current and voltage graphs are prepared for denominator and numerator of the network transfer function. Then the simple and complementary contribution from every device is computed. It is done to collect the frequency samples and if the samples are strong enough then they will be included in further graphs for terminal node contraction

else all the weak frequency samples are discarded. Meanwhile other contributions are also computed and if there is some deviation from its required value then the discarding process is stopped. By deleting the elements with some error value the graph is further simplified.

In the second approach signal the flow graphs of node current and node voltages are prepared and simplified with the help of network model transformations [19].

a) Removing congruent branches among two nodes (meta-edge) of summing vertex.
b) Removing meta-edge which does not belong to signal path.
c) Short circuit the current and voltage vertices connected to respective nodes.
d) Restoration of one part of graph with the help of some other graph keeping the same network graph connectivity.

2.6 Circuit based approach

In this method, the analysis is done directly on the basis of circuit. The components which do not contribute to network function with no impedance and admittance [19].

a) To implement this approach first to find out the contribution by contracted terminal nodes of all devices to network function and create a list.
b) Then find out the least important contraction and calculate error.
c) Now check the error value if it exceeds required value, do node contractions, take away the devices attached to those nodes and update the contraction list and repeat the previous step, else continue.
d) Then again check the contribution by removing every branch separately and create another list. Repeat step (b).
e) Now check the error value if it exceeds required value, remove branches and update the list and move to previous step, else stop further computations.

2.7 Comparison between these approaches

As mentioned earlier, removing one, two or four matrix rows or columns are done in matrix based approach. So if the removal is done at four positions it will result in the same as a complete branch removal in other two techniques, still it does not show any correspondence between each other. That is why the complications in results after SBG implementation might differ depending upon the circuit itself. On the other hand removal of one or two entries can help to simplify the results but it reduces the efficiency in analysis results and can be implemented perfectly on the circuit with less components.

Another deficiency in matrix approach is that the SDG approach must be implemented after SBG. But the effective algorithms of SDG use the graph based approach; therefore it cannot be used with the results of matrix based SBG methodology. Finally, it can be said that although the results in circuit based approach can be more complicated because of combined deletion operation on denominator and nominator, but still it provides two advantages over other methods. 1) While simplifying the results the components and nodes are directly involved, 2) There is no need to draw graphs and matrices [19].

2.8 Active devices behavioral modeling

To accomplish a project, its modeling is its most important phase. This is the reason *Spice* simulator is one of the most famous tool to design transistor at IC (Integrated Circuit) level. From its start to this level, a lot of modifications have been made to improve the circuit design and simulation accuracy. Nullor element has proved itself as the key part of analog circuit design as it helps to develop the accurate operational amplifier design and synthesis. This technique can efficiently express the voltage controlled oscillators. Pole-zero extraction is one of the useful modeling techniques, this is the reason it is widely used as the topic of interest for many researches in the world.

MOS small-signal modeling

Usually, MOS transistors are used in analog circuits, there is need to simplify the *gain* and *impedances* calculation and it can be done with the help of small-signal model. For this purpose a basic MOS transistor circuit is considered as shown in Fig. 12. It has two bias voltages V_{GS} and V_{DD} which will produce the drain current I_D. When the series small signal input v_i is given along with V_{GS}, it will create a little change in the drain current i_d. So the total drain current would be $I_d = (I_D + i_d)$ and device can operate in saturation or in active region [30].

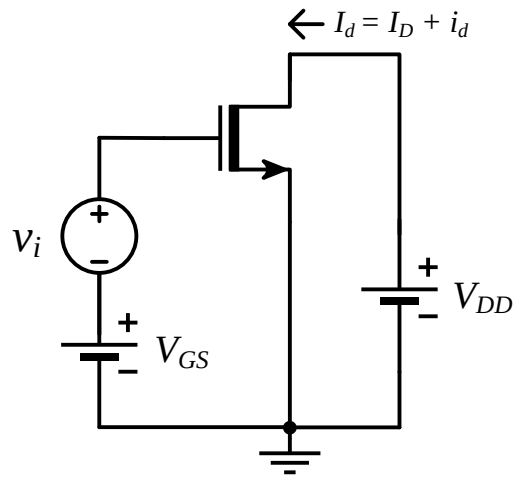

Figure 12: *Proposed NMOS circuit for small signal model.*

In case of MOS transistors the transconductance mainly depends upon the device structure and its value is the square root of bias current. MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) have a bit higher transconductance with respect to bipolar transistors in ratio to the applied current which causes a bit challenging situation to keep the lower transconductance for high quality analog circuits. The total gate capacitance of transistor is $C_{ox}WL$, which is intrinsic to its operation and controls the channel conductance of gate.

In case of MOS transistors, the input resistance is usually infinite for a small amount of gate current during low frequency operation as its channel is insulated with a dielectric. Due to this reason MOS is a useful device for different amplifier circuits. A phenomenon known as channel-length modulation increases the drain current, when there is an increase in drain to source voltage. Equation 2.10 represents the small signal output resistance mentioned in [30], where λ is the parameter of channel-length modulation.

$$\frac{\Delta V_{DS}}{\Delta I_D} = \frac{V_A}{I_D} = \frac{I}{\lambda I_D} = r_o \qquad (2.9)$$

The small signal model of above mentioned circuit is given in Fig. 13. This model shows an NMOS in active or saturation region. The current travelling from drain to source increases when the gate-source voltage rises, which will eventually increase the conductivity of channel. This small signal model is also applicable to p-channel devices. The voltage between gate and source affects the vertical electrical field, which controls the drain current and conductivity of channel. But when the voltage between the gate and source is fixed, the voltage from body to source deviates the threshold and eventually changes the drain current. This phenomenon arises due to the substrate act as second gate and call as the body effect.

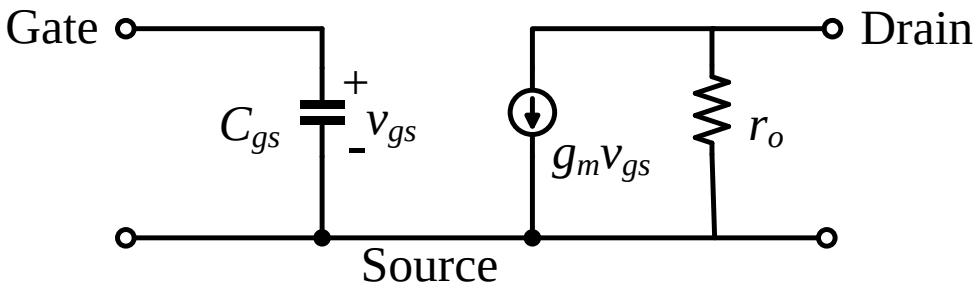

Figure 13: *Small signal model of proposed circuit.*

2.9 Modified nodal analysis

Modified nodal analysis (MNA) technique is widely used in analog circuitry to formulate the systems of equations. Though MNA creates the larger system equations and is

effectively applicable on complex circuitry but still it is very useful to implement this algorithm through computer. In this method, an equation is created for each node and then it is augmenting with the equation of each voltage source. To implement the MNA the elements of circuit are divided into two groups, one includes the elements with admittance description and second without admittance description and current needed to be solved. So the admittance matrix for group one is formed in the same way as before. But for second group, the size of matrix is increased by one row due to addition of new components and by one column due to the current flowing through these components [29]. Fig. 14 shows the basic structure of MNA matrix.

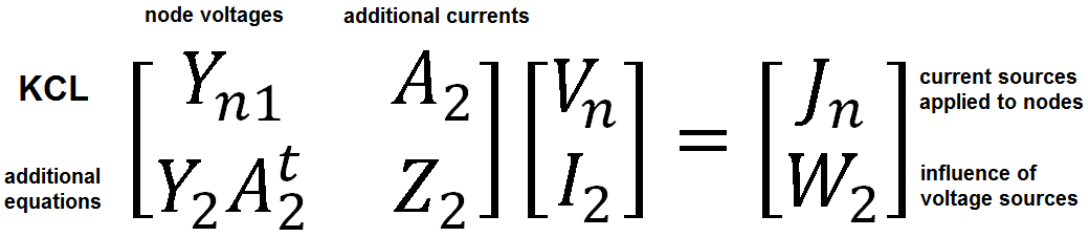

Figure 14: *MNA matrix formation.*

Model reduction

The methodology used to reduce of build compact circuit model is known as Model Order Reduction (MOR) [19]. It is a pure mathematical methodology in which only frequency is kept as a symbol. This technique uses different reduction methods.

1. The most popular technique used for MOR is moment-matching approach or Krylov subspace as it is one of the most efficient method. In this technique, a constant matching is done during projection framework. To confirm that either the simulations are stable or not the passivity of MNA methodology is kept constant.
2. Another approach is called balanced truncation where is able to deduce large scale circuits to even compact and small models. But this technique is too expensive to implement directly on the circuit. As it consumes a great effort to create numerical methods and conclude control theory.
3. With the help of local node rejection another technique is designed known as node based elimination. It is one of the closest techniques to the basic symbolic analysis. This is an easy technique as complexity contraction is done locally and no complete results for whole circuitry is needed.
4. A technique in which all devices are considered variable parameters and their successive nodes creates new terminal in circuit revision is known as variational and parameterized reduction technique. Nonetheless several other terminals are created and slow down the reduction process by making it hard.

In symbolic analysis all parameters of a circuit are used as a symbol while computing the analysis of that circuit. To compute a symbolic analysis, the circuit application must be linearized, so all the tools for analysis must be confined to linear model.

3. TIME VARYING ROOT LOCUS

3.1 Introduction

In this rapidly growing electronics world it is very important to design oscillators with modern specifications. To meet this need it is necessary to develop improved methods which can analyze an oscillator precisely. There are a number of different methods used to analyze the large signal LC oscillators during its development stage, so there is need to improvise these methods of fulfilling the requirements. These methods can be further divided into two sub categories to establish a clear understanding about several techniques. First category is known as design oriented, which provides the information regarding the mathematical physics of phase noise and the second is CAD oriented [2], which can conclude the phase noise of an oscillator with greater efficiency [1].

Design oriented method employs the simplest analytical terms in order to maintain the desired model structure. That is the reason these methods provide only a rough idea of possible outcomes and only applicable to limited type of oscillator topologies. These methods are effective in the situation where it is needed to analyze the phase noise of an oscillator while confining the physical properties and also provides solid design structure to optimize an oscillator. Furthermore, CAD oriented topologies are carried out through simulator and accurately analyzes phase noise with maximum possible efficiency [1].

Root locus methodology is a typical small signal analysis to analyze the oscillator startup process to determine different oscillation conditions [10]. By using linearization along with a characterization in Laplace transform it can be implemented into a broad spectrum. It is quantified with the different modifications in design process and then analyzing the resulted poles in both halves of the *s*-plane. If, the resulted pole exists in LHP (Left Half Plane) then it shows that the system is stable, but if the pole exists in RHP (Right Hand Plane) it means that the system is unstable. A system is set to be more stable if all the computed poles are situated in LHP and the safety limit of that system is evaluated by checking that how far away the poles are located from the imaginary axis. In case of oscillators to start proper oscillation a pole must be located in the RHP any typically this method is not applicable to analyze the behavior of large signal models [11].

Regardless of being an efficient method sometimes it may not be considered as a stable methodology as evaluating the roots become sensitive to large circuits, hence it makes difficult to compute the results especially when multiple roots are present. In this thesis

work a Time Varying Root Locus approach has been adopted and modified from the research work of Broussev and has been implemented on some inductor (passive) less (passive) oscillator circuits [14]. This technique has much resemblance with "frozen eigenvalues" concept devised by E. Linberg in his research [12], [13]. In which, he uses to freeze the circuit simulation at specific time instant and then calculate the eigenvalues at that time by linearizing the circuit. He concludes some important points with this technique such as, oscillator circuits are always nonlinear, nearer the poles to the imaginary axis greater will be the noise, and during a steady state operation the roots do not go away from imaginary axis rather they roam between RHP and LHP. The TVRL approach used here is CAD oriented semi-symbolic which is able to evaluate the complete architecture of an oscillator without any circuit simplification.

3.2 Cadence implementation to compute operating points

Before implementing the TVRL analysis for any oscillator design there is a need to find out the necessary basic simulations. For this purpose, the proposed circuit can be inserted into the "Virtuoso Schematic Editor" as shown in Fig. 15. Once the schematic is fully inserted and it shows no error while compiling the circuit, it can be used to draw operating points through different simulations.

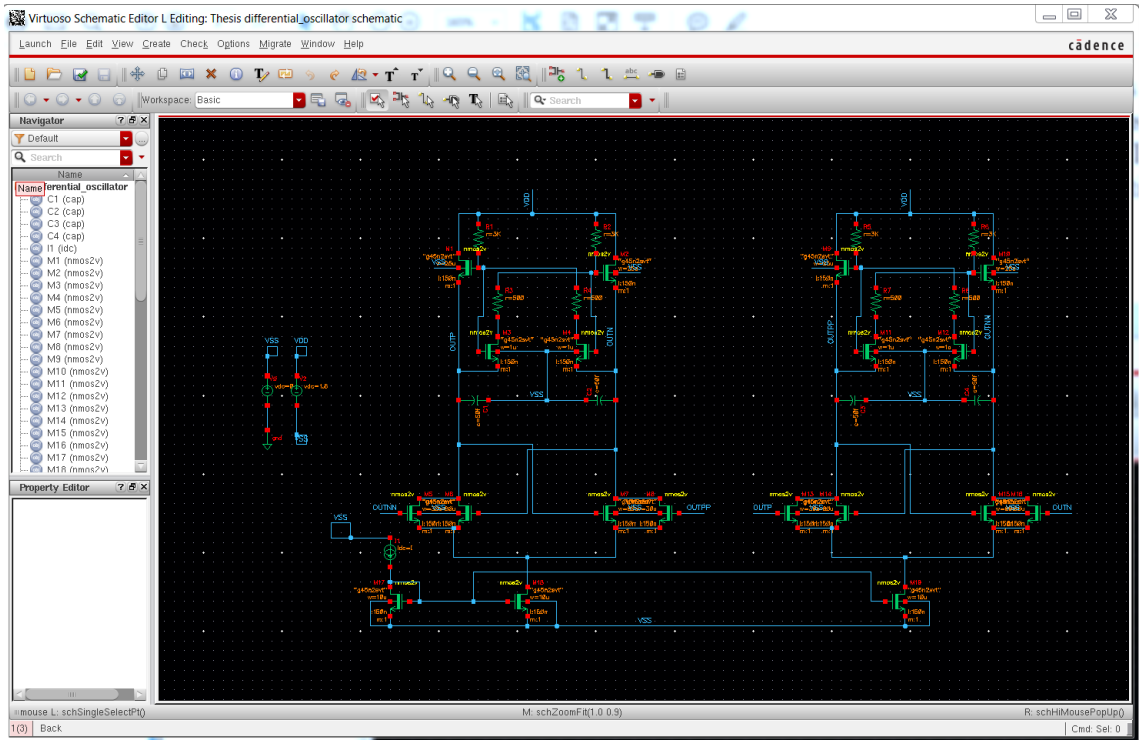

Figure 15: *VCO schematic in Virtuoso Schematic Editor.*

First of all the DC operating points of the proposed circuit is computed. It is a fundamental simulation to check whether the devices are properly biased or not. To find out the DC operating points of desired circuit, the "Virtuoso Design Environment" as

shown in Fig. 16, is initiated and then from analysis of design, the DC analysis is chosen. With the help of required setting shown in Fig. 17, the simulation is conducted. Hence the resulting point can be seen on schematic which will tells us that which of the required circuit portion is working in triode region or in saturation region.

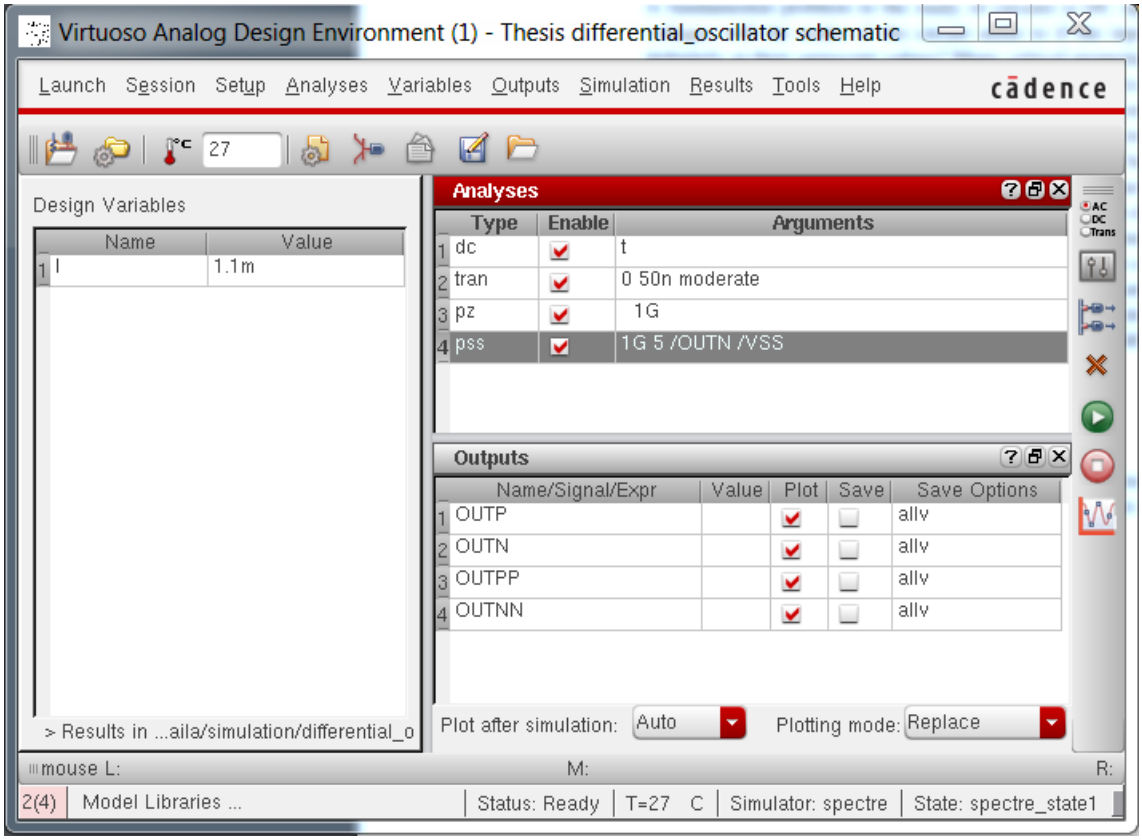

Figure 16: *Virtuoso Design Environment.*

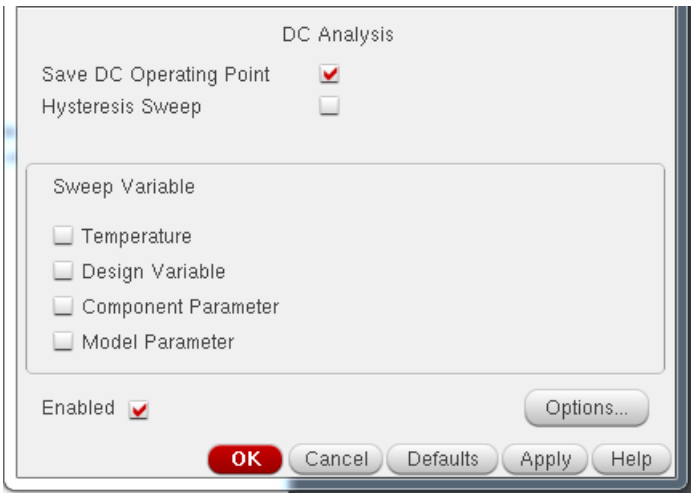

Figure 17: *DC operating points setting.*

Next the transient analysis of circuit is conducted to detect the behavior of proposed circuit. It is a time domain analysis of a circuit and can it can provide basic information about circuit start-up conditions but it cannot reveal it thoroughly. It is usually done for

a short interval of time in which a circuit can settle down for its final oscillation condition. Fig. 18 shows the required setting for transient analysis for the time period of 50ns.

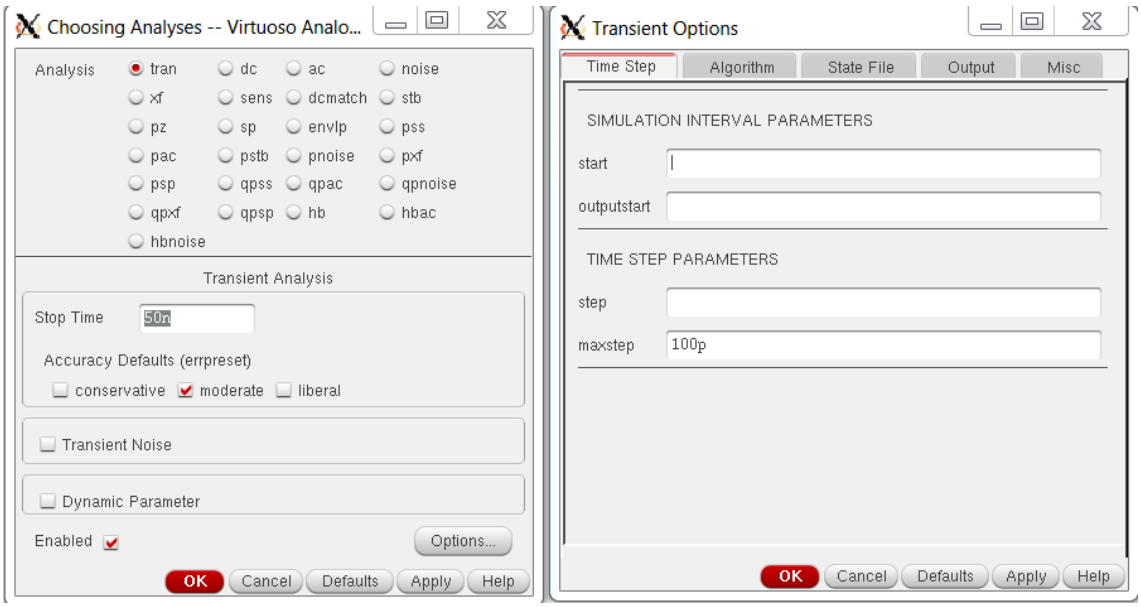

Figure 18: *Settings for transient analysis.*

Then pole-zero analysis is computed to find out the number of poles in the proposed circuit. This will later help to match the results calculated with the help of MATLAB, so that the further computations can be done with the help of TVRL algorithm. Fig. 19 shows the basic setting to compute PZ analysis and the corresponding results indicating the real and imaginary roots of the proposed circuit.

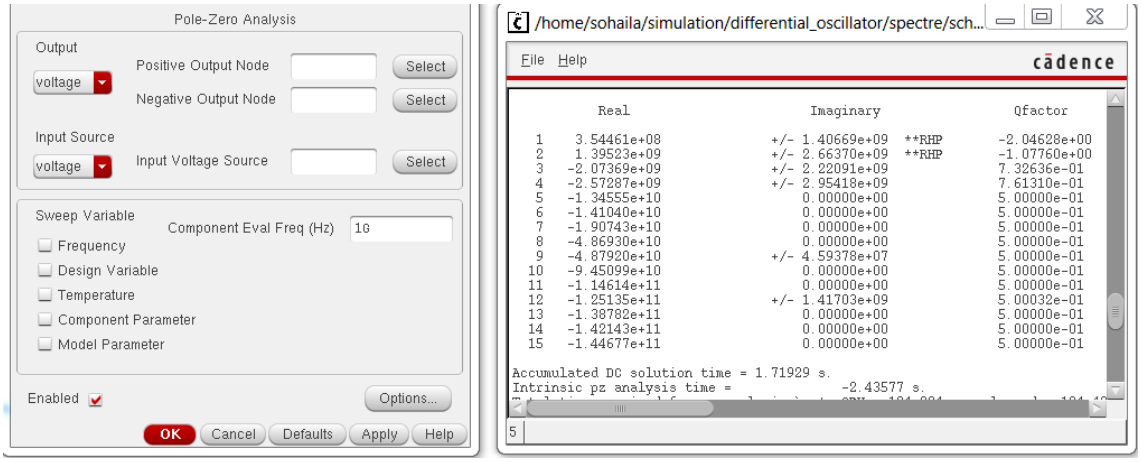

Figure 19: *Setting for PZ analysis and example of computed pole-zero.*

3.3 TVRL Algorithm description

In time varying root locus the path to the roots is computed during one oscillation period (T_0). Then the large signal oscillator behavior can be analyzed by using the obtained roots [1]. It is applicable on large signal oscillators with GHz-range frequency. This

method also avoids the feedback-loop-breaking operation [10]. Fig. 20 shows the flow chart of proposed CAD algorithm following the step by step procedure to analyze the oscillator.

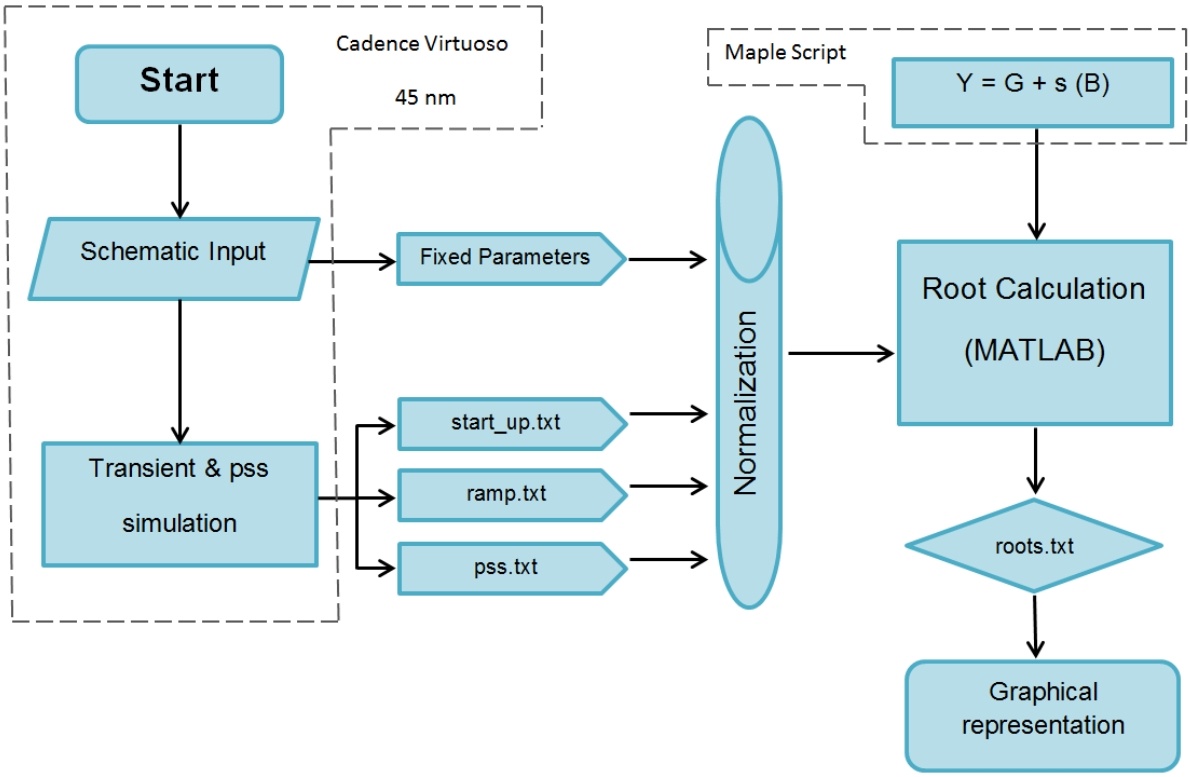

Figure 20: *CAD algorithm to compute TVRL.*

1. Periodic steady state solution:

   The PSS analysis of proposed oscillator circuit has been conducted using the Cadence 45nm generic process design kit SpectreRF simulator to obtain the required solutions. SpectreRF assures the most efficient conclusions of entire oscillator design. To carry out the simulation *gear2only* integration method is chosen. Fig. 21 shows the other options selected.

2. Generating .txt files of PSS node voltages:

   The results for active devices are linearized by using DC operating point analysis. Then the finalized node voltages are extracted through ocean script and saved in a .txt file.

3. Improving accuracy:

   Sometimes the circuit is complex enough so it is necessary to normalize the frequency and impedance of all passive and active components be-

fore composition of an admittance matrix in order to improve the efficiency of computation.

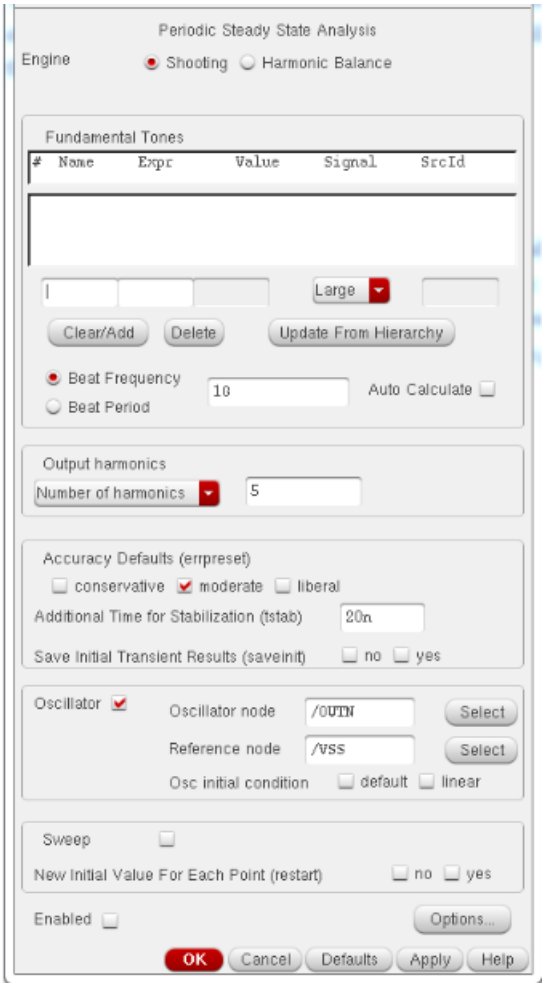

Figure 21: *Simulator setting to compute pss.*

4. Admittance Matrix formation:

   Then an admittance matrix to compute QZ is made by using the small signal parameters of transistor and fixed components values. The matrix is created with the help of *Maple Script*. The construction of matrix would be $\mathbf{Y}(s) = \mathbf{G} + s.\mathbf{B}$ [14].

5. Computing roots:

   Finally time varying roots for the specific oscillations are calculated by utilizing PSS data points along with QZ methodology with the help of MATLAB. It is compulsory to model the circuit components properly in order to quantify the exact number of operating points during simulation.

3.4 Decreasing TVRL computation duration

When the complexity of circuitry increases, it requires a need to speed up the TVRL analysis. So some adequate methods must be proposed to decrease the computational duration without affecting the essential data of oscillator behavior. Although the simulation is conducted for one period only, still the PSS points can be huge in number that can create hardship for simulation process. The solution to this problem is reducing some of the data points in which each *nth* point from PSS is taken and the rest *n-1* points are discarded. There is a drawback of this method that the real part of root can be missed which can cause the loss of critical information for root-locus. Another method is using adaptive selection. In this method, the value of change in node voltage does not increases its set limit and important points near zero axis and extra time instants used during transistor switching are taken. It does not require any comprehensive evaluation [1].

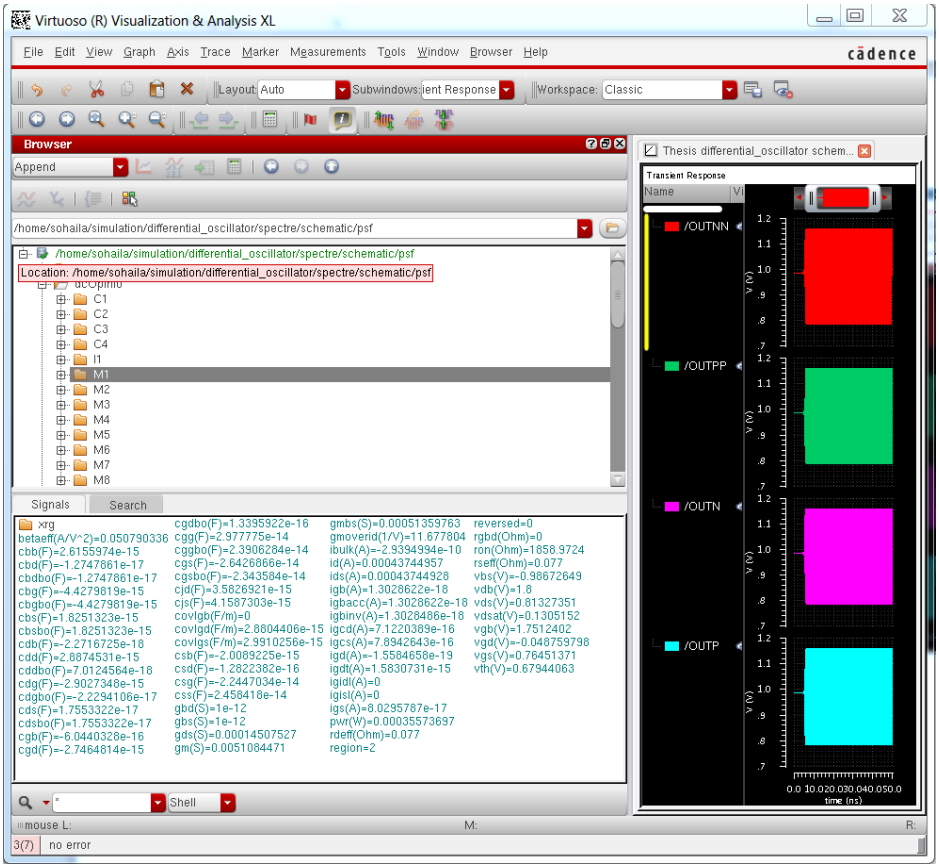

Figure 22: *Cadence result browser to access result directory.*

Secondly it takes much processing time while linearizing the active devices. So to speed up this process some modifications can be made to PSS simulation. It will help us to store the operating points directly rather than running the DC operating point simulation separately. The results can be simply extracted from Cadence result browser by accessing the result directory as shown in Fig. 22. There is also a need to insert the small signal device models separately through a model *.scs* file in which all devices must be

listed for which the small signal model is required. It will command the PSS simulator to save the parameter for small signal parameters of transistors.

Finally QZ method, which is used to compute the roots, takes an adequate time as it has to compute big matrices from complex circuits as well as infinite roots sometimes. In concern to this problem an iteration method can be introduced which will only compute those iterations that are specified by user. This will help to decrease the TVRL computational time. A user can easily choose the required iterations, as the PSS results can provide the oscillations frequency so required region can be targeted and a single pair of roots can be used to select iterations. This method can work efficiently on a specific part of a matrix rather than a full matrix used in conventional QZ method.

4. QVCO START-UP AND FREQUENCY ANALYSIS

It is presented in [16], that an LC resonator can be eliminated for a frequency synthesizer with high-level requirements. The VCO used in this design utilizes the Q enhancement topology to minimize the noise and tail current. So that circuit can efficiently conceal the phase noise along with a speedy frequency divider. Hence the resulted swing would also be large enough. The circuit used in this chapter is a further modified structure of a proposed oscillator by Jain in [17]. In that circuit, he employed a cross coupled pair of two negative channel MOS transistors to achieve negative resistance to the core of an oscillator. A common gate biasing condition is used with the help of two resistors for each transistor. This circuit does not include a passive inductor so two pairs of NMOS are fixed that will act as an active inductor. A current mirror circuit and a capacitor DC blocking circuit was also introduced in that circuit.

4.1 Circuit description

Fig. 23 shows a differential active inductor quadrature voltage controlled oscillator developed in Cadence 45nm GPDK library. In this circuit two VCOs (VCO_1, VCO_2) are combined together parallaly. To annul the resistive loss in LC tank, two pairs of cross coupled NMOSs (M_6, M_7 and M_{14}, M_{15}) are providing negative resistance to the core of VCO_1 and VCO_2 respectively. Like the circuit mentioned above, this circuit will also not use any passive inductor so there is a need to design an active inductor circuit. To achieve this, the set of MOSFETs (M_1–M_4) and (M_9–M_{12}) are forming the two port differential inductors which are able to form a behavior of an active resonator with the combination of C_0 capacitors. Right now the DC blocking circuit has not introduced in this circuit but late on it can be added if needed.

The transistors (M_1, M_2) and (M_9, M_{10}) are forming a cross coupled pair if seen according to DC point of view and the resistors R_f attached to them are improving the quality factor by acting as the feedback resistors. To get the tail current biasing a set of three transistors have been used as current mirrors from M_{17} to M_{19}. The rest of the MOSFETs (M_5, M_8, M_{13}, and M14) are connected to obtain quadrature output by parallel coupling of VCO_1 and VCO_2. While in running condition the transistors M_1, M_2, M_9, and M_{10} will always work in saturation mode but M_3, M_4, M_{11}, and M_{12} can run in both triode and saturation region depending upon the bias current.

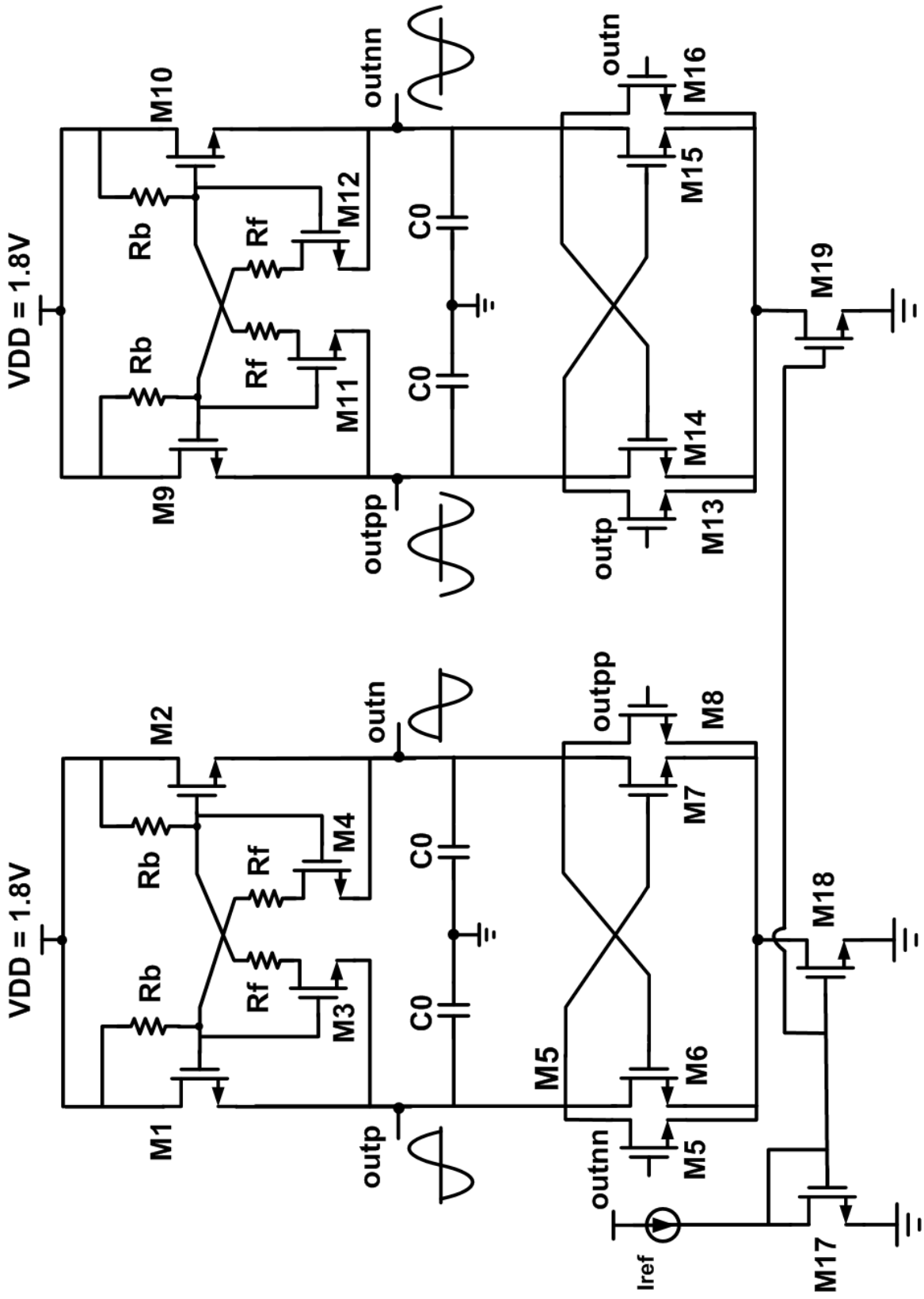

Figure 23: *Schematic of proposed quadrature VCO.*

Table 1. *Component used in above figure with channel length of 45nm.*

#	Component	Value
1.	M1, M2, M9, M10,	25 µm, *Channel Width*
2.	M3, M4, M11, M12,	1 µm, *Channel Width*
3.	M6, M7, M14, M15,	80 µm, *Channel Width*
4.	M5, M8, M13, M14,	30 µm, *Channel Width*
5.	M17, M18, M19,	10 µm, *Channel Width*
6.	Rb,	3 KΩ,
7.	Rf,	300 Ω,
8.	C0,	50 fF,

4.2 Oscillator start-up scrutiny

As Mentioned earlier the TVRL calculates the roots and trajectory associated to it, of a system during a single oscillation period. It is done with the help of time domain modeling with the help of SpectreRF simulator. To analyze the start behavior of this circuit a root locus method is used. It will not follow the feedback loop breaking action as the TVRL method will utilize the fully complex circuitry. There are total of 72 nodes for the proposed circuit. Hence the size of admittance matrix will be 72 by 72. By using start-up QZ algorithm the total roots calculated are 61. Fig. 24 shows the total computed roots.

The roots were computed with Iref= 1.1 mA and VDD =1.8 V. With Fig. 24, we can just say that many of the real negative roots are situated in the left half plane away from jω imaginary axis. But still it is not providing a clear picture of how roots are behaving. Fig. 25 shows the only interesting roots that are close to the jω axis. By reviewing Fig. 25, it can be said that the complex conjugate poles are entering to the right half of plane from the left half of s-plane with the help of acceptable loop gain. The resulted trajectory suggests that the circuit output signal will be increasing sinusoidal and hence the circuit is unstable.

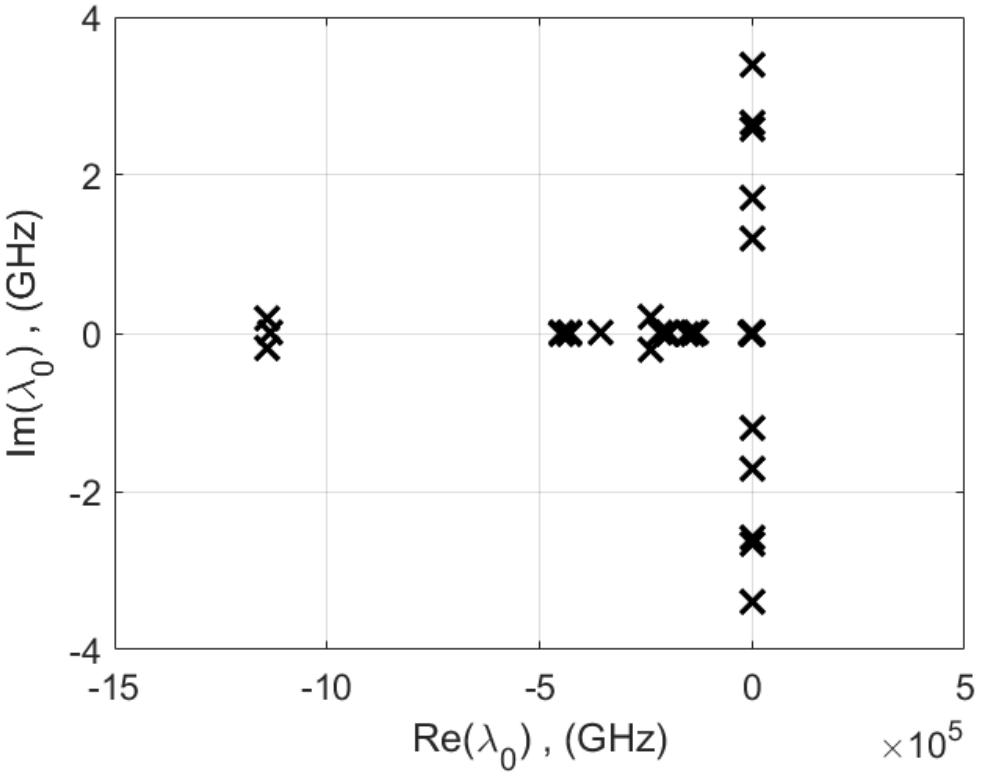

Figure 24: *All computed roots at start-up of oscillation.*

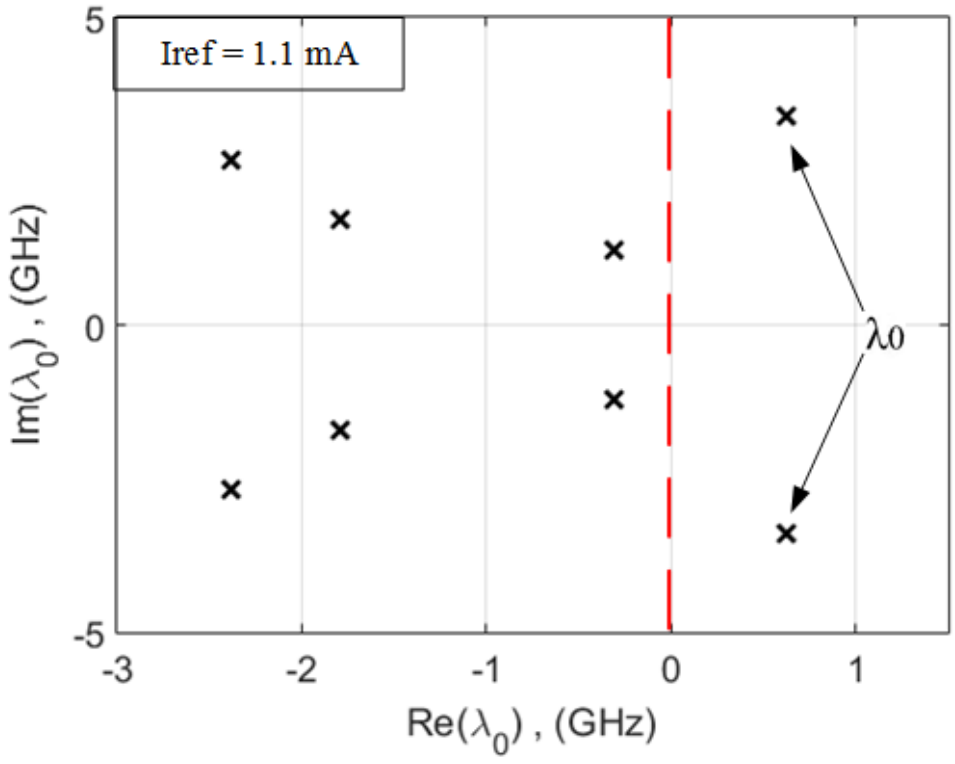

Figure 25*: Interesting roots near the border of RHP to LHP at start-up of oscillations.*

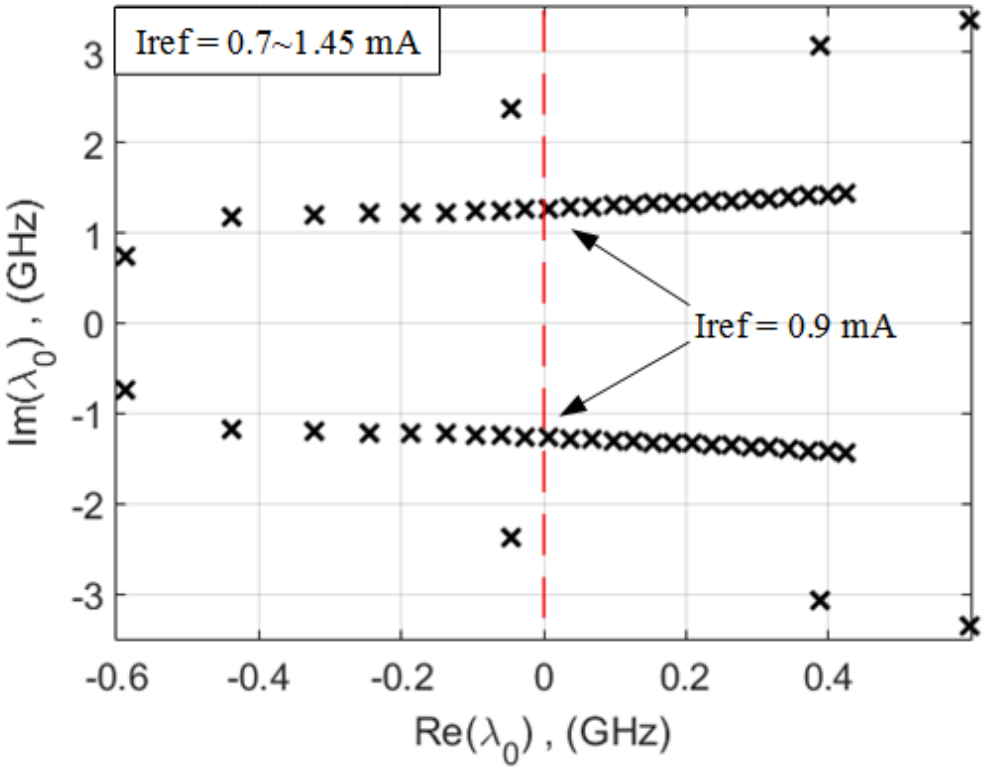

Figure 26: *Trajectory of dominant root at start-up as function of Iref.*

Fig. 26 represents the change in gm transconductance of root locus. The roots are computed with the change in Iref= 0.7 mA to 1.45 mA, hence they cross the jω axis when Iref = 0.9 mA. As the circuit has a pair of right hand poles the locus of roots shows the change in bias current. According to the Fig. 26, the complex poles mostly remain in the RHP while the loop gain is big enough.

The interesting point is, sometimes the complex poles can move to LHP again even the loop gain is too large. If this possibility is achieved the circuit becomes stable again and can produce a converging sinusoidal signal when excited. The selected circuit is not showing any converging signal.

4.3 Frequency stability investigation using TVRL

Fig. 27 shows the oscillation period from time instant A-H for the drain voltages of M_6 and M_7 along with the small signal parameters of related to this oscillation period at C, E and G.

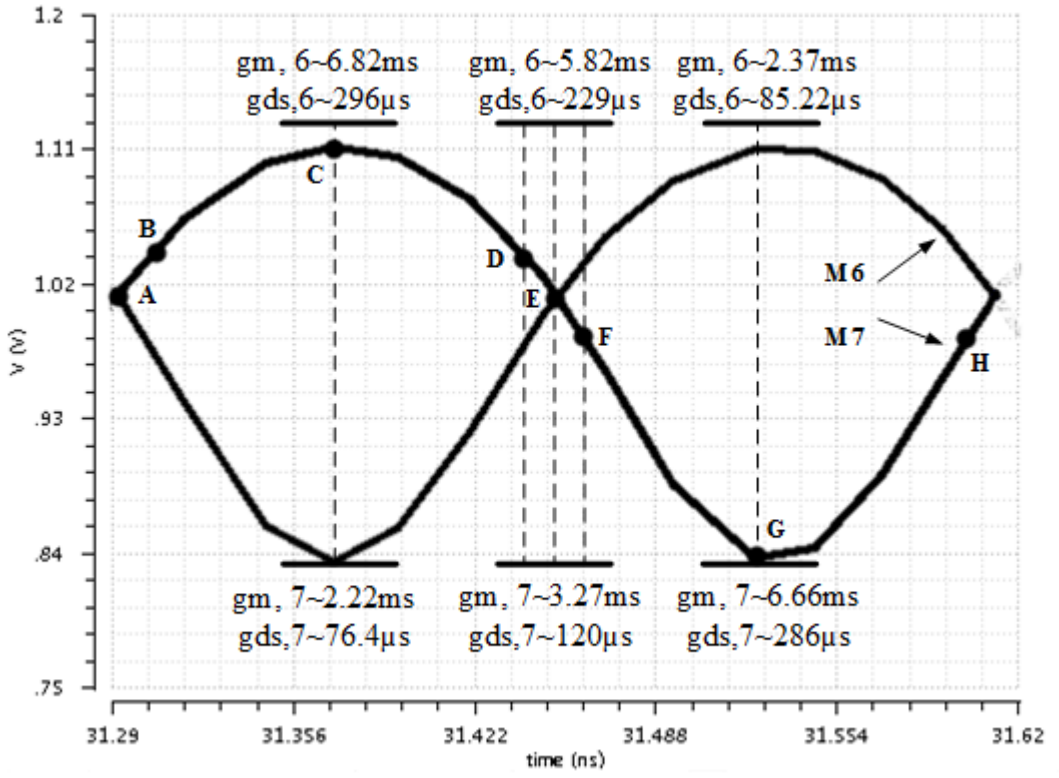

Figure 27: *Drain voltages of M6 and M7 (including gm and gds) for one oscillation period.*

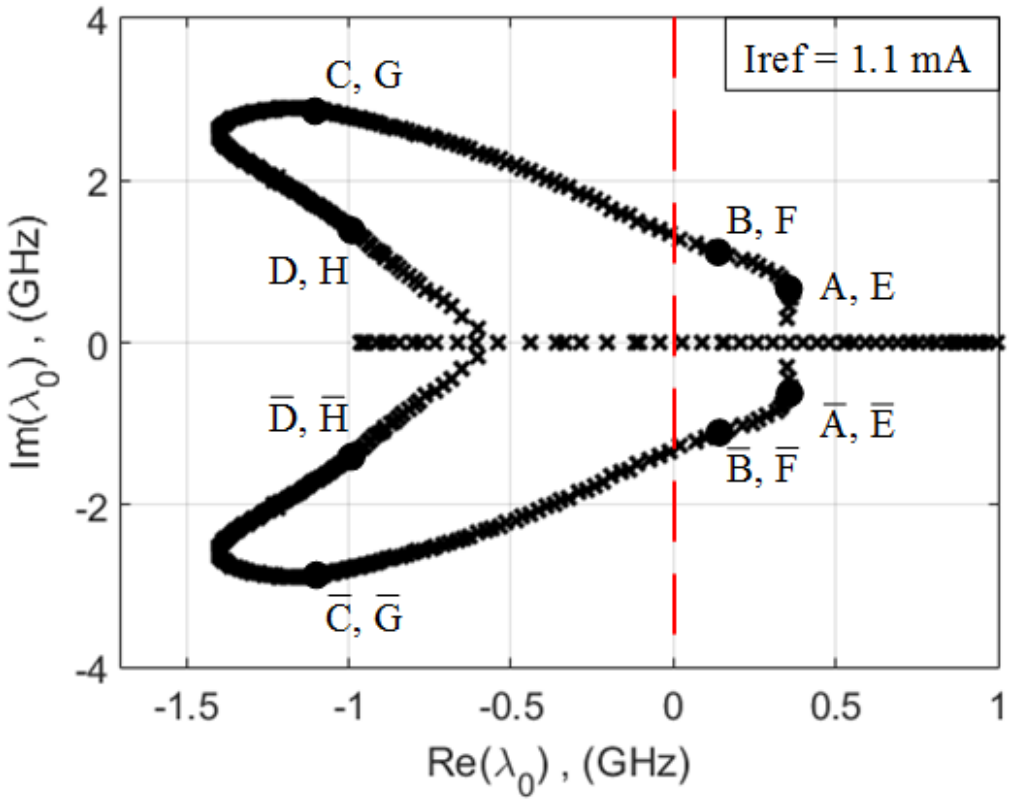

Figure 28: *Trajectories of all roots relative to one oscillation period of M6 and M7.*

Fig. 28 shows the related roots trajectory during large signal condition. It can be concluded that a single root λ0 roam among the RHP and LHP and crosses the imaginary axis jω. All the real roots that correlate during the existence of triggering multivibrator phenomenon are not negative and the remaining complex conjugate poles are located in LHP away from jω axis [17]. Thus, the analysis shows the possibility of relaxation process and oscillations can be initiated here because of positive real pole exist. The λ0 trajectory goes twice per period in the RHP and the LHP for VCO_1, hence repeats it again for VCO_2, due quadrature phases of oscillator.

The resonator quality effect factor for TVRL trajectory by varying the capacitance of the integrated capacitors C_0 has been analyzed and shown in Fig. 29. The TVRL obtained with C_0=70fF goes deeper into LHP, happens due to the excessive losses in the LHP and Iref is increased to maintain the same voltage swing [17]. While if the value of C_0 decreases further the TVRL moves to RHP. In the result of this the oscillator phase noise will decrease due to the increase in the negative conductance. Fig. 30 shows the part of a trajectory by varying the feedback resistance R_f.

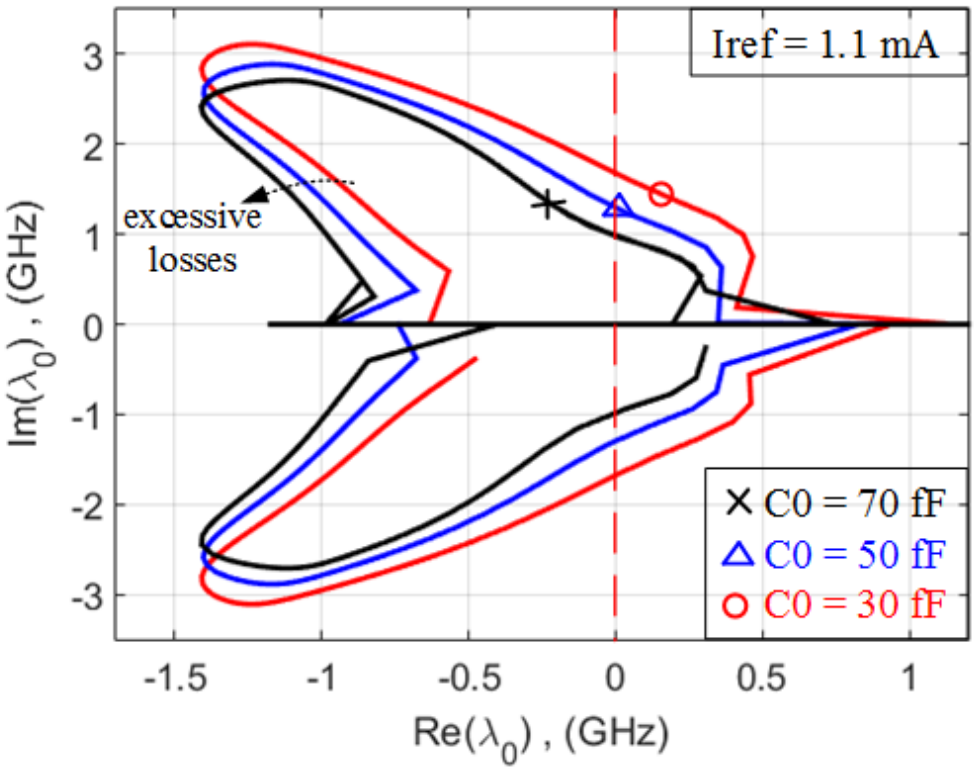

Figure 29: *Effect of capacitance (C0) variation on time varying root locus.*

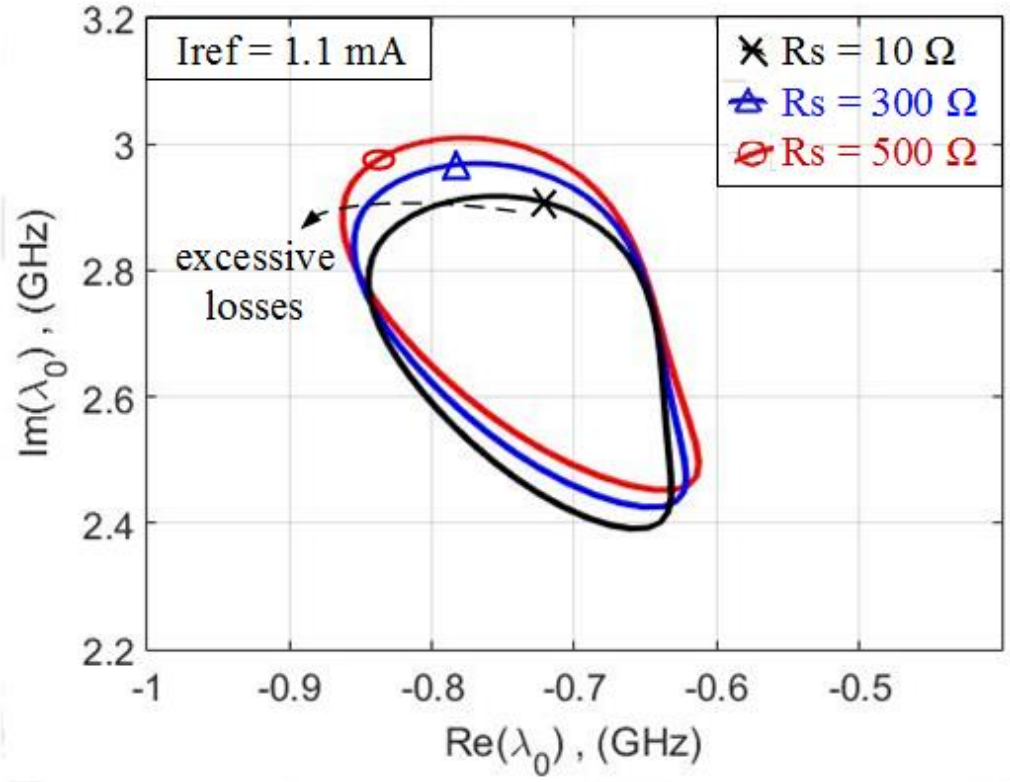

Figure 30: *Effect of resistance (Rf) variation on time varying root locus.*

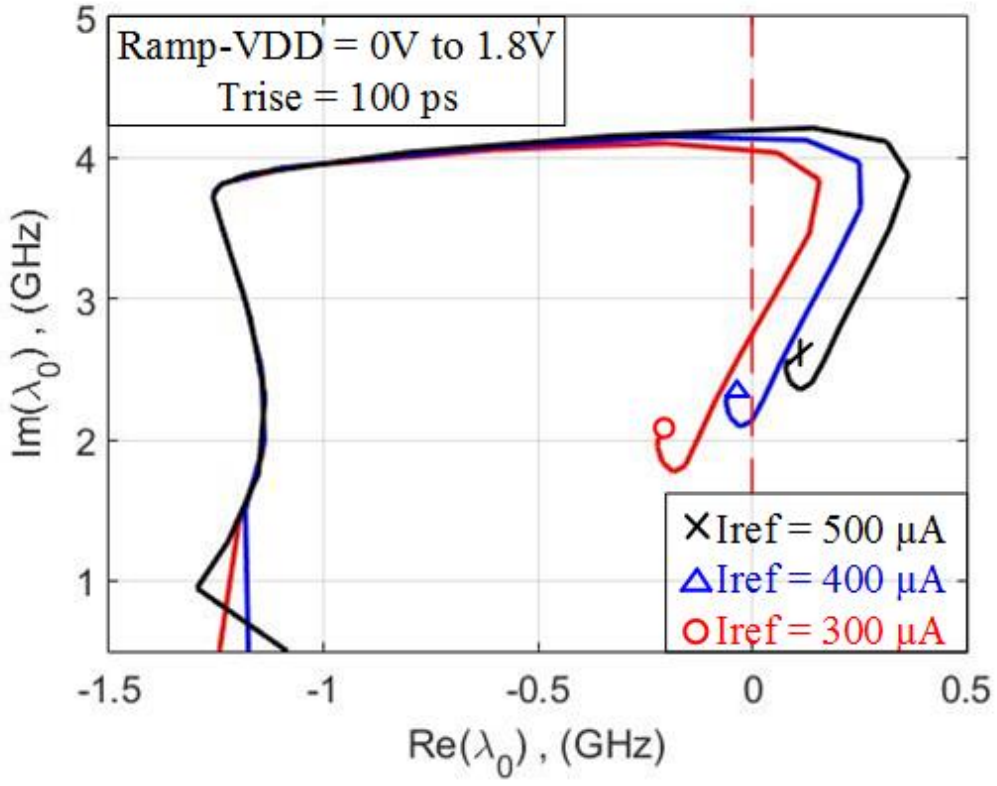

Figure 31: *Root locus for ramp power supply voltage.*

To inspect further, either the circuit is potentially stable or instable we need to supply a ramp supply voltage. Fig. 31 shows the modified circuit with ramp power supply voltage. It reveals the root locus of circuit, if the rise time is set to 100ps and VDD is changed from 0V to 1.8V. The step size is set to be 100ps and total transient time is 50ns, the dominant poles makes a small journey towards right from their final position. When Iref = 0.3mA & 0.4mA (marked with a circle and a triangle respectively), this journey is capable for the pole to cross over to the imaginary axis jω. Due to this reason the circuit is not able to attain the Dc loop gain to start oscillation and hence considered as unstable, but at end it settles in LHP finally. This condition may be expected by the initial condition created by the capacitor voltages, power supply and source current. When Iref = 0.5mA (marked with a cross), this journey is capable for the pole to cross over to the imaginary axis jω and the oscillations can be formed due to sufficient DC loop gain.

5. RING OSCILLATOR START-UP AND FREQUENCY ANALYSIS

When a combination of cascaded delay stages is connected in a closed loop chain, is known as the ring oscillator. For an ideal oscillator circuit it is very important to obtain perfect periodic signal with vey less noise perturbations. So it is one of the favorite oscillator circuits in many of the latest communication applications due to many of its helpful features to overcome this situation. With moderate power conditions it can oscillate properly, providing high oscillation frequency. It is capable of delivering wide tuning range and can be tuned electronically. Ring oscillators can be designed easily with latest CMOS (Complementary Metal Oxide Semiconductor) technologies. Most of all it can provide multiphase outputs so that the multiple clock signals can be achieved with only one basic structure. The final oscillation frequency depends on the number of stages used in the circuit and the delay caused by these stages. Now a days ring oscillators are widely used in frequency synthesizers based on Phase-lock loop [31].

5.1 Circuit description

Fig. 32 shows the five stages ring oscillator using an inverter combination with tail current source designed in Cadence 45nm Generic PDK library. The MOSFETs (M_1 -M_{12}) are used to form a five stage ring structure. Inverter is designed by using one NMOS and PMOS transistor. As for M_1 and M_2, they can operate either in saturation or triode region of operation, depending on the bias current. PMOS transistor works as a pull-up network and NMOS transistor works as a pull-down network. These five outputs can be logically combined to realize multiphase clock signals, which have considerable use in a number of applications in communication systems. The transistors (M_{11} -M_{12}) are used as current mirrors for tail current biasing.

Table 1. *Component used in above figure with the channel length of 45nm.*

#	Components	Value
1.	M1, M3, M5, M7, M9,	18 µm, *Channel Width*
2.	M2, M4, M6, M8, M10,	9 µm, *Channel Width*
3.	M12, M11,	30 µm, *Channel Width*

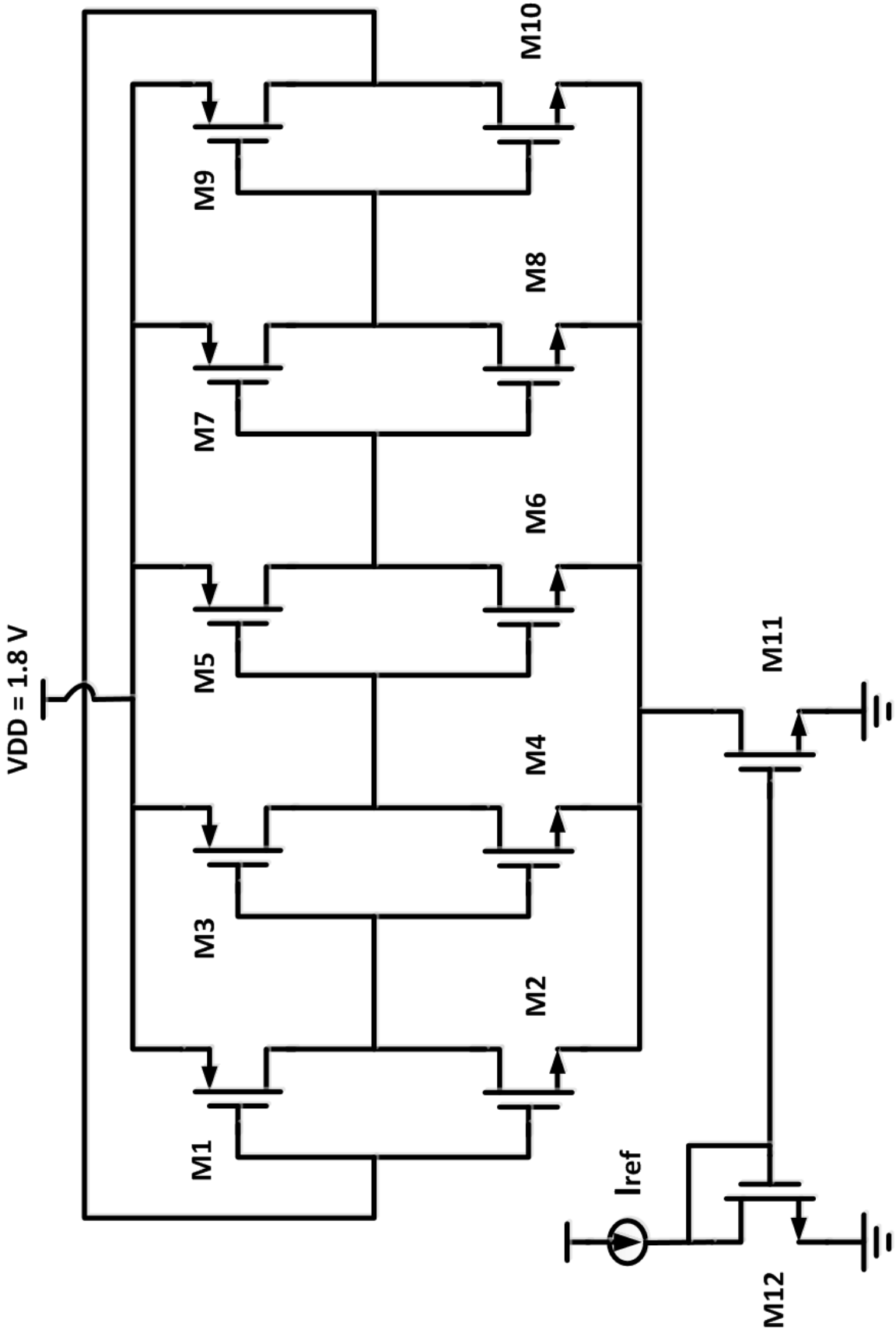

Figure 32: *Schematic of proposed ring oscillator.*

5.2 Oscillator start-up scrutiny

The TVRL calculates the roots and trajectory associated to it, of a system during a single oscillation period. It is done with the help of time domain modeling with the help of SpectreRF simulator. To analyze the start behavior of this circuit a root locus method is used. It will not follow the feedback loop breaking action as the TVRL method will utilize the fully complex circuitry. There are total of 43 nodes for the proposed circuit. Hence the size of admittance matrix will be 43 by 43. By using start-up QZ algorithm the total roots calculated are 61. Fig. 33 shows the total computed roots.

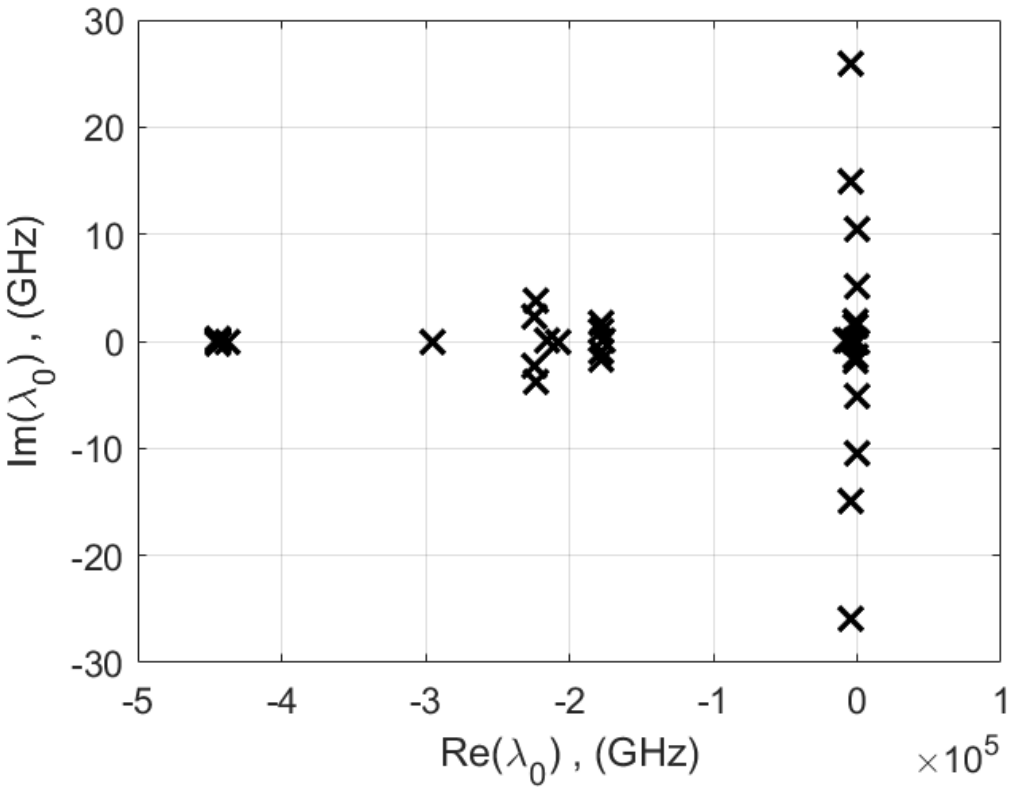

Figure 33: *All computed roots at start-up of oscillation.*

The roots were computed with Iref= 570 µA and VDD =1.8 V. With Fig. 33, we can just say that many of the real negative roots are situated in the left half plane away from jω imaginary axis. But still it is not providing a clear picture of how roots are behaving. Fig. 34 shows the only interesting roots that are close to the jω axis. By reviewing Fig. 34, it can be said that the complex conjugate poles are entering to the right half of plane from the left half of s-plane with the help of acceptable loop gain. The resulted trajectory suggests that the circuit output signal will be an increasing sinusoidal and hence the circuit is unstable.

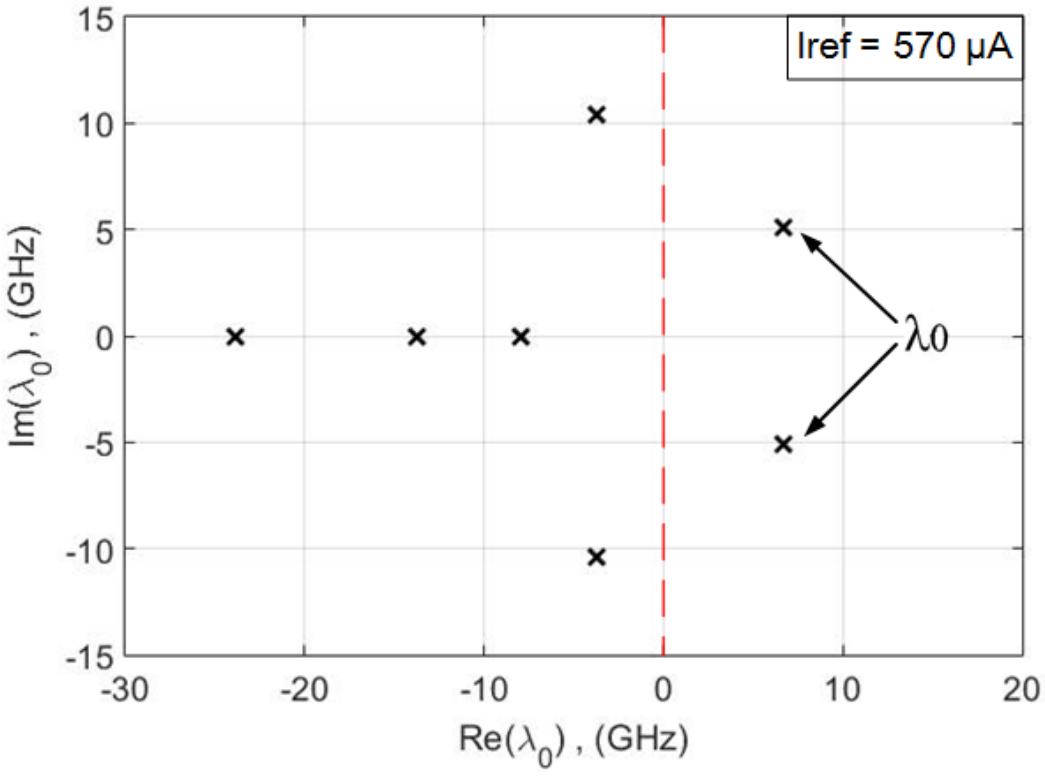

***Figure 34**: Interesting roots near the border of RHP to LHP at start-up of oscillations.*

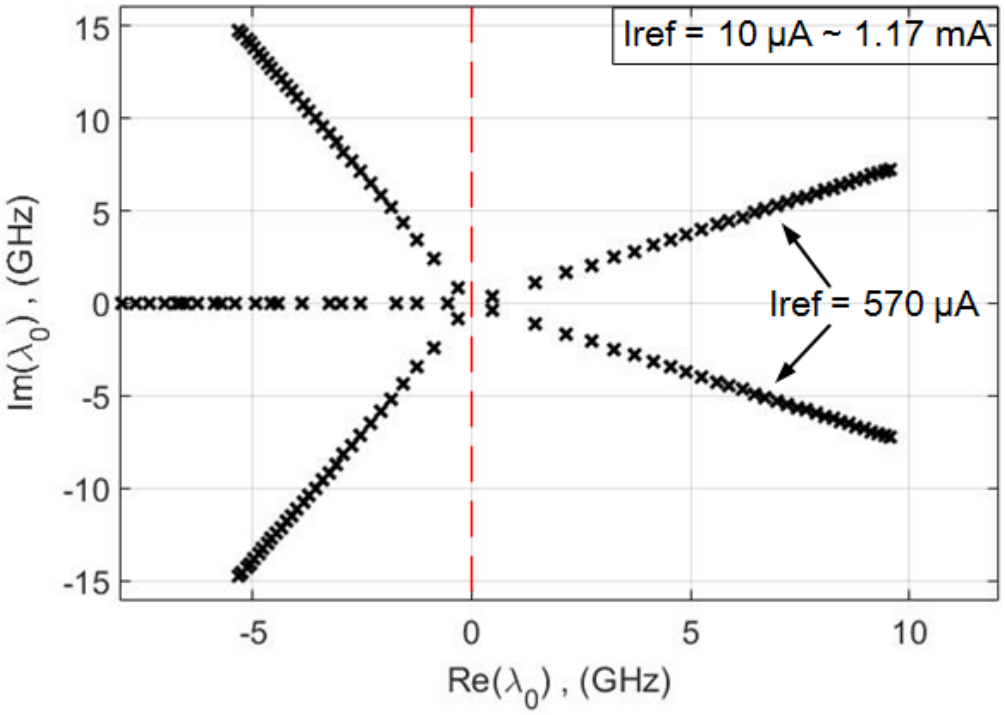

***Figure 35:** Trajectory of dominant root at start-up as function of Iref.*

Fig. 35 represents the change in gm transconductance of root locus. The roots are computed with the change in Iref= 10 µA to 1.17 mA, hence they cross the jω axis when Iref = 570 µA. As the circuit has a pair of right hand poles the locus of roots shows the change in bias current. According to the Fig. 35, the complex poles mostly remain in the RHP while the loop gain is big enough.

The interesting point is, sometimes the complex poles can move to LHP again even the loop gain is too large. If this possibility is achieved the circuit becomes stable again and can produce a converging sinusoidal signal when excited. The selected circuit is not showing any converging signal.

5.3 Frequency stability investigation using TVRL

Fig. 36 shows the oscillation period from time instant A-H for the drain voltages of M_6 and M_7 along with the small signal parameters of related to this oscillation period at C, E and G.

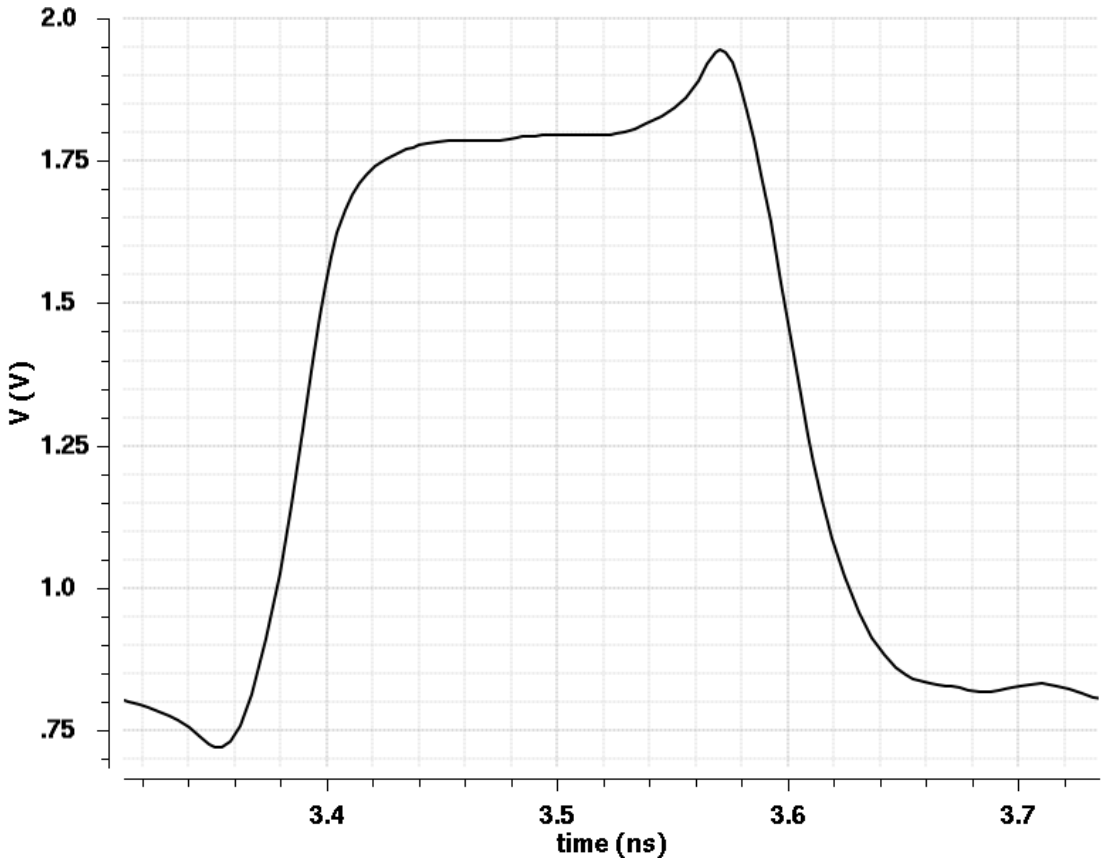

Figure 36: *Drain voltages of M6 and M7 (including gm and gds) for one oscillation period.*

Fig. 37 shows the related roots trajectory during large signal condition. It can be concluded that a single root λ0 roam among the RHP and LHP and crosses the imaginary axis jω. All the real roots that correlate during the existence of triggering multivibrator

phenomenon are not negative and the remaining complex conjugate poles are located in LHP away from jω axis [17]. Thus, the analysis shows the possibility of relaxation process and oscillations can be initiated here because of positive real pole exists. The λ0 trajectory goes twice per period in the RHP and the LHP for VCO_1, hence repeats it again for VCO_2 due quadrature phases of oscillator.

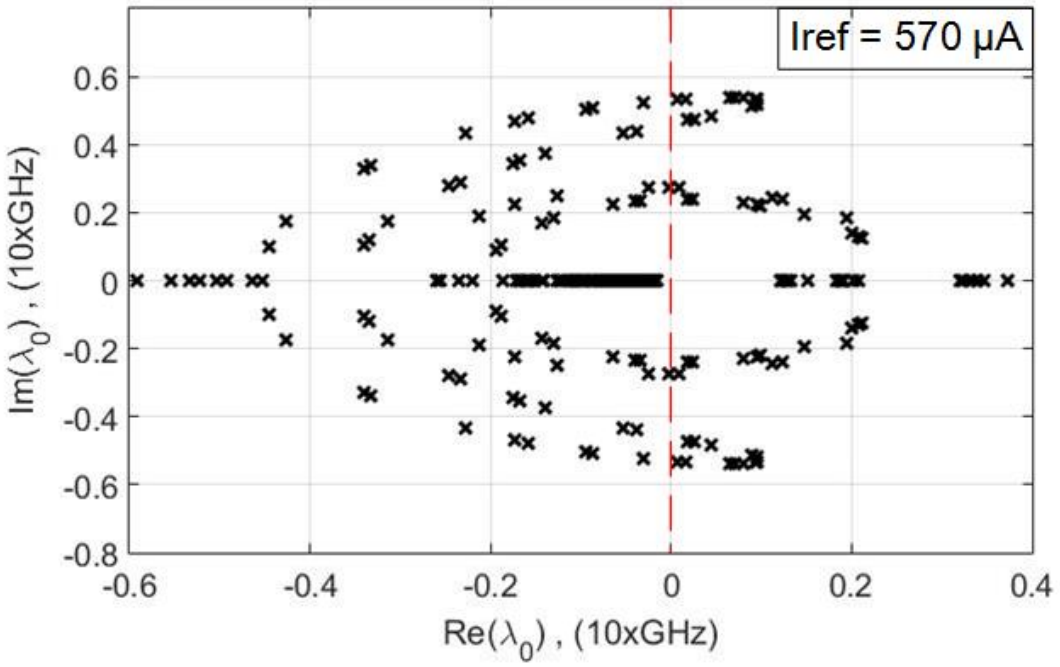

Figure 37: *Trajectories of all roots relative to one oscillation period with M_1 (W = 21µm) and M_2 (W = 10.5µm).*

The circuit is modified and all real roots are negative (shown in Fig. 38) which corresponds to the absence of multivibrators triggering phenomenon Therefore, it confirms the proper sinusoidal operation of oscillator. The key point to further investigate the potential instability of the circuit lies in applying a ramp supply voltage. Fig. 7 shows the root locus when VDD rises from 0 V to 1.8 V within 100 ps rise time, is applied. During this transient time of 50 ns and step size=100 ps, the dominant pole makes a short trip in the RHP (marked in the figure).

To inspect further, either the circuit is potentially stable or instable we need to supply a ramp supply voltage. Fig. 39 shows the modified circuit with ramp power supply voltage. It shows the root locus of circuit, if the rise time is set to 100ps and VDD is changed from 0V to 1.8V. The step size is set to be 100ps and total transient time is 50ns, the dominant poles makes a small journey towards right from their final position.

When Iref = 170 µA & 570 µA & 970 µA (marked with a circle, a triangle and a cross respectively), these trips are large enough for the main root to cross over the imaginary axis jω and the dc loop gain is sufficient to develop into oscillations.

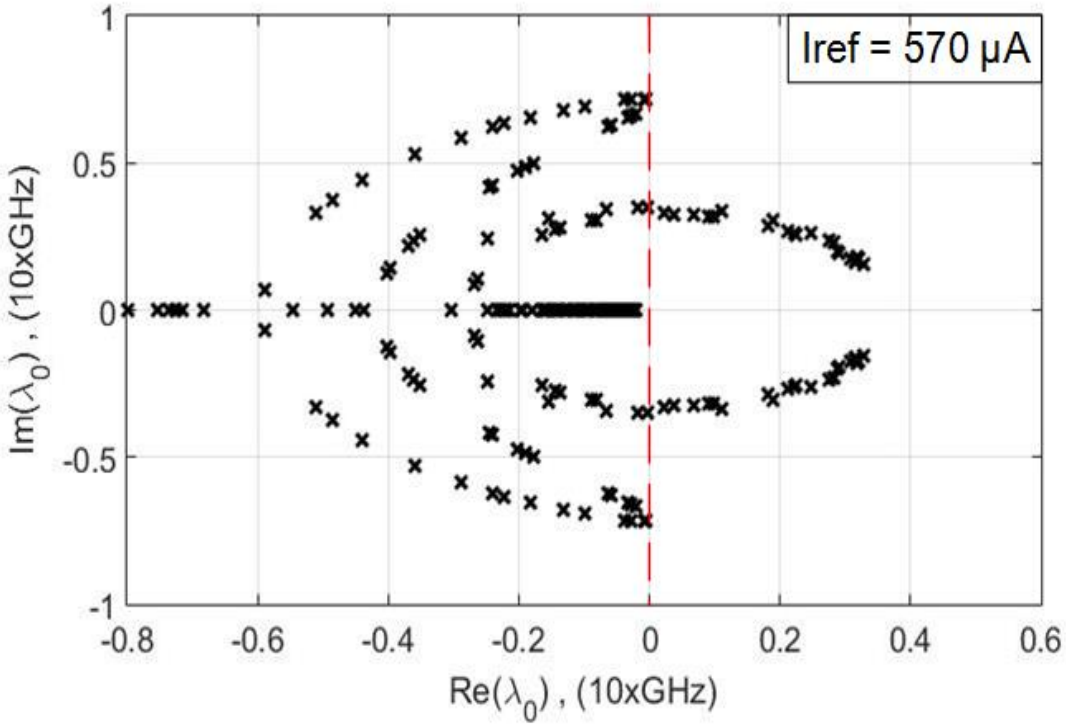

Figure 38: *Trajectories of all roots relative to one oscillation period with M_1 (W = 21µm) and M_2 (W = 10.5µm).*

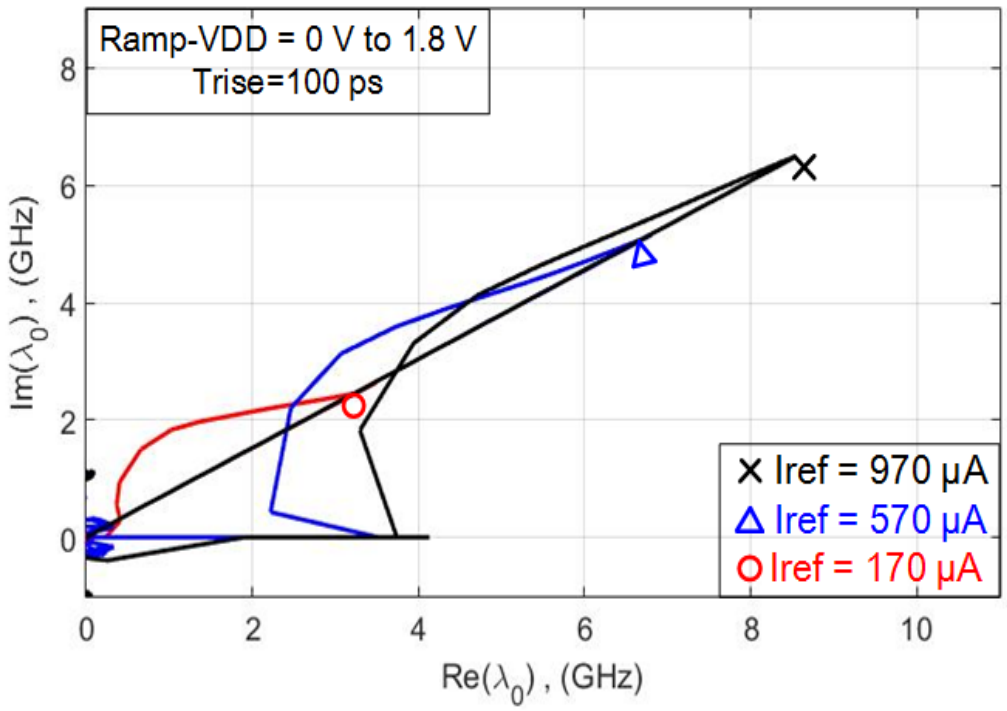

Figure 39: *Root locus for ramp power supply voltage.*

6. CONCLUSION

This draft is mainly focused on Time-Varying Root-Locus technique which was used to realize the theoretical analysis of voltage controlled oscillators. The root trajectories were associated with the trajectories of the physical aspects of oscillators. In the present world different kinds of circuit simulators are available, but if an oscillator circuit fails to provide a proper sinusoidal signal then none of them is capable of computing the operating points directly. In s-plane, complex roots are located to determine the start-up frequency of oscillators and hence QZ algorithm was applied to find out the roots of characteristic equation.

The TVRL turned out to be useful tool for evaluating the different influencing behavior during the operation of an oscillator. The mechanism of relaxation and sinusoidal oscillations was concluded with the help of Cadence SpectreRF. SpectreRF obtained the time varying periodic results to depict the TVRL trajectory of important poles. It can be said that TVRL methodology is able to compute results with acceptable numerical precision. Moreover further enhancements in pole-zero computation methodology can handover an essential design tool to circuit designers. Especially the operating points of nonlinear circuits can be analyzed with ease.

The present time varying root locus structure is not capable to fine out the exact phase noise of an oscillator circuit, so with respect to future work root trajectories can be linked directly with the phase noise for more accuracy. To achieve this, root sensitivity of design parameters and noise can be computed. As TVRL is a newly devised method so currently it has many unknowns which are yet to be digged out, so it provides a lot of opportunities for researchers in the area of RF design and development.

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