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TAMPERE UNIVERSITY OF TECHNOLOGY

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HIGH SPEED MONOLITHIC LEVEL SHIFTER FOR LC TYPE DCDC CONVERTER IN 45NM CMOS TECHNOLOGY.

Master of Science Thesis

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Examiner: Prof. Nikolay T. Tchamov and Jani Järvenhaara
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ABSTRACT

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Level shifter is an important building block in the power management system. In the DC-DC buck converter, requires a control signal with very low rise and fall time. Level shifters are used to convert low voltage signal to high voltage signal for the high side PMOS transistor of the power stage and allows increasing the efficiency of the DCDC buck converter with low rise and fall time.

This thesis presents High voltage tolerant level shifter using differentially switched cascode transistor topology in cascade structure. This high voltage tolerant level shifter is providing high voltage control signal to the power stage of the step down dc-dc converter. Output signal of the level shifter has an offset of 5VDD of the nominal supply voltage at high frequency with a very low power loss of 1.84mW where each VDD is 1V. P-Driver and N-Driver provides dead time controlled signal for the power stage PMOS and NMOS transistor. The dead time for the high to low side is 157ps and low to high side is 115ps. The layout of single stage level shifter is presented which consumes a silicon area of 83.54×121.86 [μm×μm] and layout of the all three stages consumes 262.82×124.66 [μm×μm] of silicon area. The converter is designed in standard 1V, Cadence 45nm Generic Process Design Kit (GPDK). The switching frequency is 52MHz. The converter operates with 6V input voltage and provides 1.25V constant output voltage. When the input power is 200mW, the extracted simulation gives a peak conversion efficiency of 79.65% with 200mA output current. All the result and the efficiency calculation are presented with PCB and package parasitic for real component.

PREFACE

The research work presented in this thesis was done at the RFIC Laboratory, Department of Electronics and Communications Engineering, Tampere University of Technology (TUT). It is the continuation of a project with our industry partner Ericson, who financially supported the research developments.

During the 1-year period, I have received a lot of help from my supervisor and colleagues in our group. Foremost, I would like to thank Prof. Nikolay T. Tchamov for providing me the great opportunity to work in his research group. I also would like to thank my direct consultant Jani Järvenhaara for their unconditional help. Meanwhile, I want to thank all other team members of RFIC Laboratory for the excellent work environment we have created together.

Last but not least, I would like to thank my parents for their continuous support and inspiration, which have been the main source of motivation during my M.Sc. study.

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ABBREVIATIONS

DC-DC	Direct-Current to Direct-Current
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal-Oxide-Semiconductor
IC	Integrated Circuit
PWM	Pulse Width Modulation
DTLH	Dead Time at Low-to-High transition
DTHL	Dead Time at High-to-Low transition
NOS	Non-overlapping switching
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
VPCD	Virtuoso Passive Component Designer
LVS	Layout vs. Schematic
DRC	Design Rule Check
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation

1 Introduction

Portable electronic devices have developed significantly in the recent years. These devices use batteries as their power supply. Among these batteries Li-Ion battery is commonly used. Li-Ion batteries provide output voltage from 4.2V to 2.6V [1]. As the battery voltage fluctuates, these batteries cannot be used as a direct power supply for the devices. Most of these devices operate at fixed voltage level. To overcome this problem, power management unit is used between the battery output and the electronic circuit's supply input. The fundamental purpose of Power management unit is to regulate the battery output voltage at a fixed voltage, which is appropriate for the operation of the electronics circuit. DC-DC converter is one of the major components of the Power management unit.

DC-DC converter known as switching voltage regulator provides constant, smooth regulated output voltages while the input voltage and the load current is varying widely. In the portable devices different components requires fix various voltage and current level for operation. In order to ensure coherent operation of these circuits so that a stable system can be formed and maintained, high quality voltage regulation is necessary. The power distribution system from the battery for the different electronic application blocks is illustrated in Figure 1-1. A charger with transformer line isolation converts the AC line voltage to DC voltage to charge the battery. A lithium-ion battery supply unregulated voltage to the power management unit which contain a number of DCDC converters. DCDC converters generate the regulated supply voltages required by the different application block from the unregulated battery supply voltage.

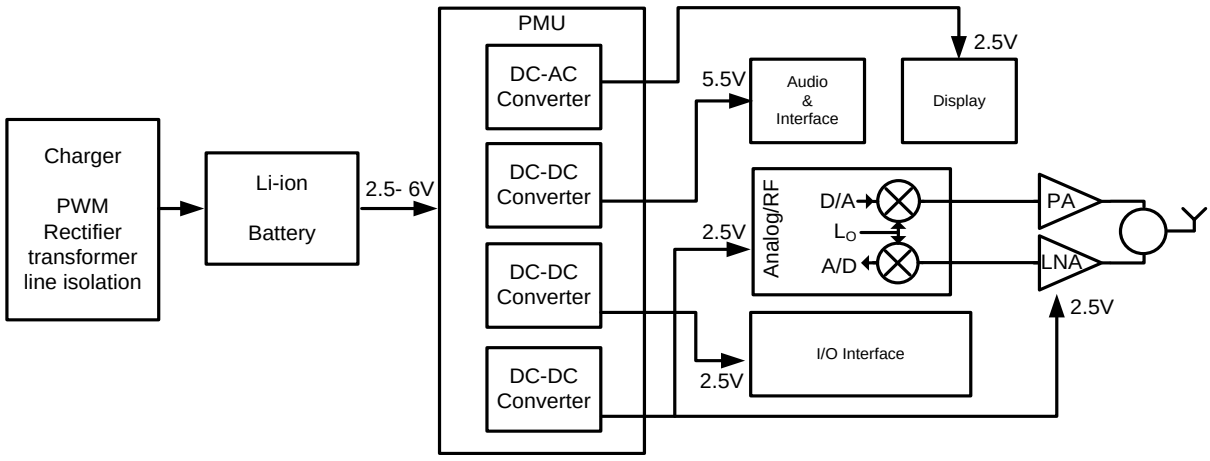


Figure 1-1: Battery operated application with DCDC converter

1.1 DCDC Converter IC Types

DCDC converter can generate a fix specified DC voltage required by the different circuit block for the system. The voltage generated from the converter must be maintained within tight voltage envelope to satisfy the guaranteed performance and functionality of the circuit. Different techniques converters can be used to achieve fix DC voltage and every technique has its own advantages and disadvantages. DCDC converter can be divided into two main topologies depending on the properties of the converter. Linear converter and switched capacitor converter are two of them. The switching converters can be buck, boost or buck-boost type converter. Buck converter provides lower output regulated voltage where boost converter provides higher regulated output voltage than the input voltage. Buck-boost converters are capable of providing both higher and lower output voltage.

I. Linear Voltage Converter

Linear converter also known as series-pass converter is very popular among the designers due to the simplicity and smaller area of the circuit. Efficiency of linear converter is a major concern as it takes the ration between output and input voltage. For the higher voltage conversion the ratio becomes less [3]. The operation of a simple linear converter is illustrated in Figure 1-2.

In the simple linear DCDC converter V_{in} is the input power supply and V_{out} is the output voltage supplied to the load resistance R_L. The variable resistor R_{var} lowers the input supply voltage to output voltage. The maximum efficiency η_{max} attained from the simple linear converter is

$$\eta = \frac{V_{OUT}}{V_{in}} \tag{1.1}$$

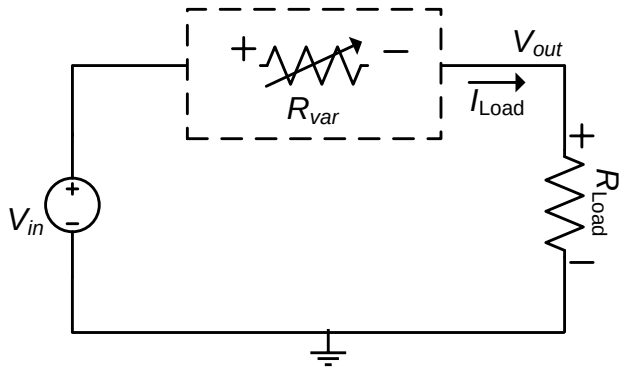


Figure 1-2: A simple model of linear DC–DC Converter.

As shown in equation (1-1), linear DCDC converter can only provide high efficiency when the voltage difference between output and input voltage is small. For the higher voltage conversion, the voltage difference between output and input voltage becomes higher and the efficiency decreases. Therefore, the switched-mode DC-DC converter topologies emerge, where high conversion ratio is needed [4].

II. Switched Capacitor Converter

Switched capacitor converter is also known as charge pump converter which can provide different DC output voltage level with different magnitude and/or an opposite polarity with respect to the input voltage. Switched capacitor type converters are widely used to in analog mixed signal circuit for the on-chip integrated circuit [3]. Capacitors are used to transfer charge from the input supply voltage to the output of the converter. This capacitor size is depended on the frequency of operation of the circuit. Higher frequency operation allows smaller valued capacitor but the losses in the capacitor prevent to achieve higher efficiency in the fully integrated Switched capacitor type DCDC converter. Figure 1-3 is an example of switched capacitor converter.

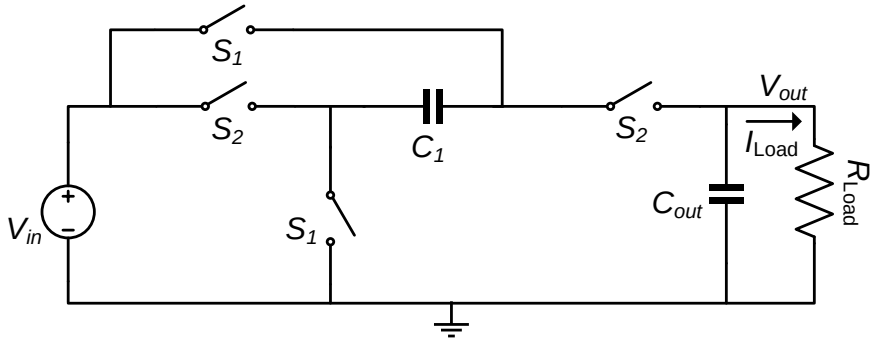


Figure 1-3: Schematic representation of a switched-capacitor DC–DC converter ($V_{out} = 2 \times V_{in}$)

The circuit has two mutually switching networks S_1 and S_2 which is controlled by two phase control signal. Switch S_1 is controlled by the phase 1 control signal and switch S_2 is controlled by the phase 2 control signal. Phase 1 and phase 2 control signals are non-overlapping control signal so when phase 1 switch is active, phase 2 switch is in cut off, capacitor C_1 is charged to input supply voltage Vin. In this state, output capacitor C_{out} supplies the output current. When capacitor C_1 is fully charged to supply voltage, phase 1 switch is cut off and phases 2 switches is activated, which allows output capacitor to be charged to twice of supply voltage. The output voltage in a practical switched capacitor converter will not be twice of the supply voltage because of the voltage drop across the series resistance of the MOSFET switches, which will degrade the efficiency of the converter.

The disadvantage of charge-pump converter is the poor efficiency characteristics, discrete output voltages and low output current as compared to inductive type switch mode converter. Switched capacitor converter relies on periodically charging and discharging of the capacitor through the resistive switches. The power loss of this type

converter is high. Switched-capacitor circuits are typically used in applications with relaxed supply voltage constraints (such as DRAMs) that do not require tight voltage regulation [3].

III. Switching DCDC Converter

Switching DCDC converters are widely used as the converter has stable output voltage regulation characteristic and high efficiency. The efficiency of the converter can approach to 100% where the transistor switches are made ideal which is different from the linear and switched capacitor DCDC converter. Switching converters can be separated in to two primary classes. The first class is the switching converter which developed with transformers and the second class which developed with inductor.

The transformer used in switching converter is the DC isolation of the input and output grounds [5]. In the DCDC converter, the input power supply voltage is high and also carries noise so for the reliable operation of the load, load and the input power supply should be isolated. The implementation of the circuit is relatively easy and converter can generate multiple DC output voltages from the single input power supply.

Inductor type switching DCDC converter does not require any isolation. Inductor used in the converter acts as a storage device and the capacitor are used for the filtering of the signal. The charging of capacitor through inductor is more efficient than charging through voltage source [5]. For the both low power and low voltage applications inductive type switching converters are widely used because of high efficiency. A switching buck converter generates lower output voltage as compared to the input voltage where boost type converters provide higher output voltage as compared to input voltage. The comparison of three converter types is summarized in Table 2-1.

Table 1-1: Converter Type Comparison

Type of DCDC Converter	Linear Converter	Switched Capacitor Converter	Inductive Switching Converter
Low to high voltage conversion	No	Yes	Yes
High to low voltage conversion	Yes	Yes	Yes
Polarity reversal	No	Yes	Yes
Efficiency	Low	Low	High
Voltage regulator	Poor	Poor	Good
Output voltage ripple	Low	High	High
Area	Small	Medium	Large
Application	DRAM, Voltage references	DRAM, flash EEPROM and mixed signal	Microprocessor, DSPs, SRAM and hard disk

1.2 Design Challenges of HV Circuit with Low Voltage CMOS Transistor

Designing of HV circuit with low voltage CMOS transistor faces number of challenges. The physical failure mechanisms can affect the reliability of CMOS IC. Electromigration, Time Dependent Dielectric Breakdown (TDDB) and Hot Carrier Damage are common mechanisms which causes reliability issues for CMOS. The life time of IC can reduce by fabrication steps which can cause stress and may lead to latent damage. Method used for Oxide Charging, caused by injection of charge into gate oxides during certain ion etching processes, will reduce TDDB lifetime and cause some transistor degradation similar to Hot Carrier Damage. Metal Stress Migration is caused by large thermal coefficient of expansion difference between metal interconnect and inter-level dielectrics (oxides), which leads to voiding of metal lines similar to damage caused by electromigration [6].

Foundries of CMOS have taken this challenge to mitigate any physical failure mechanism that affects the reliability of CMOS IC. The target is to overcome this problem in a time span of 20-40 years. This large time span is chosen to physical wear out mechanism are governed by a stochastic process with a random distribution of failure time.

To achieve this goal, the CMOS foundries will have to dig out the physics of each failure mechanism and identify any wafer process step that may detrimentally influence each mechanism. After the wafer processing is adjusted for maximum lifetime for the each physical mechanism, the foundry develops design rules to prevent IC designers from over-stressing the devices and cause the expected lifetime to fall below foundry targets. These design rules will be embodied in the form of maximum operating voltage, transistor channel length constraints for service under certain bias conditions, maximum current per unit line width in metal interconnect, maximum current per contact or via and certain constraints upon interconnect layout of very wide metal lines. IC lifetime can

become unpredictably shorter if any failure occurs to comply with the reliability design rules. This section will describe in general terms the most common physical failure mechanism and will discuss how the foundry deals with processing design and with design rules.

I. Time Dependent Dielectric Breakdown (TDDB)

TDDB is a wear-out phenomenon of SiO_2 in CMOS gate, the gate films are becoming extremely thin and the electric field strength is getting stronger in these oxide fields. The current flow between the drain and the source meaning the gate electric field has no control to the conducting path between the gate and the source. So the TDDB lifetime is affected by the number of the defects in the gate oxide procedure during wafer fabrication. TDDB mechanism can be modeled by either Schottk or by the Frenkel-Poole emission. Both of the models have similar mathematical expression of inter-metal leakage current density which is exponentially dependent on temperature [7].

The exact reason of physical mechanism of the TDDB is still under consider. The general idea is that the driving force or the applied voltage at gate level creates defects in the volume of the oxide film. In all gate voltage bias condition TDDB occurs. The focus of the foundry is to trade off gate oxide thickness with applied voltage specification to achieve both speed and lifetime target for the technology. The total amount of charge that flows through the gate oxide by tunneling current is the lifetime of the particular gate oxide thickness [6].

II. Hot Carrier Degradation (HCD)

Hot carrier degradation causes most significant problem to ensure the reliable operation for CMOS transistor characteristic. HCD occurs due to the difficulties of minimizing the power supply voltage for the transistors which are even more shrunken. So the transistors electric field strength is increasing [9]. Hot carrier is a generic name for high energy hot electrons and high–energy hot holes generated in the transistor. The average energy gain becomes zero of the transistor when electrons and holes continually absorb and emit acoustical phonons. These electrons have kinetic energies (E) that are normally slightly higher than that of the conduction band edge (E_c) by an amount kT_r (T_r is room temperature) and for the holes, kinetic energy is slightly less than the valence band edge (E_v). In these situation two things occurs, one is low electric field and other is very high electric field. For the low electric field the carrier velocity is field independent and kT_r is small compared to the carrier kinetic energy and for very high electric field the carriers gain more energy than they lose by scattering.

In case for the metal oxide semiconductor field effect transistor (MOSFET), if the gate voltage is lower than VDS then the inversion layer becomes much stronger on the source side than the drain side and on the drain side the voltage drop due to the channel current is concentrated. So most of the carriers on drain side gains high energy between two scattering events and starts to behave like hot carriers but on the other side a small number of carriers generate electrons and holes by impact ionization as they do not gain

enough energy [9]. HCI normally occurs in the high power circuits such as DC-DC converter, power amplifier. The worst HCI bias conditions, if the drain source voltage is higher than both gate source voltage and the threshold voltage and if drain source voltage is higher than the nominal supply voltage.

Impact range of hot carrier in the transistor is high with channel length at minimum design rule length and when drain source voltage is maximum allowed voltage while the gate source voltage is near to half of the drain source voltage [10]. This HCI can be minimized by reducing the drain current or by increasing the transistor channel length.

III. Electromigration

The phenomenon of the electromigration is, when the diffusion of the metal atoms along the conductor in the direction of the current flow. This diffusion process happens because the aluminum atom will move towards the electron flow so the momentum transfer between electron and the metal atoms is also in the direction of the electron flow. In the IC design, most of cases the interconnection are done by the aluminum wire. So the aluminum ions will move towards the current flow.

As the IC technology is reducing rapidly, the interconnection which carries the signal are also reducing in size. As a result current density is also increasing. So the momentum transfer between electron and the metal atoms plays a big part in this huge current density [11]. The momentum transfer is known as electron wind force. Electron wind force activates the metal atoms and metal atoms create the electric field which drives the current. Metal atoms are positive ionized and when the metal atoms are activated the electric field starts to push them against the electron wind force. The interplay of these situations determines the direction of net mass transfer. To avoid this situation, the cross section area of the circuit can be decreased and the local resistance can be increased and the current density at that point in the metallization. So electromigration can also increase as the local current density and the temperature both are increasing [9].

1.3 Breakdown Mechanisms

The previous discussion was about the physical mechanisms which cause long-term reliability problem and results in a slow degradation of the devices. Another important mechanism is the breakdown mechanism which occurs when the bias voltages are of the devices is pushed beyond the voltage limits.

I. Junction Breakdown

The most important physical mechanism among the junction breakdown is avalanche breakdown. The large electric field mechanisms starts to active which breaks down the junction and starts to flow current in reverse direction through the junction. This happens when the electric field in a reverse biased p-n junction increases with the increasing reverse bias [12].

A pair of an electron–hole can be generated by the impact of ionization when a channel hot carrier collides with a crystal atom. If the generated electron-hole pair gets enough energy from the electric field across the channel then this electron-hole pair can maintain the impact ionization. Avalanche breakdown is then defined as the condition under which the impact ionization rate becomes infinite. As a result the reverse diode current starts to significantly as the reverse bias over the junction increases [10].

II. Gate Oxide Breakdown

Junction breakdown mechanism is a breakdown mechanism of a silicon part of the MOS field effect transistor (MOSFET). If the transistors drain-gate or gate-source voltage across the oxide exceeds the supply voltage then it is possible to occur gate oxide breakdown voltage. This kind of bias condition of the transistor first pusses for the channel hot carrier effect. If this situation stress further then the oxide degradation may be damaged [12].

1.4 Cascode Structure: High Voltage CMOS Solution

Different devices can be used to sustain high supply voltage but this come with higher cost. LDMOS and VDMOS can be used but extra mask sets and process steps are required for these devices. So the best solution will be to use standard CMOS devices in different techniques. One solution could be, using of standard CMOS devices in cascode structures so that devices can operate in high supply voltages. Figure 1-4 shows an example of cascode structured CMOS devices. Figure 1-4 (a) shows if the supply voltage of the transistor is VDD then the maximum voltage across the terminal of the transistor is VDD, which is within the limit of the technology parameter and lifetime will also be within the technology limit. If two or more transistors are placed in cascode structured then the drain of the lower transistor will be connected with the source of the upper transistors as shown in the Figure 1-4 (b). Here, the node voltage of the two stack devices is limited within the VDD but the

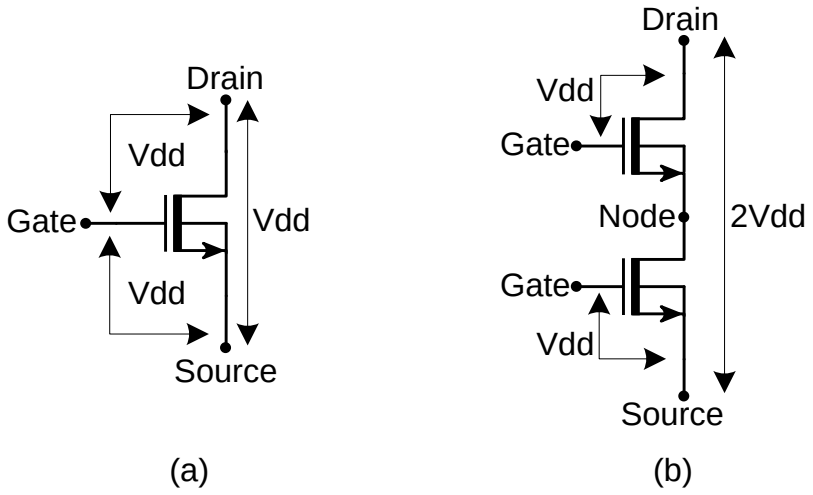


Figure 1-4: Cascode Structured Standard CMOS Devices

voltage across the drain of the upper transistor and the source of the lower transistor is now two times of the nominal supply voltage which is within the technology parameter without effecting the reliability issues and allows to operate in the higher supply voltages. Most important part of these techniques is the biasing the gate of the transistor so that the transistors terminal remains within the nominal supply voltage.

2 LC Type DCDC Buck Converter Design

In this chapter LC type DCDC buck converter for 6V design are reviewed. The switching frequency of the converter is 52 MHz. The higher operation frequency allows decreasing the inductor size of the converter. High efficiency with low output ripple are needed for the converter. By minimizing the power losses in different blocks of the converter allows higher efficiency.

2.1 Design Specification

A buck converter is designed to provide a fix output voltage for fixed input voltage with high frequency and high efficiency using 45nm CMOS technology. Low voltage transistors are used for the high voltage application. The nominal supply voltage for the designed circuit is 6V. The output voltage is chosen to be 1.25V. The detail specification is shown in the Table 2-1.

2.2 Switching Frequency Selection

The range of switching frequency of buck converter changes from several kilo Hz to several Mega Hz. Depending on the switching frequency, the size of the inductor and the capacitor changes. If switching frequency increases then the size of the inductor to produce continuous current and the size of the capacitor to limit output ripple both decrease. High switching frequency is chosen to reduce the size of the inductor and capacitor. In this design, switching frequency is chosen to be 52MHz.

2.3 Output Ripple

Inductor and capacitor filter determines the output ripple. The expression for inductor current ripple and output voltage ripple is given by equation 2.3 and 2.4 respectively. Large size filter in buck converter can achieve smaller the ripple, but it can never suppress ripple to zero. Large filter size requires larger area of the IC. Considering the trade-off between filter size and ripple amplitude, this design allows an output voltage ripple of around 10% of the average output voltage, and an inductor current ripple of around 200mA.

Table 2-1: Specification of the LC type Buck Converter

Parameter	Specification
Technology	45nm CMOS
VBAT	6V
V_{OUT}	1.25V
F_s	52MHz
Δi_L	200mA
ΔV	10%
Pin	200mW

2.4 System Architecture

This section describes the architecture block diagram of the proposed LC type DCDC buck converter. Figure 2-1 shows the proposed buck converter system. The battery supply voltage is 6V and the L_f is the filtering inductor and C_f is the filtering capacitor. The comparator is used to generate square wave of 0V to 1V. A non-overlapping switching circuit generates two output signals with delays for the level shifter and N-Driver provides controlled signal for the bottom side NMOS transistor. Level shifter generates correct voltage offset signal for the high side PMOS power transistor which was buffered through the P-Driver circuit.

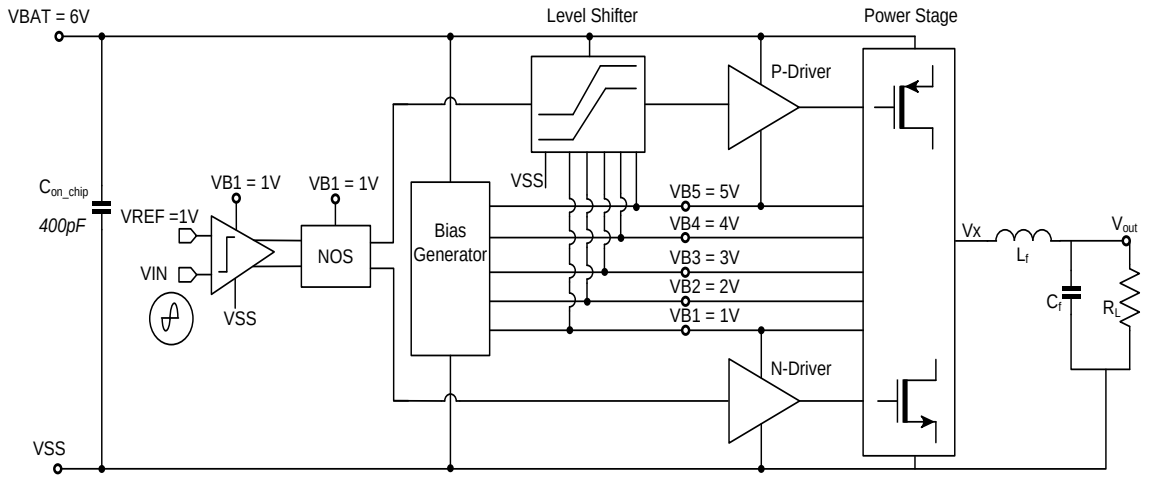


Figure 2-1: Block Diagram of the DCDC Buck Converter.

2.5 Comparator

A simple trigger circuit is used to generate the square wave signal. Schmitt trigger detects the level of the signal and provides the output signal. The circuit is designed with inverter which converts input sinusoidal into square wave signal. Duty cycle of the output signal is controlled by the circuit. The amplitude and the offset voltage of the sinusoidal input signal determines the duty cycle. Figure 2-2 shows the schematic of the comparator circuit. Figure 2-1 gives clear idea where the output of the comparator is used to provide signal to NOS circuit for generating non-overlapping signal.

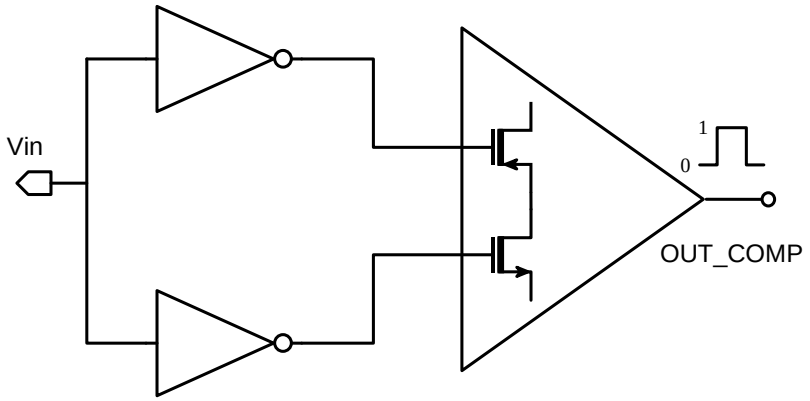


Figure 2-2: Schematic Diagram of the Schmitt Trigger

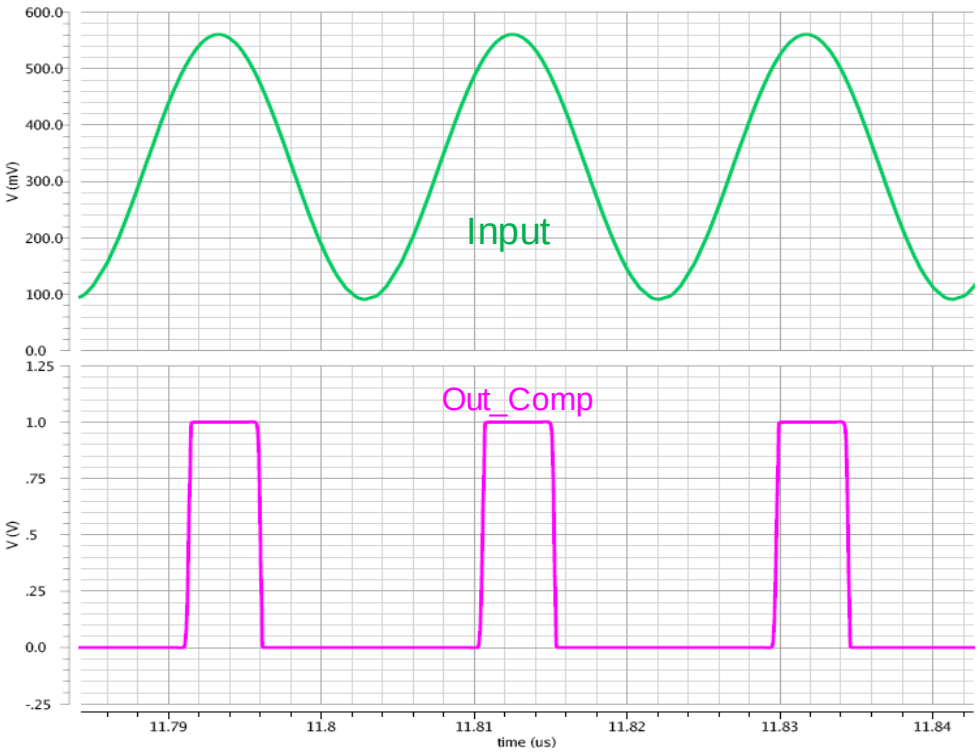


Figure 2-3: Input output characteristic of the comparator

2.6 Non-Overlapping Switching Circuit

Non-overlapping circuit allows keeping the generated signal as non-overlapping signal so the signal do not lost the charge. A simple circuit is designed where non-overlapping switching circuit generates two output signals can be constructed by using inverters, NOR gates as illustrated in Figure 2-4.

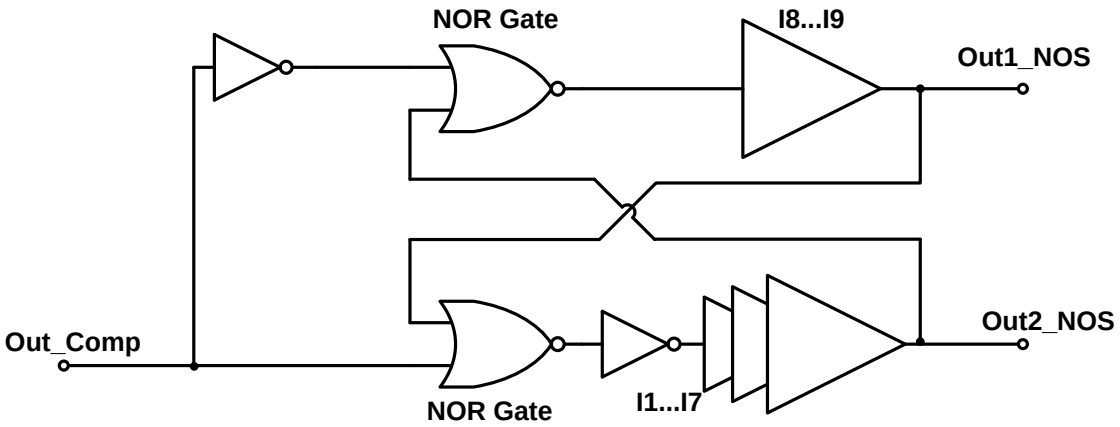


Figure 2-4: NOS circuit symbol

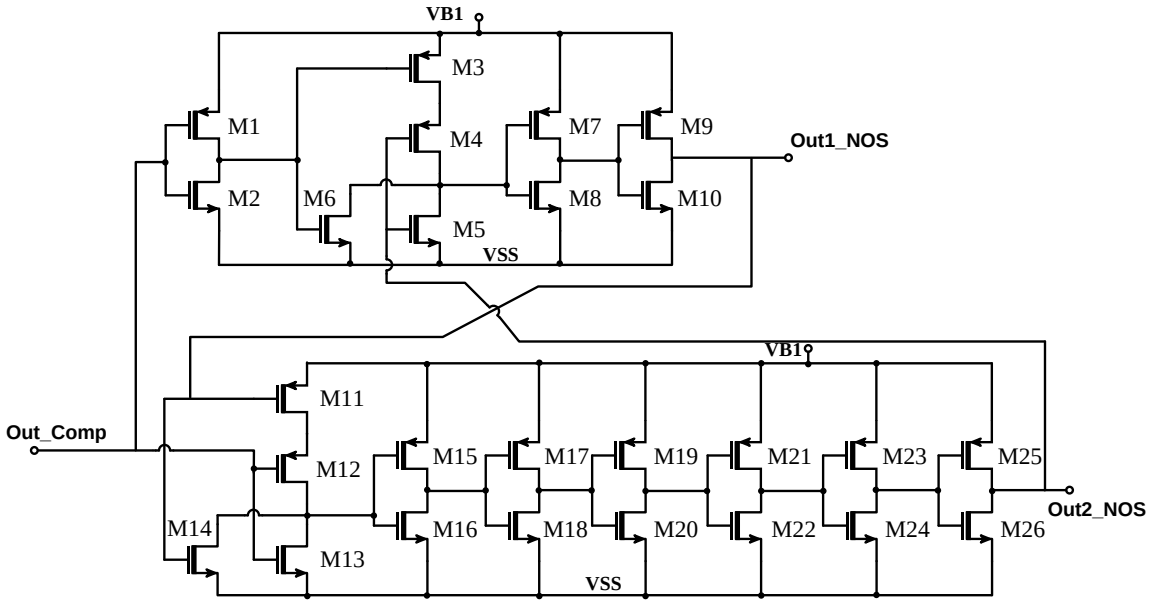


Figure 2-5: Circuit Schematic of NOS

From the Figure 2-5 it shows, number of the inverter is not same for out1_NOS and out2_NOS. Inverters are the delay element so that the two output signal out1_NOS and the out2_NOS has delay between two signals. Delay for the high to low level of the signal kept high compared to the low to high level of the signal for the design specification. This delay is called dead time of the signal. High to low delay is defined as dead time high to low DTHL and low to high side delay is defined as dead time low to high DTLH.

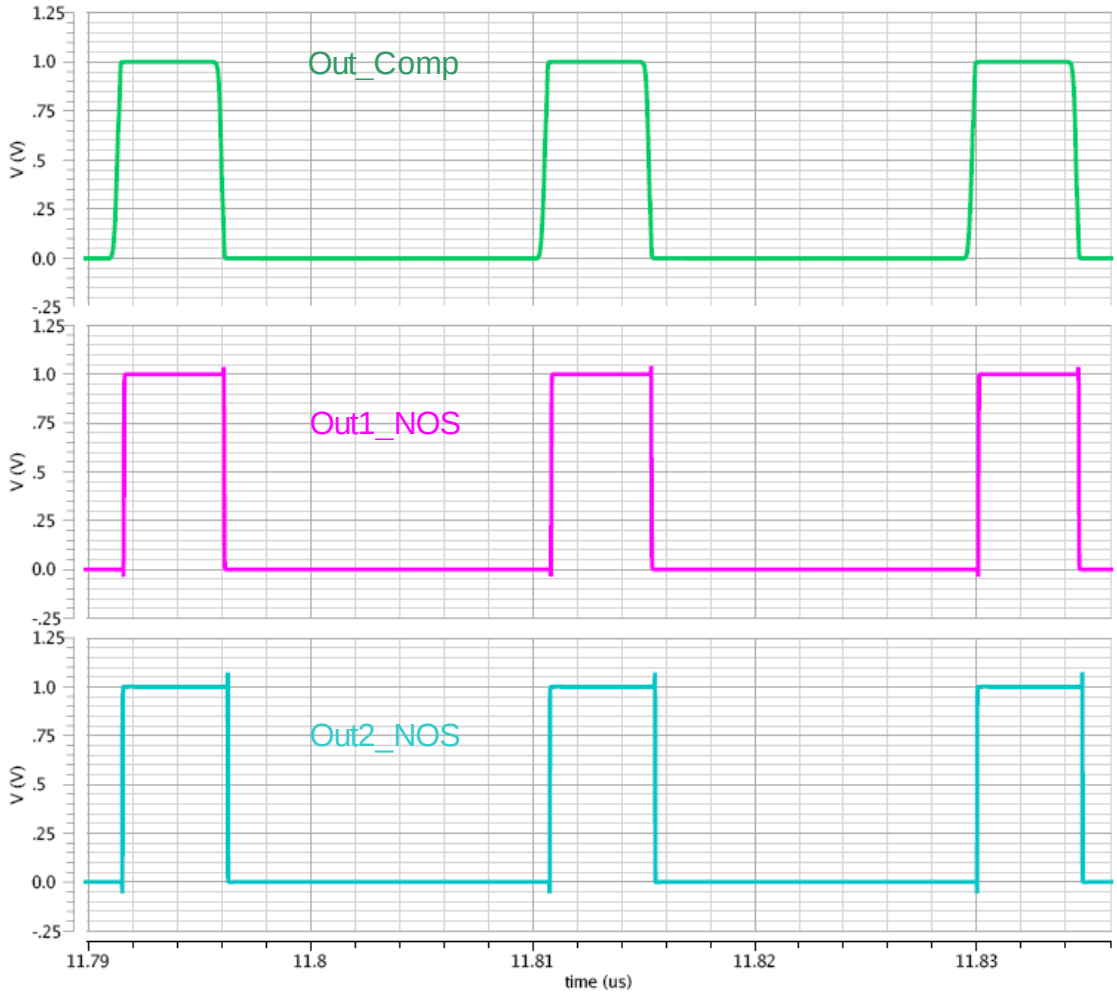


Figure 2-6: Output signal of the NOS circuit

Figure 2-6 shows the output and input signal waveform of the NOS circuit. NOS circuit generates two output signal out1_NOS and out2_NOS. Out1_NOS is the input for the high voltage level shifter and out2_NOS is the input signal for the N-Driver circuit. Duty cycle of the both signal is 23.5%. Dead time for low to high side is 89ps and for high to low side is 261ps.

2.7 High Voltage Level Shifter Circuit

Level shifter circuit is used in this DCDC converter to convert low voltage signal to the high voltage signal to drive the power stage transistor. Different types of the level shifter are presented for different application. A high voltage level shifter with fast switching speed and low rise time and fall time is design for the DCDC converter. Detail of the high voltage level shifter is discussed in the chapter 3.

2.8 Biasing Circuit

A simple biasing circuit is designed to generate the reference voltage for the DCDC buck converter. The converter requires 1V, 2V, 3V, 4V and 5V reference voltages. Figure 2-7 shows the reference voltage level for the converter.

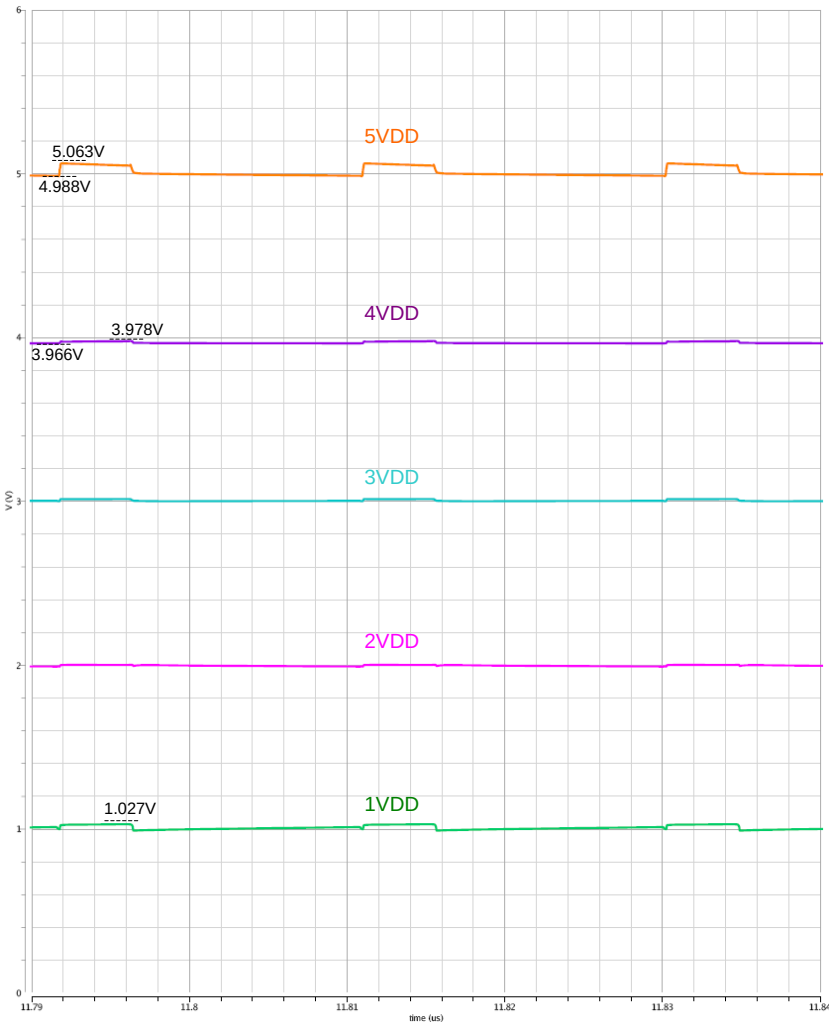


Figure 2-7: Reference voltages for the converter.

2.9 P-Driver and N-Driver Circuit

MOS inverter is used to design P-Driver and N-Driver circuit. P-Driver is placed between level shifter and the power stage. Input signal of the P-driver is the output signal of the Level shifter. N-Driver is placed between the non-overlapping switching circuit and the power stage. Driver circuit has used in the converter for the following reasons.

1. P-Driver will provide controlled signal for the high side pmos transistor of power stage and N-Driver will provide controlled signal for the low side nmos transistor of power stage.
2. Controlled signal will have higher load capacitance so that signals can drive the power stage transistor which has high gate capacitance.
3. Dead time will be controlled by the P-Driver and N-Driver.

Number of stages of the inverter depends on the input capacitance and output capacitance of the signal. Input capacitance of the P-Driver should be same as the level shifter output signal and output capacitance should be same as the gate capacitance of the high side pmos transistor of power stage. For the N-Driver, input capacitance should be same as the output capacitance of the NOS circuit and output capacitance should be same as gate capacitance of the low side nmos transistor of the power stage.

Assuming P-Driver output signal is to drive a load of C_L and input gate capacitance is C_G. For any integer $n \geq 1$, define α by the expression

$$\alpha = \left(\frac{C_L}{C_G} \right)^{1/n} \tag{2.1}$$

Alternatively, n can be represented in term of α as

$$n = \frac{\ln(C_L / C_G)}{\ln \alpha} \tag{2.2}$$

The integer number n defines the number of inverter stages. Figure 2-8 is the P-Driver circuit which generates output signal with the high capacitance signal with a high delay. The N-Driver is required design in a way so the delay between the two signals is compensated. Figure 2-9 shows the N-Driver circuit. N-Driver circuit has extra stages of inverter compare to P-Driver circuit. This extra stage allows to control the delay between the two signal of P-Driver and N-Driver. This delay in the cascade structure is defined as deed time. Delay for high to low side is defined as dead time high to low DTHL and the delay for low to high side is defined as dead time low to high DTLH.

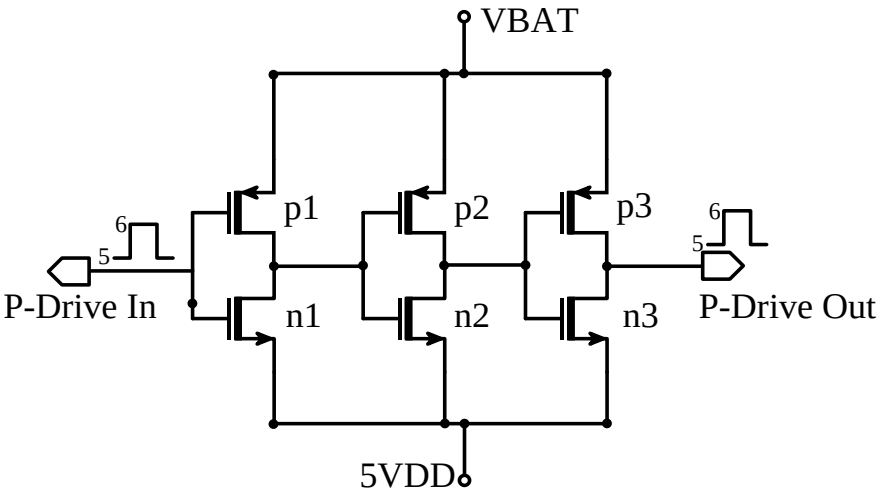


Figure 2-8: P-Driver Circuit Schematic

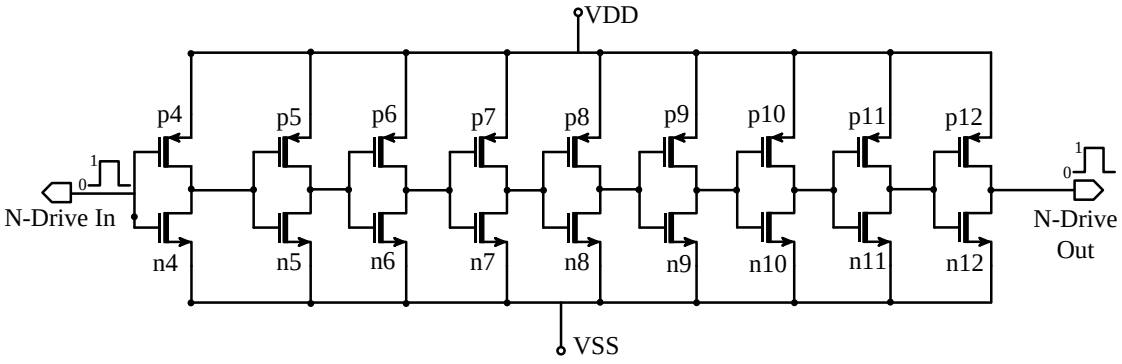


Figure 2-9: N-Drive Circuit Schematic

Figure 2-10 shows the output signal of the both P-Driver and N-Driver. Dead-time is calculated from this two output signal. The difference between the two signal from the half VDD point of the P-Driver signal to the half VDD point of the N-Driver signal in time scale for low side to high is the dead time low to high which is 162ps. Same way dead-time for high to low side is calculated. The DTHL is 163ps.

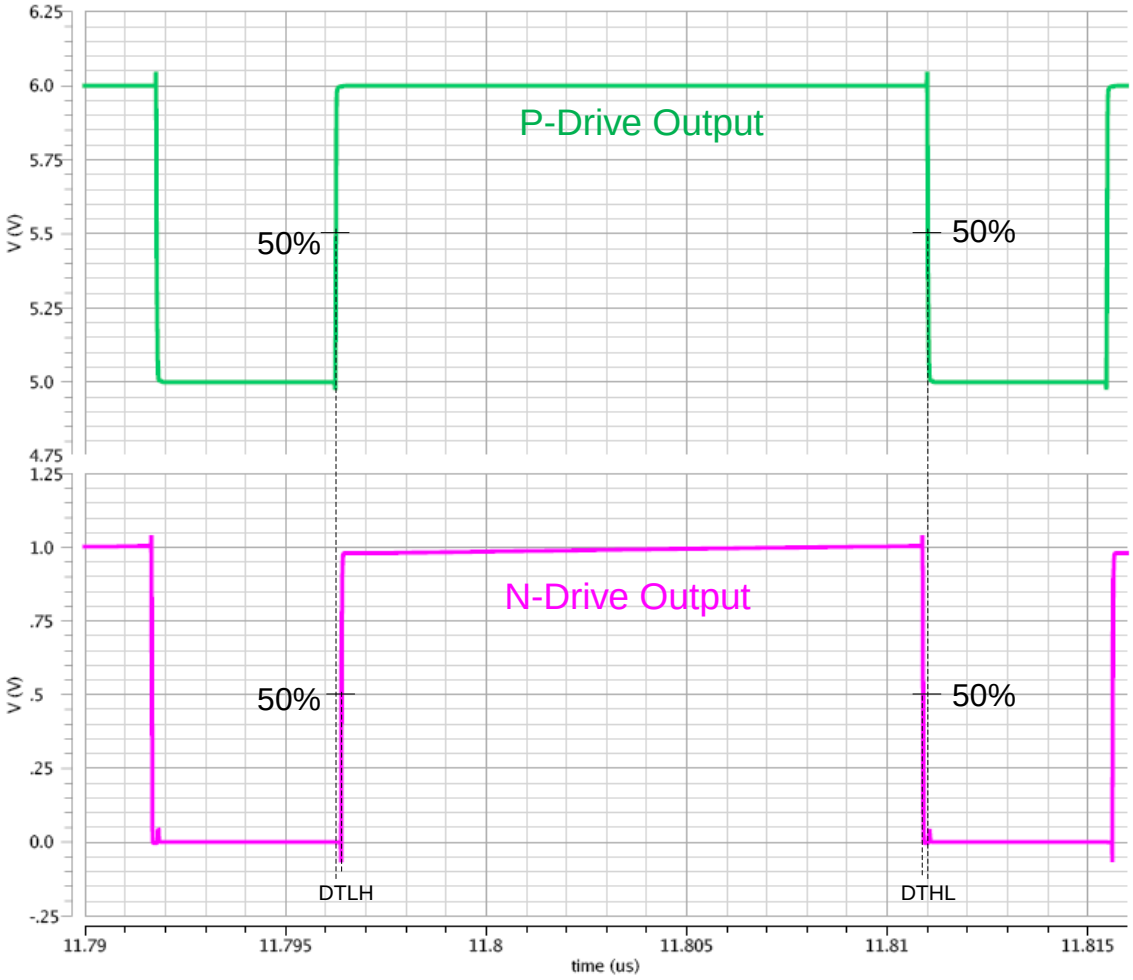


Figure 2-10: Output Signal of P-Driver and N-Driver

2.10 Power Stage

Power stage circuit is designed with cascade structure. As the battery supply voltage is 6V so the six stage cascode transistor is used where each transistor has nominal supply voltage of 1V. The output signal of the P-driver and N-driver circuit with controlled dead-time and high load capacitance is connected with the P1 and N1 transistor respectively. Figure 2-11 illustrates the power stage circuit.

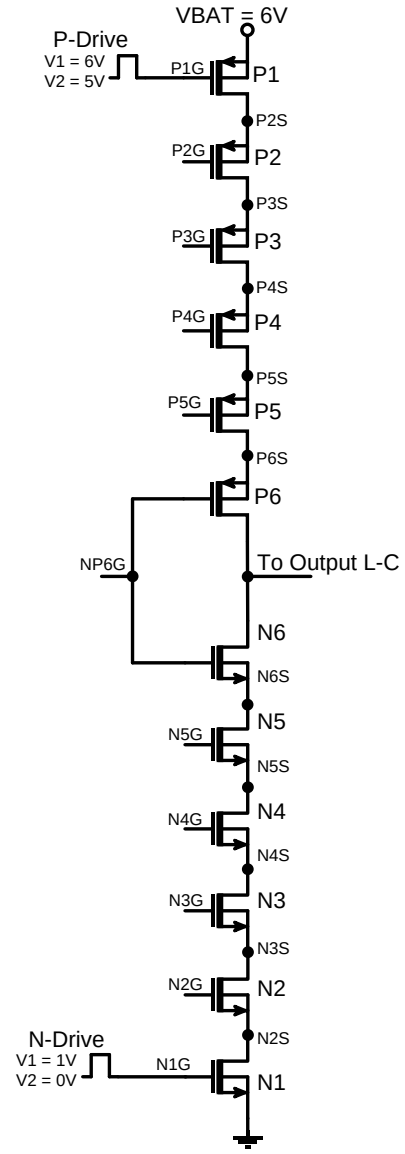


Figure 2-11: Circuit diagram of the power stage

2.11 Output Filter Design

A rectangular wave is generated by the power stage at output node Vx. The output signal is passed through the second order low pass output filter of the Buck converter circuit. The filter is designed with inductor Lf and capacitor Cf which passes the desired DC component of Vx(t) while attenuating the AC component to an acceptable ripple value. The load resistor RL draws the DC current I0 from the output LC filter. Figure 2-12 is figure of the output filter designed for buck converter.

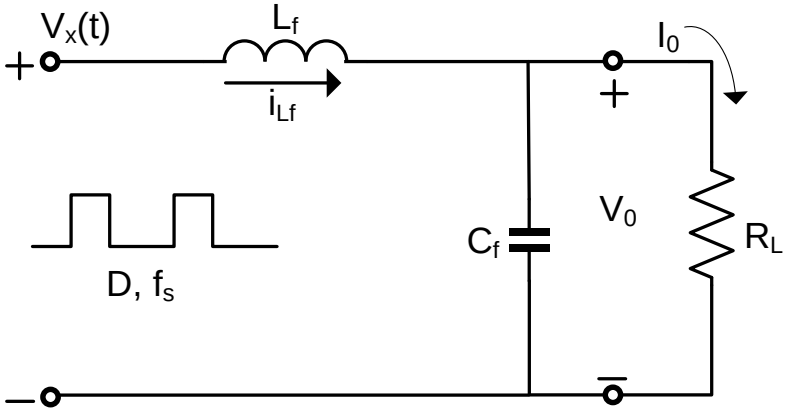


Figure 2-12: Output Filter of the Buck Converter

The large attenuation is required in a practical power circuit where $\omega_s^{-2} \gg L_f C_f$, here $\omega_s = 2\pi f_s$ and f_s is the switching frequency. The inductor value can be chosen based on the current ripple ΔI [13],

$$L = \frac{V_0(1-D)}{\Delta I f_s} \tag{2.3}$$

The filter component is sized based on the time domain analysis. By neglecting the output voltage ripple for a rectangular input with period T_s. The inductor current waveform is triangular with period T_s and peak to peak current ripple ΔI is symmetric for the load current I_0.

The output capacitor is selected in a way to meet the voltage ripple specification where to ensure the impedance at the switching frequency including the equivalent series resistance so it is small relative to the load impedance. Depending on the voltage ripple ΔV requirement, the capacitor value is calculated by [13],

$$C = \frac{V_0(1-D)}{8L_f f_s^2 \Delta V} \tag{2.4}$$

The output voltage of the converter has overshoot and undershoots voltage during the load transient because of the equivalent series resistance of the output capacitance. This voltage is given by

$$\Delta V = \frac{\Delta i_c . \Delta t}{C} + \Delta i_c . ESR \tag{2.5}$$

So the lower ESR values are preferred for the overshoot and undershoot voltage. The output filter is used as an off chip component to minimize the effect. The multilayer ceramic capacitor has low ESR and also smaller in size.

Equation 2.3 and 2.4 describes two main principle of miniaturizing a DC-DC converter. First, higher switching frequency will reduce the inductor and capacitor value results in a smaller converter. Second, the requirement of interest is output voltage ripple depends on the product of the inductor and capacitor value rather than the individual component value. Table 2-2 illustrates the output filter component detail.

Table 2-2: Output Filter Component Detail

Component	Value	Model	Parasitic Resistance
L_f	100nH	MLZ1608DR10DT000	143mΩ
C_f	100nF	C0510X6S0G104M030AC	15.5mΩ

The simulated waveforms of the buck converter are presented in Figure 2-13. The converter operates with an input voltage V_{BAT} = 6V, while producing 1.25V output voltage over 9Ω load and I_{out} = 200mA output current. All the simulation results in this chapter presented without parasitics.

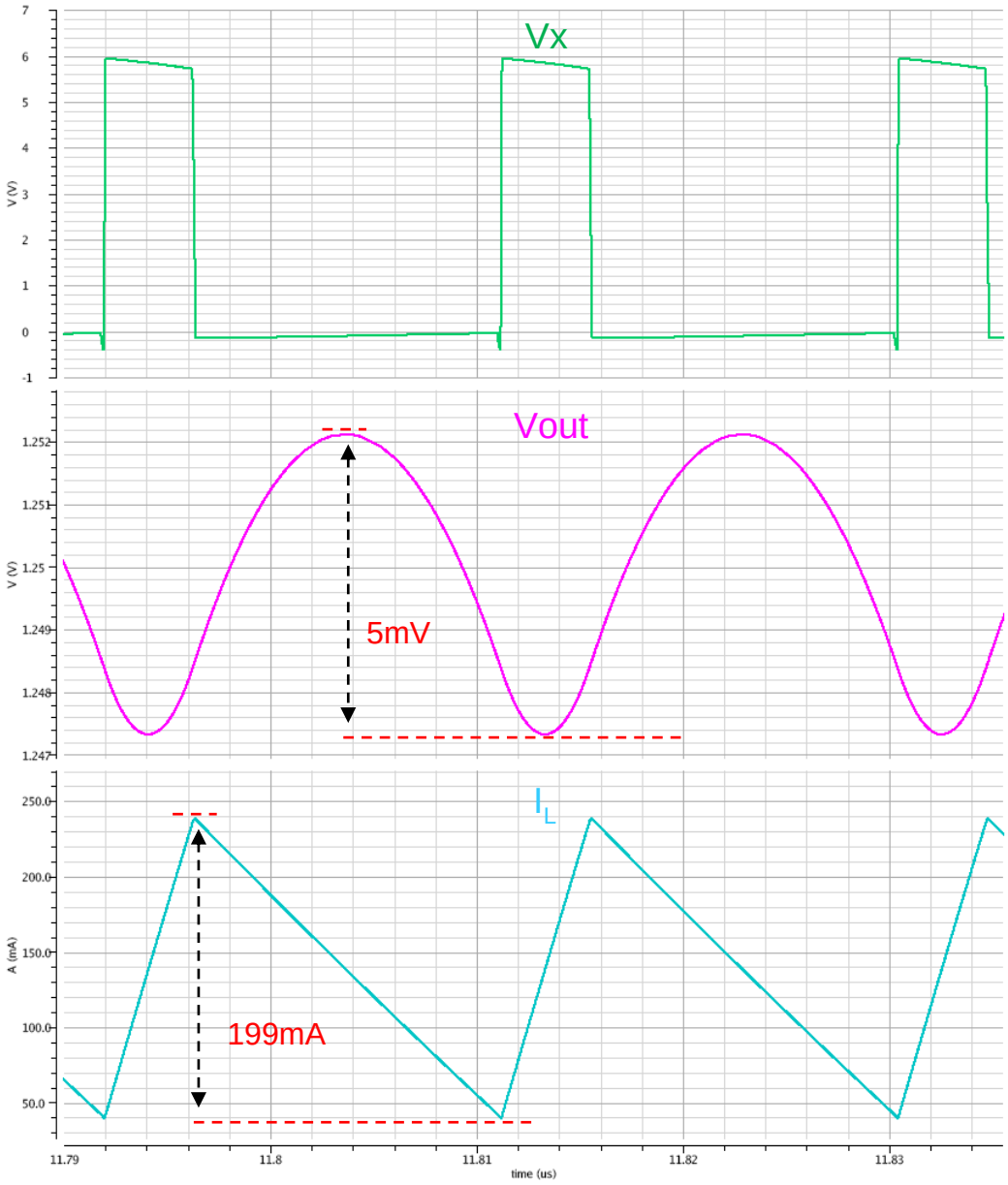


Figure 2-13: Simulated steady-state waveforms of the DCDC Converter circuit Output signal of the power stage at f_s=52MHz, V_{BAT}=6V, V_{out}=1.25V, I_{out}=200mA.

3 HV Level Shifter Design, Simulation and Layout

Level shifter is an important building block in the power management system. In the DC-DC buck converter, level shifters are used to convert low voltage signal to high voltage signal for the high side P-driver. Level shifters help to reduce the swing of the gate drive voltage and allow increasing the efficiency of the buck converter. Buck converters require a control signal with very low rise and fall time.

3.1 Conventional Cascode Structure Level Shifter Circuit

The conventional level shifter can provide the required level of high level signal but the speed of the circuit is not sufficient for the high speed circuit. Conventional level shifter is capable to operate in low speed. Another problem of the conventional level shifter is the driving capability of the output signal for the high level signal for the high side. Output signal of the level shifter will be discharged by the high side PMOS transistor. Discharging of the output signal is sub-linear and for that the output cannot be fully discharged because of the threshold loss of the high side PMOS transistor [14].

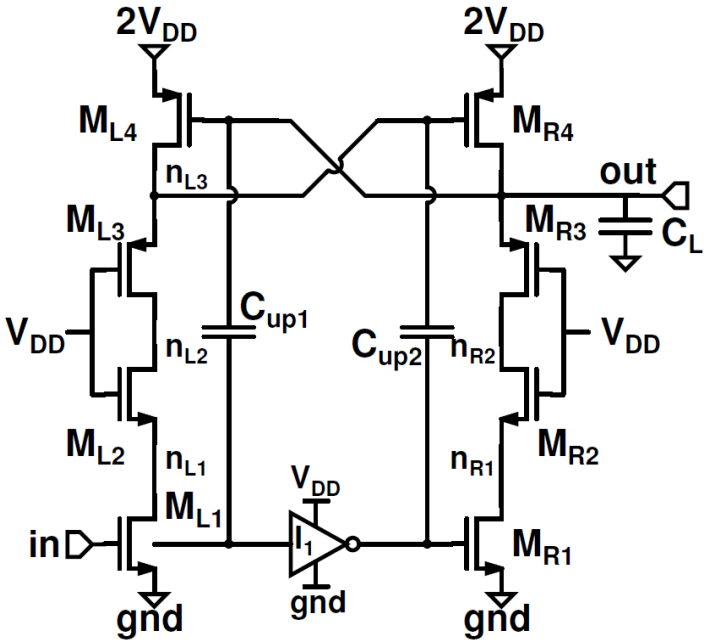


Figure 3-1: A conventional Level Shifter Circuit [15].

Figure 3-1 shows a conventional level shifter circuit in cascode structure which is capable of providing output signal of one VDD offset. In the conventional circuit, if more cascode structured is added then the circuit becomes slow and rise time and fall time of the circuit increases. Cascode structured transistors breakdown mechanism will also

affect the circuit. Breakdown voltage of the transistor is 1V so each transistor should operate within the breakdown voltage.

3.2 Standard Cascode Structure Level Shifter Circuit

Presented conventional cascode level shifters speed is not enough to operate in high speed as both capacitor cup1 and cup2 needs time to charge up and provide the signal to the PMOS transistor. So to increase the switching speed of the transistor, capacitor cup1 is omitted and inverter is placed between the gates of the PMOS transistor [16]. This two transistor MR4 and ML4 is coupled up or down by the factor of ΔV.

$$\Delta V = \frac{C_{up}}{C_{up} + C_{par}} \times VDD \tag{3.1}$$

Depending on the ΔV node nL3 and output couples up or down. Here the Cup2 act as a voltage divider between the inverter I1 and I2. C_{par} is the parasitic capacitance of the transistor MR4, inverter I2 and node nL3 for Cup2. These capacitors increase the switching speed for the transistor MR4 and ML4.

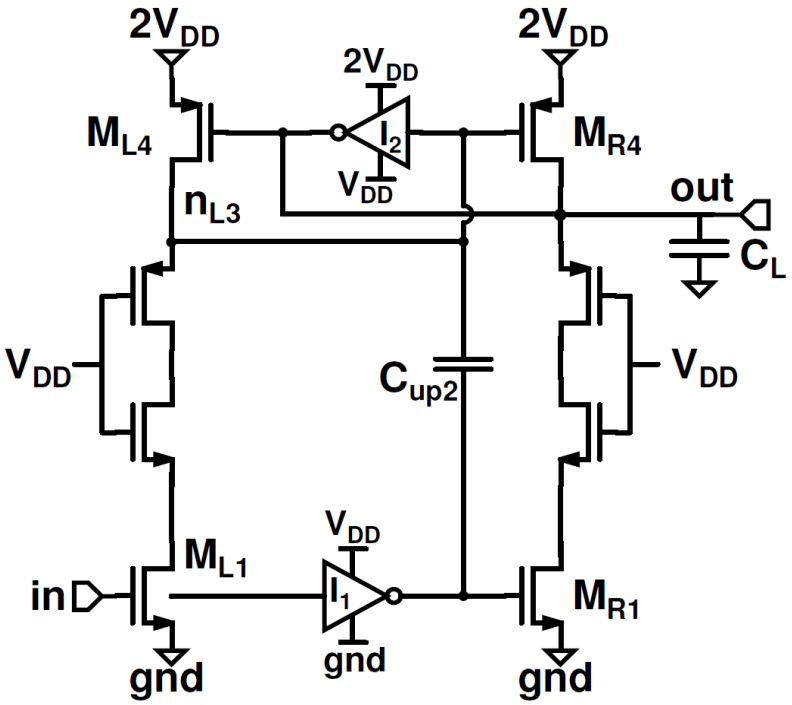


Figure 3-2: Standard Cascode Structure Level Shifter Circuit

The transistor are placed in cascode structured should operate within the technology parameter. The technology used in the [16] is 1.2V transistors so every transistor used in the circuit should operate with in 1.2V so that the breakdown voltage can be prevented. Transistor used in this work is 1V, 45nm CMOS technology. So every transistor should operate within the technology parameter used.

3.3 Modified Cascode Structure Level Shifter Circuit for one VDD offset

Breakdown voltage of the transistor is an important issue for the cascode structured circuits. Transistors drain-source voltage should be within the technology parameter but in cascode structure, transistors switching timing is different so when one transistor is off the source voltage of the transistor still goes up. As a result the drain-source voltage also increases. To control this breakdown voltage, resistor is used to control the voltage across the source and drain terminal of the transistor. For the three stack transistor structure, resistor can control the source and drain voltage so that the each transistor is one third of the drain source voltage [17]. On the other hand these resistors will allow DC leakage current to flow from the gate to drain through the resistor. This DC leakage current will increase more depending on the circuit characteristic.

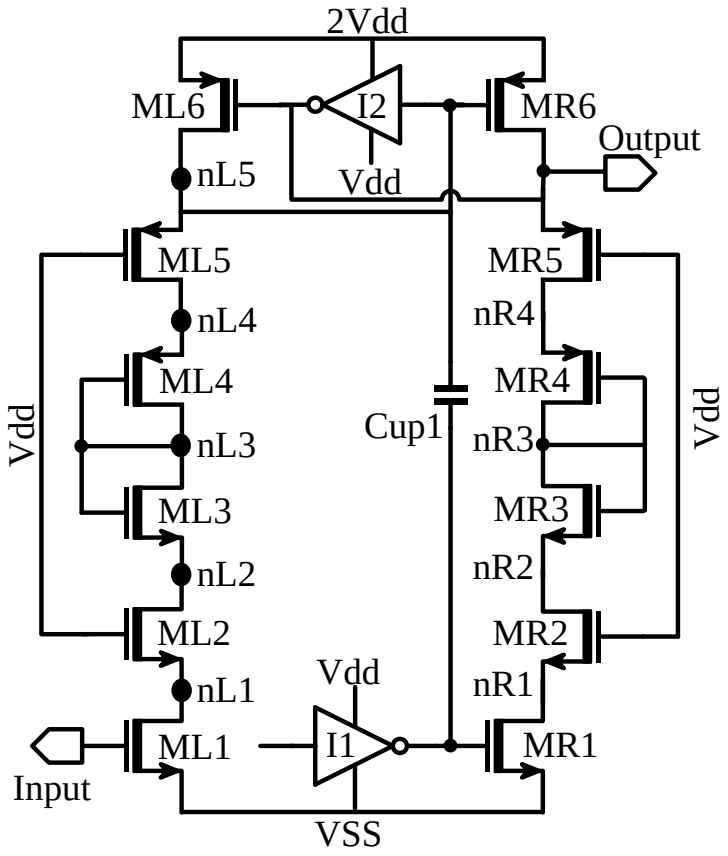


Figure 3-3: Modified Level Shifter for one VDD offset.

Figure 3-3 shows the modified level shifter for very low voltage transistor in high voltage operation. All transistor used in this circuit has breakdown voltage of 1V. When the input signal is low, the NMOS transistor M_{L1} is switches off. At the same time M_{R1} transistor is switched on because of the Inverter I_1. Inverter I_1 inverts the input signal and changes the state of the input signal. So when n_{L1} is pulled up to VDD at the same time n_{R1} is discharged to ground. When the node n_{L1} is pulled up to VDD, transistor M_{L2} is switched off as gate voltage of the transistor is biased with VDD and node n_{L2} is now charged to maximum voltage of 2VDD. At the same time n_{R1} is low and transistor M_{R2} is on so the node n_{R2} voltage goes to twice of VDD as the transistor M_{R2} gate voltage is fixed VDD. The transistor M_{L6} is switched on when the input signal is low as the input signal is almost immediately drive to the gate of the transistor M_{L4}. Now the node n_{L5} is charged to 3VDD. Transistor M_{L3} and M_{R3} is also biased at fixed voltage of VDD, so both the transistor switches on and off respectively. As the node n_{L5} is pulled up so the M_{L5} transistor is switched on and node n_{L4} is also pulled up to 3VDD. Transistor M_{L3} and M_{L4} is placed between the two cascode NMOS and PMOS to prevent voltage headroom [5]. This diode prevents the drain voltages to pull down more than the diode voltage drop and allows the transistors to operate within the breakdown voltages. Presented modified level shifter is capable of providing output signal of one VDD offset and operates within the technology parameter of 1V.

3.4 Modified Cascode Structure Level Shifter Circuit for two VDD offset

In the presented level shifter circuit Figure 3-4 can provide output voltage of two VDD offset. One extra transistor is added in the transistor cascode structure and extra supply voltage is also added and output voltage of two offset is achieved. The presented level shifter transistor breakdown voltage is also 1V like the previous circuit. Same technique is used to prevent the transistor breakdown voltages in Figure 3-3. The operation of the circuit is also same like one voltage offset circuit. Now the circuit has three cascode transistors so the transistor should operate with the technology parameter.

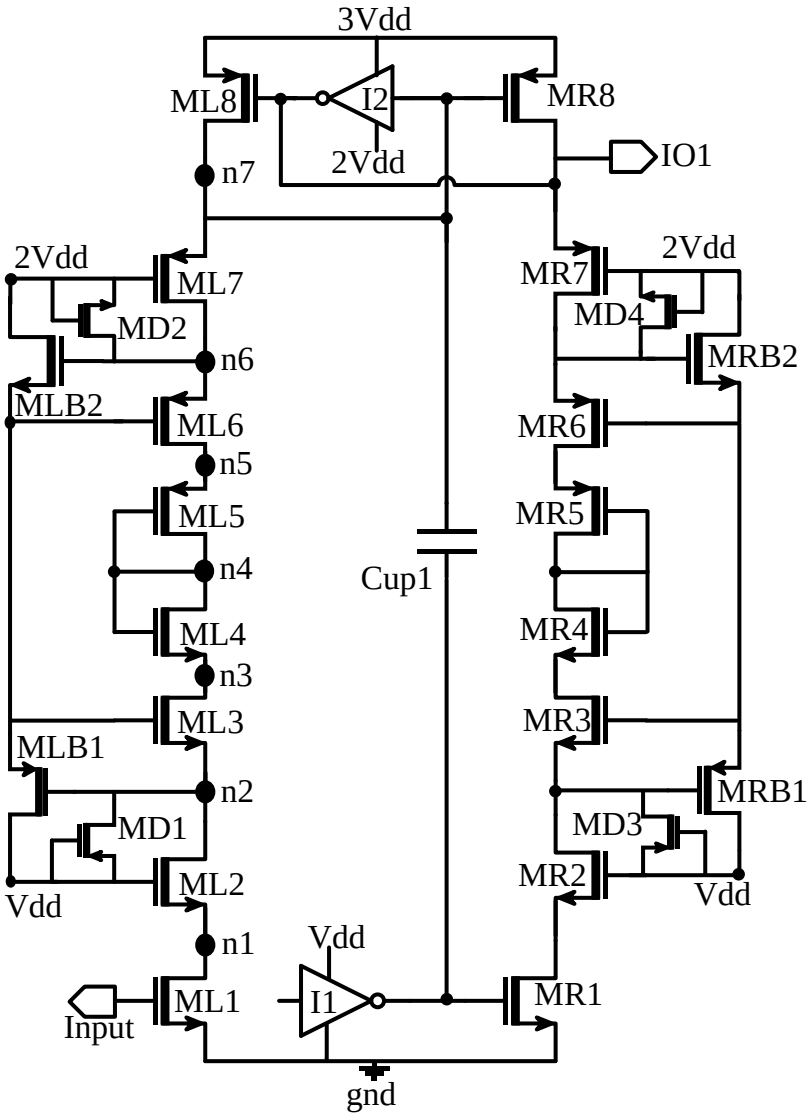
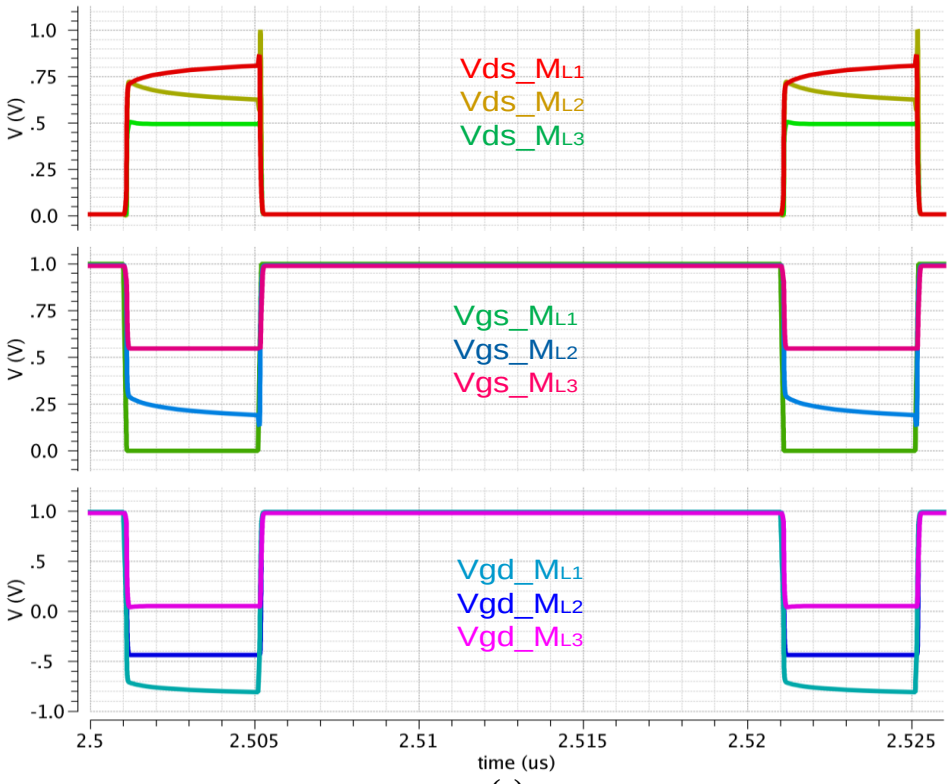
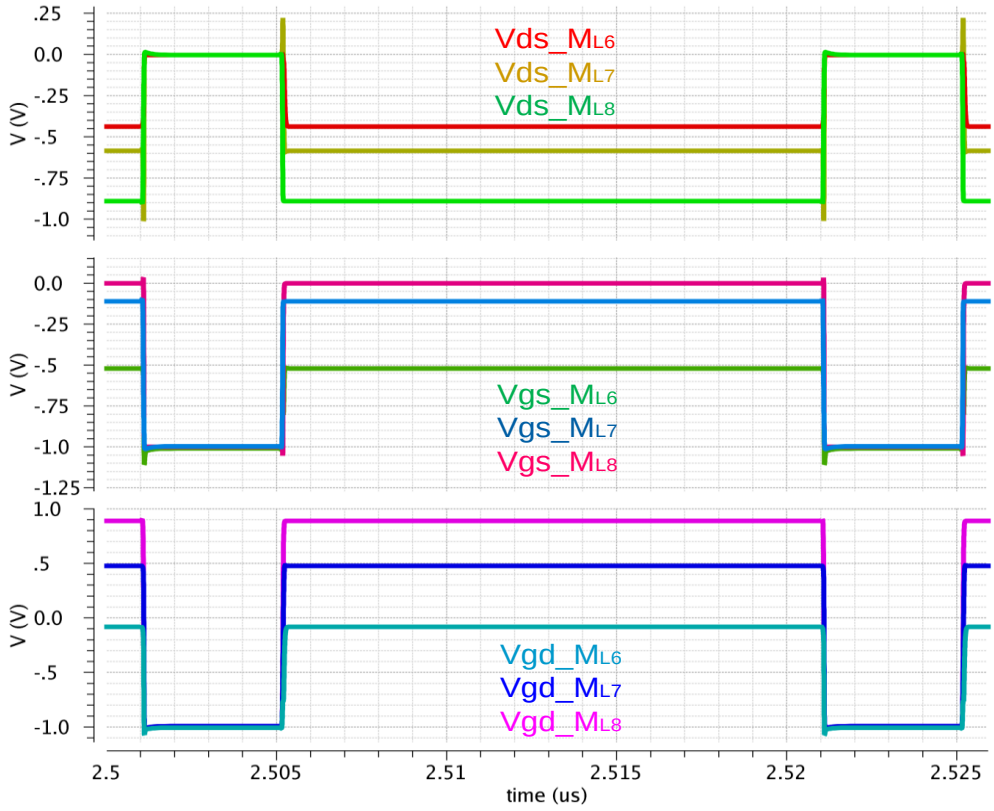


Figure 3-4: Modified Level Shifter Circuit with an offset of two VDD

If the input signal changes from VDD to ground, the NMOS transistor M_{L1} will switch off and at the same time transistor M_{L8} will change the state which means transistor will switch on. As the transistor changes the state, node voltage n_{L1} and n_{L7} will change respectively to VDD and 3VDD. Transistor M_{L2} is biased at fixed voltage of VDD- V_{tn1} and transistor M_{L7} is biased at 2VDD. So the off state of the transistor M_{L2} causes the node n_{L2} to pull up to 2VDD-$V_{tn1,2}$ and at the same time transistor M_{L7} goes to on state and node voltage is at 3VDD. Diode M_{D1}, M_{D2} connected with the transistor M_{L2} and M_{L7}. This diode prevents the drain voltages to pull down more than the diode voltage drop and allows the transistors to operate within the breakdown voltages. The transistor M_{LB1} is switched off as the node n_{L2} is charged. Transistor M_{L3} and M_{L6} are need to be biased at fixed voltage 2VDD, which is done by the transistor $M_{LB1,2}$. So the transistor breakdown voltage is also prevented. The off state of the M_{L3} transistor will pull the node voltage at 3VDD-$V_{tn1,2,3}$ and on stage of the transistor will M_{L6} will keep the node n_{L5} at ground. The transistor M_{L4} and M_{L5} acts as a diode, placed between the cascode structure of PMOS and NMOS will provide voltage headroom to set off the transient voltage peaks across the cascode transistors in order to ensure reliable operation [16]. The same operation will occur in the right side of the cascode structured transistors.



(a)



(b)

Figure 3-5: Simulation Result of the V_{ds}, V_{gs} and V_{gd} of (a) Transistor ML1 to ML3 (b) Transistor ML6 to ML8

Figure 3-5 shows the transient simulation of the high voltage level shifter at 52MHz. The design the circuit and simulation result of the level shifter presented based on the GPDK 45nm CMOS Technology. Transistors drain-source, gate-drain and gate-source voltages are presented. The breakdown voltage of the transistor is 1V. The simulation result shows that the breakdown of the gate oxide for the transistor is prevented and hot carrier generation is minimized. Figure 3-6 presents the node voltages of the level shifter. Node nL1, nL2 and nL3 are the node voltage of the NMOS cascode structure transistors and node nL5, nL6 and nL7 are the node voltages of the PMOS cascode structured transistor.

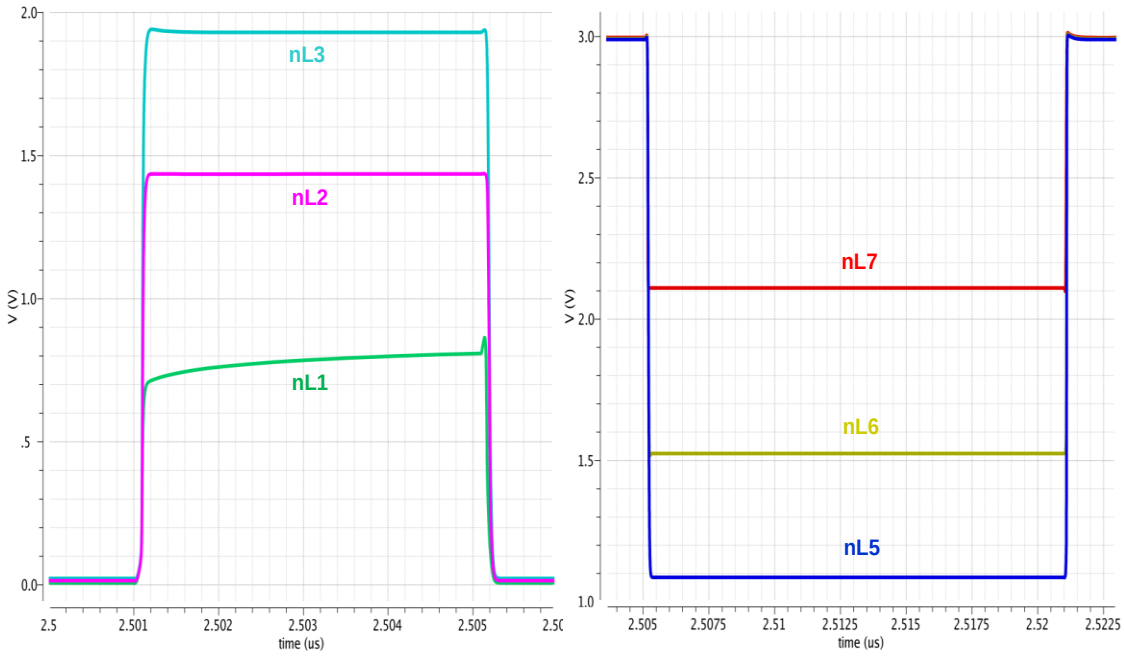


Figure 3-6: Node Voltages of the High Voltage Level Shifter

3.5 High Voltage Level Shifter Circuit for five VDD offset

Presented Figure 3-7shows a high voltage level shifter which provides an offset of five VDD output signal. The presented level shifter has three stages where first and second stage of the level shifter provides two VDD offset each and third stage has one VDD offset output signal. Output signal of the first stage is the input signal of the second stage and output signal of the second stage is the input signal of the third stage of the level shifter. Output signal of the third stage HV level shifter provides five VDD offset.

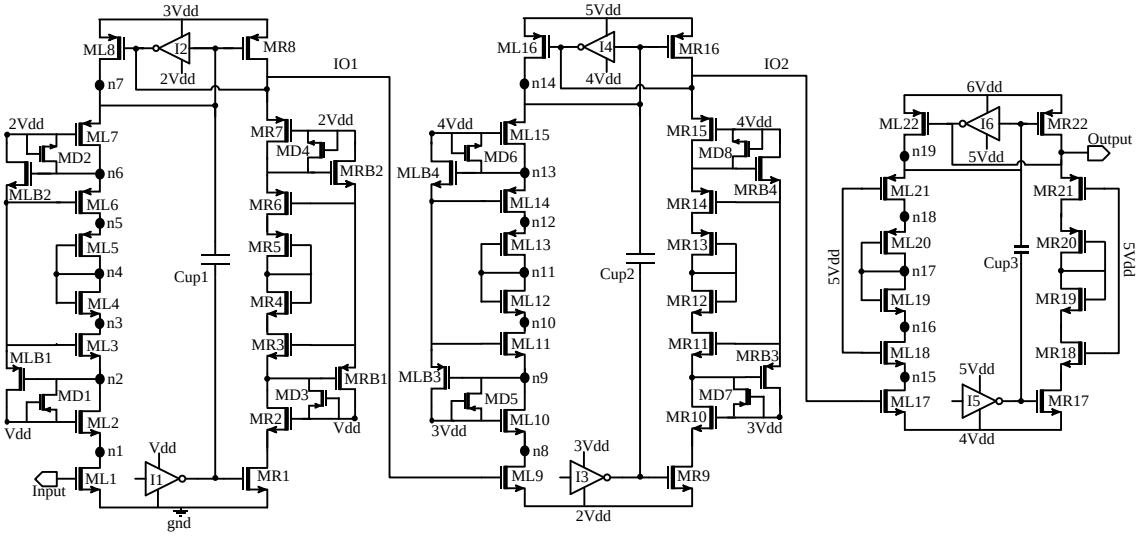


Figure 3-7: High Voltage Level Shifter with six VDD offset

Presented high voltage level shifter has an output signal level of six offset. Figure 3-9 shows the input-output characteristic of the level shifter. Output signal is shifted six times of the input signal. Delay of the signal is calculated form the half VDD point of the input signal to half VDD point of the output signal. Delay of the output signal is considered for the both high to low and low to high. Figure 3-8 shows the test bench of the high voltage level shifter. Simulation was set up for battery voltage 6V and VDD 1V, switching speed is 52MHz with duty cycle of 25%.

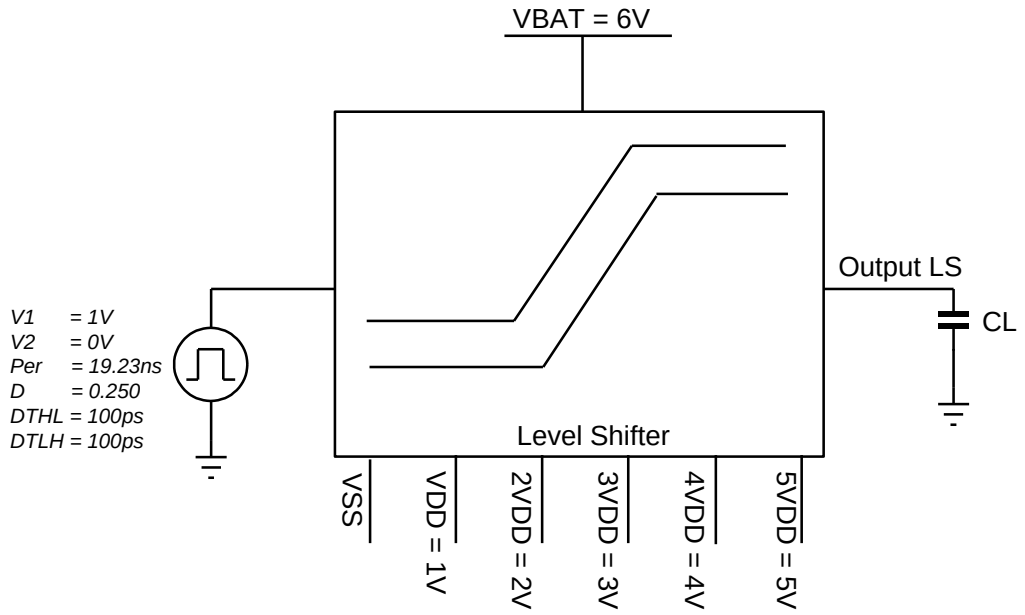


Figure 3-8: Test Bench of HV Level Shifter

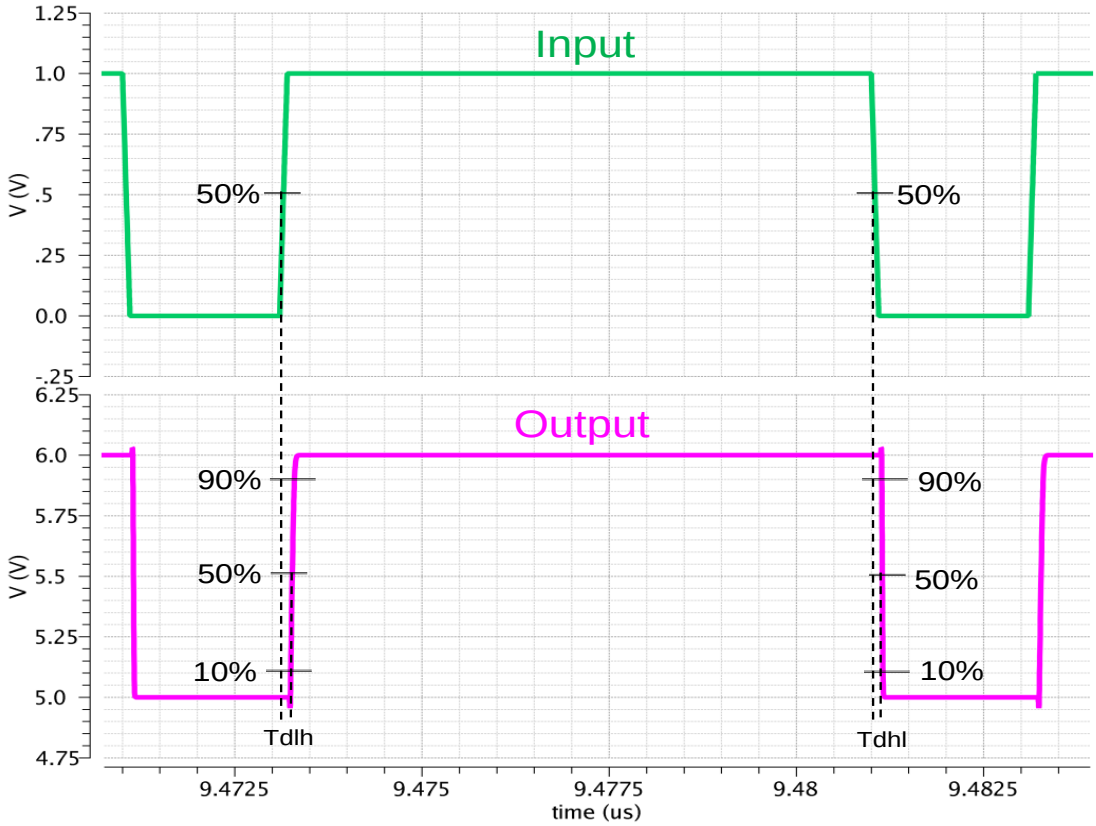


Figure 3-9: High Voltage Level Shifter Input-Output Characteristic

Figure 3-9 shows the input output characteristic of the HV level shifter for the five VDD offset. When the output signal goes from low to high, 10% of $V_{DD}+V_{low}$ to 90% of $V_{DD}+ V_{low}$ point is the rise time and when output signal goes from high to low, 10% of $V_{DD}+V_{high}$ to 90% of $V_{DD}+ V_{high}$ point is measured for the fall time. The rise time is defined as τ_r and the fall time is defined as τ_f.

Input signal of the circuit is a square wave of 52MHz with gnd and VDD as low and high voltage is applied. Supply voltage VDD is equal to 1V. Delay of low to high and high to low are 117.4ps and 97.76ps respectively. The rise time is 48.99ps and fall time is 16.13ps. The circuit is analyzed for every corner condition and the results are shown in Table 3-1.

Corner analysis is used to find the effect of process variation on the circuit. Here the result of Slow-Fast, which means slow NMOS and fast PMOS is same as typical-typical and monte carlo analysis result.

Table 3-1: Corner Analysis of Level Shifter

Analysis	T_{dlh} [ps]	T_{dhl} [ps]	τ_r [ps]	τ_f [ps]
FastFast	98.12	84.32	40.37	14.56
Slow-Slow	142.8	114	61.12	18.3
Fast-Slow	119.4	100.3	55.07	15.86
Slow-Fast	117.4	96.16	44.43	16.7
Monte Carlo	117.4	97.76	48.99	16.13
Typical-Typical	117.4	97.76	48.99	16.13

3.6 Layout Design

The layout design procedure is performed in this chapter. Cadence Virtuoso Layout Designer is utilized for the layout design. Cadence Assura RCX is used to take care of the Layout Versus Schematic (LVS) and Design Rule Check (DRC) [24]. Parasitic extraction is performed using Cadence Assura RCX.

Layout design guidelines

The tips given below are strictly considered in layout design. Floor plan is made based on these ideas and the shapes of output inductor and decoupling capacitors are well arranged to save silicon area.

- The overall layout area should be as small as possible
- Wires should be wide enough to carry the high current flowing through the converter. Multiple metal layers are used to achieve small series resistance if necessary
- The number of through-hole vias used for interconnection between different metal layers should be as large as possible
- Capacitor should be well shaped to fit the converter design
- Distance from the clock signal pin to the buffer drivers should be arranged in such way that the timing errors caused by the propagation delay are as small as possible

3.7 Layout design of The Level Shifter

Although the capacitor consume most of the silicon area, their layout design procedures are relatively simple compared to those of cascoded transistors and gate drivers. To simplify the design procedure, the idea of Unit-Cell transistor is implemented. Similar idea is also utilized in the capacitor designs.

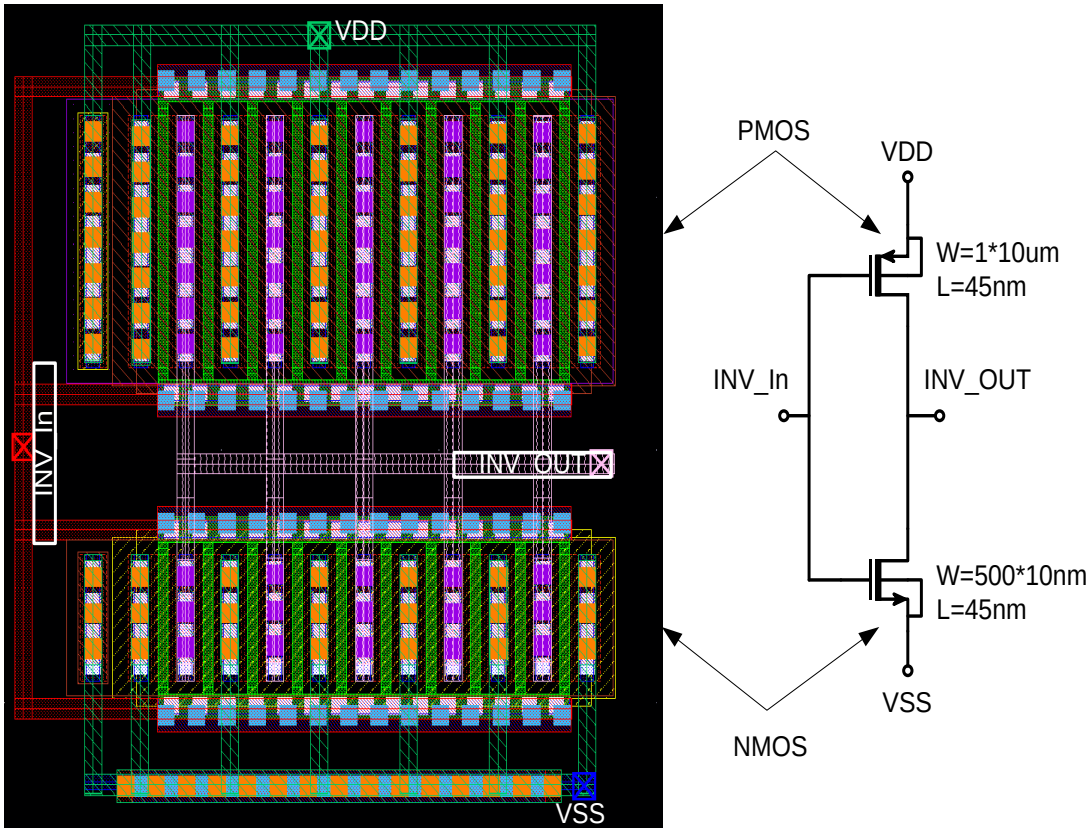


Figure 3-10: An inverter with NMOS and PMOS transistor. The size of the PMOS transistor is 1um finger width with 10 fingers and NMOS transistor is 500nm finger width 10 fingers.

An inverter with NMOS and PMOS transistors is shown in Figure 3-10. Both NMOS and PMOS transistors have ten identical fingers with 500nm and 1µm widths respectively. By dividing a 10µm transistor into ten fingers, the overall gate resistance is effectively decreased.

Figure 3-11 presents an inverter with NMOS and PMOS transistors. It consists of 15 identical NMOS segment and PMOS segments (see Figure 3-11). Metal layer 3 is used to connect the source of the transistor and metal layer 4 is used to connect the drain of the transistor which allows to reduce the parasitic resistance of the interconnection.

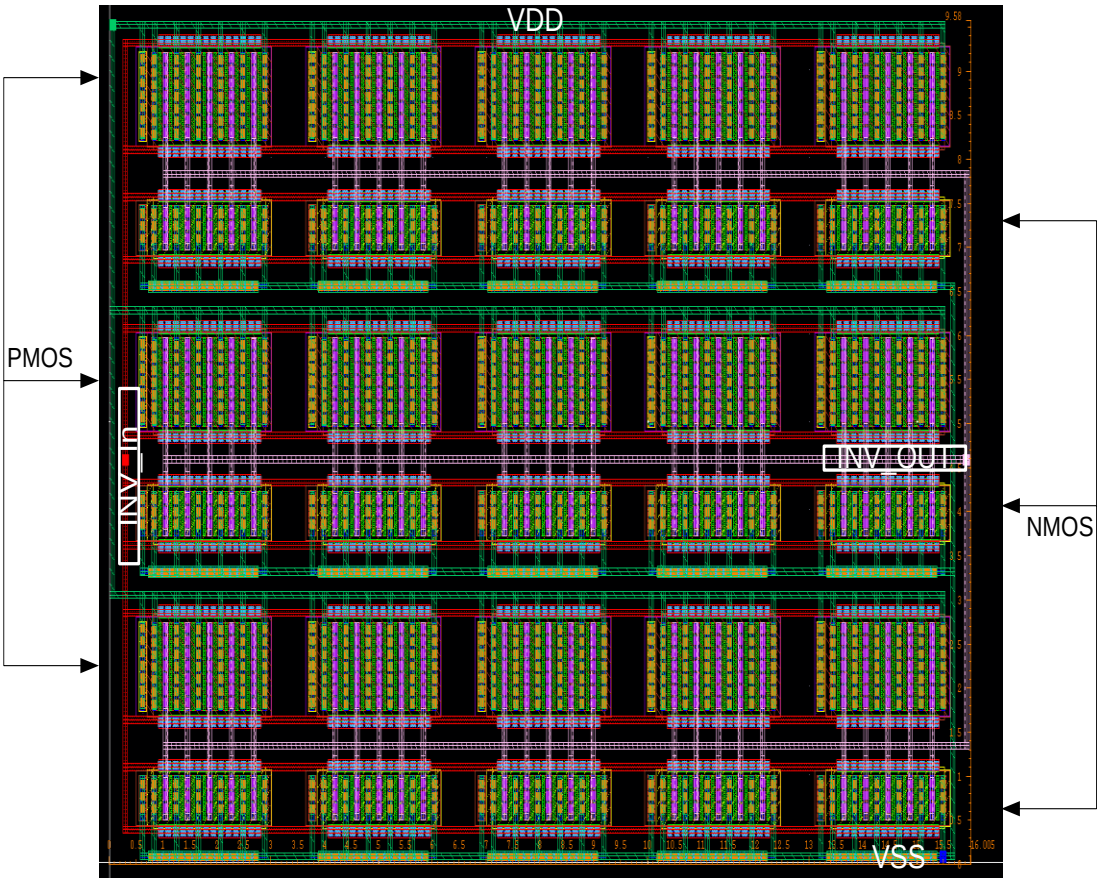


Figure 3-11: An inverter with NMOS and PMOS transistor. Both the transistor consists 15 identical PMOS and NMOS segment, which makes an overall transistor width of 150µm for PMOS and 75µm for NMOS transistor.

MIM capacitor is used to design a 5pF capacitor. Usually this type of capacitor has the highest Q-value and quite low capacitance density. Special shapes can be adopted for increasing the capacitance density. Available metal layers are used. MIM capacitor can be arranged in either lateral or vertical or combination of both ways.

The length and width of a single capacitor is limited to 5.6µm. So to design a big capacitor of 5pF, capacitor should be divided to become a unit capacitor. The maximum capacitance for a single MIM capacitor is 37.576fF. Therefore, C_{UNIT} should be less than 37.576fF. Moreover, multiplier is chosen so that an almost square capacitor is obtained (m=12x12=144). Figure 3-12 shows a MIM capacitor of 5pF of 144 multiplayers with less than 37.576fF capacitance of single unit.

$$C_{UNIT} = \frac{C_{TOTAL}}{m} = \frac{5pF}{144} = 34.76\,fF \leq 37.567\,fF$$

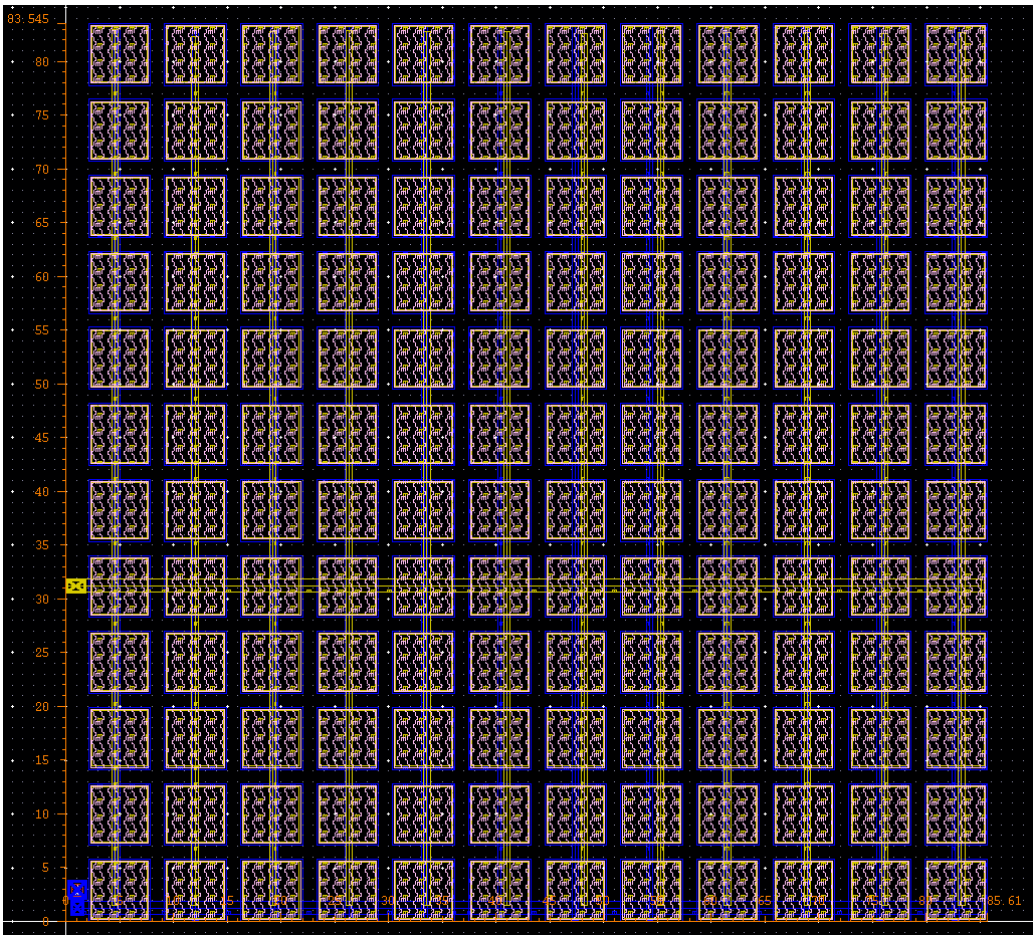


Figure 3-12: A MIM capacitor of 5pF capacitance with 144 multiplayer. Each unit has a width of 5.37µm and height of 5.37µm. The total area of the capacitor is 83.545µm×85.61µm.

Each unit has width of 5.37µm and height of 5.37µm. The capacitance of each unit cell is 34.76fF which is less than the required capacitance of each unit cell.

Figure 3-13 presents a cell of cascoded PMOS transistors and NMOS transistor. It consists of 6 identical PMOS segments and 4 identical NMOS transistor. The biasing transistor is placed at the left side of the cascaded NMOS and PMOS transistor to decrease the distance between them. Thus, the parasitic resistances of the interconnections are decreased. The whole cascoded NMOS and PMOS transistor consists of 44 cells. The drain and source of the cascode NMOS and PMOS are connected with multiple metal layers to decrease the parasitic resistance.

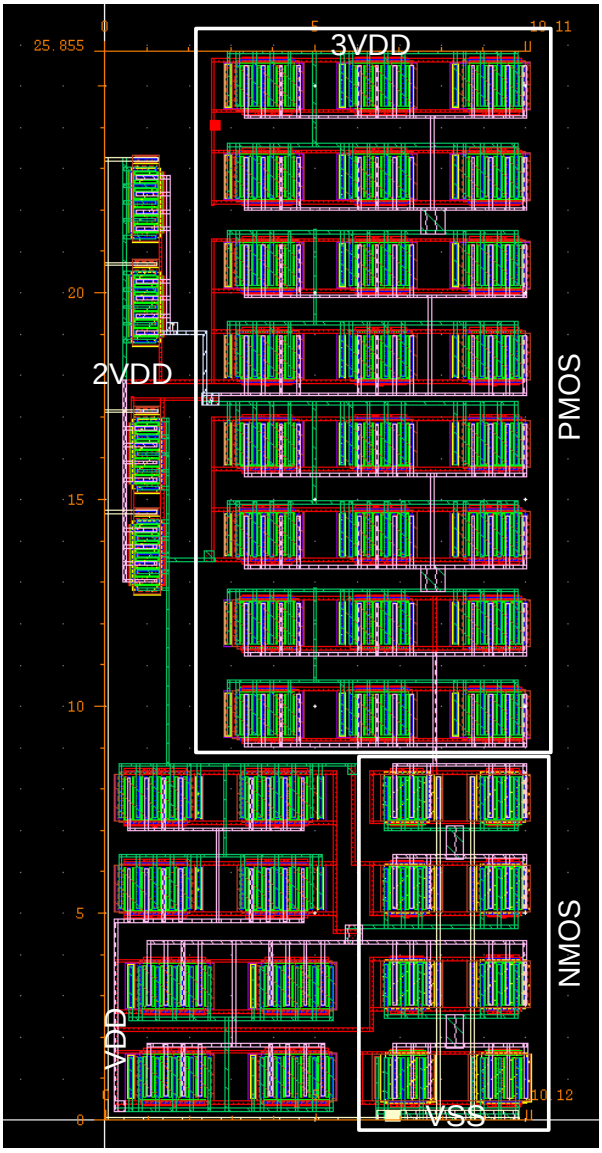


Figure 3-13: Stack NMOS and PMOS transistor used in the high voltage level shifter with biasing transistor.

Figure 3-14 shows the final layout of the single stage level shifter. Multiple metal layers are used in the interconnections to decrease the parasitic resistance. Output is taken from the right side to minimize the distance. The layout consumes a total silicon area of 83.54×121.86 [µm×µm].

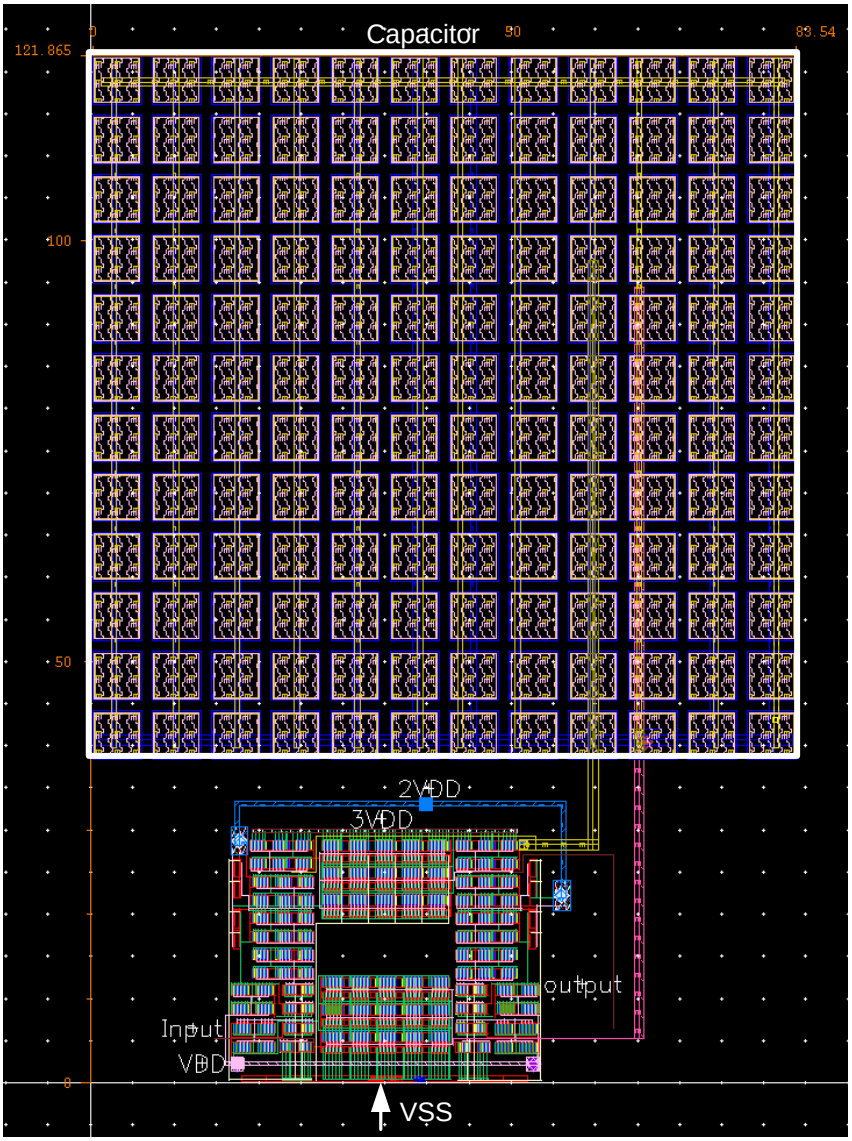


Figure 3-14: Layout of single stage level shifter. Total height is 121.86um and width is 83.54um.

Layout of the high voltage level shifter for all three stages is shown in Figure 3-15. The whole level shifter consumes a silicon area of 262.84×124.66 [µm×µm]. Power supply of VDD, 2VDD and 3VDD is placed on the left side along with input signal and on the right side power supply of 4VDD, 5VDD and 6VDD is placed along with output signal of the high voltage level shifter. Ground connection VSS is placed on the bottom of the design.

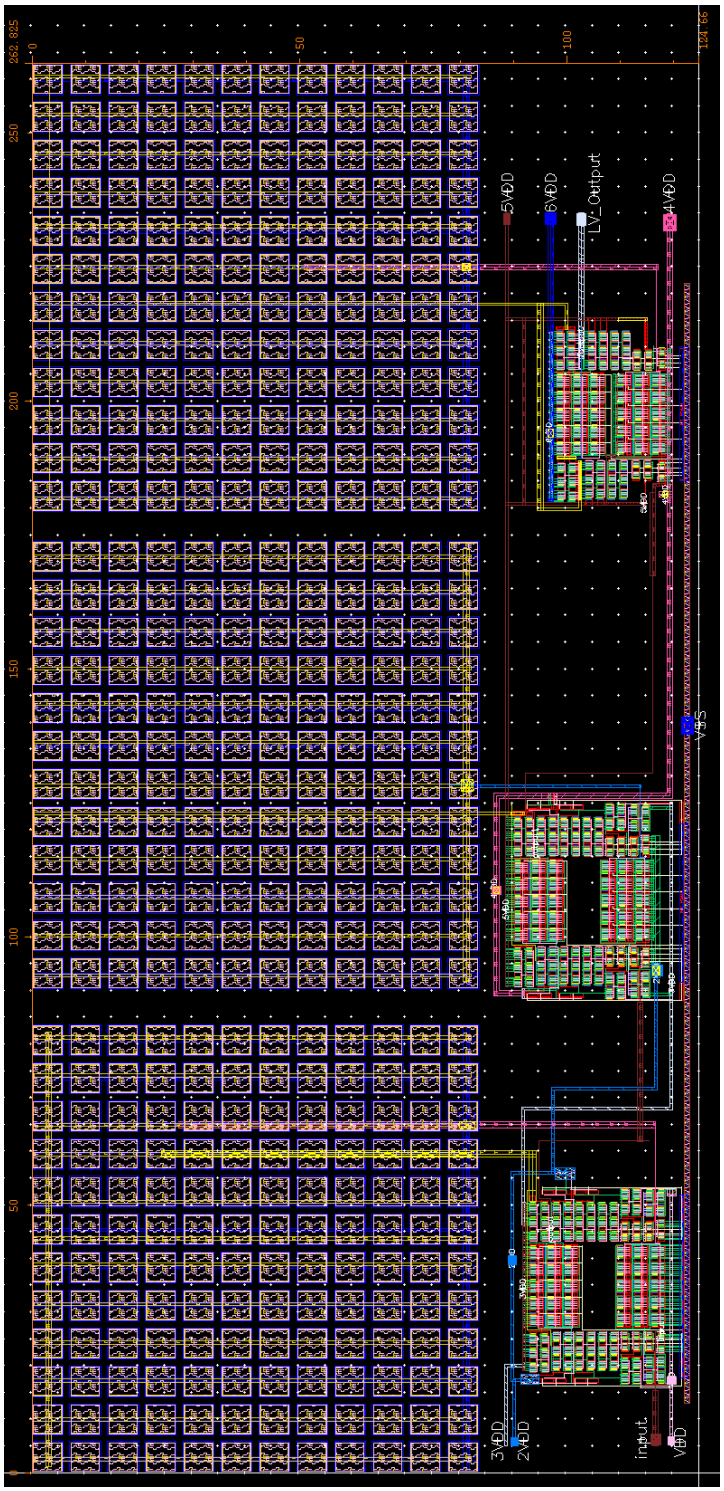


Figure 3-15: Layout of high voltage level shifter for all three stages. Total height is 124.66um and width is 262.84um.

4 Measurement Setup and Results with PCB and Package Parasitic

The DCDC converter IC is designed with PCB and package model. The simulation result is presented with all parasitic around the circuit. In addition decoupling capacitor is connected with the battery power supply VBAT. Decoupling capacitor allows to reduce the input power supply fluctuation. All the components used in the test bench are non-ideal components. The simulation test bench is shown in the Figure 4-1. All the result was presented in chapter 3 was for the ideal case.

The design of PCB for the high speed circuit like DCDC buck converter, parasitic capacitance and inductance is very important issue. Battery supply voltage is placed between the trace and ground and electric field will exit around the wire. The ration between the applied voltage and the charge that flows into the open ended trance is capacitance. So a capacitor of 2pF is place. To eliminate the unwanted inductance a stray inductance is placed between the supply voltage and the de-coupling capacitor. Same stray inductor is placed at the output filter to remove the unwanted inductance.

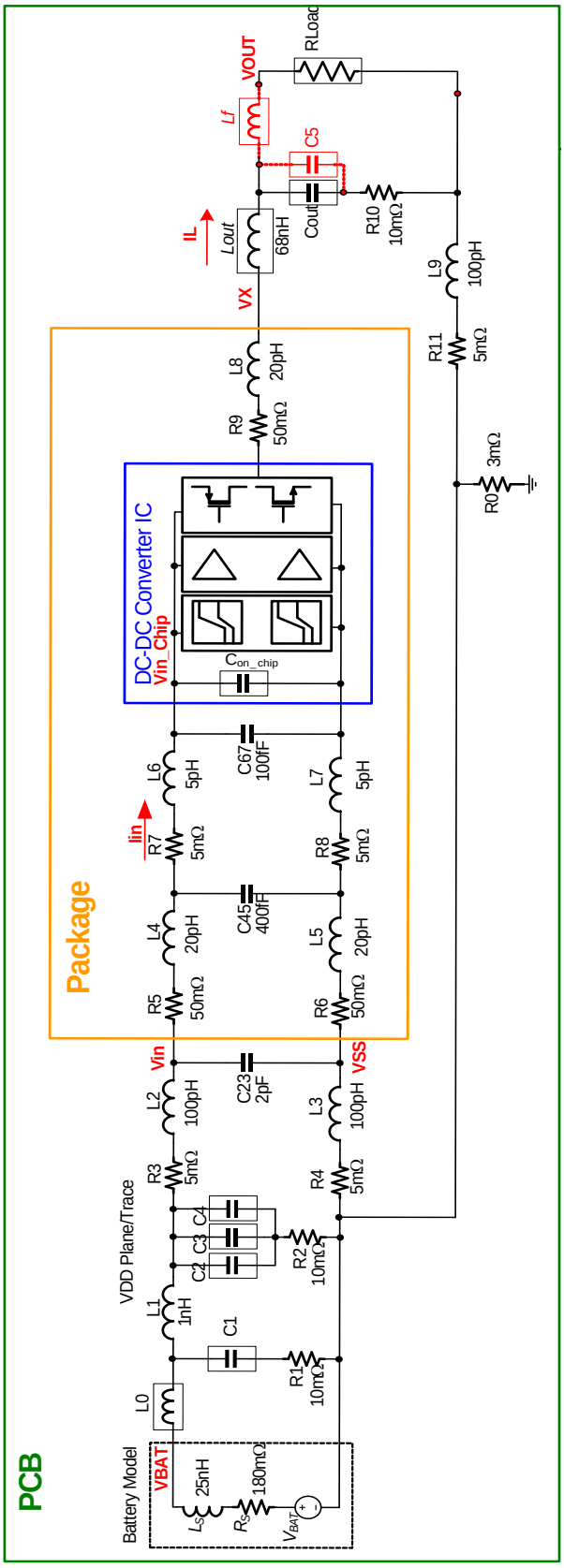


Figure 4-1: Simulation test bench of the converter with PCB and Package parasitic.

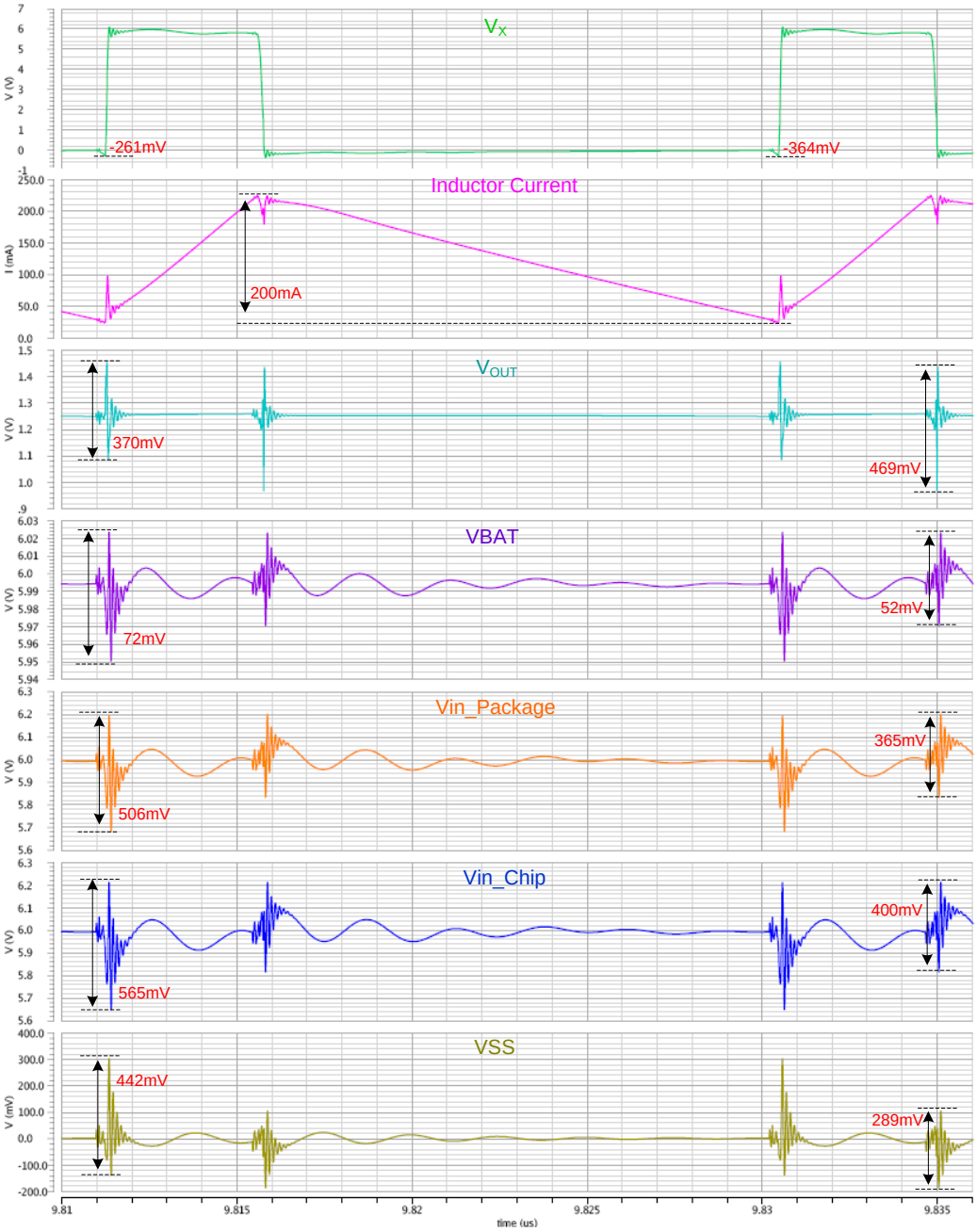


Figure 4-2: Simulated waveform of the DCDC Buck converter with all the PCB and Package parasitic and with real components.

Figure 4-2 shows the wave form of the battery voltage at VBAT node, Vin_package and Vin_chip node and ground node VSS. Figure also illustrate Vx node output voltage and the inductor current. Output voltage is 1.25V and current ripple is 200mA which is the design specification.

4.1 Component Evaluation

I. Inductor Model

Inductor has other element within them which includes DC resistance and the interwinding capacitance. At the higher frequency, inductor stops behaving like an inductor. At the transition point the impedance will have a resonance causing a substantial rise in the impedance of the inductor. This resonance can cause issues in some situations and should not be ignored. An inductor 100nH is chosen in the output filter. Figure 4-3 shows precise inductor model. The model is MLZ1608DR10DT000 [19]. Precise inductor model and datasheet results have ~5% difference.

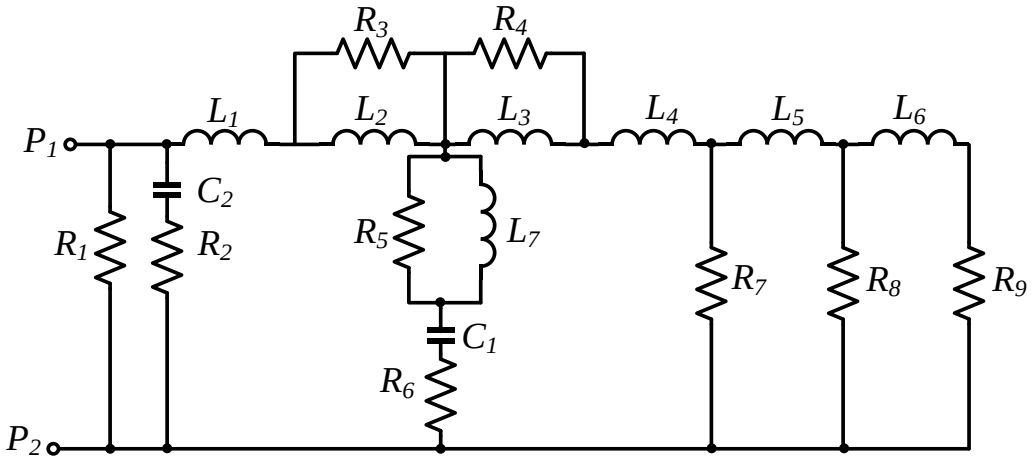


Figure 4-3: Precise Inductor Model

Table 4-1: Component Values of Precise Inductor Model MLZ1608DR10DT000

L_1	9.378nH	R_1	1GΩ
L_2	3.925nH	R_2	20Ω
L_3	83.93nH	R_3	111.3Ω
L_4	1.75nH	R_4	40.76kΩ
L_5	4.076nH	R_5	393.27Ω
L_6	11.62nH	R_6	2.216Ω
L_7	326.9nH	R_7	1.08Ω
C1	1.316pF	R_8	0.528Ω
C2	658.5fF	R_9	0.257Ω

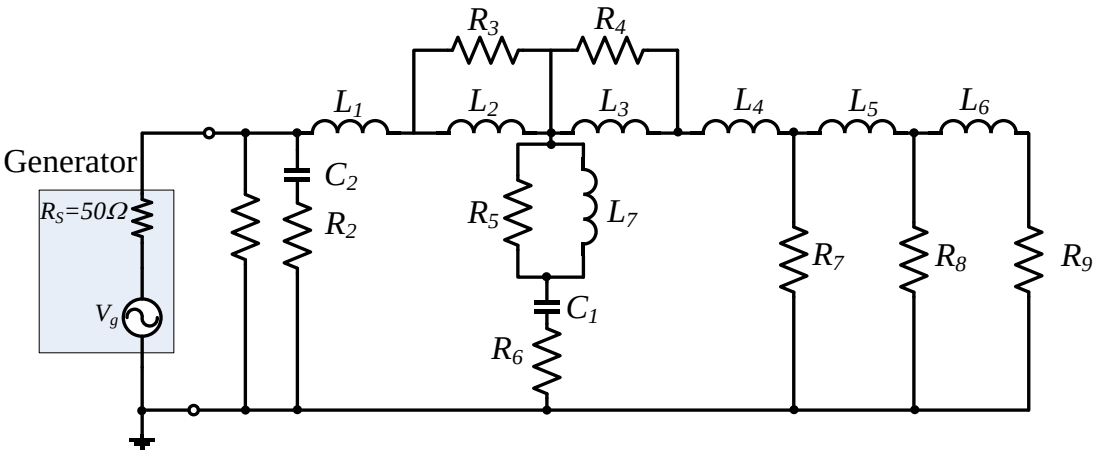


Figure 4-4: S-Parameter Simulation Setup for Characterizing Inductor

Table 4-2: Parameter Calculation Formula for Inductor

	Quality Factor	Impedance (Ω)	Inductance (H)
Inductor	$\frac{img\lvert Z_L\rvert}{real\lvert Z_L\rvert}$	$\lvert Z_L\rvert$	$\frac{\lvert Z_L\rvert}{2\pi(xval(Z_L))}$

Table 4-1 shows all the component values for the real inductor model used in the output filter. Inductor was evaluated with the datasheet. Figure 4-4 illustrates the simulation setup and Table 4-2 shows the formulas for calculating different parameter. Precise inductor model and datasheet results have ~5% difference. Comparison of the results is illustrated in Figure 4-5.

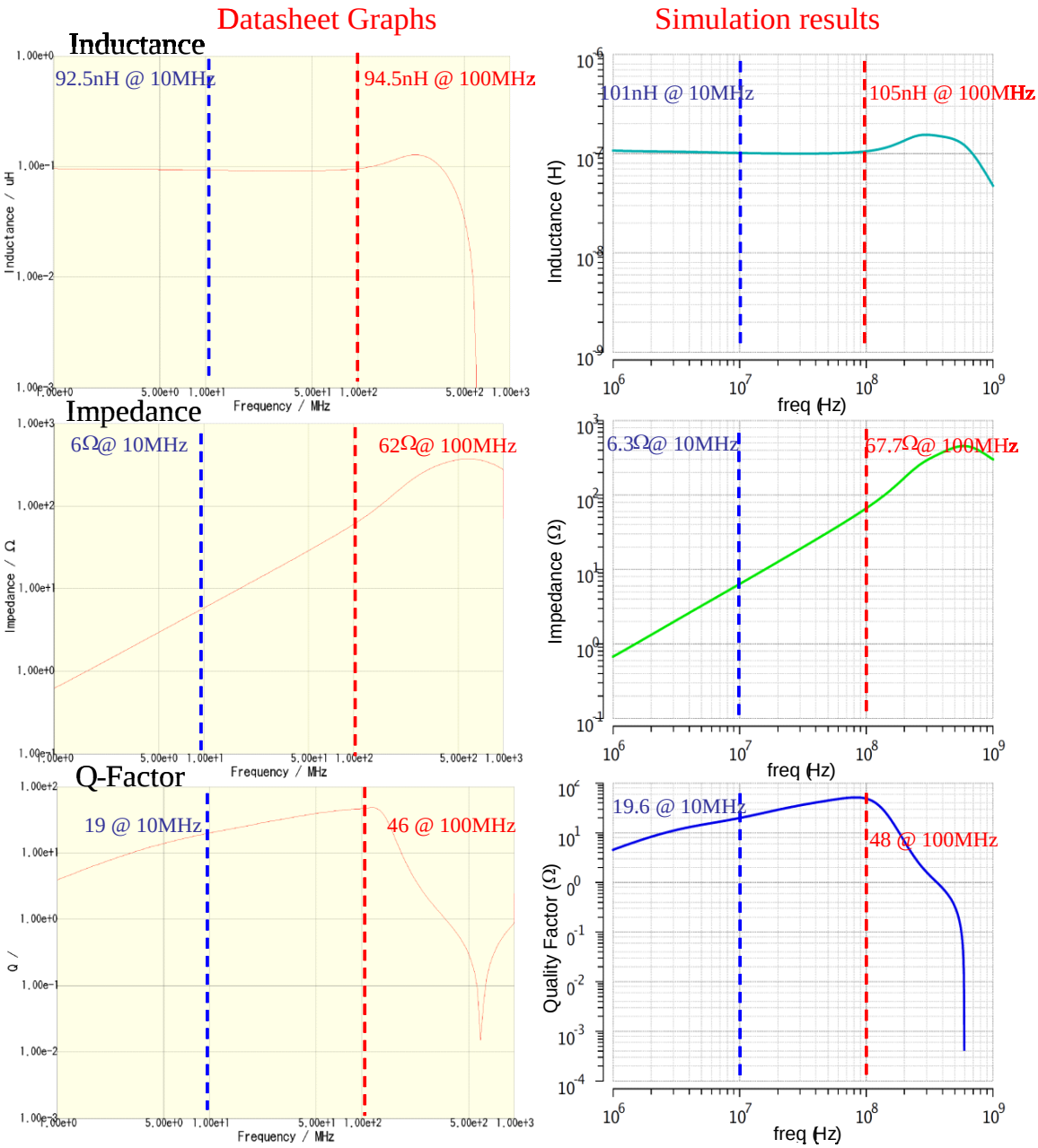


Figure 4-5: Inductor Comparison with Datasheet and Simulation.

II. Capacitor Model

Capacitors are used extensively in most system. They are used for the power-supple bypassing, AC-coupling, filtering etc. These capacitors are not perfect components. They have elements which limits their effectiveness. The most prominent elements of the capacitors are the equivalent series resistance (ESR) and equivalent series inductance (ESL). Equivalent series inductance of the capacitor prevents to act as a capacitor at higher frequency as the impedance starts to increase rather than decreasing. In this DCDC converter different types of capacitor have been used for the output filter and de-coupling capacitor.

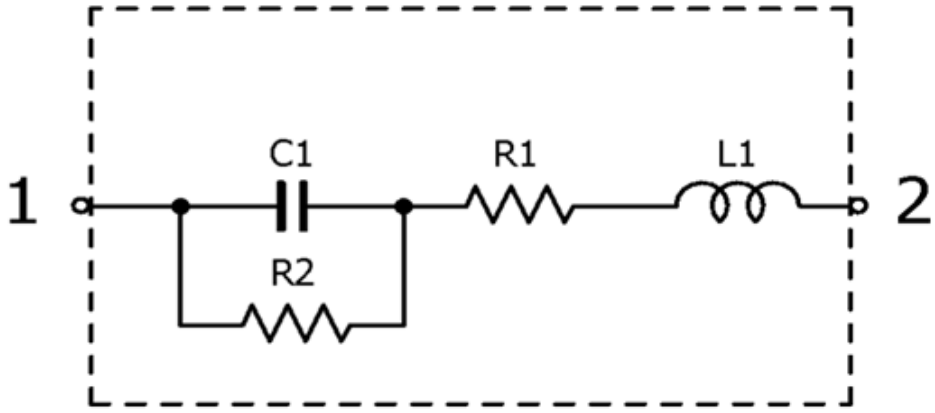


Figure 4-6: Precise Capacitor model

Table 4-3: Component Values of Capacitor Model

Model	Value	R_1	R_2	L_1	C_1
C0510X6S0G104M030AC[20]	100nF	*0.0160*Ω	*23G*Ω	*0.077nH*	*100nF*
C603X5R1E104M030BB[21]	100nF	*29.64m*Ω	*20G*Ω	*300pH*	*100nF*
C0603X7R1E101K030BA[22]	100pF	*950m*Ω	*10G*Ω	*300pH*	*100pF*
C0603X7R1E222K030BA[23]	2.2nF	*132m*Ω	*83G*Ω	*300pH*	*2.2nF*

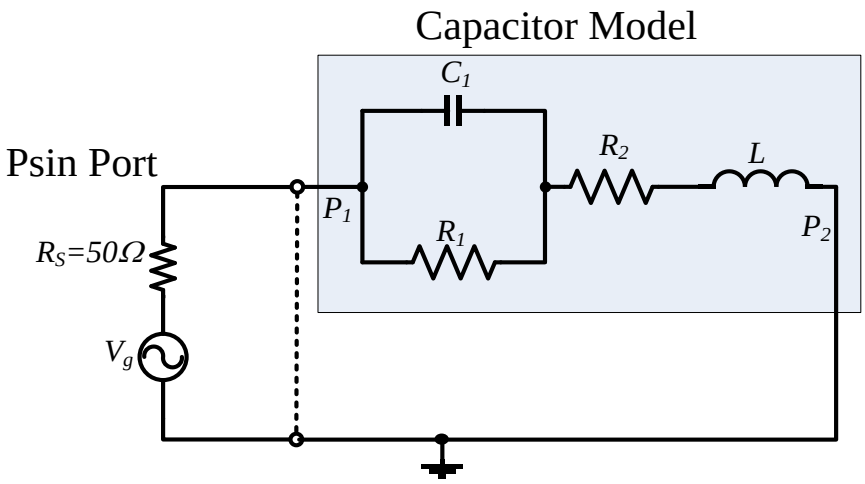


Figure 4-7: S-Parameter Simulation Setup for Characterizing Capacitor.

Table 4-4: Parameter Calculation Formula of Capacitor

	Quality Factor	Impedance (Ω)	Inductance (H)
Capacitor	$\frac{img\lvert Z_C\rvert}{real\lvert Z_C\rvert}$	$\lvert Z_C\rvert$	$\frac{\lvert Z_C\rvert}{2\pi(xval(Z_C))}$

Table 4-3 shows all the component values for the real capacitor model used in the output filter and de-coupling capacitor. All the capacitor was evaluated with the datasheet. Figure 4-7 illustrates the simulation setup and Table 4-4 shows the formulas for calculating different parameter. Precise capacitor model and datasheet results have no difference. Comparison of the results for different capacitors is illustrated in Figure 4-8, Figure 4-9, Figure 4-10 and Figure 4-11.

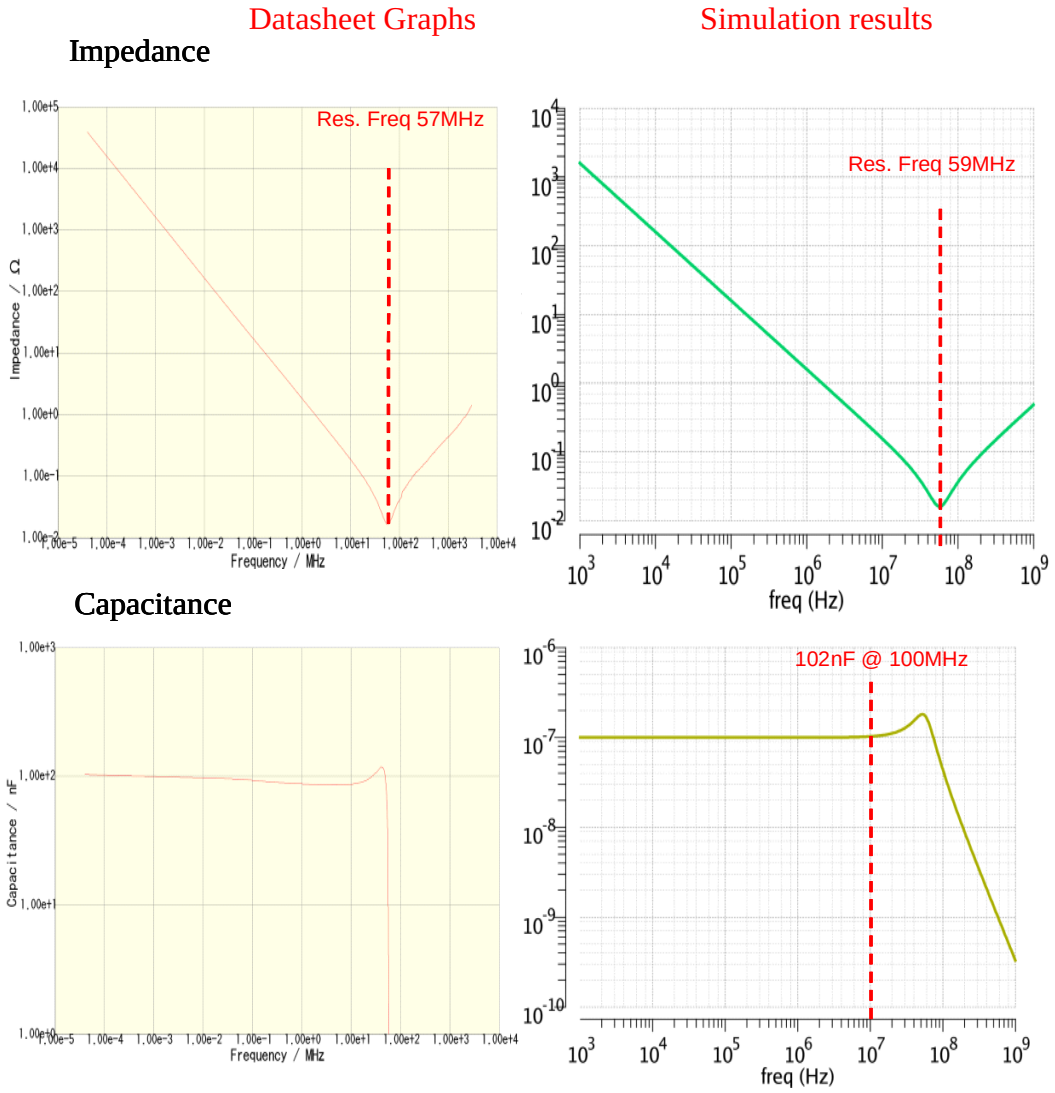


Figure 4-8: Capacitor Model C0510X6S0G104M030AC comparison with Datasheet and Simulation.

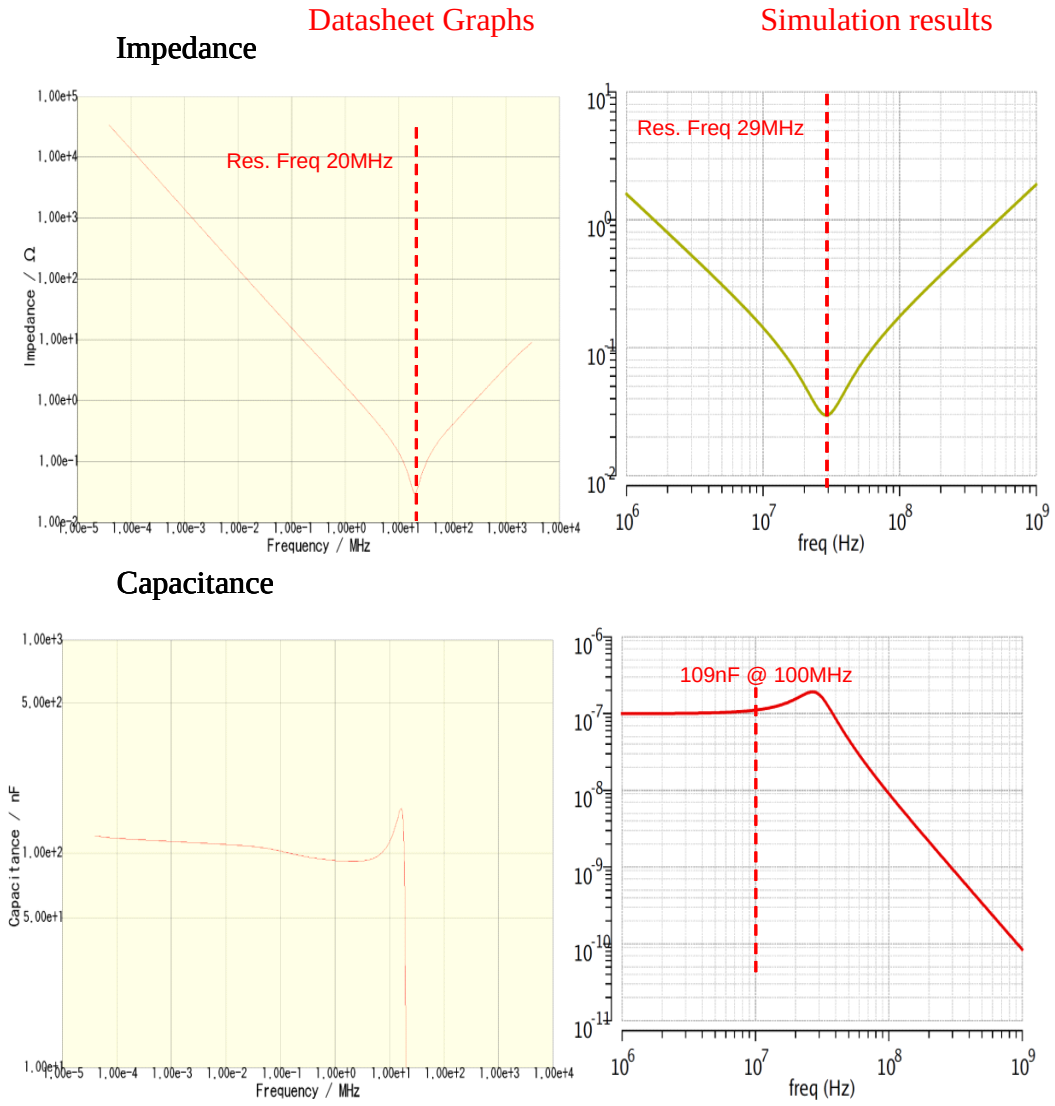


Figure 4-9: Capacitor Model C603X5R1E104M030BB Comparison with Datasheet and Simulation.

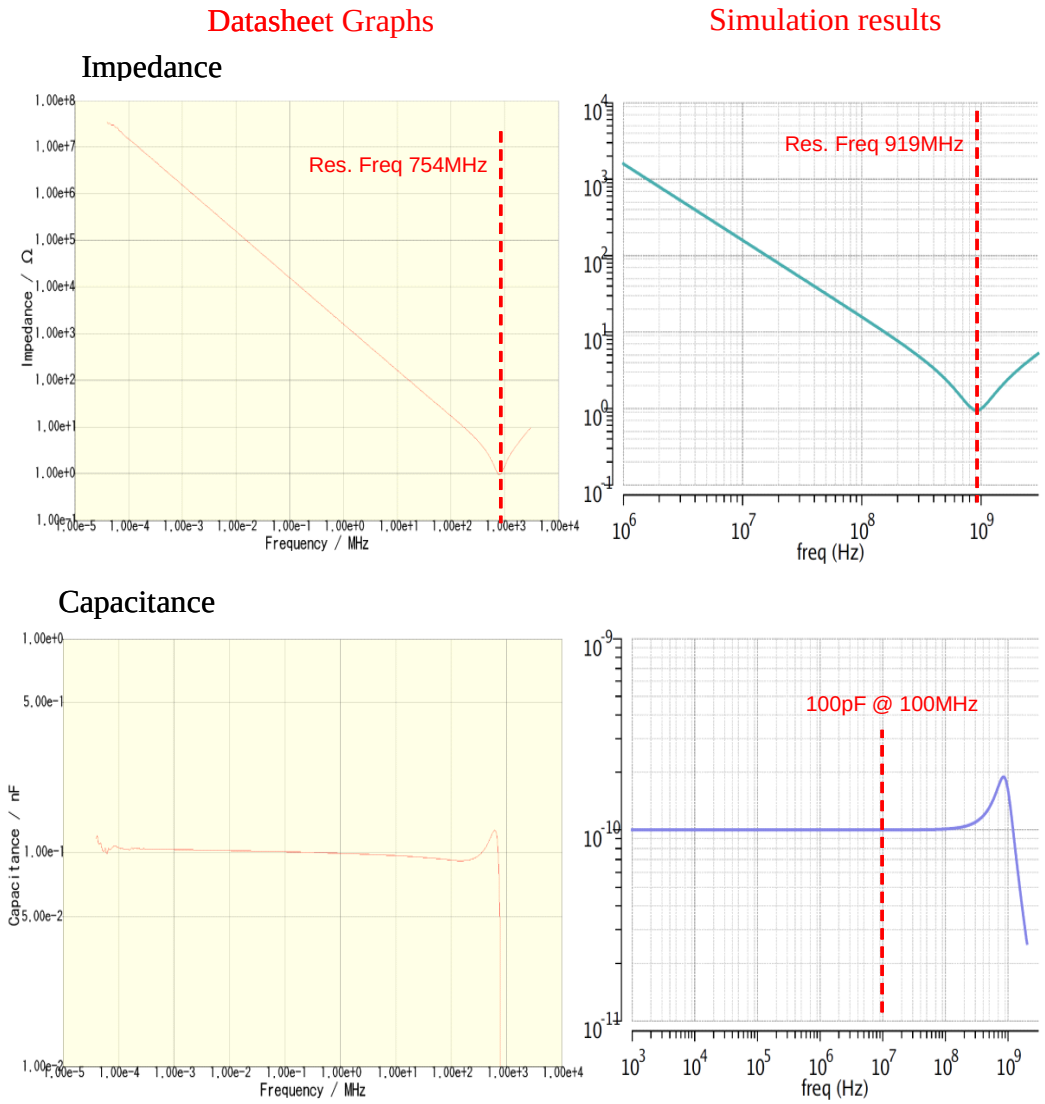


Figure 4-10: Capacitor Model C0603X7R1E101K030BA Comparison with Datasheet and Simulation.

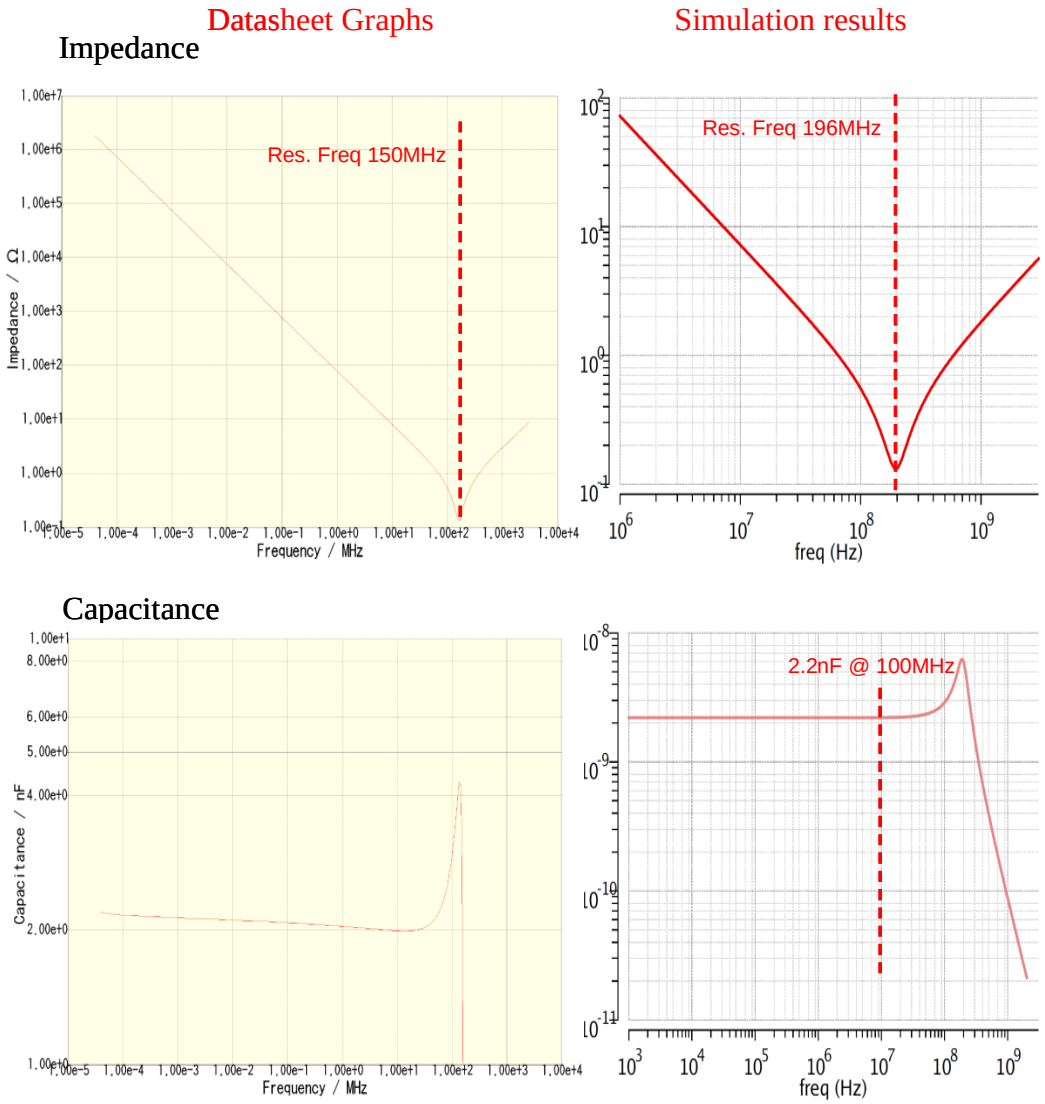


Figure 4-11: Capacitor Model C0603X7R1E222K030BA Comparison with Datasheet and Simulation.

4.2 Efficiency Calculation:

The efficiency of the buck converter is measured against fixed output current against fixed battery voltage and fixed input power. Figure 4-12 shows the power loss of different blocks of the buck converter against the design specification. The input power is measured in such a way that the battery voltage by the input source and the all blocks power loss used in the test bench is taken into consideration.

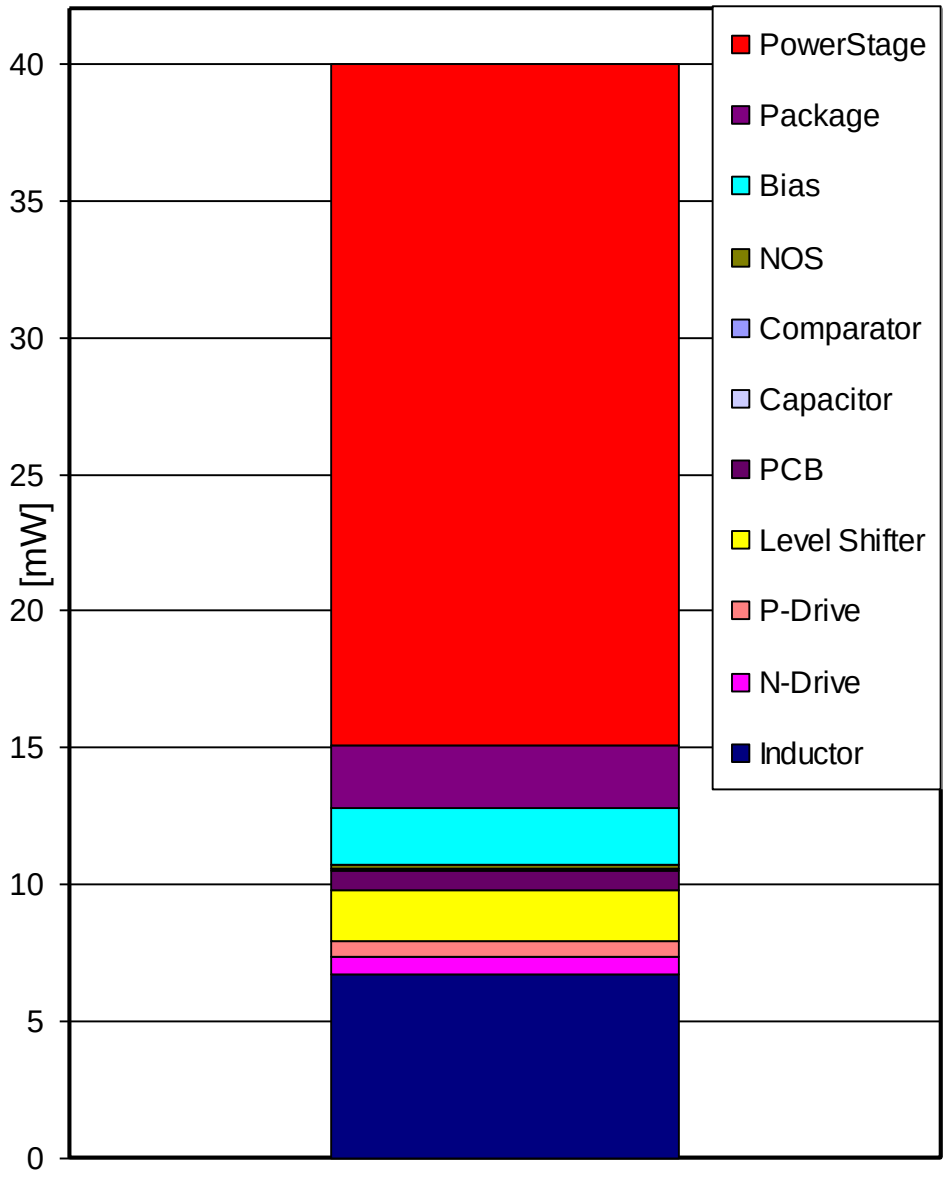


Figure 4-12: Power Loss Chart of the Different Blocks of the DCDC Converter.

So the total power loss of the buck converter calculation is

$$P_{LOSS} = P_{Powerstage} + P_{P-Drive} + P_{N-Drive} + P_{Levelshifter} + P_{NOS} + P_{Comparator} + P_{Bias} + P_{Package} + P_{PCB} + P_{Inductor} \quad (3.2)$$

Where power loss in the power stage, p-drive, n-drive, level shifter, NOS, comparator, bias, package, PCB and inductor has taken under calculation for measuring total power loss in the buck converter chip. Input power of the system is calculated as

$$P_{IN} = P_{LOAD} + P_{LOSS} \quad (3.3)$$

Here input power P_{IN} is the power delivered by the battery source which is equal to the total power loss and power consumed by the load resistor. So the efficiency calculation is as follow,

$$\eta = \frac{P_{OUT}}{P_{LOAD} + P_{LOSS}} \times 100\% \quad (3.4)$$

Efficiency of the buck converter chip has been calculated for the fixed input power of 200mW for the fixed output voltage 1.25V and load resistance of 10Ω. The battery supply voltage is 6V and the switching speed of the converter is 52MHz. Figure 4-12 shows the total power loss of the converter is 42mV. With this design specification 78.97% efficiency is achieved shown in Table 4-5.

Table 4-5: Power Calculation

Parameters	Value
P_{IN}	200.19mW
P_{OUT}	159.46mW
P_{LOSS}	39.97mV
V_{OUT}	1.25V
Efficiency	79.65%

5 Conclusion

In the system on chip application system, IC core voltages have reduced in the recent years so the importance of level shifter has also increased. Presented level shifter is capable of shifting low voltage to high voltage swing signal of 5 VDD offset. Output signal of the level shifter presents 5V to 6V swing square wave and can operate at high frequency range of 50-100MHz. First two stage of the level shifter provides 2 offset VDD each and last stage provides one VDD offset. The rise and fall time of the level shifter is 49ps and 16.13ps respectively and delay for low to high side and high to low side is 117ps and 97ps respectively. The output signal is buffered by two stage inverter to drive the high input gate capacitance of PMOS transistor for the power stage of the step down dc-dc converter.

Presented Level shifter is designed in 1V, 45nm CMOS technology. Simple modification of the circuit allows the level shifter to work within the technology parameter where oxide stresses and hot carrier degradation is minimized for the all cascode transistors. All the results were measured after connecting the comparator, NOS, level shifter, buffer driver, power stage, output filter with PCB and package parasitic component. A simple comparator generates a rectangular signal and passes through non-overlapping circuit. Level shifter converts low voltage signal to high voltage signal. P-driver circuit and N-driver circuit allows to control the required dead-time. Dead-time for low to high side is 115ps and high to low side is 157ps. Driver circuit also increases the capacitance of the signal to drive the power stage transistors. Simulation result shows, power consumption of the comparator is 0.017mW, NOS is 0.135mW, level shifter is 1.84mW, P-driver is 0.627mW and N-driver is 0.600mW at 52MHz.

Table 5-1: Comparison of presented HV Level Shifter with previous work.

Prior work	Year	Technology Type	Technology Node (µm)	Delay D (ns)	Output Voltage (V)	Frequency (MHz)
Declerq M.J [25]	1993	CMOS	2	80	50	
Dong Pan [17]	2003	HV SOI	0.35	20	18	1
Erik J. Mentze [26]	2004	PD SOI	0.25	3.5	5	10
Serneels Ben [16]	2006	CMOS	0.13	0.08	2.4	1GHz
Rocha Jose [27]	2007	CMOS	0.13	-	3.5	2
Khorasani [29]	2009	DMOS	0.8		150	-
Manoj Kumer [28]	2010	CMOS	0.35	2.33	3.3	-
Moghe Y. [18]	2011	DMOS	0.35	2.4	10	-
Present Work	2015	CMOS	0.045	0.117	6	52

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