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COMPARISON OF OUTPUT HARMONICS BETWEEN TWO- AND THREE-LEVEL THREE-PHASE SPACE VECTOR PWM INVERTERS

Master of Science thesis

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ABSTRACT

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The usage of renewable energy sources is growing. These sources, such as photovoltaic devices and wind turbines, are connected to the power grids via inverters. Power electronic inverters produce non-sinusoidal voltages and increase the amount of unwanted distortion in the grids. Standards define the quality of the electricity in the power grids. Therefore, it is sensible to study the phenomena and methods to reduce the harmonic distortion in the outputs of different inverter topologies.

LCL filters are used to suppress the harmonic components in the output waveforms of the grid connected inverters. The filter is one of the most expensive component in drive systems. The amount of harmonics can also be decreased by adding voltage levels to the inverter's DC bus, optimizing the switching sequences and increasing the switching frequency. Therefore, better output harmonic performance can be achieved with the same LCL filter by using three-level inverter instead of two-level inverter. Three-level inverter also enables higher switching frequency. However, some additional costs are created, such as more semiconductor switches are needed, and the device requires more complex control system.

The main issue in this thesis is to compare output harmonics between two- and three-level inverters. The studied topologies are two-level voltage source inverter and three-level neutral-point-clamped inverter. A detailed space vector modulation method is explained for these inverters. Requirements for a well implemented space vector modulator are also discussed. Space vector pulse width modulators are created using MATLAB® and Simulink®. Output harmonic performance is compared by simulations with different switching frequencies and modulation indexes under linear modulation region.

The simulations show that increasing the switching frequency reduces the phase current's harmonics. The switching frequency doesn't have similar effect on the line-to-line voltage's total harmonic distortion value. It only increase the frequencies where the voltage's harmonic components occur. It's also shown, that the voltage's and current's THD values in the NPC inverter are half of the THD values in the VSI. The modulation index has an effect on both, the line-to-line voltage's and phase current's THD values. When the modulation index is reduced, the voltage's and current's THD values are increased. Small modulation index value reduces the difference between output performance of the VSI and NPC inverters.

TIIVISTELMÄ

JANI HÄMÄLÄINEN: Kaksi- ja kolmitasoisten kolmivaiheisten avaruusvektorimoduloitujen PWM vaihtosuuntaajien lähdön harmonisten vertailu
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Uusiutuvien energianlähteiden käyttö on kasvussa. Vaihtosuuntaajia käytetään syöttämään tehoa sähköverkkoon aurinkopaneeli ja tuulivoimasovelluksissa. Tämä suuntaus lisää sähköverkkoon kytketyn tehoelektroniikan määrää. Standardeilla määritellään sähköverkkoon syötetyn sähkön laatua. Vaihtosuuntaajat tuottavat ei-sinimuotoisia lähtöjännitteitä ja lisäävät verkossa esiintyvien särökomponenttien määrää. Tämän vuoksi on tärkeä tutkia keinoja pienentää harmonisten komponenttien määrää eri suuntaajatopologioiden lähdöissä.

LCL suodattimia käytetään vähentämään verkkoon kytkettyjen vaihtosuuntaajien lähdöissä esiintyviä harmonisia komponentteja. Suodatin on kuitenkin yksi sähkökäyttöjen kalleimmista komponenteista. Harmonisten määrää voidaan vähentää myös lisäämällä vaihtosuuntaajan tasajännitetasoja, optimoimalla kytkentäjaksoja ja nostamalla kytkentätaajuutta. Samalla LCL suodattimella saavutetaan pienempi harmonisten määrä käyttämällä kolmitasoista vaihtosuuntaajaa kaksitasoisen sijaan. Kolmitasoinen vaihtosuuntaaja mahdollistaa myös korkeamman kytkentätaajuuden käytön. Useamman jännitetason käyttö aiheuttaa kuitenkin muita lisäkuluja, kuten pääpiirin puolijohdekomponenttien kasvaneen määrän ja laitteen monimutkaistuneen ohjauksen.

Tässä työssä vertaillaan kaksi- ja kolmitasoisten vaihtosuuntaajien lähdöissä esiintyviä harmonisia komponentteja. Tutkittavat topologiat ovat kaksitasoinen jännitesyöttöinen vaihtosuuntaaja ja kolmitasoinen nollapotentiaaliin kiinnitetty vaihtosuuntaaja. Työssä esitellään avaruusvektorimodulointimenetelmät näille suuntaajille. Lisäksi käsitellään vaatimuksia käytännön avaruusvektorimodulaattoritoteutukselle. Molemmille suuntaajille toteutetaan avaruusvektorimodulaattorit hyödyntäen MATLAB® ja Simulink® ohjelmistoja. Lähdön harmonisia vertaillaan tekemällä simulointeja eri kytkentätaajuuksilla ja modulointi-indekseillä. Simuloinnit toteutetaan lineaarisella modulointialueella.

Simuloinnit osoittavat, että kytkentätaajuuden nostaminen vähentää vaihevirran harmonisia. Kytkentätaajuuden nostolla ei ole samanlaista vaikutusta pääjännitteen THD arvoon. Sen kasvattaminen kuitenkin nostaa taajuusaluetta, missä jännitteen harmoniset esiintyvät. Tuloksista nähdään myös, että NPC vaihtosuuntaajaa käytettäessä jännitteen ja virran THD arvot puoliintuvat verrattuna VSI vaihtosuuntaajan arvoihin. Modulointi-indeksillä todettiin olevan vaikutus jännitteen ja virran THD arvoihin molemmilla suuntaajilla. Jännitteen ja virran THD arvot kasvavat, kun modulointi-indeksiä pienennetään. Pienten modulointi-indeksien käyttö kaventaa eroa VSI ja NPC vaihtosuuntaajien lähdön harmonisten määrässä.

PREFACE

I’d like to thank my family for support throughout studies. I also wish to name following fellow students: Antti Mansukoski, Jarno Naskali, Jori Lähteelä, Jukka Lehtinen, Tommi Koskinen and Toni Liimatainen. Their help was essential to make it through studies. Most importantly, I’d like to thank them for the past few years and all the shared experiences.

Vaasa, 4.10.2015

Jani Hämäläinen

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LIST OF SYMBOLS AND ABBREVIATIONS

2L	two-level
3L	three-level
DC	direct current
ESR	equivalent series resistance
IGBT	insulated-gate bipolar transistor
MTTF	mean time to failure
NPC	neutral-point-clamped
PWM	pulse-width modulation
RMS	root mean square
THD	total harmonic distortion
VSI	voltage source inverter

C_i	capacitor $i = \{1, 2, 3\ldots\}$
D_{ik}	diode $i = \{1, 2, 3\ldots\}$ $k = \{u, v, w\}$
f_{sw}	switching frequency
h	number of component
$\hat{I}_u$	amplitude of phase voltage
K	constant
L	inductance
L_i	inductor $i = \{1, 2, 3\ldots\}$
L_{load}	load inductance
m	modulation index
N	neutral point of grid voltages
n	negative DC bus
o	midpoint of DC bus
p	positive DC bus
R	resistance
R_{load}	load resistance
S_{ik}	IGBT switch $i = \{1, 2, 3\ldots\}$ $k = \{u, v, w\}$
T_S	cycle time of modulation period
t_i	switching time of switching vector for two-level inverter $i = \{0, 1, 2\}$
t_k	switching time of switching vector for three-level inverter $k = \{a, b, c\}$
u	inverter u-phase output
u_h	harmonic components of voltage u $h = \{1, 2, 3\ldots\}$
U_{dc}	DC bus voltage
u_k	grid phase voltage $k = \{u, v, w\}$
$\hat{U}_{uv}$	amplitude of line-to-line voltage
v	inverter v-phase output
w	inverter w-phase output
θ_{refn}	angle of reference vector $n = \{1, 2\}$

1. INTRODUCTION

Renewable energy sources are the topic of today's energy production. According to statistics provided by IEA, total power of installed photovoltaic energy worldwide is booming [5]. Unlike traditional electricity generation, renewable methods require inverters to feed the electricity to power grids. In addition, power electronics play an important role in several other applications with increasing prospects, such as electrical vehicles, elevators and escalators, wind power and cargo handling.

There are several different inverter topologies presented in the literature. The most common inverter type in industry is a two-level (2L) three-phase voltage source inverter (VSI). It has proven to be reliable, the control of the device is relatively easy to implement and the number of semiconductor components is low. However, the VSI has poor performance when it comes to output harmonics. The inverter's output harmonics can be decreased by increasing the number of voltage levels in a DC bus. The most common three-level (3L) inverter topology is a neutral point clamped (NPC) inverter. Thus, these two inverters are studied in this thesis.

Lowering inverters output harmonics is important, since a grid connected inverter utilization requires an output LCL filter. The filter is a relatively high-cost component in drive systems. Reducing the harmonics allow the use of smaller filters and increase savings in the production costs. Voltage ratings of the insulated-gate bipolar transistor (IGBT) modules are also limited. Voltage stress over an individual IGBT module is split in multilevel inverters. Therefore, higher output voltage levels are obtained in the multilevel topologies using the same voltage rated IGBTs. Multilevel inverter drawbacks include an increased number of semiconductor components, more required driver and measurement circuits, and more complexity in controlling the device. These factors decrease the mean time to failure (MTTF) and make the multilevel inverters less attractive.

The main purpose of this thesis is to present a detailed operation of space vector pulse-width modulation (PWM) methods for the VSI and NPC inverters. Simulation models of these two inverters are created using MATLAB® and Simulink®. The implemented models are used to investigate the relationship between different space vector modulation parameters and total harmonic distortion (THD) values in inverter's output voltage and current. The parameters of interest are the switching frequency and modulation index.

Chapter 1 introduces the subject considered in this thesis. Typical VSI and NPC inverters' main circuit topologies are given in Chapter 2. It also compares typical output waveforms of the inverters, provides a definition of harmonic components, and explains their analysis

method. General space vector PWM methods for the VSI and NPC inverters are presented in Chapter 3. More specific requirements for a well-implemented PWM method are covered in Chapter 4. Chapter 5 presents the simulation models of the VSI and NPC inverters. Simulation results are also provided in Chapter 5 before the conclusion is given in Chapter 6.

2. TWO- AND THREE-LEVEL INVERTER SCHEMES

This chapter gives an overview of three-phase implementations of the VSI and NPC inverters. These two inverter topologies are introduced in Section 2.1. A more detailed operation of the NPC inverter is showed by presenting current paths in different operational situations. Typical output voltage waveforms are presented along with a discussion about harmonics and an analyzation of the harmonic distortion in Section 2.2.

2.1 Different inverter topologies

A typical main circuit topology of the grid connected VSI with an *LCL* filter is presented in the Figure 1. This is the most common type of an inverter in today's industry.

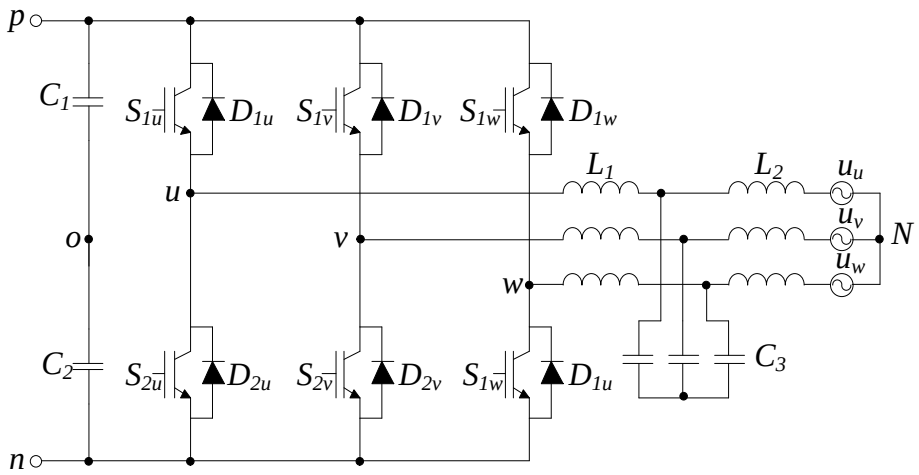


Figure 1. *The main circuit topology of a grid connected 2L three-phase VSI with LCL filter.*

The DC bus is implemented with two series connected capacitors- C_1 and C_2. The positive DC bus is marked as '*p*' and the negative as '*n*'. The midpoint of the DC bus is referred to as '*o*'. Inverter phase legs are made by using two IGBTs with inverse diodes, and they are denoted as S_1-S_2 and D_1-D_2, respectively. The output *LCL*-filter is implemented with the L_1 and L_2 inductors and the C_3 capacitor. Grid voltages are presented as u_u, u_v and u_w. The grid's neutral point is marked '*N'*. The inverter's phase outputs are denoted as '*u*', '*v*' and '*w*'.

The main circuit topology found in the scientific publications of a grid connected NPC inverter with *LCL* filter is presented in the Figure 2.

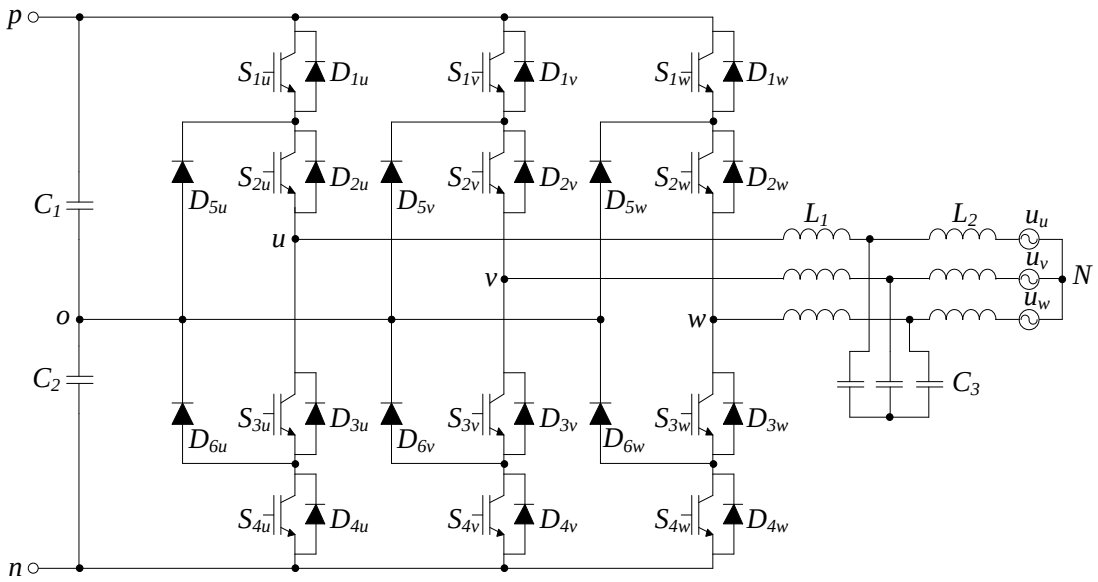


Figure 2. *The main circuit topology of a grid connected 3L three-phase NPC inverter with LCL filter.*

Naming of the components and reference points is made with the same principles as the VSI in the Figure 1. The difference between the VSI and NPC is that the NPC inverter has a pair of neutral-point-clamp diodes (D_5-D_6) and twice as many IGBTs with inverse diodes in each phase leg. This allows the third DC bus voltage level, 'o', to be connected to the inverter's phase outputs.

2.1.1 Current paths in different operational situations

More detailed operation of the NPC inverter is introduced in this section. Positive and negative current paths with all allowed IGBT state combinations are presented. Positive current denotes current from the DC bus capacitors to the phase output, and negative current flows from the phase output to the DC bus capacitors.

Current paths are presented in three different situations in Figure 3 depending on which IGBT pairs are in the on-state. Figure 3 (a) represents the combination of both upper IGBTs S_1 and S_2 when they are switched on and the phase current is positive. The positive DC bus is connected to the phase output when both of the upper IGBT switches are conducting. When both lower inverse diodes are conducting and current is positive, the phase output is connected to the negative DC bus. [13]

Figure 3 (b) demonstrates when IGBTs S_2 and S_3 are switched on. Upper neutral-point-clamp diode D_5 and IGBT S_2 are conducting so that the phase output and the DC bus midpoint are connected with positive phase current. The output is connected to the midpoint with negative phase current when the current flows through IGBT S_3 and lower neutral-point-clamp diode D_6. [13]

IGBTs S_3 and S_4 are switched on with negative phase current in Figure 3 (c). The negative phase current goes either through IGBT switches S_1 and S_2 or inverse diodes D_3 and D_4. The phase is connected to positive or negative DC bus, respectively. [13]

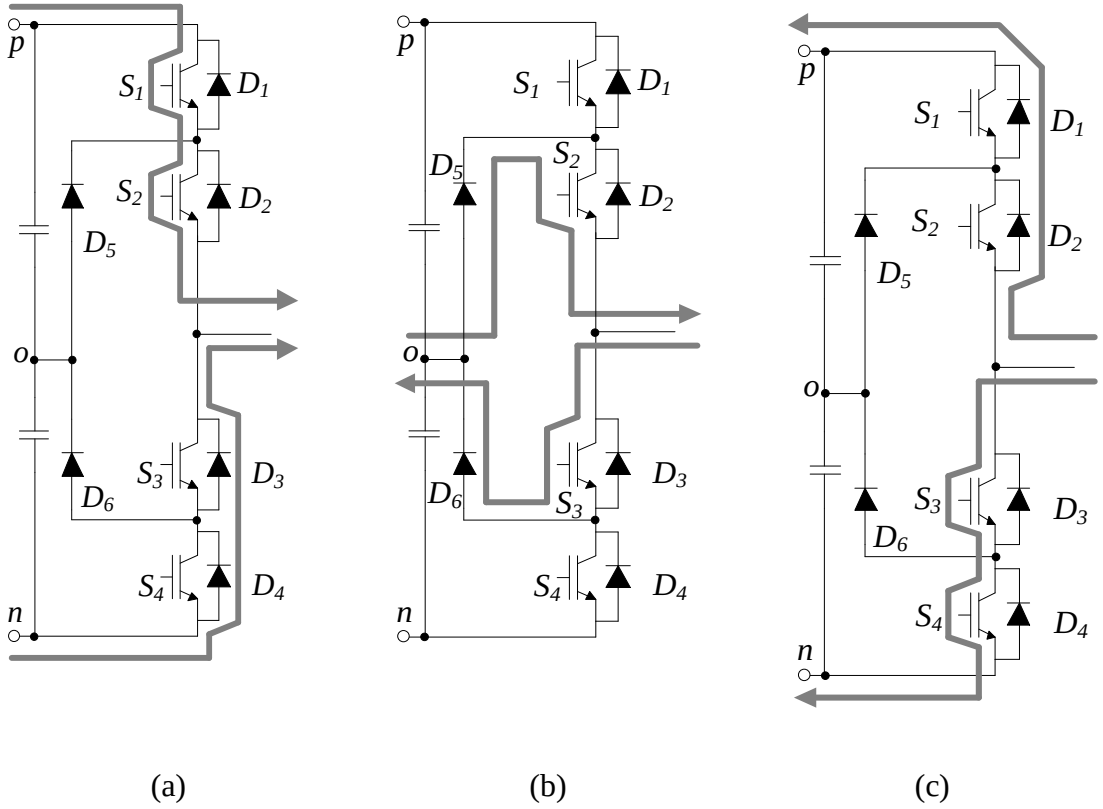


Figure 3. *(a) IGBTs S_1 and S_2 are switched on with positive phase current. (b) IGBTs S_2 and S_3 are switched on. (c) IGBTs S_3 and S_4 are switched on with negative phase current.*

2.2 Output waveform comparison between different inverters

Output voltage waveforms for VSI and NPC inverters are compared in this section. VSI's phase and line-to-line voltages are demonstrated in the Figure 4. Phase voltage of the VSI is the voltage over points '*u*' and '*o*' as shown in Figure 1. Therefore, the DC voltage level is zero. Line-to-line voltage is the voltage over points '*u*' and '*v*'. The given output voltages are produced by square wave operation for simplicity. Each switch operates with 50% duty ratio in square wave operation [8]. Therefore, the output voltages have simple square wave-shape. Since all the three phases are equal, only one phase and line-to-line voltages are presented. The cycle time of the voltages used to demonstrate the operation is 20ms.

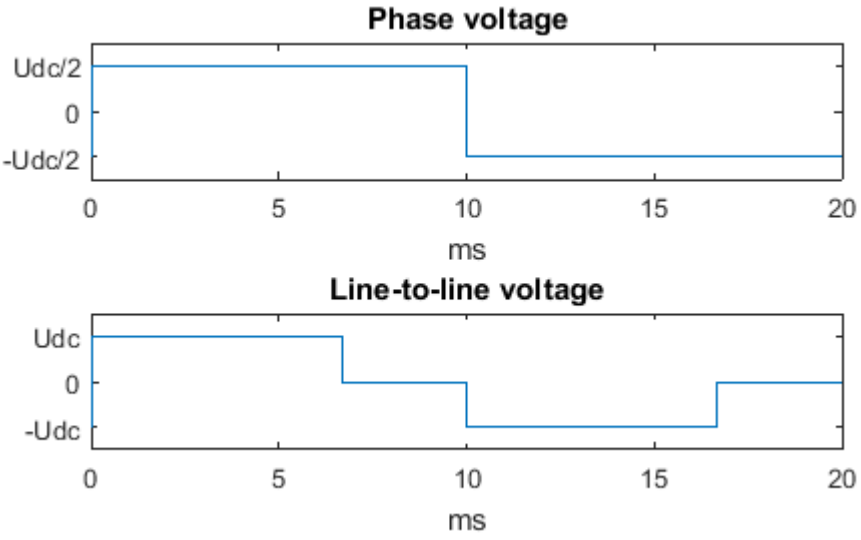


Figure 4. *VSI's phase and line-to-line voltages in square wave operation.*

Phase voltage is connected to the positive DC bus for half of the cycle. The amplitude of phase voltage is half that of the DC bus voltage (i.e. $U_{dc}/2$). During the other half cycle, the phase output is connected to the negative DC bus. Therefore, the phase voltage is $-U_{dc}/2$. Line-to-line voltage is the difference between two phase voltages. Therefore, it is alternately connected to $U_{dc}/2$, 0 and $-U_{dc}/2$ for one third of a cycle each.

Phase and line-to-line voltages produced with the NPC inverter with a 45˚ trigger angle are presented in Figure 5 [7]. Phase and line-to-line voltages equal the same potential differences as explained to VSI previously.

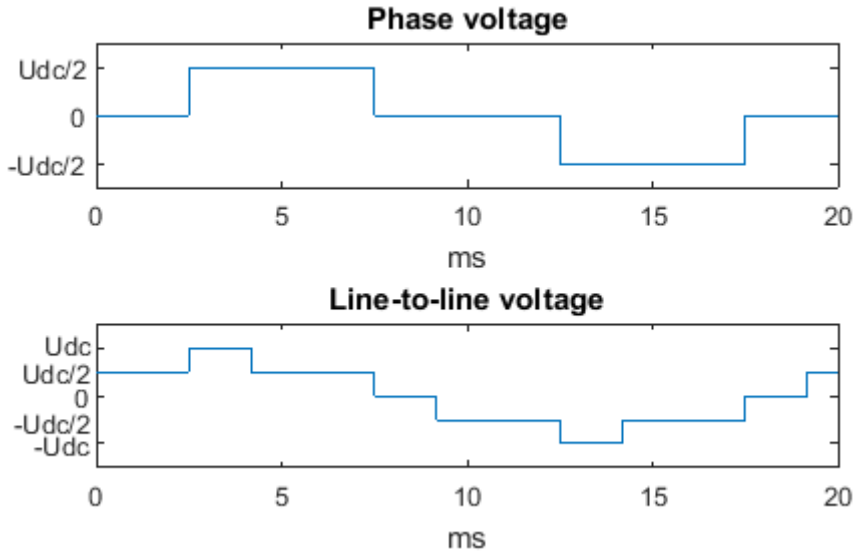


Figure 5. *NPC inverter's phase and line-to-line voltages with 45˚ trigger angle.*

The advantage gained using a three voltage level inverter can be seen by comparing Figure 4 and Figure 5. The phase voltage in the NPC inverter has one more voltage level than in the VSI. Therefore, the line-to-line voltage consists of five values: U_{dc}, $U_{dc}/2$, 0, $-U_{dc}/2$

or -U_{dc}. Thus, the resulting voltage is closer to the desired sinusoidal waveform and contains less harmonic components than VSI inverter.

2.2.1 Harmonics and THD

The harmonic components existing in non-sinusoidal signals and the definition of THD are introduced in this section. Inverter output voltage waveforms are not ideally sinusoidal, as noted in the Chapter 2.2. It is important to understand the concept of harmonics occurring in signal waveforms for further analysis.

Assuming voltage u has no DC component, it can be presented as

$$u(t) = u_1(t) + \sum_{h \neq 1} u_h(t), \tag{2.1}$$

where u_1 is the fundamental component with nominal line frequency f and u_h is the harmonic component of u. The frequency of each harmonic components can be evaluated by

$$f_h = hf_1 \text{ [8].} \tag{2.2}$$

The effect of harmonic component on a fundamental signal is demonstrated in Figure 6. The upper curves present ideally sinusoidal three-phase voltages. The lower curves are the same sinusoidal three-phase voltages containing a third harmonic component.

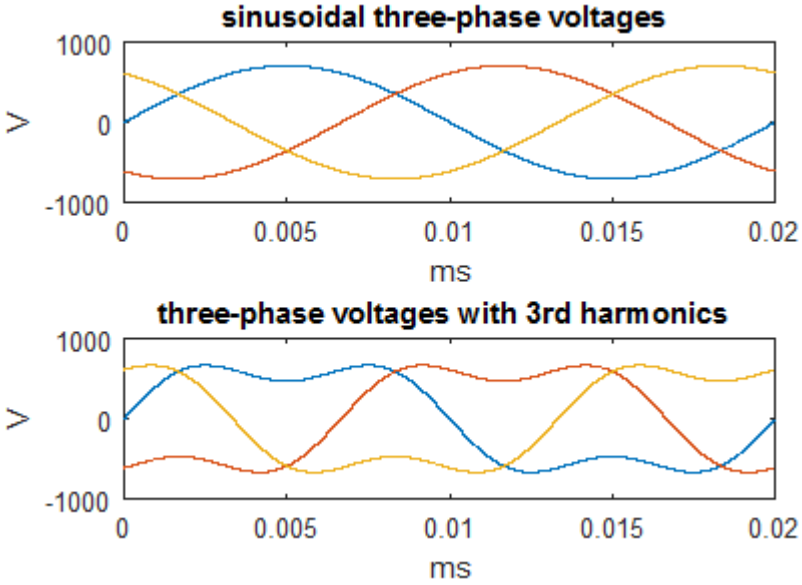


Figure 6. *Ideally sinusoidal three-phase voltages and three-phase voltages added with third harmonic component.*

THD determines the amount of distortion in a signal. It can be calculated for any periodical signal. In order to define THD, distortion component needs to be defined with RMS values first. The total distortion can be defined with voltage u by the following equation:

$$u_h(t) = u(t) - u_1(t), \tag{2.3}$$

where u_h is the total distortion, u is the voltage signal, and u_1 is the fundamental component of signal u. This can be presented in RMS terms of

$$U_h = \sqrt{U^2 - U_1^2}, \tag{2.4}$$

where U_h is RMS value of distortion components, U is the RMS value of signal u, and U_1 is the RMS value of fundamental component of u. THD percent of the voltage u can now be defined as

$$THD = 100\% \cdot \frac{U_h}{U_1} \text{ [8].} \tag{2.5}$$

2.2.2 Fourier analysis

Harmonic components need to be solved to be able to calculate the THD value of a signal. These components can be calculated using Fourier analysis. A periodical signal can be presented as a sum of sinusoidal functions according to the Fourier analysis. The signal is a sum of its fundamental component and harmonic components. A repeating waveform can be presented as [8]

$$u(t) = U_0 + \sum_{h=1}^{\infty}[a_h \cos(h\omega t) + b_h sin(h\omega t)], \tag{2.6}$$

where U_0 is the DC component of the signal u, h is the number of component, a_h is an amplitude of an even component, b_h is an amplitude of an odd component and ω is the angular velocity of the signal. Amplitudes a_h and b_h can be expressed as [8]

$$a_h = \frac{1}{\pi}\int_0^{2\pi} u(t)\cos(h\omega t)\, d(\omega t) \tag{2.7}$$

and

$$b_h = \frac{1}{\pi}\int_0^{2\pi} u(t)\sin(h\omega t)\, d(\omega t), \tag{2.8}$$

where $h = 0, 1, 2, \ldots$ Theoretically, if infinite amount of components are summed, the obtained signal is equivalent to the analyzed signal.

3. GENERAL SPACE VECTOR PWM METHOD

3.1 Introduction

General space vector PWM methods for VSI and NPC inverters are presented in this chapter. The selection of active vectors and on-time calculations are explained in details for both inverters. Section 3.2 introduces a basic space vector theorem. The space vector PWM method for VSI is presented in Section 3.3, and Section 3.4 provides the space vector modulation method for NPC inverter.

Two common methods for inverter modulator signal generation are traditional sine-PWM and space vector PWM methods. Nowadays, every inverter's control system is implemented digitally. This favors the space vector PWM implementations, since it is based on mathematics. Therefore, it is easy to put into practice in microcontroller-based modulators. Space vector PWM method has also other pros compared to sine-PWM as discussed later. Consequently, it is widely studied in recent years.

In general, a good modulator should minimize the switching losses [6], maximize the DC-bus voltage utilization [2] [12], and reduce the output harmonics [12]. In the space vector PWM, the switching losses and output harmonics can be minimized by optimally arranging the order of the applied switching vectors. The space vector PWM provides a better DC-bus voltage utilization than traditional sine-PWM method [9]. The DC-voltage utilization is discussed more thoroughly in the next chapter in Section 4.1.

There are basic steps in the space vector modulation schemes regardless of the number of the voltage levels in the inverter's DC bus. The first step is to locate the reference voltage vector and choose the switching vectors to be used in a modulation period. Next, the switching times are calculated. Finally, the switching cycle and control signals for switches are generated. The required volt-seconds are achieved in the inverter's output, i.e. the voltages in the modulation period equals the reference voltage vector in average [4].

Even though the basics of the space vector PWM schemes are similar for 2L and 3L inverters, the methods are studied separately, since the generation of the optimal modulation sequences varies.

3.2 Space vector theorem

General space vector theorem is presented in this section. The relationship between three-phase variables and space vector will be presented.

Three-phase systems can be calculated more effectively applying space vector theorem. Any time variant three-phase variables u_u, u_v and u_w can be presented by a single vector. The name 'space vector' derives from that any point in space can be defined with three *xyz*- coordinates. Transformation from three-phase variables to complex space vector in $\alpha\beta$ coordinates can be defined using Clarke transformation [3] as

$$\underline{u} = \frac{2}{3}\left(u_u e^0 + u_v e^{\frac{j2\pi}{3}} + u_w e^{\frac{j4\pi}{3}}\right) = u_\alpha + j u_\beta = |\underline{u}| e^{j\theta}, \tag{3.1}$$

where $\underline{u}$ is the resulting space vector, u_u, u_v and u_w are three-phase time domain variables, u_α and u_β are real and imaginary components of the space vector $\underline{u}$, respectively, and θ is the angle between space vector $\underline{u}$ and real axis α. Coefficient $\frac{2}{3}$ is used to retain equal amplitudes between time domain and space vector presentations. Thus, it is used also in this thesis. Simple space vector presentation in complex coordinates is given in the Figure 7.

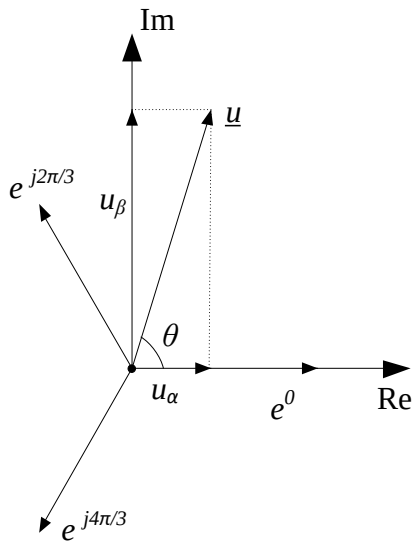


Figure 7. *Space vector presentation in a complex coordinates. Unity vectors used in the space vector definition are also presented.*

It should be noticed that the zero-sequence component is lost during the transformation. The zero-component can be calculated separately as

$$u_0 = \frac{1}{3}(u_u + u_v + u_w). \tag{3.2}$$

Zero-sequence component is canceled in a symmetrical three-phase system. It doesn't have to be taken into account when transforming sinusoidal three-phase variables into a space vector variable.

3.3 Space vector PWM for VSI

Space vector modulation method for VSI used in the simulations of this thesis is presented in this section. It should be noted that the space vector PWM method provided in this section concentrates only in a linear modulation region. An overmodulation region is neglected in the space vector PWM implementation in this thesis, however it is discussed in the next chapter in Section 4.1

VSI has two alternatives where the output of an inverter phase can be connected to: positive or negative DC bus voltage. This approach generates eight different switching vectors. Table 1 presents all the possible switching vectors and corresponding switch states for each switches. The subscripts in the switching vector names denotes whether the phase outputs *u*, *v* and *w* are connected to the positive or negative DC bus voltages. The positive connected phase output is denoted as 'p' when the output voltage is half of the DC bus voltage, i.e. $U_{dc}/2$. The negative connected phase output is marked 'n' and the phase output voltage is - $U_{dc}/2$ in this occasion. Individual IGBT switch states are presented as '1' and '0'. '1' means that the switch is in on-state and conducting, while '0' designates that the switch is in off-state and not conducting. Naming of the switches refers to Figure 1.

Table 1. *Switching vectors and switch states for 2L VSI*

	S_{1u}	S_{2u}	S_{1v}	S_{2v}	S_{1w}	S_{2w}
$\underline{SV}_{pnn}$	1	0	0	1	0	1
$\underline{SV}_{ppn}$	1	0	1	0	0	1
$\underline{SV}_{npn}$	0	1	1	0	0	1
$\underline{SV}_{npp}$	0	1	1	0	1	0
$\underline{SV}_{nnp}$	0	1	0	1	1	0
$\underline{SV}_{pnp}$	1	0	0	1	1	0
$\underline{SV}_{ppp}$	1	0	1	0	1	0
$\underline{SV}_{nnn}$	0	1	0	1	0	1

Switches S_1 and S_2 of each phase leg work as a pair: Switch pairs are not allowed to have the same state in any occasion to avoid short circuiting in DC bus. More about blanking time is discussed in the next chapter in Section 4.2.

The available switching vectors are obtained by replacing the phase output values u_u, u_v and u_w in the equation 3.1 with corresponding voltages $U_{dc}/2$ or $-U_{dc}/2$. In order to clarify the presentation and space vector scheme, the switching vectors are presented in a complex coordinates in Figure 8.

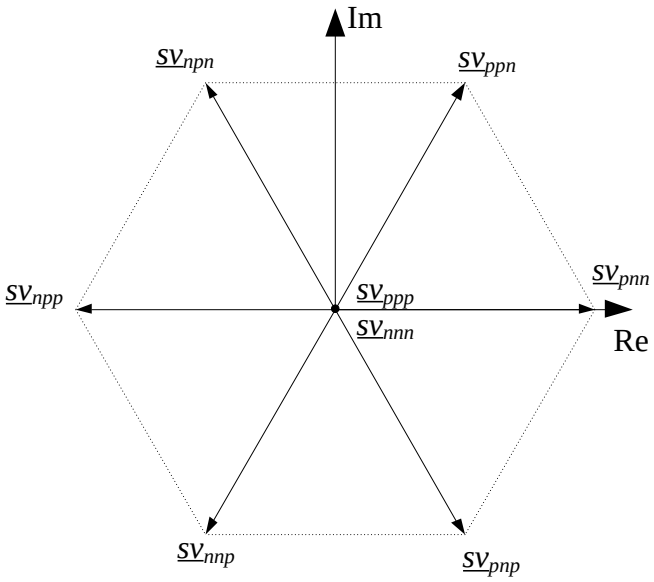


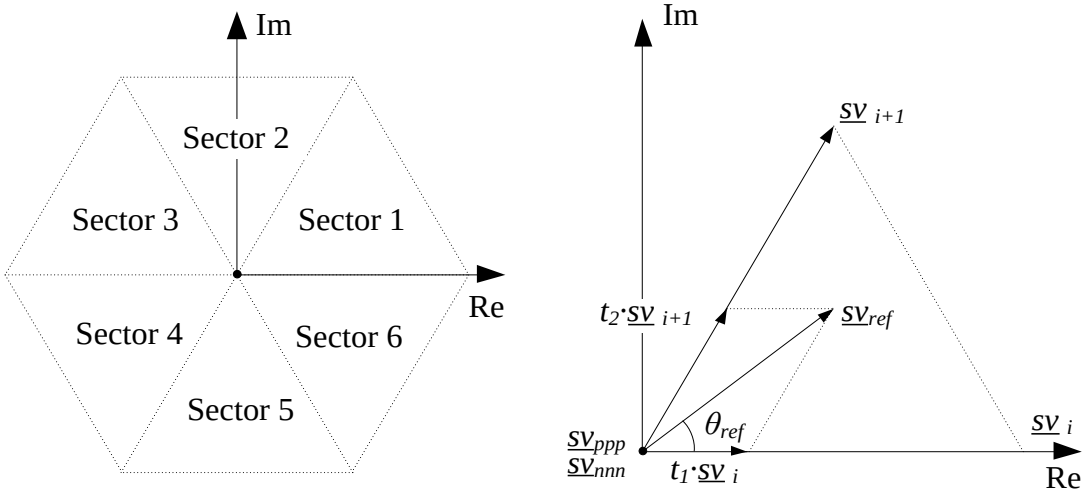
Figure 8. *Switching vectors for VSI in a complex coordinates.*

The switching vectors can be divided in two categories: active vectors and zero vectors. The active vectors are vectors that enables current paths for inverter phase outputs. There are six active vectors and two zero vectors in Figure 8. The lengths of the active vectors are $2/3U_{dc}$ for all the VSI's active vectors. Zero vectors are formed by clamping all the phase outputs to either positive or negative DC bus. Therefore, they don't provide current paths and the resulting switching vector lengths are zero.

3.3.1 Switching times and sequence for VSI

As said, the reference voltage vector is formed by averaging the discrete switching vectors. In order to do this, we need to calculate the switching times. Switching time calculations along with modulation sequence generation are explained in this section.

Switching vector presentation can be divided into six sectors (Figure 9 (a)). All the sectors are symmetric. Thus, the reference switching vector formation presented in the Figure 9 (b) is similar for all the sectors. Reference voltage vector is simply formed by using two nearest active switching vectors in VSI's space vector PWM scheme.



(a) (b)

Figure 9. *Switching vector presentation for VSI divided into six sectors (a). Formation of the reference voltage vector is presented in (b).*

Switching times for reference switching vector located in any of the sectors can be solved using trigonometry by the following equations [15]

$$t_1 = \sqrt{3}\, T_s \frac{|\underline{sv}_{ref}|}{U_{dc}} \sin(\theta_{i+1} - \theta_{ref}) \text{ and} \tag{3.3}$$

$$t_2 = \sqrt{3}\, T_s \frac{|\underline{sv}_{ref}|}{U_{dc}} \sin(\theta_{ref} - \theta_i), \tag{3.4}$$

where t_1 is the switching time for $\underline{sv}_i$, t_2 is the switching time for $\underline{sv}_{i+1}$, T_s is the cycle time of modulation period, $\underline{sv}_{ref}$ is the reference switching vector, U_{dc} is the DC bus voltage, θ_{i+1} is the angle of the switching vector $\underline{sv}_{i+1}$ respective to the real axis, θ_{ref} is the angle of the reference switching vector respective to the real axis and θ_i is the angle of switching vector $\underline{sv}_i$ respective to real axis (Figure 9 (b)).

Application time of zero vectors is easy to compute after t_1 and t_2 have been calculated as

$$t_0 = T_s - t_1 - t_2, \tag{3.5}$$

where t_0 is the switching time for zero vectors. Now we how to select the active vectors and calculate the switching times. An example of a whole modulation period is given in Figure 10.

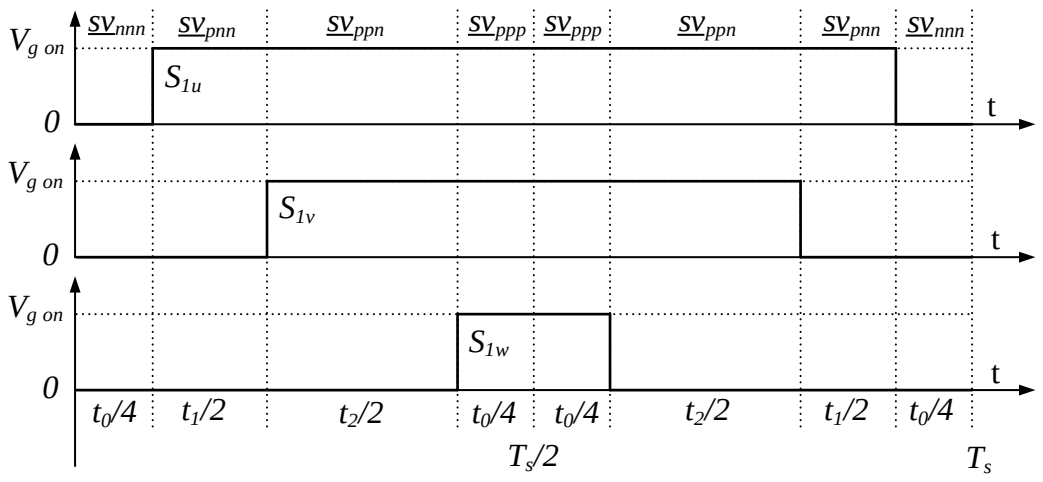


Figure 10. *Upper IGBT switches' control signals and switching vectors applied during one modulation period. The reference switching vector is located in the Sector 1 in this example.*

In this example, the reference vector is located in the Sector 1. The modulation period is divided into eight segments to split the applying time of each switching vector evenly. The modulation period always starts by applying the zero vector $\underline{sv}_{nnn}$ in a space vector scheme for VSI. The $\underline{sv}_{nnn}$ is applied for the time of $t_0/2$. The next applied switching vector is selected so that only one switch state is changed at a time. In this example, it means $\underline{sv}_{pnn}$ is followed by $\underline{sv}_{nnn}$. It is applied for the time of $t_1/2$. The next active vector is $\underline{sv}_{ppn}$ with the applying time of $t_2/2$. After the first and the second active switching vectors are applied, the other zero switching vector $\underline{sv}_{ppp}$ is followed with the switching time of $t_0/4$. After these steps, the sequence is repeated in a reverse order. The resulting switching vector can be stated as

$$\underline{sv}_{ref} = \frac{t_1}{T_s}\underline{sv}_i + \frac{t_2}{T_s}\underline{sv}_{i+1} + \frac{t_0/2}{T_s}\underline{sv}_{ppp} + \frac{t_0/2}{T_s}\underline{sv}_{nnn}. \tag{3.6}$$

As said, the modulation period is generated by carefully choosing the order of the switching vectors. The Table 2 presents the order of the switching vectors in which they should be applied to minimize the state changes during a modulation period.

Table 2. *Order of the switching vectors for VSI.*

	$t_0/2$	t_1	t_2	$t_0/2$	$t_0/2$	t_2	t_1	$t_0/2$
Sector 1	$\underline{SV}_{nnn}$	$\underline{SV}_{pnn}$	$\underline{SV}_{ppn}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppn}$	$\underline{SV}_{pnn}$	$\underline{SV}_{nnn}$
Sector 2	$\underline{SV}_{nnn}$	$\underline{SV}_{npn}$	$\underline{SV}_{ppn}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppn}$	$\underline{SV}_{npn}$	$\underline{SV}_{nnn}$
Sector 3	$\underline{SV}_{nnn}$	$\underline{SV}_{npn}$	$\underline{SV}_{npp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{npp}$	$\underline{SV}_{npn}$	$\underline{SV}_{nnn}$
Sector 4	$\underline{SV}_{nnn}$	$\underline{SV}_{nnp}$	$\underline{SV}_{npp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{npp}$	$\underline{SV}_{nnp}$	$\underline{SV}_{nnn}$
Sector 5	$\underline{SV}_{nnn}$	$\underline{SV}_{nnp}$	$\underline{SV}_{pnp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{pnp}$	$\underline{SV}_{nnp}$	$\underline{SV}_{nnn}$
Sector 6	$\underline{SV}_{nnn}$	$\underline{SV}_{pnn}$	$\underline{SV}_{pnp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{ppp}$	$\underline{SV}_{pnp}$	$\underline{SV}_{pnn}$	$\underline{SV}_{nnn}$

3.4 Space vector PWM for NPC

This section presents how the space vector modulator is implemented in the simulation model of the NPC inverter in this thesis. The basic concept of the space vector modulation is the same for 2L and 3L inverters. 3L inverter has more switching vectors, since the phase output can be connected not only to '*p*' positive or '*n*' negative DC bus, but also to middle point '*o*'. This results more switching vectors, some of which are redundant. This gives a degree of freedom to reference voltage vector generation. Therefore, there are several different space vector PWM methods for NPC inverter studied and introduced in the literature.

Switching vectors and corresponding switch states for 3L NPC inverter are presented in the Table 3.

Table 3. *Switching vectors and switch states for 3L NPC inverter*

	S_{1u}	S_{2u}	S_{3u}	S_{4u}	S_{1v}	S_{2v}	S_{3v}	S_{4v}	S_{1w}	S_{2w}	S_{3w}	S_{4w}
$\underline{SV}_{onn}$	0	1	1	0	0	0	1	1	0	0	1	1
$\underline{SV}_{poo}$	1	1	0	0	0	1	1	0	0	1	1	0
$\underline{SV}_{oon}$	0	1	1	0	0	1	1	0	0	0	1	1
$\underline{SV}_{ppo}$	1	1	0	0	1	1	0	0	0	1	1	0
$\underline{SV}_{opo}$	0	1	1	0	1	1	0	0	0	1	1	0
$\underline{SV}_{non}$	0	0	1	1	0	1	1	0	0	0	1	1
$\underline{SV}_{opp}$	0	1	1	0	1	1	0	0	1	1	0	0
$\underline{SV}_{noo}$	0	0	1	1	0	1	1	0	0	1	1	0
$\underline{SV}_{nno}$	0	0	1	1	0	0	1	1	0	1	1	0
$\underline{SV}_{oop}$	0	1	1	0	0	1	1	0	1	1	0	0
$\underline{SV}_{ono}$	0	1	1	0	0	0	1	1	0	1	1	0
$\underline{SV}_{pop}$	1	1	0	0	0	1	1	0	1	1	0	0
$\underline{SV}_{pon}$	1	1	0	0	0	1	1	0	0	0	1	1
$\underline{SV}_{opn}$	0	1	1	0	1	1	0	0	0	0	1	1
$\underline{SV}_{npo}$	0	0	1	1	1	1	0	0	0	1	1	0
$\underline{SV}_{nop}$	0	0	1	1	0	1	1	0	1	1	0	0
$\underline{SV}_{onp}$	0	1	1	0	0	0	1	1	1	1	0	0
$\underline{SV}_{pno}$	1	1	0	0	0	0	1	1	0	1	1	0
$\underline{SV}_{pnn}$	1	1	0	0	0	0	1	1	0	0	1	1
$\underline{SV}_{ppn}$	1	1	0	0	1	1	0	0	0	0	1	1
$\underline{SV}_{npn}$	0	0	1	1	1	1	0	0	0	0	1	1
$\underline{SV}_{npp}$	0	0	1	1	1	1	0	0	1	1	0	0
$\underline{SV}_{nnp}$	0	0	1	1	0	0	1	1	1	1	0	0
$\underline{SV}_{pnp}$	1	1	0	0	0	0	1	1	1	1	0	0
$\underline{SV}_{ppp}$	1	1	0	0	1	1	0	0	1	1	0	0
$\underline{SV}_{ooo}$	0	1	1	0	0	1	1	0	0	1	1	0
$\underline{SV}_{nnn}$	0	0	1	1	0	0	1	1	0	0	1	1

All the switching vectors are presented in a complex coordinates in the Figure 11. These vectors can be divided into four categories based on their length. The first 12 vectors in the Table 3 are short vectors with the length of *Udc/3*. Each short vector has one redundant short vector pair, as it can be seen in the Figure 11. The next six vectors are medium vectors. The length of the medium vectors is *Udc/√3*. The following six vectors are long vectors with the length of 2/3*Udc*. Neither medium nor long vectors have redundant switching vectors. The last three vectors are mutually redundant zero vectors.

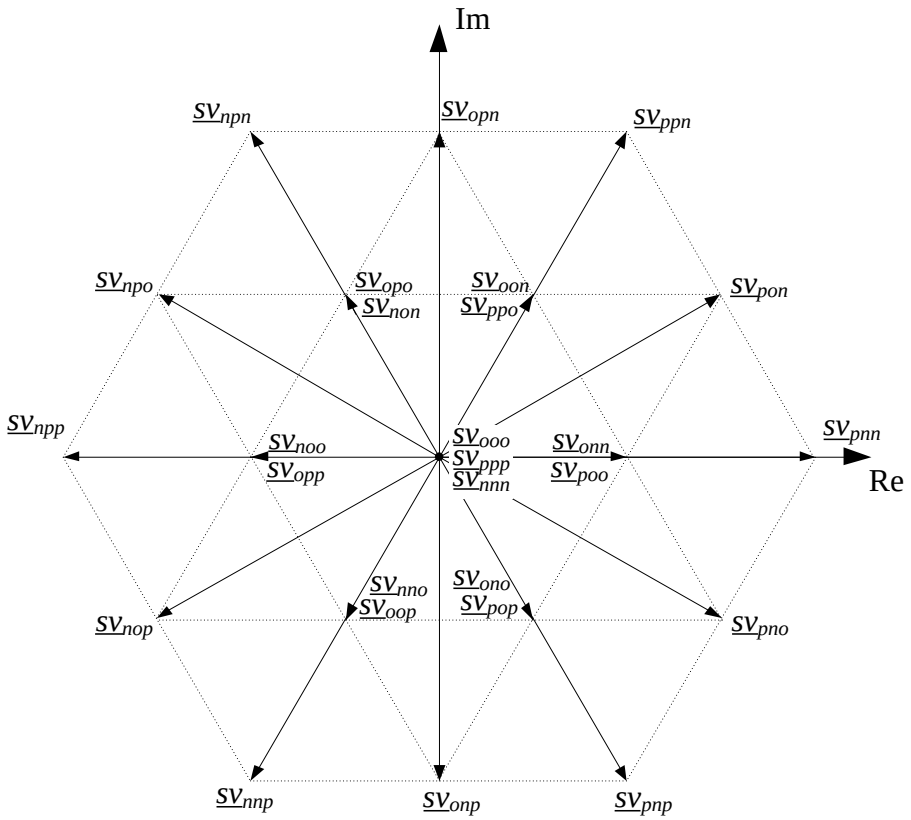


Figure 11. *Switching vectors for NPC inverter in a complex coordinates.*

3.4.1 Switching times and sequence for NPC

This section gives an explanation how the reference voltage vector is located, the switching times are calculated, and the switching sequence is generated.

Determination of the reference voltage vector location is a bit more complicated for NPC than it was for VSI. There are several reference voltage vector location defining methods for NPC inverter presented in the literature. The method implemented in this thesis is presented in the reference material [14] with slight differences. The implementation in this thesis is based on vector angles.

In order to explicitly locate the reference vector, we need to divide the previously introduced switching vector presentation. It is divided into six main sectors and 36 sub-sectors in the Figure 12.

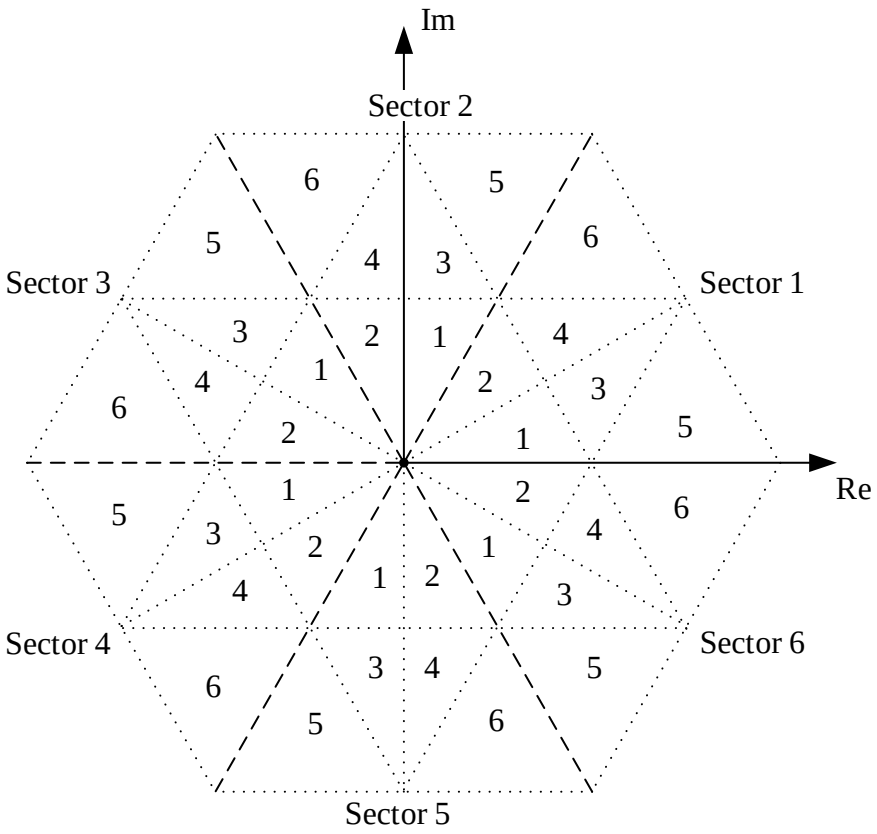


Figure 12. *Switching vectors are divided into six main sectors. Each main sector can be divided into six sub-sectors.*

Main sectors are divided analogously to VSI inverter's switching vector presentation. In addition to VSI implementation, the main sectors are divided into six sub-sectors. The endpoints of the medium and short vectors are used to form the sub-sectors. For now on in this thesis, the sub-sector 2 in the main sector 1 will be referred to S12 etc.

Now we can start to define the location of the reference voltage vector. First, we split the switching vector presentation into six segments presented in Figure 13.

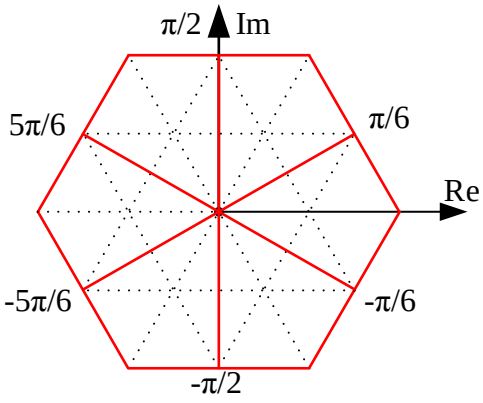


Figure 13. *Segment division for reference voltage vector location detection purposes.*

For example, if the angle of the reference vector respect to real axis is greater than *–π/6*, but smaller than *π/6*, we know that the reference vector must be located either in S11, S13, S15, S62, S64 or S66. This examination can be done similarly with all the reference vector angles. To figure out the precise main and sub-sector, we need to define a new vector $\underline{sv}_{ref2}$ as presented in the Figure 14 (a).

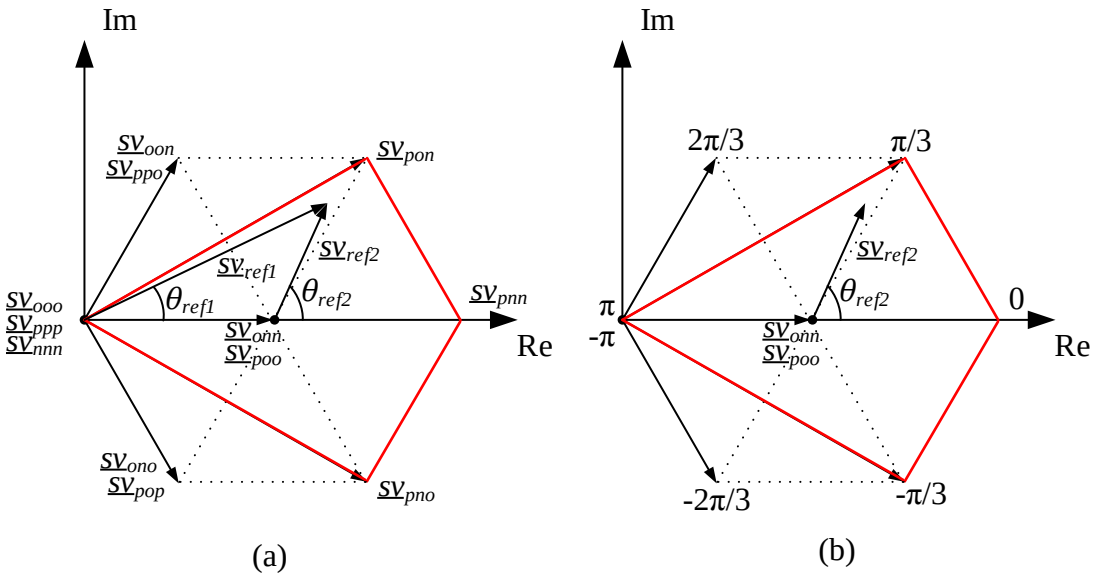


Figure 14. *(a) Definition of the new vector $\underline{sv}_{ref2}$. (b) New angles as switching vector $\underline{sv}_{onn/poo}$ is taken as an origin.*

This method is clarified with an example. The reference voltage vector $\underline{sv}_{ref1}$ is located in the sector S13 in this example. Using a simple vector calculus, the $\underline{sv}_{ref2}$ vector can be defined by the equation

$$\underline{sv}_{ref2} = \underline{sv}_{ref1} - \underline{sv}_{onn}. \tag{3.7}$$

Switching vector $\underline{sv}_{onn}$ can be considered as a new origin of this analysis. It is easy to define the angle of the vector $\underline{sv}_{ref2}$ respect to real axis after execution of equation 3.7. The angle of the $\underline{sv}_{ref2}$ is between $\pi/3$ and $2\pi/3$ in this example. Now we can be certain that the $\underline{sv}_{ref2}$ is located in S13. This method can be done similarly for all the reference vectors located in any main or sub-sectors.

The reference vectors are modulated by using the vectors defining the sub-sector where the reference voltage vector is located. In order to define later calculated switching times for corresponding switching vectors, we need to define explicit numbering of the switching vectors as introduced in the Figure 15.

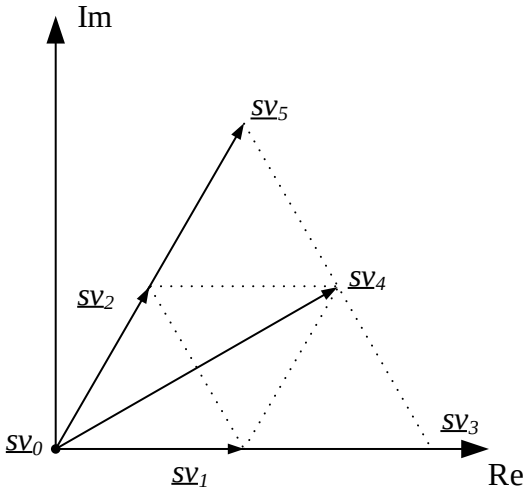


Figure 15. *NPC inverter's switching vector numbering for on-time calculation purposes.*

The modulated voltage vectors can be defined as [11]

$$\underline{sv}_{ref1} = \frac{t_a}{T_S}\underline{sv}_1 + \frac{t_b}{T_S}\underline{sv}_0 + \frac{t_c}{T_S}\underline{sv}_2 \tag{3.8}$$

for sub-sectors 1 and 2,

$$\underline{sv}_{ref1} = \frac{t_a}{T_S}\underline{sv}_1 + \frac{t_b}{T_S}\underline{sv}_4 + \frac{t_c}{T_S}\underline{sv}_2 \tag{3.9}$$

for sub-sectors 3 and 4,

$$\underline{sv}_{ref1} = \frac{t_a}{T_S}\underline{sv}_1 + \frac{t_b}{T_S}\underline{sv}_4 + \frac{t_c}{T_S}\underline{sv}_3 \tag{3.10}$$

for sub-sector 5 and

$$\underline{sv}_{ref1} = \frac{t_a}{T_S}\underline{sv}_5 + \frac{t_b}{T_S}\underline{sv}_4 + \frac{t_c}{T_S}\underline{sv}_2 \tag{3.11}$$

for subsector 6, where the t_a, t_b and t_c are switching times of the switching vectors. These equations applies for all the main sectors. The reference voltage vector just have to be rotated to the first sector to check the corresponding applying times.

The actual switching times t_a, t_b and t_c are calculated next. The calculated switching times applies for all the main sectors. The equations used to calculate the switching times depend on which of the sub-sectors the reference vector is located. The equations are defined in reference material [11] and can be written as

$$t_a = T_s 2K \sin\left(\frac{\pi}{3} - \theta_{ref1}\right) \tag{3.12}$$

$$t_b = T_s \left[1 - 2K\, sin\left(\frac{\pi}{3} + \theta_{ref1}\right)\right] \tag{3.13}$$

$$t_c = T_s 2K sin(\theta_{ref1}) \tag{3.14}$$

for sub-sectors 1 and 2,

$$t_a = T_s\left[1 - 2K\, sin\left(\theta_{ref1}\right)\right] \tag{3.15}$$

$$t_b = T_s \left[2K\, sin\left(\frac{\pi}{3} + \theta_{ref1}\right) - 1\right] \tag{3.16}$$

$$t_c = T_s \left[1 - 2K \sin\left(\frac{\pi}{3} - \theta_{ref1}\right)\right] \tag{3.17}$$

for sub-sectors 3 and 4,

$$t_a = T_s \left[2 - 2K \sin\left(\frac{\pi}{3} + \theta_{ref1}\right)\right] \tag{3.18}$$

$$t_b = T_s 2K \sin(\theta_{ref1}) \tag{3.19}$$

$$t_c = T_s \left[2K \sin\left(\frac{\pi}{3} - \theta_{ref1}\right) - 1\right] \tag{3.20}$$

for sub-sector 5 and

$$t_a = T_s\left[2K \sin\left(\theta_{ref1}\right) - 1\right] \tag{3.21}$$

$$t_b = T_s \left[2K \sin\left(\frac{\pi}{3} - \theta_{ref1}\right)\right] \tag{3.22}$$

$$t_c = T_s \left[2 - 2K \sin\left(\frac{\pi}{3} + \theta_{ref1}\right)\right] \tag{3.23}$$

for sub-sector 6, where $K = \sqrt{3} \cdot |\underline{sv}_{ref1}| / Udc$ [1].

Redundant vectors make it complicated to form switching loss minimized modulation cycles for NPC inverter. The order of the switching vectors in which they should be applied to minimize the state changes is presented in the Table 4. Switching times in the first row of the table are not denoted as t_a, t_b or t_c since the order of the applying times varies between sectors. The order needs to be checked sector sensitively using Figure 15 and equations 3.8-3.11.

Table 4. *Order of the switching vectors for NPC inverter*

	time/4	time/2	time/2	time/4	time/4	time/2	time/2	time/4
Sector 11	$\underline{SV}_{onn}$	$\underline{SV}_{oon}$	$\underline{SV}_{ooo}$	$\underline{SV}_{poo}$	$\underline{SV}_{poo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oon}$	$\underline{SV}_{onn}$
Sector 12	$\underline{SV}_{oon}$	$\underline{SV}_{ooo}$	$\underline{SV}_{poo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{poo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oon}$
Sector 13	$\underline{SV}_{onn}$	$\underline{SV}_{oon}$	$\underline{SV}_{pon}$	$\underline{SV}_{poo}$	$\underline{SV}_{poo}$	$\underline{SV}_{pon}$	$\underline{SV}_{oon}$	$\underline{SV}_{onn}$
Sector 14	$\underline{SV}_{oon}$	$\underline{SV}_{pon}$	$\underline{SV}_{poo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{poo}$	$\underline{SV}_{pon}$	$\underline{SV}_{oon}$
Sector 15	$\underline{SV}_{onn}$	$\underline{SV}_{pnn}$	$\underline{SV}_{pon}$	$\underline{SV}_{poo}$	$\underline{SV}_{poo}$	$\underline{SV}_{pon}$	$\underline{SV}_{pnn}$	$\underline{SV}_{onn}$
Sector 16	$\underline{SV}_{oon}$	$\underline{SV}_{pon}$	$\underline{SV}_{ppn}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppn}$	$\underline{SV}_{pon}$	$\underline{SV}_{oon}$
Sector 21	$\underline{SV}_{oon}$	$\underline{SV}_{ooo}$	$\underline{SV}_{opo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{opo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oon}$
Sector 22	$\underline{SV}_{non}$	$\underline{SV}_{oon}$	$\underline{SV}_{ooo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oon}$	$\underline{SV}_{non}$
Sector 23	$\underline{SV}_{oon}$	$\underline{SV}_{opn}$	$\underline{SV}_{opo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opn}$	$\underline{SV}_{oon}$
Sector 24	$\underline{SV}_{non}$	$\underline{SV}_{oon}$	$\underline{SV}_{opn}$	$\underline{SV}_{opo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opn}$	$\underline{SV}_{oon}$	$\underline{SV}_{non}$
Sector 25	$\underline{SV}_{oon}$	$\underline{SV}_{opn}$	$\underline{SV}_{ppn}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppo}$	$\underline{SV}_{ppn}$	$\underline{SV}_{opn}$	$\underline{SV}_{oon}$
Sector 26	$\underline{SV}_{non}$	$\underline{SV}_{npn}$	$\underline{SV}_{opn}$	$\underline{SV}_{opo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opn}$	$\underline{SV}_{npn}$	$\underline{SV}_{non}$
Sector 31	$\underline{SV}_{non}$	$\underline{SV}_{noo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{noo}$	$\underline{SV}_{non}$
Sector 32	$\underline{SV}_{noo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opp}$	$\underline{SV}_{opp}$	$\underline{SV}_{opo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{noo}$
Sector 33	$\underline{SV}_{non}$	$\underline{SV}_{noo}$	$\underline{SV}_{npo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opo}$	$\underline{SV}_{npo}$	$\underline{SV}_{noo}$	$\underline{SV}_{non}$
Sector 34	$\underline{SV}_{noo}$	$\underline{SV}_{npo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opp}$	$\underline{SV}_{opp}$	$\underline{SV}_{opo}$	$\underline{SV}_{npo}$	$\underline{SV}_{noo}$
Sector 35	$\underline{SV}_{non}$	$\underline{SV}_{npn}$	$\underline{SV}_{npo}$	$\underline{SV}_{opo}$	$\underline{SV}_{opo}$	$\underline{SV}_{npo}$	$\underline{SV}_{npn}$	$\underline{SV}_{non}$
Sector 36	$\underline{SV}_{noo}$	$\underline{SV}_{npo}$	$\underline{SV}_{npp}$	$\underline{SV}_{opp}$	$\underline{SV}_{opp}$	$\underline{SV}_{npp}$	$\underline{SV}_{npo}$	$\underline{SV}_{noo}$
Sector 41	$\underline{SV}_{noo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oop}$	$\underline{SV}_{opp}$	$\underline{SV}_{opp}$	$\underline{SV}_{oop}$	$\underline{SV}_{ooo}$	$\underline{SV}_{noo}$
Sector 42	$\underline{SV}_{nno}$	$\underline{SV}_{noo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oop}$	$\underline{SV}_{oop}$	$\underline{SV}_{ooo}$	$\underline{SV}_{noo}$	$\underline{SV}_{nno}$
Sector 43	$\underline{SV}_{noo}$	$\underline{SV}_{nop}$	$\underline{SV}_{oop}$	$\underline{SV}_{opp}$	$\underline{SV}_{opp}$	$\underline{SV}_{oop}$	$\underline{SV}_{nop}$	$\underline{SV}_{noo}$
Sector 44	$\underline{SV}_{nno}$	$\underline{SV}_{noo}$	$\underline{SV}_{nop}$	$\underline{SV}_{oop}$	$\underline{SV}_{oop}$	$\underline{SV}_{nop}$	$\underline{SV}_{noo}$	$\underline{SV}_{nno}$
Sector 45	$\underline{SV}_{noo}$	$\underline{SV}_{nop}$	$\underline{SV}_{npp}$	$\underline{SV}_{opp}$	$\underline{SV}_{opp}$	$\underline{SV}_{npp}$	$\underline{SV}_{nop}$	$\underline{SV}_{noo}$
Sector 46	$\underline{SV}_{nno}$	$\underline{SV}_{nnp}$	$\underline{SV}_{nop}$	$\underline{SV}_{oop}$	$\underline{SV}_{oop}$	$\underline{SV}_{nop}$	$\underline{SV}_{nnp}$	$\underline{SV}_{nno}$
Sector 51	$\underline{SV}_{nno}$	$\underline{SV}_{ono}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oop}$	$\underline{SV}_{oop}$	$\underline{SV}_{ooo}$	$\underline{SV}_{ono}$	$\underline{SV}_{nno}$
Sector 52	$\underline{SV}_{ono}$	$\underline{SV}_{ooo}$	$\underline{SV}_{oop}$	$\underline{SV}_{pop}$	$\underline{SV}_{pop}$	$\underline{SV}_{oop}$	$\underline{SV}_{ooo}$	$\underline{SV}_{ono}$
Sector 53	$\underline{SV}_{nno}$	$\underline{SV}_{ono}$	$\underline{SV}_{onp}$	$\underline{SV}_{oop}$	$\underline{SV}_{oop}$	$\underline{SV}_{onp}$	$\underline{SV}_{ono}$	$\underline{SV}_{nno}$
Sector 54	$\underline{SV}_{ono}$	$\underline{SV}_{onp}$	$\underline{SV}_{oop}$	$\underline{SV}_{pop}$	$\underline{SV}_{pop}$	$\underline{SV}_{oop}$	$\underline{SV}_{onp}$	$\underline{SV}_{ono}$
Sector 55	$\underline{SV}_{nno}$	$\underline{SV}_{nnp}$	$\underline{SV}_{onp}$	$\underline{SV}_{oop}$	$\underline{SV}_{oop}$	$\underline{SV}_{onp}$	$\underline{SV}_{nnp}$	$\underline{SV}_{nno}$
Sector 56	$\underline{SV}_{ono}$	$\underline{SV}_{onp}$	$\underline{SV}_{pnp}$	$\underline{SV}_{pop}$	$\underline{SV}_{pop}$	$\underline{SV}_{pnp}$	$\underline{SV}_{onp}$	$\underline{SV}_{ono}$
Sector 61	$\underline{SV}_{ono}$	$\underline{SV}_{ooo}$	$\underline{SV}_{poo}$	$\underline{SV}_{pop}$	$\underline{SV}_{pop}$	$\underline{SV}_{poo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{ono}$
Sector 62	$\underline{SV}_{onn}$	$\underline{SV}_{ono}$	$\underline{SV}_{ooo}$	$\underline{SV}_{poo}$	$\underline{SV}_{poo}$	$\underline{SV}_{ooo}$	$\underline{SV}_{ono}$	$\underline{SV}_{onn}$
Sector 63	$\underline{SV}_{ono}$	$\underline{SV}_{pno}$	$\underline{SV}_{poo}$	$\underline{SV}_{pop}$	$\underline{SV}_{pop}$	$\underline{SV}_{poo}$	$\underline{SV}_{pno}$	$\underline{SV}_{ono}$
Sector 64	$\underline{SV}_{onn}$	$\underline{SV}_{ono}$	$\underline{SV}_{pno}$	$\underline{SV}_{poo}$	$\underline{SV}_{poo}$	$\underline{SV}_{pno}$	$\underline{SV}_{ono}$	$\underline{SV}_{onn}$
Sector 65	$\underline{SV}_{ono}$	$\underline{SV}_{pno}$	$\underline{SV}_{pnp}$	$\underline{SV}_{pop}$	$\underline{SV}_{pop}$	$\underline{SV}_{pnp}$	$\underline{SV}_{pno}$	$\underline{SV}_{ono}$
Sector 66	$\underline{SV}_{onn}$	$\underline{SV}_{pnn}$	$\underline{SV}_{pno}$	$\underline{SV}_{poo}$	$\underline{SV}_{poo}$	$\underline{SV}_{pno}$	$\underline{SV}_{pnn}$	$\underline{SV}_{onn}$

4. REQUIREMENTS FOR ADVANCED SPACE VECTOR MODULATOR

Chapter 3 introduced the basic space vector PWM schemes and explained how the modulation is implemented in the simulation models in this thesis. This chapter concentrates on special requirements a practical well-implemented space vector modulator needs to include. The requirements discussed in this chapter are modulator working in the overmodulation region, insertion and compensation of a blanking time, minimum times between the IGBT's control pulses, DC capacitors unbalance and loss optimal switching scheme. It should be noted that the methods explained in this chapter are not implemented in the simulation models presented in Chapter 5.

4.1 Limit on amplitude of the reference voltage vector

The operation of the modulator can be divided in two regions based on the length of the reference voltage vector. The sections are linear modulation and overmodulation regions. These regions are clarified in the Figure 16.

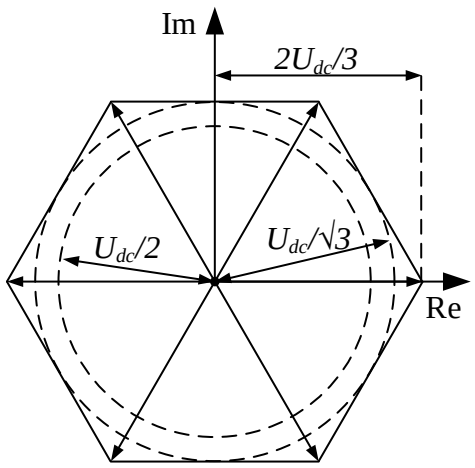


Figure 16. *DC voltage utilization in different modulation methods.*

The amplitude of the reference voltage vector needs to be limited to ensure that the operation will be in the linear modulation region. The maximum length of the reference vector is $U_{dc}/\sqrt{3}$ when using space vector modulation method. That equals the length of the medium switching vectors of NPC inverter. It applies for both, VSI and NPC inverters. The outer circle in the Figure 16 illustrates the boundary between linear and overmodulation regions in space vector PWM. It can be seen that a vector with the length over $U_{dc}/\sqrt{3}$ can exceed the sector defined by long switching vectors with the length of $2U_{dc}/3$. Thus, it would be require overmodulation operation.

The inner circle with the length of $U_{dc}/2$ demonstrates the maximum linearly modulated phase voltage amplitude when using a traditional sine-PWM method [8]. Therefore, the DC voltage utilization is roughly 15% better in space vector implementations. This is one of the reasons the space vector PWM has overtaken the traditional modulation scheme.

The term modulation index m is used in the simulations of this thesis. It refers to the length of the reference voltage vector compared to the DC voltage U_{dc} divided by $\sqrt{3}$ and can be written as

$$m = \frac{|\underline{sv}_{ref}|}{U_{dc}/\sqrt{3}}. \tag{4.1}$$

4.2 Blanking time

IGBTs are not ideal switches. Real life switches have turn-on and turn-off delay times, and finite rise and fall times. When it comes to a voltage source inverters, a well-implemented modulator needs to make sure that a short circuiting between DC busses are avoided. This phenomenon is prevented by adding delay to the on-switching instants. The time used to delay the on-switching instants is called a blanking time [8]. Unintentional short circuiting during IGBT switch state changes would cause undesired effects, such as additional losses, increased wear of the components and decreased MTTF. Long enough short circuiting can easily destroy the IGBT modules at once. The blanking time is typically few microseconds with today's IGBT technology. Blanking time effect on switching pulses is presented in the Figure 17.

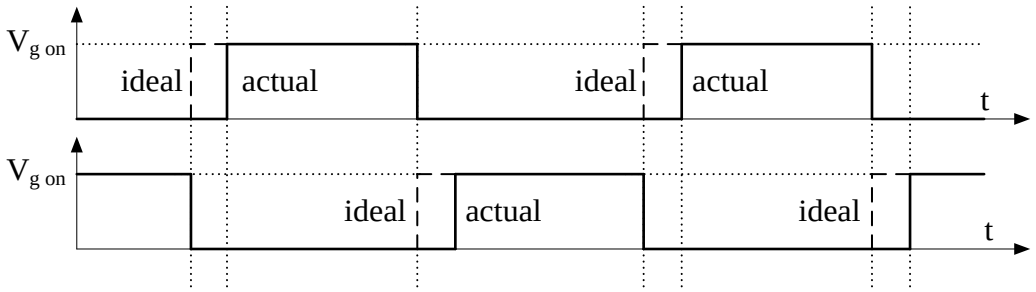


Figure 17. *Blanking time implementation to IGBTs' control signals. On-time signals are delayed with blanking time.*

Dashed line represents the ideal switching instants. The actual switching pulse is provided after the blanking time. Blanking time is drawn relatively too long compared to the switching time to make the presentation clearer.

There is no voltage provided to the inverter's output phase during the blanking time. This cause changes to the output voltage. The change is either positive or negative, depending on the direction of the current [8].

4.3 Minimum pulse-width time

A minimum pulse-width time limitation is another requirement deriving from IGBT switch non-idealities. The minimum pulse-width time requirement relates to a small on-time control pulse durations [17]. It is desired to allow the IGBT module to fully change its state between changes in the control pulse. This manner is applied to avoid IGBT switch failures [17]. Pulses with a length less than the minimum allowed time can be either dropped, or applied for a specified time duration. Figure 18 presents the situation, when the pulses are applied for a minimum pulse-width time.

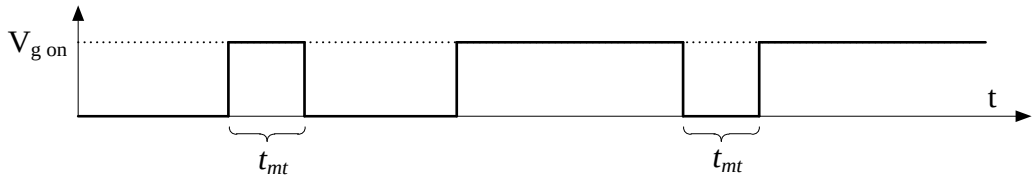


Figure 18. *Implementation of the minimum pulse-width time in control pulse of an individual IGBT switch.*

The minimum off-time is also controlled in the implementation presented. This is because the IGBTs work as a pairs as stated earlier. There is always another switch, which is in on-state during the off-state of the studied switch. Therefore, also the off-time cannot be shorter than the defined minimum pulse. The minimum pulse-width time has an effect on the resulted output voltages.

4.4 Minimum time between successive pulses

Time between the state changes in different phase legs of an inverter should also be discussed [16]. A well implemented modulator should be safe and reliable to use in motor applications. Requirement of the minimum time between successive pulses relate to the motor utilizations. Modulator needs to prevent instantaneous state changes between two different phase outputs. The magnitudes of line-to-line voltage transients are doubled if this is not prevented. It is obvious that not preventing this kind of operation would cause a damage to the motor insulation.

It is also desired that the oscillation occurring in motor cables after state changes has enough time to settle. If consecutive pulse is applied too early, the previous oscillation seen in the cables hasn’t necessarily settled. It is possible that the previous oscillation pulse adds up with the new state change. Usually, the implemented criterion of minimum time between successive pulses is few microseconds [16].

4.5 DC-bus unbalance

The DC capacitors may be loaded differently during modulation periods. This is an issue with the multilevel inverters, such as NPC. DC-bus unbalance causes some movements to the switching vectors. It should be noted that the redundant short vectors move to different directions if the capacitors are unbalanced as shown in the Figure 19.

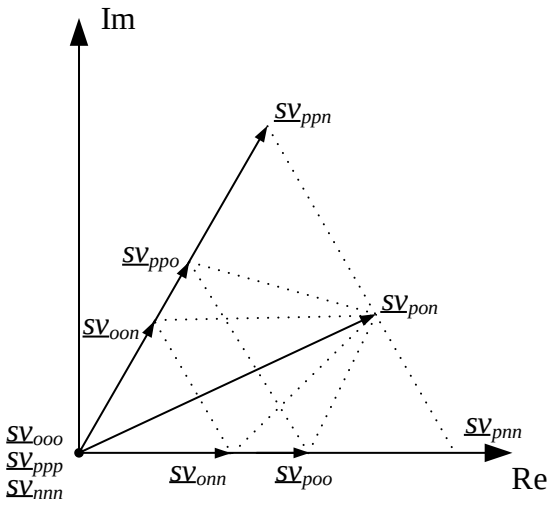


Figure 19. *Unbalance in the DC bus capacitors causes movement to the switching vectors.*

The situation presented in the Figure 19 is a consequence of the capacitor C_1 having a greater voltage than the capacitor C_2 (Figure 2). This kind of voltage drifting can be handled with an advanced modulation algorithm. More of it can be read from the reference material [10].

4.6 Loss optimal modulation scheme

There are multiple modulation methods presented in the literature to minimize the switching losses. A method presented in reference material [6] is discussed in this section. The basic of the method is that there are sections in the inverter's phase outputs when the output state is not changed. It is said that the phase output is 'clamped' to a certain DC bus. The 'no-switching' period is located in the middle of the peak of the load current to minimize the switching losses. In order to locate the 'no-switching' instants, the load power factor must be known.

Switching losses depends on the actual number of switching events per switching cycle. Switching losses can be decreased at least by 33% applying 'no-switching' periods for 60 degrees per modulation cycle for each phase outputs [6].

5. SIMULATIONS

Simulink® models used in the simulations are presented in this chapter along with the simulation results conducted with them. The construction and simplifications of the models are introduced. Simulations with different switching frequencies and modulation indexes were executed with the VSI and NPC inverter models. THD values of line-to-line voltages and phase currents are compared in the results.

5.1 Simulation model of VSI

A top-level model of the control signal generation for the VSI is presented in the Figure 20.

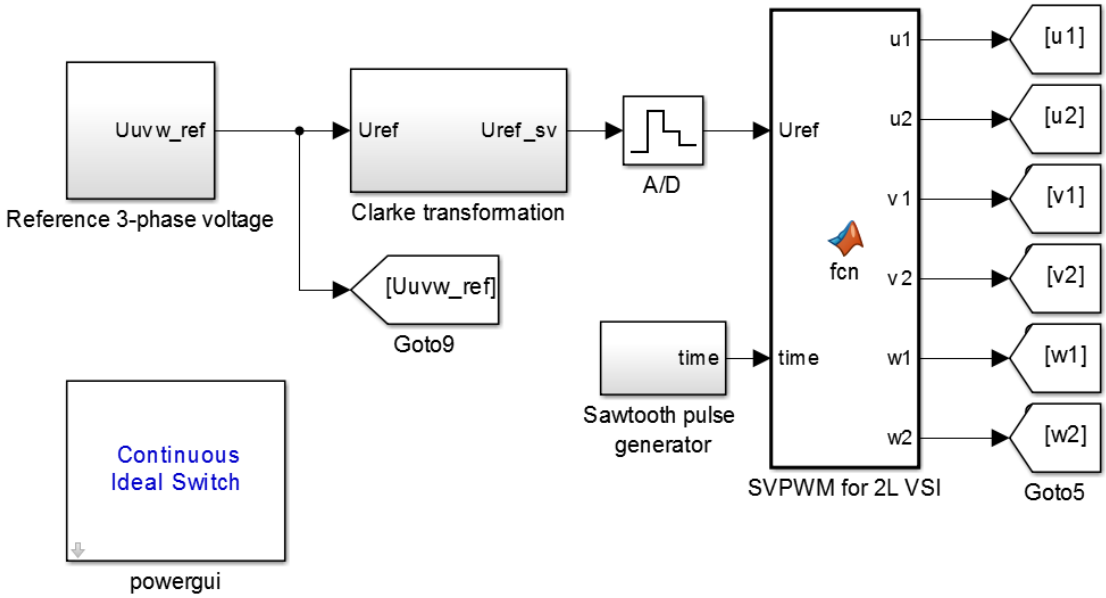


Figure 20. *The control signal generation model for the VSI.*

Three-phase time domain reference voltages are created in the subsector called 'Reference 3-phase voltage'. These three-phase variables are transformed into a space vector variable by Clarke transformation. This space vector is digitalized in the 'A/D' block. The sample time of the analog-to-digital conversion is being set to $1/f_{sw}$.

The actual space vector PWM is carried out in the MATLAB® function block denoted 'SVPWM for 2L VSI'. The code for the VSI space vector PWM is provided in the Appendix A. Ideal switching devices are selected from the Simulink®'s powergui block.

The main circuit model of the VSI is given in the Figure 21.

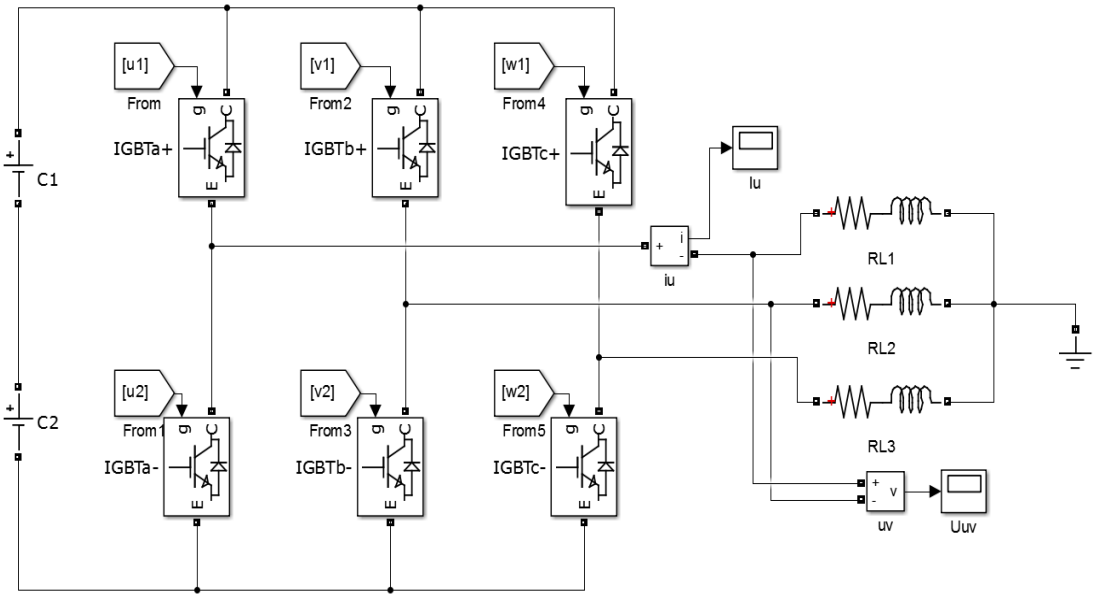


Figure 21. *VSI's main circuit model.*

The phase load is implemented with a simple resistor and inductor connected in series. Each phase output has an equal load. MATLAB's scopes are being used to save data of the phase current and line-to-line voltage. The data is later used to analyze the THD content of the particular variables. The analyzation of the data is implemented using powergui's integrated FFT analysis tool. It is a simple and effective way to solve the THD value of the data. It also provides information about the harmonic component frequencies and magnitudes.

5.2 Simulation model of NPC

Simulink model of the NPC inverter's control signal generation is given in the Figure 22. The model is similar to the implementation of the VSI's control signal generation. NPC inverter has 12 IGBT switches in the main circuit. Therefore, the difference between these two models is that there are 12 gate signals created in the '3L NPC SVPWM' block. The code used for space vector PWM scheme is available in the Appendix B.

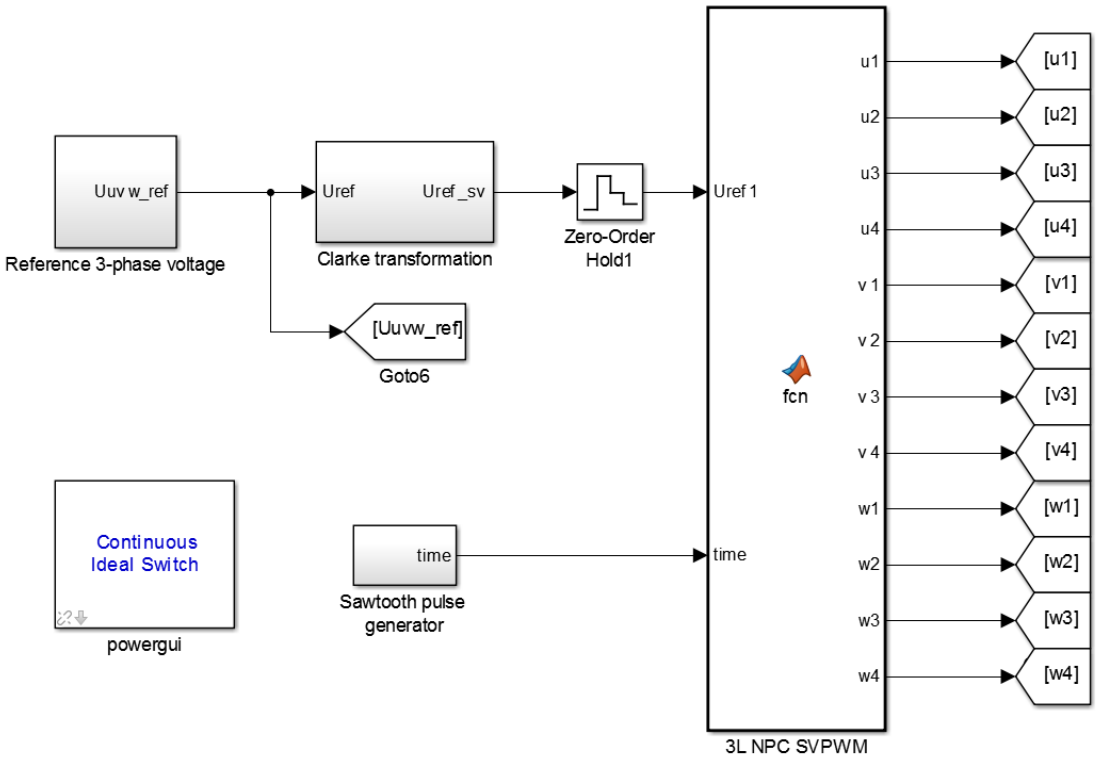


Figure 22. *The control signal generation model for the NPC inverter.*

The main circuit model of the NPC inverter can be seen in the Figure 23. It is modeled accordingly to the NPC's main circuit presented in the Figure 2. The load used in the phase outputs is the same as used for VSI model: Series connected *RL* circuits. Scopes are used to save desired voltage and current data.

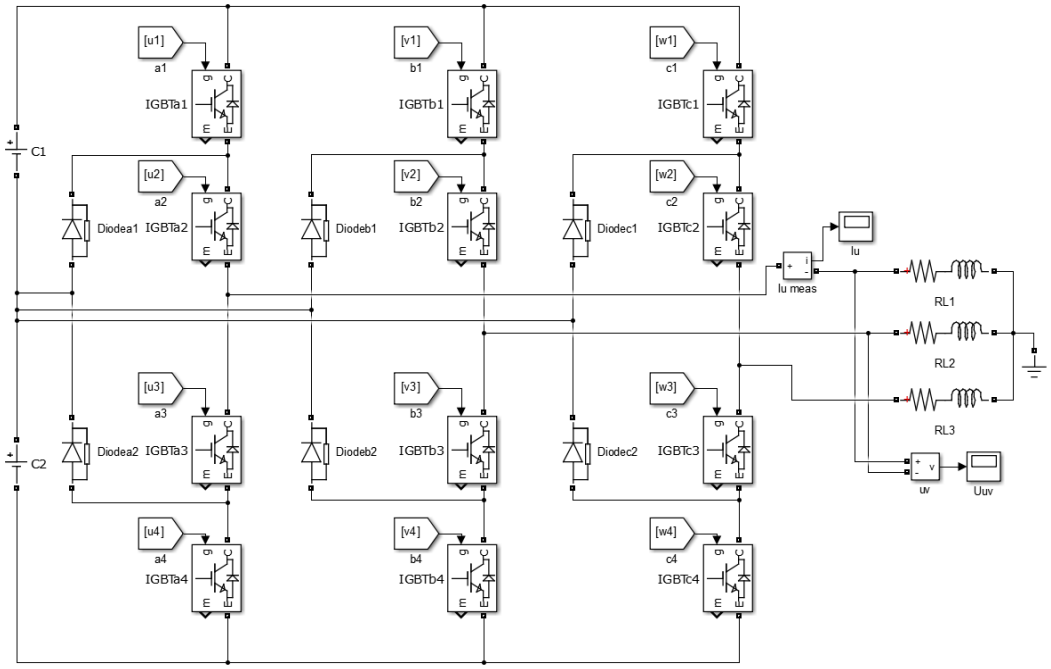


Figure 23. *NPC inverter's main circuit model.*

5.3 Inverters' voltage and THD with different switching frequencies

Effects of the different switching frequencies on the line-to-line voltage harmonics between VSI and NPC inverters are studied in this section. The studied voltage is the line-to-line voltage provided between inverter's phase outputs '*u*' and '*v*'. Parameters for these simulations are provided in the Table 5. The frequency of the reference phase voltage is 50 Hz.

Table 5. *Parameters for voltage THD comparison simulations with different* f_{sw}.

variable	value
U_{dc} (V)	690·√2
R_{load} (Ω)	10.0
L_{load} (H)	1.0
m	1.0

The different switching frequencies used in the simulations are 1, 2, 3, 5, 10, 15, 20 and 30 kHz. The THD results with all the simulated frequencies are given later in this section. The resulting voltage waveforms along with FFT analysis are provided for 1, 10 and 30 kHz simulations. The VSI model's line-to-line voltage and FFT analysis obtained with switching frequency of 1 kHz are presented in the Figure 24.

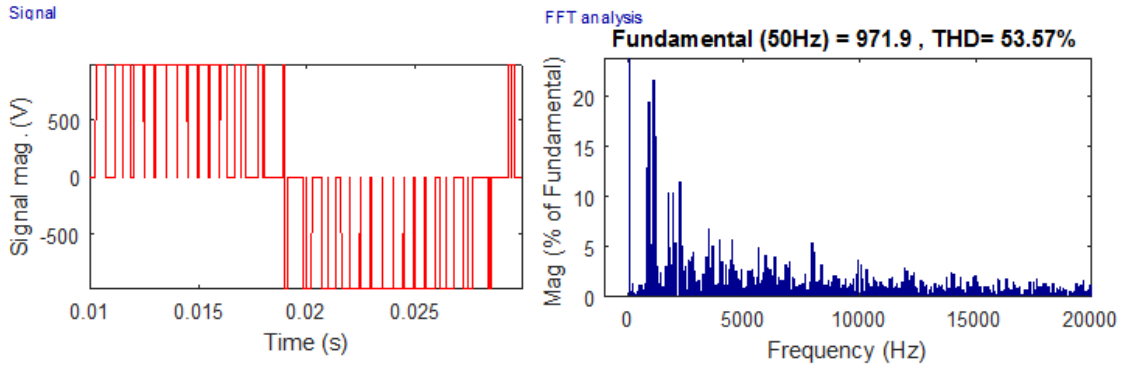


Figure 24. *VSI's line-to-line voltage and FFT analysis with f_{sw}=1 kHz.*

1 kHz is a relatively low switching frequency when it is desired to modulate a signal which a frequency is 50 Hz. As a result, the state changes in the line-to-line voltage can easily be seen in the waveform. Harmonics with the greatest magnitude are located at the multiples of the switching frequency. Magnitudes of the harmonic components are given as a percentage value of the fundamental component in the FFT analysis graph.

The VSI model's voltage waveform and FFT analysis simulated with f_{sw} = 10 kHz are given in the Figure 25.

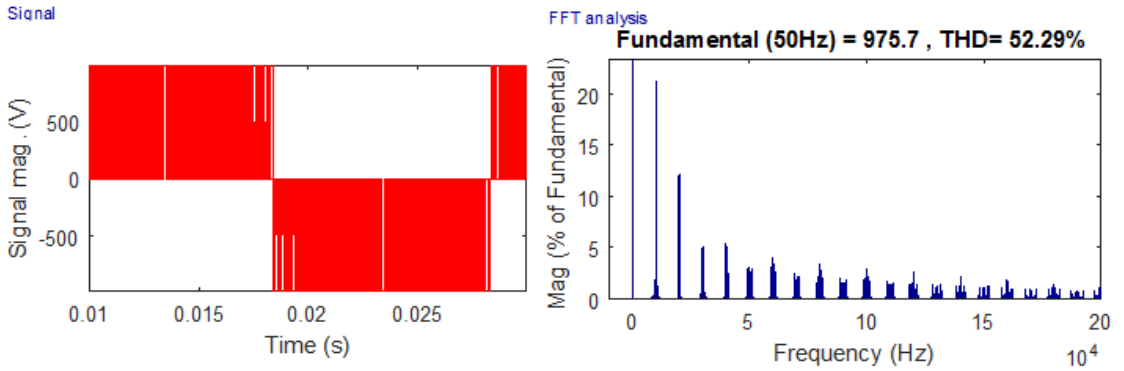


Figure 25. *VSI's line-to-line voltage and FFT analysis with f_{sw}=10 kHz.*

10 kHz is more reasonable switching frequency than 1 kHz when modulating a 50 Hz signal. The state changes in voltage waveform cannot be seen in the figure given. The harmonic components are located at higher frequencies when compared to results gained with 1 kHz switching frequency. This goes well with the fact that the harmonic peaks are located at the multiples of the switching frequency. The first significant harmonic component peak is at 10 kHz, the second is at 20 kHz etc.

Last given VSI's waveforms of the line-to-line voltage and FFT analysis simulated with f_{sw} = 30 kHz are given in the Figure 26.

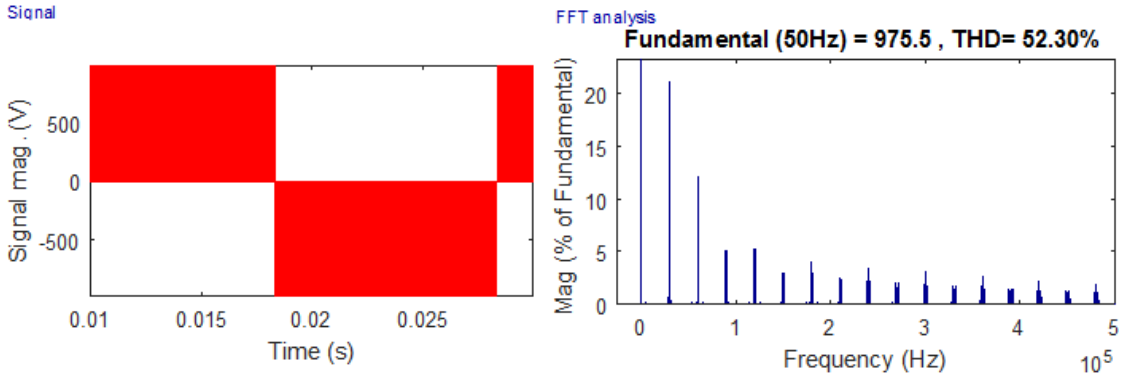


Figure 26. *VSI's line-to-line voltage and FFT analysis with f_{sw}=30 kHz.*

The difference to the previous simulation is that the harmonic components are moved to higher frequencies. 30 kHz is a relatively high switching frequency for today's IGBT technology. Using it as a switching frequency would cause a lot of switching losses in a practical inverter.

The same simulations with the same parameters are executed with the NPC inverter model. Figure 27 gives the NPC inverter's line-to-line voltage waveform and FFT analysis with f_{sw} = 1 kHz.

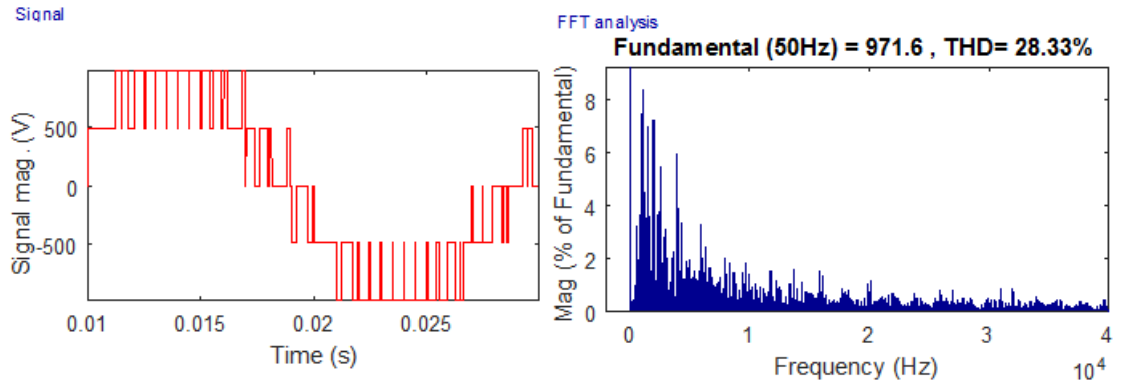


Figure 27. *NPC's line-to-line voltage and FFT analysis with f_{sw}=1 kHz.*

There are five voltage levels in the line-to-line voltage of the NPC inverter. This gives the voltage more sinusoidal shape when comparing to voltages gained with the VSI and three available voltage levels. The harmonic components are spread mostly in the frequencies under 10 kHz. The greatest harmonic peak is theoretically at 1 kHz. As said, 1 kHz is a relative low frequency for this kind of modulation. Real life inverters use greater switching frequencies for modulation.

Figure 28 gives NPC inverter's voltage waveform and FFT analysis with f_{sw} = 10 kHz.

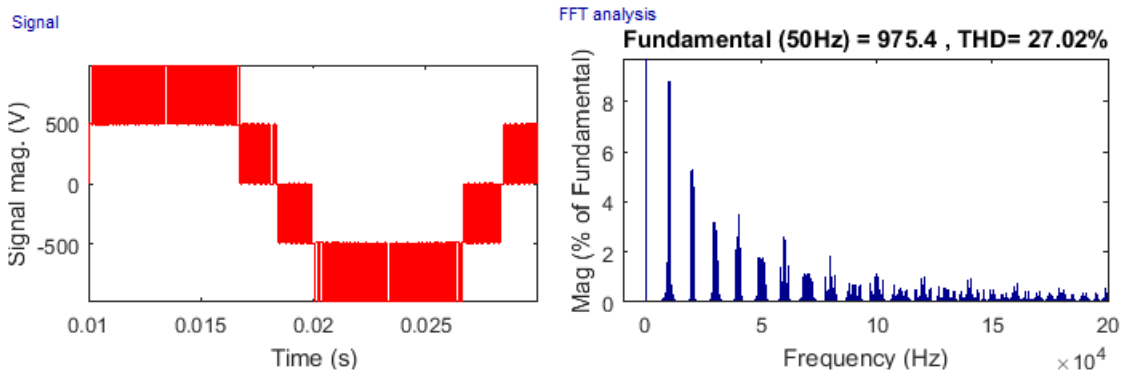


Figure 28. *NPC's line-to-line voltage and FFT analysis with f_{sw}=10 kHz.*

The harmonic component peaks can clearly be indicated to multiples of the switching frequency in the Figure 28. Finally, the NPC voltage waveform and FFT analysis are simulated with the switching frequency of 30 kHz in the Figure 29.

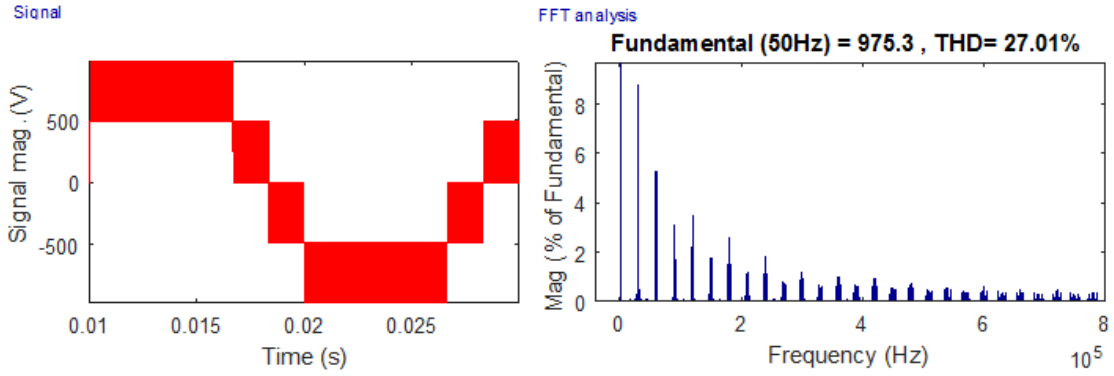


Figure 29. *NPC's line-to-line voltage and FFT analysis with f_{sw}=30 kHz.*

The results gained with the VSI inverter with different switching frequencies are collected in the Table 6.

Table 6. *Fundamental line-to-line voltage amplitudes and THD values of the VSI.*

f_{sw} (kHz)	$\hat{U}_{uv}$ (V)	THD_{uv} (%)
1	971.9	53.57
2	974.7	52.60
3	975.2	52.28
5	975.5	52.34
10	975.7	52.29
15	975.7	52.28
20	975.4	52.32
30	975.5	52.30

It is logical that the changes in the switching frequency doesn't affect to the amplitudes of the line-to-line voltages. It is also worth noting that increasing the switching frequency doesn't affect to the THD value of the voltage seen in the inverter's output phases. It only relocates the harmonic components to greater frequencies, as can be seen in the FFT analysis graphs.

Fundamental line-to-line voltage amplitudes and THD values obtained with NPC inverter simulations are presented in the Table 7.

Table 7. *Fundamental line-to-line voltage amplitudes and THD values of the NPC.*

f_{sw} (kHz)	$\hat{U}_{uv}$ (V)	THD_{uv} (%)
1	971.6	28.33
2	974.5	27.34
3	975.0	26.88
5	975.3	27.05
10	975.4	27.02
15	975.5	26.99
20	975.3	27.02
30	975.3	27.01

The amplitudes of the line-to-line voltages are the same as amplitudes obtained with VSI simulations. The difference between these two inverter's output voltages is that the THD value in the NPC's voltage is roughly half of the THD value in the VSI's voltage. This observation is presented in the Figure 30.

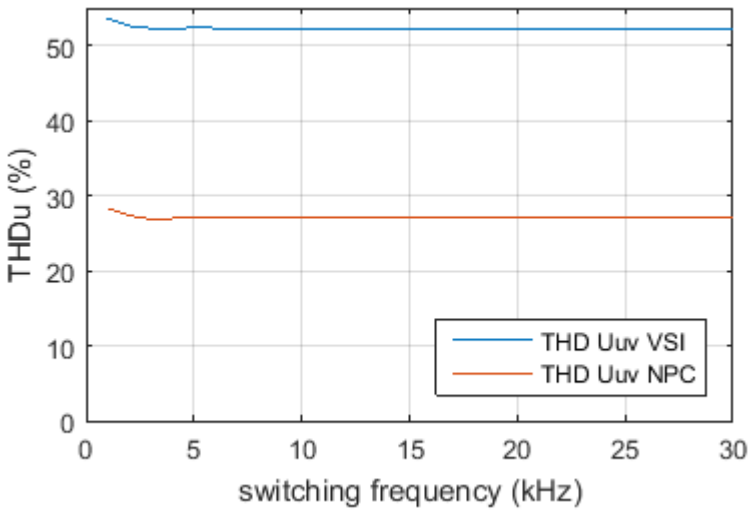


Figure 30. *Line-to-line voltage's THD comparison between VSI and NPC with different switching frequencies.*

5.4 Inverters' phase current and THD with different switching frequencies

This section studies the differences between phase current THD values of the VSI and NPC inverters. The phase current examined in these simulations is the current provided by the inverter's phase output '*u*' to the *RL* load. Parameters for simulations presented in this section are provided in the Table 8.

Table 8. *Parameters for phase current THD comparison simulations with different* f_{sw}.

variable	value
U_{dc} (V)	690·√2
R_{load} (Ω)	10.0
L_{load} (H)	1.0
m	1.0

All the simulated switching frequencies are 1, 2, 3, 5, 10, 15, 20 and 30 kHz. Current waveforms and FFT analysis of simulations with switching frequency 1, 10 and 30 kHz are presented. Figure 31 gives a presentation of the current waveform simulated with VSI model and 1 kHz switching frequency.

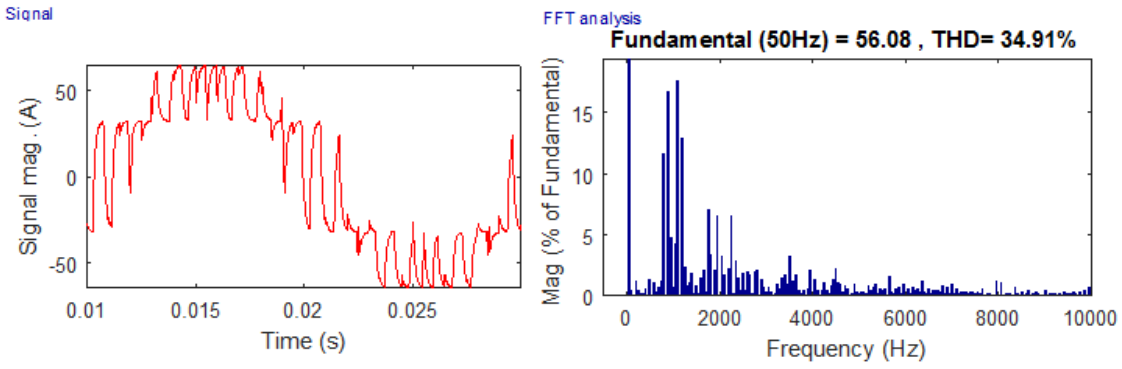


Figure 31. *VSI's phase current waveform and FFT analysis with* f_{sw}*=1 kHz.*

There are intense transitions in the current waveform. The output filter would require a massive inductance to smoothen the phase current harmonics to a reasonable level. The biggest peak magnitudes of the current harmonics are located around 1 and 2 kHz: The multiples of the switching frequency.

The simulated phase current and FFT analysis of the VSI with f_{sw} = 10 kHz is given in the Figure 32.

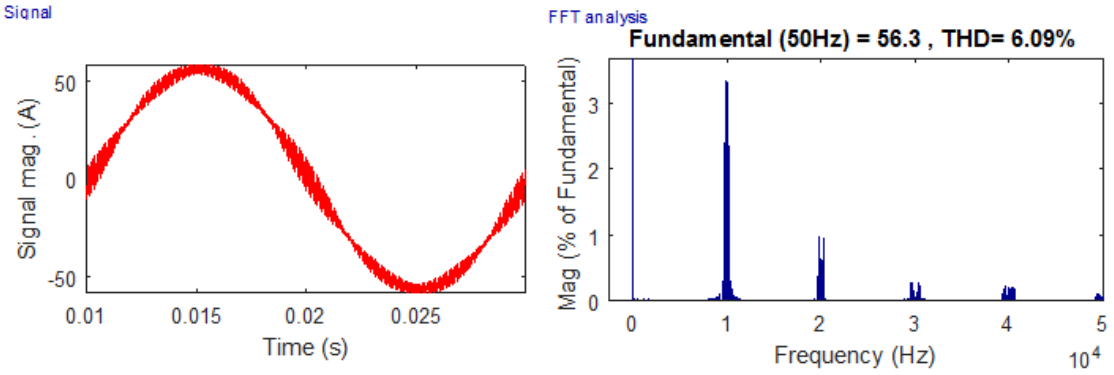


Figure 32. *VSI's phase current waveform and FFT analysis with f_{sw}=10 kHz.*

The phase current waveform is much more sinusoidal than with 1 kHz switching frequency. Thus, the THD value is decreased significantly. Relative magnitudes of the dominant harmonic components are reduced and located more clearly at the multiples of the switching frequency.

VSI's phase current and FFT analysis simulated with f_{sw} = 30 kHz is presented in the Figure 33.

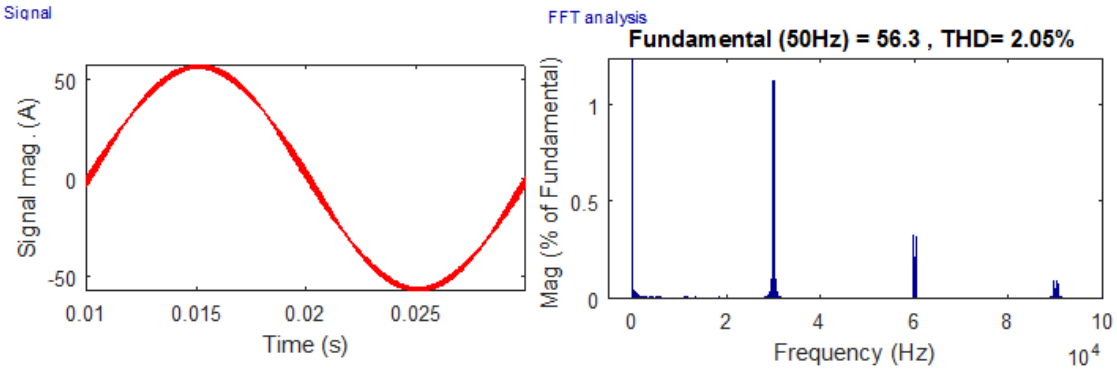


Figure 33. *VSI's phase current waveform and FFT analysis with f_{sw}=30 kHz.*

The obtained phase current waveform is close to a sinusoidal. Only a small ripple can be found. The first harmonic component peak is at 30 kHz with a magnitude of only just over 1% of the fundamental component.

Corresponding simulations were conducted with the NPC inverter model. Figure 34 presents the current and FFT analysis of the NPC inverter simulated with f_{sw} = 1 kHz.

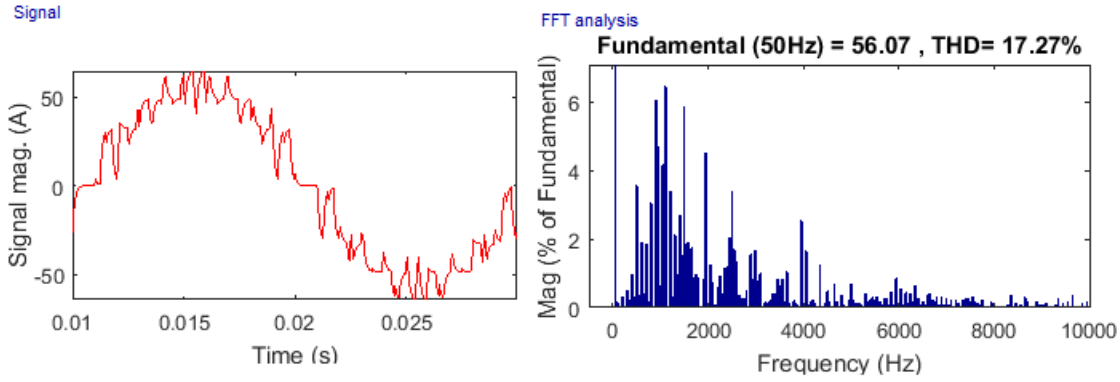


Figure 34. *NPC's phase current waveform and FFT analysis with f_{sw}=1 kHz.*

The NPC inverter's current waveform transients are not that intense compared to the corresponding simulation with the VSI in Figure 31. Majority of the harmonic components are located around frequency of 1 kHz, which is the switching frequency used in this simulation.

NPC inverter's phase currents and FFT analyses with 10 and 30 kHz switching frequencies are presented in the Figure 35 and Figure 36, respectively.

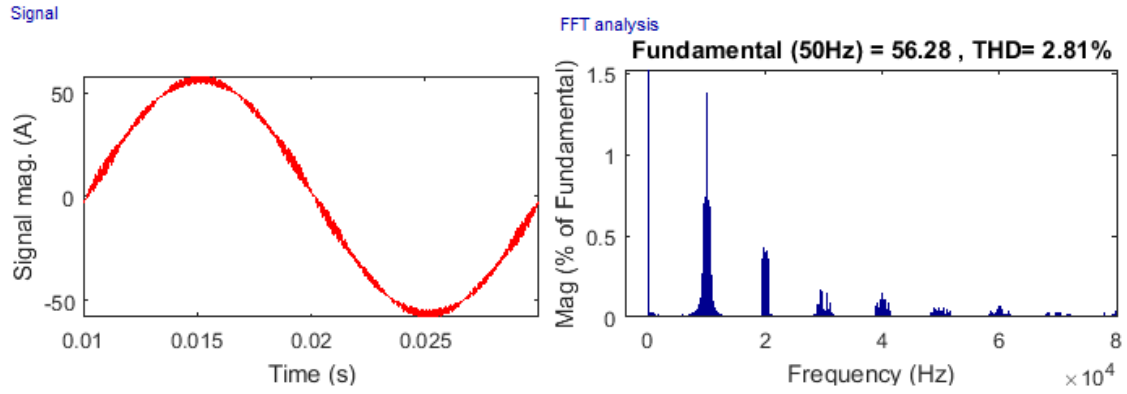


Figure 35. *NPC's phase current waveform and FFT analysis with f_{sw}=10 kHz.*

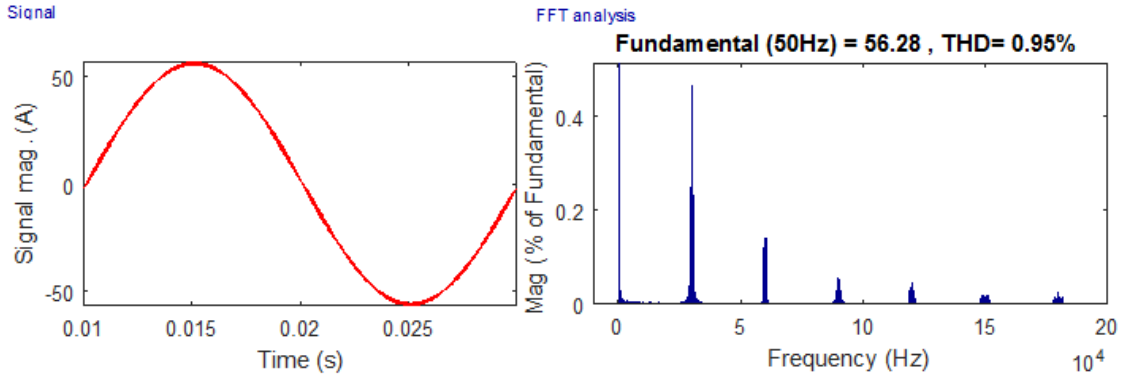


Figure 36. *NPC's phase current waveform and FFT analysis with f_{sw}=30 kHz.*

We can see that the current waveform is really close to sinusoidal in both of these figures. Harmonic components are clearly distributed around multiples of the switching frequencies. The magnitudes of the first harmonics are below 0.5% of the fundamental amplitude with f_{sw} = 30 kHz.

Fundamental phase current amplitudes and THD values simulated with VSI are gathered in the Table 9.

Table 9. *Fundamental phase current amplitudes and THD values of VSI.*

f_{sw} (kHz)	$\hat{I}_u$ (V)	THD_i (%)
1	56.08	34.91
2	56.25	24.57
3	56.28	18.32
5	56.29	11.79
10	56.30	6.09
15	56.30	4.09
20	56.28	3.07
30	56.30	2.05

The same data obtained with NPC inverter simulations is presented in the Table 10.

Table 10. *Fundamental phase current amplitudes and THD values of NPC.*

f_{sw} (kHz)	$\hat{I}_u$ (V)	THD_i (%)
1	56.07	17.27
2	56.23	11.5
3	56.26	8.49
5	56.28	5.45
10	56.28	2.81
15	56.29	1.88
20	56.28	1.42
30	56.28	0.95

It is clear that changing the switching frequency doesn't affect to the amplitude of the fundamental current component. However, increasing the switching frequency reduces the current's THD value. It also moves the peak harmonic components to higher frequency ranges. The phase current's THD value dependence on the switching frequency is presented in the Figure 37.

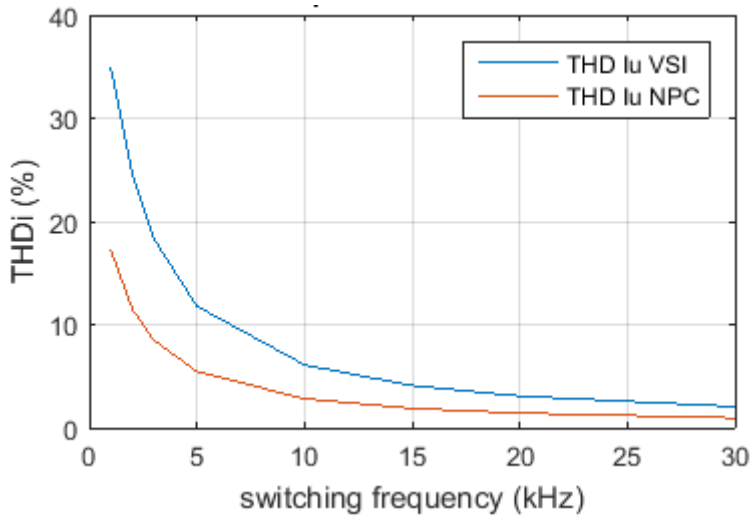


Figure 37. *Phase current's THD dependence on the switching frequency in VSI and NPC inverters.*

It can be seen that the current's THD value in NPC inverter is half of the value in VSI in every switching frequency. The rate of change in the THD value is faster in low switching frequencies.

5.5 Inverters' voltage and THD with different modulation indexes

This section studies the effect of different modulation indexes on inverters' line-to-line voltage. The simulations are conducted with five different modulation indexes: 1, 0.8,

0.6, 0.4 and 0.2. The other parameters used in the simulations are presented in the Table 11. The results of all the simulations are presented in the end of this section.

Table 11. *Parameters for voltage THD comparison simulations with different modulation indexes.*

variable	value
U_{dc} (V)	690·√2
R_{load} (Ω)	10
L_{load} (H)	1
f_{sw} (kHz)	6

Waveforms and FFT analyses of the simulated line-to-line voltages are presented with the modulation indexes of 1, 0.6 and 0.2. The obtained line-to-line voltage and FFT analysis of VSI simulation with modulation index of 1 are presented in the Figure 38.

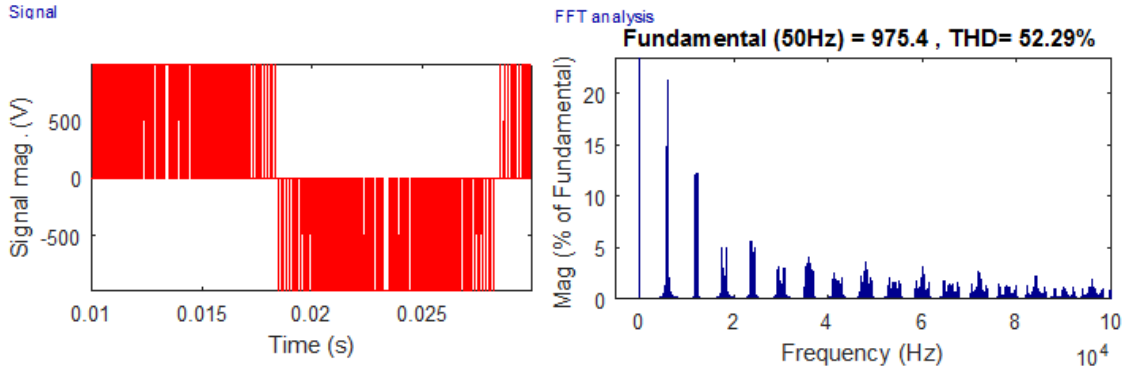


Figure 38. *VSI's line-to-line voltage waveform and FFT analysis with m=1.*

The amplitude of the fundamental component and THD value matches with the previous simulations with m = 1 presented in the Section 5.3. The Figure 39 illustrates the simulation with modulation index of 0.6.

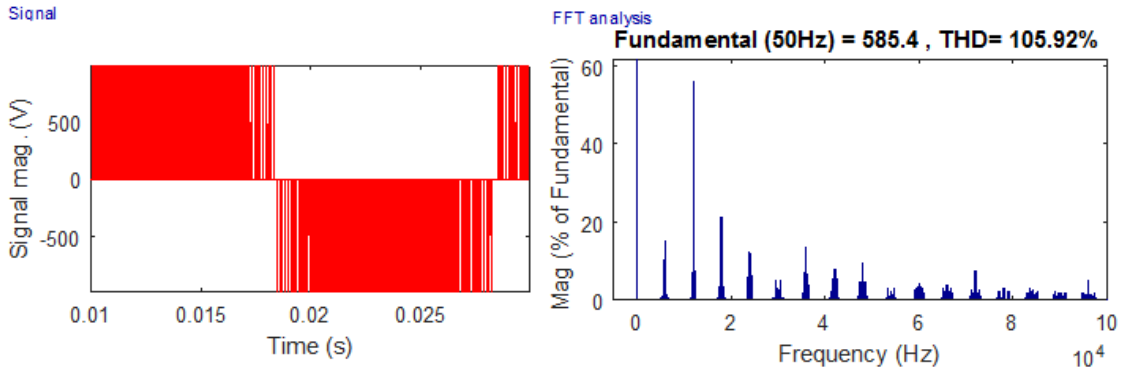


Figure 39. *VSI's line-to-line voltage waveform and THD analysis with m=0.6.*

The amplitude of the voltage's fundamental component decreases directly proportional to the reduction in the modulation index. Also, the THD value is increased substantially. Harmonic peaks are located at the multiples of the switching frequency. The most dominant harmonics are located at the frequency of 12 kHz.

Simulation results of the VSI inverter with modulation index of 0.2 is presented in the Figure 40.

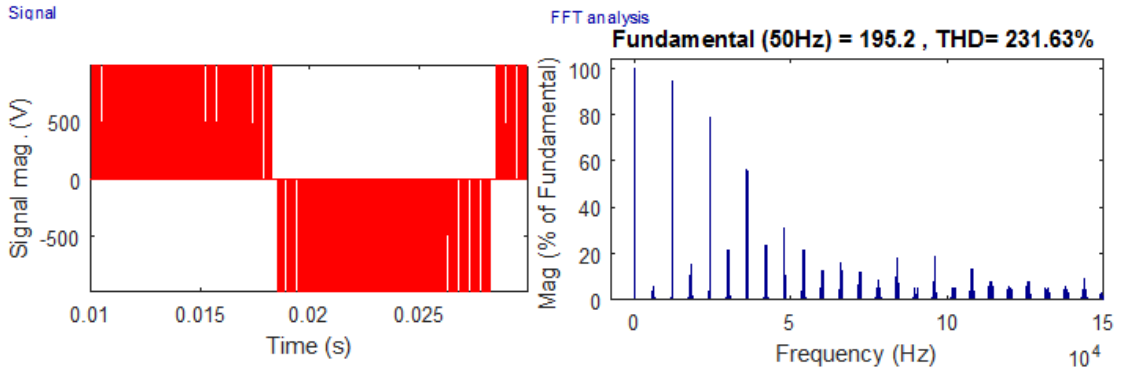


Figure 40. *VSI's line-to-line voltage waveform and THD analysis with m=0.2.*

There are harmonics with over 90% magnitude of the fundamental component as can be seen in the FFT analysis graph. The increase in the voltage THD value is remarkable when using low modulation index. It is obvious from the FFT analysis graph that there are significant harmonic components at relatively high frequencies.

Similar simulations are conducted with the NPC inverter. Line-to-line voltage and FFT analysis of the NPC inverter with modulation index of 1 are presented in the Figure 41.

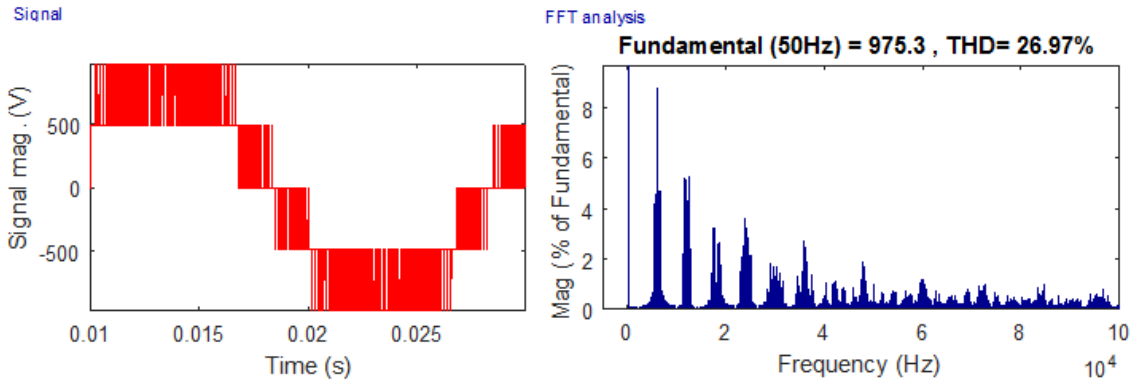


Figure 41. *NPC's line-to-line voltage waveform and THD analysis with m=1.*

The results matches to the ones carried out previously with different switching frequencies and modulation index of 1. Modulation index of 0.6 is used in the simulation presented in Figure 42.

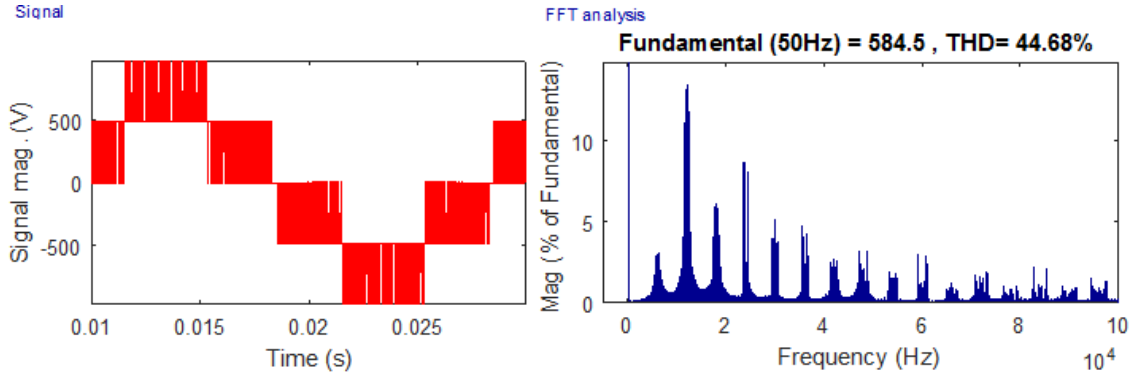


Figure 42. *NPC's line-to-line voltage waveform and THD analysis with m=0.6.*

Again, the amplitude of the fundamental component is reduced directly proportional to decrease in the modulation index. The magnitude of the harmonics at the frequency of 12 kHz are more substantial than the harmonics at the frequency of 6 kHz.

Modulation index of 0.2 is used for the final NPC inverter's voltage simulation. The results are presented in the Figure 43.

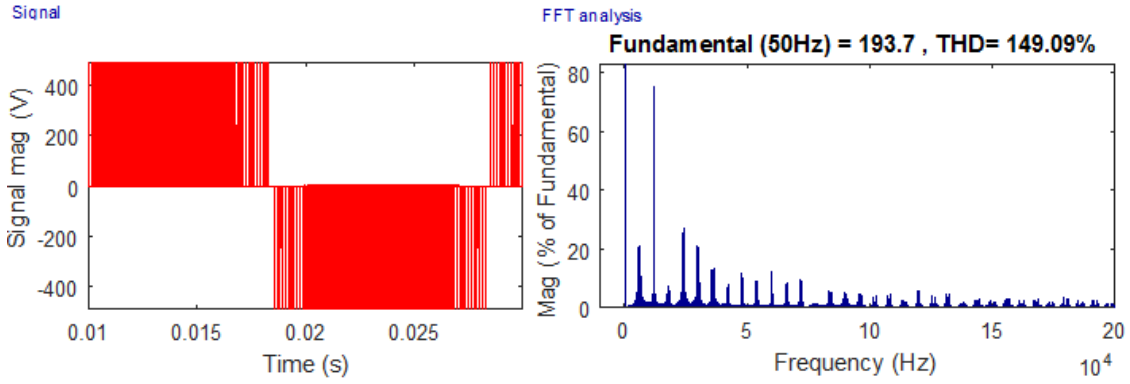


Figure 43. *NPC's line-to-line voltage waveform and THD analysis with m=0.2.*

Now that the modulation index is reduced to 0.2, the inverter modulates using only short vectors. This can be seen from the line-to-line voltage waveform as there are only three voltage levels. Therefore, the shape of the modulated signal is similar to those simulated with the VSI. However, the amplitudes of the voltage pulses are only half of the amplitude seen in the VSI. This is why the voltage's THD value is smaller in the NPC inverter than it is in the VSI inverter with m = 0.2.

All the results simulated with the VSI in this section are presented in the Table 12.

Table 12. *Fundamental line-to-line voltage amplitudes and THD values of VSI.*

m	$\hat{U}_{uv}$ (V)	THD_{uv} (%)
1	975.4	52.29
0.8	780.6	76.91
0.6	585.4	105.92
0.4	390.2	147.77
0.2	195.2	231.63

Fundamental line-to-line voltage amplitudes and THD values obtained from the NPC inverter simulations are given in the Table 13.

Table 13. *Fundamental line-to-line voltage amplitudes and THD values of NPC.*

m	$\hat{U}_{uv}$ (V)	THD_{uv} (%)
1	975.3	26.97
0.8	780.0	38.46
0.6	584.5	44.68
0.4	389.1	77.24
0.2	193.7	149.09

Figure 44 indicates the relationship between different modulation indexes and voltage's THD values based on the data presented in the tables above.

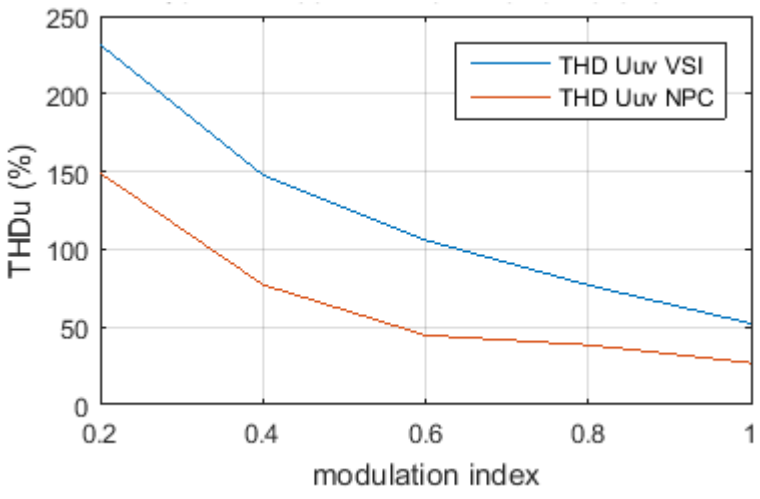


Figure 44. *The effect of different modulation indexes on line-to-line voltage's THD values in VSI and NPC inverters.*

It can be seen in the figure that with modulation indexes over 0.8, the line-to-line voltage's THD value in NPC inverter is half of the THD value in VSI. The relative difference in the THD values between the VSI and NPC inverters reduce with modulation indexes

smaller than 0.8. The absolute difference in the THD value increases when the modulation index decreases. This occurs because the NPC inverter isn't able to utilize all the DC bus voltage levels effectively with small modulation indexes.

5.6 Inverters' phase current and THD with different modulation indexes

This section studies the effect of different modulation indexes on inverters' phase currents. The simulations are conducted with m = 1, 0.8, 0.6, 0.4 and 0.2. The other parameters used in the simulations in this section are given in the Table 14.

Table 14. *Parameters for phase current THD comparison simulations with different modulation indexes*

variable	value
U_{dc} (V)	690·√2
R_{load} (Ω)	10
L_{load} (H)	1
f_{sw} (kHz)	6

The presentation of the results is similar to the previous sections: Current waveforms and FFT analyses with modulation indexes of 1, 0.6 and 0.2 are presented first for VSI followed by the results for NPC inverter. Figure 45 presents the simulation results of VSI with modulation index of 1.

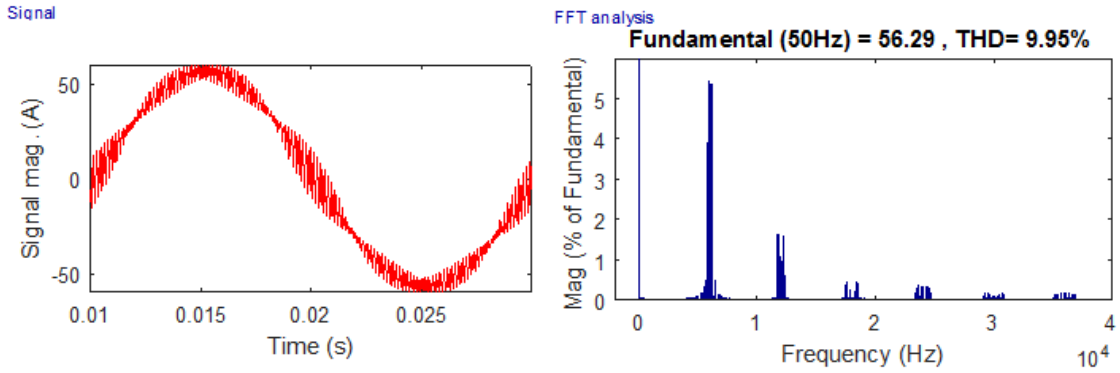


Figure 45. *VSI's phase current waveform and THD analysis with m=1.*

The resulting THD value matches to the results provided in Section 5.4. Current waveform and FFT analysis of the VSI with modulation index of 0.6 are presented in the Figure 46.

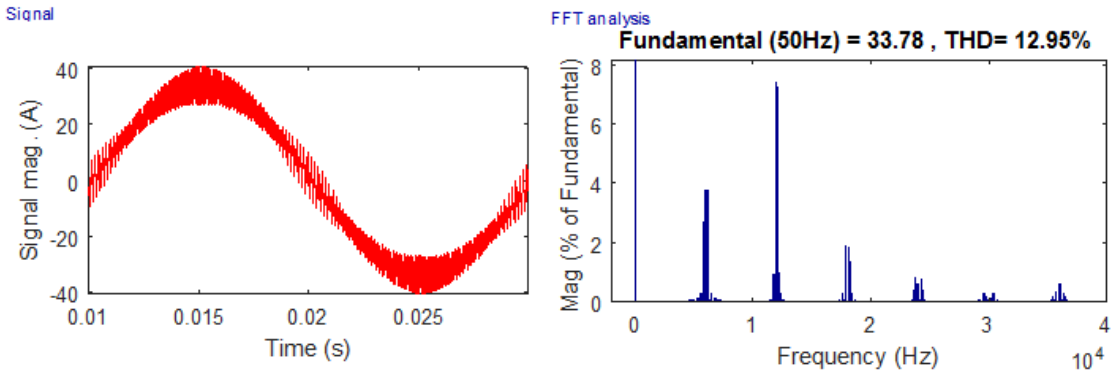


Figure 46. *VSI's phase current waveform and THD analysis with m=0.6.*

The amplitude of the phase current's fundamental component is reduced directly proportional to the reduction in the modulation index similarly as the amplitude of the line-to-line voltage's fundamental component was reduced. The most significant current harmonic component can be found at the frequency of 12 kHz.

The simulated current waveform and FFT analysis with m = 0.2 for VSI is presented in the Figure 47.

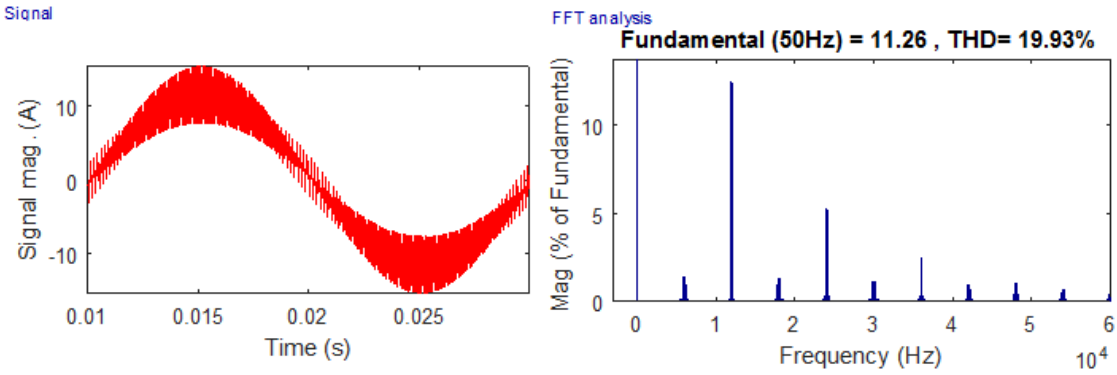


Figure 47. *VSI's phase current waveform and THD analysis with m=0.2.*

It can be seen that there are significant harmonic components at high frequency areas like in the corresponding voltage simulations with small modulation indexes in Section 5.5. Also, the magnitude of the first harmonic components are increased compared to a larger modulation index simulations presented in Figure 45 and Figure 46.

Simulation results obtained with the NPC inverter are presented next. Figure 48 presents the current waveform and FFT analysis of the NPC inverter with modulation index of 1.

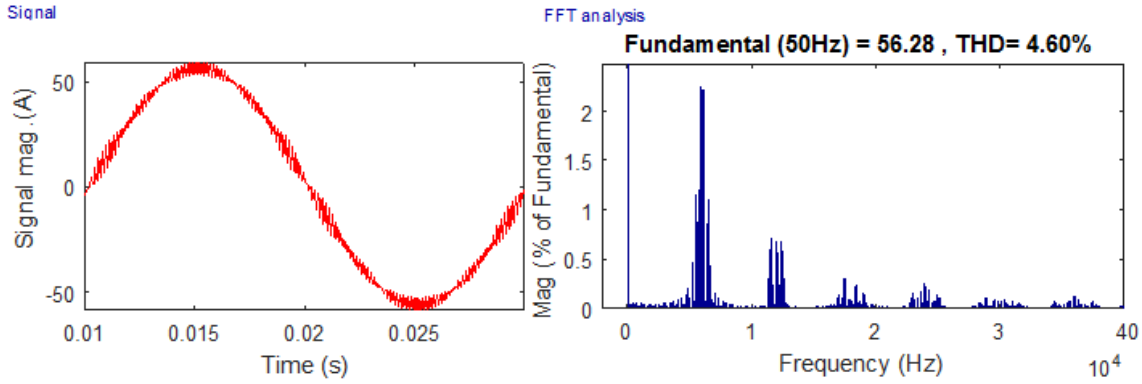


Figure 48. *NPC's phase current waveform and THD analysis with m=1.*

The resulting THD value corresponds the NPC inverter simulations with modulation index of 1 and the curve presented in Figure 37. NCP inverters phase current waveform and FFT analysis with modulation index of 0.6 are presented in Figure 49.

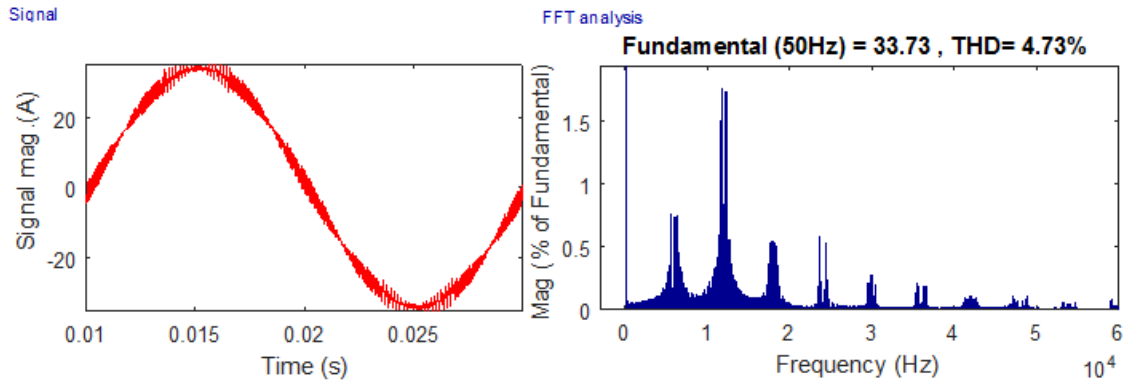


Figure 49. *NPC's phase current waveform and THD analysis with m=0.6.*

The current's THD values are almost the same with modulation indexes of 1 and 0.6. The amplitude of the phase current's fundamental component is decreased directly proportional to the modulation index.

Finally, the simulated current waveform and FFT analysis with modulation index of 0.2 are given in the Figure 50.

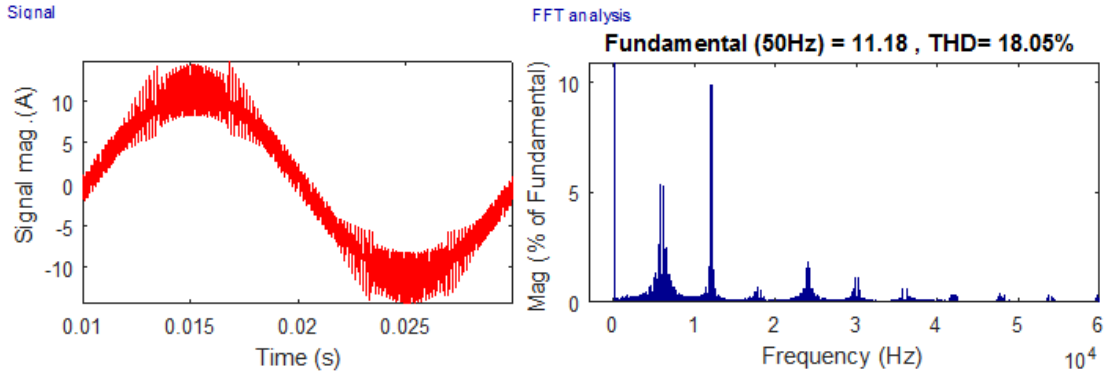


Figure 50. *NPC's phase current waveform and THD analysis with m=0.2.*

Current's amplitude of the fundamental component is decreased proportionally to the reduction in modulation index. The significance of the first harmonic components are increased as the magnitudes of them are grown.

All the VSI simulation results obtained with different modulation indexes are presented in the Table 15.

Table 15. *Fundamental phase current amplitudes and THD values of VSI.*

f_{sw} (kHz)	$\hat{I}_u$ (V)	THD_i (%)
1	56.29	9.95
0.8	45.04	10.65
0.6	33.78	12.95
0.4	22.52	16.20
0.2	11.26	19.93

Fundamental phase current amplitudes and THD values obtained from the NPC inverter simulations are presented similarly in the Table 16.

Table 16. *Fundamental phase current amplitudes and THD values of NPC.*

f_{sw} (kHz)	$\hat{I}_u$ (V)	THD_i (%)
1	56.28	4.6
0.8	45.01	4.53
0.6	33.73	4.73
0.4	22.46	8.85
0.2	11.18	18.05

The data of the previous tables are summarized in the Figure 51.

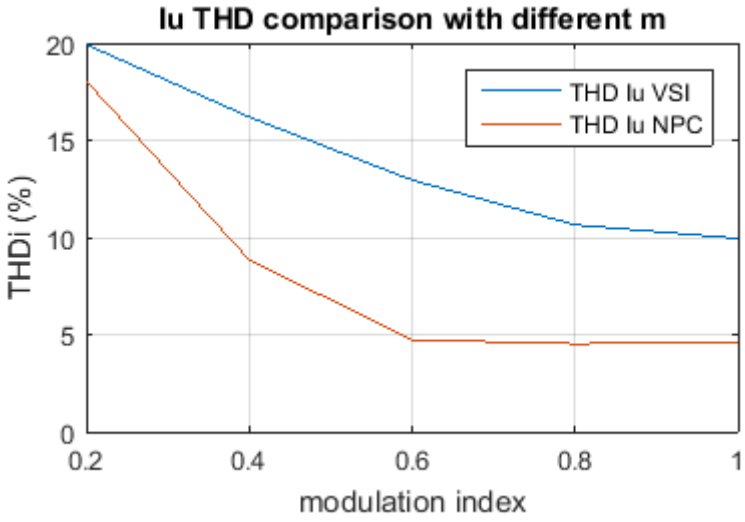


Figure 51. *Phase current's THD relationship to different modulation indexes between VSI and NPC inverters.*

It is showed that the modulation index doesn't affect to the NPC inverter's current THD value until the *m* is reduced under 0.6. The NPC inverter cannot utilize the available voltage levels with small modulation indexes. Therefore, the difference in the current's THD value decrease when the modulation index is reduced. The biggest percentage difference in current's THD value between NPC and VSI is with the modulation index of 0.6.

6. CONCLUSIONS

The utilization of power electronics is increasing. Inverters supplying electricity to the power grids creates non-sinusoidal waveforms. Therefore, the distortion in the grids may increase. This distortion can be reduced by using a high-cost *LCL* filter. Space vector PWM is a method used to create control pulses for IGBTs in today's inverters. It has a good output harmonics performance, it is easy to implement in today's microcontroller based control logics, and the DC voltage utilization is better than in a traditional sine-PWM method. THD value of the inverter can also be decreased by adding voltage levels to inverters' DC bus. Therefore, a space vector modulated NPC inverter's output performance is compared to VSI inverter in this thesis.

The aim of this thesis was to provide a detailed implementation of the space vector PWM schemes for 2L and 3L inverters. Simulink® models of VSI and NPC inverters were modeled. The objective of these models were to simulate and compare the output line-to-line voltage's and phase current's THD performance with different switching frequencies and modulation indexes.

Chapter 1 introduced to the subject and gave a motivation to the study of the inverters. Chapter 2 provided an introduction of the VSI and NPC inverter topologies studied in this thesis. The definition of harmonics and THD were also introduced. Chapter 3 presented a general space vector modulation methods for VSI and NPC inverters. Different phases of the modulation method were discussed in details, such as the selection of the voltage vectors in a modulation period. More advanced modulation methods were introduced in the Chapter 4. Simulink® models created for the simulation purposes were presented in the Chapter 5. The simulation results were presented followed by graphs of the dependence of the switching frequency and modulation indexes on voltage's and current's THD values. Chapter 6 gave a conclusion to the thesis.

The results showed that the switching frequency affected to the phase current's THD value in VSI and NPC inverters. Increasing the switching frequency reduced the current's THD value. It was shown that the switching frequency didn't affect to the absolute line-to-line voltage's THD value. However, increasing the switching frequency relocated the voltages' and currents' harmonic components to higher frequencies. The voltage's and current's THD values in NPC inverter were half of the THD values in VSI if modulation index of 1 was used. The effect of different modulation indexes was also studied. It was observed that the modulation index affected to the line-to-line voltage's and phase current's values. Decrease in the modulation index increased the THD values in both of the studied variables. It was seen that the NPC inverter's output performance stayed in a better level compared to VSI's if the modulation index was kept roughly over 0.6 Modulation

indexes under 0.6 limited the usage of all the DC bus's voltage levels and the output performance gap between VSI and NPC inverters decreased.

Future studies related to this subject could improve the simulation models and take all the neglected practical modulator requirements into account. The models used in the simulations of this thesis were highly simplified, and adding functions such as blanking time, IGBT non-idealities, minimum pulse control and operation in overmodulation region could be added to gain more detailed simulation results. Studies could also focus on the filter design and investigate how the frequency ranges of the harmonic components affects to the filter design. The boundary conditions using the NPC inverter versus the VSI could also be studied in a financial point of view.

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APPENDIX A: VSI SPACE VECTOR PWM MODULATOR CODE

```
function [u1, u2, v1, v2, w1, w2] = fcn(Uref, Vdc, fsw, time)
%#codegen

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% define and initialize persistent variables %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
persistent sv_act1 sv_act2 t1 t2 ua1 ua2 va1 va2 wa1 wa2;
if isempty(sv_act1, sv_act2, t1, t2, ua1, ua2, va1, va2, wa1, wa2)
    sv_act1 = [0 0 0 0 0 0];
    sv_act2 = [0 0 0 0 0 0];
    t1=0;
    t2=0;
    ua1=0;
    ua2=0;
    va1=0;
    va2=0;
    wa1=0;
    wa2=0;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% define switching vectors for 2L VSI %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
sv1=[1 0 0 0 1 1]; % pnn 2/3*Vdc;
sv2=[1 1 0 0 0 1]; % ppn 2/3*Vdc*exp(i*pi/3);
sv3=[0 1 0 1 0 1]; % npn 2/3*Vdc*exp(i*2*pi/3);
sv4=[0 1 1 1 0 0]; % npp 2/3*Vdc*exp(i*pi);
sv5=[0 0 1 1 1 0]; % nnp 2/3*Vdc*exp(i*4*pi/3);
sv6=[1 0 1 0 1 0]; % pnp 2/3*Vdc*exp(i*5*pi/3);
sv7=[0 0 0 1 1 1]; % nnn
sv8=[1 1 1 0 0 0]; % ppp

%%%%%%%%%%%%%%%%%%%%%%%
% switching frequency %
%%%%%%%%%%%%%%%%%%%%%%%
Ts=1/fsw;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% On times are calculated and active switching vectors are %
% chosen here based on the angle of the reference vector   %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Uref_amp=abs(Uref);
Uref_ang=angle(Uref);   %[-pi...pi]
% Uref is in the 1st sector
if Uref_ang>=0 && Uref_ang<(pi/3)
    sv_act1=sv1;
    sv_act2=sv2;
    t1=sqrt(3)*Ts*Uref_amp/Vdc*sin(pi/3-Uref_ang);
    t2=sqrt(3)*Ts*Uref_amp/Vdc*sin(Uref_ang-0);
end
% Uref is in the 2nd sector
if Uref_ang>=(pi/3) && Uref_ang<(2*pi/3)
```

```
    sv_act1=sv3;
    sv_act2=sv2;
    t1=sqrt(3)*Ts*Uref_amp/Vdc*sin(Uref_ang-pi/3);
    t2=sqrt(3)*Ts*Uref_amp/Vdc*sin(2*pi/3-Uref_ang);
end
% Uref is in the 3nd sector
if Uref_ang>=(2*pi/3) && Uref_ang<(pi)
    sv_act1=sv3;
    sv_act2=sv4;
    t1=sqrt(3)*Ts*Uref_amp/Vdc*sin(pi-Uref_ang);
    t2=sqrt(3)*Ts*Uref_amp/Vdc*sin(Uref_ang-2*pi/3);
end
% Uref is in the 4nd sector
if Uref_ang>=(-pi) && Uref_ang<(-2*pi/3)
    sv_act1=sv5;
    sv_act2=sv4;
    t1=sqrt(3)*Ts*Uref_amp/Vdc*sin(Uref_ang-(-pi));
    t2=sqrt(3)*Ts*Uref_amp/Vdc*sin(-2*pi/3-Uref_ang);
end
% Uref is in the 5nd sector
if Uref_ang>=(-2*pi/3) && Uref_ang<(-pi/3)
    sv_act1=sv5;
    sv_act2=sv6;
    t1=sqrt(3)*Ts*Uref_amp/Vdc*sin(-pi/3-Uref_ang);
    t2=sqrt(3)*Ts*Uref_amp/Vdc*sin(Uref_ang-(-2*pi/3));
end
% Uref is in the 6nd sector
if Uref_ang>=(-pi/3) && Uref_ang<(0)
    sv_act1=sv1;
    sv_act2=sv6;
    t1=sqrt(3)*Ts*Uref_amp/Vdc*sin(Uref_ang-(-pi/3));
    t2=sqrt(3)*Ts*Uref_amp/Vdc*sin(0-Uref_ang);
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% switching time for zero vector %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
t0=Ts-t1-t2;

%%%%%%%%%%%%%%%%%%%%%%%%%%
% Gate signal generation %
%%%%%%%%%%%%%%%%%%%%%%%%%%
if time >= 0 && time < (t0/4)
    ua1=sv7(1);
    ua2=sv7(4);
    va1=sv7(2);
    va2=sv7(5);
    wa1=sv7(3);
    wa2=sv7(6);
end
if time >= t0/4 && time < (t0/4+t1/2)
    ua1=sv_act1(1);
    ua2=sv_act1(4);
    va1=sv_act1(2);
    va2=sv_act1(5);
    wa1=sv_act1(3);
    wa2=sv_act1(6);
end
if time >= (t0/4+t1/2) && time < (Ts/2-t0/4)
```

```
        ua1=sv_act2(1);
114     ua2=sv_act2(4);
        va1=sv_act2(2);
116     va2=sv_act2(5);
        wa1=sv_act2(3);
118     wa2=sv_act2(6);
    end
120 if time >= (Ts/2-t0/4) && time < (Ts/2)
        ua1=sv8(1);
122     ua2=sv8(4);
        va1=sv8(2);
124     va2=sv8(5);
        wa1=sv8(3);
126     wa2=sv8(6);
    end
128 if time >= (Ts/2) && time < (Ts/2+t0/4)
        ua1=sv8(1);
130     ua2=sv8(4);
        va1=sv8(2);
132     va2=sv8(5);
        wa1=sv8(3);
134     wa2=sv8(6);
    end
136 if time >= (Ts/2+t0/4) && time < (Ts-t1/2-t0/4)
        ua1=sv_act2(1);
138     ua2=sv_act2(4);
        va1=sv_act2(2);
140     va2=sv_act2(5);
        wa1=sv_act2(3);
142     wa2=sv_act2(6);
    end
144 if time >= (Ts-t1/2-t0/4) && time < (Ts-t0/4)
        ua1=sv_act1(1);
146     ua2=sv_act1(4);
        va1=sv_act1(2);
148     va2=sv_act1(5);
        wa1=sv_act1(3);
150     wa2=sv_act1(6);
    end
152 if time >= (Ts-t0/4) && time < Ts
        ua1=sv7(1);
154     ua2=sv7(4);
        va1=sv7(2);
156     va2=sv7(5);
        wa1=sv7(3);
158     wa2=sv7(6);
    end
160
    u1=ua1;
162 u2=ua2;
    v1=va1;
164 v2=va2;
    w1=wa1;
168 w2=wa2;
```

APPENDIX B: NPC SPACE VECTOR PWM MODULATOR CODE

```
function [u1, u2, u3, u4, v1, v2, v3, v4, w1, w2, w3, w4] = fcn(Uref1,
Vdc, fsw, time)
%#codegen

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% define and initialize persistent variables %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
persistent sv1 sv2 sv3 sv4 origin Uref2 Uref2_ang subsector N t0 t1 t2
ua1 ua2 ua3 ua4 va1 va2 va3 va4 wa1 wa2 wa3 wa4;

if isempty(sv1, sv2, sv3, sv4)
    sv1 = [0 0 0 0 0 0 0 0 0 0 0 0];
    sv2 = [0 0 0 0 0 0 0 0 0 0 0 0];
    sv3 = [0 0 0 0 0 0 0 0 0 0 0 0];
    sv4 = [0 0 0 0 0 0 0 0 0 0 0 0];
end

if isempty(origin, Uref2, Uref2_ang, subsector, N)
    origin = 0+0i;
    Uref2 = 0+0*1i;
    Uref2_ang=0;
    subsector=0;
    N=0;
end

if isempty(t0, t1, t2, ua1, ua2, ua3, ua4, va1, va2, va3, va4, wa1, wa2,
wa3, wa4)
    t0=0;
    t1=0;
    t2=0;
    ua1=0;
    ua2=0;
    ua3=0;
    ua4=0;
    va1=0;
    va2=0;
    va3=0;
    va4=0;
    wa1=0;
    wa2=0;
    wa3=0;
    wa4=0;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% define short switching vectors for sector defining purposes %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
sv_onn=Vdc*(1/3+0*1i);
sv_oon=Vdc*(1/6+sqrt(3)/6*1i);
sv_opo=Vdc*(-1/6+sqrt(3)/6*1i);
sv_noo=Vdc*(-1/3+0*1i);
sv_nno=Vdc*(-1/6-sqrt(3)/6*1i);
sv_ono=Vdc*(1/6-sqrt(3)/6*1i);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% define switching vectors for 3L NPC %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
onn = [0 1 1 0 0 0 1 1 0 0 1 1];
poo = [1 1 0 0 0 1 1 0 0 1 1 0];
oon = [0 1 1 0 0 1 1 0 0 0 1 1];
ppo = [1 1 0 0 1 1 0 0 0 1 1 0];
opo = [0 1 1 0 1 1 0 0 0 1 1 0];
non = [0 0 1 1 0 1 1 0 0 0 1 1];
opp = [0 1 1 0 1 1 0 0 1 1 0 0];
noo = [0 0 1 1 0 1 1 0 0 1 1 0];
nno = [0 0 1 1 0 0 1 1 0 1 1 0];
oop = [0 1 1 0 0 1 1 0 1 1 0 0];
ono = [0 1 1 0 0 0 1 1 0 1 1 0];
pop = [1 1 0 0 0 1 1 0 1 1 0 0];
pon = [1 1 0 0 0 1 1 0 0 0 1 1];
opn = [0 1 1 0 1 1 0 0 0 0 1 1];
npo = [0 0 1 1 1 1 0 0 0 1 1 0];
nop = [0 0 1 1 0 1 1 0 1 1 0 0];
onp = [0 1 1 0 0 0 1 1 1 1 0 0];
pno = [1 1 0 0 0 0 1 1 0 1 1 0];
pnn = [1 1 0 0 0 0 1 1 0 0 1 1];
ppn = [1 1 0 0 1 1 0 0 0 0 1 1];
npn = [0 0 1 1 1 1 0 0 0 0 1 1];
npp = [0 0 1 1 1 1 0 0 1 1 0 0];
nnp = [0 0 1 1 0 0 1 1 1 1 0 0];
pnp = [1 1 0 0 0 0 1 1 1 1 0 0];
ppp = [1 1 0 0 1 1 0 0 1 1 0 0];
ooo = [0 1 1 0 0 1 1 0 0 1 1 0];
nnn = [0 0 1 1 0 0 1 1 0 0 1 1];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Reference vector 2 angle is calculated based %
% on reference vector 1 angle                  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Uref1_ang=angle(Uref1);     % angle range from -pi...pi
% Sectors S11,S13,S15,S62,S64,S66
if Uref1_ang >= -pi/6 && Uref1_ang < pi/6
    origin=sv_onn;
    Uref2=Uref1-origin;
    Uref2_ang=angle(Uref2);
end
% Sectors S12,S14,S16,S21,S23,S25
if Uref1_ang >= pi/6 && Uref1_ang < pi/2
    origin=sv_oon;
    Uref2=Uref1-origin;
    Uref2_ang=angle(Uref2);
end
% Sectors S22,S24,S26,S31,S33,S35
if Uref1_ang >= pi/2 && Uref1_ang < 5*pi/6
    origin=sv_opo;
    Uref2=Uref1-origin;
    Uref2_ang=angle(Uref2);
end
% Sectors S32,S34,S36
if Uref1_ang >= 5*pi/6 && Uref1_ang < pi
    origin=sv_noo;
    Uref2=Uref1-origin;
```

```
    Uref2_ang=angle(Uref2);
end
% Sectors S41,S43,S45
if Uref1_ang >=-pi && Uref1_ang < -5*pi/6
    origin=sv_noo;
    Uref2=Uref1-origin;
    Uref2_ang=angle(Uref2);
end
% Sectors S42,S44,S46,S51,S53,S55
if Uref1_ang >=-5*pi/6 && Uref1_ang < -pi/2
    origin=sv_nno;
    Uref2=Uref1-origin;
    Uref2_ang=angle(Uref2);
end
% Sectors S52,S54,S56,S61,S63,S65
if Uref1_ang >=-pi/2 && Uref1_ang < -pi/6
    origin=sv_ono;
    Uref2=Uref1-origin;
    Uref2_ang=angle(Uref2);
end
Uref2_ang2=Uref2_ang;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Main- and subsector, in which the reference %
% vector 1 is located, is solved here.        %
% Active switching vectors are also defined.  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%
% Subsectors in sector 1 %
%%%%%%%%%%%%%%%%%%%%%%%%%%
% Sector S11
if  Uref1_ang  >=  0  &&  Uref1_ang  <  pi/6  &&  Uref2_ang2  >=2*pi/3  &&
Uref2_ang2 < pi
    N=1;
    subsector=1;
    sv1=onn;
    sv2=oon;
    sv3=ooo;
    sv4=poo;
end
% Sector S12
if Uref1_ang >=(pi/6) && Uref1_ang < (pi/3) && Uref2_ang2 >= -2*pi/3 &&
Uref2_ang2 < -pi/3
    N=1;
    subsector=2;
    sv1=oon;
    sv2=ooo;
    sv3=poo;
    sv4=ppo;
end
% Sector S13
if Uref1_ang >= 0 && Uref1_ang < pi/6 && Uref2_ang2 >= pi/3 && Uref2_ang2
< 2*pi/3
    N=1;
    subsector=3;
    sv1=onn;
    sv2=oon;
    sv3=pon;
```

```
    sv4=poo;
end
% Sector S14
if Uref1_ang >=(pi/6) && Uref1_ang < (pi/3) && Uref2_ang2 >= -pi/3 &&
Uref2_ang2 < 0
    N=1;
    subsector=4;
    sv1=oon;
    sv2=pon;
    sv3=poo;
    sv4=ppo;
end
% Sector S15
if Uref1_ang >= 0 && Uref1_ang < pi/6 && Uref2_ang2 >=0 && Uref2_ang2 <
pi/3
    N=1;
    subsector=5;
    sv1=onn;
    sv2=pnn;
    sv3=pon;
    sv4=poo;
end
% Sector S16
if Uref1_ang >=(pi/6) && Uref1_ang < (pi/3) && Uref2_ang2 >=0 &&
Uref2_ang2 < pi/3
    N=1;
    subsector=6;
    sv1=oon;
    sv2=pon;
    sv3=ppn;
    sv4=ppo;
end

%%%%%%%%%%%%%%%%%%%%%%%%%
% Subsectors in sector 2 %
%%%%%%%%%%%%%%%%%%%%%%%%%
% Sector S21
if Uref1_ang >=(pi/3) && Uref1_ang < (pi/2) && Uref2_ang2 >= -pi &&
Uref2_ang2 < -2*pi/3
    N=2;
    subsector=1;
    sv1=oon;
    sv2=ooo;
    sv3=opo;
    sv4=ppo;
end
% Sector S22
if Uref1_ang >=(pi/2) && Uref1_ang < (2*pi/3) && Uref2_ang2 >= -pi/3 &&
Uref2_ang2 < 0
    N=2;
    subsector=2;
    sv1=non;
    sv2=oon;
    sv3=ooo;
    sv4=opo;
end
% Sector S23
if Uref1_ang >=(pi/3) && Uref1_ang < (pi/2) && Uref2_ang2 >=2*pi/3 &&
Uref2_ang2 < pi
```

```
        N=2;
232     subsector=3;
        sv1=oon;
234     sv2=opn;
        sv3=opo;
236     sv4=ppo;
    end
238 % Sector S24
    if Uref1_ang >=(pi/2) && Uref1_ang < (2*pi/3) && Uref2_ang2 >=0 &&
240 Uref2_ang2 < pi/3
        N=2;
242     subsector=4;
        sv1=non;
244     sv2=oon;
        sv3=opn;
246     sv4=opo;
    end
248 % Sector S25
    if Uref1_ang >=(pi/3) && Uref1_ang < (pi/2) &&  Uref2_ang2 >= pi/3 &&
250 Uref2_ang2 < 2*pi/3
        N=2;
252     subsector=5;
        sv1=oon;
254     sv2=opn;
        sv3=ppn;
256     sv4=ppo;
    end
258 % Sector S26
    if Uref1_ang >=(pi/2) && Uref1_ang < (2*pi/3) && Uref2_ang2 >= pi/3 &&
260 Uref2_ang2 < 2*pi/3
        N=2;
262     subsector=6;
        sv1=non;
264     sv2=npn;
        sv3=opn;
266     sv4=opo;
    end
268
    %%%%%%%%%%%%%%%%%%%%%%%%%
270 % Subsectors in sector 3 %
    %%%%%%%%%%%%%%%%%%%%%%%%%
272 % Sector S31
    if Uref1_ang >=(2*pi/3) && Uref1_ang < (5*pi/6) && Uref2_ang2 >= -2*pi/3
274 && Uref2_ang2 < -pi/3
        N=3;
276     subsector=1;
        sv1=non;
278     sv2=noo;
        sv3=ooo;
280     sv4=opo;
    end
282 % Sector S32
    if Uref1_ang >=(5*pi/6) && Uref1_ang < pi && Uref2_ang2 >=0 && Uref2_ang2
284 < pi/3
        N=3;
286     subsector=2;
        sv1=noo;
288     sv2=ooo;
        sv3=opo;
```

```
290     sv4=opp;
    end
292 % Sector S33
    if Uref1_ang >=(2*pi/3) && Uref1_ang < (5*pi/6) && Uref2_ang2 >= -pi &&
294 Uref2_ang2 < -2*pi/3
        N=3;
296     subsector=3;
        sv1=non;
298     sv2=noo;
        sv3=npo;
300     sv4=opo;
    end
302 % Sector S34
    if Uref1_ang >=(5*pi/6) && Uref1_ang < pi && Uref2_ang2 >= pi/3 &&
304 Uref2_ang2 < 2*pi/3
        N=3;
306     subsector=4;
        sv1=noo;
308     sv2=npo;
        sv3=opo;
310     sv4=opp;
    end
312 % Sector S35
    if Uref1_ang >=(2*pi/3) && Uref1_ang < (5*pi/6) && Uref2_ang2 >=2*pi/3
314 && Uref2_ang2 < pi
        N=3;
316     subsector=5;
        sv1=non;
318     sv2=npn;
        sv3=npo;
320     sv4=opo;
    end
322 % Sector S36
    if Uref1_ang >=(5*pi/6) && Uref1_ang < pi && Uref2_ang2 >=2*pi/3 &&
324 Uref2_ang2 < pi
        N=3;
326     subsector=6;
        sv1=noo;
328     sv2=npo;
        sv3=npp;
330     sv4=opp;
    end
332
    %%%%%%%%%%%%%%%%%%%%%%%%%%
334 % Subsectors in sector 4 %
    %%%%%%%%%%%%%%%%%%%%%%%%%%
336 % Sector S41
    if Uref1_ang >=-pi && Uref1_ang < -5*pi/6 && Uref2_ang2 >= -pi/3 &&
338 Uref2_ang2 < 0
        N=4;
340     subsector=1;
        sv1=noo;
342     sv2=ooo;
        sv3=oop;
344     sv4=opp;
    end
346 % Sector S42
    if Uref1_ang >=-5*pi/6 && Uref1_ang < -2*pi/3 && Uref2_ang2 >= pi/3 &&
348 Uref2_ang2 < 2*pi/3
```

```
        N=4;
350     subsector=2;
        sv1=nno;
352     sv2=noo;
        sv3=ooo;
354     sv4=oop;
    end
356 % Sector S43
    if Uref1_ang >=-pi && Uref1_ang < -5*pi/6 && Uref2_ang2 >= -2*pi/3 &&
358 Uref2_ang2 < -pi/3
        N=4;
360     subsector=3;
        sv1=noo;
362     sv2=nop;
        sv3=oop;
364     sv4=opp;
    end
366 % Sector S44
    if Uref1_ang >=-5*pi/6 && Uref1_ang < -2*pi/3 && Uref2_ang2 >=2*pi/3 &&
368 Uref2_ang2 < pi
        N=4;
370     subsector=4;
        sv1=nno;
372     sv2=noo;
        sv3=nop;
374     sv4=oop;
    end
376 % Sector S45
    if Uref1_ang >=-pi && Uref1_ang < -5*pi/6 && Uref2_ang2 >= -pi &&
378 Uref2_ang2 < -2*pi/3
        N=4;
380     subsector=5;
        sv1=noo;
382     sv2=nop;
        sv3=npp;
384     sv4=opp;
    end
386 % Sector S46
    if Uref1_ang >=-5*pi/6 && Uref1_ang < -2*pi/3 && Uref2_ang2 >= -pi &&
388 Uref2_ang2 < -2*pi/3
        N=4;
390     subsector=6;
        sv1=nno;
392     sv2=nnp;
        sv3=nop;
394     sv4=oop;
    end
396
    %%%%%%%%%%%%%%%%%%%%%%%%%%
398 % Subsectors in sector 5 %
    %%%%%%%%%%%%%%%%%%%%%%%%%%
400 % Sector S51
    if Uref1_ang >=-2*pi/3 && Uref1_ang < -pi/2 && Uref2_ang2 >=0 &&
402 Uref2_ang2 < pi/3
        N=5;
404     subsector=1;
        sv1=nno;
406     sv2=ono;
        sv3=ooo;
```

```
    sv4=oop;
end
% Sector S52
if Uref1_ang >= -pi/2 && Uref1_ang < -pi/3 && Uref2_ang2 >=2*pi/3 &&
Uref2_ang2 < pi
    N=5;
    subsector=2;
    sv1=ono;
    sv2=ooo;
    sv3=oop;
    sv4=pop;
end
% Sector S53
if Uref1_ang >=-2*pi/3 && Uref1_ang < -pi/2 && Uref2_ang2 >= -pi/3 &&
Uref2_ang2 < 0
    N=5;
    subsector=3;
    sv1=nno;
    sv2=ono;
    sv3=onp;
    sv4=oop;
end
% Sector S54
if Uref1_ang >= -pi/2 && Uref1_ang < -pi/3 && Uref2_ang2 >= -pi &&
Uref2_ang2 < -2*pi/3
    N=5;
    subsector=4;
    sv1=ono;
    sv2=onp;
    sv3=oop;
    sv4=pop;
end
% Sector S55
if Uref1_ang >=-2*pi/3 && Uref1_ang < -pi/2 && Uref2_ang2 >= -2*pi/3 &&
Uref2_ang2 < -pi/3
    N=5;
    subsector=5;
    sv1=nno;
    sv2=nnp;
    sv3=onp;
    sv4=oop;
end
% Sector S56
if Uref1_ang >= -pi/2 && Uref1_ang < -pi/3 && Uref2_ang2 >= -2*pi/3 &&
Uref2_ang2 < -pi/3
    N=5;
    subsector=6;
    sv1=ono;
    sv2=onp;
    sv3=pnp;
    sv4=pop;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%
% Subsectors in sector 6 %
%%%%%%%%%%%%%%%%%%%%%%%%%%
% Sector S61
if Uref1_ang >= -pi/3 && Uref1_ang < -pi/6 && Uref2_ang2 >= pi/3 &&
Uref2_ang2 < 2*pi/3
```

```
        N=6;
468     subsector=1;
        sv1=ono;
470     sv2=ooo;
        sv3=poo;
472     sv4=pop;
    end
474 % Sector S62
    if Uref1_ang >= -pi/6 && Uref1_ang < 0 &&  Uref2_ang2 >= -pi &&
476 Uref2_ang2 < -2*pi/3
        N=6;
478     subsector=2;
        sv1=onn;
480     sv2=ono;
        sv3=ooo;
482     sv4=poo;
    end
484 % Sector S63
    if Uref1_ang >= -pi/3 && Uref1_ang < -pi/6 && Uref2_ang2 >=0 &&
486 Uref2_ang2 < pi/3
        N=6;
488     subsector=3;
        sv1=ono;
490     sv2=pno;
        sv3=poo;
492     sv4=pop;
    end
494 % Sector S64
    if Uref1_ang >= -pi/6 && Uref1_ang < 0 &&  Uref2_ang2 >= -2*pi/3 &&
496 Uref2_ang2 < -pi/3
        N=6;
498     subsector=4;
        sv1=onn;
500     sv2=ono;
        sv3=pno;
502     sv4=poo;
    end
504 % Sector S65
    if Uref1_ang >= -pi/3 && Uref1_ang < -pi/6 && Uref2_ang2 >= -pi/3 &&
506 Uref2_ang2 < 0
        N=6;
508     subsector=5;
        sv1=ono;
510     sv2=pno;
        sv3=pnp;
512     sv4=pop;
    end
514 % Sector S66
    if Uref1_ang >= -pi/6 && Uref1_ang < 0 &&  Uref2_ang2 >= -pi/3 &&
516 Uref2_ang2 < 0
        N=6;
518     subsector=6;
        sv1=onn;
520     sv2=pnn;
        sv3=pno;
522     sv4=poo;
    end
524
```

```
%%%%%%%%%%%%%%%%%%%%%%%%
% On time calculation %
%%%%%%%%%%%%%%%%%%%%%%%%

Uref1_amp=abs(Uref1);
Uref1_ang=angle(Uref1)-(N-1)*pi/3;
K=sqrt(3)*Uref1_amp/(Vdc);
Ts=1/fsw;

if (N==1 || N==3 || N==5) && subsector==1
    t0=Ts*(2*K*sin(pi/3-Uref1_ang));
    t1=Ts*(2*K*sin(Uref1_ang));
    t2=Ts*(1-2*K*sin(pi/3+Uref1_ang));
end
if (N==2 || N==4 || N==6) && subsector==1
    t0=Ts*(2*K*sin(pi/3-Uref1_ang));
    t1=Ts*(1-2*K*sin(pi/3+Uref1_ang));
    t2=Ts*(2*K*sin(Uref1_ang));
end
if (N==1 || N==3 || N==5) && subsector==2
    t0=Ts*(2*K*sin(Uref1_ang));
    t1=Ts*(1-2*K*sin(pi/3+Uref1_ang));
    t2=Ts*(2*K*sin(pi/3-Uref1_ang));
end
if (N==2 || N==4 || N==6) && subsector==2
    t0=Ts*(2*K*sin(Uref1_ang));
    t1=Ts*(2*K*sin(pi/3-Uref1_ang));
    t2=Ts*(1-2*K*sin(pi/3+Uref1_ang));
end
if (N==1 || N==3 || N==5) && subsector==3
    t0=Ts*(1-2*K*sin(Uref1_ang));
    t1=Ts*(1-2*K*sin(pi/3-Uref1_ang));
    t2=Ts*(2*K*sin(pi/3+Uref1_ang)-1);
end
if (N==2 || N==4 || N==6) && subsector==3
    t0=Ts*(1-2*K*sin(Uref1_ang));
    t1=Ts*(2*K*sin(pi/3+Uref1_ang)-1);
    t2=Ts*(1-2*K*sin(pi/3-Uref1_ang));
end
if (N==1 || N==3 || N==5) && subsector==4
    t0=Ts*(1-2*K*sin(pi/3-Uref1_ang));
    t1=Ts*(2*K*sin(pi/3+Uref1_ang)-1);
    t2=Ts*(1-2*K*sin(Uref1_ang));
end
if (N==2 || N==4 || N==6) && subsector==4
    t0=Ts*(1-2*K*sin(pi/3-Uref1_ang));
    t1=Ts*(1-2*K*sin(Uref1_ang));
    t2=Ts*(2*K*sin(pi/3+Uref1_ang)-1);
end
if (N==1 || N==3 || N==5) && subsector==5
    t0=Ts*(2-2*K*sin(pi/3+Uref1_ang));
    t1=Ts*(2*K*sin(pi/3-Uref1_ang)-1);
    t2=Ts*(2*K*sin(Uref1_ang));
end
if (N==2 || N==4 || N==6) && subsector==5
    t0=Ts*(2-2*K*sin(pi/3+Uref1_ang));
    t1=Ts*(2*K*sin(Uref1_ang));
    t2=Ts*(2*K*sin(pi/3-Uref1_ang)-1);
end
```

```
    if (N==1 || N==3 || N==5) && subsector==6
586     t0=Ts*(2-2*K*sin(pi/3+Uref1_ang));
        t1=Ts*(2*K*sin(pi/3-Uref1_ang));
588     t2=Ts*(2*K*sin(Uref1_ang)-1);
    end
590 if (N==2 || N==4 || N==6) && subsector==6
        t0=Ts*(2-2*K*sin(pi/3+Uref1_ang));
592     t1=Ts*(2*K*sin(Uref1_ang)-1);
        t2=Ts*(2*K*sin(pi/3-Uref1_ang));
594 end

596 %%%%%%%%%%%%%%%%%%%%%%%%%
    % Gate signal generation %
598 %%%%%%%%%%%%%%%%%%%%%%%%%
    if time >= 0 && time < (t0/4)
600     ua1=sv1(1);
        ua2=sv1(2);
602     ua3=sv1(3);
        ua4=sv1(4);
604     va1=sv1(5);
        va2=sv1(6);
606     va3=sv1(7);
        va4=sv1(8);
608     wa1=sv1(9);
        wa2=sv1(10);
610     wa3=sv1(11);
        wa4=sv1(12);
612 end
    if time >= t0/4 && time < (t0/4+t1/2)
614     ua1=sv2(1);
        ua2=sv2(2);
616     ua3=sv2(3);
        ua4=sv2(4);
618     va1=sv2(5);
        va2=sv2(6);
620     va3=sv2(7);
        va4=sv2(8);
622     wa1=sv2(9);
        wa2=sv2(10);
624     wa3=sv2(11);
        wa4=sv2(12);
626 end
    if time >= t0/4+t1/2 && time < Ts/2-t0/4
628     ua1=sv3(1);
        ua2=sv3(2);
630     ua3=sv3(3);
        ua4=sv3(4);
632     va1=sv3(5);
        va2=sv3(6);
634     va3=sv3(7);
        va4=sv3(8);
636     wa1=sv3(9);
        wa2=sv3(10);
638     wa3=sv3(11);
        wa4=sv3(12);
640 end
    if time >=Ts/2-t0/4 && time < Ts/2
642     ua1=sv4(1);
        ua2=sv4(2);
```

```
644      ua3=sv4(3);
         ua4=sv4(4);
646      va1=sv4(5);
         va2=sv4(6);
648      va3=sv4(7);
         va4=sv4(8);
650      wa1=sv4(9);
         wa2=sv4(10);
652      wa3=sv4(11);
         wa4=sv4(12);
654  end
     if time >= Ts/2 && time < Ts/2+t0/4
656      ua1=sv4(1);
         ua2=sv4(2);
658      ua3=sv4(3);
         ua4=sv4(4);
660      va1=sv4(5);
         va2=sv4(6);
662      va3=sv4(7);
         va4=sv4(8);
664      wa1=sv4(9);
         wa2=sv4(10);
666      wa3=sv4(11);
         wa4=sv4(12);
668  end
     if time >= Ts/2+t0/4 && time < Ts/2+t0/4+t2/2
670      ua1=sv3(1);
         ua2=sv3(2);
672      ua3=sv3(3);
         ua4=sv3(4);
674      va1=sv3(5);
         va2=sv3(6);
676      va3=sv3(7);
         va4=sv3(8);
678      wa1=sv3(9);
         wa2=sv3(10);
680      wa3=sv3(11);
         wa4=sv3(12);
682  end
     if time >= Ts/2+t0/4+t2/2 && time < Ts-t0/4
684      ua1=sv2(1);
         ua2=sv2(2);
686      ua3=sv2(3);
         ua4=sv2(4);
688      va1=sv2(5);
         va2=sv2(6);
690      va3=sv2(7);
         va4=sv2(8);
692      wa1=sv2(9);
         wa2=sv2(10);
694      wa3=sv2(11);
         wa4=sv2(12);
696  end
     if time >= Ts-t0/4 && time < Ts
698      ua1=sv1(1);
         ua2=sv1(2);
700      ua3=sv1(3);
         ua4=sv1(4);
702      va1=sv1(5);
```

```
        va2=sv1(6);
704     va3=sv1(7);
        va4=sv1(8);
706     wa1=sv1(9);
        wa2=sv1(10);
708     wa3=sv1(11);
        wa4=sv1(12);
710 end

712 u1=ua1;
    u2=ua2;
714 u3=ua3;
    u4=ua4;
716 v1=va1;
    v2=va2;
718 v3=va3;
    v4=va4;
720 w1=wa1;
    w2=wa2;
722 w3=wa3;
    w4=wa4;
```