TAMPERE UNIVERSITY OF TECHNOLOGY

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DESIGN OF A CASCADE CONTROLLED BOOST-POWER-STAGE CONVERTER FOR PHOTOVOLTAIC APPLICATION

Master of Science Thesis

Examiner: Teuvo Suntio
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Aurinkosähkögeneraattori muuttaa auringon sähkömagneettisen säteilyn sähköenergiaksi. Tehoelektroniikkalaitteet ovat tärkein väline tuotetun aurinkosähköenergian hallinnoinnissa esimerkiksi lähteen ja verkon välillä. Aurinkosähkögeneraattoriin kytketyn tehoelektroniikkalaitteen suunnittelu perustuu generaattorin sähköisiin ominaisuuksiin, kuten maksimilähtötehoon, oikosulkuvirtaan ja avoimen piirin jännitteeseen, jotka ovat riippuvaisia säteilytehotiheydestä ja lämpötilasta. Myös aurinkosähkögeneraattorin lähtöimpedanssilla on merkittävä vaikutus esimerkiksi säädön suunnitteluun. Tietyissä olosuhteissa mitattua Raloss SR30-36 aurinkopaneelin mittausdataa käytettiin hyödyksi tässä työssä.

Tässä työssä suunniteltiin aurinkosähkögeneraattorin lähtöön kytketty kaskadisäädetty jännitettä nostava teholähde. Säätö toteutettiin siten, että sisempi säätösilmukka kontrolloi kelavirtaa ja ulompi säätösilmukka vastaavasti sisäänmenojännitettä. Tämän työn päätavoitteena oli oikean dynaamisen mallin löytäminen, sekä dynaamisen resistanssin vaikutuksen tutkiminen säädön suunnittelussa. Prototyyppiteholähde rakennettiin ja digitaalinen säätö toteutettiin työssä esitellyn suunnittelun pohjalta. Prototyyppilaitteen suljetun silmukan taajuusvasteet, sekä jännitereferenssin askelvasteet mitattiin teoreettisen mallin avulla saatujen tulosten vahvistamiseksi. Idea tällaisen säädön testaamiseen saatiin hiljattain julkaistuista tutkimuksista.

Mittaustulokset vahvistivat, että työssä luotu teoreettinen malli vastaa oikean laitteen toimintaa. Tosin, jos säätö toteutetaan digitaalisesti, tulee näytteenottoviive ottaa huomioon suunnittelussa. Kaksi PI-säädintä riitti stabiilin järjestelmän aikaansaamiseen. Dynaamisella resistanssilla oli huomattava vaikutus säädön suorituskykyyn. Säätö reagoi hitaammin referenssin muutokseen, kun toimintapiste oli aurinkosähkögeneraattorin vakiojännitealueella. Dynaamisella resistanssilla ei ollut vaikutusta järjestelmän lähtöimpedanssiin. Lisätutkimusta tarvitaan esitellyn säädön toteuttamiskelpoisuuden varmistamiseksi, johon tämä työ antaa hyvän pohjan.

ABSTRACT

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A photovoltaic generator converts solar radiation into electrical energy. Power electronic converters are of prime importance in managing the produced energy e.g. between source and grid. Design of a photovoltaic generator interfacing converter is based on the electrical characteristics of the generator. Characteristics such as: maximum output power, short circuit current and open circuit voltage, which are dependent on the amount of insolation and the value of ambient temperature, are important to know when the converter is designed. Also, the dynamic resistance of a photovoltaic generator has a significant effect especially on the control design. Measurement data of the electrical characteristics of a Raloss SR30-36 solar panel measured in certain climate conditions was used in the design in this thesis.

In this thesis, a boost-power-stage converter with a cascaded inner inductor-current and outer input-voltage control was designed for photovoltaic generator interfacing. The main focus of this work is in obtaining a correct dynamic model for such a system, as well as, to evaluate the effect of the dynamic resistance on control. A prototype converter was built based on the design, and the control was implemented digitally. Every closed-loop frequency response of the converter and the responses to a voltage reference step-change were measured in order to verify the theoretical findings. The idea for testing this type of control was obtained from recent publications.

The measurement results confirmed that the obtained system model was correct, however, if the control is implemented digitally, the sampling delay should be taken into account in the design. Two PI-controllers were sufficient for providing a stable system. Control performance was significantly affected by the dynamic resistance. The control was much slower when the operation point was in the constant voltage region. The dynamic resistance had no effect on the system output impedance. More research is needed in order to determine the feasibility of the proposed control, for which this thesis gives a good foundation.

PREFACE

This Master of Science thesis was made for the Department of Electrical Engineering at Tampere University of Technology. The examiner of the thesis was Professor Teuvo Suntio.

I would like to thank Prof. Teuvo Suntio for providing me with an interesting research topic, and also for his effort in revising this work. I would also like to thank M.Sc. Juha Jokipii for his help with the converter model and especially M.Sc. Jukka Viinamäki, who operated as my mentor during this process and helped me in pretty much every step of the way. A special acknowledgement belongs to my parents for their support.

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Mikko Niku

CONTENTS

TERMS AND SYMBOLS

NOTATION

$\mathbf{A}$	System matrix
A_c	Cross-sectional area of the core
A_L	Inductance per turn
A_w	Cross-sectional area of the wire
α	Material constant of the core
a	Diode ideality factor
$\mathbf{B}$	Input matrix
B_{max}	Maximum flux density
B_{sat}	Saturation flux density of the core
β	Material constant of the core
$\mathbf{C}$	Output matrix
C	Capacitance
Δ	Characteristic polynomial
$\Delta i_{L,pp}$	Inductor current peak-to-peak ripple
$\mathbf{D}$	Input-output matrix
d	Duty ratio
d'	Complement of duty ratio
D	Steady-state value of duty ratio
f_r	Resonant frequency
f_s	Switching frequency
G	Solar irradiance
$\mathbf{G}$	Converter transfer function matrix
g	Core air gap length
γ	Auxiliary variable
G_a	Modulator gain
G_{cc-L}	Inductor-current controller transfer function
G_{ci-c}	Closed current-loop control-to-input transfer function
G_{ci-c}^S	Source-affected closed current-loop control-to-input transfer function
G_{ci-cc}	Closed voltage-loop control-to-input transfer function
G_{ci-cc}^S	Source-affected closed voltage-loop control-to-input transfer function
G_{ci-o}	Open-loop control-to-input transfer function
G_{ci-o}^S	Source-affected open-loop control-to-input transfer function
G_{cL-o}	Control-to-inductor-current transfer function

G^S_{cL-o}	Source-affected control-to-inductor-current transfer function
G_{co-c}	Closed current-loop control-to-output transfer function
G_{co-cc}	Closed voltage-loop control-to-output transfer function
G_{co-o}	Open-loop control-to-output transfer function
G^S_{co-o}	Source-affected open-loop control-to-output transfer function
G_{cv}	Input-voltage controller transfer function
G_{iL-o}	Input-to-inductor-current transfer function
G^S_{iL-o}	Source-affected input-to-inductor-current transfer function
G_{io-c}	Closed current-loop input-to-output transfer function
G_{io-cc}	Closed voltage-loop input-to-output transfer function
G_{io-o}	Open-loop input-to-output transfer function
G^S_{io-o}	Source-affected open-loop input-to-output transfer function
G_n	Solar irradiance in standard test condition
G_{oL-o}	Output-to-inductor-current transfer function
G^S_{oL-o}	Source-affected output-to-inductor-current transfer function
G_{se-in}	Voltage sensing transfer function
i_0	Saturation current
$i_{0,n}$	Nominal saturation current
$I_{\mathrm{d,rms}}$	Root mean square of diode current
I_e	Magnetic path length of the core
i_{in}	Converter input current
I_L	Steady-state value of inductor-current
I_{max}	Converter maximum peak input current
i_o	Converter output current
i_{ph}	Photocurrent
$i_{ph,n}$	Photocurrent in standard test condition
$i_{sc,n}$	Short circuit current in standard test condition
$I_{\mathrm{SC,MAX}}$	Maximum short circuit current
$I_{\mathrm{sw,rms}}$	Root mean square of switch current
$\mathbf{I}$	Identity matrix
K	Current controller gain
K_v	Voltage controller gain
K_I	Temperature coefficient
K_g	Geometrical constant of the core
K_u	Winding fill factor
k	Boltzmann constant
K_m	Material constant of the core
K_c	Auxiliary variable
K_{cv}	Auxiliary variable

L	Inductance
L_c	Current loop gain
L_c^S	Source-affected current loop gain
L_{cv}	Voltage loop gain
L_s	Equivalent series inductance
M	Input to output modulo
μ_e	Effective permeability of the core
N_s	Number of series connected cells
N	Number of turns
ω_p	Angular frequency of current controller pole
ω_{p1}	Angular frequency of voltage controller pole
ω_z	Angular frequency of current controller zero
ω_{z1}	Angular frequency of voltage controller zero
$P_{\mathrm{d,cond}}$	Conduction power loss of the diode
$P_{\mathrm{d,rev}}$	Reverse leakage current power loss of the diode
$P_{\mathrm{d,tot}}$	Total power loss of the diode
P_{fe}	Time average core loss per unit volume
P_{sw}	Average switching power loss
$P_{\mathrm{sw,c}}$	Switch conduction loss
$P_{\mathrm{sw,tot}}$	Total power loss of the switch
q	Electron charge
r_{pv}	Dynamic resistance of a photovoltaic generator
R_{sL}	Current sensing transfer function
$\mathbf{s}$	Laplace variable
T_{amb}	Ambient temperature
T_{oi-c}	Closed current-loop reverse voltage transfer ratio
T_{oi-cc}	Closed voltage-loop reverse voltage transfer ratio
T_{oi-o}	Open-loop reverse voltage transfer ratio
T_{oi-o}^S	Source-affected open-loop reverse voltage transfer ratio
T_s	Switching period
$u_{oc,n}$	Open-circuit voltage in standard test condition
V_e	Effective magnetic volume of the core
W_A	Window area of the core
$W_{c(on)}$	Switch turn-on energy loss
$\hat{x}$	AC-perturbation around a steady-state operation point
Y_{o-c}	Closed current-loop output admittance
Y_{o-cc}	Closed voltage-loop output admittance
Y_{o-cc}^S	Source-affected closed voltage-loop output admittance
Y_{o-o}	Open-loop output admittance

Y_{o-o}^{S}	Source-affected output admittance
$Y_{o-\infty}$	Ideal output admittance
Y_s	Output admittance of a non-ideal source
Z_{in-c}	Closed current-loop input impedance
Z_{in-cc}	Closed voltage-loop input impedance
Z_{in-o}	Open-loop input impedance
Z_{in-o}^{S}	Source-affected input impedance
Z_{in-oco}	Open circuit input impedance
$Z_{in-\infty}$	Ideal input impedance
Z_{o-cc}^{S}	Source-affected closed voltage-loop output impedance
Z_o	Open-loop output impedance
Z_s	Output impedance of a non-ideal source

ABBREVIATIONS

AM	Air mass
CC	Constant current
CCM	Continuous current conduction
$CF-CO$	Current-fed current output
CO_2	Carbon dioxide
CV	Constant voltage
DC	Direct current
DCM	Discontinuous current conduction
DDR	Direct duty-ratio
DSP	Digital signal processor
ESL	Equivalent series inductance
ESR	Equivalent series resistance
$I-V$	Current to voltage
LHP	Left half-plane
MLT	Mean length per turn
MPP	Maximum power point
$MPPT$	Maximum power point tracking or tracker
PV	Photovoltaic
PVG	Photovoltaic generator
PWM	Pulse width modulation
RHP	Right half-plane
RMS	Root-mean-square
SAS	Solar array simulator
SF	Sizing factor
STC	Standard test conditions

1. INTRODUCTION

The world's energy consumption has skyrocketed after the years of industrial revolution. The energy need has increased because of growing population and higher standard of living. The current trend is that the energy demand is only going up. Globally in 2010, around 87% of the consumed energy was produced with fossil fuels i.e. coal (28%), natural gas (21%) and oil (38%). 6% came from nuclear plants and the remaining 7% came from renewable energy sources, such as hydro, wind, solar, geothermal and biofuels. The problem is, however, that the burning of fossil fuels generates pollutant gases, notably CO_2, which is the main contributor to greenhouse effect i.e. global warming. Another problem is, that the reserve of fossil fuels is limited, and it is estimated that e.g. oil would run out in 50 to 100 years. The global warming has serious effect on the world's ecological structure in the long run, such as severe droughts near the equator and the rise in sea level, which would ultimately drive 100 million people away from their homes. The need for renewable and clean energy is real, which is why many governments have started to invest on them, and new laws are legislated in order to cut down emissions. [1]

Recent studies have shown that all of the world's energy demand could be produced with renewable energy sources, assuming that there is an adequate storage for it. One of the alternatives is the solar or photovoltaic (PV) energy. The pros of solar energy are that it is abundantly available and the cost of PV panels, which convert the solar insolation directly into electricity, is decreasing due to intense development of these devices. However, the availability of solar energy is intermittent in nature, and therefore it needs a back-up support. All of these energy management issues can be handled with power electronics, which means that the design of reliable and efficient power electronic systems are of prime importance in fullfilling the recognized needs and to secure the availibility of energy in the future. [1]

In grid connected or energy storaging PV power systems, the PV generator (PVG) is usually interfaced with a dc-dc boost-power-stage converter with an added input-capacitor [2][3]. The converter is operated under input-voltage control, which changes the converter to be a current-fed converter [4]. The reference value for input-voltage control is obtained from a maximum power point (MPP) tracker to ensure maximum energy yield at all times. The operation of the converter and its control is affected by the operation point dependent output-impedance of the PVG,

which is referred to as a *dynamic resistance* in literature. The variance of dynamic resistance between operation points results in a variable damping factor in the boost converter duty cycle to input-voltage transfer function, but the system can be easily controlled with a simple I-controller. [5]

However, the performance of an input-voltage control is limited due to the resonance between the inductor and input-capacitor, thus resulting in a slow operation point tracking or ringing. Therefore, in order to improve the operation point tracking, reject the effect of abrupt irradiance variations, and eliminate the effect of dynamic resistance on control in a PVG interfacing converter, several new control methods have been proposed all based on a cascaded inner current and outer voltage control [6] [7] [8].

In this thesis, a simple cascade controlled boost-power-stage converter was designed for low power PVG application. The control consisted of an inner inductor-current control, which got its set-value from an outer input-voltage controller, thus forming a cascade. The objective of this thesis was to design a working device in its simplest form, obtain a correct method for modelling the dynamics associated with the system, as well as, to evaluate the effect of the dynamic resistance on closed-loop dynamics. A prototype converter was built and measured in order to verify the theoretical model and to present the performance of the designed control.

The rest of the thesis is organized as follows: Chapter 2 presents how the dynamics of the converter are modelled, and how the effect of the dynamic resistance can be included into it. In Chapter 3 the converter components are selected and their corresponding dynamic model values are determined. In Chapter 4 the control system is designed, and in Chapter 5 the measurements of the prototype converter built for this thesis are presented. It should be noted, that the control was designed without taking the sampling delay into account. The effect of sampling delay has been discussed in Chapter 5 ”Measurements”. The final chapter summarizes the most important results of this study.

2. BOOST-POWER-STAGE CONVERTER

The interfacing of photovoltaic generators (PVGs) into a downstream power system is usually done by utilizing power electronic converters. The interfacing scheme depends on the nature of the load. If the load is a dc battery, a dc-dc converter is applied, and if the load is an ac grid a dc-ac converter i.e. *an inverter* is needed. The ac grid interfacing can be divided further into two schemes: a single-stage and a double-stage conversion schemes. In the single-stage conversion scheme, the inverter input is directly connected to the PVG, and the ac side is feeding the grid. In the double-stage conversion scheme, there is a dc-dc converter between the PVG and the inverter (see Fig. 2.1). [9] [10, p. 5-6]

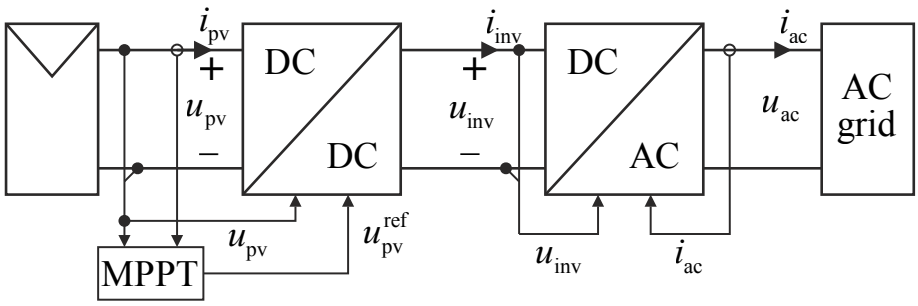

Figure 2.1. The principle of a double-stage conversion scheme used in the grid-connected PV systems. [11]

Typically the converter topology used in a double-stage conversion scheme is a conventional boosting converter with an added input-capacitor [2][3]. Due to its voltage boosting property there can be less series connected photovoltaic (PV) cells or modules, which can be also beneficial in partial shading conditions [12]. The other advantages are that the topology includes an output-diode, which prevents current from flowing into the PVG at times of low irradiation, and the converter has continuous input-current, which reduces the size of the input-capacitor [2].

A PVG interfacing converter should control its input-current or input-voltage for setting the desired operation point. The desired operation point is usually the maximum power point (MPP) on the PVG's current to voltage (I-V) curve (see Fig. 2.7). A MPP-tracker (MPPT) is a general name to a piece of equipment that is allocated for tracking the MPP. The MPPT measures the PVG's output-current and output-

voltage, which are used to determine the MPP, and provides a duty-cycle or, as in Fig. 2.1, a set-value for the input-voltage controller of the dc-dc converter. The MPPT ensures that maximal power is transferred into the downstream system. [13]

Controlling the input-voltage of a PVG interfacing converter has advantages over the input-current control. The PV current is directly proportional to solar irradiation, which can change rapidly and in large scale. This means that the input-current control needs to be extremely fast in order to accurately follow the desired operation point, and if this is not the case, the control can easily saturate. The photovoltaic voltage on the other hand is only slightly affected by the insolation. The most significant factor affecting the photovoltaic voltage is the temperature, which has slow dynamics. This means that the preferred control variable is the PV voltage, and thus it has been conventionally used in a PVG interfacing converters. [2][13]

In this thesis, the control system designed for the boost converter is a cascaded inductor-current and input-voltage control. The current controller gets its set-value from the voltage controller, thus the current loop is inside the voltage loop. In this type of control, the outer control loop is the primary control loop, since the control is based on its reference value. This means that the input-voltage is effectively controlled.

According to general control engineering principles, the output variables are controllable and the input variables are uncontrollable. This means, that in order to control the input-voltage, which is usually adopted in the PVG interfacing converters, the input-voltage must be an output-variable i.e. a current-fed converter [3] [4]. Furthermore, the converter designed in this thesis is thought to be an a PVG interfacing converter feeding an input-voltage controlled inverter or a battery load. Dynamically these loads are seen approximately as a constant voltage loads. Based on the information presented in preceding paragraphs the converter designed here should be considered as a current-fed current output (CF-CO) converter.

2.1 Basic Operation

The main circuit of a boost-power-stage converter with an added input-capacitor is presented in Fig. 2.2, which is also the circuit configuration used for the boost converter designed in this thesis. It should be noted, that the load side inductor-current sensing resistor (see Fig. B.1) is omitted from this figure, since it does not affect the dynamics of the converter and introduces only more losses, at least in theory. The value of this resistor was added to the dc-resistance of the inductor in the converter model. A current-source at the input and a voltage-source load refer to a current-fed current out (CF-CO) type converter, which is discussed more closely in the next section.

A boost converter produces a dc output-voltage greater in magnitude than the

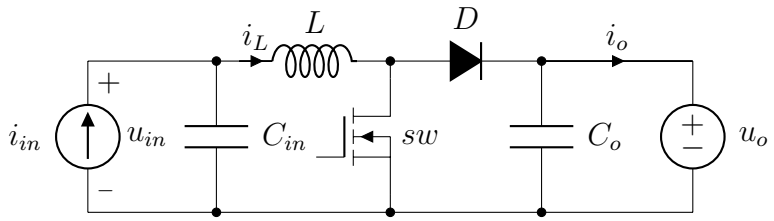

Figure 2.2. Main circuit of a boost-power-stage converter with an added input-capacitor.

dc input-voltage. This is possible because of the inductor stored energy. When the switch "*sw*" is closed and conducting current (on-time), the input-voltage appears across the inductor, current through it raises and energy is stored in the magnetic field of the inductor. When the switch is open and not conducting (off-time), the inductor-voltage switches polarity and the output-diode becomes forward biased. Both the energy stored in the magnetic field of the inductor, and the energy from the input source flows through the diode to the output in the form of electrical current. During this period the inductor current falls. On-time and off-time periods form one switching cycle, and by changing the length of these periods (i.e. changing duty-cycle D), one can affect the magnitude of the output-voltage.

Mathematically this can be represented by using an inductor volt-second balance concept i.e. the average inductor-voltage over one time-period must be zero:

$$\begin{aligned} \int_0^{DT_s} u_{L_{on}} dt + \int_{DT_s}^{T_s} u_{L_off} dt = 0 \Leftrightarrow \\ \int_0^{DT_s} U_{in} dt + \int_{DT_s}^{T_s} U_{in} - U_o \, dt = 0 \Leftrightarrow \\ M(D) = \frac{U_o}{U_{in}} = \frac{1}{1-D}, \end{aligned} \tag{2.1}$$

which applies when the voltage-ripples at the input and output are considered negligible, components are ideal, and the converter is at steady state. The input-to-output modulo $M(D)$ is always one or higher, meaning that the output-voltage is equal to the input-voltage or higher, respectively. Furthermore, assuming an ideal converter, the input power equals the output power. This means, that a dc-dc converter operates as a dc-dc transformer. [14, p. 22-27]

A steady-state condition is reached when the circuit waveforms repeat with a certain time period. In the case of switched-mode converters the time period is one switching cycle ($T_s = \frac{1}{f_s}$). After some time during start up, a switched-mode converter reaches a steady-state condition. When the inductor-current is flowing in positive direction (see Fig.2.2) changing around some average value as the on-time and off-time alternates, and never reaching zero, the converter is in continuous

current conduction mode (CCM).

The inductor-current peak-to-peak ripple in CCM can be calculated simply by using the inductor voltage-to-current relation:

$$u_L(t) = L\frac{di_L(t)}{dt} \approx L\frac{\Delta i_{L,pp}}{\Delta t} \Leftrightarrow \Delta i_{L,pp} = \frac{DT_s U_{in}}{L}, \tag{2.2}$$

where $\Delta i_{L,pp}$ is the inductor-current peak-to-peak ripple, $\Delta t = DT_s$ is the on-time time interval and $u_L = U_{in}$ is the inductor-voltage during on-time. In the same way, an analysis for the input- and output-voltage ripple could be done, and the results would show that the amount of ripple present depends on the capacitance of the respective capacitor. The input-voltage and inductor-current ripples need to be considered when designing the inductor-current and input-voltage measurement circuits, and their respective controllers. Moreover, the input-voltage ripple affects the operation point of the PV generator, which then again affects the energy yield.

It should be noted, that the dynamic analysis, which will be presented next, is valid only for CCM. In discontinuous current conduction mode (DCM), there is a third time-interval where the inductor-current is zero, which changes the dynamic behaviour of the converter substantially. [15]

2.2 Dynamic Modelling

The state-space averaging technique, first presented in [16], is the standard modelling technique for dc-dc converters. The same basic principles can be applied for modelling other power electronic converters also. The procedure yields in this case a linear small-signal model of a dc-dc converter, linearized around a steady-state operating point. Then the state-space model is Laplace-transformed to s-domain (i.e. frequency domain) yielding all transfer functions representing the system. At open-loop, a dc-dc converter operates as a dc-dc transformer having its dynamic properties determined by the source and the load.

In [5], the modelling of a CF-CO boost-power-stage converter with an input-capacitor is done by using a structured approach. The main circuit of a converter (same as in Fig. 2.2) is divided into two different subunits, which are modelled separately and then unified. The first part is the LC input-filter circuit, and another is PWM switching shunt unit. This method was implemented in the study, because it clearly shows that the LC-circuit is the source of two RHP-zeros appearing in the output dynamics of the converter. In this thesis, the whole circuit is modelled as a one unit.

The basis of the state-space averaging technique is to define the different states in which the converter can be. In the case of a dc-dc converter in CCM there are two states: the on-time, and the off-time states. During on-time in steady-state

the output circuit is isolated from the input, because the output-voltage is higher than the input-voltage. The on-time subcircuit of a boost-power-stage converter is presented in Fig. 2.3.

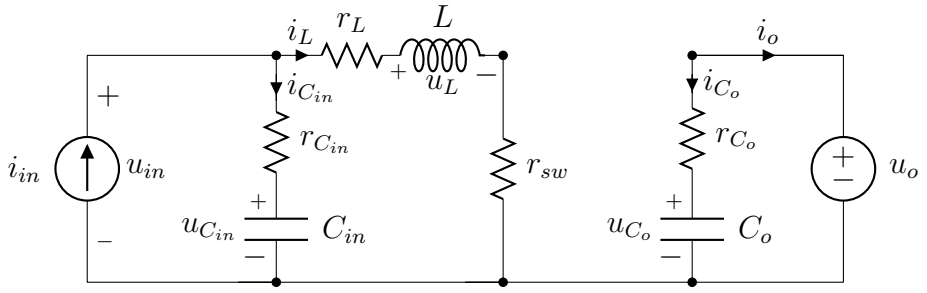

Figure 2.3. An on-time subcircuit of a boost-power-stage converter with an input capacitor.

In Fig. 2.3, the r_L represents both the *equivalent series resistance* (ESR) of the inductor and the value of the inductor-current sensing resistor. The inductor-current sensing resistor is discussed more in the converter design chapter. r_{sw} is the resistance of the switching component and $r_{C_{in}}$,r_{C_o} are the ESRs of the input and output capacitors, respectively. These values are usually found in the component datasheets fairly easily. Depending on the components, and the amount of measurement data given in their datasheets, one can build a fairly accurate model by using this level of accuracy in the converter model. However, in practice the parameters change from component to component (tolerance), so for the best accuracy one should measure the specific components, which are used to build the actual device on a printed circuit board.

Applying Kirchhoff's laws to the circuit in Fig. 2.3 and rearranging yields:

$$\begin{aligned} u_{L,on} &= i_{in} r_{C_{in}} + u_{C_{in}} - i_L(r_L + r_{C_{in}} + r_{sw}) \\ i_{C_{in},on} &= i_{in} - i_L \\ i_{C_o,on} &= \frac{u_o - u_{C_o}}{r_{C_o}} \\ u_{in,on} &= r_{C_{in}}(i_{in} - i_L) + u_{C_{in}} \\ i_{o,on} &= \frac{u_{C_o} - u_o}{r_{C_o}}. \end{aligned} \tag{2.3}$$

The off-time subcircuit is presented in Fig. 2.4. Inductor-voltage switches polarity at the same exact moment when the switch is turned off, and the sum of input-voltage and inductor-voltage is momentarily higher than the output-voltage. Now, because the switching component does not conduct current, the current has to flow through the diode.

Applying Kirchhoff's laws to the circuit in Fig. 2.4 and rearranging yields:

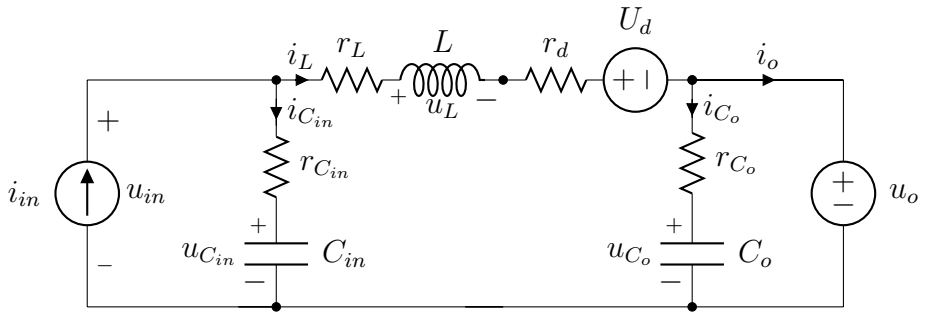

Figure 2.4. An off-time subcircuit of a boost-power-stage converter with an input capacitor.

$$
\begin{aligned}
u_{L,off} &= i_{in} r_{C_{in}} + u_{C_{in}} - i_L(r_L + r_{C_{in}} + r_d) - U_d - u_o \\
i_{C_{in},off} &= i_{in} - i_L \\
i_{C_o,off} &= \frac{u_o - u_{C_o}}{r_{C_o}} \\
u_{in,off} &= r_{C_{in}}(i_{in} - i_L) + u_{C_{in}} \\
i_{o,off} &= i_L + \frac{u_{C_o} - u_o}{r_{C_o}},
\end{aligned}
\tag{2.4}
$$

where r_d is the parasitic resistance of the diode and U_d is the voltage drop across it.

The next step is to average the on-time equations in Eq. 2.3 and the off-time equations in Eq. 2.4 over one switching cycle using duty-ratio (d) and complementary duty-ratio (d'), and recognizing that $d + d' = 1$. This yields the averaged state-space representation:

$$
\begin{aligned}
\frac{d\langle i_L\rangle}{dt} &= \frac{1}{L}(du_{L,on} + d'u_{L,off}) \\
&= -\frac{(r_{C_{in}} + r_L + dr_{sw} + d'r_d)}{L}\langle i_L\rangle + \frac{\langle u_{C_{in}}\rangle}{L} + \frac{r_{C_{in}}}{L}\langle i_{in}\rangle - \frac{d'(\langle u_o\rangle - U_d)}{L} \\
\frac{d\langle u_{C_{in}}\rangle}{dt} &= \frac{1}{C_{in}}(di_{C_{in},on} + d'i_{C_{in},off}) \\
&= \frac{\langle i_{in}\rangle - \langle i_L\rangle}{C_{in}} \\
\frac{d\langle u_{C_o}\rangle}{dt} &= \frac{1}{C_o}(di_{C_o,on} + d'i_{C_o,off}) \\
&= \frac{\langle u_o\rangle - \langle u_{C_o}\rangle}{C_o r_{C_o}} \\
\langle u_{in}\rangle &= du_{in,on} + d'u_{in,off} \\
&= r_{C_{in}}(\langle i_{in}\rangle - \langle i_L\rangle) + \langle u_{C_{in}}\rangle \\
\langle i_o\rangle &= di_{o,on} + d'i_{o,off} \\
&= \frac{\langle u_{C_o}\rangle - \langle u_o\rangle}{r_{C_o}} + d'\langle i_L\rangle .
\end{aligned}
\tag{2.5}
$$

The steady-state operating point can be solved from averaged state-space Eq. 2.5 by recognizing that the derivatives of the average values are zero in steady-state and replacing average values with the corresponding steady-state values. This procedure and rearranging gives:

$$
\begin{aligned}
U_{in} &= D'U_o + (r_L + Dr_{sw} + D'r_d)I_{in} + D'U_d \\
D' &= \frac{U_{in} - (r_L + r_{sw})I_{in}}{U_o + U_d + (r_d + r_{sw})I_{in}} \\
I_L &= I_{in} \\
U_o &= U_{C_o} \\
U_{in} &= U_{C_{in}} \\
I_o &= D'I_L.
\end{aligned}
\tag{2.6}
$$

The final small-signal model for the converter can be found when the average state-space model in Eq. 2.5 is linearized at a desired operation point by developing partial derivatives for every variable (i.e. average value). Mathematically this can be presented e.g. for variable x_1:

$$
\left.\frac{\partial f(x_1, x_2 = X_2, ..., x_n = X_n)}{\partial x_1}\right|_{x_1 = X_1} \cdot \hat{x}_1, \tag{2.7}
$$

which means verbally that variable x_1 is first differentiated with itself, and the other variables are replaced with their corresponding steady-state values. Then

variables of x_1 are replaced with steady-state values, and finally the whole equation is multiplied with small signal variable $\hat{x}_1$.

Linearizing of the averaged state-space representation yields the following:

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} &= -\frac{R_{eq}}{L}\hat{i}_L + \frac{1}{L}\hat{u}_{C_{in}} + \frac{r_{C_{in}}}{L}\hat{i}_{in} - \frac{D'}{L}\hat{u}_o + \frac{U_{eq}}{L}\hat{d} \\
\frac{d\hat{u}_{C_{in}}}{dt} &= \frac{\hat{i}_{in} - \hat{i}_L}{C_{in}} \\
\frac{d\hat{u}_{C_o}}{dt} &= \frac{\hat{u}_o - \hat{u}_{C_o}}{C_o r_{C_o}} \\
\hat{u}_{in} &= r_{C_{in}}(\hat{i}_{in} - \hat{i}_L) + \hat{u}_{C_{in}} \\
\hat{i}_o &= \frac{\hat{u}_{C_o} - \hat{u}_o}{r_{C_o}} + D'\hat{i}_L - I_{in}\hat{d},
\end{aligned} \tag{2.8}$$

where

$$\begin{aligned}
R_{eq} &= r_{C_{in}} + r_L + Dr_{sw} + D'r_d \\
U_{eq} &= (r_d - r_{sw})I_{in} + U_o + U_d.
\end{aligned} \tag{2.9}$$

The linearized state-space representation in Eqs: 2.8 and 2.9 can also be presented in matrix form:

$$\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{u}_{C_{in}}}{dt} \\ \frac{d\hat{u}_{C_o}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{eq}}{L} & \frac{1}{L} & 0 \\ -\frac{1}{C_{in}} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_o r_{C_o}} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{u}_{C_{in}} \\ \hat{u}_{C_o} \end{bmatrix} + \begin{bmatrix} \frac{r_{C_{in}}}{L} & -\frac{D'}{L} & \frac{U_{eq}}{L} \\ \frac{1}{C_{in}} & 0 & 0 \\ 0 & \frac{1}{C_o r_{C_o}} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \\ \hat{d} \end{bmatrix} \tag{2.10}$$

$$\begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} -r_{C_{in}} & 1 & 0 \\ D' & 0 & \frac{1}{r_{C_o}} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{u}_{C_{in}} \\ \hat{u}_{C_o} \end{bmatrix} + \begin{bmatrix} r_{C_{in}} & 0 & 0 \\ 0 & -\frac{1}{r_{C_o}} & -I_{in} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \\ \hat{d} \end{bmatrix}, \tag{2.11}$$

which can be then again presented as follows:

$$\begin{aligned}
\frac{d\hat{\mathbf{x}}(t)}{dt} &= \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) \\
\hat{\mathbf{y}}(t) &= \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{D}\hat{\mathbf{u}}(t).
\end{aligned} \tag{2.12}$$

One should now see that the column vectors: $\hat{\mathbf{x}}(t) = \begin{bmatrix} \hat{i}_L & \hat{u}_{C_{in}} & \hat{u}_{C_o} \end{bmatrix}^\top$, $\hat{\mathbf{u}}(t) = \begin{bmatrix} \hat{i}_{in} & \hat{u}_o & \hat{d} \end{bmatrix}^\top$ and $\hat{\mathbf{y}}(t) = \begin{bmatrix} \hat{u}_{in} & \hat{i}_o \end{bmatrix}^\top$ consists of state variables, input variables, and output variables, respectively. The Laplace transformations of equations in (2.12) are:

$$\begin{aligned}
s\mathbf{X}(s) &= \mathbf{A}\mathbf{X}(s) + \mathbf{B}\mathbf{U}(s) \\
\mathbf{Y}(s) &= \mathbf{C}\mathbf{X}(s) + \mathbf{D}\mathbf{U}(s).
\end{aligned} \tag{2.13}$$

Now by using common matrix manipulation techniques the input-to-output trans-

fer functions can be solved. First the upper equation in (2.13) is solved for $\mathbf{X}(s)$ yielding transfer functions for input-to-state variables: $\mathbf{X}(s) = [s\mathbf{I} - \mathbf{A}]^{-1}\mathbf{B}\mathbf{U}(s)$, which is then substituted to the lower equation. The result is:

$$\mathbf{Y}(s) = [\mathbf{C}[s\mathbf{I} - \mathbf{A}]^{-1}\mathbf{B} + \mathbf{D}]\mathbf{U}(s) = \mathbf{G}(s)\mathbf{U}(s), \tag{2.14}$$

where

$$\mathbf{G}(s) = \begin{bmatrix} Z_{in-o} & T_{oi-o} & G_{ci-o} \\ G_{io-o} & -Y_{o-o} & G_{co-o} \end{bmatrix} \tag{2.15}$$

contains every transfer function describing the system from input to output variables.

The final solution can be given in form:

$$\begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in-o} & T_{oi-o} & G_{ci-o} \\ G_{io-o} & -Y_{o-o} & G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \\ \hat{d} \end{bmatrix}. \tag{2.16}$$

The symbolic solutions for the open-loop transfer functions are:

$$\begin{aligned} \Delta Z_{in-o} &= \frac{1}{LC_{in}}(R_{eq} - r_{C_{in}} + sL)(1 + sr_{C_{in}}C_{in}) \\ \Delta T_{oi-o} &= \frac{D'}{LC_{in}}(1 + sr_{C_{in}}C_{in}) \\ \Delta G_{ci-o} &= \frac{-U_{eq}}{LC_{in}}(1 + sr_{C_{in}}C_{in}) \\ \Delta G_{io-o} &= \frac{D'}{LC_{in}}(1 + sr_{C_{in}}C_{in}) \\ Y_{o-o} &= \frac{D'}{L}\frac{s}{\Delta} + \frac{sC_o}{1 + sr_{C_o}C_o} \\ \Delta G_{co-o} &= -I_{in}(s^2 - (\frac{D'U_{eq}}{LI_{in}} - \frac{R_{eq}}{L}) + \frac{1}{LC_{in}}), \end{aligned} \tag{2.17}$$

where $\Delta = s^2 + \frac{R_{eq}}{L}s + \frac{1}{LC_{in}}$ is the characteristic equation.

The dynamics of the converter can also be represented with a linear two-port model (Fig. 2.5) shown inside the dashed line. The linear model is another way of representing the Eq. 2.16, and gives physical insight of the operation of the converter. The minus sign in front of Y_{o-o} originates from the fact that the direction of the output-current is out of the converter.

As it was stated earlier, the converter uses a cascade controller, in which there is an inner inductor-current control loop. For designing the inductor-current controller, the transfer functions from input-variables to inductor-current are needed. These can be obtained by using the two uppermost equations in linearized state-space

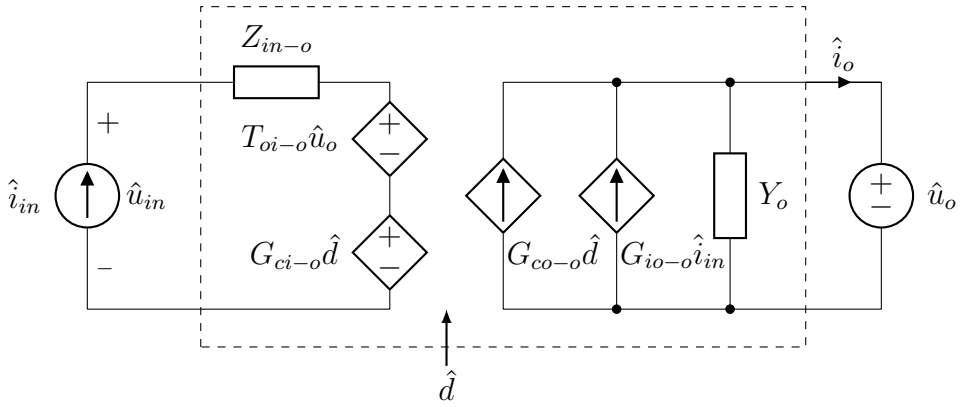

Figure 2.5. Linear two-port model of a CF-CO dc-dc converter with ideal terminations.

representation (see 2.8). The equations are repeated here for convenience:

$$\frac{d\hat{i}_L}{dt} = -\frac{R_{eq}}{L}\hat{i}_L + \frac{1}{L}\hat{u}_{C_{in}} + \frac{r_{C_{in}}}{L}\hat{i}_{in} - \frac{D'}{L}\hat{u}_o + \frac{U_{eq}}{L}\hat{d}$$
$$\frac{d\hat{u}_{C_{in}}}{dt} = \frac{\hat{i}_{in} - \hat{i}_L}{C_{in}}.$$

Now by recognizing that the Laplace-transform for time-derivative is s, and substituting $\hat{u}_{C_{in}}$ from the lower equation to the upper, the inductor current becomes:

$$\hat{i}_L = \underbrace{\frac{r_{C_{in}}s + \frac{1}{C_{in}}}{\Delta L}}_{G_{iL-o}}\hat{i}_{in} - \underbrace{\frac{D's}{\Delta L}}_{G_{oL-o}}\hat{u}_o + \underbrace{\frac{U_{eq}s}{\Delta L}}_{G_{cL-o}}\hat{d}, \tag{2.18}$$

where $\Delta = s^2 + \frac{R_{eq}}{L}s + \frac{1}{LC_{in}}$, and the corresponding input-to-inductor-current transfer functions are underbraced and denoted. The most important transfer function considering the inductor-current controller design is the control-to-inductor-current transfer function G_{cL-o}, which shows how pulse-width affects the inductor-current.

2.2.1 Photovoltaic Generator Effect

A PV generator is a device, which directly converts sunlight into electricity. A basic unit in a PVG is a photovoltaic cell. A set of connected cells form a panel (or a PV module). Series connection of PV cells yield higher output voltage, and parallel connection yield larger output current. PV cells can be connected in any way inside a solar panel to achieve wanted electrical properties. Usually, however, there are mostly series connected cells since the voltage of a one cell is fairly small (≈ 0.7V). Series and/or parallel connection of solar cells and solar panels form solar arrays. PV generator is the general term used to describe these systems. [17]

A PV cell is basically a p-n junction exposed to sunlight. When there is no light, the p-n junction is in thermal equilibrium, where the currents of majority - and minority charge carries are equal. Irradiance of light (or insolation) on the cell disrupts this equilibrium, and if the cell is short-circuited an electrical current is produced. Depending on the loading of a PV generator i.e. the balance between accumulation and the flow of charge carries, the PV generator inflicts different electrical properties at its output. The accumulation of charge carries means a raise in voltage, and the flow of charge carries corresponds with a current increase, respectively. [18] [17]

The electrical properties of a PV cell can be modelled with sufficient accuracy by using a one-diode model. This is presented in Fig. 2.6.

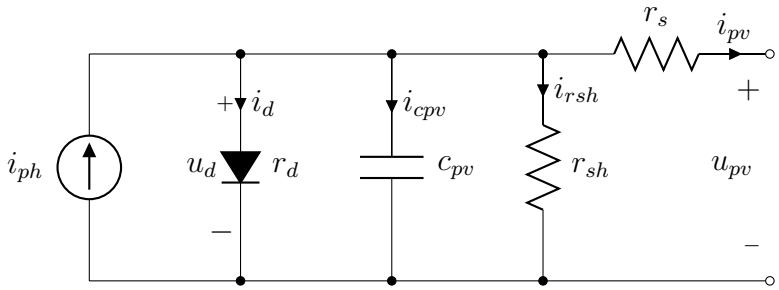

Figure 2.6. Simplified electrical equivalent circuit of a photovoltaic cell.

In Fig. 2.6 i_{ph} is the photocurrent, which is directly proportional to irradiance, u_{pv} and i_{pv} are the output-terminal voltage and current respectively, i_{rsh} is the current through the shunt resistance r_{sh} and i_{cpv} is the current through shunt capacitance c_{pv}. The shunt resistance r_{sh} represents non-idealities in the p-n junction and impurities near the junction [18]. The series resistance r_s results from the bulk resistance of the semiconductor material, metallic contacts and their interconnections [18]. The diode symbol illustrates the electrical properties of a p-n junction. The one-diode model can be used for modelling PV modules i.e. series connection of PV cells, by scaling model parameters [17].

An equation, which mathematically describes the static I-V (current to voltage) characteristics of a PV module can be formulated as:

$$i_{pv} = i_{ph} - i_o \left[\exp\left(\frac{u_{pv} + r_s}{N_s a k T/q} \right) - 1 \right] - \frac{u_{pv} + r_s i_{pv}}{r_{sh}}, \tag{2.19}$$

where N_s is the number of series connected cells, a is the diode ideality factor, k is the Bolzmann constant, T is the temperature of the p-n junction and q is the electron charge [17]. It should be noted, that this equation represents a static (DC) situation, so the capacitor in the one-diode model is an open circuit and does not contribute to this equation.

The saturation current i_0 in Eq. 2.19 is:

$$i_0 = i_{0,n} \left(\frac{T_n}{T}\right)^3 \exp\left[\frac{qE_g}{ak}\left(\frac{1}{T_n} - \frac{1}{T}\right)\right], \tag{2.20}$$

where T_n is the temperature of the p-n junction in *standard test conditions* (STC), which is defined in next paragraph, T is the actual temperature, E_g is the bandgap energy of the semiconductor and $i_{0,n}$ is the nominal saturation current, which can be expressed as:

$$i_{0,n} = \frac{i_{sc,n}}{\exp(u_{oc,n}q/N_s akT_n) - 1}, \tag{2.21}$$

where $i_{sc,n}$ is the short circuit current and $u_{oc,n}$ is the open circuit voltage both in the STC.

The term "STC" refers to climate conditions, in which the solar irradiance G is $1000\frac{W}{m^2}$, the ambient temperature T is $298.15K$, and *Air mass* is 1.5, which is usually abbreviated as AM1.5. The Air mass is the mass of air between a surface of the Earth and the Sun. The mass of air affects the spectral distribution of the light received by the PV device. The number after the abbreviation, as in AMx, indicates the length of the path the light travels through atmosphere. [19, p. 12]

The Eq. 2.19 can be enhanced by including the effect of the ambient temperature on photocurrent:

$$i_{ph} = (i_{ph,n} + K_I \Delta_T)\frac{G}{G_n}, \tag{2.22}$$

where $i_{ph,n}$ is the photovoltaic current at the STC, K_I is the temperature coefficient, Δ_T is the difference between actual temperature and the temperature in STC, G is the actual irradiance on the surface of the PV module and G_n is the irradiance on the surface of the PV module in STC. Equations 2.19-2.22 form the basis, from which the PVG model used in this thesis was built.

Typical static and dynamic characteristics of a PV module are shown in Fig. 2.7 as per unit values. The figure shows that a PV generator is internally a power limited non-linear current source having both constant current and constant voltage properties depending on the operation point. At MPP, the power produced by the PV module is at maximum value. The operating region from MPP to short circuit current i.e. maximum i_{pv}, is called a constant current (CC) region, and the operating region from MPP to open-circuit voltage i.e. maximum u_{pv} is called a constant voltage (CV) region, respectively.

The dynamic behaviour of a PV module is determined by its dynamic resistance $r_{pv} = r_d||r_{sh} + r_s$ and the shunt capacitor c_{pv}, which are non-linear and dependent on the operation point. As it is shown in [11], the dynamic capacitance can be

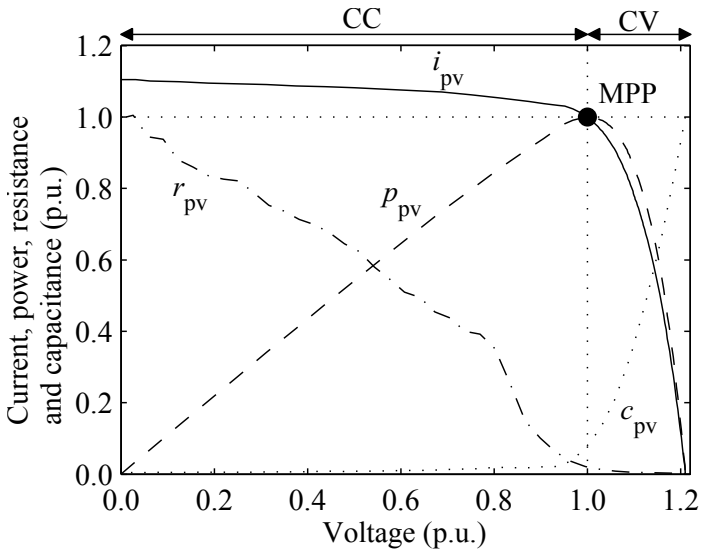

Figure 2.7. Static and dynamic terminal characteristics of a PV module. [11]

approximated from the PVG impedance measured in the study as:

$$c_{pv} \approx \frac{1}{2\pi r_{pv} f_{-3dB}}, \tag{2.23}$$

which is sufficiently accurate.

On the interfacing converter point of view the operating point dependent dynamic effect of a PVG can be taken into account by introducing a source admittance $Y_S = \frac{1}{Z_S}$. The source impedance is according to Fig. 2.6:

$$Z_S = r_s + r_d||r_{sh}||\frac{1}{sc_{pv}}, \tag{2.24}$$

which can be approximated to

$$Z_S \approx r_d||r_{sh}||\frac{1}{sc_{pv}} \approx r_{pv}||\frac{1}{sc_{pv}}, \tag{2.25}$$

under the assumption that $r_s = 0$ and $r_{pv} = r_d||r_{sh}+r_s$. Moreover at low frequencies:

$$Z_S \approx r_{pv}, \tag{2.26}$$

which is the approximation used in this thesis. The use of Eq. 2.26 is justified if the input capacitance of an interfacing converter is larger than the dynamic capacitance i.e. $C_{in} >> c_{pv}$, which is typically the case. [11]

Now the source effect on the dynamics of a converter can be included in the dynamic model by using the source admittance Y_S. See Fig. 2.8.

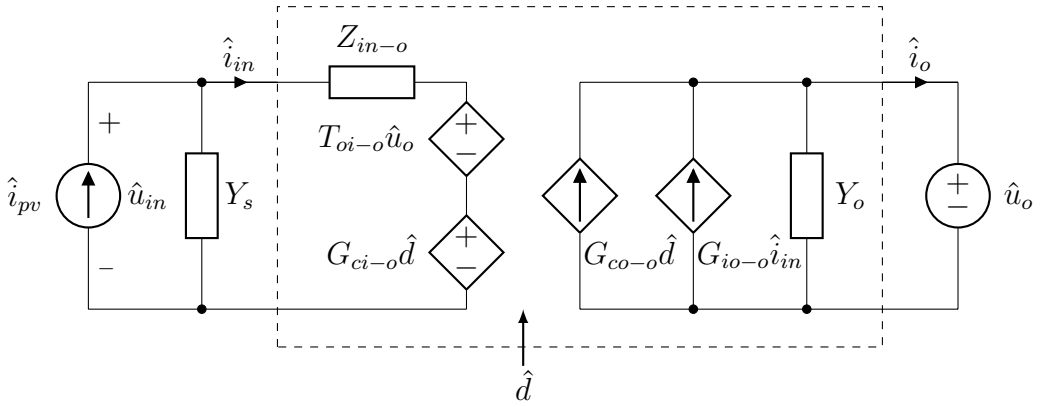

Figure 2.8. Linear two-port model of a CF-CO dc-dc converter with non-ideal source.

By comparing the input sources in figures 2.8 and 2.5 it can be seen that

$$\hat{i}_{in} = \hat{i}_{pv} - \hat{u}_{in} Y_S, \tag{2.27}$$

and by solving the input-voltage from Eq. 2.16 one gets:

$$\hat{u}_{in} = Z_{in-o}\hat{i}_{in} + T_{oi-o}\hat{u}_o + G_{ci-o}\hat{d}. \tag{2.28}$$

Substituting Eq. 2.27 to Eq. 2.28 and rearranging yields the source-affected input-voltage:

$$\hat{u}_{in} = \frac{Z_{in-o}}{1 + Z_{in-o}Y_S}\,\hat{i}_{pv} + \frac{T_{oi-o}}{1 + Z_{in-o}Y_S}\,\hat{u}_o + \frac{G_{ci-o}}{1 + Z_{in-o}Y_S}\,\hat{d}. \tag{2.29}$$

It should be noted, that the input-variable $\hat{i}_{in}$ has now changed to $\hat{i}_{pv}$ due to the source effect.

The source affected output-current can be solved in the same manner e.g. by substituting Eq. 2.29 into Eq. 2.27, and substituting the result into expression for output-current solved from Eq. 2.16. Rearraging gives:

$$\hat{i}_o = \frac{G_{io-o}}{1 + Z_{in-o}Y_S}\,\hat{i}_{pv} - Y_{o-o}\frac{1 + Y_S Z_{in-oco}}{1 + Z_{in-o}Y_S}\,\hat{u}_o + G_{co-o}\frac{1 + Y_S Z_{in-\infty}}{1 + Z_{in-o}Y_S}\,\hat{d}, \tag{2.30}$$

where

$$Z_{in-oco} = Z_{in-o} + \frac{G_{io-o}T_{oi-o}}{Y_{o-o}} \quad \text{and} \quad Z_{in-\infty} = Z_{in-o} - \frac{G_{io-o}G_{ci-o}}{G_{co-o}} \tag{2.31}$$

are the open circuit input impedance and ideal input impedance, respectively. Equations:(2.29)-(2.31) give the symbolic solutions to source affected dynamic model of

the converter at open loop:

$$\begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z^S_{in-o} & T^S_{oi-o} & G^S_{ci-o} \\ G^S_{io-o} & -Y^S_{o-o} & G^S_{co-o} \end{bmatrix} \begin{bmatrix} \hat{i}_{pv} \\ \hat{u}_o \\ \hat{d} \end{bmatrix}. \tag{2.32}$$

Next the source affected input-to-inductor-current transfer functions are solved. From the linearized state-space representation in Eq. 2.8 one can solve the following:

$$\begin{aligned} \hat{u}_{in} &= r_{C_{in}}(\hat{i}_{in} - \hat{i}_L) + \hat{u}_{C_{in}} \\ \hat{u}_{C_{in}} &= \frac{\hat{i}_{in} - \hat{i}_L}{sC_{in}}, \end{aligned}$$

and by substituting the lower to the upper, and rearraging one gets:

$$\hat{u}_{in} = (\frac{1}{sC_{in}} + r_{C_{in}})(\hat{i}_{in} - \hat{i}_L). \tag{2.33}$$

Substituting Eq. 2.33 into Eq. 2.27, solving it for $\hat{i}_{in}$, and substituting the result into 2.18 yields after rearranging:

$$(\frac{L\Delta}{s} - \frac{\gamma^2}{1+\gamma})\hat{i}_L = \frac{\frac{1}{sC_{in}} + r_{C_{in}}}{1+\gamma}\hat{i}_{pv} - D'\hat{u}_o + U_{eq}\hat{d}, \tag{2.34}$$

where $\gamma = Y_S(\frac{1}{sC_{in}} + r_{C_{in}})$, and $\Delta = s^2 + \frac{R_{eq}}{L}s + \frac{1}{LC_{in}}$. Solving equation 2.34 for $\hat{i}_L$ yields the wanted source affected input-to-inductor-current transfer functions.

2.3 Simulation Model of The Open-loop System

In previous sections, a dynamic model of the CF-CO boost-power-stage converter, and how the effect of a PVG can be included into it, was presented. In this section, a simulation model of the converter and PVG is built for analyzing the time-domain behaviour of the system. The software used for modelling and simulation was MATLAB^{TM}Simulink.

The simulation model of the converter can be built from the on -and off-time equations: 2.3 and 2.4. The resulting model is presented in Fig. A.1. It should be noted, that the notation is different in Fig. A.1 from the one used in previous sections. The converter variables: "C1, C2, rC1, rC2, uC1, uC2 and rds" in the simulation model correspond with variables: "C_{in}, C_o, $r_{C_{in}}$, r_{C_o}, $u_{C_{in}}$, u_{C_o}, and r_{sw}" used in the dynamic modelling section, respectively. The variables: "ipv, uo and duty" in the figure are the input-variables of the converter and correspondingly "upv and io" are the output-variables. The output "iL" is obviously the inductor-current output, and it is needed for connecting the inductor-current controller. Furthermore,

the inductor-current can not be negative due to the inherent output-diode in a boost converter, so its minimum value is limited to zero.

The Simulink model of a PV generator used in this thesis was developed in [18, p. 47-56] according to principles presented in [17]. The basic equations for the modeling were introduced in this thesis earlier Eqs: 2.19-2.21. The input-variables for the model are G the intensity of solar irradiation, T_{amb} the ambient temperature in Kelvins and voltage U, which determines the operating point on the PVG I-V curve. The output of the block is the PVG current. The model also takes other parameters for defining a given PVG.

In this thesis a commercial Raloss SR30-36 solar panel was selected as an example PVG. The Raloss SR30-36 is composed of 36 series connected 2A monocrystalline silicon cells with no bypass diodes in parallel with any of the cells. The model parameters of Raloss SR30-36 were:

Table 2.1. PVG model parameters for Raloss SR30-36 in STC.

Parameter	Value
Nominal power	30W
Short-circuit current in STC (I_{sc})	1.91A
Open-circuit voltage in STC (U_{oc})	21.81V
Temperature in STC	$298.15K$
Irradiance in STC (G)	$1000\frac{W}{m^2}$
Series resistance	0.9201Ω
Shunt resistance	346.3546Ω
Temperature coefficient of I_{sc}	0.0012
Temperature coefficient of U_{oc}	-0.0828
Temperature increase due to G	$0K$
Boltzmann constant	$1.3806503 \times 10^{-23}\frac{J}{K}$
Elementary charge	$1.60217646 \times 10^{-19}C$
Ideality factor	1.0
Number of cells	36

The PVG model parameters were determined experimentally through an iterative process as presented in [17]. The whole idea of the process is to match the remarkable points I_{sc}, U_{oc} and MPP of the model I-V curve to the ones presented on the datasheet.

The electrical -and dynamic properties of a real Raloss SR30-36 solar panel were measured during earlier studies in Tampere University of Technology. The measurement setup can be found e.g. from [20]. The measurement data included output-voltages -and currents with short-circuit current (I_{sc}) of 1A corresponding with an

irradiance of $G \approx 500\frac{W}{m^2}$. The average temperature during the measurements were $T \approx 44.2\text{C}^\circ$ according to the data. Also, the dynamic resistance r_{pv} was measured in several different operation points.

In Fig. 2.9, two I-V curves are presented. The measured I-V curve is based on the measured data of a Raloss SR30-36 panel, and another is simulated by using the PVG model and parameters presented in Table 2.1. The simulation was done in the same temperature as the average measurement temperature. The exact irradiance was not known, so it was selected to $G = 520\frac{W}{m^2}$, since it matched the measured short circuit current.

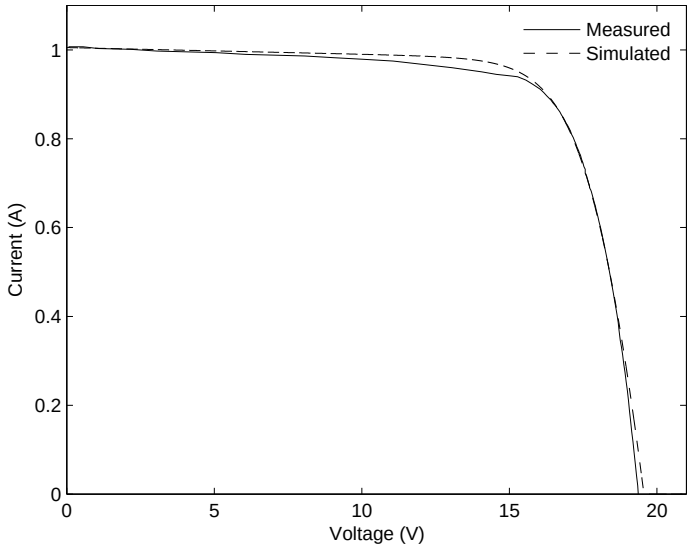

Figure 2.9. Measured and simulated Raloss SR30-36 I-V curves.

As it can be seen from Fig. 2.9, the correspondence of the I-V curves is fairly high. There is a slight deviance in the open-circuit voltage and in the CC region curve, however.

From the measurement data and the simulated I-V curve, the PVG operation points and the corresponding dynamic resistances for simulations and drawing the system transfer functions were selected as:

Table 2.2. The steady-state operation points of the system.

Operation region	Voltage U_{in}	Current I_{in}	Dynamic resistance r_{pv}
Constant current region (CC)	12V	0.99A	157Ω
Maximum power point (MPP)	16V	0.92A	17.4Ω
Constant voltage region (CV)	17V	0.82A	7.2Ω

The simulation model of the open-loop system is presented in Fig. A.2. The

simulation process advances as follows. At the beginning of a simulation, the operation point is selected from the table 2.2. Then the Duty-ratio D is calculated by using the second equation from top in 2.6 and the voltage and current values of the selected operation point. U_o is a constant. The switching pulse is generated in the PWM-block by comparing the calculated steady-state duty-ratio to a ramp signal having an amplitude of 1 and frequency of f_s. Some time after the simulation has been started, the converter reaches a steady-state point, and the output-values can be read. The converter is said to be at open-loop, and this type of control is called as the *direct duty-ratio control* (DDR-control).

3. CONVERTER DESIGN

In this chapter, a boost converter with an additional input capacitor in Fig. 2.2 is designed based on the maximum input-current of the source PVG. The principles used for selecting and designing the components are discussed, and their corresponding dynamic model parameter values are determined. The chapter is organized as follows: First, the properties of the source PVG are discussed, namely the maximum current it can provide. Next, based on the maximum input-current, an inductor is designed. Thirdly, the selection of the semiconductor components i.e. switch and diode is verified in terms of their loss power. Finally, the selection of the input and output-capacitors is discussed.

3.1 Maximum Input Current

There are several possible ways to determine the maximum input-current. In [21], the author designed two dc-dc converters using different design methods. In first of the methods, which was called as a conventional design method, the maximum input-current was determined by using a minimum input-voltage value of the PVG at MPP, and a sizing factor (SF). The sizing factor was presented as:

$$SF = \frac{P_{nom}}{P_{\text{PVG-STC}}}, \tag{3.1}$$

where P_{nom} is the nominal power of a solar inverter, which consists of a dc-dc converter and an inverter, and $P_{\text{PVG-STC}}$ is the maximum power of a given PVG at STC. Then a following equation was used:

$$I_{\text{IN,MAX}} = \frac{P_{\text{PVG-STC}}\text{SF}}{U_{\text{MPP,MIN}}}. \tag{3.2}$$

$U_{\text{MPP,MIN}}$ was calculated based on the fact that a rise in temperature decreases the open-circuit voltage of a PVG, which then again decreases the MPP voltage, and the fact that in partial shading conditions depending on the inner structure of a PVG, there might be some groups of series connected cells bypassed by diodes, which leads to lower output-voltage.

In the second method, which was referred as a new design method, the maximum input-current was determined by analyzing measurement data. The measured data

was obtained from the solar energy system located on the roof of Tampere University of Technology. The PV module used in the study was NAPS NP190Gkg. It was found that the maximum output-current of the NAPS NP190Gkg in any climate conditions is about 1.4 times the short-circuit current in STC.

The results of the study in question were that by using the new design method, the inductor core becomes smaller, there is less capacitance at the input, and the switching component heat sink becomes smaller than by using the conventional design method. Based on these results, the new design method i.e. determining the maximum input-current according to peak solar irradiance, was selected for designing the converter in this thesis. For Raloss SR30-36, the short-circuit current in STC is 1.91A according to the datasheet [22], so the maximum short-circuit current $I_{\mathrm{SC,MAX}}$ is $1.91A * 1.4 \approx 2.67A$, which is the converter maximum input-current.

By using a current value this high in the design, eventhough the actual converter is simulated and measured with smaller currents ($\leq$ 1.005A), it becomes certain that the converter could be supplied with a real Raloss SR30-36 solar panel, and the inductor core does not saturate in any condition.

3.2 Inductor Design

By solving duty-ratio from Eq. 2.1 and substituting the result into the Eq. 2.2, the equation for the inductor-current ripple can be formulated as:

$$\Delta i_{L,pp} = -\frac{T_s {U_{in}}^2}{U_o L} + \frac{T_s U_{in}}{L}. \tag{3.3}$$

Now by differentiating the Eq. 3.3 with respect to U_{in}, equating it to zero and solving it for U_{in} yields that the maximum inductor-current ripple can be found when $U_{in} = \frac{U_o}{2}$. Substituting this result back into Eq. 3.3, the minimum value of the inductance can be obtained as:

$$L = \frac{U_o}{4\Delta i_{L,pp} f_s}. \tag{3.4}$$

In this thesis, the value of the U_o was selected as 26V, because of the actual load configuration used in the measurements. The switching frequency was selected to 100kHz, since the control was coded on the digital signal processor (DSP) in such way, that the sampling frequency was the same, thus providing accurate enough transfer functions for the controllers. Furthermore, the maximum amount of inductor-current ripple was selected to be 20% of the input-current of 1A. With these values inserted into Eq. 3.4, the minimum value of the inductance becomes $L \approx 325\mu$H.

A power inductor consists of a magnetic core and a copper wire wound around it. The electrical and magnetic characteristics of a power inductor depends on numerous factors, which are e.g. the size of the magnetic core, and the material from which it is made of. One way for evaluating the size of a magnetic core for a given application is the core geometrical constant K_g, which is the first step in the inductor design procedure presented in [14, p.544-545]. According to this procedure the selected magnetic core has to satisfy the inequality:

$$\frac{{A_c}^2 W_A}{\mathrm{MLT}} \geq \frac{\rho L^2 {I_{max}}^2}{{B_{max}}^2 R K_u}, \quad (\mathrm{cm}^5) \tag{3.5}$$

where the left side of the equation equals the K_g. A_c is the cross-sectional area of the core, W_A is the core window area, MLT is the mean length per turn, ρ is the resistivity of the coil winding wire (1.724 $\mu\Omega \cdot$ cm at 25C° for copper), L is the desired inductance, I_{max} is the maximum current inside the converter: $I_{max} = I_{\mathrm{SC,MAX}} + \frac{\Delta i_{L,pp}}{2}$, B_{max} is the selected maximum flux density (should be lower than the saturation flux density B_{sat}), R is the resistance of the coil winding wire and K_u is the winding fill factor.

Epcos ETD29 core made of N87 (MnZn) ferrite was selected as the magnetic core of the inductor, since it was readily available. Ferrites in general are a popular choice for switched mode converter applications due to their low cost and low power loss. For the selected core, the geometrical parameters: saturation flux density, core window fill factor, size of an air gap, A_L value and effective permeability are presented in table 3.1. Values presented in the table can be found from the manufacturers datasheets: [23] and [24].

Table 3.1. Values for the ETD29 type core made of N87 material.

Variable	Explanation	Value
A_c	Core cross-sectional area	0.76cm^2
W_A	Core window area	0.97cm^2
MLT	Mean length per turn	5.28cm
B_{sat}	Saturation flux density	0.49T (25C°)
B_{sat}	Saturation flux density	0.39T (100C°)
K_u	Winding fill factor	0.4
g	Air gap	0.5±0.05mm
A_L	Inductance per turn	≈ 201nH
μ_e	Effective permeability	148
I_e	Magnetic path length	70.4mm
V_e	Effective magnetic volume	5350mm^3

Using the values presented in table 3.1, the rest of the unknown variables in Eq. 3.5 can be determined. Peak current through the inductor can be calculated as:

$$I_{max} = I_{\mathrm{SC,MAX}} + \frac{\Delta i_{L,pp}}{2} = 2.67A + \frac{0.2A}{2} = 2.77A. \tag{3.6}$$

The maximum flux density can be selected to any value lower than the saturation flux density. This was selected to 0.3 T for some safety margin. The A_L value is related to inductance and number of turns (N) by:

$$L = A_L N^2 \Leftrightarrow N = \pm\sqrt{\frac{L}{A_L}} = \sqrt{\frac{325\mu H}{201nH}} \approx 40 \text{ turns}. \tag{3.7}$$

The final unknown variable is the winding resistance, which can be calculated with an equation:

$$R = \rho_{Cu}\frac{N(\mathrm{MLT})}{A_w} = \frac{1.724\mu\Omega \cdot \mathrm{cm} * 40 * 5.28\mathrm{cm}}{0.00636\mathrm{cm}^2} \approx 0.0572\Omega, \tag{3.8}$$

where wire cross-sectional area A_w is for a wire of 0.9mm in diameter.

Now by substituting the presented values into Eq. 3.5, the right-hand side becomes:

$$\frac{\rho L^2 {I_{max}}^2}{{B_{max}}^2 R K_u} = \frac{1.724\frac{\mu\Omega}{\mathrm{cm}}(325\mu H)^2(2.77A)^2}{(0.3T)^2 * 0.056\Omega * 0.4}10^8 \approx 0.07 \text{ cm}^5, \tag{3.9}$$

where the multiplication with 10^8 is made to match the units. The left-hand side i.e. the geometrical constant K_g becomes:

$$K_g = \frac{{A_c}^2 W_A}{\mathrm{MLT}} = \frac{(0.76\mathrm{cm}^2)^2 * 0.97\mathrm{cm}^2}{5.28\mathrm{cm}} \approx 0.106 \text{ cm}^5, \tag{3.10}$$

so the inequality holds, and the selected core is large enough for the application.

During the previous analysis, the number of turns needed for obtaining the desired inductance was calculated. It should be verified that the selected number of turns does not saturate the core. This can be done with the following equation:

$$N_{max} = \frac{B_{sat} I_e}{\mu_o \mu_e I_{max}} = \frac{0.49\mathrm{T} * 0.0704\mathrm{m}}{4\pi * 10^{-7}\frac{\mathrm{H}}{m} * 148 * 2.77A} \approx 67 \text{ turns}. \tag{3.11}$$

In fact, if the Eq. 3.11 was solved for B, when N is the selected number of turns i.e. 40, the result is 0.293T. Furthermore, when it is taken into account that the maximum current fed into the converter in measurements is 1A, the core should not saturate in any situation.

Power is lost in the inductor due to core losses and copper losses. The core losses are a sum of hysteresis, eddy current and residual losses. The copper losses are

mainly caused by the dc resistance of the winding, however, at high frequencies the losses are further increased due to skin and proximity effects.

For estimating the time average core loss per unit volume, the general Steinmetz equation in Eq. 3.12 for sinusoidal excitation can be used [25, p. 14].

$$P_{fe} = K_m f^{\alpha} (\frac{\Delta B}{2})^{\beta} \tag{3.12}$$

In Eq. 3.12, K_m, α and β are material constants, which can be usually found from manufacturers' datasheets. For N87 material these values are: $K_m = 16.9$, $\alpha = 1.25$ and $\beta = 2.35$ [25, p. 20]. The ΔB is the variance in flux density due to the inductor-current ripple. This can be calculated by applying the Eq. 3.11. With an inductor-current ripple of 0.2A, the ΔB is 21.1mT. By substituting these values into Eq. 3.12, the approximated total core loss per unit volume is $683 \frac{W}{m^3}$, and by multiplying this result with effective magnetic volume V_e in Table 3.1 yields a total core power loss of 3.65mW.

The copper losses due to the average inductor-current can be calculated simply by Eq. 3.13.

$$P_{Cu,DC} = {I_L}^2 R \tag{3.13}$$

For $I_{\mathrm{SC,MAX}}$ this yields approximately 0.408W of power loss and for 1A the result is 57.2mW. Copper losses due to the inductor-current ripple were omitted from the total loss calculations, because of their relatively small size. The results of power loss calculations are presented in Table 3.2.

Table 3.2. Calculated power losses in the designed inductor.

Current	P_{CORE} (mW)	$P_{\mathrm{Cu,DC}}$ (mW)	P_{TOTAL} (mW)
$I_{\mathrm{SC,MAX}}$	3.65	408	412
$1A$	3.65	57.2	60.9

It should be noted, that the power loss calculation presented above does not include the power loss in the inductor-current sensing resistor. An inductor-current sensing resistor is needed for measuring the inductor-current. The sensing resistor is placed between the input-capacitor and the MOSFET on the returning current route, thus implementing a load-side current sensing (see Fig. B.1). As the current flows through the device and the inductor, a voltage related to this current appears across the sensing resistor. This voltage can be used to control the inductor-current. The prototype converter designed in this thesis used this type of current sensing technique. The measurement circuit used in the prototype converter is presented in Fig. B.3. The measurement circuit is designed in such way, that only the average value of the inductor-current is passed to the ad converter of the DSP board, meaning

that effectively the average value is controlled.

A Vishay WSL-series surface mountable resistor [26] of value 50mΩ was selected as the sensing resistor. The power loss in this component can be calculated similarly as the copper losses in the inductor by using the Eq. 3.13. This yields 50mW for an average inductor-current of 1A and for $I_{\mathrm{SC,MAX}}$ the result is 356mW. From this point forward, the value of the sensing resistor r_{SENSE} is included into the inductor resistance r_L.

3.3 Selection of Switching Component and Diode

In this section, the power lost in the selected switching component and diode during one switching cycle is calculated, since it verifies that the components can withstand the stress that is directed to them. A 2SK4017 n-channel MOSFET was selected as the switching component, and SK56C Schottky diode was selected as the rectifying output diode. These components were selected, since they were readily available, and there were no special demands regarding the converter design, except that the system should be stable.

The selection of n-channel MOSFET is justified, because the converter switching frequency is as high as 100kHz, and the converter operates at a fairly low currents i.e. low power application. Schottky diodes are used in the power electronic converters because of their low forward voltage drop and negligible reverse recovery loss. [27]

As it was stated in [21], the power loss in a switching component is maximized at a minimum input voltage (i.e. CC operation point), and in the diode it is at maximum in MPP. Keeping this in mind, the currents through the semiconductor components can be calculated as follows:

$$I_{\mathrm{sw,rms}} = I_L\sqrt{D}\sqrt{1+\frac{1}{3}\Big(\frac{\Delta i_{\mathrm{L,pp}}}{2I_L}\Big)^2}, \tag{3.14}$$

$$I_{\mathrm{d,rms}} = I_L\sqrt{D'}\sqrt{1+\frac{1}{3}\Big(\frac{\Delta i_{\mathrm{L,pp}}}{2I_L}\Big)^2}, \tag{3.15}$$

where 3.14 is the RMS-current through the switch, 3.15 is the RMS-current through the diode, respectively, and D' is the complementary duty-ratio $1-D$. The equation for inductor-current ripple is the same as in Eq. 2.2 and the duty-ratio must be calculated in a respective operation point by applying the equations in 2.6.

As it can be seen e.g. from Fig. 2.4, the diode is modelled in the dynamic model as a series connection of a voltage source U_d and a resistor r_d. The values of these components were determined via a graphical method from the forward characteristic curve of the diode, as illustrated in Fig. 3.1. The reciprocal of the red line slope in

Fig. 3.1 is the value of the diode dynamic resistance:

$$g_d = \frac{1}{r_d} = \frac{\Delta i_d}{\Delta U_d} \approx \frac{0.1A - 5A}{0.35V - 0.6V} = 19.6 \Leftrightarrow r_d \approx 51\text{m}\Omega, \tag{3.16}$$

and the starting point of the red line represents the value of the diode voltage $U_d \approx 0.35$V. This technique gives a fairly good approximation of the diode operation in the converter input-current range 0A-$I_{\text{SC,MAX}}$A.

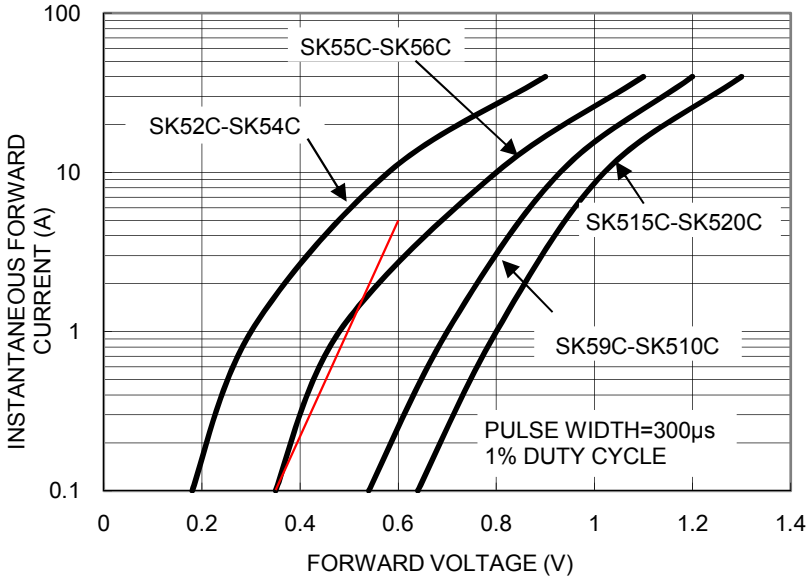

Figure 3.1. Typical forward characteristics of a SK56C diode and determination of a dynamic resistance (red line). [28]

Now by using this information, the on-time conduction loss of the MOSFET can calculated simply by:

$$P_{\text{sw,c}} = R_{\text{ds,on}} I^2_{\text{sw,rms}}, \tag{3.17}$$

where the $R_{\text{ds,on}}$ is the on-time resistance of the MOSFET, which is dependent on the drain-source voltage and the junction temperature. This value can be found from the device datasheet.

In reality, there are also losses generated by the switching action of the MOSFET, since the device turns on and off in a finite time. These losses can be approximated by assuming that the voltage across the device and the current through it vary linearly when the switch is changing its state. This is not the case in a real device, however, but it gives a sufficient approximation. This event is illustrated in Fig. 3.2 for the turn-on period.

In Fig. 3.2, the upper drawing illustrates the voltage and current of the MOSFET during turn-on time period t_{on} and the lower illustrates the energy loss $W_{c(on)}$

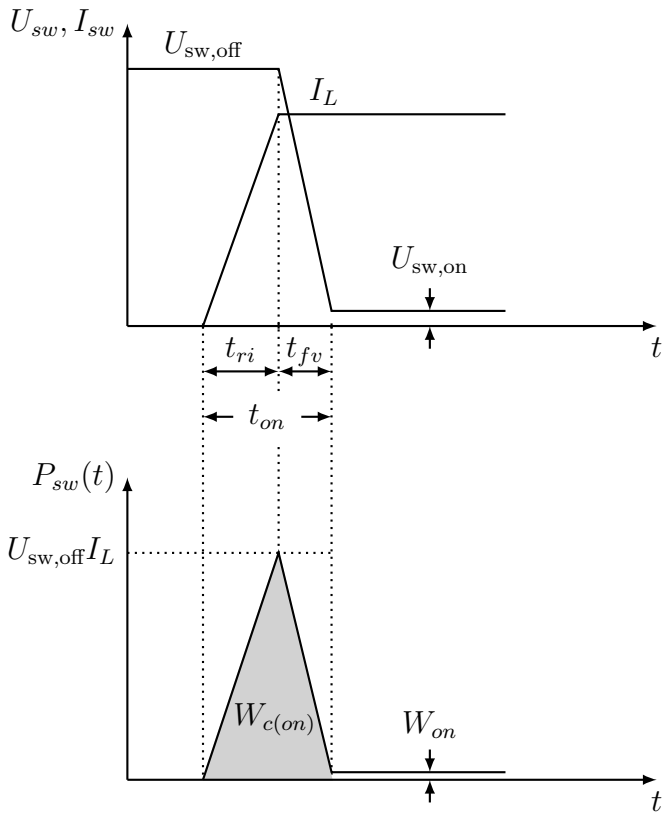

Figure 3.2. Turn-on voltage and current waveforms and energy loss of the switching component.

associated with it. Also, the conduction loss W_{on} is illustrated. It can be seen, that the turn-on event happens in two stages. First, there is the rise of the current during time period t_{ri} and then the fall of voltage during time period t_{fv}. These values can be found from the datasheet of the switching device. By using these values one can calculate turn-on loss as:

$$W_{c(on)} = \frac{1}{2} U_{\text{sw,off}} I_L t_{on}, \tag{3.18}$$

where $U_{\text{sw,off}} = U_o + U_d$. It can be also seen, that the energy loss during the switch transition is actually more significant than the conduction loss.

Similar event occurs during turn-off of the switch, although in reverse order. Depending on the switching device the turn-off time t_{off} might not be equal to the turn-on time, as it is the case with the selected 2SK4017 n-MOSFET. There are f_s such turn-on and turn-off transitions per second. Hence, the average switching power loss can be approximated as:

$$P_{sw} = \frac{1}{2} U_{\text{sw,off}} I_L f_s (t_{on} + t_{\text{off}}). \tag{3.19}$$

Schottky diodes have negligible reverse recovery loss due to their fast transition times. For this reason, the total power loss in the diode is the sum of the forward bias power loss $P_{\mathrm{d,cond}}$ and the power loss due to reverse leakage current $P_{\mathrm{d,rev}}$.

$$P_{\mathrm{d,tot}} = P_{\mathrm{d,cond}} + P_{\mathrm{d,rev}}, \tag{3.20}$$

where $P_{\mathrm{d,cond}} = U_d I_{\mathrm{d,rms}}$, and $P_{\mathrm{d,rev}} = U_{\mathrm{d,rev}} I_{\mathrm{d,rev}} D$. U_d is the forward voltage drop of the diode, $U_{\mathrm{d,rev}}$ is the reverse voltage of the diode and $I_{\mathrm{d,rev}}$ is the reverse leakage current. These values can be found from the diode datasheet, except the reverse voltage $U_{\mathrm{d,rev}}$, which can be calculated as follows: $U_o - I_L R_{\mathrm{ds,on}}$. Multiplication with the duty-ratio has to be made, since the reverse loss occurs only on during the on-time of the switch.

The values needed for the loss calculation can be found from the datasheets of the corresponding semiconductor devices: [29] for MOSFET and [28] for the diode. The diode forward voltage is $U_d \approx 0.48\mathrm{V}$ @ 1A, MOSFET turn-on time is $t_{on} = 20\mathrm{ns}$ and turn-off time is $t_{\mathrm{off}} = 35\mathrm{ns}$ respectively. By substituting these values into Eq. 3.19 one gets $P_{\mathrm{sw}} \approx 72.1\mathrm{mW}$ for switching loss.

By calculating the switch RMS-current with Eq. 3.14 at a CC operation point and substituting this value and $R_{\mathrm{ds,on}} = 0.07\Omega$ (typical @ $V_{GS} = 10\mathrm{V}$, $I_D = 2.5\mathrm{A}$ and $\mathrm{T} = 25°\mathrm{C}$) [29] into Eq. 3.17 one gets: $P_{\mathrm{sw,c}} \approx 38\mathrm{mW}$ for switch conduction loss.

For the diode conduction loss at MPP operation point $P_{\mathrm{d,cond}} = U_d I_{\mathrm{d,rms}}$, the forward voltage of the diode is $U_d \approx 0.46\mathrm{V}$ @ 0.92A according to datasheet [28], and $I_{\mathrm{d,rms}}$ was calculated according to Eq. 3.15. This yields $P_{\mathrm{d,cond}} \approx 0.33\mathrm{W}$.

The power loss due to the reverse leakage current:

$$P_{\mathrm{d,rev}} = U_{\mathrm{d,rev}} I_{\mathrm{d,rev}} D = (U_o - I_L R_{\mathrm{ds,on}}) I_{\mathrm{d,rev}} D, \tag{3.21}$$

where D and I_L are the converter steady-state values at MPP, and $I_{\mathrm{d,rev}}$ is $2.3\mu\mathrm{A}$ @ $\mathrm{T} = 25°\mathrm{C}$ and 42.26% of the rated peak reverse voltage, which is 60V for the selected diode ($\frac{U_{\mathrm{d,rev}}}{60V} \cdot 100\%$) [28]. This yields $P_{\mathrm{d,rev}} \approx 23.8\mu\mathrm{W}$.

The values used for the earlier loss calculations e.g. $I_{\mathrm{d,rev}}$ and $R_{\mathrm{ds,on}}$ vary in respect of temperature. For drain-to-source resistance $R_{\mathrm{ds,on}}$ this variance is not that significant (0.1Ω @ $\mathrm{T} = 100°\mathrm{C}$), but for the $I_{\mathrm{d,rev}}$ the variance is large (2.3mA @ $\mathrm{T} = 125°\mathrm{C}$). However, these variances do not affect much on the total power loss in the corresponding components.

The results of the power loss calculations are presented in Table 3.3.

Table 3.3. Results of the power loss calculations.

2SK4017 n-MOSFET (CC)	$P_{\mathrm{sw,c}}$	P_{sw}	$P_{\mathrm{sw,tot}}$
T = 25°C	38mW	72.1mW	100.1mW
T = 100°C	54.2mW	72.1mW	126mW

SK56C diode (MPP)	$P_{\mathrm{d,cond}}$	$P_{\mathrm{d,rev}}$	$P_{\mathrm{d,tot}}$
T = 25°C	0.33W	23.8 μW	0.33W
T = 125°C	0.33W	23.8 mW	353mW

Maximum average forward rectified current of the diode is 5A [28], which is never exceeded in this application, since the absolute maximum input-current I_{max} is 2.77A. Furthermore, the rated peak reverse voltage of 60V is not exceeded, as it can be deduced from the presented information. So, the diode is operating within safety margins, and thus it is suitable for the application.

Maximum drain power dissipation of the selected MOSFET is 20W @ T = 25°C and 7.5W @ T = 100°C [29]. According to presented power loss calculations these values are not exceeded in a continuous operation. The worst-case scenario occurs when the switch is half-way in changing its state from off to on i.e. the peak in Fig. 3.2. At this point the drain-to-source voltage is $U_{\mathrm{sw,off}} = U_o + U_d = 26V + 0.5V = 26.5V$, assuming CC operation point ($I_L = 0.99A$) and zero voltage drop across the inductor-current sensing resistor. Drain cutoff current i.e. off-time leakage current of the MOSFET is practically negligible $\approx 100\mu A$ @ $V_{DS} = 60V$, $V_{GS} = 0V$. This event is presented in Fig. 3.3 with a red line, for the idealized switching behaviour of the MOSFET. As it can be seen, the safety limits are never reached even if the input-current would be at maximum $I_{\mathrm{SC,MAX}} = 2.67\mathrm{A}$. Thus, the selected MOSFET is also suitable for the application.

3.4 Selection of Input and Output Capacitors

Panasonic FC-series radial lead type low-ESR aluminum electrolytic capacitors were selected for the actual converter, since they were easily available. In the series datasheet: [30], the capacitor impedance is given for every voltage rating and capacitance value at a 100kHz frequency, which is the same as the switching frequency f_s. From this value one can calculate an estimation for the ESR of a given capacitor as follows:

$$Z = \sqrt{(\mathrm{ESR})^2 + \left(\frac{1}{2\pi f C} - 2\pi f L_s\right)^2}, \tag{3.22}$$

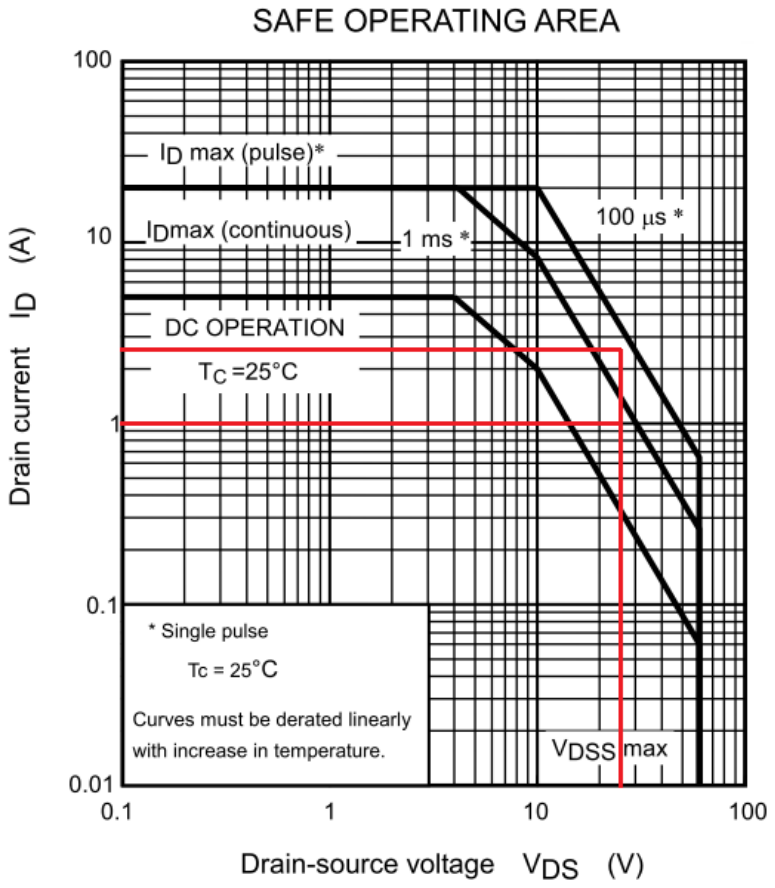

Figure 3.3. Idealized turn-on switching behaviour of the MOSFET (red line). Safety limits are presented assuming T=25°C. [29]

where L_s is the *equivalent series inductance* ESL of the capacitor, which was not given in the datasheet and therefore is unknown. This does not present a problem, however, since the ESR dominates the magnitude of the impedance at switching frequencies [31]. By estimating this value $L_s \approx 0$, and solving the equation for ESR gives:

$$\mathrm{ESR} = \sqrt{Z^2 - \left(\frac{1}{2\pi f C}\right)^2}. \tag{3.23}$$

Capacitors presented in 3.4 were selected from the series as candidates for being used in the converter.

Table 3.4. Capacitor candidates for the converter.

Capacitance (DC rating)	Impedance(100kHz,+20°C)	ESR	Max. ripple
10μF (50V)	1.3Ω	1.29Ω	163mV
22μF (35V)	0.8Ω	0.797Ω	140mV
47μF (50V)	0.6Ω	0.599Ω	156mV
68μF (63V)	0.342Ω	0.341Ω	139mV
100μF (35V)	0.117Ω	0.116Ω	65mV

Equation 3.23 was used for calculating the ESRs in Table 3.4 and the maximum voltage ripple rating of a given capacitor was calculated by multiplying the RMS (root-mean-square) ripple current rating with impedance. The ripple current ratings can also be found from the capacitor series datasheet.

As it can be seen from the Table 3.4, the ESR forms the most significant part of the component impedance at a switching frequency. Furthermore, the component impedance (i.e. ESR) tends to decrease as the capacitance increases. From the capacitor datasheet [30], one can see that the impedance decreases when the voltage rating rises. The maximum voltage ripple should not be exceeded or otherwise the component does not meet its spesified life-expectancy and in higher temperatures the electrolyte might reach its boiling point eventually leading to destruction of the component [31, p. 172].

The values of the input and output capacitors and their respective ESRs affect the voltage ripple at their corresponding terminals. The general trend is that when the ESR increases the ripple also increases, and when capacitance increases the ripple decreases.

The input-voltage ripple can be simulated by using the converter model developed in previous chapter, but the output-voltage ripple must be solved by other means, since it is an input-variable in the converter model, and thus cannot be simulated. The output-voltage peak-to-peak ripple can be estimated e.g. with a method presented in [14, p.26-27], where it is assumed that the load is a pure resistance yielding:

$$\Delta U_o = \frac{U_o D T_s}{2RC_o}. \tag{3.24}$$

The 100μF capacitor candidate from table 3.4 was selected for both the input and the output capacitor. As it can be deduced from the previous discussion, this candidate produces the least amount of ripple, and isn't too large for it to suppress the effect of the PVG output impedance i.e. dynamic resistance on frequency responses.

4. CONTROL DESIGN

In this chapter, two controllers are designed in order to control the inductor-current and the input-voltage simultaneously in a cascaded configuration. The inductor-current control loop is the inner loop and the input-voltage loop is the outer, thus the current controller gets its set-value from the voltage controller.

First, a short revision of relevant control engineering concepts and principles is presented. Then, the inductor-current controller is designed and the closed loop transfer functions are calculated. Next, the input-voltage controller is designed based on the closed loop transfer functions. The control design is done by using bode-diagrams and standard figure of merits associated with them i.e. the gain and the phase margins.

Table 4.1. CF-CO dc-dc boost converter dynamic model parameters. Note, that r_L includes the value of the inductor-current sensing resistor see Fig. B.1.

Parameters	Notation	Value
Inductor	L	325μH
Inductor ESR + r_{SENSE}	r_L	107.2 mΩ
Capacitors	C_{in} & C_o	100μF
Capacitor ESRs	$r_{C_{in}}$ & r_{C_o}	116 mΩ
Switch resistance	r_{sw}	70 mΩ
Diode voltage	U_d	0.35V
Diode resistance	r_d	51 mΩ
Output voltage	U_o	26V
Switching frequency	f_s	100kHz

The values of dynamic model parameters determined in previous chapter are collected in table 4.1. The control design is done by using these values.

4.1 Control Theory

A transfer function $G(s)$ of a given system describes its dynamic response. A transfer function is usually a ratio of two polynomials of s, where 's' is a Laplace variable. The roots of the numerator polynomial are called zeros ω_{zi}, and the roots of the denominator polynomial are called poles ω_{pi}. The zeros and poles can be real or

complex numbers. The location of zeros and poles on a complex plane determine the dynamic characteristics of a given system. The Laplace variable is related to complex numbers with $s = j\omega$, where ω is the angular frequency. Replacing the Laplace-variable s by $j\omega$ in a transfer function model $G(s)$ we get the so-called frequency response description. Hence, the frequency response describes the system's response to sinusoids of varying frequency. [32, p. 18]

The most common visualization methods of frequency responses are the polar and bode plots. When a polar plot is drawn for both positive and negative frequencies it is called a Nyquist plot. Plotting the magnitude (or gain) of a given system transfer function $|G(j\omega)|$ in decibels (dB) and phase angle $\angle G(j\omega)$ in degrees with respect to logarithmic frequency scale is a Bode plot.

A standard feedback control is used in this thesis for both variables wanted to be controlled. When designing feedback controllers one of the main issues is that if the closed-loop system is stable. Assuming a negative feedback the closed-loop transfer function from controller reference to output is $\frac{L(s)}{1+L(s)}$ i.e. the sensitivity function $S(s)$, where $L(s)$ is the loop gain. $L(s)$ consists of transfer functions of the system $G(s)$, controller and measurement circuit, as well as other dynamics in the feedback loop. The denominator of $S(s)$ i.e. $1 + L(s)$ is the characteristic equation. If the roots of a characteristic equation, i.e. the poles of a closed-loop transfer function, are located on the left half-plane (LHP) of a complex plane, the closed-loop system is stable. Correspondingly, if the poles of a closed-loop transfer function are located on the right half-plane (RHP) including the imaginary axis of a complex plane, the system is unstable. Zeros located on the RHP do not necessarily make the system unstable, but they introduce difficulties in the control design. A transfer function having a zero or zeros on the RHP or time delay is classified as a nonminimum phase transfer function, whereas if the zero(s) are located on the LHP, the transfer function is of minimum phase. [33, p. 320-321, 570]

The stability condition discussed in the previous paragraph can be determined directly from the frequency response plots. The Nyquist stability criterion states that the system is stable if the locus of a loop gain on a $L(s)$-plane does not pass through the point (-1,0) or encircle it in the clockwise direction when both of the loci are considered. Passing through the (-1,0) point in a Nyquist plot corresponds with a logarithmic magnitude of 0dB and a phase angle of 180° or -180° in a Bode plot of the loop gain $L(s)$. For open-loop stable systems (no RHP poles in $G(j\omega)$) where $\angle G(j\omega)$ crosses -180° only once "from above", one may use *Bode's stability condition* which says that the closed-loop system is stable if and only if the loop gain $|L|$ is less that 1 at this frequency [32]. Bode plots are used exclusively in this thesis, as well as, Bode's stability condition to determine the stability of a given system. [32, p. 28]

The gain and phase margins are related to the Bode's stability condition. The phase margin is the phase angle of a loop transfer function plus 180 degrees ($\angle L(s)+180°$) at the frequency where $|L(s)| = 1$ (i.e. at loop crossover frequency ω_{gco} or f_{gco}). The gain margin is $\frac{1}{|L(s)|}$ at frequency where $\angle L(s) = -180°$ or at phase crossover frequency ω_{phco} or f_{phco}. In other words, the gain and phase margins give margins for the stability of the system indicating robustness of the control. Typically a phase margin of 30° and a gain margin of 6dB is at least required [32, p. 35,36]. [15, p. 48]

Generally it can be deduced from a bode plot of a loop gain, that the higher the crossover frequency, the faster is the time-domain transient response of a system. Furthermore, in case of a second-order closed-loop system, to which many closed-loop systems approximate to, the larger the peak magnitude at resonant frequency, the more oscillatory the time response will be. [34, p. 172,191]

4.2 Inductor-Current Control

As it was stated, the open-loop transfer function needed for the inductor-current controller design is the duty-ratio-to-inductor-current transfer function:

$$G_{cL-o} = \frac{U_{eq}s}{\Delta L}, \tag{4.1}$$

where $U_{eq} = (r_d - r_{sw})I_{in} + U_o + U_d$, and $\Delta = s^2 + \frac{R_{eq}}{L}s + \frac{1}{LC_{in}}$. The equation in question does not contain RHP-zeros, so the system is of minimum phase. Because, the real source feeding the converter is a PV generator, its source-effect should be taken into account when designing the control system. Note, that the time-delay due to sampling and low-pass filtering of the inductor-current measurement circuit are not considered. It is shown later in "Measurements" -chapter, that especially the time-delay has a significant impact on the frequency responses. The source affected duty-ratio-to-inductor-current transfer function was solved in Eq. 2.34, and is repeated here for convenience:

$$G^S_{cL-o} = \frac{U_{eq}}{\frac{L\Delta}{s} - \frac{\gamma^2}{1+\gamma}}. \tag{4.2}$$

In Eq. 4.2 $\gamma = Y_S(\frac{1}{sC_{in}} + r_{C_{in}})$, and the other variables are the same as in Eq. 4.1.

The physical operation of the converter can be determined from the equations in 2.6. It can be seen, that the average inductor-current is equal to the average input-current, and cannot be controlled directly with duty-ratio. The inductor-current controller sets the operation point on the PVG I-V curve via input-voltage, which directly depends on the duty-ratio.

Now by substituting the converter values from Table: 4.1 and 100μF capacitor

value from Table: 3.4 into Eq. 4.2, and drawing the resulting transfer function in CC and CV operation points, which were given in Table: 2.2, yields the bode-diagram presented in Fig. 4.1.

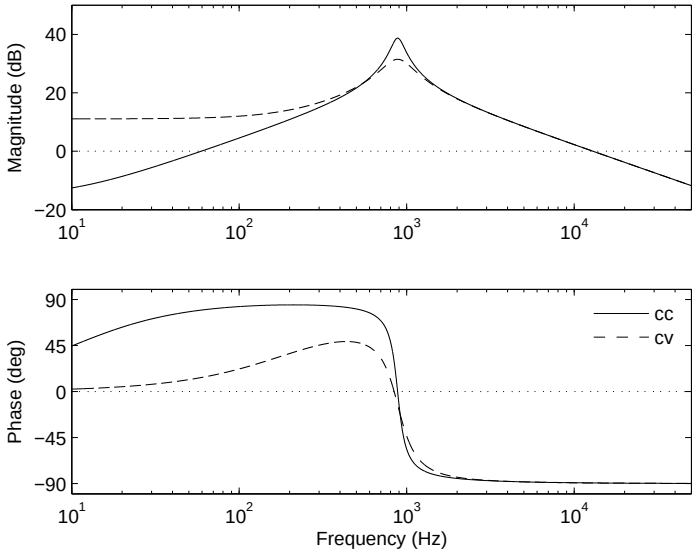

Figure 4.1. Bode-diagram of a source-affected duty-ratio to inductor-current transfer function G^S_{cL-o} in CC and CV operation points with a 100μF input-capacitor.

As it can be seen from the Fig. 4.1, a change in operation point i.e. in the dynamic resistance, affects both the magnitude and the phase curves. At CC operation point, the dynamic resistance is high (see Fig. 2.7) meaning that the source admittance $Y_s = \frac{1}{Z_s} \approx \frac{1}{r_{pv}}$ is low, and situation is similar to the ideal transfer function, where the dynamic resistance is infinitely high i.e. there is not much damping present at the resonant frequency and the slopes deviate from the ideal only at low frequencies ($f < 10$Hz). At CV operation point, the situation is another way around, the source admittance is high, which dampens the resonance peak and prevents the resonance circuit from operating (hence, the phase response). The high peaking at the resonant frequency is also due to the low ESR of the input-capacitor and low series resistance of the inductor.

Just to clarify the talk, the resonant frequency can be found around the area where the magnitude curve is peaking and the phase changes abruptly from positive to negative side. In Fig. 4.1, this frequency is about 900Hz. The resonant circuit is formed by the input-capacitor and the inductor of the converter. The resonant frequency can be calculated with a standard equation for the LC-resonant circuit:

$$f_r = \frac{1}{2\pi\sqrt{LC_{in}}}, \tag{4.3}$$

which indicates that when the capacitance of the input-capacitor is lowered, the

resonant frequency rises. This means that the magnitude curve crosses the 0dB at a higher frequency, effectively changing the loop crossover frequency when the control is applied i.e. affecting the control system performance. Because, the inductance used in the converter is large, the resonant frequency can be kept inside the control bandwidth, thus removing difficulties it might bring into the control design.

The following transfer function was used for the inductor-current controller:

$$G_{cc-L} = \frac{K(1 + \frac{s}{w_z})}{s(1 + \frac{s}{w_p})}, \tag{4.4}$$

where K is the gain of the controller, and w_z is the angular frequency of the zero, and w_p is the frequency of the pole. By looking the Fig. 4.1, one can see that at least an integrator is needed to modify the gain curve at low frequencies to over 0dB, as well as, to remove the steady-state error. The addition of integrator term shifts the phase curve down by -90°, which makes the loop nearly marginally stable, because of this a zero is needed to give enough phase margin. Finally, the controller gain is chosen in such way, that the wanted loop crossover frequency is obtained and the phase margin is maximized.

The pole in the controller transfer function is basically not needed, but it was added to modify the transfer function in such a way, that a limited integrator could be added into the simulink model of the converter, thus providing some limits for the controller response, which were 0-$I_{\mathrm{SC,MAX}}$ for the inductor-current controller. The same was done for the input-voltage controller for setting the output limits to 0-21.8V.

By selecting $K = 10^{\frac{65}{20}} \approx 1780$, $w_z = 2\pi * 950$, $w_p = 2\pi * 22000$, substituting them into Eq. 4.4 and multiplying the resulting transfer function with the transfer function represented in Fig. 4.1 yields the bode-diagram of the inductor-current loop in Fig. 4.2. It can be seen from Fig. 4.2 that the inductor-current loop is stable with a phase and gain margins of about 68° and infinite in this scope, respectively, and the crossover frequency is about 4.1kHz. The gain is 13.6dB at minimum inside the control bandwidth. It was decided, that these performance values are enough and reasonable. The control could be easily made much faster, with higher crossover frequency, and with a higher phase margin.

A control block diagram of the system at this state is illustrated in Fig. 4.3. In the figure, R_{sL} is the transfer function for inductor-current sensing. This was selected as 1, because the measurement gain is scaled to one in the control software, and the time-delay and the low-pass filtering action of the measurement circuit were not taken into account at this point in the design. Furthermore, G_a in the figure is modulator gain, which is an inverse of the height of a PWM ramp signal. Under digital control the modulator gain is an inverse of the number of steps in the digital

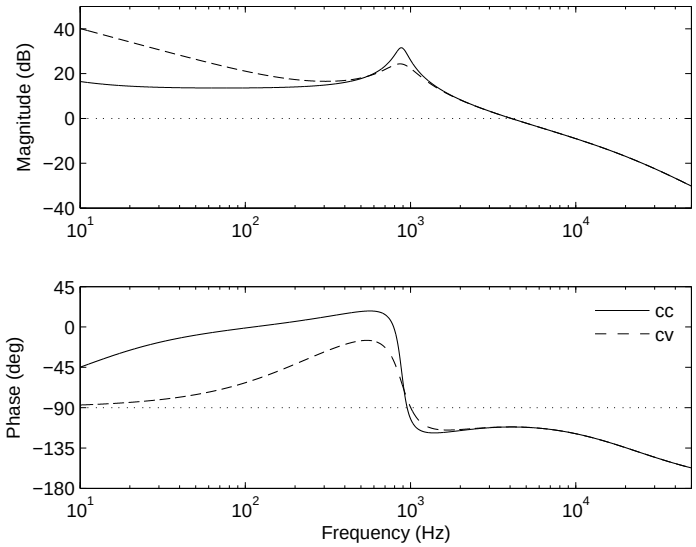

Figure 4.2. Bode-diagram of source-affected inductor-current loop ($G_{cc-L} * G^S_{cL-o}$) in CC and CV operation points with a 100μF input-capacitor.

ramp. The modulator gain was also selected as 1, because the height of the PWM-ramp signal is scaled to one inside the program code implementing the controller on the DSP board. The frequency response of the inductor-current loop "$G_{cc-L}G^S_{cL-o}$" is presented in Fig. 4.2.

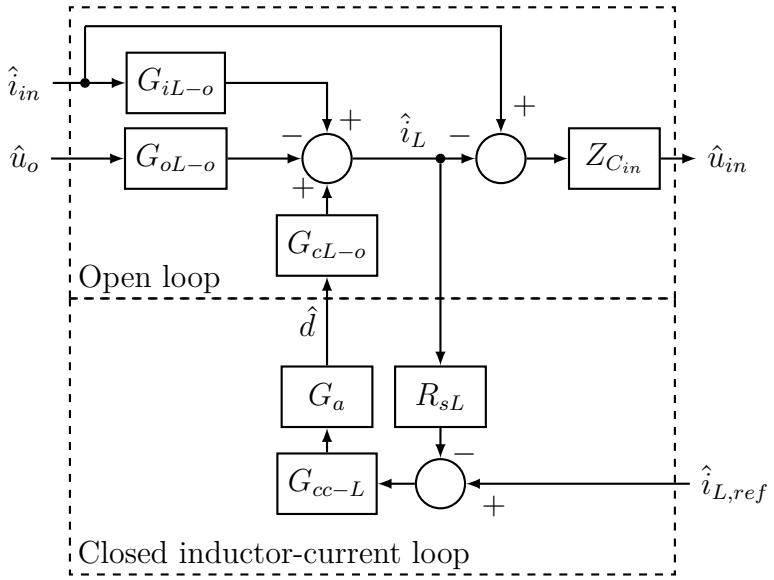

Figure 4.3. A control block diagram for solving the input-related closed-loop transfer functions.

It should be noted, that when the inductor-current loop is closed, a new system has formed, which has different input-variables $\hat{i}_{in}$,$\hat{u}_o$ and $\hat{i}_{L,ref}$. Fig. 4.3 describes

the prevailing situation only from an input-side point of view i.e. how the new input-variables affect the input-voltage. The transfer functions from new input-variables to output-current are not basically needed, since the controller designed in next section is an input-voltage controller. However, they are provided at the end of this section for the sake of completeness.

From Fig. 4.3 the following can be solved:

$$\hat{i}_L = (\hat{i}_{L,ref} - R_{sL}\hat{i}_L)G_{cc-L}G_aG_{cL-o} - G_{oL-o}\hat{u}_o + G_{iL-o}\hat{i}_{in}. \tag{4.5}$$

Solving Eq. 4.5 for $\hat{i}_L$, substituting the result into equation $\hat{u}_{in} = Z_{C_{in}}(\hat{i}_{in} - \hat{i}_L)$ and rearranging gives:

$$\hat{u}_{in} = Z_{in-c}\hat{i}_{in} + T_{oi-c}\hat{u}_o + G_{ci-c}\,\hat{i}_{L,ref}, \tag{4.6}$$

where

$$\begin{aligned} Z_{in-c} &= Z_{C_{in}} - \frac{Z_{C_{in}}G_{iL-o}}{1+L_c} \\ T_{oi-c} &= \frac{Z_{C_{in}}G_{oL-o}}{1+L_c} \\ G_{ci-c} &= -\frac{Z_{C_{in}}L_c}{(1+L_c)R_{sL}}, \end{aligned} \tag{4.7}$$

and $L_c = R_{sL}G_{cc-L}G_aG_{cL-o}$, $Z_{C_{in}} = r_{C_{in}} + \frac{1}{sC_{in}}$. A change in the subscripts from 'o' to 'c' after the dash in the transfer function denotation means that the loop is closed.

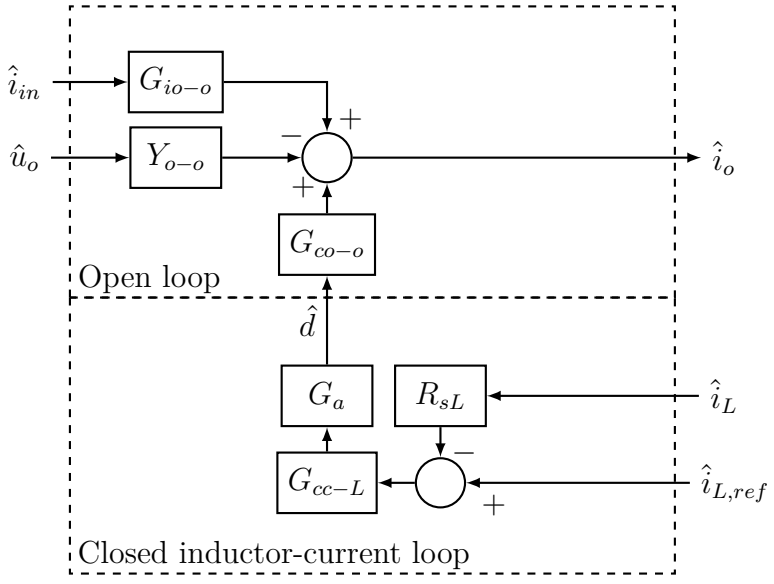

Figure 4.4. A control block diagram for solving the output-related closed-loop transfer functions.

The closed inductor-current loop transfer functions from input-variables to output-

current are:

$$\begin{aligned} G_{io-c} &= G_{io-o} - \frac{K_c G_{iL-o}}{1 + L_c} \\ Y_{o-c} &= \frac{K_c G_{oL-o}}{1 + L_c} - Y_{o-o} \\ G_{co-c} &= \frac{K_c}{R_{sL}(1 + L_c)}, \end{aligned} \tag{4.8}$$

where $K_c = R_{sL} G_{cc-L} G_a G_{co-o}$. The equations can be solved from Fig. 4.4 in same manner as in the case of input-voltage. The source-effect can be added to the presented equations similarly as in the case of open-loop transfer functions (see Eqs. 2.27-2.29).

In Figs. 4.3 and 4.4 the reference (or the set-value) for the inductor-current controller, denoted as $\hat{i}_{L,ref}$, is obtained from the input-voltage controller, which forms the outer control loop. So, the transfer function needed for designing the outer input-voltage controller is the source-affected transfer function from $\hat{i}_{L,ref}$ to $\hat{u}_{in}$ i.e. G^S_{ci-c}.

4.3 Cascade Control

"Cascade control arises from the control of two sequential processes where the output of the first or inner process supplies the second or outer process in the sequence." [35, p. 103] The steady-state solution of the converter in Eq. 2.6 describes the physical operation of the device. It can be seen, that this dependence exists since $I_L = I_{in}$, and U_{in} is affected by I_{in}. Thus, there are two main objectives in cascade control: "1. Use the inner measure to attenuate the effect of supply disturbances or any internal process disturbance on the outer process in the sequence. 2. Use the outer process measurement to control the process final output quality." [35, p. 104] Furthermore, the inner control loop should have sufficiently larger bandwidth than the outer control loop in order for them to be decoupled (not affecting each other much) [36]. It was assumed in this thesis that a ten times larger bandwidth would be sufficient.

As it can be seen from Eq. 4.7, the G_{ci-c} has a negative sign. Same observation can be made from a bode-diagram of the transfer function G^S_{ci-c} in Fig. 4.5, since the phase curve starts from 180°. This means that by using a conventional feedback control in the input-voltage loop, i.e. subtracting the measured value from the reference, would render the closed-loop system unstable. Therefore, in order to avoid this, the signs of measurement and reference values in the feedback loop have to be interchanged. When the signs are interchanged, the phase and gain margins have to evaluated from a zero degree line.

The minus sign in front of G^S_{ci-c} originates from the PWM shunt-unit, which is part of a boost converter [5]. The minus sign indicates also, that duty-ratio has to

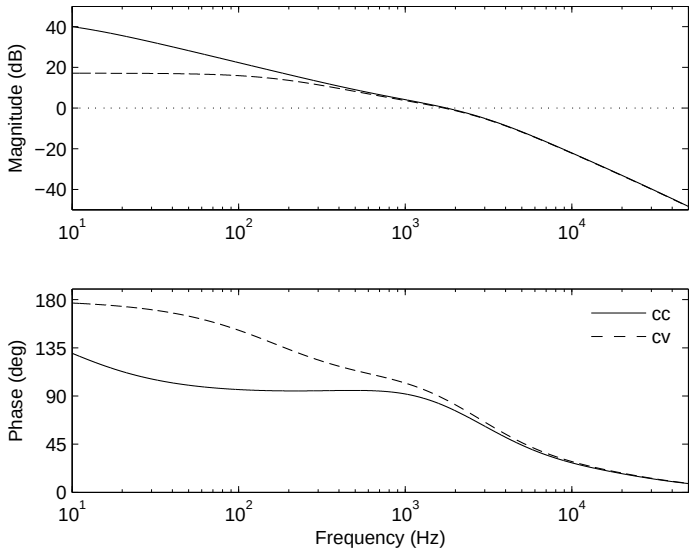

Figure 4.5. A bode-diagram of G^S_{ci-c} in CC and CV operation points with a 100μF input-capacitor.

be decreased in order to increase the input-voltage.

Furthermore, by studying the frequency response in Fig. 4.5 one can see, that the closed inductor-current loop eliminates the resonance between inductor and input-capacitor i.e. there is no peaking in gain and no phase drop at respective frequency.

The input-voltage controller sets the PVG operation point and gets its set-value from a MPP-tracker in a real world system. This means, that the input-voltage controller should at least be an I-controller (i.e. $\frac{K}{s}$), so that there would not be any steady-state error and the operation point would be set accurately by the control. However, using only the I-controller would result in a borderline unstable closed-loop system at CC operation point i.e. very low phase margin, which means that a PI-controller must be used.

By selecting a PI-controller:

$$G_{cv} = \frac{K_v(1 + \frac{s}{w_{z1}})}{s(1 + \frac{s}{w_{p1}})}, \tag{4.9}$$

where $w_{z1} = 2\pi * 30$, $w_{p1} = 2\pi * 4000$ and $K_v = 10^{\frac{35}{20}} \approx 56.2$, the loop gain $G^S_{ci-c}G_{cv}$ becomes as presented in Fig. 4.6.

With this controller, the input-voltage loop is stable with a phase margin of about 110° at CV operation point, and crossover frequency (bandwidth) of about 346Hz according to the figure. At CC operation point the phase margin and bandwidth are 85° and 413Hz, respectively. The outer control loop is approximately 10 times slower than the inner control loop, as it was required.

The closed input-voltage loop control block diagrams are presented in Figs. 4.7

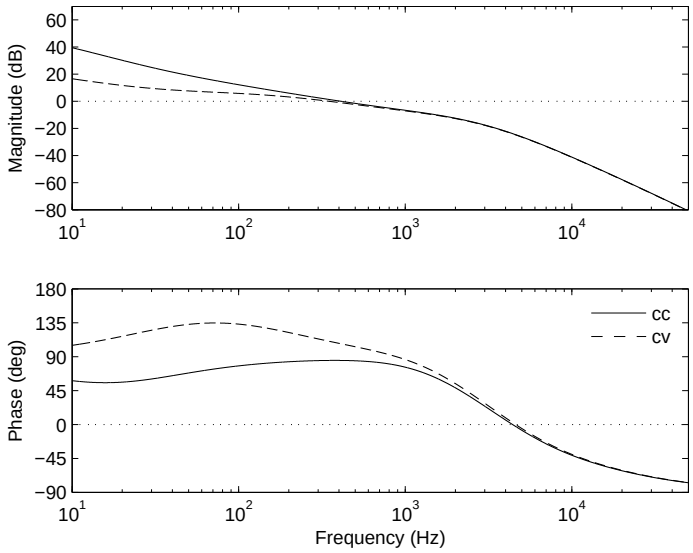

Figure 4.6. A bode-diagram of the input-voltage loop in CC and CV operation points with a 100μF input-capacitor.

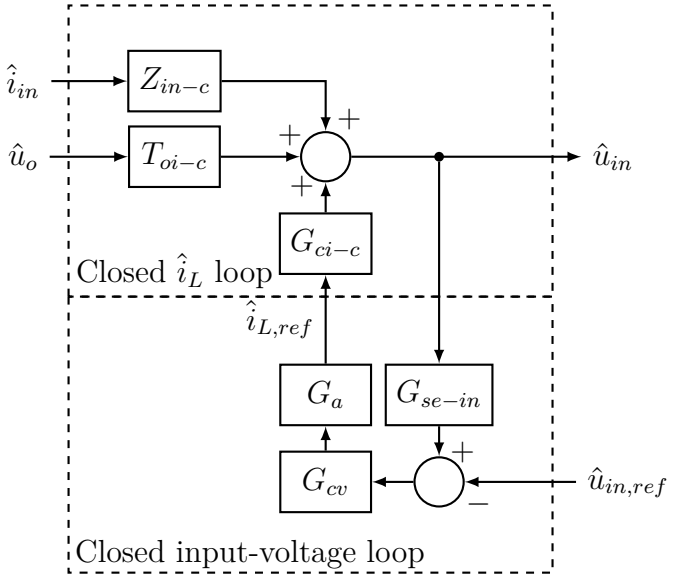

Figure 4.7. A control block diagram for solving the input-related closed voltage-loop transfer functions.

and 4.8. The former illustrates the solution for the input-voltage, and the latter for the output-current. The closed voltage-loop transfer functions can be solved, and the source-effect added, similarly as it was done for the current-loop in the preceding section.

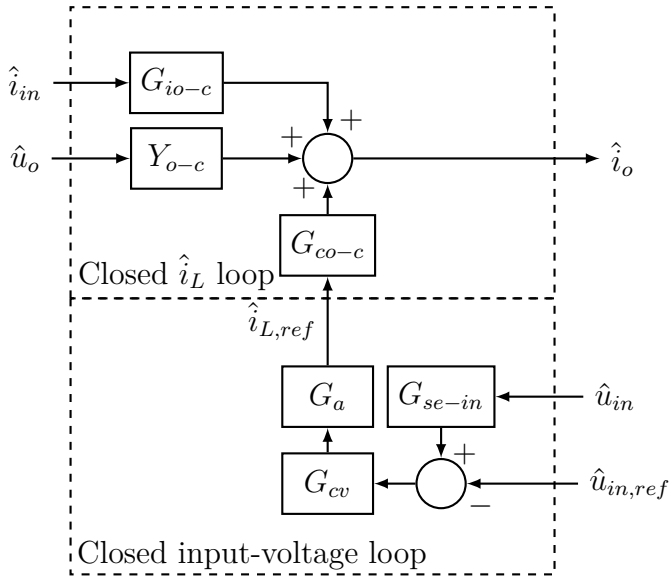

Figure 4.8. A control block diagram for solving the output-related closed voltage-loop transfer functions.

The input-related closed voltage-loop transfer functions are:

$$\begin{aligned} Z_{in-cc} &= \frac{Z_{in-c}}{1 - L_{cv}} \\ T_{oi-cc} &= \frac{T_{oi-c}}{1 - L_{cv}} \\ G_{ci-cc} &= -\frac{L_{cv}}{(1 - L_{cv})G_{se-in}}, \end{aligned} \tag{4.10}$$

where $L_{cv} = G_{se-in}G_{ci-c}G_aG_{cv}$, and the output-related closed voltage-loop transfer functions are:

$$\begin{aligned} G_{io-cc} &= G_{io-c} + \frac{K_{cv}Z_{in-c}}{1 - L_{cv}} \\ Y_{o-cc} &= Y_{o-c} + \frac{K_{cv}T_{oi-c}}{1 - L_{cv}} \\ G_{co-cc} &= -\frac{K_{cv}}{G_{se-in}(1 - L_{cv})}, \end{aligned} \tag{4.11}$$

where $K_{cv} = G_{se-in}G_{cv}G_aG_{co-c}$. The transfer function G_{se-in} describes dynamics related to the sensing of the input-voltage. G_{se-in} was set to one '1' during the control design, because of the same reasons discussed in the previous chapter. Now, that the voltage-controller has been added, the system input-variables are: $\hat{i}_{in}$,$\hat{u}_o$ and $\hat{u}_{in,ref}$.

5. MEASUREMENTS

A prototype converter was built in order to verify the theoretical findings. Measurement setup consisted of an Agilent E4360A solar array simulator (SAS) as a source and a load of two series connected 12.8V batteries in parallel with a Chroma 63103A electronic load configured as a current sink. The control was implemented with a Texas instruments' eZdsp TMS320F28335 development platform. The SAS in question is known to emulate the dynamic properties of a real PV generator as shown in [11]. The SAS was configured to correspond with the properties of a Raloss SR30-36 solar panel in weather conditions similar to the case in Fig. 2.9, which were $I_{sc} =$ 1.005A, $U_{oc} = 19.56$V and $I_{mpp}, U_{mpp} = 0.92$A, 16V, respectively. The measurements were made in the selected CC and CV operation points, which were given in Table 2.2.

5.1 Prototype Converter

The schematics of a prototype converter are presented in Figs. B.1-B.5. The first figure represents the power-stage, which was designed in chapter 3, the 2nd and 3rd figures represent the measurement circuits, and the last two figures represent the driver and the voltage-regulator circuits, respectively.

The purpose of the measurement circuits is to scale the measured values to an acceptable level for the ad - converter of the DSP, as well as, to provide low-pass filtering. A differential amplifier circuit configuration was used in both of the measurement circuits. The required duty-ratio is calculated on the DSP according to measured values and the controller parameters, and a square-wave signal having the calculated duty-ratio is outputted to the PWM-input of the gate driver circuit. The 10V supply voltage for the gate driver was provided with a laboratory power supply.

5.2 Measurement Results

Impedances of the designed inductor and both of the capacitors were measured in order to determine the real values of the converter model parameters. Also, the output-impedance of the SAS was measured, which is presented in Fig. A.4. These measurements were done in order to get as good match as possible between the measured and theoretical closed-loop frequency responses. The closed-loop transfer functions were measured in CC and CV operation points with the cascade controller

attached. Also, input-voltage controller response to a reference-value step-change was measured in both operation regions. The frequency responses were measured with a Venable Instruments' frequency response analyzer model 3120, and step-response measurements were made with a LeCroy 104MXi oscilloscope.

It was assumed, that the inductance of the inductor remains constant in every operation point, since the current through it is fairly small in this application. Furthermore, it was assumed that the characteristics of the capacitors remain constant while the operation point is changed.

Measured and predicted frequency responses of the input-voltage loop are presented in Fig. 5.1. The loop gains in the figure were calculated from the measured reference to input-voltage i.e. $G^S_{ci-cc} = \frac{\hat{u}_{pv}}{\hat{u}_{pv,ref}}$ transfer functions with a following equation:

$$L_{cv} = \frac{-G^S_{ci-cc}}{1 - G^S_{ci-cc}}. \tag{5.1}$$

The measured output impedance of the SAS was used as a source effect when the predicted frequency responses in the figure were calculated.

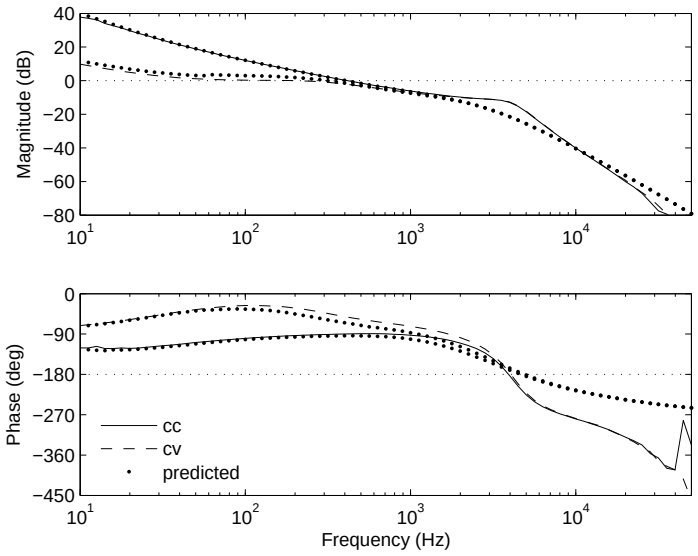

Figure 5.1. Measured frequency response of input-voltage loop and the model predictions.

The measured (solid line in the CC region, dashed line in the CV region) and predicted (dots) frequency responses have fairly high correlation until a frequency of about 1kHz, where they start to deviate drastically. This difference occurs, because the dynamic model of the system developed in earlier chapters does not take the sampling delay of the DSP nor the low-pass filtering action of the measurement circuits into account.

Adding a sampling delay of one switching cycle T_s i.e. e^{-sT_s} to the inductor-

current sensing transfer function R_{sL} and the input-voltage sensing transfer function G_{se-in}, as well as, using the actual transfer functions of the corresponding measurement circuits (Figures B.2 and B.3) results in a very good match between the measured and predicted transfer functions, as it can be seen from Fig. 5.2. It seems that the system model corresponds now fairly accurately with the actual device.

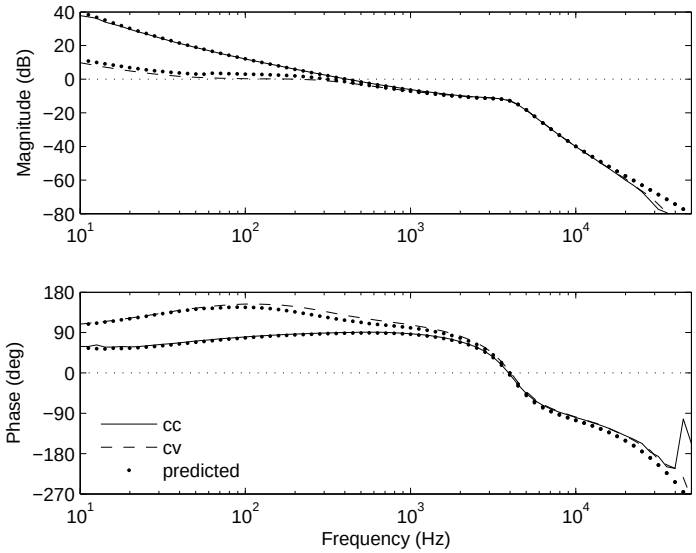

Figure 5.2. Measured and predicted frequency responses of the input-voltage loop when the effect of the time-delay and the measurement circuit gain is included into the prediction.

The inductor-current loop gain L_c^S is redrawn in Fig. A.5 with the effect of the delay and the measurement circuit added into it. As it can be seen, the time-delay has reduced the phase margin to 25° and the gain margin to 7.2dB, resulting in slightly worse performance than what was defined acceptable. Also, the time-delay changes the shape of the closed-loop transfer function G_{ci-c}^S reducing the gain margin of the voltage-loop. However, the performance of both loops can be enhanced with a proper controller retuning.

From Fig. 5.2 one can see that the measured voltage-loop crossover frequency at CV operation point is 200Hz with a phase margin of 148° and a gain margin of 13dB. At CC operation point these values are 400Hz, 90° and 13dB, respectively.

Measured time-domain step-responses are presented in figures 5.3 and 5.4. In the figures, the undermost curve represents the measured input-voltage, and above it is the reference step-signal. The thicker (more noisier) curve is the measured output-current, and the upmost is output-voltage. Fig. 5.3 represents the result when the input-voltage controller reference is stepped from 16V to 17V i.e. in CV region, and similarly Fig. 5.4 illustrates the result in CC region (from 12V to 13V).

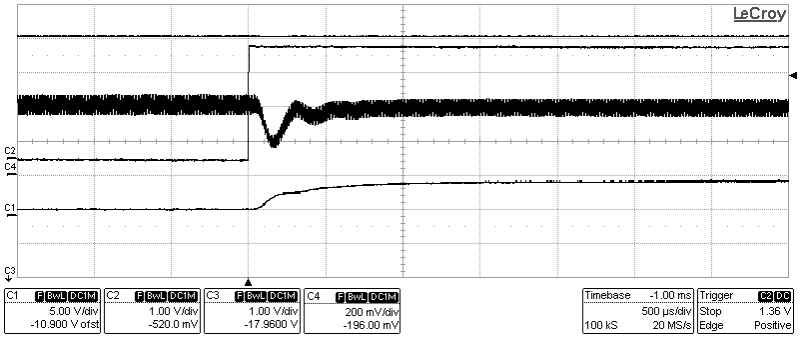

Figure 5.3. Input-voltage controller reference step-change in CV region (16V to 17V).

As it can be seen, the control seems to set the selected operation point in both regions i.e. the system works. However, the responses seem overdamped especially in the CV region. This was expected because the dc gain at CV operation point is quite low, the crossover frequency is low, and the phase margin is very large. In CC region the response is fairly good setting the operation point in just over 1ms. Also, the control delay can be observed from the figures; the input-voltage does not start to rise immediately after the reference has been stepped.

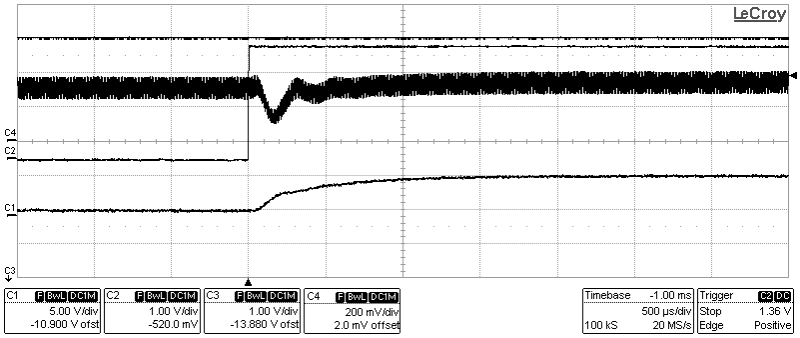

Figure 5.4. Input-voltage controller reference step-change in CC region (12V to 13V).

The measured converter output-impedance ($Z^S_{o-cc} = \frac{1}{Y^S_{o-cc}}$) under cascade control is presented in Fig. 5.5 with model predictions. As it can be seen, the predicted and measured frequency responses have very high correlation. The low-frequency value for the converter output impedance is therefore:

$$Z^S_{o-cc}(s=0) = \frac{U_o + U_d + (r_d - r_{sw})I_{in}}{D' I_{in}}, \tag{5.2}$$

which is exactly same as it is for the input-voltage controlled boost-converter [5]. However, the results also show that the device output-impedance does not depend

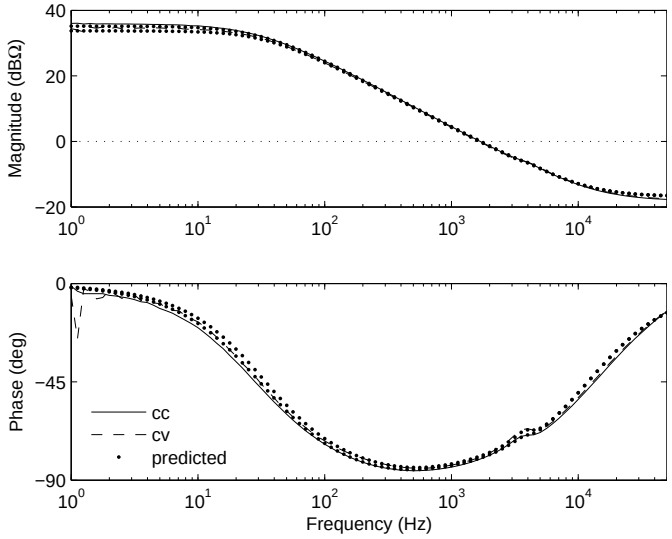

Figure 5.5. The measured system output-impedance.

on the dynamic resistance r_{pv}. The output impedance is only dependent on the operation point voltage and current assuming that other parameters remain constant.

It can be deduced from these results that the boost-power-stage converter under cascaded inductor-current and input-voltage control blocks the PVG from affecting the downstream converters (e.g. grid-connected inverter in double-stage conversion scheme) similarly as the input-voltage controlled converter does. However, the cascade controlled converter seems to eliminate the effect of the dynamic resistance in the entire frequency range. Furthermore, if the MPP-tracking is utilized, the control forces the downstream converters to operate in conditions similar to the MPP due to constant power nature of the converter. [5] [37]

6. CONCLUSIONS

A boost-power-stage converter with a cascaded inductor-current and input-voltage control was designed in this thesis for photovoltaic generator application. The current controller got its set-value from the voltage controller, thus the current control loop was inside the voltage loop. In addition, a prototype converter was built based on the maximum values of the selected example PV module output and its dynamics, as well as, transient response with a cascade control on were measured.

The measurement results verify that the modelling procedure described in this thesis yields a correct dynamic model for the cascade controlled device. However, the predicted and measured output-impedances had a 180 degree phase difference. It was not found within the time limit what caused this difference. It was assumed that the measurement result was correct indicating a positive output-impedance. The analytical low frequency solution for the output-impedance showed that it was independent on the dynamic resistance of the PVG.

Very limited amount of information was found from the literature regarding cascade control. It was assumed in this thesis, that both control loops should be stable, and that the current loop bandwidth should be at least five times the voltage loop bandwidth in order to obtain a robust control. Two PI-controllers were sufficient for meeting these requirements. It was found, that eventhough the closed current loop eliminated the effect of resonance from the voltage loop, the performance of the control did not improve significantly compared to conventional input-voltage control due to flat gain response of the voltage loop, and hence, slow transient response. The effect of sampling delay should be addressed if the control system is implemented digitally, since it reduces the performance of both control loops.

Cascade control blocks the PVG from affecting the downstream converters e.g. in a double-stage conversion scheme, and if a MPP-tracking is utilized it forces them to operate in MPP-like conditions. This same behaviour occurs in a convential input-voltage controlled boost-power-stage converter. Also, the load-side current sensing results in higher losses in a high power system and higher costs due to an extra measurement circuit compared to the convential control method. Thus, the evidence presented in this thesis suggests that the cascade control is not feasible. More research is needed, however, on different current sensing techniques, as well as, more advanced control strategies and design methods.

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A. APPENDIX

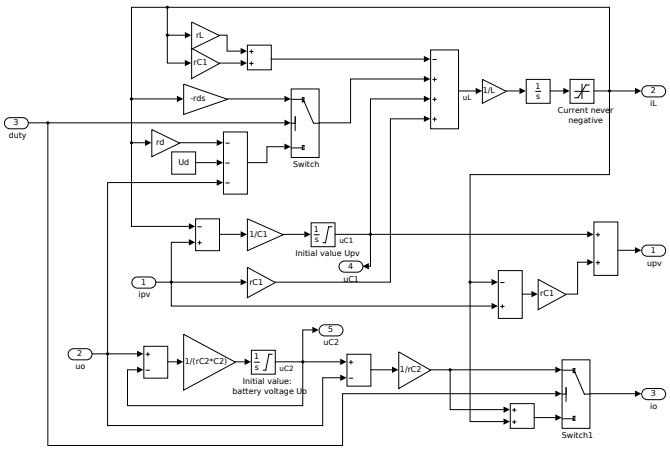

Figure A.1. Simulink model of a dc-dc CF-CO boost-power-stage converter.

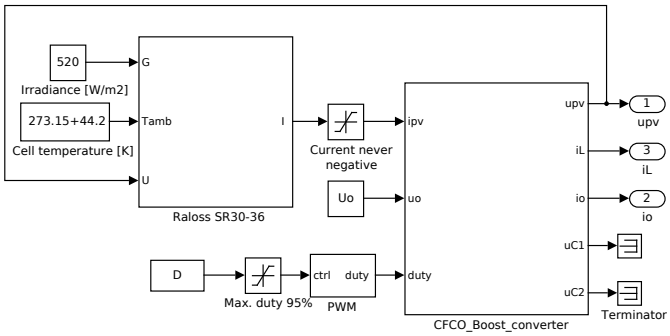

Figure A.2. Simulink model of a dc-dc CF-CO boost-power-stage converter under DDR control and the PVG model.

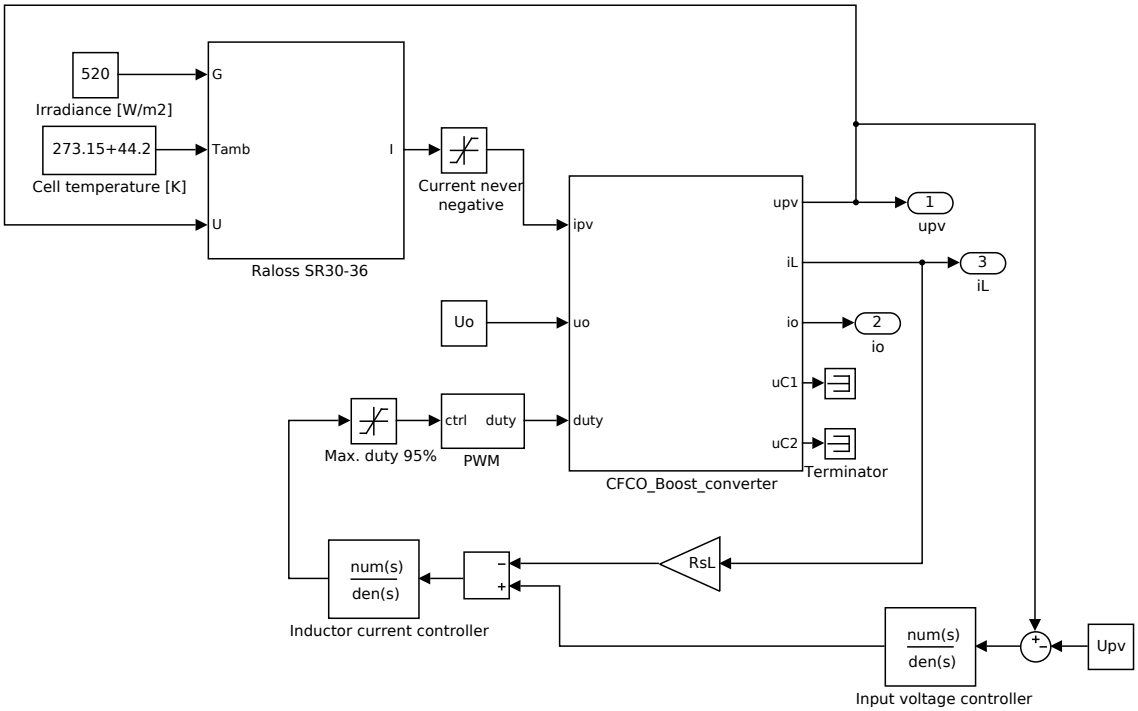

Figure A.3. Simulink model of a dc/dc CF-CO boost converter under cascade control and the PVG model.

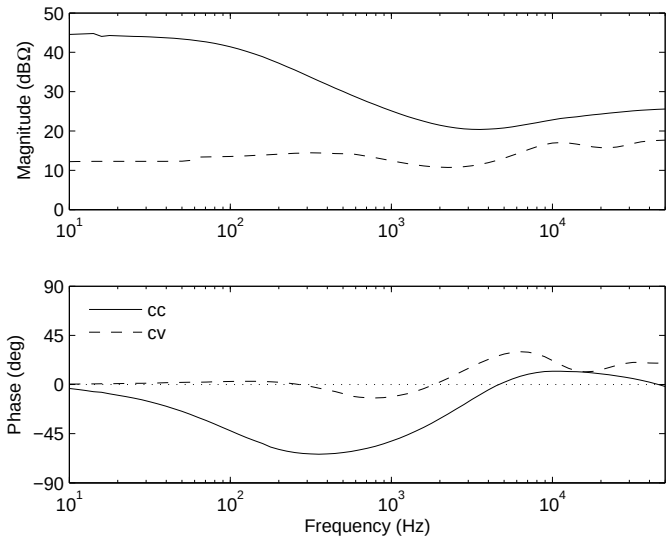

Figure A.4. Measured output-impedance of the SAS in CC and CV operation points.

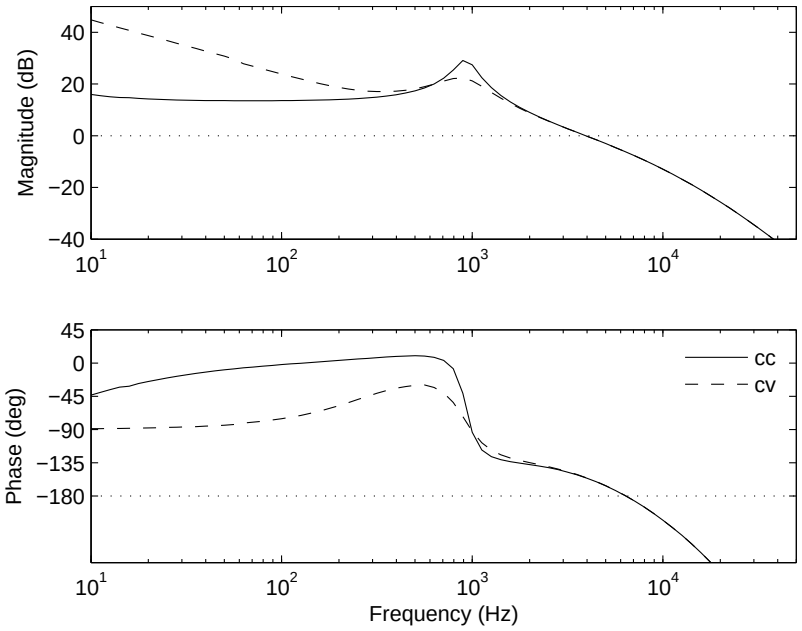

Figure A.5. Frequency response of the inductor-current loop in CC and CV operation points when the time delay and the frequency response of the inductor-current measurement circuit are taken into account.

B. SCHEMATICS OF THE PROTOTYPE CONVERTER

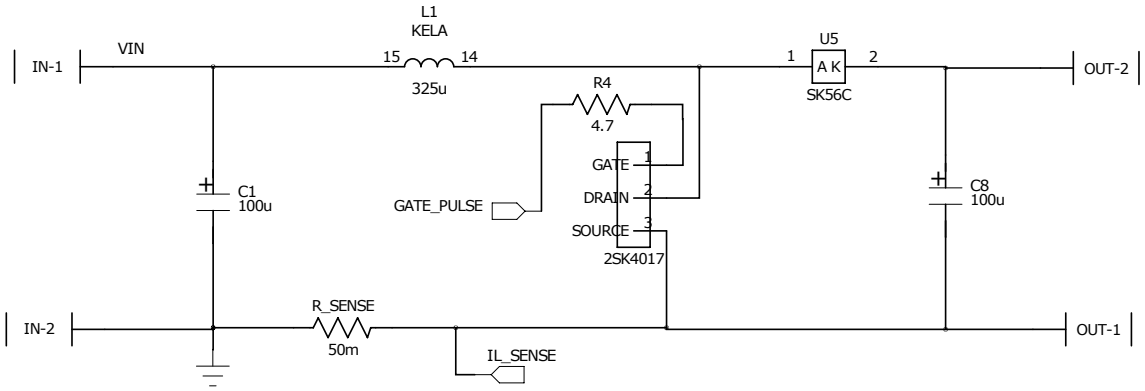

Figure B.1. Power-stage of the converter.

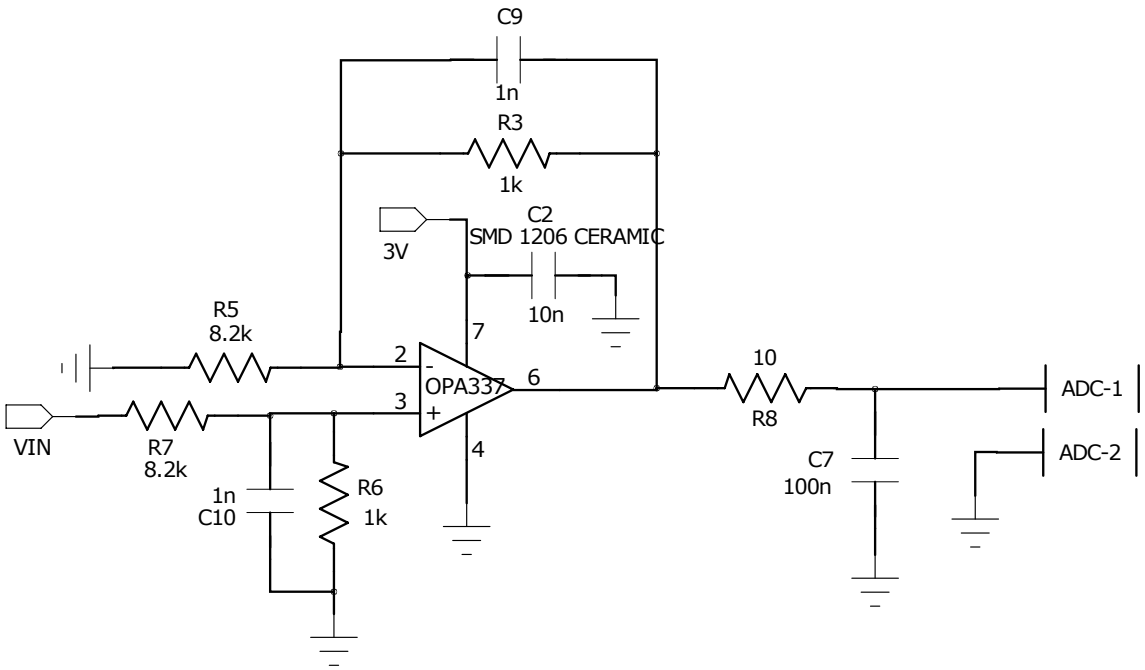

Figure B.2. Input-voltage measurement circuit.

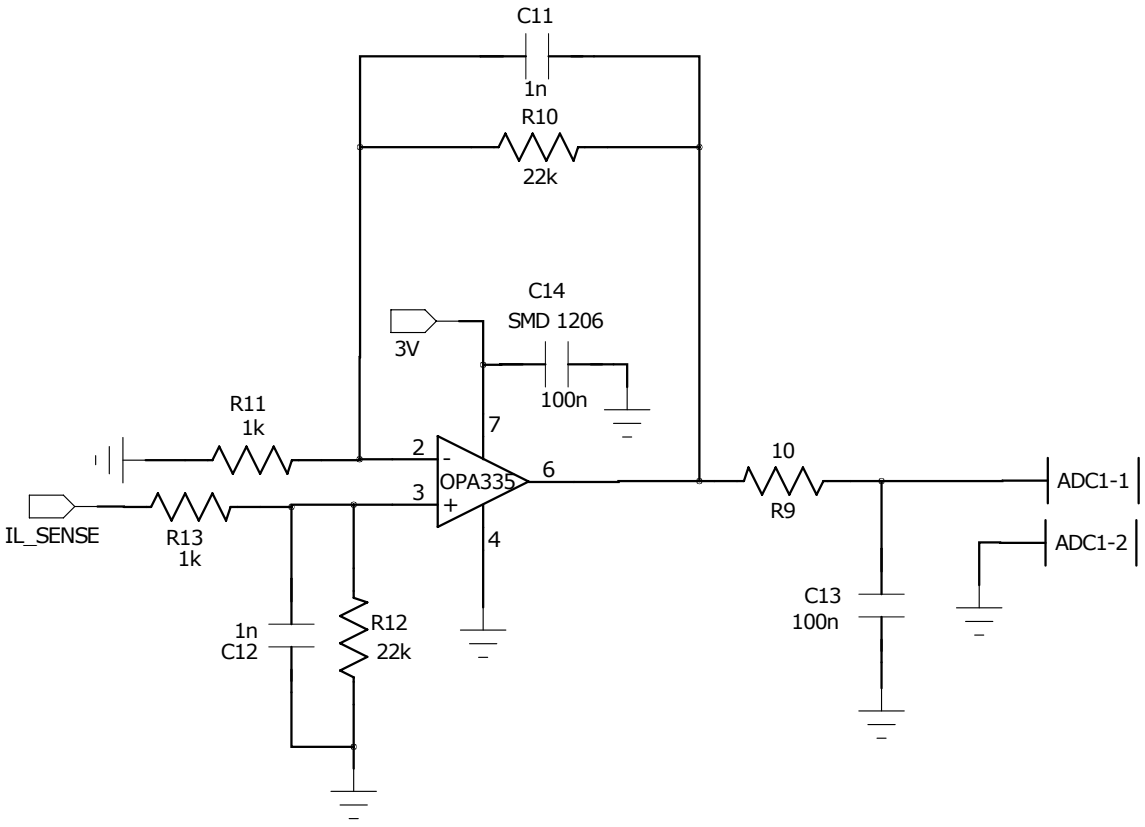

Figure B.3. Inductor-current measurement circuit.

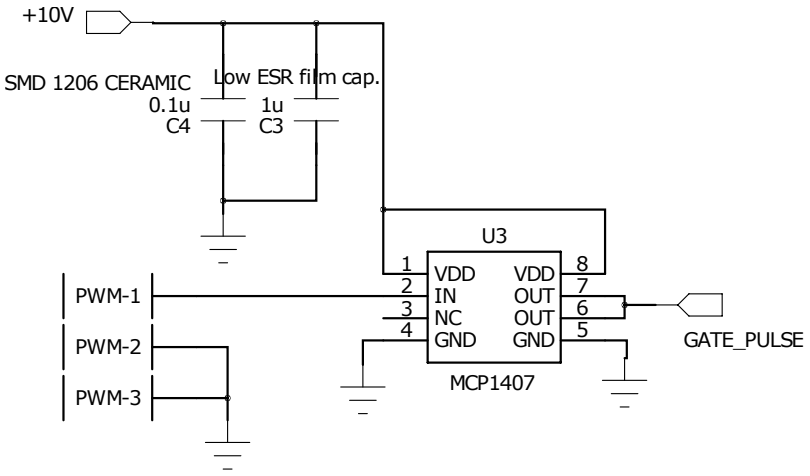

Figure B.4. Gate driver circuit.

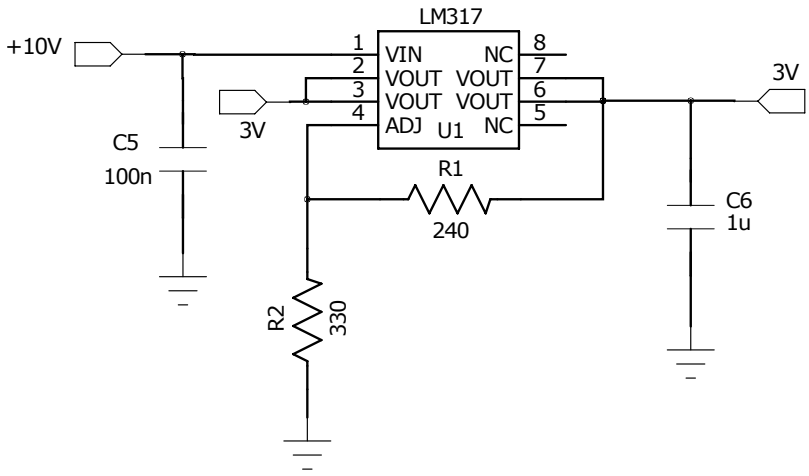

Figure B.5. Voltage-regulator.