TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

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HIGH SPEED FULLY MONOLITHIC SELF-TRIGGERED DC-DC BUCK CONVERTER

Master of Science Thesis

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DC-DC-muuntimien sisällyttäminen CMOS-prosessiin sisältää useita haasteita, joista esimerkkeinä matalat transistoreiden läpilyöntijännitteet ja pienen Q-arvon suurikokoiset piille integroidut kondensaattorit ja kelat. Perinteisesti MOS-transistoreiden matalat läpilyöntijännitteet on ratkaistu kytkemällä useita transistoreita kaskadikytkentään pääteasteessa.

Jännitettä laskeva DC-DC-muunnin koostuu puolisillasta, jossa yläpuolen PMOS-kytkinelementtiä ja alapuolen NMOS-kytkinelementtiä ohjataan päälle ja pois signaaleilla, joiden käyttöjakso määrittää muuntimen ulostulojännitteen. Ohjaussignaalit eivät saa kytkeä transistoreita samaan aikaan päälle oikosulkutilanteiden välttämiseksi, joten ohjaussignaalien välillä tulee olla lyhyt kuollut aika. Puolisillan PMOS- tai NMOS-kytkinelementtien matalien läpilyöntijännitteiden ratkaisemiseksi voidaan kytkeä useita transistoreita kaskadikytkentään, joka lisää haasteita yksittäisten transistorien ohjaamiseen, sillä niiden ohjausjännitteet toimivat eri jännitealueilla. Tämä ongelma voidaan ratkaista tasomuuntimilla, jotka muuntavat ohjaussignaaleita jännitealueiden välillä. Tasomuuntimien käyttö voi kuitenkin huonontaa DC-DC-muuntimen kokonaishyötysuhdetta ajastusviiveiden ja tehonkulutuksen kautta.

Tasomuuntimissa esiintyvien ongelmien ohittamiseksi tässä työssä esitellään itseliipaiseva laskeva DC-DC-muunnin. Tässä muuntimessa puolisillan yläpuolen kytkimen ohjaussignaali tuotetaan induktiivisella takaisinkytkennällä muuntimen ulostulosta. Induktiivisen takaisinkytkennän käyttö poistaa tasomuuntimien tarpeen yläpuolen kytkinelementin ohjauksessa, sekä on samanaikaisesti nopeavasteinen ja mahdollistaa muuttuvan kuolleen ajan ohjauksen ilman ylimääräisiä komponentteja. Ulostulojännitteen ohjaus toteutetaan muuttamalla alapuolen kytkinelementin ohjaussignaalin käyttöjaksoa. Ehdotetun DC-DC-muuntimen simulointi on tehty Cadencen 45 nanometrin CMOS General Process Design Kit (GPDK) -työkalulla, joka antaa itseliipaisevan DC-DC-muuntimen hyötysuhteeksi 64.25 %. Tätä tulosta verrataan ilman kuollutta aikaa käytettävän DC-DC-muuntimen simulaatiotuloksiin, jotka antavat hyötysuhteeksi sen 63.21 %, jossa ei ole mukana tasomuuntimissa esiintyvien viiveiden ja tehonkulutuksen vaikutuksia. Itseliipaiseva DC-DC-muunnin tuottaa 1.5V ± 20mV

ulostulojännitteen 100mA ± 3mA kuormavirralla 3V-3.6V sisäänmenojännitteestä 360 MHz kytkentätaajuudella. Todellisen käyttäymisen mallintamiseksi työssä on totetuttu DC-DC-muuntimen piirileiska, josta lopulliset simulaatiot voidaan suorittaa piirin parasiittisten komponenttien kanssa. DC-DC-muunnin on rakennettu kokonaisuudessaan 1.73 x 1.62 mm piialueelle kytkinkomponenttien, muuntajan, ohituskondensaattorin sekä juotospisteiden kanssa.

ABSTRACT

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The integration of DC-DC converter in standard CMOS process faces challenges from the low transistor breakdown voltages, poor quality factor and large size on-chip capacitors and inductors. The standard solution to deal with the problem of MOS transistor's low breakdown voltage is using cascode configuration in the output stage.

High-side PMOS and low-side NMOS power transistors in on-chip buck converter are switched ON and OFF with non-overlapping driving signals whose duty-cycle regulate the output voltage of converter. The non-overlapping driving signals are required to avoid short-circuit losses through power transistors. By using the cascode configuration, driving signals for high-side PMOS and low-side NMOS power switching transistors operate in different voltage domains. To overcome this problem, the voltage level shifters are needed to transfer driving signals between two voltage domains. However, associated power losses and additional timing delays in conventional level shifters may deteriorate the overall efficiency of converter

In order to avoid the losses and timing delays associated with the level shifters, a self-triggered buck converter is proposed in this work. The high-side driving signal is generated from the converter output via inductive feedback. The inductive feedback eliminates the required level shifters needed for transferring the driving signal to high-side power transistor. The inductive feedback has fast response and provides adaptive dead-time that avoids short circuit losses with no additional hardware. Output voltage regulation is realized by controlling the duty-cycle of the signal switching the low-side NMOS transistor. Simulations are done on Cadence 45nm CMOS General Process Design Kit(GPDK) and show that the efficiency of self-triggered converter (64.25%) is better than the efficiency of a hard-switching buck converter(63.21%), even when the level shifter losses and delays are not taken into account. The converter generate output voltage ~1.5V ± 20mV and average load current 100mA ± 3mA from 3V-3.6V input at a switching frequency of 360MHz. In order to closely match real circuit behavior, layout is made and final simulations are carried out with extracted layout and PCB Parasitics. The converter is fully integrated with 1.73×1.62[mm×mm] area on silicon including power stage, transformer, decoupling capacitors and pads.

PREFACE

The research work presented in this thesis was done at the RFIC Laboratory, Department of Electronics and Communications Engineering, Tampere University of Technology (TUT). It is the continuation of a project with our industry partner Infineon Technology AG, who financially supported the research developments.

During the one-year period, I have received a lot of help from my supervisor and colleagues in our group. Foremost, I would like to thank Prof. Nikolay T. Tchamov for providing me the great opportunity to work in his research group. I also would like to thank my direct consultants Jani Järvenhaara and Faizan-Ul-Haq for his unconditional help. Meanwhile, I want to thank all other team members of RFIC Laboratory for the excellent work environment we have created together.

Finally yet importantly, I would like to thank my parents for their continuous support and inspiration, which have been the main source of motivation during my M.Sc. study.

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LIST OF FIGURES

CONTENTS

ABBREVIATIONS

DC-DC	Direct-Current to Direct-Current
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal-Oxide-Semiconductor
IC	Integrated Circuit
PWM	Pulse Width Modulation
t_{LH}	Dead Time at Low-to-High transition
t_{HL}	Dead Time at High-to-Low transition
ZVS	Zero Voltage Switching
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
VPCD	Virtuoso Passive Component Designer
LVS	Layout vs. Schematic
DRC	Design Rule Check
PCB	Printed Circuit Board
Esr	Effective series resistance

1 Introduction

The possibility to integrate multiple electronic blocks in standard CMOS processes has resulted in battery powered portable electronic systems. However, batteries have an inherent problem of variable output voltages. As performance of electronic blocks in integrated circuits is dependent on fixed supply voltage, using a variable output voltage of batteries directly as power supply of these circuits can change the performance level of these blocks. Furthermore, different electronic block may require different power supply voltages for proper operation. Therefore, to generate these different supply voltages from single battery source, electronic circuits called as Direct-Current-to-Direct-Current (DC-DC) converters are required. See Figure 1-1.

Among the battery technologies, lithium batteries are widely used as energy source for portable devices due to compact in size, high energy storage density and low self-discharging. However, the lithium battery provides unregulated voltage varies from 2.8V-4.2V [13]. In Figure 1-1, shows system architecture where several voltage converters generate the regulated supply voltages required by different electronic application blocks from this unregulated lithium battery input voltage.

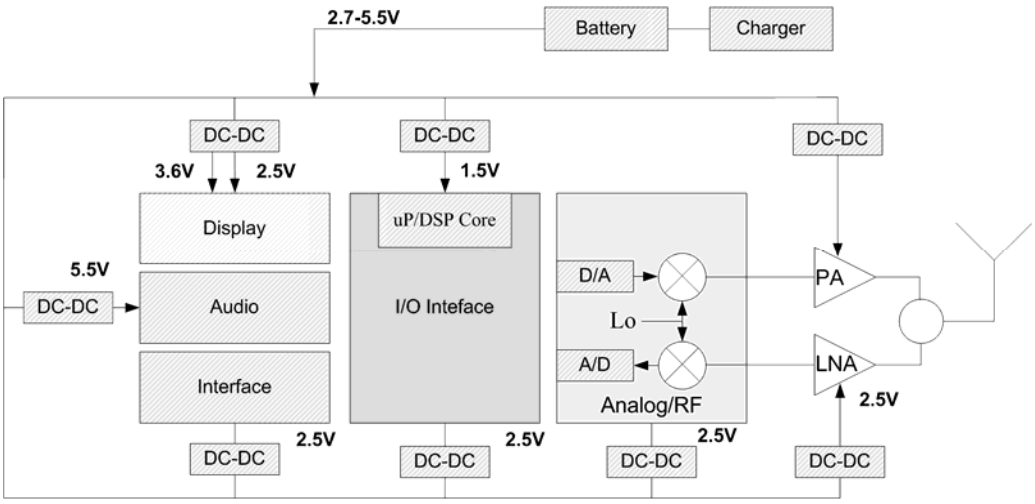

Figure 1-1: Battery operated applications with DC-DC Converters.

Standard CMOS Processes demands greater amounts of current at lower supply voltages from external battery source. For efficient delivery of power to advanced integrated circuits, board-level (PCB) voltages should be high. Distributing power at a higher voltage to the input pads of an integrated circuit reduces the supply current. At a reduced power supply current, resistive voltage drop and parasitic power dissipation of the off-chip power distribution network is reduced, thereby enhancing the energy efficiency and quality of the distributed voltage. Once the required energy reaches the

input pads of integrated circuit, a monolithic DC-DC converter can generate a lower supply voltage for particular application circuit.

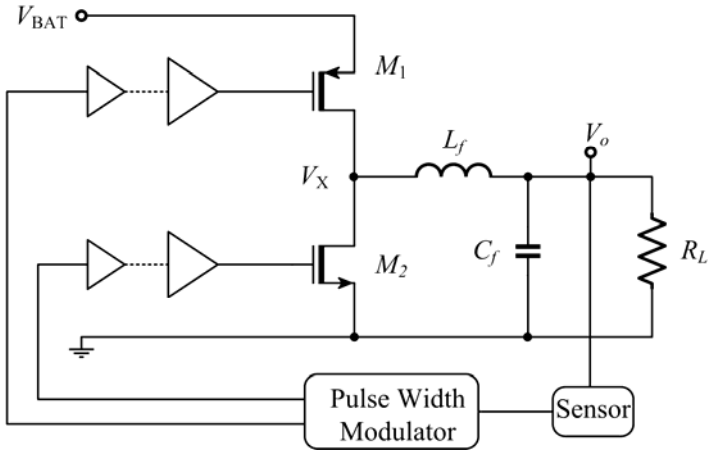

Figure 1-2: Off-chip standard buck converter

Due to advantages of high voltage power delivery on PCB and monolithic DC-DC conversion for standard CMOS process integrated circuits, leads to new challenges. The maximum battery voltage applies to the standard buck converter in Figure 1-2 is limited due to transistor's maximum gate-oxide breakdown voltage of standard CMOS processes. Therefore, standard switching DC–DC converter topology is not suitable for future high performance integrated circuits. To attain high voltage conversion ratio from monolithic DC-DC converter, cascoded transistor structure is appropriate [2]. Cascoded transistor structure shown in Figure 1-3(a) can operate at input voltage higher (V_{BAT}=2V_{max}) than maximum transistor allowed gate-oxide breakdown voltage (V_{max}).

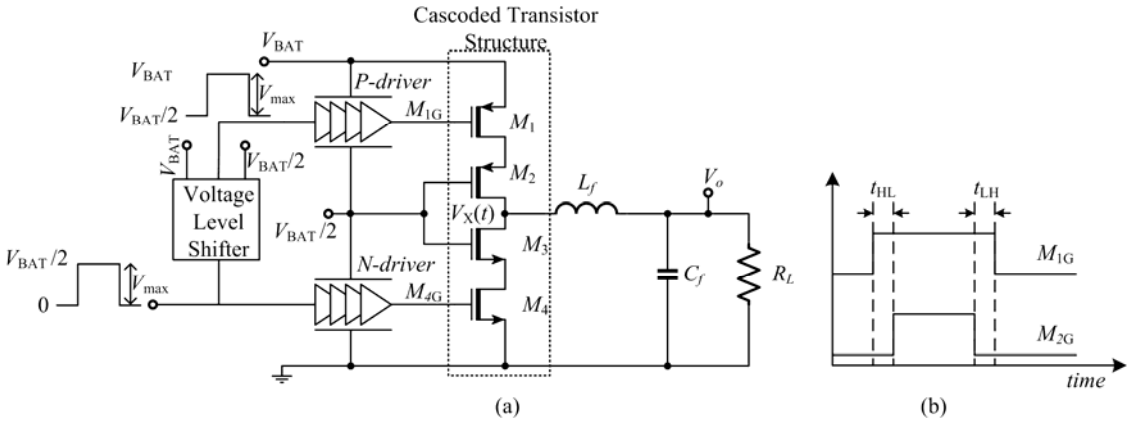

Figure 1-3: implementaion of buck converter with cascoded transistor structure

The P-driver and the N-driver form the switching signals M_{1G} and M_{4G} applied to the gates of M_1 and M_4 respectively. The waveforms of M_{1G} and M_{4G} are shown in Figure 1-3 (b), where t_{HL} and t_{LH} are intentionally introduced dead-times between the driving pulses, which assure no short-circuit currents through the transistor chain M_1–M_2–M_3–

M_4. However, switching signals M_{1G} and M_{4G} are operating in two different voltage domains. The transfer of switching signals between different voltage domains requires level shifters. By adding level shifter, we introduce additional power losses and delays in the switching signal that affect the efficiency of buck DC-DC converter.

The integration of buck DC-DC converter, however, imposes a challenge On-chip integration of inductors and capacitors are required for energy storage and output signal filtering. These integrated capacitors/inductors become impractical above certain values due to the tight area constraints required by integrated circuits. Another significant issue with integrated inductors is the poor quality factor that can degrade the efficiency of a DC-DC converter. The physical size, value and parasitic impedances of inductors and capacitors can reduce by increasing switching frequency of DC-DC converter. By increasing switching frequency, the converter efficiency decreased dramatically[2]. A reduction the switching losses can be achieved by using fast MOS devices and implementing Zero-Voltage Switching (ZVS) techniques. The ZVS technique requires tight control of the dead-times t_{HL} and t_{LH}, which should be adaptive in order to provide appropriate switching instant under load and input voltage variations.

Recent researches have tried to overcome some of the above technical limitations. New innovative techniques in [14], [15], [16], [17] are reported for integration of DC-DC converters for low voltage applications at high switching frequencies.

This thesis proposes a new technique for integrated buck converter. Which describe the issues related to voltage level shifter in standard buck converter and gave solution, how self-triggered buck converter topology eliminates the need of voltage level shifter and their related issues. In addition, the self-triggered converter has better efficiency than standard buck converter even we do not include the voltage level shifter losses.

The background theory and characteristics of synchronous DC-DC buck is presented in Chapter 2. Chapter 3 is dedicated on the operation of the proposed self-triggered converter. The converter design procedure and pre-layout simulation results are depicted in Chapter 4. Chapter 5 gives the layout design procedure of the proposed converter. Chapter 6 gives an example of measurement setup for the designed buck converter as well as the post-layout simulation results and compare the Self-triggered converter results with standard buck converter in hard and soft switching mode. Chapter 7 concludes the thesis.

2 Background

As explained in chapter one, devices requiring certain degree of user mobility e.g. cell phones, laptops etc. are normally operated by batteries. Most of the devices used Li-ion batteries as a power source having nominal output voltages of 3.6V [1]. However, the electronics circuits inside the portable devices need different supply voltages e.g. 1.5V, 1.8V, 4.2V, 5V etc. these different voltages need to be generated from single battery. See Figure 1-1 [6]. Furthermore, variable battery output voltages under charged/discharged conditions can change the overall performance of electronic block. Therefore, portable electronic circuits must posses a circuit that converts variable battery voltage into constant voltages for different power domains inside the IC. Electronic circuits that perform this DC voltage conversion are known as DC-DC converters.

There are two major types of DC-DC converters, Linear and Switched-mode (Inductive and Capacitive) converter. Switching DC-DC converters are widely used among these topologies due to high efficiency, good voltage regulation and ability to provide high load currents. A switching DC–DC converter that generates a higher output supply voltage compared to the input supply voltage is knows as boost converter. Alternatively, a switching DC–DC converter that generates a smaller output supply voltage as compared to the input supply voltage is known as buck converter. Before going into details of converter types let us first analyze the requirements and characteristics of converter. The DC-DC converter characteristics are divided into two main categories: static and the dynamic characteristics [6].

2.1 Static Characteristics

Static characteristics are mainly describing the nature of converter in steady-state regime. This is related to the converter stage itself and to the control technique used by the converter [6]. The main characteristics are:

Voltage Conversion Ratio: is the ratio between output voltage and the input voltage of the converter stage.

$$VCR = \frac{Vout}{Vin} \qquad (2\text{-}1)$$

For voltage conversion ratio *VCR* is greater than one, DC-DC converter is known as step-up converter. While for *VCR,* less than one, DC-DC converter is called as step-down converter.

Noise: Ideally, voltage source has zero output impedance and provides the noise free constant DC supply regardless of output current. However, practically voltage source has some output impedance and parasitic components from source to load. These parasitic components also add to output impedance of voltage source as shown in Figure 2-1. When the varying current flows through the RLC lumped component model of interconnection between voltage source and load then voltage source turned into DC+AC source. The additional AC is known as input noise. Usually, decoupling capacitors are used to reduce the input noise.

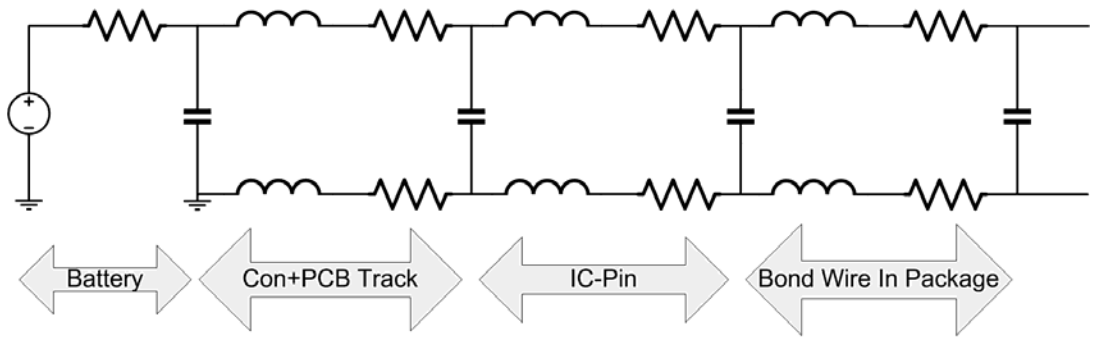

Figure 2-1: Lumped model of the physical connection between battery and chip mounted on PCB.

Efficiency η A primary factor that determines the quality of a DC–DC converter is the output voltage regulation i.e. the stability of the output voltage over a wide range of input voltages and load currents. The output voltage drop and peak-to-peak output voltage ripple under changing conditions of the load current and input voltage characterizes the output stability of voltage regulator. Another important factor that determines the quality of a DC-DC converter is the energy efficiency of the voltage conversion process. The parasitic impedances of a DC–DC converter dissipate a specific amount of energy in order to generate a supply voltage. The choice of DC–DC conversion topology and related circuit techniques for a specific application is critical to the energy efficiency of the voltage conversion process. The energy efficiency of DC–DC converter is:

$$\eta = \frac{P_{out}}{P_{in}} \qquad (2\text{-}2)$$

Where *Pout* is output power supplied to the load and *Pin* is total supplied power. The power consumed by parasitic components in the voltage Converter is:

$$P_{lost} = pin - pout = pout(\frac{1}{\eta} - 1) \qquad (2\text{-}3)$$

2.2 Dynamic Characteristics

The dynamic characteristics are describing the nature of converter stage as by the control method of the DC-DC converter. The most fundamentals characteristics are as follow:

Line Regulation is a measure of the variation in the output voltage by changing the input voltage of converter. The variation is not necessarily linear over the whole input range [6] therefore line regulation can be calculated at two different input voltages (minimum and maximum input) and output voltages according to input and normalize this variation with respect to line variation describe as:

$$\text{Line Regulation} = \frac{V_{out,in2} - V_{out,in1}}{V_{in2} - V_{in1}} \times 100\% \qquad (2\text{-}4)$$

Load Regulation is a measure of the variation in output voltage at different output currents. The output voltage variation is not necessarily linear over the whole load range [6]. Therefore, output variation can be calculated for the maximum and minimum load current as follow:

$$\text{Load Regulation} = \frac{V_{out,I_2} - V_{out,I_1}}{I_2 - I_1} \times 100\% \qquad (2\text{-}5)$$

Bandwidth: of the DC-DC converter describes how fast is the transient response of the converter with changes in load, line and control-signal. This feature can be tested by changing load from minimum to maximum with a predefined rise/fall time [6].

Overshoot and Undershoot: is the deviation from the nominal output voltage due to transient in load-line or control. It should be exactly specified under which circumstances and operating points the overshoot and undershoot occurs.

2.3 DC-DC Converter Types

Several methods exist to achieve DC-DC voltage conversion from kilowatt range to few watts. Each topology having its own advantages and disadvantages. Main interest of this work is battery operated monolithic high speed switching buck DC-DC converter. The discussion on converter topologies limited to Integrated DC-DC converters in the following sections. The main two topologies are Linear and switched-mode converters.

Linear Voltage Converter

Linear voltage converters are popular due to simple structure and well suited for monolithic integration due to simple in nature. Linear DC-DC converters operate on the principle of resistive voltage division. The operation of simple linear converter is illustrated in Figure 2-2(a). A variable resistor R_{var} lowering V_{in} to V_{out} and I_{Load} is equal to current drawn by the primary source V_{in}. The maximum efficiency η_{max} attained from Ideal linear voltage regulator is,

$$\eta_{\max} = \frac{V_{out}}{V_{in}} \qquad (2\text{-}6)$$

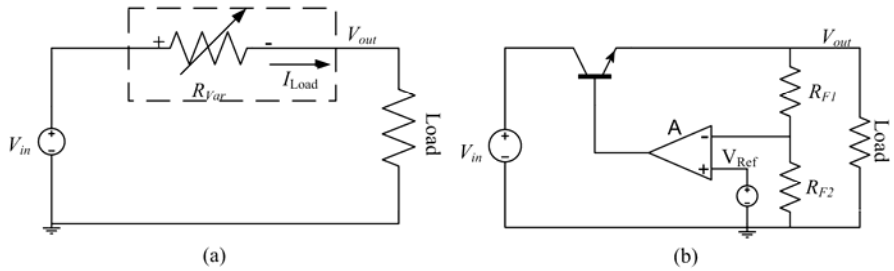

Figure 2-2: (a) Model of Linear voltage regulator. (b). A feedback varies the voltage at the gate of the series transistor (which is act as variable resistor) by comparing the output voltage V_{out} with the reference voltage V_{Ref}.

Therefore, the linear converter can offer high efficiency if voltage conversion ratio is small. For the high conversion ratio, the efficiency becomes small. Therefore, the switched-mode DC-DC converter topologies emerge, where high conversion ratio needed [1].

Charge-Pump DC-DC converter

Charge-Pump or switched-capacitor converter can generate different DC output voltage of different magnitude and/or opposite polarity compared to input voltage supply [11]. On-chip charge-pump converters are widely used in supply analog mixed signal circuits, non-volatile flash memories [11].

a) Charge Transfer

Charge-Pump converter utilizes capacitor to transfer charge from the input to the output of the converter. Figure 2-3 demonstrates the concept of charge-pump converter that divide the input voltage by two. Both structures contain equal amount of charge. The first state store charge is in series while second one in parallel connected capacitors.

In charge-pump converter energy transfer from input to the load by means of single capacitor is modeled as charging capacitor by supply voltage through resistor in Figure 2-4. The process of charging the capacitor is described by the following equation:

$$V_{in} + RC\frac{dV_c}{dt} + V_c = 0 \qquad (2\text{-}7)$$

By solving the equation 2.6 for V_c(t) and current through capacitor I_c(t) the following expression are given:

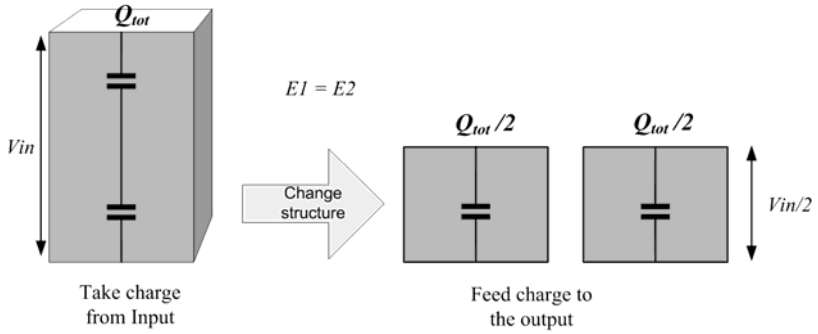

Figure 2-3: concept of capacitive conversion from charge point of view.

$$V_c(t) = V_{in} - (V_{in} - V_{c,0})e^{-\frac{t}{RC}} \qquad (2\text{-}8)$$

$$I_c(t) = \frac{V_{in} - V_{c,0}}{R}e^{-\frac{t}{RC}} \qquad (2\text{-}9)$$

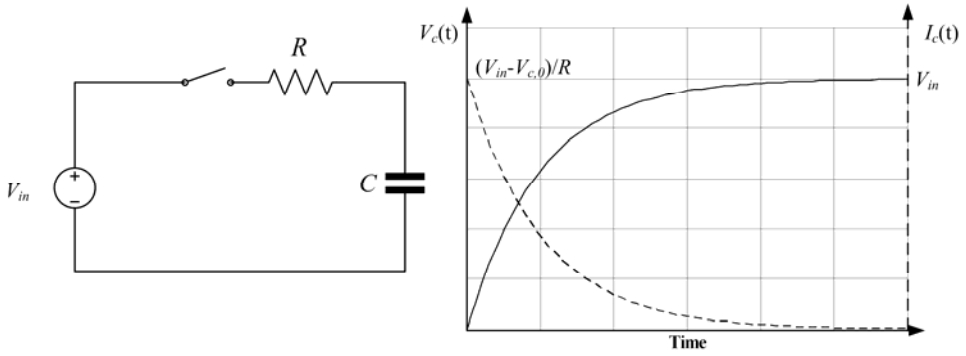

Figure 2-4: Charging of capacitor

Moreover, Energy added to the capacitor by means of this process:

$$E_c = \frac{(V_{dd}^2 - V_{c,0}^2)}{2}C \qquad (2\text{-}10)$$

In addition, total energy delivered by the voltage supply source can be calculated as:

$$E_{tot} = V_{in}(V_{in} - V_{c,0})C \qquad (2\text{-}11)$$

The part of the energy is loss due to resistor R, $V_{c,0}$ is the voltage across Capacitor C at time zero. The charging efficiency $\eta_{c,charge}$ can be quantified by [1]:

$$\eta_{c,Charge} = \frac{1}{2}\frac{V_{c,0} + V_{in}}{V_{in}} \qquad (2\text{-}12)$$

The equation 2.11 demonstrates that efficiency of charging capacitor depends upon ratio of initial voltage and charging voltage. It is also clear that even when capacitor has no series resistance, the power loss will occur. To increase the charging efficiency the voltage difference between initial and final charging voltage should be small. Equation (2-9) demonstrates that if voltage difference is small the energy transfer is small. For high transfer of energy, result in large capacitors.

The operation of charge-pump converter circuit shown in Figure 2-5 works in the following manner. There are two switching networks S1 and S2 are controlled by two-phase control signals. Switches controlled by phase 1 control signal are labeled by S1 and phase 2 with S2. As phase 1 switches are activated while Phase 2 switches are in cutoff mode. C1 is charged to Vin, then output current is supplied by Cout. Once C1 is charged to Vin as a results phase 1 switches are in cut off state and Phase 2 switches are activated. Because of this connection, Cout is charged to 2xVin [6].

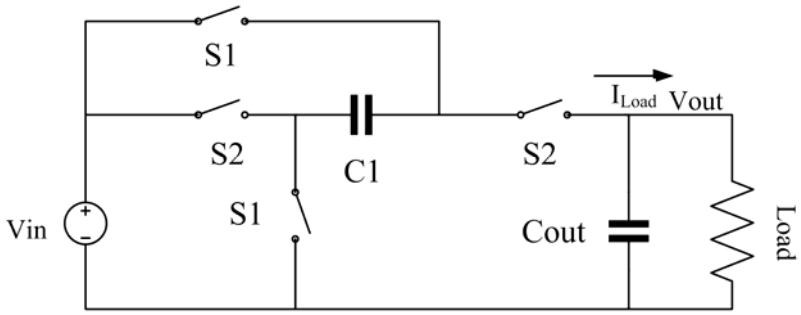

Figure 2-5: Schematic representation of Charge-Pump converter (Vout = 2 x Vin)

The disadvantage of charge-pump converter is the poor efficiency characteristics, discrete output voltages and low output current as compared to inductive type switch-mode converter. However, have better efficiency than linear converters with large voltage conversion ratio. Easy to integrate on silicon, small in size compared to other switched-mode converters and provide opposite polarity output voltages are the main advantages [1].

Inductive Type DC-DC converters

Instead of using the capacitors as storing element, Inductive type DC-DC converters utilize inductor as energy storage element and capacitor for filtering/smoothing output voltage and act as energy reservoir for the load, when converter is not delivering any power to the load. The charging of capacitor through inductor is more efficient than charging through voltage source [1]. Such converters are widely used is both low power and low voltage applications because of high efficiency. Inductive type DC-DC buck

converters will be discussed in detail in the next section. The comparison of three converter types is summarized in Table 2-1.

Table 2-1: Comparison Table of Converter Types

Type of DC-DC Conversion	Linear	Charge-Pump	Inductive Type
Low-to-high voltage conversion	No	Yes	Yes
High-to-low voltage conversion	Yes	Yes	Yes
Polarity reversal	No	Yes	Yes
Efficiency	Low	Low	High
Voltage regulation	Poor	Poor	Good
Output voltage Ripple	low	high	high
Area	Small	Medium	Large
Typical applications	DRAM, Voltage References	DRAM, flash, EEPROM, and mixed-signal	Microprocessors, DSPs, SRAM and hard disks

2.4 Standard Buck Converter

Buck converter is a standard switching DC-DC converter circuit topology with high efficiency and good output voltage regulation characteristics [15], [16], [21]. A buck converter circuit with the synchronous rectifier is shown in Figure 2-6. The operation of buck converter circuit is as follow. The power transistor M_1 and M_2 are switched ON and OFF with the feedback driving signal. This produce the rectangular wave of duty-cycle D and time period T_s at V_X node as shown in Figure 2-6. The rectangular pulses at V_X node is then applied to a second order filter composed of inductor and capacitor. Assuming the filter corner frequency is much smaller than the switching frequency f_s of the power transistors, the low pass filter passes DC component of the signal at V_X node and produce DC desired output voltage V_o.

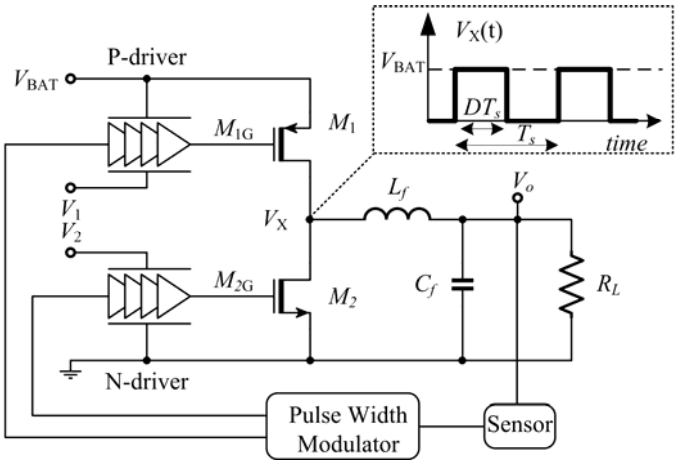

Figure 2-6: (a) standard Buck Converter

Typically, power transistors have high input parasitic capacitances. To control the operation of power transistors, therefore, M_{1G} and M_{2G} are generated from series of gate drivers [5]. These gate driver buffers are typically tapered to drive these large capacitances. The gate drive buffers are controlled by PWM (pulse width modulated). Using feedback circuit, the PWM generates the necessary control signals for the power transistors M_1 and M_2 such that a rectangular pulses with an appropriate duty cycle is produced at V_X(t) as shown in Figure 2-7. During the operation of buck converter, duty-cycle may be modified in order to maintain the output voltage at desired value under variation of load current and input voltage.

The inductor current I_{Lf}(t), output voltage V_o and waveforms of buck converter are shown in Figure 2-7. The filter capacitance is chosen such that the series resistance of the capacitor is much smaller than load resistance. The AC component of the inductor current, therefore, passes through the filter capacitor while the DC component I_o passes through the load. The output voltage increases whenever the inductor current rises above I_o, as the filter capacitor is being charged. Similarly, the output voltage falls whenever the inductor current decreases below I_o, as the filter capacitor is being discharged. The expressions for the inductor ripple current ΔI_o and amplitude of the output voltage ripple is [1]:

$$\Delta I_o = \frac{(V_{BAT} - V_o)D}{2L_f f_s} \tag{2-13}$$

$$\Delta V_o = \frac{(V_{BAT} - V_o)D}{8L_f C_f f_s^2} \tag{2-14}$$

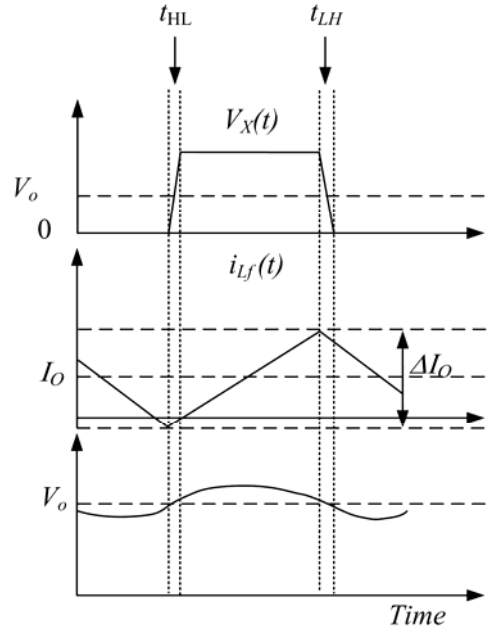

Figure 2-7: nominal steady-state waveforms of inductor current, output voltage and at V_X node.

For a given battery, voltage V_{BAT}, V_o is output voltage for duty-cycle D of switching frequency f_s. C_f and L_f are the output filter capacitor and inductor. Equation (2-12) and (2-13) illustrate the two principle means of miniaturizing a DC-DC converter. The physical size of filter components gets smaller as the switching frequency increases. Second, the requirement of good output voltage regulation with the small voltage ripple, which is possible with higher current ripple as a result of lowering the inductance of filter.

a) Main Losses in Buck Converter

The circuit model of buck converter in Figure 2-8 shows the main losses [22]. The power consumption of a buck converter is combination of the conduction losses caused by the parasitic resistive impedances while the switching losses due to the parasitic capacitive impedances of the circuit components.

MOSFET Power Losses: are due to series resistance while conduction and charging/discharging of parasitic capacitance related to transistors shown in Figure 2-8, in each switching cycle. The power loss due series resistance and parasitic capacitances are:

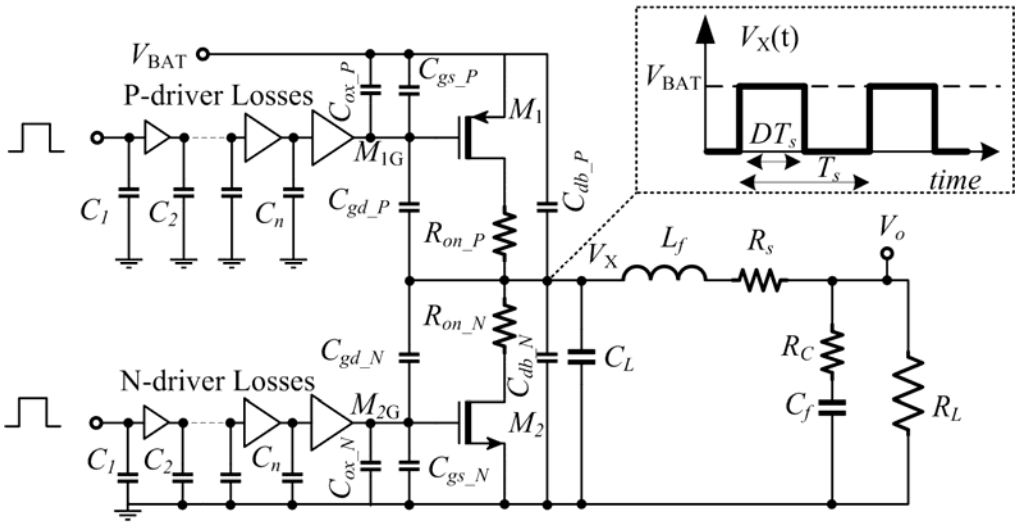

Figure 2-8: circuit model for parasitic impedances of buck converter.

$$P_{mos} = \frac{i_{rms}^2 R_{on}}{W} + E_g f_s W \tag{2-15}$$

$$E_g = \frac{\alpha}{1-\alpha}\left(C_{OX} + C_{gs} + 2C_{gd} + C_{db}\right)V_{BAT}^2 \tag{2-16}$$

Where W is width of transistor, α is tapering factor of buffers, R_{on} is the equivalent series resistance of power transistors (R_{on_P} or R_{on_N}), i_{rms} is the *rms* current passing through the power transistors. C_{ox}, C_{gs}, C_{gd}, and C_{db} are the gate oxide, gate-to-source overlap, gate-to-drain overlap, and drain-to-body junction capacitances, respectively.

From equation (2-15), it is clear that W width of the transistor reduces the conduction losses but increases the switching losses. An optimum transistor width exists that minimize the total transistor power losses [22].

$$W_{opt} = \sqrt{\frac{R_{on} i_{rms}^2}{f_s E_g}} \tag{2-17}$$

$$P_{mos(\min)} = 2\sqrt{R_{on} i_{rms}^2 f_s E_g} \tag{2-18}$$

Filter Inductor Power Losses: are due to series resistance R_s and stray capacitance of filter inductor. Integrated planer spiral inductor losses are high due to poor quality factor [1]. But in recent years, novel low resistance inductors has been reported in [15]. The total power loss in filter inductor is [22]:

$$P_{ind} = b\left[\frac{I_o^2}{\Delta I_o f_s} + \frac{\Delta I_o}{3 f_s} + \frac{C_{Lf} V_{BAT}^2}{R_s \Delta I_o}\right] \tag{2-19}$$

$$b = \frac{(\Delta V_o) D R_s}{2} \tag{2-20}$$

Where C_{Lf} is stray capacitance and D is duty-cycle of switching signal.

Filter Capacitor Power Losses: Standard CMOS technology offers two options of on-chip capacitors, MOM (metal-oxide-metal) and MOS capacitors. The MIM (metal-insulator-metal) capacitor requires additional processing steps [1]. Typically, MOM capacitance densities are in the range of 100 pF/mm^2 to1.5 nF/mm^2. The benefits of MOM capacitors are their ability to withstand higher voltages than the nominal technology supply voltage, their potentially low parasitic series resistance and the possibility to place circuits underneath them. As a drawback, they have a low capacitance density. The second most used on-chip MOS capacitor have capacitance densities are in the range of 3 nF/mm^2 to 20 nF/mm^2 [1]. The main advantage of MOS capacitors is their high capacitance density. The draw back of MOS capacitor, they have high parasitic series resistance as compared to MOM capacitor. In General MOM capacitor offer parasitic series resistance of 200 mΩ to 300 mΩ (for area >1 mm^2) and MOS capacitor offers 300 mΩ to 400 mΩ. However, high MOS capacitor densities save space on silicon. Which makes the MOS capacitor is optimum choice.
The losses in MOS capacitor are due to effective series resistance (esr) R_c. assuming the integrated capacitor is implemented with gate-oxide capacitance of transistor, the total power loss in filter capacitor is [22]:

$$P_{Cap} = df_s \Delta I_o \tag{2-21}$$

$$d = \frac{8R_c L_{Cap} C_o \Delta V_o}{3} \tag{2-22}$$

Where R_c is esr resistance of 1μm wide MOS transistor, L_{Cap} is channel length of transistor and C_{o} is gate–oxide capacitance of μm^2.

Short Circuit Losses: are related to simultaneous conduction of High-side PMOS and low-side NMOS. As in Figure 2-9 shows, if $M_{1\mathrm{G}}$ and $M_{2\mathrm{G}}$ driving signals switch ON power transistors without dead-time, the short-circuit path from VBAT to ground may exists temporarily. To avoid this condition, optimum dead-time introduce between driving signals.

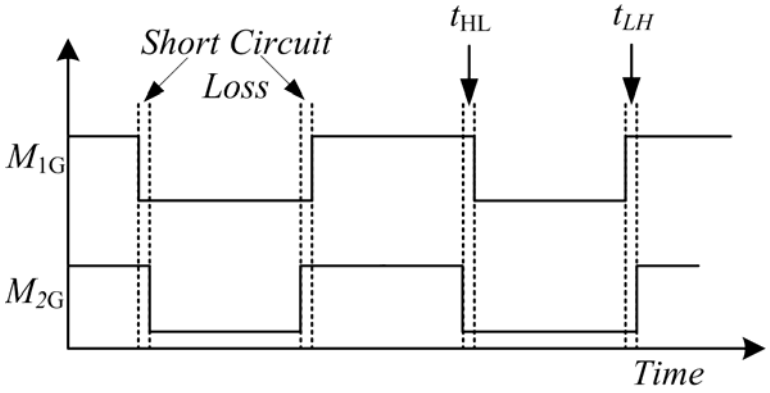

Figure 2-9: Short circuit Losses

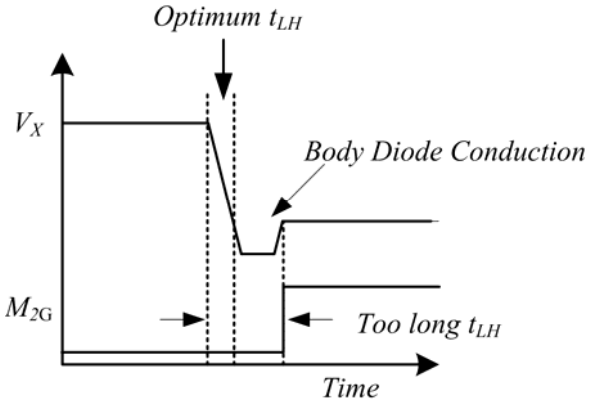

Figure 2-10: Body Diode Conduction

Body Diode Reverse Recovery Losses: are associated with the body diode conduction of switching transistors. To avoid short-circuit losses, we introduce dead-time between driving signal (both power transistors are OFF). If the dead-time is not optimum (too long) in Figure 2-10, the inductor reverse current will force the body diode of low-side NMOS (or High-side PMOS) to conduct. When transistor is turn ON, it removes the excess carrier charge from the body diode, dissipating an energy bounded by:

$$E_{rr} = Q_{rr} V_{BAT} \qquad (2\text{-}23)$$

Where Q_{rr} is the charge stored in the body diode.

2.5 Zero Voltage Switching

Typically, switching DC-DC converters have large inductive and capacitive storage components and power switches that occupy significant area and power. In order to achieve full integration of converter, the sizes of passive and active components of converter are reduced with higher switching frequency. Increasing switching frequency, also increase the power transistor switching losses given in equation (2-14). For reducing switching losses, ZVS (zero voltage switching) technique is often used.

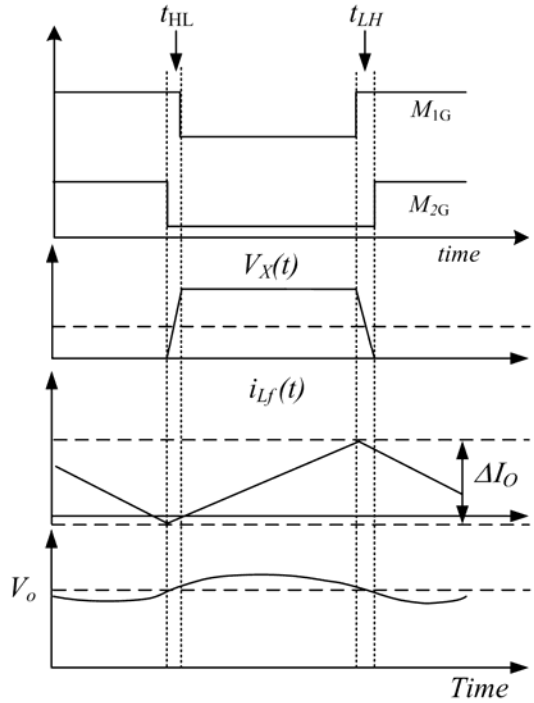

Figure 2-11: ZVS (soft switching) waveforms

In ZVS scheme, filter inductor in Figure 2-8 used to charge/discharge the parasitic capacitances at V_X node in lossless manner, by providing the optimum dead-time between switching signal of M_1 and M_2. If M_1 or M_2 are turned ON immediately after the V_X node charged or discharged by the filter inductor, the power transistor are switched to zero drain-to-source voltage difference (see Figure 2-11), thereby eliminating the switching power losses that would have, otherwise, been dissipated in the power transistor while charging or discharging V_X node.

2.6 Cascode Structure

As discussed earlier in chapter one, with the scaling of CMOS technology, limits the maximum allowed voltage that can be applied across the terminals of transistor for the specific technology. Due to this, the current demand of ICs increase at low voltages, further degrading the efficiency of the off-chip converter. If off-chip converter provides such low voltages at high currents, the losses on Printed circuit board are very high. Therefore, integrating the DC-DC converter on the same IC improves the efficiency, and enhances the quality of the output voltage regulation.

Integration of DC-DC converter on new CMOS technologies, high battery voltage is a problem. In order to solve this issue, cascade structure is appropriate for monolithic integration of converter. The cascade structure can operate at higher battery input voltages than the maximum allowed voltage V_{max} that can be applied across the terminals of transistor in low voltage CMOS technology. The circuit shown in Figure 2-6 is not suitable for monolithic integration of converter. If $V_{Bat} = 2V_{max}$, the buck converter configuration with cascode structure is shown in Figure 2-12. M_2 and M_3 are coscode transistors and M_1 and M_4 are switching transistors.

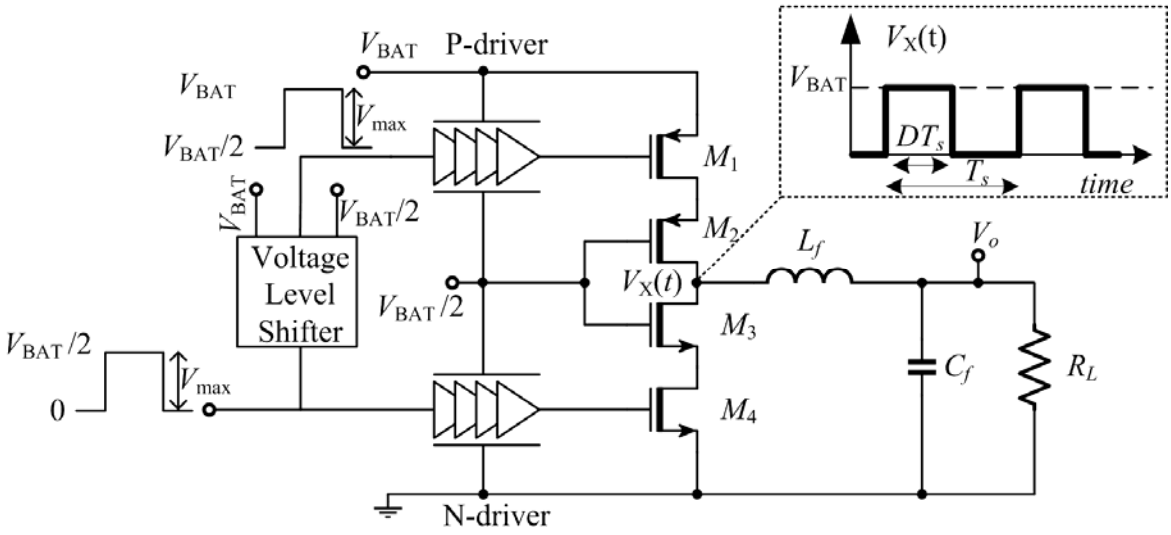

Figure 2-12: standard buck converter with cascode connection.

The cascode structure generates an output signal swinging between V_{BAT} and ground at V_X node from an input control signal swinging between ground and V_{max}, while guaranteeing that the voltages applied across the gate-to-source, gate-to-drain, and gate-to-body terminals of the transistors do not exceed the maximum voltage difference, V_{max}, to avoid gate oxide breakdown in a CMOS technology.

2.7 Voltage Level Shifter

Level shifters are important building blocks in power management systems. In DC-DC buck converters they are used to interface blocks operating at different supply domains. Figure 2-12 gives the general idea of voltage level shifters, which converts the low voltage control signal of the low-side N-driver to the high voltage control signal for high-side P-driver with the DC offset of $V_{BAT}/2$.

Level shift circuit topologies in low voltage technologies found in literature [31] suffer from large delays between input and output and are not able to drive large capacitive loads in an efficient way. This can lead to excess power dissipation in the following circuits. Due to non-idealities of level shifters, this thesis proposed to avoid level shifters and direct signal transfer between the high-side PMOS driver and the low-side NMOS driver. The low-side NMOS driver is driven with PWM signal to control the output voltage. The high-side driver is synchronized from the output via an inductive triggering scheme. The inductive feedback provides fast response, which is coherent with the high-frequency DC-DC converter. The inductive feedback is most suitable for fully integrated DC-DC converters, since the sensing winding can be placed beneath the main coil. Special means are provided to avoid short-circuit current by adjusting the ON-time of the PMOS power transistors.

3 Self-Triggered DC-DC Converter

The idea of self-triggered converter is to remove level shifter to improve power efficiency. In addition, synchronize the high-side driving signal from the output via inductive feedback and obtains automatic dead-time to avoid short circuit losses with no additional hardware. The output voltage regulation can be realized by feedback PWM signal controlling the low-side NMOS switching transistor. The idea of self-triggered is originated from self-oscillating PWM converter [19] which is similar to the proposed self-triggered converter utilize the information from the output and inductive feedback to create driving pulses. Before going into detail operation of proposed topology, let us first discuss the operation of self-oscillating converter, it will help to understand the operation of self-triggered converter.

3.1 Self- oscillating Converter

The self-oscillating converter in Figure 3-1, the low-side NMOS and high-side PMOS drivers are replaced with the trifiliar transformer that provide positive feedback for switching ON and OFF M_1 and M_4 transistors. In trifiliar transformer, main winding L_M is inversely coupled L_{gp} and L_{gn} windng. M_1 and M_4 represent the switching transistors while M_2 and M_3 are cascoded transistors. The capacitive divider C_{r1} and C_{r2} are large enough to create the reference voltage V_R (or AC-ground) while charging and discharging current of main winding L_M. L_f and C_f are the output filtering components.

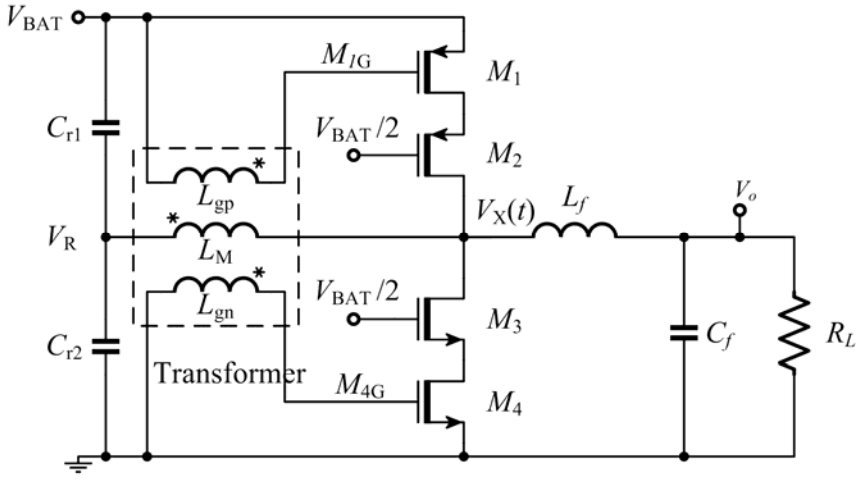

Figure 3-1: Self-oscillating converter topology

When V_{BAT} voltage is applied, $V_{BAT}/2$ will appear at V_R node through capacitive divider. Initially the voltage at switching node V_X is zero. The main winding of the transformer L_M is placed between the switching node (V_X) of the converter and V_R node. The voltage difference across main winding L_M become plus $V_{BAT}/2$ transfer to L_{gp} and

L_{gnd}, switch ON M_1 and charge the V_X node to V_{BAT}. Afterwards, minus $V_{BAT}/2$ voltage appear across the main winding and switch ON M_4. The oscillation frequency depends on the transformer inductances, on the transformer magnetic characteristic, and on the parasitic capacitance connected to the gates of the switching transistors. Thus, the oscillation frequency depends on the load current and battery voltage. The amplitude of the voltages supplied to the gates of M_1 and M_4 can be controlled by designing the transformer ratios (L_{gp} / L_M / L_{gn}), but it cannot be used for electronic control. The amplitude of M_{4G} goes below zero, while M_{1G} goes above V_{BAT}, which guarantees secure switch OFF of the power switches, but it introduces extra losses. However, self-oscillating converter has no voltage and load regulation even the duty cycle is around 50%. They are difficult to implement on silicon because small saturable core inductors are used in [20] and no magnetic core available on standard silicon process. Self-oscillating converters are mostly used in high power applications some state-of-art self-oscillating DC-DC converters are reported in Table 3-1.

Table 3-1: Comparison of State-of-Art Self-Oscillating DC-DC converter

Reference	**[26]**	**[19]**	**[28]**	**[25]**	**[27]**
Vin	12V	600V	48V	24V	1.1V
Vout	32V	300V	12V	3-20V	7V
Switching Frequency	110MHz	9KHz	100KHz	200KHz	1MHz
Max.Efficiency	87%	>90%	86%	93%	25%
Converter Type	Boost	Buck	Buck	Buck	Boost
Power	23W	3KW	100W	4W	1mW
Integrated	No	No	No	No	No
Saturable Cores	No	Yes	Yes	Yes	Yes
Year of Publication	2009	2002	2005	2012	2012

3.2 Self-Triggered Converter

A proposed self-triggered converter working principle is quite same as self-oscillating converter. In self-oscillating converter, the gate drivers are replaced with the trifilar transformer but the driving signal is more sinusoidal than square wave as well as it is not suitable for integrated circuits. In self-triggered converter, we replace the trilfilaar transformer with single winding (called secondary winding) for inductive feedback and pulse-forming circuit for signal shaping and creating dead-time. The primary winding of the transformer is used for both transferring the feedback signal to the secondary

winding, and for filtering the output voltage. The low-side NMOS is driven by external feedback PWM signal. Therefore, the self-triggered converter does not start oscillating by itself but it has driven by external PWM signal (or driven converter). The self-triggered title reflects the triggering scheme of high-side PMOS control signal that generates the dead-time between high-side and low-side control signals.

The proposed self-triggered DC-DC converter is depicted in Figure 3-2. Transistors M_1 through M_4 form the cascode switch-bridge and L_f and C_f are the filtering inductor and capacitor, respectively. The low-side NMOS transistor is controlled by PWM signal applied to the gate of M_4 through the low-side driver. The output voltage is regulated for line or load variations by adjusting the duty-cycle of the PWM signal.

The high-side driver is replaced with the coupled inductor L_{sec} and pulse forming block, as shown in Figure 3-2, isolates the gate capacitance of the M_1 from the secondary winding of the transformer and performs shaping of the gate voltage to obtain a square-wave signal at the gate of M_1 rather than a sinusoidal one. Furthermore, since the input impedance of the pulse-forming block is substantially bigger than the impedance of M_1, the secondary winding carries very small current and the losses associated with L_{sec} are minor. The capacitors C_{r1} and C_{r2} are coupling capacitors and should be large enough so that their voltage remains nearly constant during the charging and discharging currents of L_{pr} and L_{sec}. The orientation of the L_{pr}-L_{sec} windings is such that a decreasing voltage at V_X node causes voltage at the gate of M_1 to increase and vice versa.

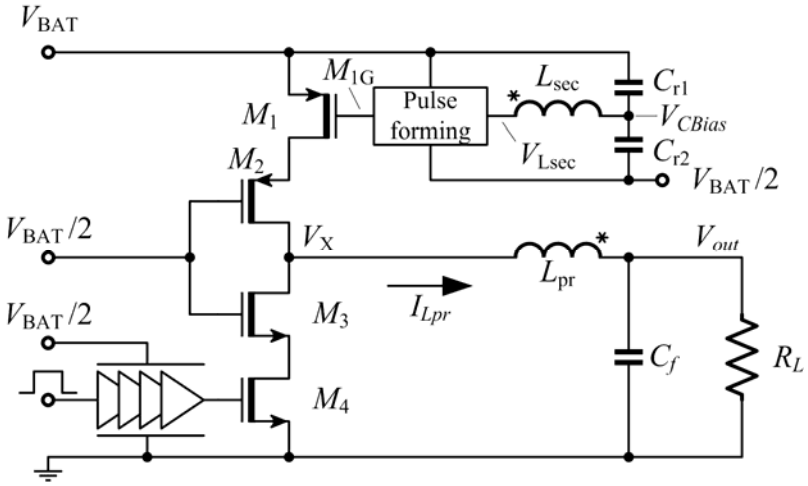

Figure 3-2: the proposed self-triggered converter

The implementation of the pulse-forming block is shown in Figure 3-3. The inverters, M_{p1}-M_{n1} and M_{p2}-M_{n2}, provide the delay time, t_{LH}, between the moments when V_X node voltage starts increasing and when M_1 switch ON see Figure 3-5. The resistive combination of R_{B1}, R_{B2}, R_{fb} and transistor M_{fb} form a resistive divider, which create a certain dc-bias voltage at the input of inverters M_{p1}-M_{n1} and M_{p2}-M_{n2}.

The working principle of proposed converter can be explained from Figure 3-5. At time t_1, M_4 is switched OFF, causes the V_X node starts rising to V_{BAT} (due to reverse inductor current operating in ZVS). Inverse transformer operation causes the rising edge at V_X

node to transfer as falling edge at V_{Lsec} (Figure 3-5). V_{Lsec} is then applied at the input of pulse-forming block inverters. Here the inverters provide the delay time, t_{LH}, between the falling edge of V_{Lsec} and $M_{1\mathrm{G}}$.

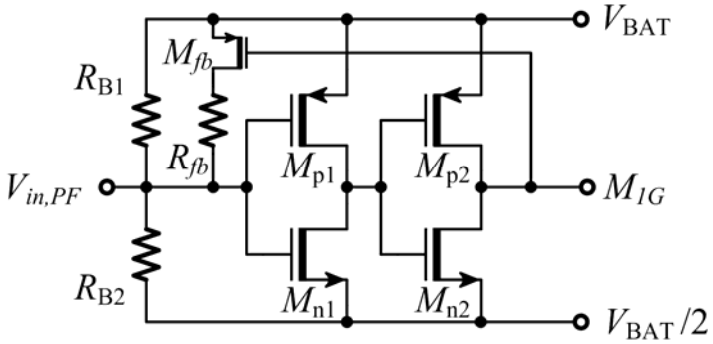

Figure 3-3: pulse forming block

At time, t_2 in Figure 3-5 $M_1$is already switched ON and V_X node voltage has reached V_{Bat}. The primary side current I_{Lpr} is continuously increasing from time t_2 to t_3, which causes the voltage decrease across L_{Pr} winding due to series resistance of L_{Pr}. As an effect of inversely coupled winding, the V_{Lsec} voltage starts increasing. At the same time t_2, the signal at $M_{1\mathrm{G}}$ also switch ON M_{fb}, pulling up the DC-Level at the input put of pulse forming block V_{CBias} see Figure 3-5 . After a transient process at the input of the pulse-forming block, the voltage crosses a triggering level, which terminates the ON pulse for M_1. The duration of the ON pulse is adjusted via feedback resistance R_{fb}. By changing value of R_{fb}, V_{Lsec} voltage reaches the triggering level V_{trig} of pulse forming block inverters at different time instances; see Figure 3-4 (a). This generates output $M_{1\mathrm{G}}$ after pulse forming block inverters delay and switch OFF M_1 and M_{fb}. Creating t_{HL} dead-time, which would not have been without the presence of M_{fb} and R_{fb}. In addition, if the duty cycle of $M_{4\mathrm{G}}$ pulse is changed, the time delay t_{HL} does not only remain dependent on R_{fb} value, it also becomes dependent on duty cycle of switching frequency.

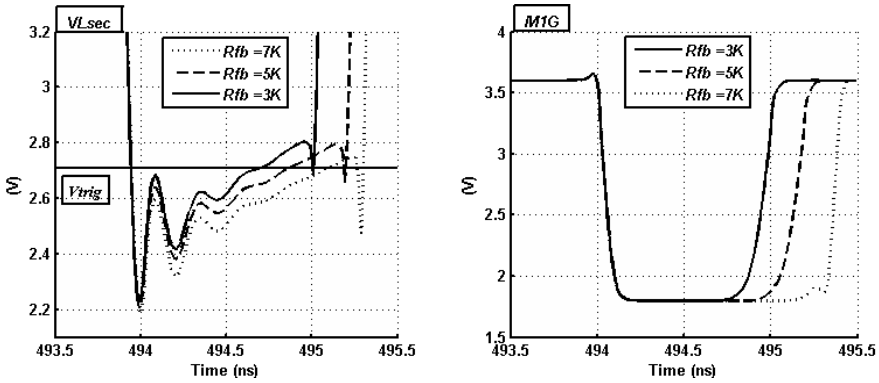

Figure 3-4: (a) Close up of V_{Lsec} at different R_{fb} values (b) Effect of changing R_{fb} on the turn-on time of M_1.

This is because of the fact that changing duty cycle changes timing instant for rising edge of $M_{4\mathrm{G}}$ pulse. As a result, for changing duty cycle at $M_{4\mathrm{G}}$, R_{fb} value needs to be

changed electronically in order to generate optimum time delay t_{HL}. The automatic tuning of R_{fb} with respect to duty cycle has been left for future work of modified converter.

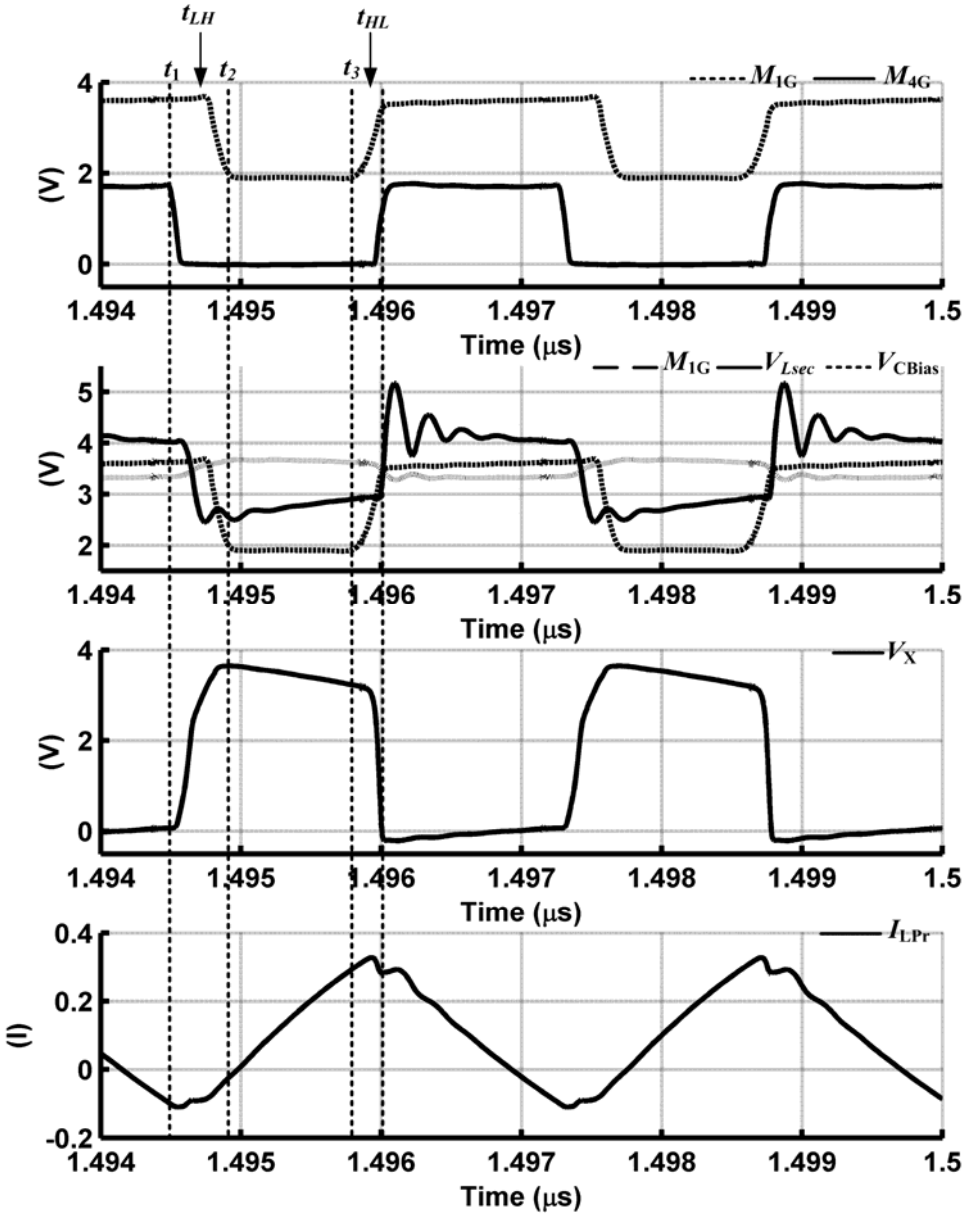

Figure 3-5: simulated waveforms of self-triggered converter

3.3 Transformer Design for Self-Triggered Converter

High-Quality factor inductors (μH Range) are needed to achieve high efficiency converters. Unfortunately, the inductance density of on-chip inductors yields small inductances (nH range) and high series resistance, which result in low-efficiency converters. To overcome these issues, there is need to decrease the size of on-chip inductors, which is possible by increasing the switching frequency of buck converter

[1]. In self-triggered DC-DC Converter, the filtering inductor L_{pr} shown in Figure 3-2 is used as current source to charge and discharge the V_X node and magnetically couple with L_{sec}, which provides the driving signal for high-side transistor $M_{1G.}$ The magnetic coupling between $L_{pr} - L_{sec}$ can be realized by stacking the two inductors (transformer action) stacked on each other above the silicon substrate.

The design and modeling of monolithic planer transformer is a demanding task. In contrast to ideal transformer, monolithic transformers have parasitic effects and imperfect coupling between winding, which result is coupling factor less than one. Here, the goal is to model monolithic planer transformer at desired frequency range with minimum possible losses of primary winding L_{pr} and coupling factor k = 0.7 approximately. The modeling of monolithic planer transformer is done with 2.5D electromagnetic simulator FastModel (FastHenry and FastCap) [6]. The FastHenry and FastCap are based on Finite Element Method (FEM) core. FastHenry is used to calculate the inductances, and resistive losses of complex structures. FastCap is used to extract the capacity of complex geometries [7].

The modeling of a transformer in FastHenry starts with definition of its geometry. To define the geometry, subroutine is written in Ms-Excel, geometry is shown in Figure 3-6. The geometry of primary winding L_{pr} is constructed in such a way to get the minimum possible resistive losses. The distance between primary and secondary winding is adjusted to 3um to get coupling factor k = 0.7 approximately. The secondary winding is providing the scaled and inverted voltage of voltage across the L_{pr} for switching ON and OFF the M_1 power transistor. The geometrical parameters of transformer are shown in Table 3-2.

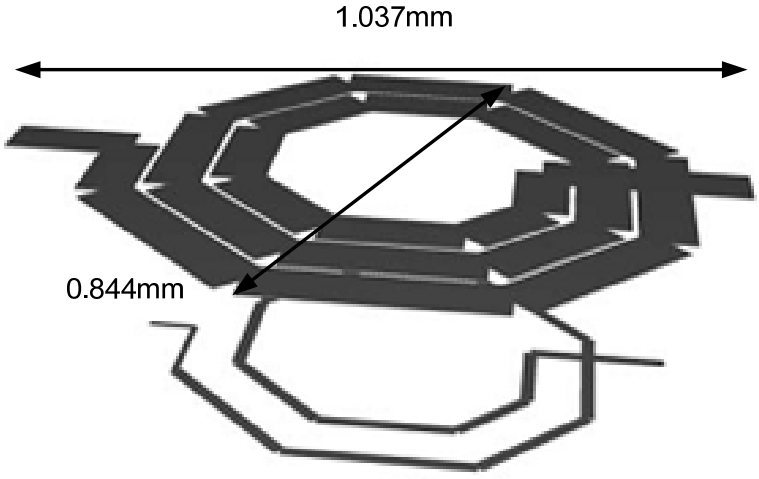

Figure 3-6: Transformer Geometry from FastHenry

Next step is to find the substrate losses and capacitive coupling between L_{pr}-L_{sec} winding, L_{pr} to substrate and L_{sec} to substrate. The substrate material of silicon technologies has mixture of conductors and dielectric, which means substrate have finite

conductivity σ and permeability εr ≥ 1. Capacitive coupling from L_{pr} and L_{sec} winding to substrate and finite conductivity of substrate causes finite current flow from winding through the substrate down to ground plane. The current flow represents the additional losses, which are model by substrate resistance *Rsubp* and *Rsubs*. The geometry in Figure 3-7 shows how L_{pr} and L_{sec} winding are suspended over the substrate.

Table 3-2: Transformer Geometrical Parameters

Parameters	Values
Inner Radius L_{pr}	200um
Outer Radius L_{pr}	416um
Track Width L_{pr}	80um
Separation b/w L_{pr} Track	10um
Inner Radius L_{sec}	205um
Outer Radius L_{sec}	293um
Track Width L_{sec}	20um
Separation b/w L_{sec} Track	78um
Size of Transformer	1.037mm x 0.844mm

The formula for the specific substrate resistance of an L_{pr} and L_{sec} winding placed on the substrate can be written as [10]:

$$Rsubp = \frac{\rho}{\pi lmp} \ln\left[2\coth\left(\frac{\pi}{8}\frac{Wp + 6Hox + T}{Hsub}\right)\right] \qquad (3\text{-}1)$$

$$Rsubs = \frac{\rho}{\pi lms} \ln\left[2\coth\left(\frac{\pi}{8}\frac{Ws + 6Hox + T}{Hsub}\right)\right] \qquad (3\text{-}2)$$

Where:

$$Wp = rop - rip \quad : rop\ and\ rip\ are\ outer\ and\ inner\ radius\ of\ winding$$

$$Ws = ros - ris \quad : rop\ and\ rip\ are\ outer\ and\ inner\ radius\ of\ winding$$

$$lmp = 8(arop + arip) \quad : perimeter\ of\ octagonal\ winding$$

$$lms = 8(aros + aris) \quad : perimeter\ of\ octagonal\ winding$$

The resistance *Rsubp1*, *Rsubp2* and *Rsubs1*, *Rsub2*of the model shown in Figure 3-9 can be determined as [10]:

$$\begin{aligned} Rsubp1 &= RsubP2 = 2Rsubp \\ Rsubs1 &= Rsubs2 = 2Rsubs \end{aligned} \qquad (3\text{-}3)$$

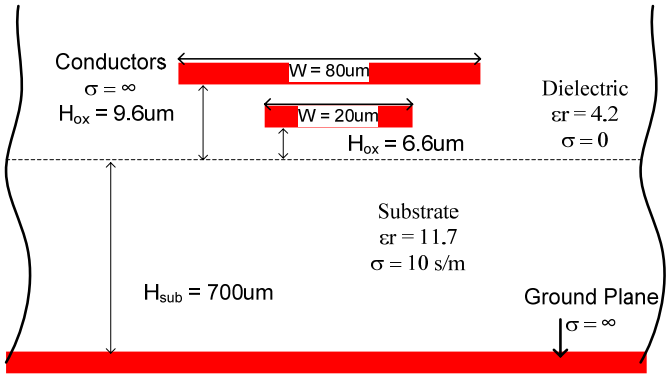

Figure 3-7: L_{pr} and L_{sec} suspended in dielectric above substrate

For capacity extraction between L_{pr}-L_{sec} winding, L_{pr} to substrate and L_{sec} to substrate, FastCap is used. The input file for FastCap is different than FastHenry input file. To make input file for FastCap is very lengthy and time-consuming process to ovoid this ConvertHerny is used [7]. ConvertHenry is separate software utility, which converts the FastHenry input File into FastCap input file. FastCap calculate the capacitance of structure shown in Figure 3-7 in meters unit. Therefore to calculate the capacitance in μm, need to multiply results by 10^{-6} [7]. The FastCap output is in Matrix form called Maxwell capacitance matrix shown in Figure 3-8.

$$\begin{bmatrix} C_{11}+C_{12}+C_{13} & -C_{12} & -C_{13} \\ -C_{21} & C_{21}+C_{22}+C_{23} & -C_{23} \\ -C_{31} & -C_{32} & C_{31}+C_{32}+C_{33} \end{bmatrix}$$

Figure 3-8: The Maxwell Capacitance Matrix

The C_{12}, C_{13}, C_{23} are capacitances between L_{pr}-L_{sec} winding, L_{pr} to substrate and L_{sec} to substrate respectively. The capacitance shown in Figure 3-9 can be determined as given in [10]. The complete model and parameter values of transformer are shown in Figure 3-9.The response of transformer model is given in Section 4.3

$$C_k = \frac{C_{12}}{4} \tag{3-4}$$

$$C_{OXP1} = C_{OXP2} = \frac{C_{13}}{2} \tag{3-5}$$

$$C_{OXS1} = C_{OXS2} = \frac{C_{23}}{2} \tag{3-6}$$

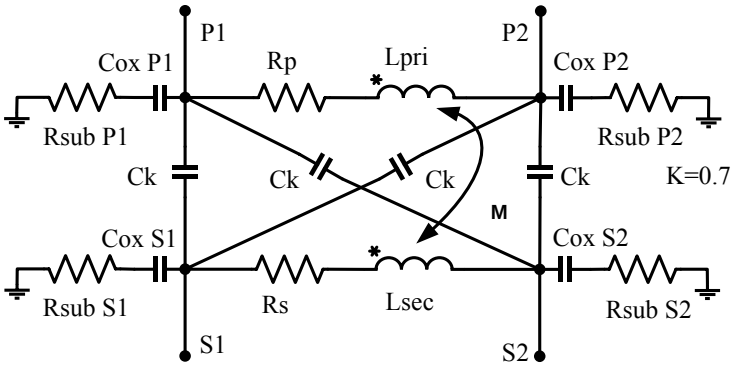

Figure 3-9: Model of Transformer

Model Parameters Values

Parameters	Values
Lpri	5nH
Lsec	2.36nH
Rp	1.01 Ω
Rs	12.18 Ω
Coxp1, Coxp2	517fF
Coxs1, Coxs2	86fF
Ck	190fF
Rsubp1, Rsubp2	145 Ω
Rsubs1, Rsubs2	100 Ω

4 Design and Simulations

GPDK 45 nm CMOS process [29] was used to design and simulate the self-triggered converter as shown in Figure 4-1. The design was divided into following modules: Casocoded power transistors, which consists of high-side PMOS and low-side NMOS transistors, low-side NMOS driver, transformer for inductive feedback and pulse forming circuit for wave shaping.

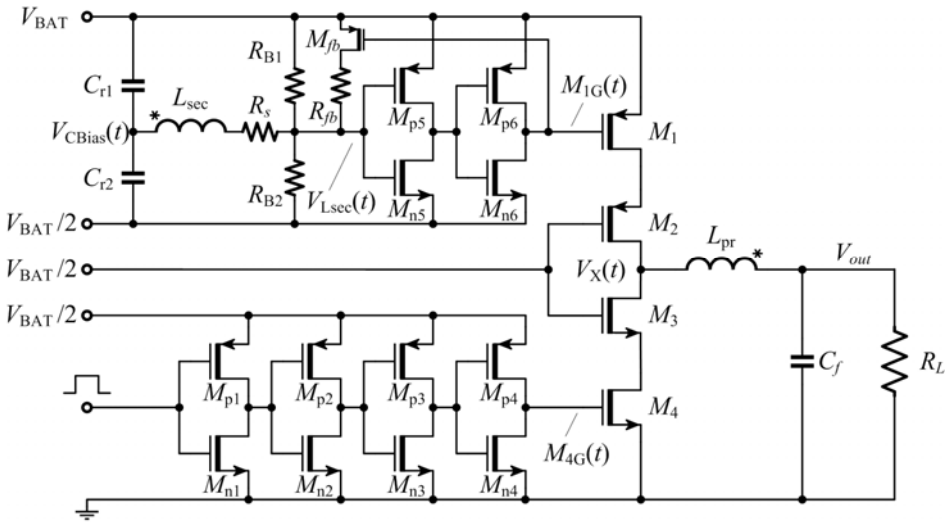

Figure 4-1: Self-triggered DC-DC converter

All transistors in this design make use of 1.8 devices. The operating switching frequency of converter has to be high enough to achieve practical transformer size for on-chip integration and satisfy the requirement of ZVS. Large output capacitor can be used at the output, in order to achieve the small voltage ripple. The converter generates 1.5 V output voltage from 3.6 V input voltage, while providing 100mA current to the load. The converter is operating at switching frequency of 360 MHz. The specifications of proposed converter are shown in Table 4-1.

Table 4-1 : Specifications of proposed Self-Triggered buck Converter

Technology	Vin [V]	f_s [MHz]	L_{pr}-L_{sec} [nH]	I_{out}(TYP) [mA]	V_{out} [V]	ΔV_{out} /*Vout* [%]	η(*Max*) [%]
45nm CMOS	3-3.6	360	5-2.36	100	1.5	<10	>63

4.1 Power Transistor Sizing

The sizing of transistor are mainly depends on conduction and switching losses of the power transistors as described in equation (2-4). The decrease in conduction losses

increases the switching losses. The optimum transistor sizes for 360MHz (transformer is designed for 360MHz switching frequency) are achieved when the conduction losses are equal to switching losses [2]. For the proposed converter, the minimum channels length is 150nm is used for power transistors. Figure 4-2 gives the simulated conversion efficiency as a function of PMOS power transistor widths. The NMOS size is half of PMOS size. The maximum conversion efficiency is achieved at 3.7mm PMOS power transistor width.

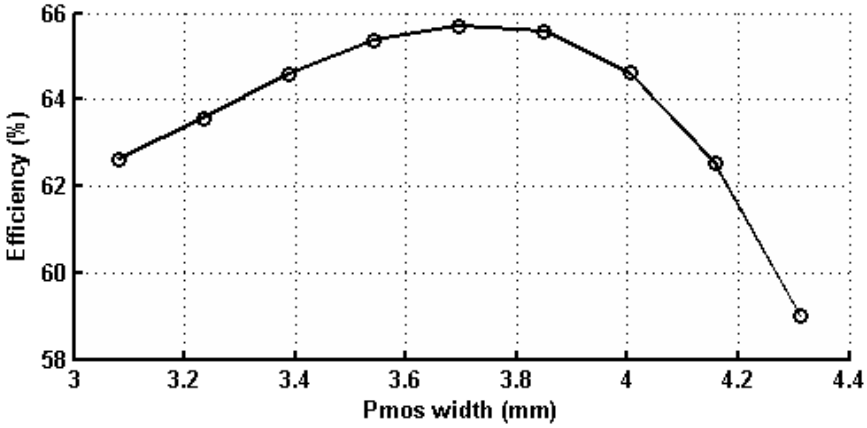

Figure 4-2: PMOS power transistor width Vs. Efficiency (W_{NMOS} = 1/2 W_{PMOS})

4.2 Switching Frequency

In practice, it is hard to determine the switching frequency of the converter. Switching frequency of converter should be high enough so that filtering inductor and capacitor sizes become small enough for on-chip integration. In addition, switching frequency should be far below 1GHz where the substrate effects become significant. As transformer is designed for 360MHz switching frequency converter, efficiency of converter were simulated at different frequencies. Figure 4-3 shows converter achieved maximum efficiency at switching frequency of 360MHz.

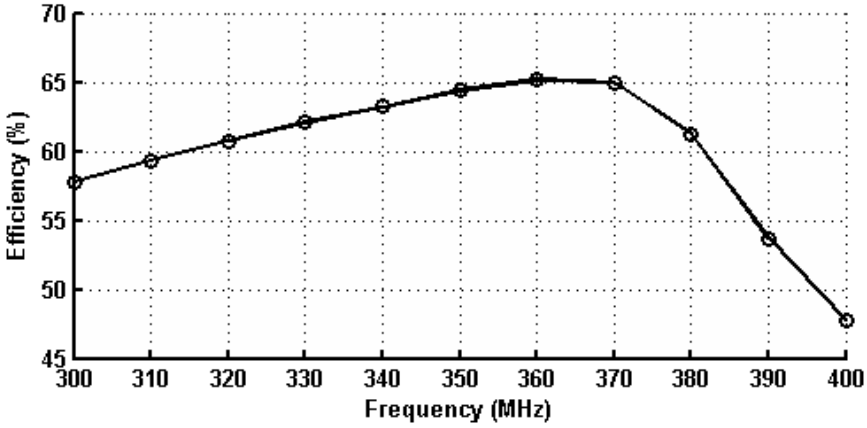

Figure 4-3 : Frqeuency vs. Efficiency

4.3 Transformer Design Simulations

In self-triggered converter, the primary winding is used as filtering inductor and for inductive feedback. The design procedure of transformer has been described in section 3.3 . The transformer's characteristics will discuss in this section.

The S-parameter describes the electrical behavior of a monolithic planer transformer completely. However, not only the scattering parameters must be observed. The Z-parameters, Y-parameters, K-factor and Q-factor give a fundamental insight to the transformer's characteristics. These parameters can be derived directly from S-parameters. Figure 4-4 (a)-(d) and (e) shows simulation setup for quality factor of primary and secondary winding and K-factor respectively.

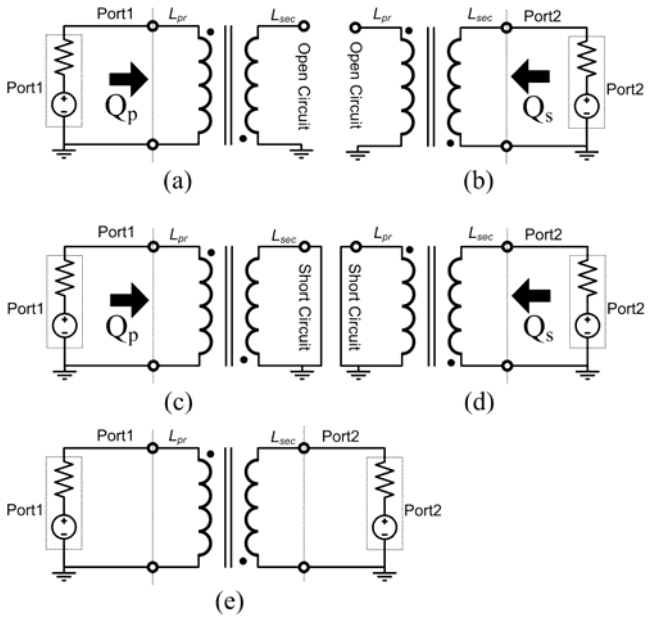

Figure 4-4: from (a)-(d) simulation setup for Quality factor of transformer. (e) Simulation setup for coupling factor K.

Figure 4-5 shows the characteristic Q-factor of the primary and secondary winding. Therefore, the output is left open (see Figure 4-4(a) (b) and Figure 4-5(b)). Q-factor value at 360MHz of primary winding is 12 and secondary winding is 0.55. Figure 4-5(a) shows the quality factor of the transformer with shorted output. The quality factor is analyzed using the following expression [10].

$$Q = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \qquad (4\text{-}1)$$

Analyzing the coupling coefficient as a function of frequency the relation is useful

$$M = \sqrt{\left(Y_{11}^{-1} - Z_{11}\right)\frac{Z_{22}}{\omega^2}} \qquad (4\text{-}2)$$

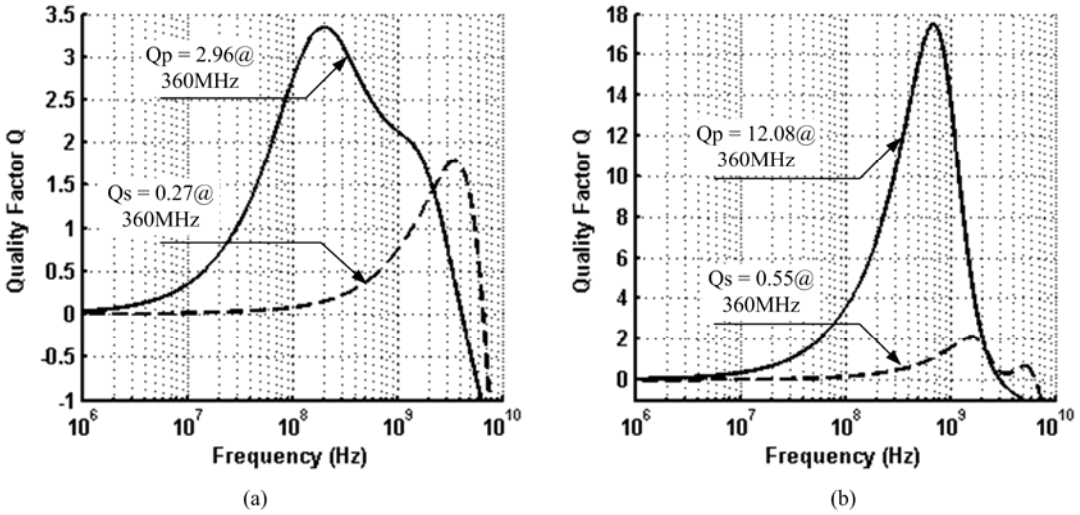

Figure 4-5: (a) Quality factor of primary and secondary winding, when other side winding short-circuit respectively. (b) Quality factor of primary and secondary winding, when other side winding open-circuit respectively.

Then the coupling coefficient can be written as [10]:

$$k(L_{pr}, L_{\sec}) = \frac{M}{\sqrt{L_{pr} L_{\sec}}} = \sqrt{\frac{\left(Y_{11}^{-1} - Z_{11}\right) Z_{22}}{\mathrm{Im}(Z_{11})\,\mathrm{Im}(Z_{22})}} \qquad (4\text{-}3)$$

Figure 4-6 shows the K-factor is ~0.7 at 360MHz is good value for monolithic planer transformer.

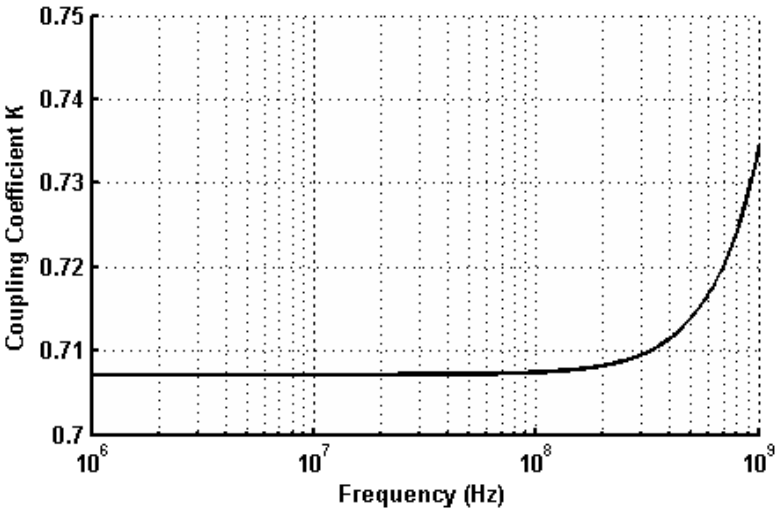

Figure 4-6: K-factor Vs. Frequency.

4.4 NMOS gate driver design

Other than switching and conduction losses of DC-DC converter (given in section 2.4), timing delays and driving losses of gate driver are also major power dissipation contributors in DC-DC converter. The driving loss is represented in the following equation [5]:

$$P_{driving} = f_s V_{Supply} Q_g \qquad (4\text{-}4)$$

Where V_{Supply} is supply voltage, f_s is switching frequency and Q_g is gate charge capacitance of the output stage power transistor. The driving losses can be reduced by lowering the gate charge capacitance; however, reducing the gate charge increases the R_{on} series resistance of Power transistor. Another possibility of reducing gate drive loss by decreasing the supply voltage of the gate driver, it enable the fast switching and reduce the delays of driver. While designing the NMOS gate driver cascaded tapered inverters configuration is used, this increases the current capability to minimize the delay. Figure 4-7 shows the four tapered cascaded inverter stages with the tapering factor of ~3. The sizes of transistors are adjusted with electrical simulation to get minimum time delay of the driver.

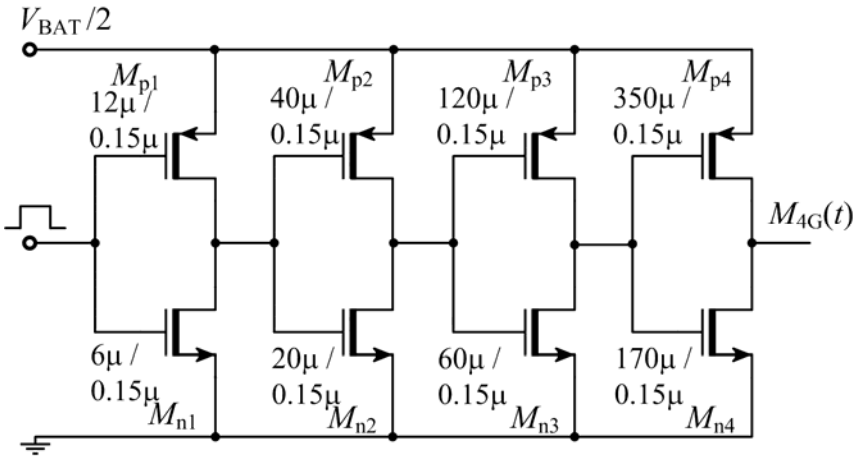

Figure 4-7: NMOS Cascaded gate driver.

In proposed self-triggered converter, the timing delay of NMOS gate driver is important. Because, high-side PMOS driving signal is depend on M_{1G} and automatically obtain dead-times that avoid short-circuit losses with no additional hardware or driving signal adjustment (improvement in comparison to the standard buck converter, which requires special arrangement of driving signals).

4.5 Pulse Forming Block

The pulse forming block contain a tapered buffer stage, feedback transistor M_{fb}, resistor R_{fb} and biasing resistors R_{B1} and R_{B2}. The biasing resistors set the DC-level of signal coming from secondary winding. Buffer stage isolates the potentially big input capacitance of the M_1 transistor from the secondary winding and makes a square-wave M_{1G} signal from distorted signal (more like sinusoidal shape) coming secondary winding. M_{fb} and R_{fb} define the ON pulse width of M_1 transistor.

The buffer delay determines t_{LH} dead-time and R_{fb} determines t_{HL} dead-time by changing the DC-level of pulse. The size of buffer is adjusted according to dead-time in which

ZVS satisfy (V_X node charge to V_{BAT}) and capable to drive big input capacitance of M_1 and M_{fb}. The size of feedback transistor M_{fb} is adjusted so that R_{on} resistance of transistor does not affects the DC-level at the input of pulse forming block when it switch ON.

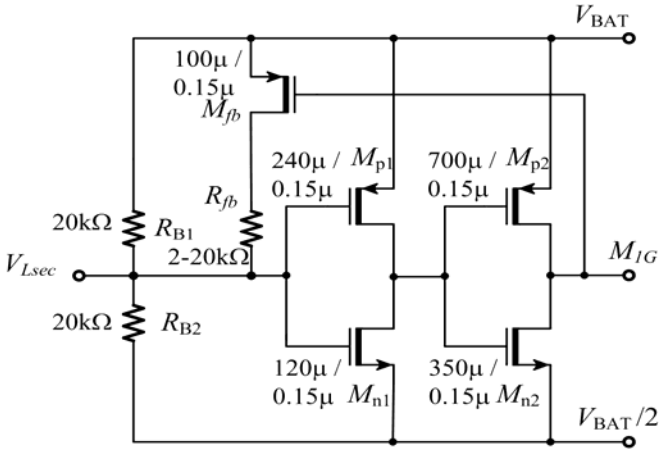

Figure 4-8: Pulse Forming Block

4.6 Simulation Results

Initially, circuit was designed with ideal components. The principle of operation and the performance of the Self-Triggered Converter are demonstrated by using the proposed topology shown in Figure 4-1 and test bench used for simulations is shown in Figure 4-9.

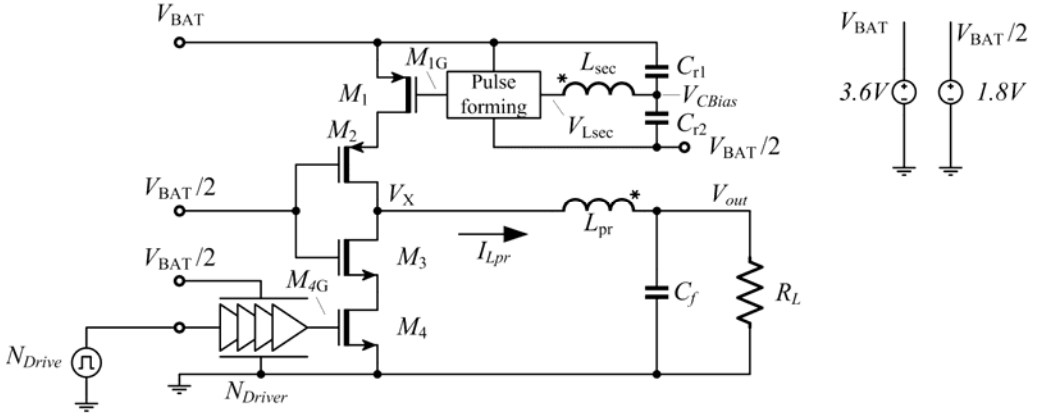

Figure 4-9: Test Bench of self-triggered converter

Waveform analysis

Simulated waveforms of the self-triggered converter in Figure 4-1 are shown in Figure 4-10. The driving signals applied to the gates of transistors M_1 and M_4 have square-wave shape (Figure 4-10), which help to achieve good converter efficiency. The dead-times between M_{1G} and M_{4G} are automatically created, as described in the section 3.2 , to achieve ZVS operation. The duty-cycle of the input signal controls only the duty-cycle of M_{4G}. When M_{4G} goes to zero, the inductor current is negative (Figure 4-10),

which is required condition for achieving ZVS operation. The negative inductor current charges the capacitance associated with the V_X node, and the V_X node voltage increases from zero to V_{BAT} (Figure 4-10). The rising front of the V_X voltage is transferred as a falling front at the input of the pulse forming block (Figure 4-10), which triggers the high-side driver. The delay of the two inverters in the high-side driver provides the dead-time t_{LH} needed for the V_X node to reach V_{BAT} level in a ZVS fashion.

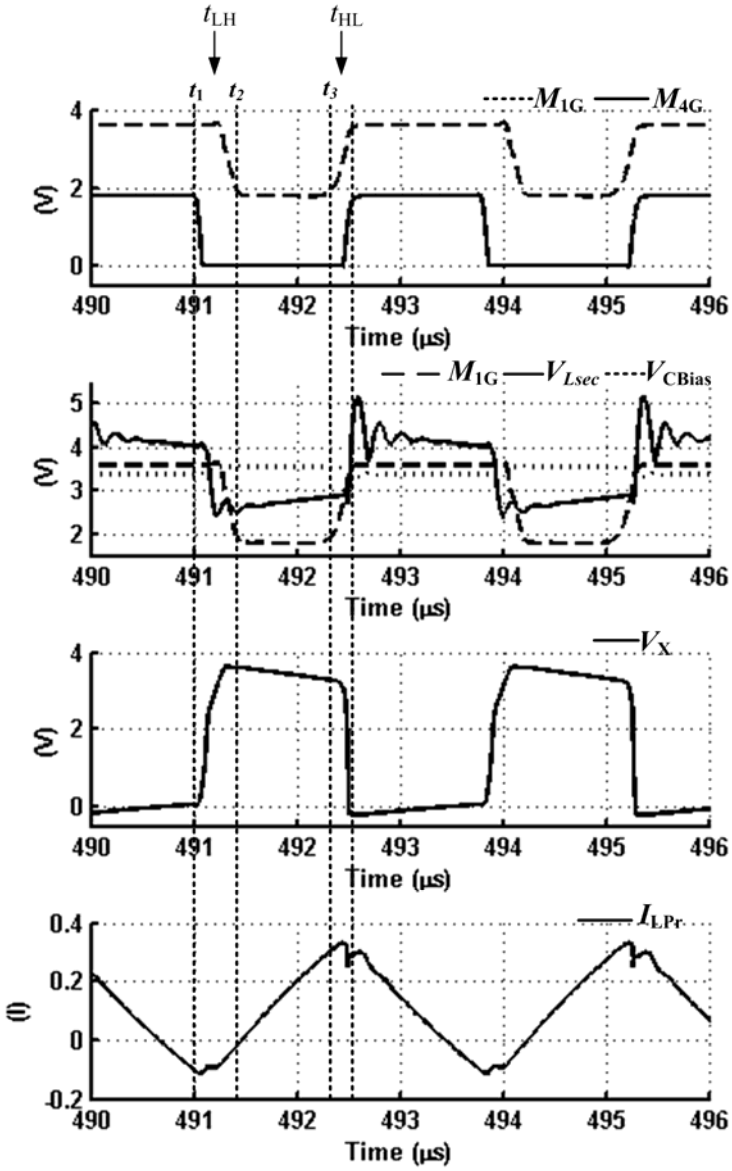

Figure 4-10: simulated waveforms with ideal components.

The transistor M_1 switched ON after the delay t_{LH} and also switch ON feedback transistor M_{fb}, which pulls up the DC-level of the input of the Pulse-Forming Block. After a transient process at the input of the Pulse-Forming Block, the voltage crosses a triggering level, which terminates the ON pulse for M_1. The duration of the ON pulse can be controlled via the feedback resistance R_{fb}. The M_{4G} signal should stay at low-voltage level during the whole duration of the ON pulse to avoid short-circuit current.

After termination of the ON pulse, M_1 is switched ON. The dead-time t_{HL} is created between the termination of the ON pulse for M_1 and the triggering of M_4. The adjustment of t_{HL} could be realized either by varying the duty-cycle of M_{4G}, either by changing the duration of the ON-pulse via R_{fb}.

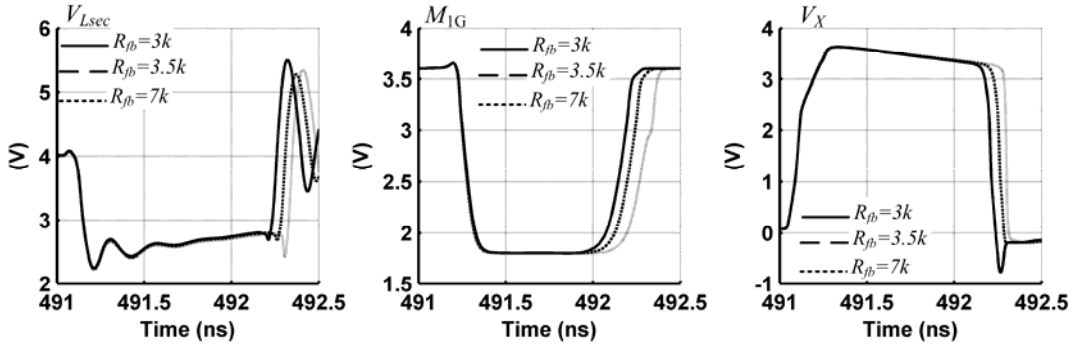

Figure 4-11: Fine adjustment of the M_{1G} duty-cycle via the feedback resistance R_{fb} (a) input voltage of the Pulse-Forming Block (b) M1G signal (c) effect on the VX node voltage.

Figure 4-11 shows a fine-tuning of the duration of the M_{1G} signal via R_{fb}. Shorter time duration is achieved with smaller R_{fb} resistor. A pulse duration that is shorter than optimum causes body-diode conduction (respectively efficiency loss). The body-diode conduction is seen as a negative pulse around the high-to-low voltage transition in the V_X node voltage. Longer than optimum pulse duration may cause simultaneous conductions of all power transistors, leading again to deteriorated efficiency. The pulse duration, respectively the feedback resistor R_{fb}, can be adjusted electronically to achieve optimum converter performance.

Simulated conversion efficiency

The efficiency of self-triggered is calculated by equation (4-5). Where $P_{V_{BAT}}$ is the power delivered from V_{BAT} source and $P_{V_{BAT\_2}}$ is the power delivered from V_{BAT_2} source. The output power, P_{out}, is the power consumed by the load resistor. The simulation parameters and results are given in Table 4-2.

$$\eta = \frac{P_{out}}{P_{V_{BAT}} + P_{V_{BAT\_2}}} \times 100\% \qquad (4\text{-}5)$$

Table 4-2: simulation parameters and results (without parasitics of converter)

V_{BAT} (V)	V_{BAT_2} (V)	R_L (Ω)	f_s (MHz)	Duty-Cycle (PMOS) (%)	t_{HL} (ps)	t_{LH} (ps)	η (%)	I_o (mA)	V_{out} (V)
3.6	1.8	15	360	52	~300	~50	65.4	100	1.5

5 Layout Design

Cadence generic process kit 45nm was used to implement self-triggered buck DC-DC converter. Cadence Assura RCX is used to take care of the Layout Versus Schematic (LVS) and Design Rule Check (DRC) [13]. Parasitic extraction is performed using Cadence Assura RCX.

5.1 Layout design guidelines

While designing Floor plan and Layout the following points were taken into account.

- Try to make the structure as symmetric as possible.
- V_{Bat} , $V_{Bat/2}$,N_{drive} and V_{SS} paths, connections between switching node and output filter, should be as short as possible
- Wires should be wide enough to carry the high current flowing through the converter. Multiple metal layers are used to achieve small series resistance if necessary
- The number of through-hole vias used for interconnection between different metal layers should be as large as possible
- Decoupling capacitor should be well shaped to fit the converter design
- The shape of output decoupling capacitor is made close to a square to achieve smaller series resistance, which corresponds to higher quality factor
- Distance from the clock signal pin to the buffer drivers should be arranged in such way that the timing errors caused by the propagation delay are as small as possible

5.2 Floor plan

Figure 5-1 depicts the floor plan of the layout design for the proposed converter. It shows the relative sizes and positions of the power transistors, transformer, pulse forming circuit and decoupling capacitors as well as their interconnections. The transformer is placed on the right side of the power transistors. The power stage block contain power transistors, pulse forming block and gate drivers. Thus, the routings between the power stage, transformer and output capacitor are kept minimized. The overall layout structure is a rectangular block with I/O pins on the both sides.

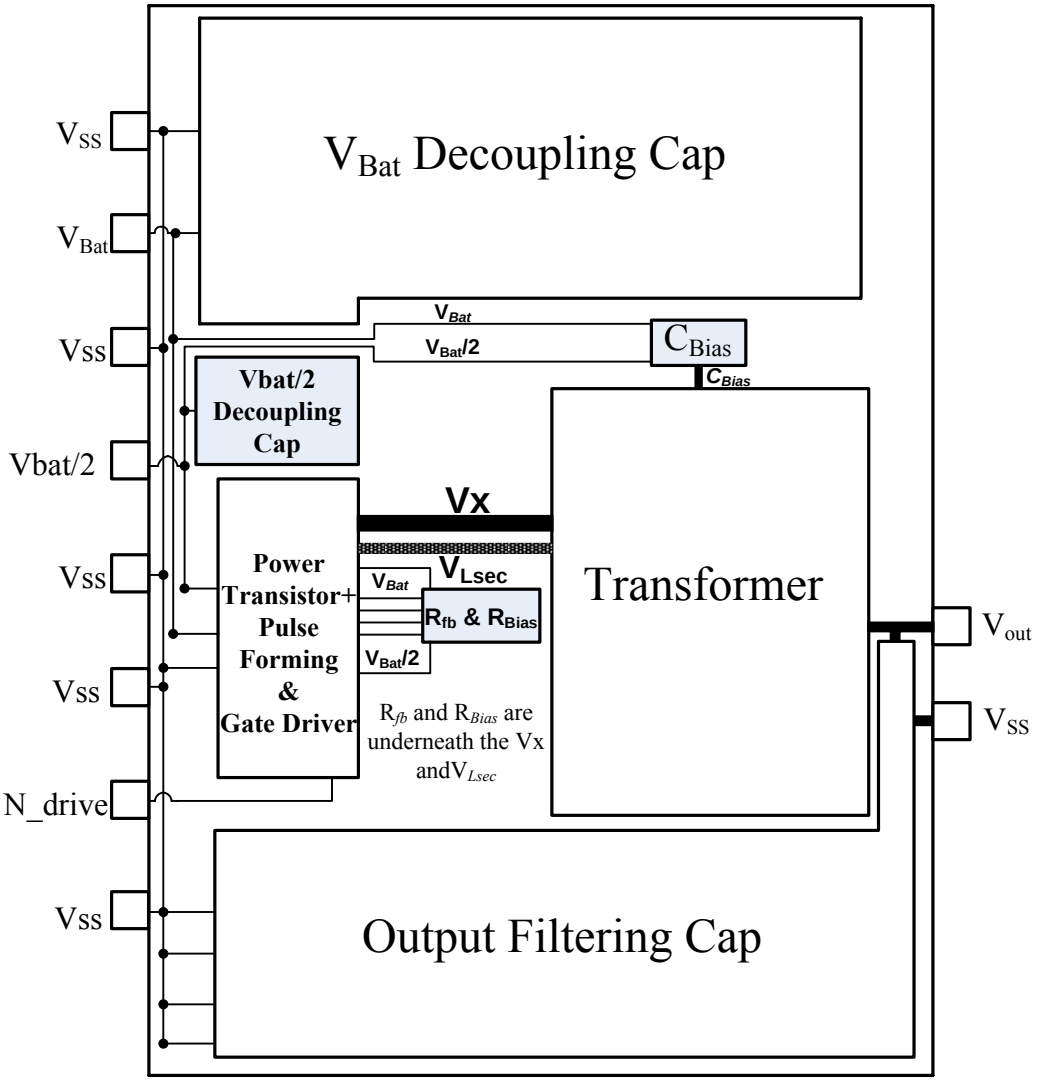

Figure 5-1: The floor plan of proposed converter. I/O pins are placed on both sides and power stage is surrounded by transformer and decoupling capacitors to minimize their interconnections.

5.3 Layout design

Although the transformer and decoupling capacitors consume most of the silicon area, their layout design procedures are relatively simple compared to cascoded power transistors, NMOS gate drivers and pulse forming circuit. However, the layout is constructed with bottom to top hierarchal style. First implement the Unit-Cell of every block and then combine all blocks. Due to this, the design becomes simple and easy to debug. The transformer layout is generated with Virtuoso Passive Component Designer (VPCD). The primary and secondary windings are generated separately with VPCD and combine in one block. The pulse forming circuit is distributed in different blocks, feedback and biasing resistor have separate block, bias capacitors block and pulse forming buffer block.

Total size of high-side PMOS cascoded transistor is 3675µm each. A segment of cascoded PMOS transistor is shown Figure 5-2. Both PMOS transistors have seven

identical fingers with 1.25µm widths. By dividing 8.75µm transistor into seven fingers, the overall gate resistance is effectively decreased.

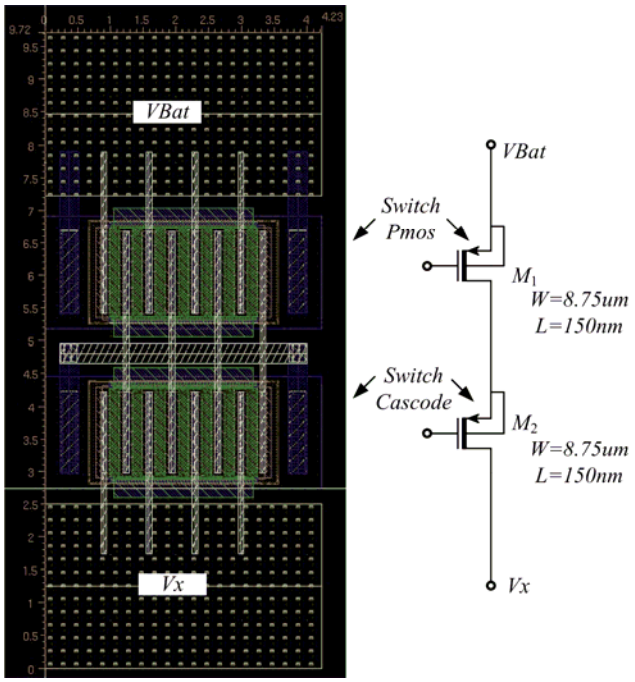

Figure 5-2: A segment of cascaded Pmos transistors. The size is 4.23x9.7 [umxum].7 fingers with 1.25um width are used for each transistor to decrease the gate resistance. The interconnections between cascaded Pmos transistors are minimized by putting both of them in one segment.

Figure 5-3 shows a cell of cascoded PMOS transistors. It consists of 21 identical PMOS segments (see Figure 5-2). The pulse forming buffer and feedback transistor M_{fb} is placed at the bottom of each PMOS block to decrease the distance between them. Therefore, the parasitic resistances of the interconnections are decreased. The whole cascoded PMOS transistor consists of 4 blocks like shown in Figure 5-3, resulting in an overall width of PMOS sided transistors (include cascade and switching transistor) 8.75µm×21×5×4 = 3675µm. The drain and source of the cascode PMOS configuration, corresponding to V_X and V_{BAT} respectively, are connected with multiple metal layers to decrease the parasitic resistance. The cascoded NMOS transistors and the low-side gate driver are designed in similar manner shown in Figure 5-4 and Figure 5-5. The total size of low-side NMOS cascoded structure is 1837.5µm each. As a result overall width of structure is 8.75µm×21×5×2 = 1837.5µm.

The layout of the power transistor stage with NMOS side gate drivers and pulse forming buffer and feedback transistor M_{fb} is shown in Figure 5-8. The size of the upper picture in Figure 5-8 is tuned to match its size in the floor plan. The zoomed view is depicted in the lower picture. Pins V_{BAT}, V_{SS}, $V_{\mathrm{BAT}}/2$ DC voltages and N_{drive} PWM signal will be connected from the left side and V_X path is placed on the right side to ease the connection with the transformer. To increase the capacitance between V_{BAT} (and $V_{\mathrm{BAT}}/2$) and V_{SS}, they are stacked over each other. V_{BAT} is placed on metal layer M11, M10 layer, $V_{\mathrm{BAT}}/2$ on M9 and M8 Layer and V_{SS} on M7, M6 and M8. The NMOS

driving signal is placed on M8 to decrease the capacitance from V_{SS} and other signals. To decrease the resistance capacitance at V_X, top metal layers are used.

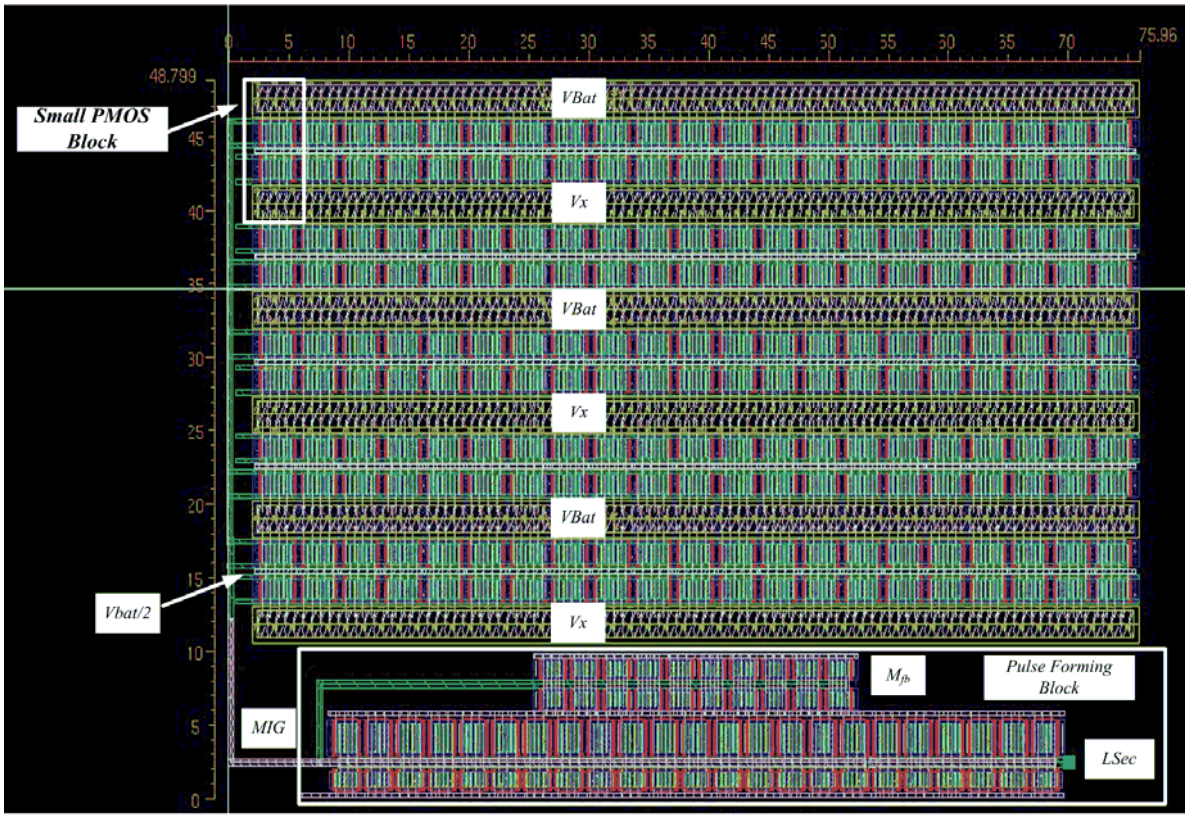

Figure 5-3: A unit cell of cascoded PMOS transistor with enabled pulse forming buffer and feedback transistor M_{fb}. It consists of 21 identical PMOS segments, which makes an overall transistor width of 183.5µm. The overall size is 48×75 [µm×µm]. The pulse-forming buffer is place under each transistor cell to minimize their interconnections.

The feedback and biasing resistor and biasing capacitor blocks are shown in Figure 5-6and Figure 5-7 respectively. The resistor block includes resistors for each PMOS cascoded block. The terminals A1, B1, C1 and D1 will connect to each pulse forming feedback transistor M_{fb}. V_{BAT} and $V_{BAT}/2$ are supply voltage of pulse forming circuit. V_{Lsec} is input of the pulse forming circuit. V_{Lsec} is also connected to biasing capacitors shown in Figure 5-7. For the biasing capacitors centroid layout technique is used. Each biasing capacitor divided into 2 blocks and palace in cross manner.

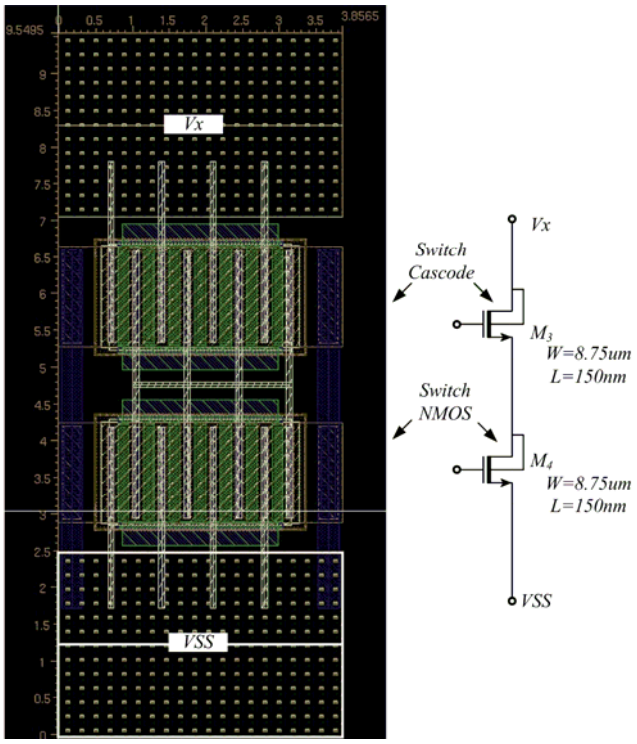

Figure 5-4: A segment of cascaded Pmos transistors. The size is 3.8x9.5 [umxum].7 fingers with 1.25um width are used for each transistor to decrease the gate resistance. The interconnections between cascaded Pmos transistors are minimized by putting both of them in one segment.

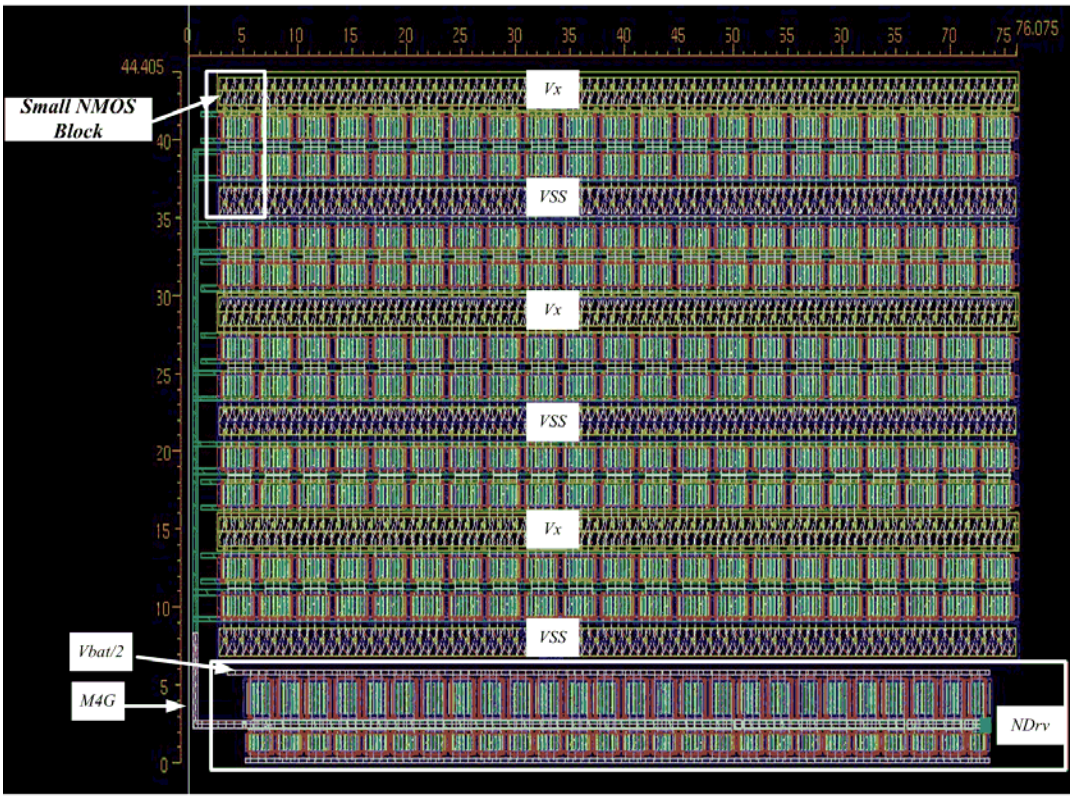

Figure 5-5: A unit cell of cascoded NMOS transistor with enabled gate driver. It consists of 21 identical PMOS segments, which makes an overall transistor width of 183.5µm. The overall size is 44×76 [µm×µm]. The gate driver is place under each transistor cell to minimize their interconnections.

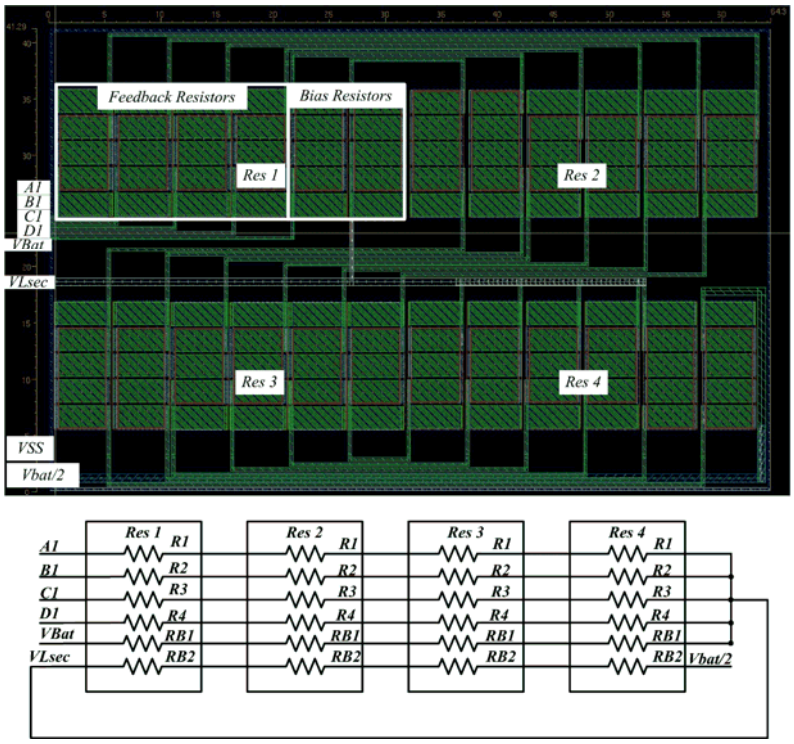

Figure 5-6: Feedback and Biasing Resistors of pulse forming circuit. It consists of 4 blocks one for each block of the cascoded PMOS.

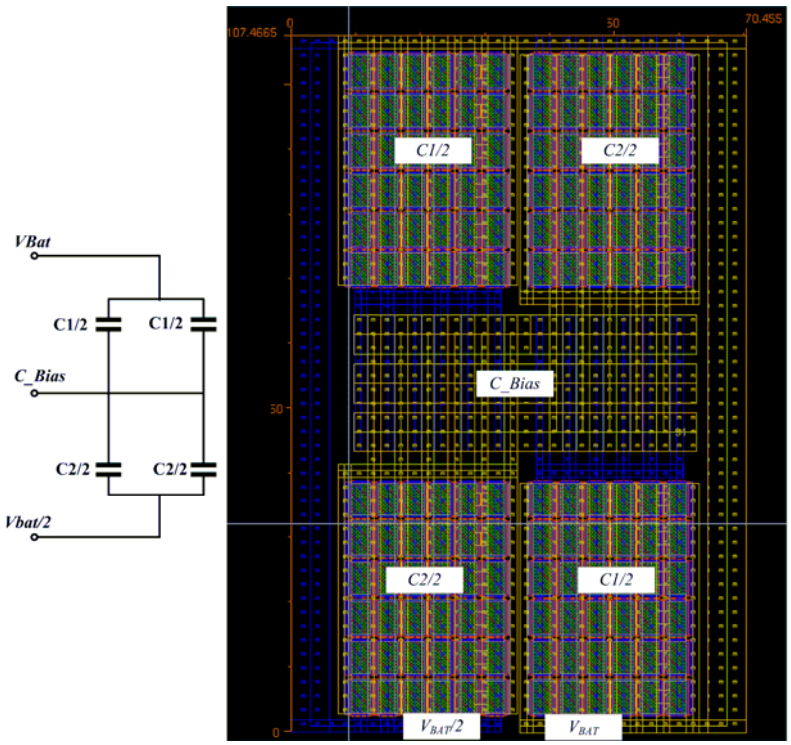

Figure 5-7: Biasing Capacitors of pulse forming circuit. Layout is formed in common centroid style.

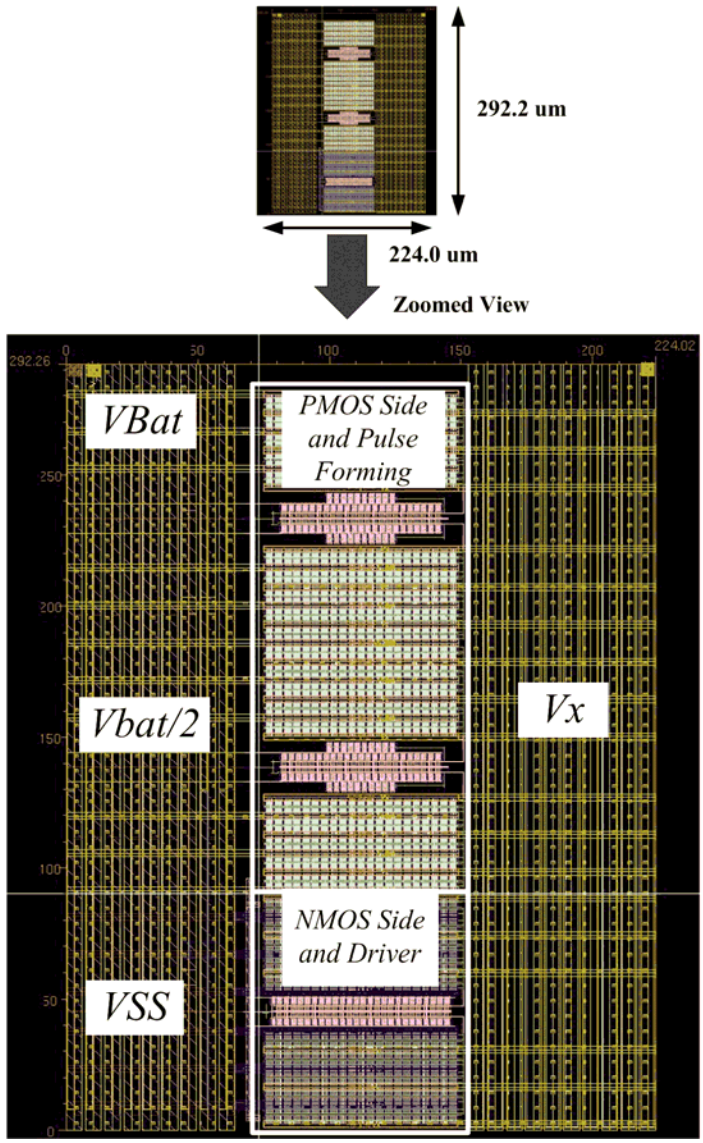

Figure 5-8: Power stage of proposed self-triggered converter. The upper picture shows the size of the power stage in the floor plan and the lower picture shows its zoomed view. The PMOS transistor consists of 4 unit PMOS transistor cells, resulting in a total transistor width of 3.675mm. The NMOS transistor has 2 unit NMOS transistor cells, which makes a total transistor width of 1.8375mm The overall size of the power stage is 224×292 [µm×µm].

In the decoupling capacitor layout design, the concept of Unit-Cell capacitor is implemented. Each unit PMOS capacitor cell, shown in Figure 5-9, consists of 100 PMOS transistors with 10µm widths and lengths, resulting in a total capacitance of 95pF. The output decoupling capacitor is made of 42 such cells, yielding an overall capacitance of 3.99nF. The 1.5nF input decoupling capacitor consists of 2 series connected 3nF PMOS capacitors, which helps to tolerate a maximum input voltage of 3.6V.

It is very difficult to make transformer of the specifications given Table 2.2 with VPCD the whole model of transformer is designed in FastHerny and FastCap but FastHenry do not have exporting GDSKII format file (that Layout Editor support) application. We already know the dimensions of each winding so Virtuoso Passive

Component Designer (VPCD) is used to generate the each winding separately and then combine in one block. The primary inductor has 80µm track width with 10µm space of between adjacent turns. Its inner radius is 200µm. It has 2.5, which minimizes the path from power transistors to the output pin. Multi-layer configuration including top metal layers M10 and M11 is used to build the metal track and M9 is used as the bridge. The secondary inductor has 20µm with 78µm spacing between adjacent turns. It has 1.25 turns, which makes pins are shifter in 180degree. Metal layer M5 and M6 are used for winding and M4 for bridge. The size of the transformer is 1037×844 [µm×µm].

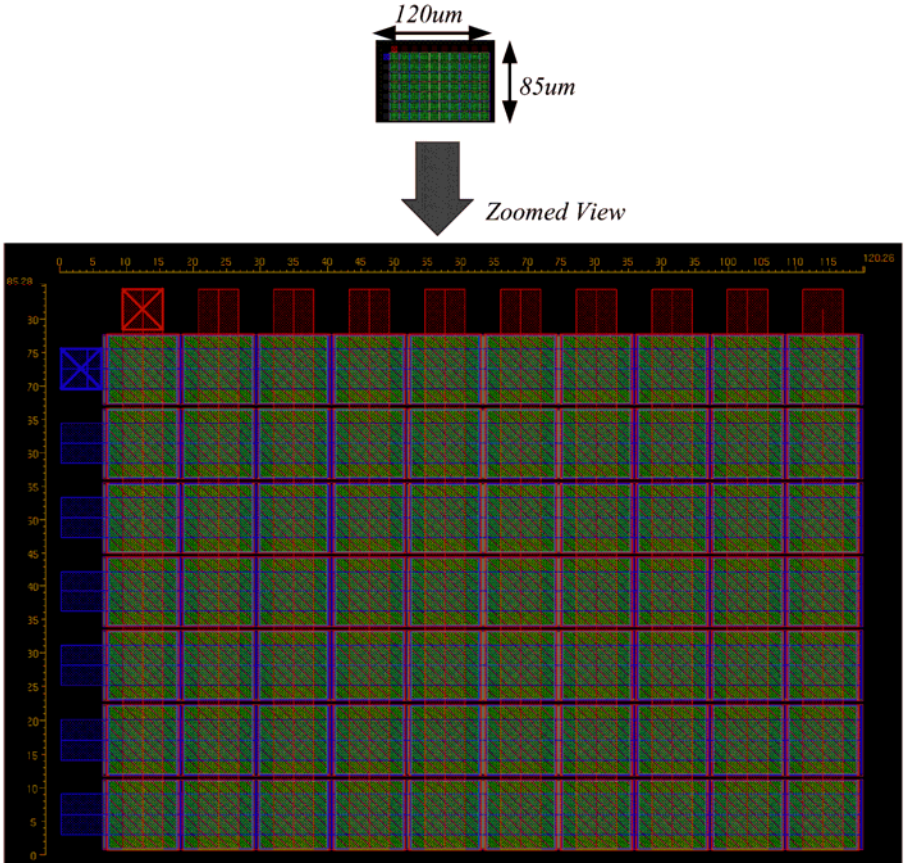

Figure 5-9: A unit cell of PMOS capacitor. The upper picture shows the size of the unit capacitor cell in the floor plan and the lower picture shows its zoomed view. The unit cell consists of 100 PMOS transistor with 10µm gate width and 10µm gate length, which gives a total capacitance of 95pF. The overall size of the unit PMOS capacitor cell is 120×85 [µm×µm].

The top layout is designed according to the floor plan. Multiple metal layers are used in the interconnections to decrease the parasitic resistance. Input, driving signals, and biasing voltage pins are placed on the left side. Output is taken from the right side to minimize the distance between the inductor and the load pins. The final layout of the proposed converter is shown in Figure 5-11. It consumes a total silicon area of 1.72×2.67 [mm×mm].

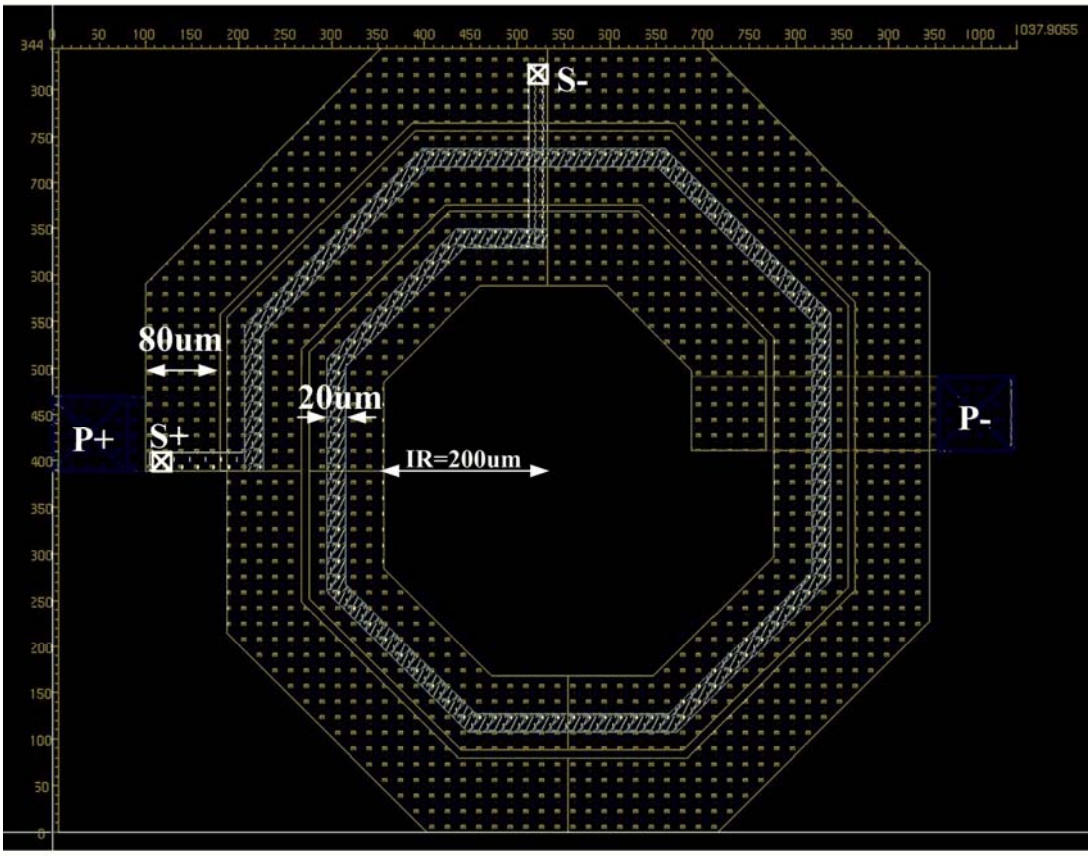

Figure 5-10: the transformer generated by Virtuoso Passive Component Designer. The metal width is 80µm with 10µm distance between adjacent turns. The number of turns is set to 2.5 so that its pins are shifted by 180 degrees, which minimizes the interconnections between the primary inductor and the output pin. The secondary winding has 20µm with 78µm sapacing between adjacent trace.The overall transformer layout size is 1037×844 [µm×µm].

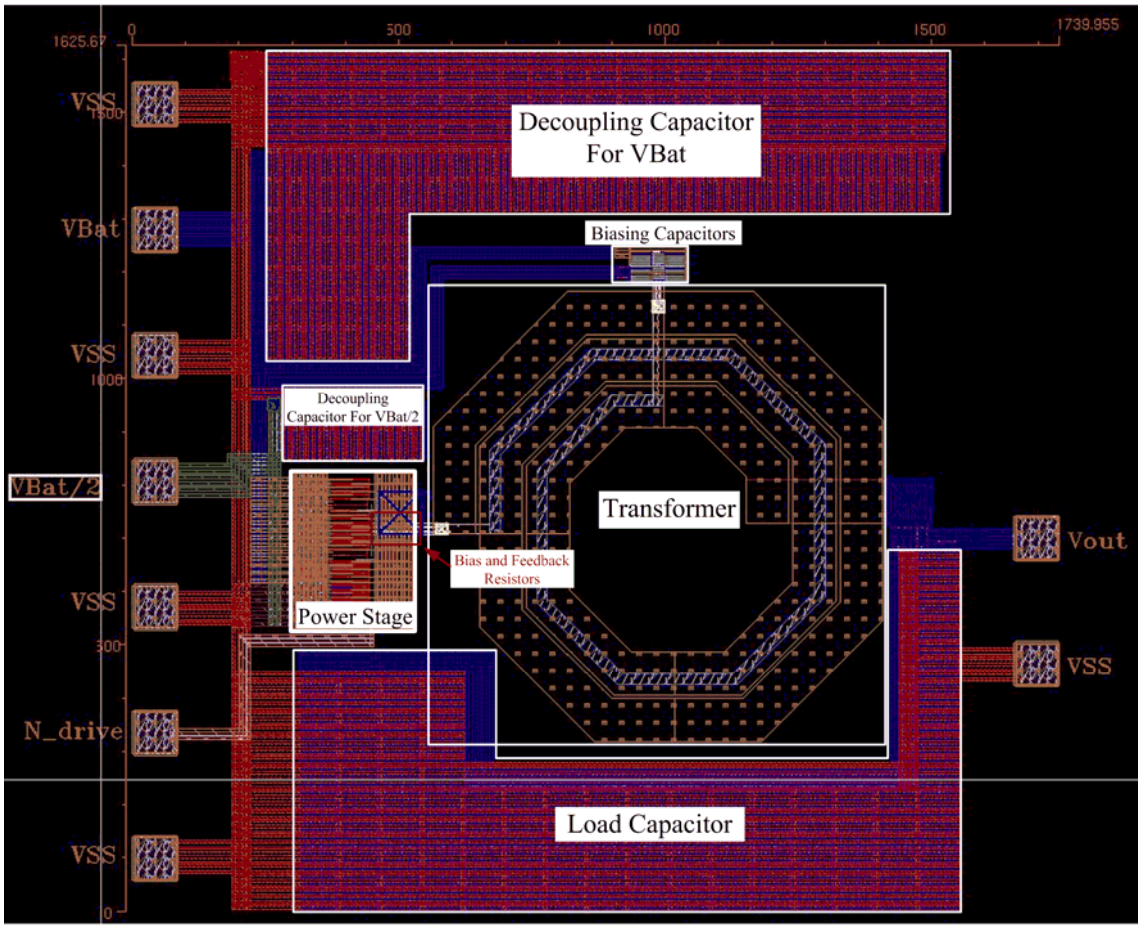

Figure 5-11: Layout of proposed synchronous buck converter. It is designed according to the floor plan. Input, driving signals, and biasing voltage pins are placed on the left side. Output pin is placed on the right side to minimize the distance between the inductor and the load. The overall converter consumes a total silicon area of 1.739×1.625 [mm×mm]

6 Measurement Setup and Post-Layout Simulations

The measurement setup of self-triggered buck converter is proposed in this chapter including all PCB and measurement instrument parasitics. The driving PWM signal is generated externally to control the output voltage regulation. Because, we only proposed the power stage of converter, not control circuitry of the converter. Agilent pulse generator 81134A is needed to provide the PWM control signal N_{drive}. Regarding the bias voltages, LM38511 linear regulator is utilized to produce $V_{BAT}/2$ voltage from a DC voltage source. The load consists of 6 parallel connected EIA standard resistors with tolerance of 1%.

6.1 Load resistor calculations

The resistor combinations, shown in Table 6-1, utilizing 39Ω and 47.5Ω resistors, are used as load for self-triggered converter. In this way, the proposed converter could be measured in a wide range of output current. Figure 6-1 shows an example of six resistors connected in parallel to realize a load resistance of ~12Ω, which corresponds to an output current of 125mA at V_{out}=1.5V.

Table 6-1: Load resistor combinations

Resistor	Overall resistance	Output Current (V_{out}=1.5V)
47.5//47.5	23.75Ω	62.5mA
39//47.5	21.41Ω	70mA
39//39	19.5Ω	79mA
47.5//47.5//47.5	15.83Ω	95mA
47.5//47.5//47.5//47.5	11.875Ω	126mA

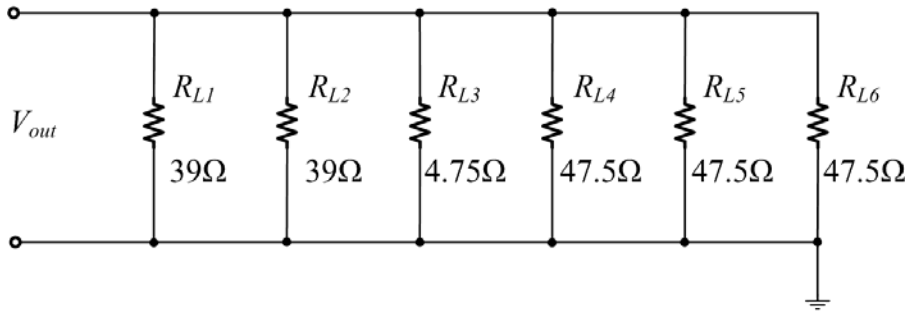

Figure 6-1: Circuit of load resistors

6.2 LDCL015 voltage regulator for biasing

Linear voltage regulator LDCL015 IC is used to generate the desired bias voltage. A typical application circuit of such regulator is shown in Figure 6-2. The output voltage

V_o is determined by the resistance ratio between R_1 and R_2. R_{var} is used to tune the output voltage by varying this resistance ratio.

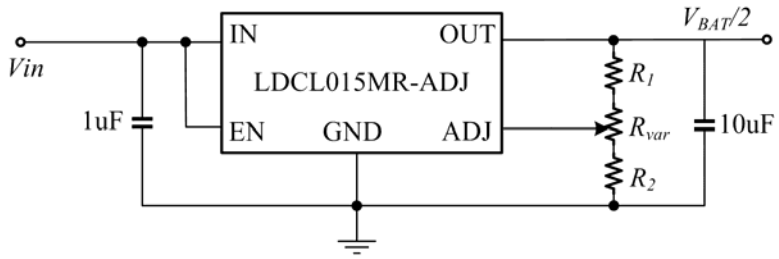

Figure 6-2: Application of LDCL015 voltage regulator

When the input voltage varies from 2.25V-5.5V, the output voltage is given as:

$$V_o = V_{ADJ} \times (1 + \frac{R_1}{R_2}) \qquad (6.1)$$

Where V_{ADJ} = 0.8V. It is recommended to use resistors with values in the range of 10kΩ to 50kΩ. Lower values can also be suitable, but will increase current consumption. Based on (6.1), the calculations are done for 1.5 to 1.8V, for battery voltage. Table 6-2 gives the calculated values for R_1, R_2 and R_{var} as well as the corresponding output voltage range.

Table 6-2: Bias voltage calculations

V_o (V)	R_1 (Ω)	R_2 (Ω)	R_{var} (Ω)	Voltage range (V)
1.8	12.75K	8.98K	0-1.2K	1.5-1.8

6.3 Measurement setup

An example of measurement setup for efficiency and output voltage ripple measurement is shown in Figure 6-3. The components in blue colour are parasitics of instruments and PCB traces. The converter pin descriptions are given by Table 6-3.

Table 6-3: Descriptions of converter pins

Pin name	Description
V_{BAT}	Input voltage pin
V_{out}	Output voltage pin
V_{SS}	Ground pin
$V_{BAT}/2$	Cascode bias voltage, N-driver VDD, P-driver VEE
N_{drive}	Ground voltage pin for PMOS gate-drive buffer

Table 6-4 gives the electrical characteristics of the proposed converter. The maximum input voltage is 3.6V and maximum output current is 125mA. Bias voltage should be adjusted according to the input voltage level.

Table 6-4: Electrical characteristics of the proposed converter

Symbol	Min	Typ	Max	Unit
V_{BAT}	3	3.6	3.6	V
$V_{BAT}/2$		$V_{BAT}/2$		V
V_{out}		1.5		V
$\Delta V_{out}/V_{out}$			10	%
I_{out}	62.5	100	125	mA
R_{fb}	2k	3.5k	20k	Ω
Switching frequency	-	360	-	MHz

The synchronous control signals are generated by Agilent pulse generator 81134A and fed with two phase matched cables. Output voltage ripple is measured by an oscilloscope and efficiency can be calculated by calculating the input and output power. Different output current can be achieved by modifying the load resistor combination.

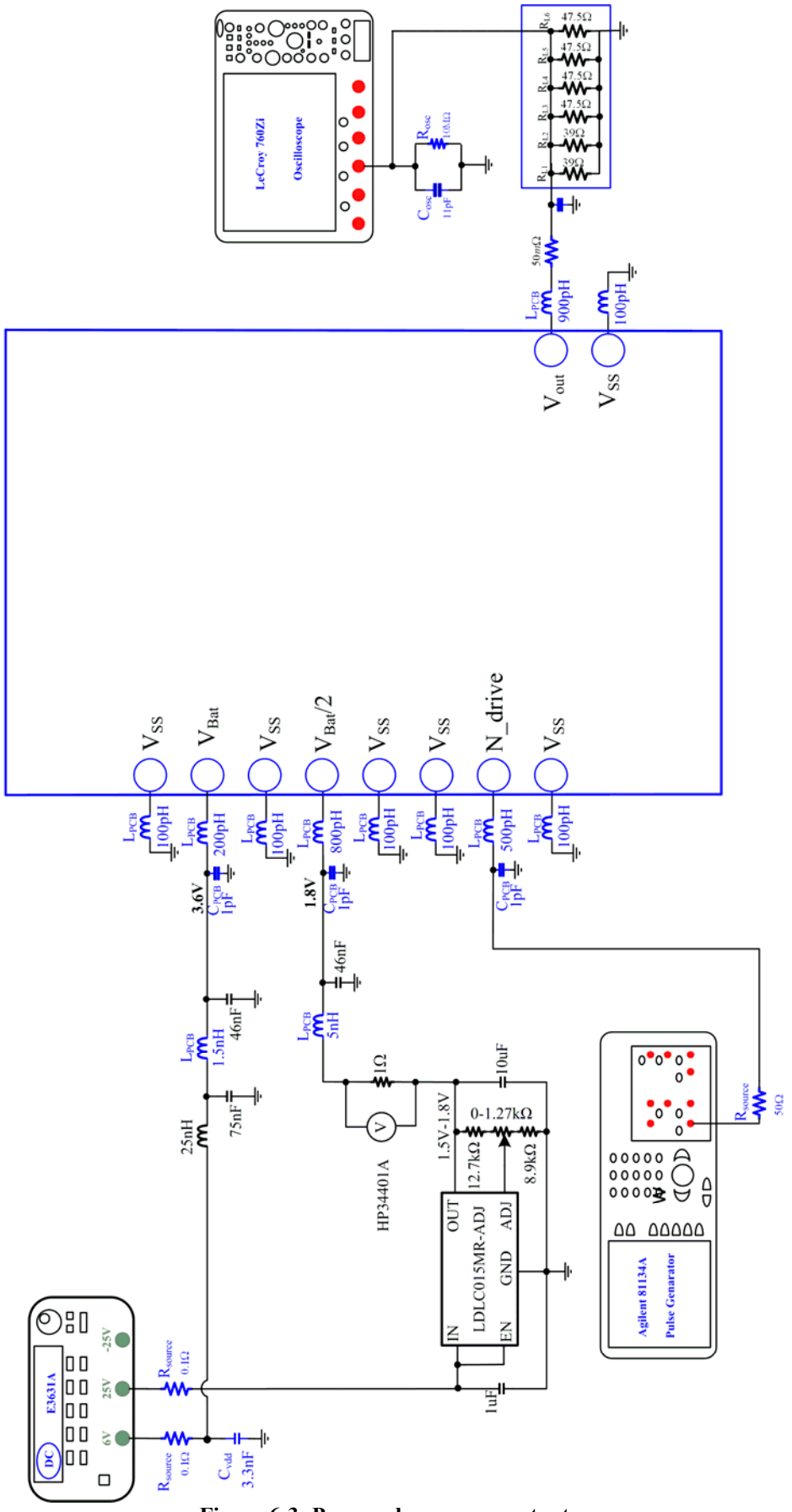

Figure 6-3: Proposed measurement setup

6.4 Post-Layout Simulations

The simulation results are shown in section (4.6), are without on-chip decoupling capacitors and major Parasitics (PCB, IC Pads and layout). In order to see behavior of converter in the presence of all possible Parasitics around the circuit are included and run post layout simulations. In addition, on-chip decoupling capacitors are connected with V_{BAT} and V_{BAT_2} to reduce the supply fluctuation. The simulation test bench used for post-layout simulations is shown in Figure 6-3.The simulated waveforms are given in Figure 6-4. In post-layout simulation, the dead-time (t_{LH} and t_{HL}) are adjusted same as without Parasitics simulation (shown in Table 4-2) by fine tuning of feedback resistor R_{fb}.

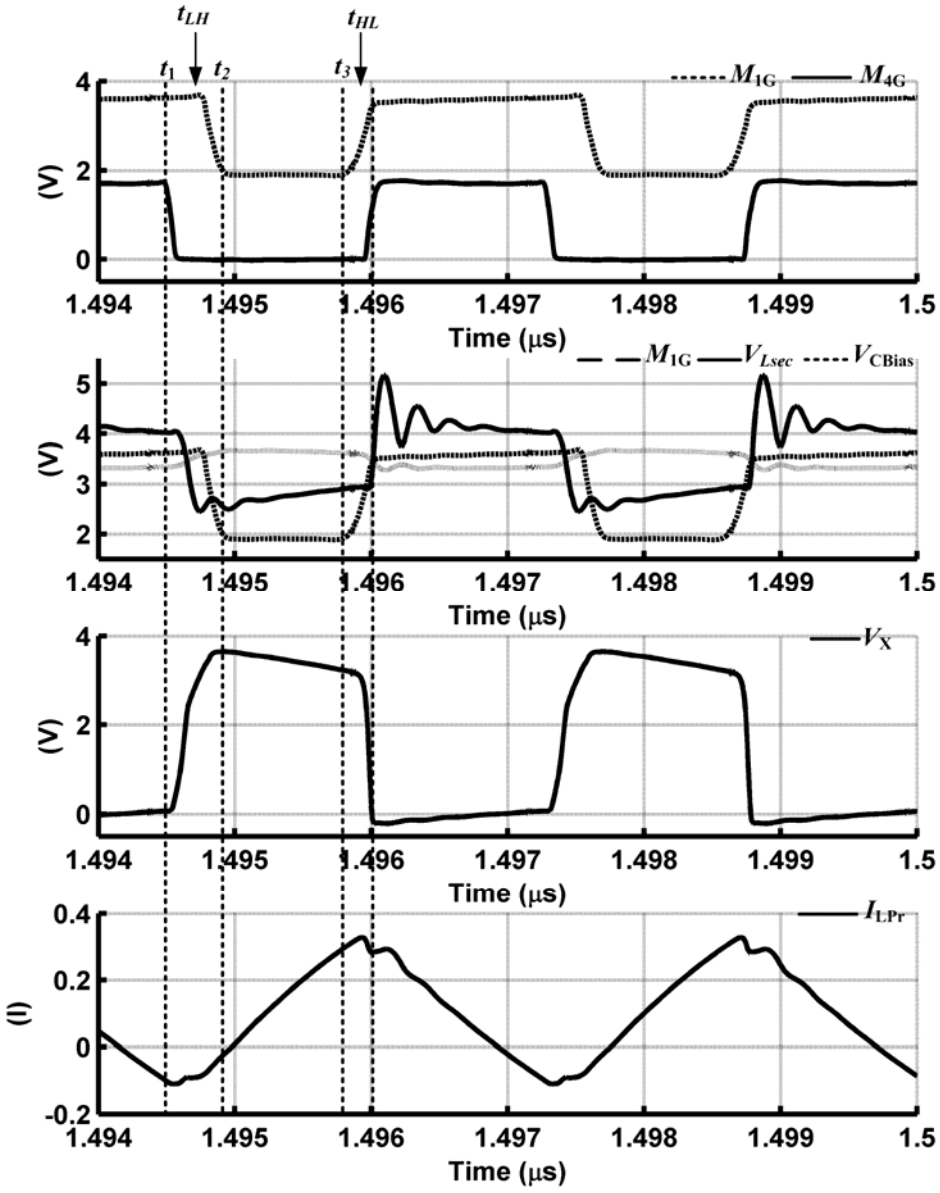

Figure 6-4: simulated waveform of converter with all Parasitics.

Line Regulation

For Line regulation simulations, same simulation test bench is used in Figure 6-3 and result is shown in Figure 6-5. Input voltage V_{BAT} change from 3-3.6V and keep the

voltage V_{out} = ~1.5V, I_o = ~100mA and V_{BAT_2} = V_{BAT}/2 at switching frequency 360MHz. By changing the input voltage of Converter the bias point V_{CBias} is changed, with this, dead-time of converter will change. To keep the dead-time same for all variations in supply voltages R_{fb} is adjusted manually.

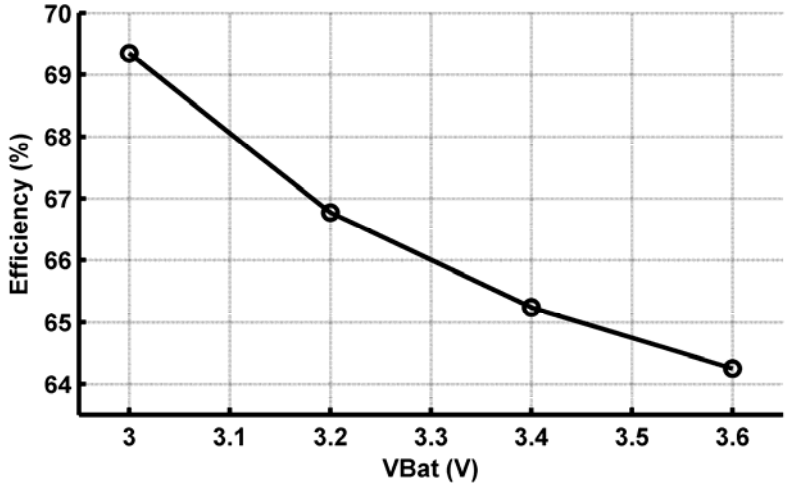

Figure 6-5: Line regulation of Self-triggered DC-DC Converter. (V_{BAT} = 3-3.6V, f_s = 360MHz, R_L = 15Ω)

Load Regulation

For load regulation simulation given in Figure 6-6, R_L changed from 12 -24Ω, while keeping the output voltage ~1.5V and input voltage 3.6V. Out of this R_L range, the converter is not working properly, because below 12Ω the duty-cycle require to get 1.5V at output is very low that dead-time will not same. Above the 24Ω, feedback resistor R_{fb} gets out of range mentioned in Table 6-4.

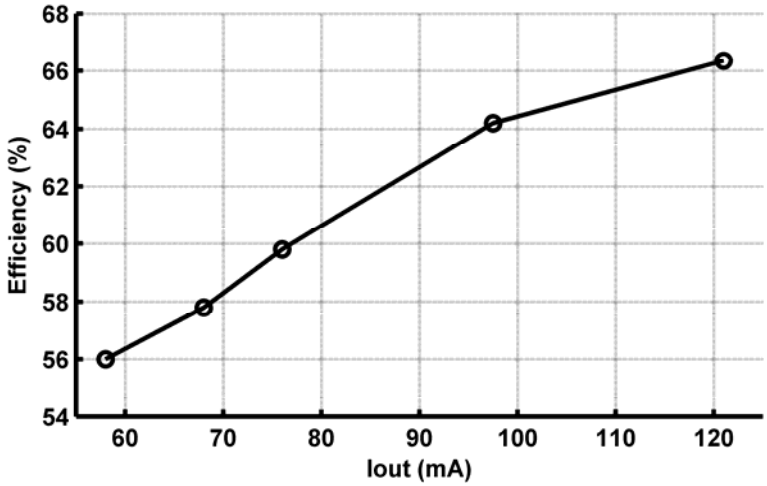

Figure 6-6: Load Regulation of Self-triggered DC-DC Converter. (V_{BAT} = 3.6V, f_s = 360MHz, R_L = 15Ω)

Comparison between Standard Buck Converter

A comparison between the efficiency achieved by the standard buck converter (in hard- and soft-switching operation) and the self-triggered converter is shown in Figure 6-8 as a function of the output current. The standard converter uses the same switching

frequency, the same load and input voltage conditions, the same active devices and passive components. No level shifters are included in the simulations of the standard buck converters shown in Figure 6-7 . Dead times (t_{HL} and t_{LH}) of 30ps are introduced between the driving signals in order to avoid short-circuit losses in the hard-switching converter. In the soft-switching converter, t_{LH} is increased to 300ps in order to allow the V_X parasitic capacitor to be charged by the negative inductor current in ZVS fashion.

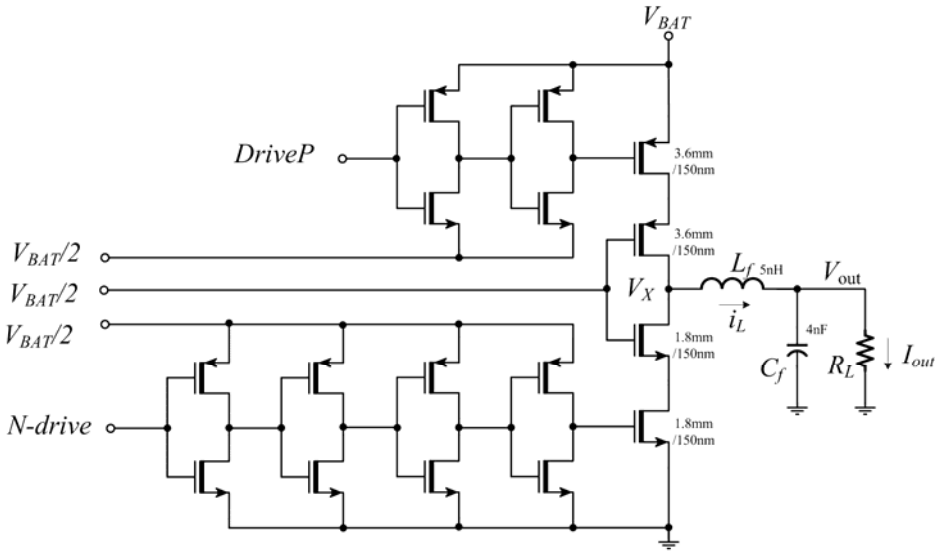

Figure 6-7: Standard Buck Converter Schematic.

The efficiencies of the three converters and the losses in different building blocks are summarized in Table 6-5, where "*Transformer*" denotes the dissipated losses in main L_{pr} and auxiliary feedback winding L_{sec}. On the other hand, L_f denotes losses in output filter inductor of standard buck converter. Furthermore, "*P-driver*" denotes the losses in the high-side driver for the standard buck converter and the losses in the pulse-forming block for the self-triggered architecture while, "*N-driver"* denotes losses in low-side driver.

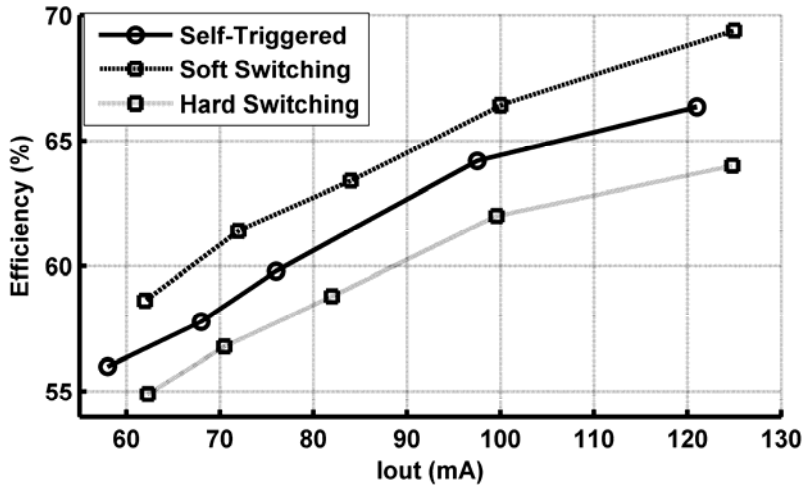

Figure 6-8: Efficiency comparison between hard-switching buck converter, Soft-switching buck converter, and Self-Triggered converter (V_{BAT} = 3.6V, f_s = 360MHz, R_L = 15Ω)

The proposed self-triggered converter has slightly higher efficiency ($\Delta\eta$~0.5-1%) than the hard-switching buck converter, even when the level-shifter losses are not taken into account for standard buck converter. Although the level shifter does not need to handle large power, the high switching frequency and the required short propagation delay may result in high current consumption. Thus, the inclusion of the level shifter power consumption would further underline the advantages of the self-triggered converter. The self-triggered topology requires no additional blocks and power consumption, which will make the topology even more competitive when all losses of the standard buck converter are included.

Table 6-5: POWER LOSS comparison between the converters for V_{out} = ~1.5V and f_s =360MHz.

Parameters	Hard-Switching	Soft-Switching	Self-Triggered
V_{out}	1.499V	1.50V	1.52V
M_1-M_2	24.95mW	14.64mW	16.79mW
M_3-M_4	12.55mW	9.69mW	9.22mW
L_f	25.62mW	24.62mW	-
Transformer	-	-	29.07
N-driver	5.80mW	5.85mW	5.71mW
P-driver	12.74mW	12.60mW	14.31mW
η	63.21%	66.99%	64.25%

7 Conclusion and Discussion

This work addresses two issues of cascoded DC-DC buck converter, short circuit current losses and voltage level shifter losses and delays. In order to solve them, a cascoded output power stage with dead-time generation and inductive feedback for driving high-side PMOS is proposed. An inductive feedback scheme is proposed in order to transfer driving signal for high-side PMOS. Inductive feedback provides fast response and consumes less power, which is coherent with the high-frequency DC-DC converter. Additionally, pulse forming block generates the dead-time (DTHL and DTLH) to achieve ZVS. The main achievements of this thesis are depicted as below:

1. Reduced power loss and remove timing delays uncertainties associated with the voltage level shifter, which leads to higher achievable efficiency.
2. Voltage regulation is realized with smooth regulation of the duty-cycle supplied to the NMOS switching devices or by changing the feedback resistance R_{fb} (improvement in comparison to the self-oscillating converter),
3. Simple transformer used in the feedback, no good quality factor is required for the secondary winding, thus integration on silicon is feasible.

In proposed converter, fine adjustment of the duty-cycle of high-side PMOS transistor requires change in feedback resistor R_{fb} value. However, to tune R_{fb} resistor electronically needs a feedback control to achieve optimum converter performance. Other drawbacks of proposed converter are resistors and capacitors used for biasing secondary coil. Although, biasing capacitors are small, still consume large space and using resistors on silicon is not good idea. Resistors on silicon have tolerance of about 15- 30%.

Tuning of R_{fb} resistor electronically could be solve by using technique reported in [37]. It generates the dead-time (DTHL and DTLH) by monitoring the mid-point node voltage of high-side PMOS and low-side NMOS cascaded transistor. The driving signals for high-side PMOS and Low-side NMOS are generated synchronously.

To overcome Bias problems, secondary coil biasing should use active components (transistors) instead of capacitors and resistors. Secondary coil is biased with two diode-connected NMOS transistors. In addition, the biasing transistors require less space and problem of resistors matching is resolved. The implementaion of this work is discussed in the Appendix-II.

REFRENCES

[1] M. Wens, and M. Steyaert, "Design and implementation of fully-integrated inductive DC-DC converters in standard CMOS," in *Analog Circuits and Signal Processing*, Springer Science+Business Media B.V., 2011.

[2] Kursun, V.; Schrom, G.; De, V.K.; Friedman, E.G.; Narendra, S.G., "Cascode buffer for monolithic voltage conversion operating at high input supply voltages,"*proc. IEEE Int. symp. Circ. And Syst. 2005, Vol. 1*, pp.464-467

[3] C. Yoo, "A CMOS buffer without short-circuit power consumption," *IEEE Trans. Circuits and Systems II: Analog and Digital Sig. Proc.*, vol.47, no.9, pp.935-937, Sep 2000.

[4] C. F. Lee and Mok, P.K.T., "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE J. Solid-State Circuits,* vol.39, no.1, pp.3-14, Jan 2004.

[5] A. Fomani and W. Ng, "A segmented gate driver with adjustable driving capability for efficiency optimization," *in IEEE inten. Power Electronics Conference (IPEC),* pp.1646-1650, 2010.

[6] T. V. Breussegem, and M. Steyaert, "CMOS Integrated Capacitive DC-DC Converters." *In Anlalog Circuits and Signal Processing*, Springer Science+Business media., 2013.

[7] FastHenry User's Guide, Version 3.0, Sep.1996 [Online] Available: http://www.fastfieldsolvers.com/.

[8] FastCap User's Guide, Version 3.0, Sep.1996 [Online]Available: http://www.fastfieldsolvers.com/

[9] E.Di Lorenzo "The Maxwell Capacitance Matrix",[online]Available: http//www.fastfieldsolver.com

[10] Kehrer. D "Design of Monolithic Integrated Lumped Transformers in Silicon-based Technologies up to 20 GHz" Msc Thesis, Technical University Wien Austria, Dec 2000.

[11] Chandrakasan AP, Brodersen RW.Low Power CMOS Digital Design.Kluwer Academic: Norwell, MA, 1995.

[12] Wang C-C, Wu J-C. Efficiency improvement in charge pump circuits.IEEE Journal of Solid-State Circuits.1997 June; 32 (6): 852–860

[13] GPDK 45nm mixed signal process spec, June 18, 2011

[14] M. Chen and G.A.Rincon-Mora, “Accurate, compact and power-efficient Li-ion battery charger circuit,” in IEEE Trans. On Citcuits and Systems II, Exp Briefs, pp. Vol.53, No.11, 2006.

[15] Steyaert, M.; Van Breussegem, T.; Meyvaert, H.; Callemeyn, P.; Wens, M., "DC-DC converters: From discrete towards fully integrated CMOS," *ESSCIRC (ESSCIRC), 2011 Proceedings* , pp.42,49, 12-16 Sept .

[16] Wens, M.; Cornelissens, K.; Steyaert, M., "A fully-integrated 0.18µm CMOS DC-DC step-up converter, using a bondwire spiral inductor," *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European* , pp.268,271, 11-13 Sept.2007

[17] Wens, M.; Steyaert, M., "A Fully Integrated CMOS 800-mW Four-Phase Semiconstant ON/OFF-Time Step-Down Converter," *Power Electronics, IEEE Transactions on* , vol.26, no.2, pp.326,333, Feb. 2011.

[18] Broussev, S.S.; Tchamov, N.T., "Two-Phase Self-Assisted Zero-Voltage Switching DC–DC Converter," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.60, no.3, pp.157,161, March 2013.

[19] C. Theron et all, “Soft Switching Self-Oscillating IGBT Based DC-DC Converters”, IEEE 2002.

[20] H. Sakamoto et all, “Self Oscillated PWM Converter with Impulse Resonant Soft-switching,” IEEE 2003.

[21] C. F. Lee, and P. Mok, “A Monolithic Current-Mode CMOS DC–DC Converter With On-Chip Current-Sensing Technique,” *IEEE J. Solid-State Circ.*, vol. 39, no. 1, pp. 3–14, Jan. 2004.

[22] Kursun V, Narendra SG, De VK, Friedman EG, “Efficiency analysis of a high frequency buck converter for on-chip integration with a dual-VDD microprocessor”. Proceedings of the IEEE European Solid-State Circuits Conference, pp. 743–746, Sept 2002.

[23] Kursun .V, Friedman, E.G “Multi-voltage CMOS Circuit Design” John Wiley & Sons 2006.

[24] Onizuka, K.; Kawaguchi, H.; Takamiya, M.; Sakurai, T., "Stacked-chip Implementation of On-Chip Buck Converter for Power-Aware Distributed Power Supply Systems," *Solid-State Circuits Conference, 2006. ASSCC 2006. IEEE Asian*, pp.127,130, 13-15 Nov. 2006

[25] Yi Chen; Yurong Nan; Qinggang Kong, "A Loss-Adaptive Self-Oscillating Buck Converter for LED Driving," *Power Electronics, IEEE Transactions on* , vol.27, no.10, pp.4321,4328, Oct. 2012

[26] Pilawa-Podgurski, R.C.N.; Sagneri, A.D.; Rivas, J.M.; Anderson, D.I.; Perreault, D.J., "Very-High-Frequency Resonant Boost Converters," *Power Electronics, IEEE Transactions on* , vol.24, no.6, pp.1654,1665, June 2009.

[27] Adami, S-E; Marian, V.; Degrenne, N.; Vollaire, C.; Allard, B.; Costa, F., "Self-powered ultra-low power DC-DC converter for RF energy harvesting," *Faible Tension Faible Consommation (FTFC), 2012 IEEE* , vol., no., pp.1,4, 6-8 June 2012.

[28] Feng-Yin Chen; Tsorng-Juu Liang; Ray-Lee Lin; Jiann-Fuh Chen, "A novel self-oscillating, boost-derived DC-DC converter with load regulation," *Power Electronics, IEEE Transactions on* , vol.20, no.1, pp.65,74, Jan. 2005.

[29] Virtuoso Multi Mode Simulation Datasheet. [WWW]. [Cited 22/5/2013]. http://www.cadence.com/rl/Resources/datasheets/virtuoso_mmsim.pdf

[30] STMicroelectronics, "LDLC015MR-ADJ datasheet"

[31] Maderbacher, G.; Jackum, T.; Pribyl, W.; Michaelis, S.; Michaelis, D.; Sandner, C., "Fast and robust level shifters in 65 nm CMOS," *Proceedings of the ESSCIRC (ESSCIRC)*, pp.195, 198, 12-16 Sept. 2011.

[32] da Rocha, J.F.; dos Santos, M.B.; Dores Costa, J.M.; Lima, F.A., "Level Shifters and DCVSL for a Low-Voltage CMOS 4.2-V Buck Converter," *IEEE Transactions on Industrial Electronics,*, vol.55, no.9, pp.3315,3323, Sept. 2008.

[33] Serneels, B.; Steyaert, M.; Dehaene, W., "A High speed, Low Voltage to High Voltage Level Shifter in Standard 1.2V 0.13µm CMOS," *13th IEEE International Conference on Electronics, Circuits and Systems, 2006. ICECS '06.* , pp.668, 671, 10-13 Dec. 2006.

[34] Maderbacher, G.; Jackum, T.; Pribyl, W.; Michaelis, S.; Michaelis, D.; Sandner, C., "Fast and robust level shifters in 65 nm CMOS," *Proceedings of the ESSCIRC (ESSCIRC)*, pp.195, 198, Sept. 2011.

[35] Takatsu, K.; Niitsu, K.; Shidei, T.; Miura, N.; Kuroda, T., "A 0.45V-to-2.7V inductive-coupling level shifter," *IEEE Asian Solid State Circuits Conference (A-SSCC),* pp.1,4, 8-10 Nov. 2010.

[36] K. Van Schuylenbergh and R. Puers, "Inductive Powering: Basic Theory and Application to Biomedical Systems, 41 Analog Circuits and Signal Processing", (Springer Science + Business Media B.V. 2009), pp. 41–76.

[37] Jing Tian, *Automatic Dead-Time Control for DC-DC Buck Converter*, M.Sc. Thesis, Tampere University of Technology, Hervanta, Finlnad, 2013.

APPENDIX-I

I.1 Theoretical Analysis

The theoretical analysis of proposed self-triggered converter is carried out with simplified model in Fig 1 and Fig 2 respectively. In Fig 1 (a) high-side and low-side power transistors are replaced with ideal switches *S*1 and *S*2. Primary winding is modeled as L_{pr} and series resistance R_p, C_f is filtering capacitor and R_L is load resistor. Secondary winding in Fig 2 is modeled as voltage controlled voltage source ($1.41K/V_{Lpr}$), leakage inductance L_{K2} and series resistance R_s [27]. C_{in} is input capacitance of pulse forming block. To make analysis simple R_{B1}, R_{B2}, C_{r1}, C_{r2}, M_{fb} and R_{fb}, are disconnected. This is because R_{B1}, R_{B2}, M_{fb} and R_{fb} are only setting the DC-bias voltage at pulse forming block input.

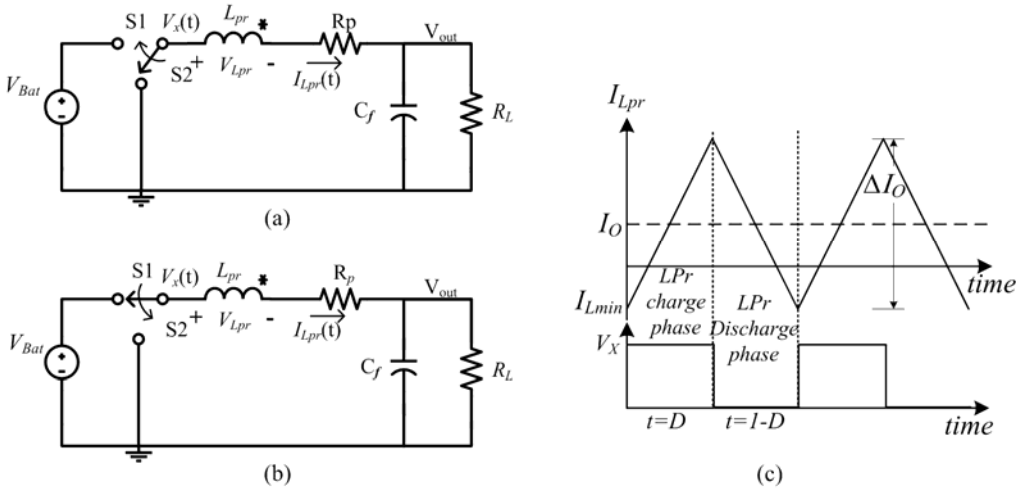

Fig 1: (a) when V_X node connected to V_{BAT} (b) when V_X node connected to Ground (c) Inductor current with input at V_X node in ZVS fashion.

At time t_1 in Figure 3-5 , the V_X node connected to V_{Bat} via *S*1 is called charge phase of inductor L_{Pr}. The second order differential equations (1) and (2) describes the equivalent charge circuit shown in Fig 1(a).

$$V_X - L_{pr}\frac{dI_{Lpr}(t)}{dt} - I_{Lpr}(t)R_p - V_{out}(t) = 0 \quad (1)$$

$$I_{Lpr}(t) = C_f\frac{dV_{out}(t)}{dt} + \frac{V_{out}(t)}{R_L} \quad (2)$$

Substitute V_{out} from equation (8-1) in (8-2) to get equation (8-4) in the form of I_{Lpr}:

$$V_{out}(t) = V_X - L_{pr}\frac{dI_{Lpr}(t)}{dt} - I_{Lpr}(t)R_p \quad (3)$$

$$\frac{d^2I_{Lpr}(t)}{dt^2} + \frac{1}{C_fL_{pr}}(R_pC_f + \frac{L_{pr}}{R_L})\frac{dI_{Lpr}(t)}{dt} + \frac{1}{C_fL_{pr}}(1-\frac{R_p}{R_L})I_{Lpr}(t) = \frac{V_X}{R_LC_fL_{pr}} \quad (4)$$

If the component values are R_p = 1Ω, R_L = 15Ω, *Lpr* = 5nH and C_f = 4nF, the equation (4) reduced to:

$$\frac{d^2 I_{Lpr}(t)}{dt^2} + \alpha_1 \frac{dI_{Lpr}(t)}{dt} + \omega^2{}_o I_{Lpr}(t) = \frac{V_X}{R_L C_f L_{pr}} \tag{5}$$

Where:

$$\omega^2{}_o = \frac{\left(\frac{R_L + R_p}{R_L}\right)}{C_f L_{pr}} = 5.3333 \times 10^{16}$$

And

$$\alpha = \frac{1}{C_f L_{pr}} \left(1 + \frac{R_p}{R_L}\right) = 216.66 \times 10^6$$

The equation (5) is non-homogeneous equation. It has two solutions, complementary and particular solution:

$$I_{Lpr}(t) = I_{Lpr\_c}(t) + I_{Lpr\_p}(t) \tag{6}$$

The complementary solution $I_{Lpr\_c}(t)$ can be found by Characteristic (Auxiliary) Equation method:

$$\frac{d^2 I_{Lpr\_c}(t)}{dt^2} + \alpha_1 \frac{dI_{Lpr\_c}(t)}{dt} + \omega^2{}_o I_{Lpr\_c}(t) = 0 \tag{7}$$

The roots of equation (7) are complex conjugate.

$$S = -\alpha_p \pm \omega_{dp}$$
$$S_1 = -1.0833 \times 10^8 + i2.0395 \times 10^8$$
$$S_2 = -1.0833 \times 10^8 - i2.0395 \times 10^8$$

The general solution of equation (7) is:

$$I_{LC}(t) = K_1 e^{(-\alpha_p t)} \cos(\omega_{dp} t) + K_2 e^{(-\alpha_p t)} \sin(\omega_{dp} t) \tag{8}$$

To find particular solution $I_{Lpr}(t)$ method of undetermined coefficient is used:

$$I_{Lp}(t) = K_3 \tag{9}$$

Substitute equation (9) in (5) to find K_3:

$$K_3 = \frac{\left(\frac{V_X}{R_L C_f L_{pr}}\right)}{\omega_o^2} = 0.225 \qquad (10)$$

The solution of equation (4) is:

$$I_{Lpr\_c}(t) = K_1 e^{(-\alpha_p t)} \cos(\omega_{dp} t) + K_2 e^{(-\alpha_p t)} \sin(\omega_{dp} t) + K_3 \qquad (11)$$

Equation (11) is general solution and K_1, K_2 are unknown constants. In order to find them, initial conditions of circuit are applied. First initial condition, under ZVS operation the current ripple is $\Delta I_o = 2I_o$ which is equal to:

$$\Delta I_o = \frac{V_{out}(1-D)}{L_{pr} f_s} \qquad (12)$$

For 50% duty cycle the $V_{out} = 1.5$, $I_o = 100mA, f_s = 360mHz$ and $L_{pr} = 5nH$. The total output current ripple is 416mA. The current ripple is equally divided above and below the I_o see Fig 1(c). From this at time t = 0, $I_{L\min} = -120mA$, put initial condition in equation (11) find K_1:

$$I_L(0) = K_1 + K_3$$
$$K_1 = -0.345$$

Second initial condition $\frac{dI_{Lpr}(0)}{dt}$ can be found from equation (4):

$$L_{pr} \frac{dI_{Lpr}(0)}{dt} = V_X - V_{out}(0) - I_{Lpr}(0) R_p$$

Take derivative of equation (3-11) , put $I_{Lpr}(0)$ and K_2 is:

$$K_2 = \frac{\left(396 \times 10^6 - 37.37 \times 10^6\right)}{2.0395 \times 10^8} = 1.759$$

Substitute K_1 and K_2 in equation (12) to have exact solution:

$$I_{Lpr}(t) = -0.345\left(e^{(-\alpha_p t)} \cos(\omega_{dp} t)\right) + 1.759\left(e^{(-\alpha_p t)} \sin(\omega_{dp} t)\right) + 0.225 \qquad (13)$$

The voltage across the inductor L_{pr} can be found by:

$$V_{Lpr} = V_X - I_{Lpr}(t) R_p - V_{out}(t) \qquad (14)$$

When switch S1 in circuit Fig 1(a) is ON, the voltage rise across inductor L_{pr} will cause voltage fall in coupled secondary inductor L_s. This transformer action can be expressed by the following equations:

$$V_{Lpr} = L_{pr}\frac{dI_{Lpr}(t)}{dt} - M\frac{dI_s(t)}{dt}$$
$$V_{Ls} = L_{\sec}\frac{dI_s(t)}{dt} - M\frac{dI_{pr}(t)}{dt} \quad (15)$$

The L_{pr}, L_s and M are the self-inductance of each winding and mutual inductance between them, respectively. The expression can rearrange as:

$$V_{Lpr} = L_{k1}\frac{dI_L(t)}{dt} - k\sqrt{\frac{L_{pr}}{L_s}}V_{LS}$$
$$V_{Ls} = L_{k2}\frac{dI_S(t)}{dt} - k\sqrt{\frac{L_{pr}}{L_s}}V_{LP} \quad (16)$$

Where $k = \frac{M^2}{L_{pr}L_S} \le 1$ is the coupling coefficient and $L_{k1} = L_{pr}\left(1-k^2\right)$ and $L_{k2} = L_S\left(1-k^2\right)$ are commonly referred as leakage inductances. The equation (16) can describe as one Voltage controlled voltage source on secondary side with leakage inductance shown in Fig 2. R_s represent the resistive losses on secondary side and C_{in} represent the input capacitance of buffer stage of pulse forming circuit.

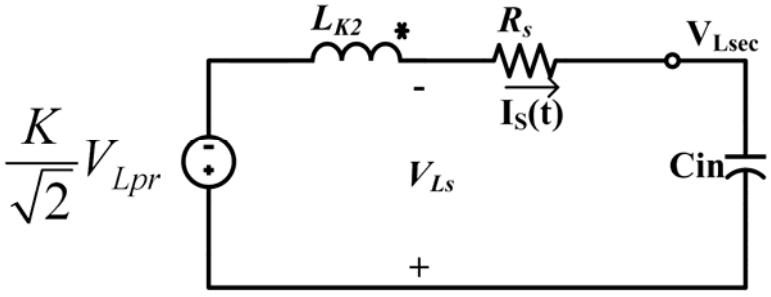

Fig 2: Secondary side coupled Inductor circuit when V_X node connected to V_{BAT}.

The differential equations (17) and (18) describe the circuit shown in Fig 2 :

$$-\frac{K}{\sqrt{2}}\left(V_X - V_{out} - I_{Lpr}(t)R_p\right) - L_{k2}\left(\frac{dI_s(t)}{dt}\right) - I_s(t)R_s - V_{L\sec} = 0 \quad (17)$$

$$I_s(t) = C_{in}\left(\frac{dV_{L\sec}(t)}{dt}\right) \quad (18)$$

Substitute $I_s(t)$ from equation (18) in (17):

$$\frac{d^2V_{L\sec}(t)}{dt^2}+\frac{Rs}{L_{k2}}\frac{dV_{L\sec}(t)}{dt}+\frac{V_{L\sec}}{C_{in}L_{k2}}=-\frac{K}{C_{in}L_{k2}\sqrt{2}}\left(V_x-V_{out}-\begin{pmatrix}-0.345\left(e^{(-\alpha_p t)}\cos(\omega_{dp}t)\right)\\+1.759\left(e^{(-\alpha_p t)}\sin(\omega_{dp}t)\right)\\+0.225\end{pmatrix}R_p\right) \tag{19}$$

The equation (19) is non-homogeneous differential equation. It also has two solutions, complementary and particular solution:

$$V_{L\sec}(t)=V_{L\sec\_c}(t)+V_{L\sec\_p}(t) \tag{20}$$

Complementary solution $V_{L\sec\_c}(t)$ can be found by characteristics equation method:

$$\frac{d^2V_{L\sec\_c}(t)}{dt^2}+\frac{Rs}{L_k}\frac{dV_{L\sec\_c}(t)}{dt}+\frac{V_{L\sec\_c}}{C_{in}L_k}=0 \tag{21}$$

If $R_s=12\Omega, L_k=1.275nH$ and $C_{in}=600\,fF$ then:

$$\alpha_2=\frac{R_s}{L_k}=9.41\times10^9$$
$$\omega^2{}_o=\frac{1}{C_{in}L_k}=1.307\times10^{21}$$

The roots of equation (21)

$$S=-\alpha_s\pm\omega_{ds}$$
$$S_1=-4.706\times10^9+3.587\times10^9$$
$$S_2=-4.706\times10^9\text{-}3.587\times10^9$$

The genral solution of equation (21) is:

$$V_{L\sec\_c}(t)=K_1e^{(-\alpha_s t)}\cos(\omega_{ds}t)+K_2e^{(-\alpha_s t)}\sin(\omega_{ds}t) \tag{22}$$

To find the particular solution of (8-21) method of undetermined coefficient is used:

$$V_{L\sec\_p}(t)=A_1e^{(-\alpha_p t)}\cos(\omega_{dp}t)+A_2e^{(-\alpha_p t)}\sin(\omega_{dp}t)+A_3 \tag{23}$$

The particular solution is:

$$V_{L\sec\_p}(t) = -0.169e^{(-\alpha_p t)}\cos(\omega_{dp}t) + 0.853e^{(-\alpha_p t)}\sin(\omega_{dp}t) + -0.927$$

The general solution of equation (19) is:

$$V_{L\sec}(t) = V_{L\sec\_c}(t) + V_{L\sec\_p}(t)$$
$$V_{L\sec}(t) = K_1 e^{(-\alpha_s t)}\cos(\omega_{ds}t) + K_2 e^{(-\alpha_s t)}\sin(\omega_{ds}t) - 0.169e^{(-\alpha_p t)}\cos(\omega_{dp}t) + 0.853e^{(-\alpha_p t)}\sin(\omega_{dp}t) - 0.927 \quad (24)$$

To find the initial condition go back to circuit in Fig 1(b). Solve the circuit in same manner as did for circuit in Fig 1(a). The circuit equation will be same as equation (7) and solution is same as equation (11) but with different initial conditions:

$$I_{Lpr}(t) = C_1 e^{(-\alpha_p t)}\cos(\omega_{dp}t) + C_2 e^{(-\alpha_p t)}\sin(\omega_{dp}t) \quad (25)$$

The equation (25) initial condition I_{Lmax}=320mA at time t = 0, and $\frac{dI_{Lpr}(0)}{dt}$ are:

$$\frac{dI_L(0)}{dt} = \frac{-V_{out} - I_L(0)R_P}{L_P} = -364\times10^6$$

Moreover, equation (25) becomes:

$$I_{Lpr}(t) = 0.320e^{(-\alpha_p t)}\cos(\omega_{dp}t) - 1.614e^{(-\alpha_p t)}\sin(\omega_{dp}t) \quad (26)$$

In addition V_{Lpr} is:

$$V_{Lpr}(t) = V_{out} - I_{Lpr}(t)R_p \quad (27)$$

With the 50% duty cycle when Switch S1 is ON Fig 1(a) at that time V_{Lsec} was at 678mV and I_S is zero that is first initial condition for circuit in Fig 2 and $\frac{dV_{L\sec}(0)}{dt}$ from equation (18):

$$V_{L\sec}(0) = K_1 - 0.169 - 0.927$$
$$0.678 = K_1 - 0.169 - 0.927$$
$$K_1 = 0.678 + 0.169 + 0.927$$
$$K_1 = 1.774$$
$$Is(0) = C_{in}\frac{dV_{L\sec}(0)}{dt}$$
$$\frac{dV_{L\sec}(0)}{dt} = \frac{Is(0)}{C_{in}} = 0$$

And

$$\frac{dV_{L\sec}(0)}{dt} = -K_1\alpha_s + K_2\omega_{ds} + 0.169\alpha_p + 0.853\omega_{dp}$$

$$K_2 = \frac{K_1\alpha_s - 0.169\alpha_p - 0.853\omega_{dp}}{\omega_{ds}}$$

$$K_2 = \frac{8.540\times10^9}{3.587\times10^9} = 2.4$$

$$V_{L\sec}(t) = 1.939e^{(-\alpha_s t)}\cos(\omega_{ds}t) + 2.575e^{(-\alpha_s t)}\sin(\omega_{ds}t) - 0.169e^{(-\alpha_p t)}\cos(\omega_{dp}t) + 0.853e^{(-\alpha_p t)}\sin(\omega_{dp}t) - 0.927 \quad (28)$$

When S1 is switch ON in Fig 1(a) inductor L_{pr} is in charging phase shown in Fig 3(a) is result of equation (13) and corresponding voltage across inductor L_{pr} in Fig 3(b) is result of equation (14). The discharging of inductor occurs when S2 is switch ON in Fig 1(b) and discharging curves are shown in Fig 3 (c) and (d) are the results of equation (25) and (27), respectively.

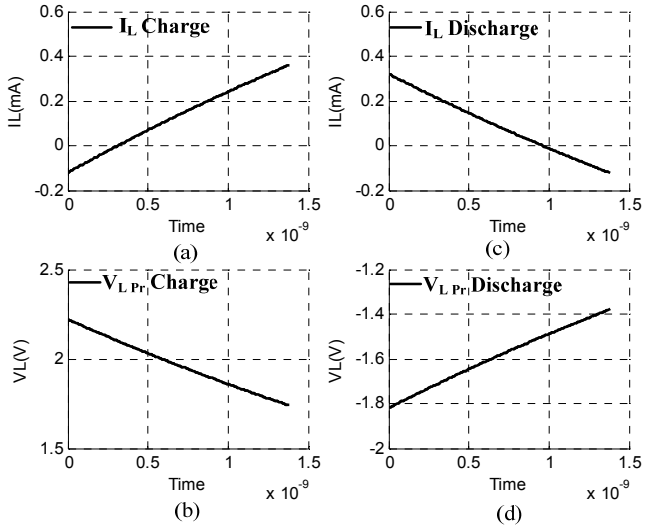

Fig 3: (a) inductor charging phase current (b) voltage across inductor during charging phase (c) inductor discharging phase current (d) voltage across inductor during discharging phase

When the S1 turns ON in circuit Fig 3(a), at the same time the voltage across V_{Lsec} is shown in Fig 4.

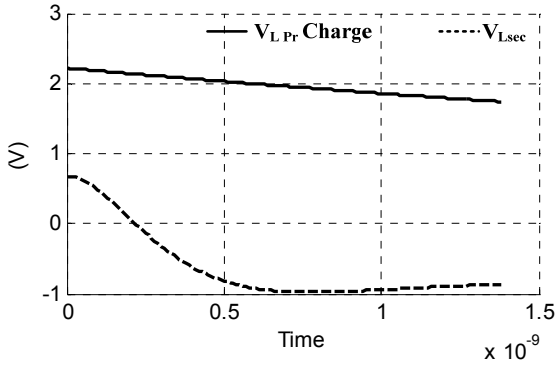

Fig 4: primary inductor voltage (V_{Lpr} Charge) during charging phase and voltage at input of pulse forming circuit (V_{Lsec})

Equation (14) and (28) are without any DC-Bias Level shown in Fig 4. To include the DC-Bias, Equation (28) will be:

$$V_{L\sec} = V_{L\sec}(t) + (V_{Bat} - \frac{V_{Bat}}{2})(\frac{R_{B2}}{R_{B1} + R_{B2}}) + 1.8 \qquad (29)$$

And

$$V_{L\sec} = V_{L\sec}(t) + (V_{Bat} - \frac{V_{Bat}}{2})(\frac{R_{B2}}{R_{B1} // R_{fb} + R_{B2}}) + 1.8 \qquad (30)$$

The equation (29) is in discharge phase of inductor L_{Pr} without feedback resistor R_{fb} and equation (30) is in charge phase of inductor L_{Pr} in which R_{fb} defines the duration of ON pulse of M_1.

APPENDIX-II

II.1 Future work on Self-Triggered converter

A feedback is implemented in [37] to drive the high-side PMOS transistor. The driving signal for the high-side PMOS transistor is generated from the converter output by using inductive feedback. The inductive feedback eliminates the level shifters required for transferring a driving signal to high-side PMOS transistor. Simulations on 45nm CMOS process show that it is possible to drive the high-side transistor via inductive feedback.

In this work, we focus on voltage level shifter issue and rest of circuit will be same. The techniques used in this work, uses an inductive feedback, which provide the voltage feedback from the converter output to generate the control signals for high-side transistor. This technique is much faster than conventional voltage level shifter [35].

II.2 Cascoded Power Stage with Feedback

The converter with automatic dead time control with feedback is shown in Fig 5 (a). In the previous work we assumed *DriveP* and *DriveN* are synchronized without dead-time and driving externally. Now power stage is only driven by *DriveN* and *DriveP* is generated from feedback. *Lsec* is biased at the middle of V_B and V_{SSP} by two diode-connected M_{NB1} and M_{NB2} transistors. The *Lsec* and *Lpr* inversely coupled (means decreasing voltage at V_X causing voltage *DriveP* to increase and vice versa) with the coupling factor K = 0.7. M_{fb} pulls the DC-biased level at the input of inverter *IP*. The rest of the circuit, *IN* and *IP* are ordinary inverters, the second stage of inverter for M_1 and M_2, M_6 is included. The gate of M_6 is connected to *PFB* node and M_1 would not switch OFF until M6 is switched ON. Similar arrangement is done for cascoded M_3 and M_4 second inverter driving stage, where M_9 is added in the inverter M_8 and M_{10}.

In the following V_{TN} and $|V_{TP}|$ are the threshold voltages of n-and p-channel transistors, as usual, and V_{NFB}, V_{NDR}, V_{PFB}, and V_{PDR} are the voltages of corresponding nodes in Fig 5(a).

The initial transient of circuit in Fig 5(a) is more complicated, still trying to understand it. I will describe the operation, when the circuit gets steady state; the operation of the circuit is as follow. Assume the duty-cycle of *DriveN* is 50%. Consider the generation of DTLH dead-time when the inductor *Lpr* current becomes negative (the load capacitor C_L is discharging). To obtain DTLH dead-time, it is necessary, first, to turn M_4 OFF, causes V_X node start charging (see Fig 5(b)). At the instant, when M_4 is switched OFF, the gate of M_9 is (practically) at zero voltage, so that M_9 is ON, and the inverter M_8, M_{10} switches OFF M_4 without delay. The V_X node will not charge immediately, first, the negative current charge C_n and C_X. When C_n is charged to $V_B/2\text{-}V_{TN}$ then M_3 is OFF, and the coil current start charging C_X only. Now V_X start increasing faster. When V_X

achieves the value $V_B/2+|V_{TP}|$, M_2 will go in inverse operation, and V_X will start increasing with lower speed. But M_1 is not switch ON yet until M_6 is will not ON, to turn ON M_6, *PFB* node will charge to $V_{SSP}+V_{TN}$.

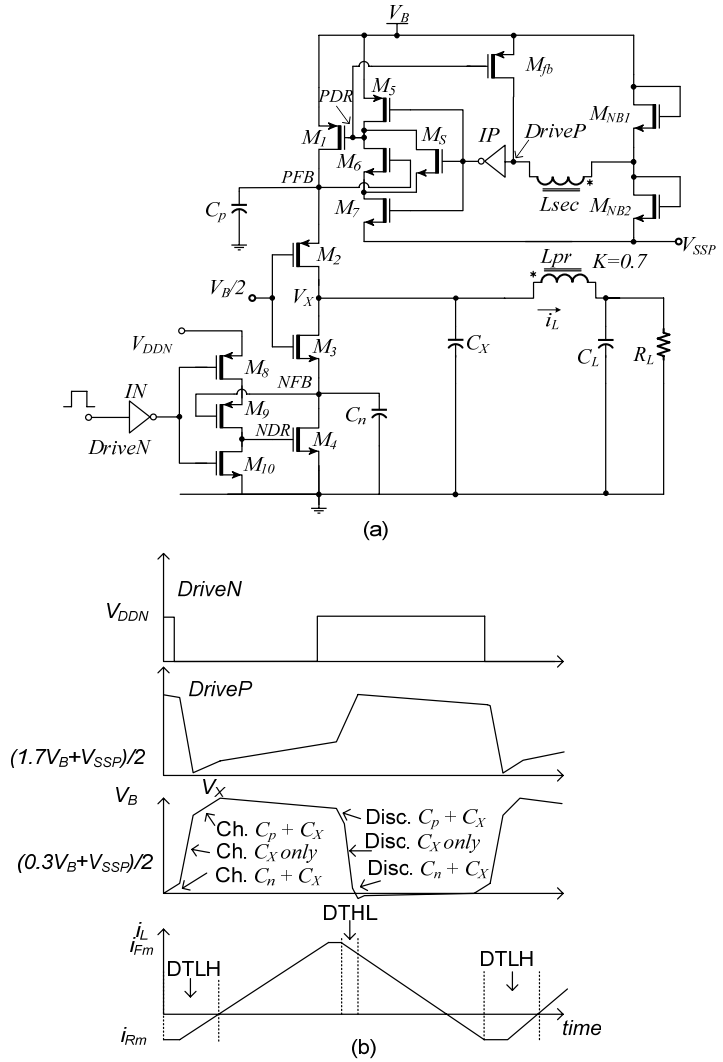

Fig 5: output stage with automatic dead-time generation with feedback: (a) Circuit (b) Waveform

During the transient of charging V_X node, the inverse transformer operation causes the rising edge at V_X node to transfer as falling edge at *DriveP*. The transfer of signal is so fast, that *DriveP* reaches the triggering level (voltage level require to turn ON M_1) before the M_6 turn ON. When M_1 is turn ON, at the same time *PDR* will also turn ON M_{fb}. This creates the higher DC-bias voltage for *DriveP* than before (created by M_{NB1} and M_{NB2}). This helps in controlling the ON time of M1 (or reached the turn OFF voltage level of *IP* faster). If M_{fb} is not present, the ON time of M_1 will be long enough to take two-three frequency cycles to turn OFF. Because *DriveP* will start increasing from $(0.3V_B + V_{SSP})/2$ (V_X node voltage will not stay constant, it start decreasing due to inductor resistive losses (see Fig 5 (b)) to trigger OFF voltage level (about 3.1V), which takes time of two to three cycles.

Let us now consider the generation of DTHL dead time, when *DriveP* reaches the voltage level requires to turn OFF M_1. The transistor M_1 will turn OFF practically simultaneously with this command (M_6 is "invisible" for turning M_1 OFF). When M_1 turned OFF, C_P is close to V_B (ZVS switching). The transistor M_2 will be turned OFF later (see below). At the instant *DriveN* already turns the transistor M_8 ON, the voltage V_{NFB} (i.e. the gate voltage of M_9) is equal to $V_B/2\text{-}V_{TN}$. Even though the source of M_9 is at the voltage close to V_{DDN} the transistor M_9 is still OFF and does not allow M_8 to provide the current which is necessary to charge the gate capacitance of M_4 and to turn it ON (of course, this requires that $V_{DDN} > V_B/2\text{-}V_{TN}$). To make this turning happen, the current i_L will, first, discharge C_X and C_P. C_P will discharge via M_2 because at the instant when M_1 turned OFF, the voltage across C_P close to V_B. C_P will discharge up to $V_B/2 + |V_{TP}|$, M_2 will be OFF. Afterwards, CX will start discharging and VX node voltage is decreasing faster. When VX becomes equal to $V_B/2\text{-}V_{TN,}$ M_3 will enter inverse operation (i.e. source and drain are changing their roles), discharging C_n and C_X. The voltage V_X and V_{NFB} start decreasing together with slow speed. When the voltage across C_n reaches $V_B/2 - |V_{TP}|$ transistor M_9 will turn ON and current via M_8, M_9 charge the gate capacitance of M_4 and M_4 will start to turn ON. In the next cycle, same process will happen for DTHL and DTLH.

II.3 Feedback Design considerations

Transformer Design: For the correct operation of proposed converter requires bidirectional *Lpr* inductor current to charge and discharge the capacitances C_X, C_n and C_p. the *Lpr* inductor current will be bidirectional if current ripple $\Delta i_L = i_{Fm}\text{-}i_{Rm}$, will be two times greater than average inductor current I_L. The *Lpr* inductor value can be expressed as [36].

$$Lpr = \frac{Vo(1-D)}{f_s \Delta I_L} \qquad (7\text{-}31)$$

Where $V_o = V_B$.D is output voltage, V_B is given battery voltage, D is duty-cycle and f_s is switching frequency of converter. Since primary *Lpr* and secondary *Lsec* coils are AC-coupled, secondary coil can be biased at arbitrary voltage independent of secondary coil voltage. In addition, secondary coil voltage depends upon the coil-turn ratio between primary and secondary coil. To estimate the value of secondary coil *Lsec*, transformer equivalent circuit in Fig 6 is used; in which voltage-dependent-voltage-source represent the mutual-inductance [36], *n* is square-root turn ratio of coils, $Lpr(1\text{-}K^2)$ and $Lsec(1\text{-}K^2)$ are the leakage inductance of primary and secondary coils, respectively. R_{sec} represents the secondary coil resistance and R_{oe} is cascoded switch resistance r_{SW}, output filter capacitor C_L resistance and *Lpr* coil resistance.

$$R_{oe} = r_{SW} + r_C + R_{pr} \tag{7-32}$$

$$n = \sqrt{L_{pr} / L_{\sec}} \tag{7-33}$$

The voltage across secondary coil V_{Lsec} can be express as:

$$V_{L\sec} = K.n.V_{Lpr} - V_{Lleak} \tag{7-34}$$

The value of secondary coil is adjusted, so that its voltage should not exceed the breakdown voltage transistor. For V_O = 1.8V, *Lsec* is set to 0.25*Lpr*.

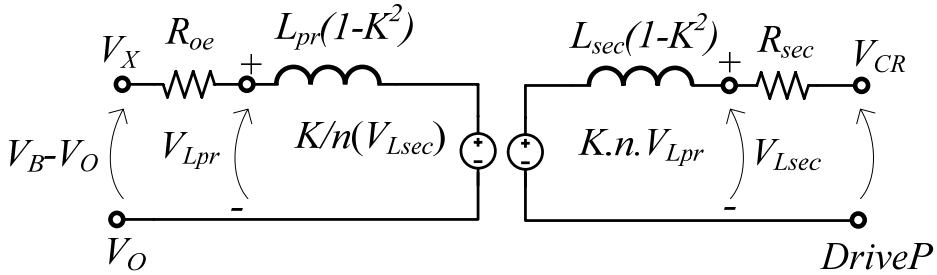

Fig 6: Voltage-dependent-voltage-source to represent the equivalent Transformer circuit.

Biasing Secondary Coil: Secondary coil is biased in the middle of V_B and V_{SSP} by using two diode-connected NMOS transistors M_{NB1} and M_{NB2} (see Fig 5(a)). The bias voltage V_{CR} can be expressed as:

$$V_{cr} = \frac{\alpha_2}{\alpha_1 + \alpha_2}(V_B - V_{SSP}) + \frac{\alpha_1 V_{TNB1} - \alpha_2 V_{TNB2}}{\alpha_1 + \alpha_2} \tag{7-35}$$

$$\alpha_1 = \sqrt{\left(\frac{W}{L}\right)_{MNB1}}$$

$$\alpha_2 = \sqrt{\left(\frac{W}{L}\right)_{MNB2}} \tag{7-36}$$

V_{TNB1} and V_{TNB2} are the threshold voltages of corresponding transistors. The threshold voltages of M_{NB1} and M_{NB2} would be different because of body-effect. The M_{NB1} and M_{NB2} have same sizes. In addition, their sizes are adjusted to provide the minimum current while transient. The transistor size is set to 300μm.

Feedback transistor: The feedback transistor M_{fb} (see Fig 5(a)) is adjusting the ON time of M_1. When V_{PDR} turns ON the M_1, M_{fb} also turns ON and pulls up the *DriveP* DC-biased voltage. The size of M_{fb} is adjusted by simulation to have V_o =1.8 V approximately.

The supply voltage and start-up transistor *Ms* circuit design considerations are the same as mention in [37].

II.4 Simulation

The buck converter output stage with automatic dead-time generation with feedback was designed in 45 nm CMOS process. The converter switching frequency is 240MHz, and it generates 1.8 V output voltage from V_B = 3.6 V battery voltage for the load of 12 Ω (i.e. load current 150 mA). The filter inductance *Lpr* was taken 5nH, secondary coil inductance *Lsec* 0.25*Lpr*, the feedback transistor M_{fb} is adjusted to 100 μm.

Based on the requirement defined in [37], the voltage V_{DDN} and V_{SSP} are selected as 1.1 V and 2.5 V respectively. These reduced supply voltages for drivers help to decrease the gate-driver switching loss and achieve better conversion efficiency.

The simulated waveforms of purposed converter are shown in Fig 7. The converter power stage is only driven by *DriveN* and *DriveP* is generated by inductive feedback. The circuit in Fig 5(a) is generating dead-times (DTHL and DTLH) automatically, hence, eliminating the short circuit current between V_B and ground. The DTLH = 400ps and DTHL = 100ps are achieved.

The converter efficiency, η, was calculated as

$$\eta = \frac{P_{load}}{P_{VB} + P_{SSP} + P_{DDN} + P_{VB/2}} \times 100\% \qquad (7\text{-}37)$$

Where P_{load} is the power delivered from the stage to load, P_{VB}, P_{SSP}, P_{DDN} and $P_{VB/2}$ are the power delivered from battery and bias voltage sources V_{SSP}, V_{DDN} and $V_B/2$ to the stage. The simulated efficiency achieved 73.5% at output voltage approximately 1.8 V and load current 150 mA.

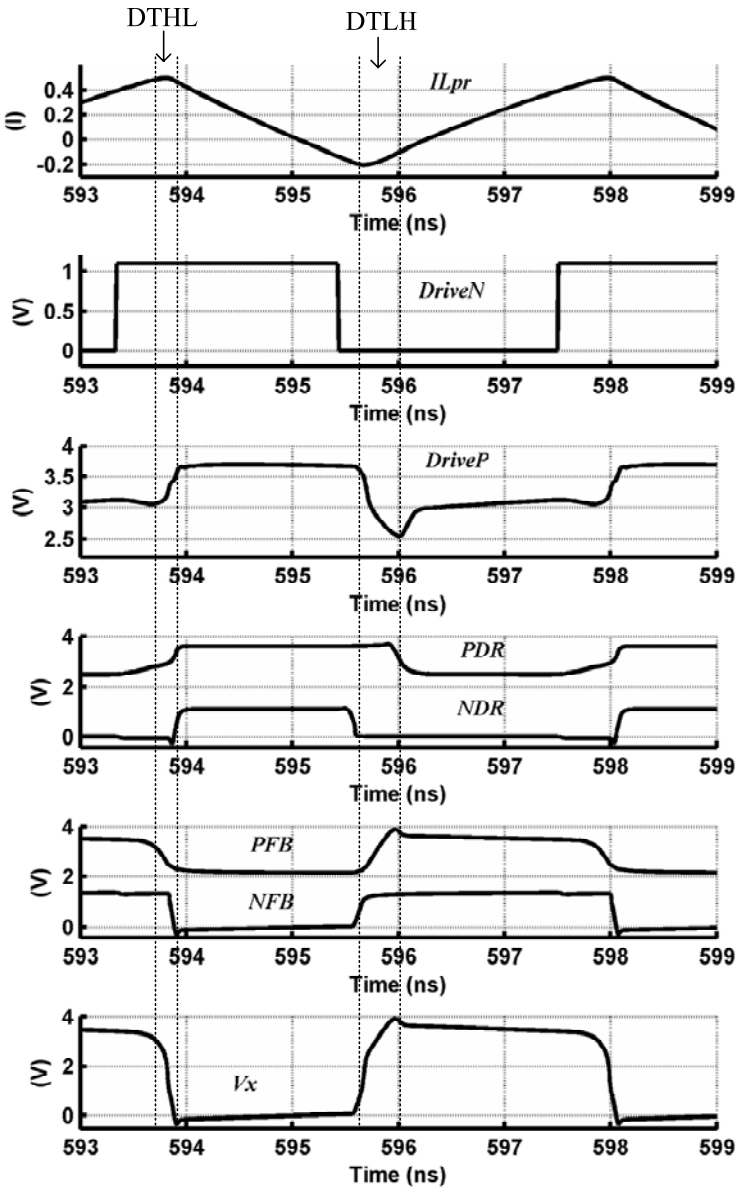

Fig 7: Simulated Waveforms for V_B = 1.8 V, I_{out} = 150 mA

II.5 Conclusion

An inductive feedback technique for driving PMOS power transistor in automatic dead-time generation power stage is proposed. A transfer of signal between different voltage domains is faster and consumes less power. With this, we can avoid the delay and losses related to voltage level shifters. It can be seen by comparing the converter power stage efficiency with (this work) and without [37] inductive feedback is same (without parasitic).

The output voltage regulation of converter can be realized by changing the size of feedback transistor. To change the size of feedback transistor needs a control system that monitors the output voltage and change size of transistor according to it.