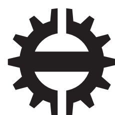


KONSTANTIN RYKOV

QUASI-LINEAR MODELING OF POWER SATURATION IN BIPOLAR JUNCTION TRANSISTORS

Master's thesis

Examiners: Professor Leena Ukkonen,
Postdoctoral Researcher Toni Björninen.
Examiners and topic approved by the Faculty Council of the Faculty of Computing and Electrical Engineering on 4 September 2013.

Abstract

TAMPERE UNIVERSITY OF TECHNOLOGY
Master's Degree Programme in Electrical Engineering
RYKOV, KONSTANTIN: Quasi-Linear Modeling of Power Saturation in Bipolar Junction Transistors

Master of Science Thesis, 57 pages, 1 Appendix page
November 2013
Major subject: Radio Frequency Electronics
Examiners: Professor Leena Ukkonen, Postdoctoral Researcher Toni Björninen.
Keywords: Quasi-linear network analysis, output power, power saturation prediction in transistors, small-signal model, transadmittance, transistor modeling.

Nowadays the problem of accurate power saturation prediction becomes more eminent. The powerful and expensive CAD systems provide approximate behaviors of power saturation that do not always coincide with the realistic scenario. The state-of-the-art quasi-linear transistor model that is a logical development of the small-signal hybrid-π model has been initially applied for oscillation analysis. In this thesis we investigate the quasi-linear model for power saturation prediction in bipolar junction transistors. The efficiency of the modeled power saturation is verified by comparing it with the simulation in Agilent Advanced Deign System 2009 and measurement results. According to the extensive computational analysis the quasi-linear modeling presents high accuracy in the linear region of power saturation in the range of 0.01 – 0.35 dBm, whereas the simulated curves lag behind in the range of 2 dBm – 7 dBm. Moreover, the quasi-linear model predicts the power saturation point more accurately compared to the simulations using the CAD systems.

Preface

This thesis concludes a long-term research on quasi-linear modeling of power saturation in BJT based amplifiers under supervision of Professor Olli-Pekka Lundén started in January 2013. This work is a continuation of the research on a quasi-linear power analysis of the Clapp oscillator, which was conducted in Tampere University of Technology by Professor Olli-Pekka Lundén, Kristian Konttinen and Masoumeh Hasani. As a part of my Master's Major studies, this thesis describes in detail the achieved results related to the topic and comprises a self-sufficient study on the transistor small-signal model and prediction of power saturation in bipolar junction transistors. The conducted research and the obtained results carry a scientific importance and, as a result, the further publication is going to be prepared.

I wish to express my gratitude to my diploma supervisor Professor Olli-Pekka Lundén for giving me the chance to pursue the studies for my Master's thesis in Finland, his highly professional guidance and natural ability to involve students, and particularly me, into research work that resulted in successful cooperation.

I am very grateful to my examiners Professor Leena Ukkonen and Doctor Toni Björninen for their prompt important comments on the structure of the work and language, and for valuable advices.

I also wish to thank my family and my girlfriend who managed to create an appreciating environment that helped me to overcome the hardest moments.

30.09.2013
KONSTANTIN RYKOV

Contents

Abbreviations and symbols v

List of tables viii

List of figures ix

1 Introduction 1

1.1 Structure of the thesis . . . 3

2 Theoretical background 4

2.1 Transistor amplifier design . . . 4

2.1.1 Common-emitter amplifier scheme. Key parameters . . . 4

2.1.2 Gain compression in high-power amplifiers . . . 5

2.2 Transistor models . . . 6

2.2.1 Large-signal model . . . 7

2.2.2 Small-signal hybrid-π model . . . 8

2.2.3 Quasi-linear transistor model . . . 10

2.3 Research goals . . . 12

3 Measurements 14

3.1 Calibration Procedure . . . 14

3.2 Measurement setup and component placement . . . 18

3.3 S-parameter measurements: frequency sweep . . . 19

3.4 S-parameter measurements: power sweep . . . 21

4 Quasi-linear analytical modeling 33

4.1 Circuit element values extraction . . . 33

4.2 Load power evaluation . . . 36

4.3 Experimental results . . . 39

5 Simulations 43

5.1 Simulated amplifier circuit . . . 43

5.2 Simulated power saturation curves . . . 44

6 Discussion 48

6.1 Transadmittance analysis . . . 48

6.2 Steepness of power saturation . . . 49

6.3 Power saturation analysis . . . 49

Conclusion 53

Appendix 1: Programing code for MATLAB outer function for the quasi-linear power analysis **54**

References **56**

Abbreviations and symbols

- AC (Alternating Current) – a periodical harmonic flow of electrical charges.
- ADS (Advanced Design System) – the Agilent electronic CAD system that is commonly used for simulations of electrical circuits, designing the printed circuit boards and research of nonlinear phenomena in electronics.
- BC-junction (Base-Collector-junction) – a junction in bipolar junction transistors between base and collector.
- BE-junction (Base-Emitter-junction) – a junction in bipolar junction transistors between base and emitter.
- BJT (Bipolar Junction Transistor) – a semiconductor active device used for transformation (amplification and oscillation) of electrical signals.
- CAD (Computer-Aided Design) – a computer system (program) used for creation, modification, simulation, analysis or optimization of a certain design.
- CP1 (Component Placement 1) – a certain placement of the electrical components on the breadboard discussed in this thesis.
- CP2 (Component Placement 2) – another certain placement of the electrical components on the breadboard discussed in this thesis.
- DC (Direct Current) – a unidirectional flow of electric charge in electrical schemes produced by the sources such as batteries, solar cells and DC generators.
- DCB (Direct Current Block) – an electrical component (a capacitor at high frequencies) that prevents the DC flow in the circuit.
- DUT (Device Under Test) – a unit (an electrical device), which parameters are measured during the measurement procedure.
- FET (Field-Effect Transistor) – a semiconductor active device that uses an electric field to control the shape of the transformed signal.
- HP (Hewlett Packard) – an American corporation that produces the electrical devices including the RF measurement equipment (network analyzers, multimeters, oscilloscopes and etc.).
- IMD (Intermodulation Distortion) – an amplitude modulation of signals including the signals that cause nonlinearities in the frequency range.
- NA (Network Analyzer) – a measurement device that measured parameters of electrical network, such as S-parameters with frequency or power sweep.

- RF (Radio Frequency) – the frequency range from 3 kHz till 300 GHz, which correspond to the radio waves and alternating currents that carry radio signals.
- RFC (Radio Frequency Choke) – an electrical component (an inductor at high frequencies) that passes signals only with the certain frequency component.

Table 1: Symbols and Notation.

Variable	Description
v_{eb}, v_{cb}	emitter-base and collector-base voltages
v_{be}, v_{ce}	base-emitter and collector-emitter voltages
v_{bc}, v_{ec}	base-collector and emitter-collector voltages
i_e , i_c i_b	emitter, collector and base currents
R_b, R_c	base resistor and collector resistor
v_{ce0}	collector-emitter voltage
V_{CC}, I_{DC}	DC voltage and current
E_g	generator voltage
Z_g	generator impedance
Z_0	characteristic impedance
Z_{in}	input impedance
Z_L	load impedance
Z_1, Z_2	an equivalent impedances
P_{out}	output power
P_{in}	input power
P_{avg}, P_{av}	available power from the generator
$P_{out,1dB}$	the point in nonlinear region at which the output power level decreases by 1 dB from the ideal characteristics
d_R	dynamic range
$P_{out,min}$	minimum detectable output power
α_R, α_F	reverse and forward current gains
I_s	transistor saturation current
g_m	transconductance
V_{BE}^Q, I_C^Q	base-emitter voltage and collector voltage at bias Q-point
β_0	small-signal current gain
r_π, r_0	input and output resistances
Y-parameters (Y_{ij})	admittance parameters
y_m	transadmittance
y_{m0}	small-signal transadmittance
r	empirical parameter
$\hat{i}_{c,max}$	amplitude of the maximum collector current
$\hat{v}_{be}$	amplitude of the base-emitter voltage
ϕ	angle
$e^{j\phi}$	phasor of the complex number
f	frequency
Δf	bandwidth
C_{be}, C_{bc}, C_{ce}	base-emitter, base-collector and collector-emitter capacitances
P_L	power at the load
v_L	voltage at the load
S-parameters (S_{ij})	scattering parameters
f_{start}, f_{stop}	start and stop frequencies
P_{start}, P_{stop}	start and stop powers

List of Tables

1 Symbols and Notation. vii
2 The BJT modes of operation [1, p. 209]. 1
3 The list of the amplifier electrical components. 16
4 The list of the amplifier electrical components. 18
5 Measured S-parameters of nine PN3563. CP1, $f = 100$ MHz, $P = -20$ dBm. 20
6 Measured S-parameters of PN3563. CP2, $f = 100$ MHz, $P = -20$ dBm. . 20
7 Measured S-parameters of NTE108, $f = 100$ MHz, $P = -20$ dBm. 21
8 Measured S-parameters of PN3563. CP1, $P = -20$ dBm, $f = 100$ MHz. . 23
9 Measured S-parameters of PN3563. CP2, $P = -20$ dBm, $f = 100$ MHz. . 23
10 Measured S-parameters of NTE108 for component placements CP1 and CP2. 25
11 Measured S-parameters of BF959. 26
12 Measured S-parameters of BFW16, component placement CP2. 27
13 Measured S-parameters of 2N5179. 28
14 Measured S-parameters of 2N5109. 29
15 The evaluated values of $|y_{m0}|$, $i_{c,max}$ and r. 31
16 Resistor values for simulated transistors. 45

List of Figures

1 The *n-p-n* bipolar junction transistor: simplified schematic structure (left) and electrical symbol (right). 1
2 Three types of bipolar-junction transistor connections: common-base (left), common-emitter (central), common collector (right). 2
3 Example of the equivalent transistor model [1, p. 250]. 2
4 Common-emitter amplifier scheme used in RF range. 4
5 Power saturation. 6
6 Static large-signal Ebers-Moll circuit model. 7
7 Dynamic large-signal Ebers-Moll model. 8
8 Small-signal hybrid-π Ebers-Moll BJT model. 8
9 Simplified hybrid-π small-signal model. 9
10 Quasi-linear transistor model used in the power saturation analysis. 10
11 Smooth transadmittance functions (18) with different r values (solid lines). The piecewise transadmittance function (17) (dashed line). 11
12 Research task. 12
13 Variants of the component placement on the breadboard. 14
14 The calibration algorithm. 15
15 The breadboard SOLT set for calibration (CP1). 16
16 The breadboard SOLT set for calibration (CP2). 17
17 The S-parameter measurement setup. 18
18 Measured S-parameters for BJT PN3563, CP1. 19
19 Ideal and real measured compression curves. 22
20 Measured S-parameters of one PN3563 with power sweep. CP2, $f = 100$ MHz, $P = -20 ... -1$ dBm. 22
21 Family of gain compression curves. BJT PN3563, component placement CP2. 23
22 Transadmittance y_{m0} as a function of voltage v_{be} for BJT PN3563. 24
23 Measurement results for BJT NTE108: (a) the gain compression curves; (b) the transadmittance $y_{m0}(v_{be})$ behavior. 25
24 Measurement results for BJT BF959: (a) the gain compression curves; (b) the transadmittance $y_{m0}(v_{be})$ behavior. 26
25 Measurement results for BJT BFW16: (a) the gain compression curves; (b) the transadmittance $y_{m0}(v_{be})$ behavior. 27
26 Measurement results for BJT 2N5179: (a) the gain compression curve; (b) the transadmittance $y_{m0}(v_{be})$ behavior. 28
27 Measurement results for BJT 2N5109: (a) the gain compression curve; (b) the transadmittance $y_{m0}(v_{be})$ behavior. 29

28 The measured $|y_{m0}|$ (symbols) vs. v_{be} and the fitted functions (solid lines) of the measured transistors at bias point $I_C^Q = 20$ mA, $V_{CE}^Q = 5$ V. 30
29 The power saturation graphs for BJT PN3563 for CP1 and CP2 both for frequency and power sweeps. 31
30 The power saturation curves of all measured transistors. 32
31 The quasi-linear transistor model is connected to generator and load. . . . 33
32 Algorithm of the extraction of the element values from S-parameters. . . . 34
33 Quasi-linear model used for deriving the Y-parameters. 35
34 Simplified scheme of the quasi-linear transistor model. 37
35 Power saturation for PN3563 using the analytical model. 39
36 Obtained transadmittance behavior for PN3563 when $r = 1$, $r = 2$, $r = 3$, $r = 5$, $r = 9$. 40
37 Obtained graphs for 2N5179 using the analytical model. 40
38 Obtained graphs for 2N5109 using the analytical model. 40
39 Obtained graphs for NTE108 using the analytical model. 41
40 Obtained graphs for BFW16 using the analytical model. 41
41 Obtained graphs for BF959 using the analytical model. 41
42 Transadmittance $|y_m(\hat{v}_{be})|$ behaviors for tested transistors. 42
43 Simulated circuit of power amplifier in ADS 2009. 43
44 Simulated power saturation for PN3563 and NTE108. 45
45 Simulated power saturation for 2N5179. 46
46 Simulated power saturation for 2N5109. 46
47 Simulated power saturation for BFW16. 47
48 Simulated power saturation for BF959. 47
49 Transadmittance magnitude $|y_m(\hat{v}_{be})|$: measured (colored markers), fitted (black solid lines) and modeled (dashed lines) curves. 48
50 Measured (red line) and modeled (blue lines) power saturation curves. . . 49
51 Simulated, measured and modeled power saturation curves for PN3563. . 50
52 Simulated, measured and modeled power saturation curves for BF959. . . 50
53 Simulated, measured and modeled power saturation curves for 2N5179. . 51
54 Simulated, measured and modeled power saturation curves for 2N5109. . 51
55 Simulated, measured and modeled power saturation curves for NTE108. . 52
56 Simulated, measured and modeled power saturation curves for BFW16. . 52

1 Introduction

Nowadays the signal amplification is required in a number of electrical devices, such as mobile phones, personal computers, mobile base station transceivers, TV, microphones, loud-speakers and etc. Despite of the huge amount of active electrical components, transistors, which represent the semiconductor structures that transform the electrical signals, are commonly used in an amplifier design [1, pp. 208]. There are two main types of transistors – a bipolar junction transistor (BJT) and field-effect transistor (FET), the operation modes of which are completely different [1, pp. 208-209], [2, pp. 170-275]. For the BJT transistors there are two types of structures: with P-doped semiconductor between two N-doped layers (*n-p-n*) and N-doped semiconductor between two P-doped layers (*p-n-p*). This work concentrates only on the BJT with *n-p-n*-structures.

The simplified schematic structure of the *n-p-n* BJT and the BJT symbol are presented in Figure 1 from left to right parts, respectively. Petrov states [1, pp. 208-209] that each of the *p-n*-junctions, denoted on the figure as a base-collector (BC)- and base-emitter (BE)-junctions, may be opened or closed. Therefore, there can be four modes of BJT operation presented in Table 2.

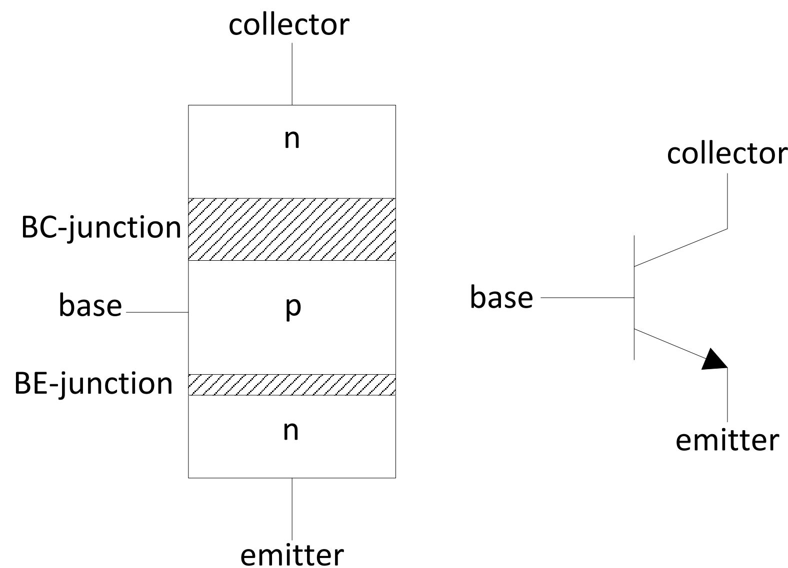


Figure 1: The *n-p-n* bipolar junction transistor: simplified schematic structure (left) and electrical symbol (right).

Table 2: The BJT modes of operation [1, p. 209].

N	Mode	BE-junction	BC-junction
1	Active (forward-active)	Opened	Closed
2	Reverse (reverse-active)	Closed	Opened
3	Saturation	Opened	Opened
4	Cutt-off	Closed	Closed

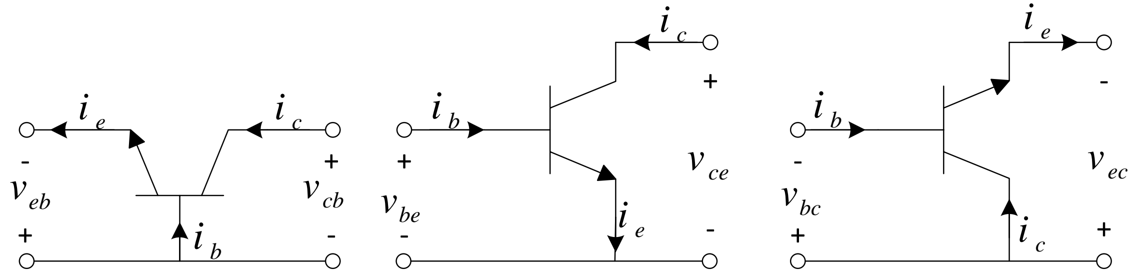


Figure 2: Three types of bipolar-junction transistor connections: common-base (left), common-emitter (central), common collector (right).

Regarding [1, pp. 210-211] and [3, pp.79-80], the amplification of the signal is performed by setting the BJT to an active mode and connecting it as one of three possible schemes presented in Figure 2: common-base, common-emitter and common-collector connections. There are six types of voltages between two electrodes specified by a double index: emitter-base v_{eb}, collector-base v_{cb}, base-emitter v_{be}, collector-emitter v_{ce}, base-collector v_{bc} and emitter-collector v_{ec} voltage. Figure 2 illustrates the voltage polarities that set the BJT in active mode and the current directions, where i_b, i_c and i_e are the base, collector and emitter currents, respectively.

The bipolar junction transistors have a complex operation that requires a good understanding of solid-state (conductor, insulator and semiconductor) physics [2, pp. 141-147]. Fortunately, the so-called equivalent electrical transistor models allow describing the operation of the BJT and they are commonly used for amplifier engineering and analysis [1, pp. 235-240, 250-251]. The equivalent transistor model is an electrical scheme that consists of a number of elements, such as diodes, ideal current sources, resistors, capacitors and etc., the connection of which allows imitating the physical processes in BJT. An example of a simple equivalent transistor model that is connected using the common-base scheme is presented in Figure 3 [1, p. 250].

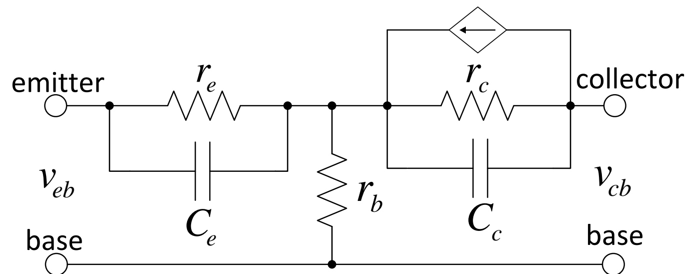


Figure 3: Example of the equivalent transistor model [1, p. 250].

Unfortunately, the transistor models do not take all physical phenomena into account [4, p. 367]. For instance, the transistor models can not predict accurately some nonlinearities that happen in BJT, such as a power saturation. To make matters worse, the prediction of power saturation is a challenging problem even for the powerful and

expensive computer-aided design (CAD) systems. Consequently, the power saturation analysis in bipolar junction transistors is a topical problem that requires an innovative solutions. The best candidate for this role is the new quasi-linear transistor model that is a state-of-the-art invented by Olli-Pekka Lundén [5]. This model has shown an excellent results in oscillation analysis [5] – [6], but it has never been considered in terms of power amplification analysis.

1.1 Structure of the thesis

The thesis is organized as follows. The theoretical background in Chapter 2 provides an insight into the BJT amplifier design and comprehends the transistor models that are commonly used in describing the BJT operation. On top of that, an applicability of the new quasi-linear transistor model to power saturation prediction compared to other models is considered in detail, and the major goals of this research are declared.

Three major parts of the research are presented in this thesis as follows. The measurement procedure and the obtained results are presented in Chapter 3, while the quasi-linear modeling of power saturation is described in Chapter 4. The simulation results of the power amplifier using the CAD Agilent Advanced Design System 2009 are shown in Chapter 5. The detailed discussion is considered in Chapter 6 and, finally, conclusions are drawn.

2 Theoretical background

This chapter presents the theoretical background related to the amplifier design. Firstly, the common-emitter scheme of a BJT based amplifier is considered and the key parameters are discussed. Secondly, the definition of the gain compression is given and the importance of the power saturation prediction is presented. Thirdly, the different types of transistor models are evaluated and the state-of-the-art quasi-linear model is performed. Lastly, the research goal of this thesis is declared in the end of this chapter.

2.1 Transistor amplifier design

A bipolar-junction transistor is the semiconductor device, which is commonly used in amplification and oscillation of the electrical signals. If an amplifier is designed, then the BJT should be biased to work in the active region [7, pp. 787-789], which means that the direct current (DC) operating point has to be fixed.

There are three possible connections of the BJT used in engineering: common-base, common-emitter and common-collector schemes. The most popular connection of the BJT used for designing amplifiers is the common-emitter scheme, which will be considered in the following discussion.

2.1.1 Common-emitter amplifier scheme. Key parameters

The general scheme of a simple common-emitter amplifier can be found in Jaeger's [7, pp. 790-791] and Fonstad's [8, p. 329] books. The modified version of this scheme that operates in radio frequency (RF) range is presented in Figure 4.

The resistors R_b and R_c are used to set the DC operating point aka the bias point. Usually, the values of these resistors are set to satisfy the condition $v_{ce0} = V_{cc}/2$, where

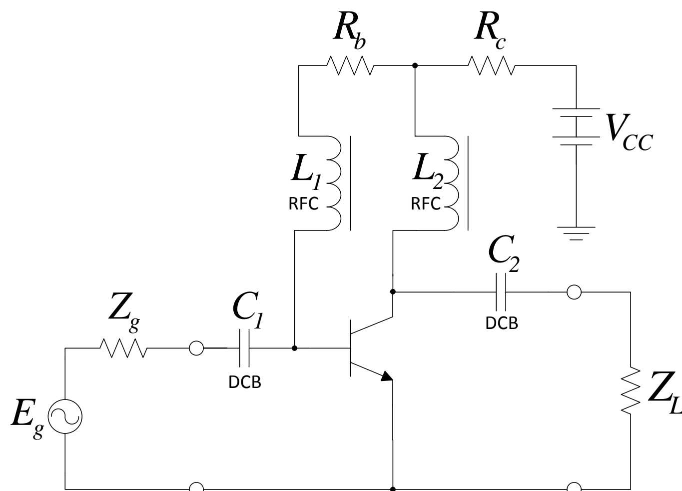


Figure 4: Common-emitter amplifier scheme used in RF range.

v_{ce0} is the collector-emitter voltage and V_{cc} is the DC voltage. The generator with voltage E_g and impedance Z_g produces the signal to be amplified. Ludwig and Bogdanov state in their book [4, pp. 19-25] that an inductor works as the RF choke (RFC), while a capacitor works as the DC block (DCB) at high-frequencies. Hence, when an amplifier operates in RF frequency range, the inductors L_1 and L_2 are connected to the base and collector respectively, while the capacitors C_1 and C_2 are used to prevent the DC current from leaking to source and load. The latter is described by the load impedance Z_L.

Regarding Ludwig [4, pp. 486-487], the main characteristics that affect the performance of an amplifier are:

- Gain (dB);
- Operating frequency and bandwidth (Hz);
- Output power (dBm);
- DC operating point;
- Noise figure (dB);
- Input and output reflection coefficients.

In addition to this, it is necessary to take into account the effects, which negatively influence the amplifier parameters, such as gain compression, harmonic distortion, intermodulation distortion (IMD), cross modulation and heating. Gain compression is the nonlinear phenomenon that is difficult to predict accurately, and accordingly, is considered in this work.

2.1.2 Gain compression in high-power amplifiers

Pozar states [9, pp. 511-513] that due to the noise effects all realistic components are not ideally linear at low signal levels. These nonlinearities are negligible and it is usually assumed that an electrical device operates linearly. However, such assumptions cannot be adopted at high signal levels. Note, that for active components, such as transistors, these nonlinearities can be caused by gain compression. Let us consider the gain compression phenomenon in detail that will be useful for further discussions of BJT amplifiers.

The operation mode of the BJT, which is expressed by minimum and maximum realistic power range, can be divided into two regions: linear and nonlinear. Regarding to Ludwig [4, pp. 540-542], Pozar [9, pp. 511-513] and Kazimierczuk [10, pp. 27-28], the typical relationship between output P_{out} and input P_{in} powers is presented on a log-log scale in Figure 5. The characteristics of the ideal linear amplifier is presented by the straight line. In the linear region the output power P_{out} rises proportionally to the input power P_{in} incrementation. Then the output power reaches the point of the so-called *power saturation*, causing *a gain compression*. This region is specified as the nonlinear. The

point in nonlinear region at which the output power level decreases by 1 dB from the ideal characteristic is called the *1 dB compression point* and it is expressed by $P_{out,1dB}$ for amplifiers (and $P_{in,1dB}$ for mixers). The linear region is usually specified by the *dynamic range* d_R, which is the region between 1 dB compression point and the minimum detectable power $P_{out,min}$.

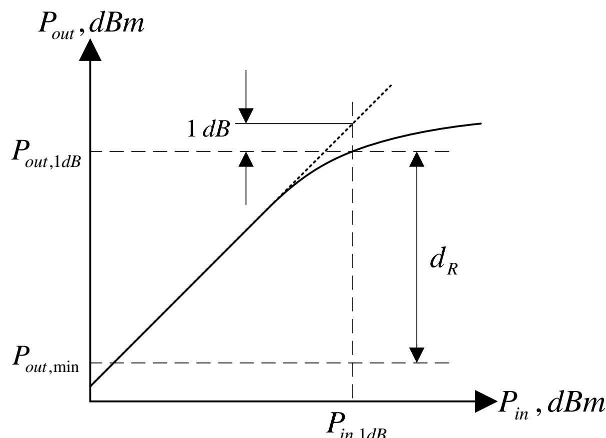


Figure 5: Power saturation.

The prediction of power saturation (or the gain compression) can be done by a number of methods, such as CAD simulations, statistical analytical models and others, and nowadays it is a topical problem.

2.2 Transistor models

The design of an amplifier is usually done with the help of the so-called equivalent circuit models of the transistor. These circuit models show the internal structure of the transistor and they are formed for alternating currents (AC) and voltages. As it is said in [4, p. 367], a number of large- and small-signal transistor models were developed during the past years. The large-signal model implies a common analysis used in electrical engineering, which assumes that the AC signals have high amplitude to produce nonlinear phenomena. The small-signal model assumes that the signals (voltages and currents) are small enough to use a linear circuit AC analysis techniques [7, p. 796].

The most known transistor models are the Ebers-Moll [11] and the Gummel-Poon [12] circuit models. These models characterize low-frequency and RF modes of operation, respectively. The so called hybrid-π small-signal model was developed from the large-signal Ebers-Moll circuit model, which consists of linear capacitors and resistances, and voltage-controlled current source expressed by transconductance g_m [7, pp. 799-802], [8, pp. 208-223], [4, pp. 367-388].

2.2.1 Large-signal model

The Ebers-Moll model [11] is a widely used large-signal model, which was introduced in 1954. This model takes into account essential phenomena, including a current flow through the $p-n$ junction. Its scheme is shown in Figure 6 [4, pp. 367-370]. Each $p-n$

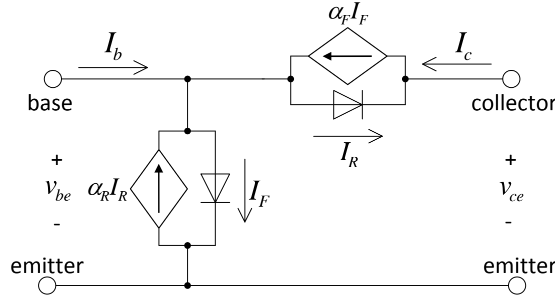


Figure 6: Static large-signal Ebers-Moll circuit model.

junction is presented by the diodes connected in forward and reverse polarity, and their interaction is denoted by the current-controlled current sources. Regarding [8, pp. 208-213] the transistor model is based on the Ebers-Moll equations that describe the large-signal characteristics of an ideal BJT

$$I_e = \alpha_R I_R - I_F, \tag{1}$$

$$I_c = \alpha_F I_F - I_R, \tag{2}$$

where α_R and α_F are the reverse and forward current gains. The diode currents I_R and I_F are expressed below, respectively

$$I_R = I_{cs}\left(e^{v_{bc}/v_T} - 1\right), \tag{3}$$

$$I_F = I_{es}\left(e^{v_{be}/v_T} - 1\right). \tag{4}$$

The reverse collector I_{cs} and emitter I_{es} saturation currents relate to the transistor saturation current I_s in the following way

$$I_s = \alpha_F I_{es} = \alpha_R I_{cs}. \tag{5}$$

The converted static Ebers-Moll model into the dynamic form is presented in Figure 7. The details on conversion of the static model into dynamic one are presented in Ludwig's book [4, pp. 367-373]. Note that the large-signal model characterizes the major processes in BJT. However, it cannot examine a number of phenomena exist in real transistors, such as a presence of emitter, base and collector resistances, an influence of the base-collector

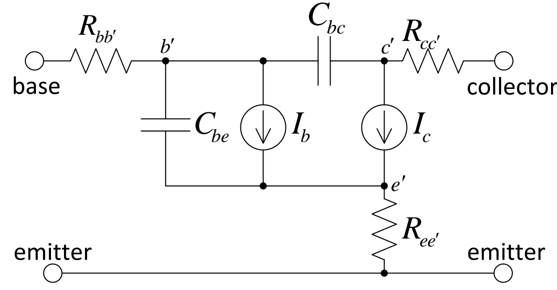


Figure 7: Dynamic large-signal Ebers-Moll model.

voltage on the saturation current I_s (Early effect) and an alteration of the base width when the collector voltage varies.

2.2.2 Small-signal hybrid-π model

According to Ludwig [4, pp. 376-380] the small-signal model was derived from the Ebers-Moll large-signal model by linearizing it. This linear small-signal hybrid-π model is presented in Figure 8. As can be seen in Figure 8, the collector current source is replaced by the voltage-controlled current source, which is specified by the transconductance g_m and the input voltage v_π. Moreover, the introduced resistance r_μ and the capacitor C_μ make the model more realistic taking into account the so-called Miller effect.

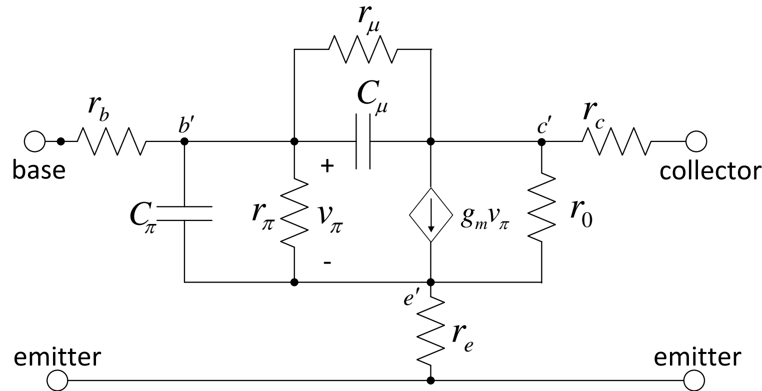


Figure 8: Small-signal hybrid-π Ebers-Moll BJT model.

This model serves for evaluation of small-signal parameters by expanding the input voltage V_{BE} and output current I_C near the bias point in terms of the small AC voltage v_{be} and collector current i_c

$$V_{BE} = V_{BE}^{Q} + v_{be}, \tag{6}$$

$$I_C = I_C^Q + i_c, \tag{7}$$

where current i_c is a multiplication of transconductance g_m and voltage v_{be}.

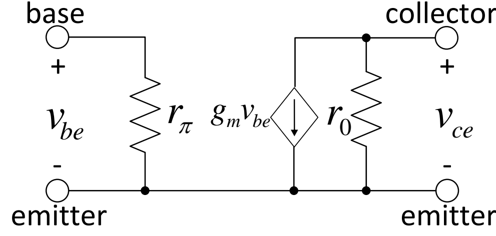


Figure 9: Simplified hybrid-π small-signal model.

Due to a high complexity of the small-signal model (Figure 8), the simplified hybrid-π model demonstrated in Figure 9 is commonly used in analysis [7, pp. 801-802]. Both Jaeger [7, pp. 801-802] and Ludwig [4, pp. 377] exploit the following parameters for defining the simplified small-signal hybrid-π model

- transconductance[1] g_m

$$g_m = \left.\frac{dI_C}{dV_{BE}}\right|_Q, \tag{8}$$

- small-signal current gain β_0 at operating point

$$\beta_0 = \left.\frac{dI_C}{dI_B}\right|_Q, \tag{9}$$

- input resistance r_π

$$r_\pi = \frac{\beta_0}{g_m}, \tag{10}$$

- output resistance r_0 at operating point

$$r_0 = \left.\frac{dV_{CE}}{dI_C}\right|_Q = \frac{V_A}{I_C^Q}, \tag{11}$$

where V_A is the Early voltage.

Despite its simplicity the generic hybrid-π model (Figure 9) allows covering the most essential phenomena: the linearity of resistors r_π and r_0, the Early effect and the relation between transconductance g_m and the input voltage v_{be}. However, at high frequencies the model cannot be applied to predict the nonlinear behavior of BJT due to the following reasons described below.

Let us consider a harmonic small-signal

$$v_{be}(t) = \hat{v}_{be} \sin(\omega t), \tag{12}$$

where the base-emitter voltage $v_{be}(t)$ with the amplitude $\hat{v}_{be}$ is superimposed on the bias

[1] The prefix *trans* in definition comes from the dependancy of an output upon the input [13, pp. 619-620]– [14, p. 109].

voltage, and the collector current $i_c(t)$ for low amplitudes of $\hat{v}_{be}$ is

$$i_c(t) \approx g_m \hat{v}_{be} \sin(\omega t). \tag{13}$$

Note that with a rise of the voltage $\hat{v}_{be}$, the collector current i_c increases until the BJT starts saturating. In case when the base-emitter voltage v_{be} drops, the collector current i_c decreases until the BJT is in a cut-off mode. Hence, the collector current i_c is limited or in other words is clipped for large values of $\hat{v}_{be}$, therefore, it imposes a constraint on the nonlinearity of the BJT. Moreover, there is a huge difference in phases between current i_c and voltage v_{be} at high frequencies.

By examining the relation between voltage $\hat{v}_{be}$ and collector current i_c, it can be concluded that the constant transconductance g_m in the simplified hybrid-π model is not taking into account the major phenomena, including clipping and phase difference. This problem is overcome in a quasi-linear model, which is described in the next subsection.

2.2.3 Quasi-linear transistor model

The quasi-linear transistor model presented in Figure 10 is the state-of-the-art approach developed in [5] and [6]. Its quasi-linearity is described by a number of linear components, including resistances r_π and r_0, shunt base-emitter C_{be} and collector-emitter C_{ce} capacitances, and a series connected C_{bc} that takes into account the Miller effect, and one nonlinear component known as transadmittance y_m.

In this quasi-linear transistor model the nonlinear transadmittance phasor

$$y_m = |y_m(\hat{v}_{be})| e^{j\phi}, \tag{14}$$

substitutes the transconductance g_m that allows using it at high frequencies. Indeed, the transadmittance magnitude $|y_m(\hat{v}_{be})|$ is a decreasing function of input voltage amplitude $\hat{v}_{be}$, while the phase angle ϕ specifies the phase difference between current i_c and base-emitter voltage v_{be}.

Let us derive the empirical transadmittance function for further analysis of the model.

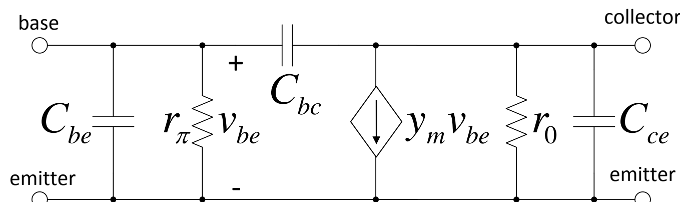


Figure 10: Quasi-linear transistor model used in the power saturation analysis.

For small input amplitudes of voltage $\hat{v}_{be}$ the transadmittance is constant and it is defined

$$|y_m(\hat{v}_{be})| = |y_{m0}|. \tag{15}$$

For large amplitudes of $\hat{v}_{be}$ the signal is no longer sinusoidal and as a result clipping appears, which leads to occurrence of the input frequency harmonic components. Moreover, the collector current amplitude $\hat{i}_c$ does not rise. Hence, it reaches its maximum $\hat{i}_{c,max}$ and the transadmittance magnitude becomes

$$|y_m(\hat{v}_{be})| = \frac{\hat{i}_c}{\hat{v}_{be}} = \frac{\hat{i}_{c,max}}{\hat{v}_{be}}. \tag{16}$$

As far as $i_{c,max}$ is constant, the transadmittance magnitude is inversely proportional to the input voltage $\hat{v}_{be}$. Thus, the transadmittace for small and large amplitudes $\hat{v}_{be}$ can be specified

$$|y_m(\hat{v}_{be})| = \begin{cases} |y_{m0}|, & \text{if } \hat{v}_{be} \leq \frac{\hat{i}_{c,max}}{|y_{m0}|} \\ \frac{\hat{i}_{c,max}}{\hat{v}_{be}}, & \text{if } \hat{v}_{be} > \frac{\hat{i}_{c,max}}{|y_{m0}|}. \end{cases} \tag{17}$$

The empirical equation that combines two cases from (17) is defined

$$|y_m(\hat{v}_{be})| = \frac{|y_{m0}|}{\left(1 + \left(\frac{\hat{v}_{be}|y_{m0}|}{\hat{i}_{c,max}}\right)^r\right)^{1/r}}, \tag{18}$$

where the empirical parameter $r > 0$ adjusts the curve near $\hat{v}_{be} = \frac{\hat{i}_{c,max}}{|y_{m0}|}$, as can be seen in

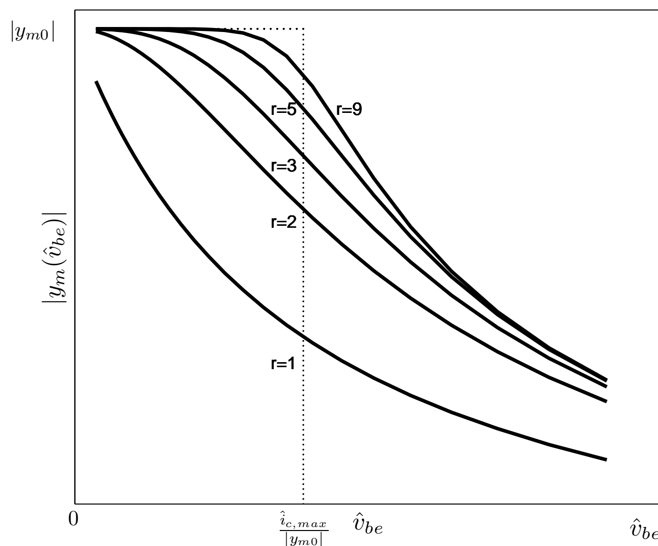


Figure 11: Smooth transadmittance functions (18) with different r values (solid lines). The piecewise transadmittance function (17) (dashed line).

Figure 11.

Note that the function (17) can be easily derived from (18). Indeed, at small values of $\hat{v}_{be}$ the function becomes $|y_m(\hat{v}_{be})| \approx |y_{m0}|$, whereas for large values of $\hat{v}_{be}$ it can be simplified to

$$|y_m(\hat{v}_{be})| = \frac{|y_{m0}|}{\left(\left(\frac{\hat{v}_{be}|y_{m0}|}{\hat{i}_{c,max}}\right)^r\right)^{1/r}} = \frac{\hat{i}_{c,max}}{\hat{v}_{be}}. \tag{19}$$

To summarize, the quasi-linear transistor model is a transformed version of the hybrid-π small-signal model. The usage of transadmittance y_m instead of transconductance g_m allows taking into account the phase difference between the collector current and the base-emitter voltage. This difference is denoted by the phase angle ϕ. The voltage-controlled current source is specified by the input voltage $\hat{v}_{be}$ and the nonlinear complex transadmittace $y_m = |y_m|e^{j\phi}$, which magnitude $|y_m|$ is amplitude dependent, while other model components are linear. The evaluated quasi-linear transistor model is going to be used in the further power saturation analysis.

2.3 Research goals

The quasi-linear transistor model is a logical improvement of the small-signal hybrid-π model, which has shown an excellent performance in oscillation analysis [5] – [6]. Its sufficiency at high frequencies makes it an ideal candidate for an amplifier design. However, it has never been used for amplifier analysis and prediction of power saturation in BJT. The major goal of this research is to attest the applicability of the quasi-linear transistor model to amplifier design and to verify the accuracy of the model in power saturation analysis. Therefore, the research is divided into three parts: measurements, quasi-linear analysis of power saturation (analytical model) and simulations. The accuracy and relevancy of the quasi-linear modeling is proved by obtaining the given approximate behavior of the power saturation curves shown in Figure 12. Let us go through the minor goals in

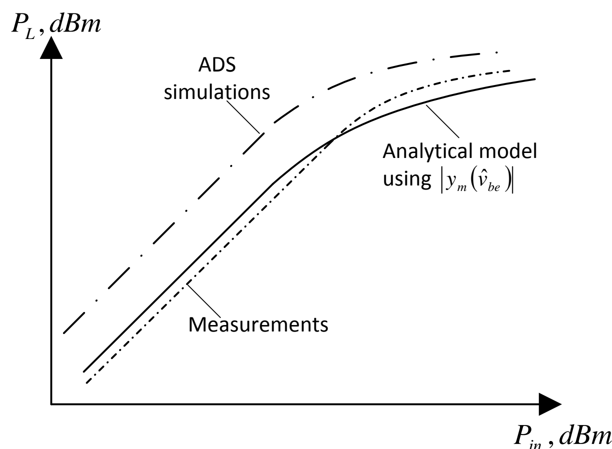


Figure 12: Research task.

more detail.

Firstly, we aim to measure the scattering S-parameters with frequency sweep that will be used as input in the quasi-linear model. For this reason six different BJT types (PN3563, NTE108, 2N5179, 2N5079, BFW16, BF959) are tested at the operating frequency $f = 100$ MHz and the bias point $V_{CE}^{Q} = 5$ V, $I_{C}^{Q} = 20$ mA. The measured S-parameters with power sweep are used to create the realistic power saturation curves. Moreover, a transadmittance magnitude $|y_{m0}|$, current $i_{c,max}$ and empirical parameter r are evaluated for further analytical usage. At last, the accuracy of measurements is verified by comparing the S-parameters with frequency and power sweeps at the user-specified point ($f = 100$ MHz and $P = -20$ dBm).

Secondly, we would like to perform the quasi-linear-based analytical modeling and for this reason the elements of the model (C_{be}, r_{π}, C_{bc}, y_{m0}, r_0, C_{ce}) and voltage $\hat{v}_{be}$ are to be derived from the measured S-parameters. Accordingly, the transadmittance $|y_m(\hat{v}_{be})|$ (18) is obtained using the measured collector current $i_{c,max}$, empirical parameter r and measured transadmittance y_{m0}. Lastly, the power at the load P_L is determined as a function of input power P_{in}.

Thirdly, the simulation procedure is done using the Agilent Advanced Design System (ADS) 2009 software. The simulations are to be performed based on the electrical scheme presented in Figure 4 and the power saturation curves are obtained.

To summarize it up, the accuracy and relevance of the suggested quasi-linear analytical model can be proved comparing the simulated, measured and modeled power saturation curves.

3 Measurements

The measurement procedure of the large-signal S-parameters is described in this Section. Firstly, the detailed calibration procedure of the network analyzer (NA) Hewlett Packard (HP) 8722D is presented. Secondly, the measurement setup is shown and thirdly, the component placement is discussed. The mentioned NA allows performing measurements in two modes: with frequency and power sweep. So the procedures of S-parameter measurements with frequency and power sweeps are considered and related graphs and tables are shown.

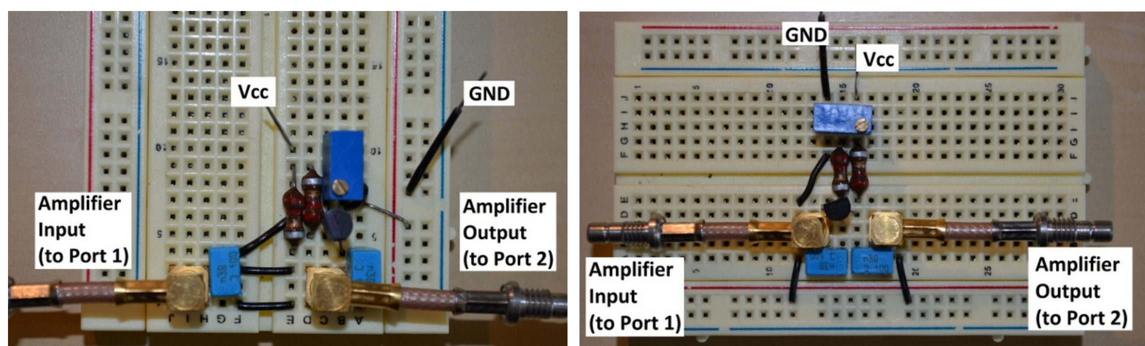
3.1 Calibration Procedure

The calibration procedure, which removes undesired effects of cable interconnection, has to be done before each type of the measurements with frequency and power sweeps. Moreover, the calibration differs slightly for the selected component placement, the two types of which are presented in Figure 13. Let us define acronyms for the first and second component placements as CP1 and CP2, respectively. Several compact component placements are considered due to the fact that a more compact disposition leads to better measurement results, e.g. the higher output power.

As can be seen from calibration algorithm, which is presented in Figure 14, the NA has to be warmed up for about 30 minutes after switching it on [16] –[18]. Then, the breadboard, on which the device under test (DUT) is placed, is connected to the NA.

The next step is to set up the settings of the NA that vary for frequency and power sweeps. In this thesis the following settings are selected as the ones that are commonly used in RF electronics (Table 3).

Note that in the algorithm (Figure 14) the physical buttons of the NA are presented in quotation marks, e.g. the button “Start”, while the functional buttons that are displayed in NA’s display menu are defined using the @ sign, e.g. @POWER@. In addition to this, the calibration is no longer accurate if any settings are changed during the measurements.



(a) Component placement 1 (CP1). (b) Component placement 2 (CP2).

Figure 13: Variants of the component placement on the breadboard.

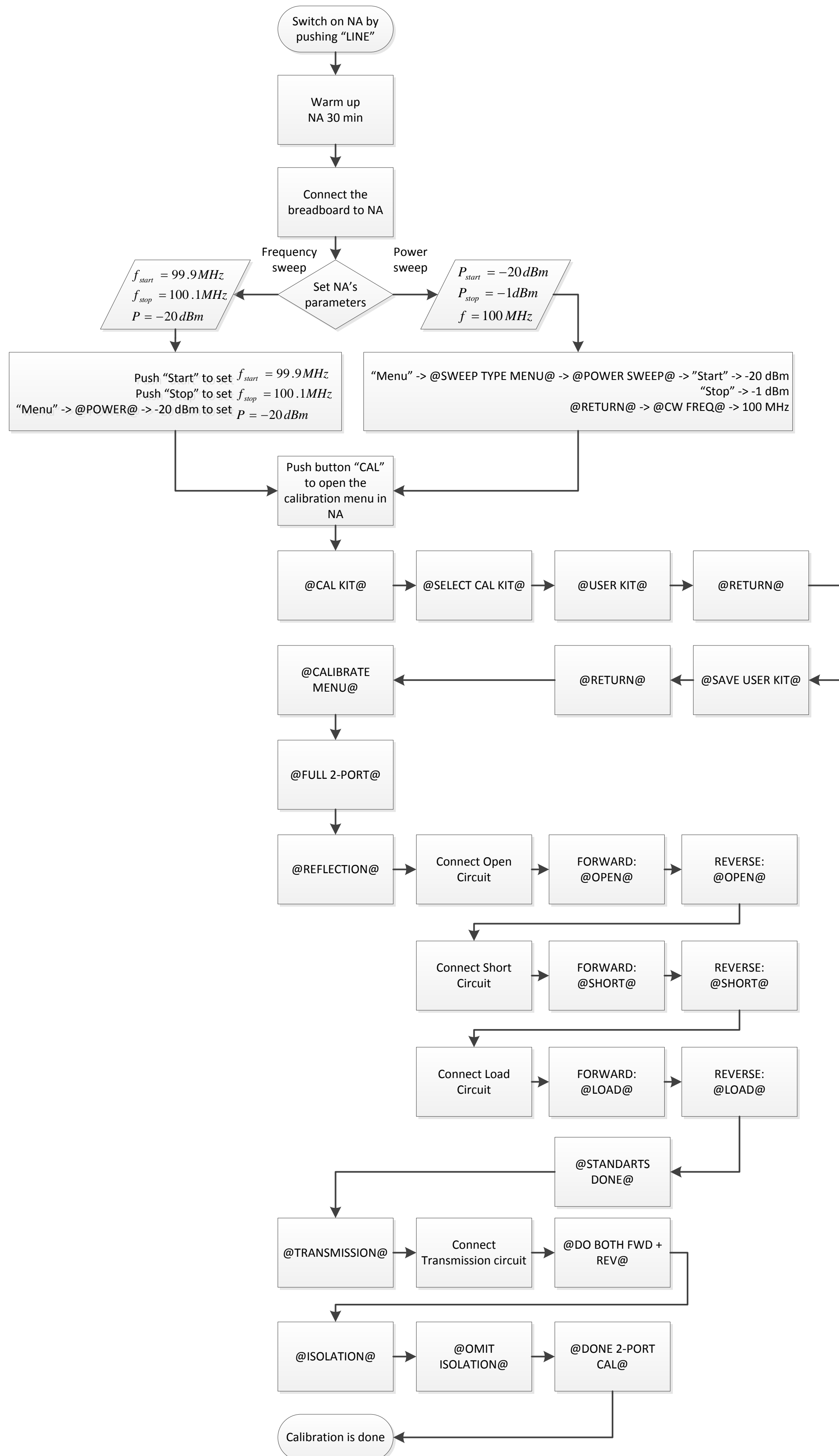


Figure 14: The calibration algorithm.

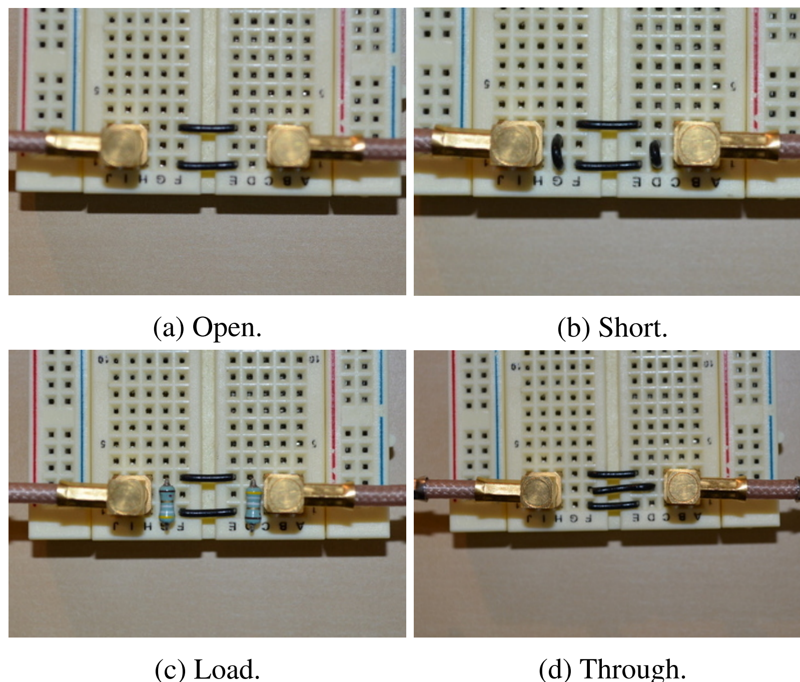
Table 3: The list of the amplifier electrical components.

Scenario	Values	Description
Frequency sweep	$P = -20$ dBm	output power of the NA
	$f_{start} = 99.9$ MHz	start frequency
	$f_{stop} = 100.1$ MHz	stop frequency
Power sweep	$f = 100$ MHz	operating frequency
	$P_{start} = -20$ dBm	start power
	$P_{stop} = -1$ dBm	stop power

After pushing the calibration button "CAL"the calibration kit has to be selected in the opened menu. Usually, the standard manufacturer calibration kits that comprise different connectors functioning as short, open and other circuits are used [15, pp. 89-99]. However, the DUT in these measurements is an amplifier, which consists of a number of elements placed on the breadboard. Hence, the calibration should be done using the breadboard (@USER KIT@ is selected) instead of the standard calibration kit.

An amplifier that is known to be a two port network requires the full two-port calibration procedure. For this reason the breadboard is connected to the NA using the so-called SOLT (Short-Open-Load-Through) connection, which is presented in Figure 15 for CP1 and in Figure 16 for CP2, where cables are connected to the two ports of NA: Port 1 and Port 2, respectively.

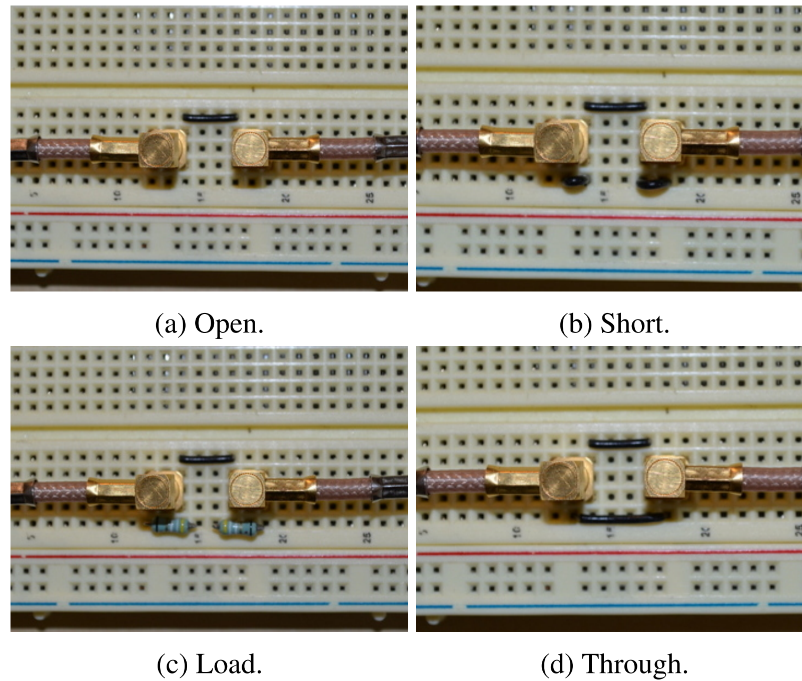
The first step in the full two-port calibration is a reflection calibration, which consists of an open, short and load calibrations that are further described in detail. Firstly, the breadboard is connected to the NA as an open circuit. As it was mentioned earlier,



(a) Open. (b) Short.

(c) Load. (d) Through.

Figure 15: The breadboard SOLT set for calibration (CP1).



(a) Open. (b) Short.

(c) Load. (d) Through.

Figure 16: The breadboard SOLT set for calibration (CP2).

the calibration procedure differs slightly for different component placements that results in two different connections presented in Figure 15a and Figure 16a. When an open circuit is connected the forward and reverse calibrations are done by pressing @FORWARD:OPEN@ and @REVERSE:OPEN@ buttons. Secondly, the short circuit is connected to the NA as it is shown in Figure 15b and Figure 16b for CP1 and CP2, respectively. Then, the forward and reverse calibrations are set by pushing the functional buttons @SHORT@. Thirdly, we conclude the reflection calibration procedure by connecting the load circuit in a way demonstrated in Figure 15c for CP1 and Figure 16c for CP2. The functional buttons @LOAD@ are pushed both for forward and reverse calibrations. It is worth mentioning that the NA HP 8722D offers three modes for the load calibration: “broadband”, “sliding” and “lowband” and the first one is selected for the given scenario.

The second step in a full two-port calibration is a transmission calibration. The breadboard is connected as a through element to the NA presented in Figures 15d, 16d for CP1 and CP2, respectively. Next, the transmission calibration is done automatically after pushing the functional button @DO BOTH FWD + REV@ in calibration menu.

The last step in calibration is the isolation that is omitted by pushing the functional button @OMIT ISOLATION@, as can be seen in Figure 14. Next, the button @DONE 2-PORT CAL@ is selected and the NA starts computing the calibration coefficients. After that the full-two port calibration is completed and the NA is prepared for measuring the scattering *S*-parameters of the DUT.

3.2 Measurement setup and component placement

In order to find the scattering S-parameters of the DUT using the network analyzer, the following measurement setup presented in Figure 17 is required. Note that the settings for both frequency and power sweeps were discussed in calibration procedure and they can be also seen in Figure 17 in the block "Network Analyzer".

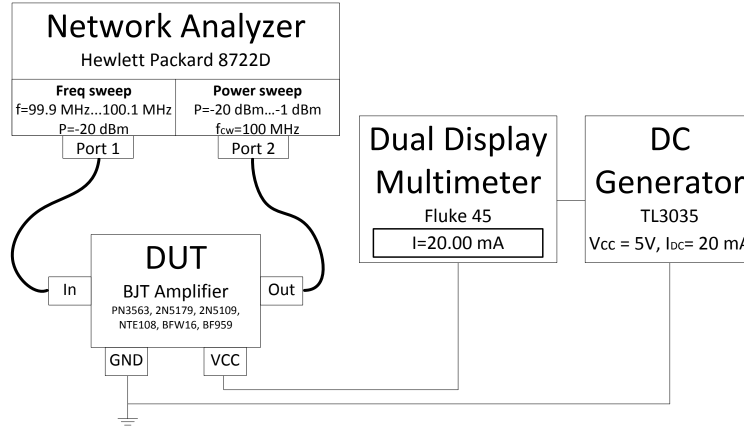


Figure 17: The S-parameter measurement setup.

Figure 17 shows that the input and output ports of the DUT are connected to the NA through the Port 1 and Port 2, respectively. The list of the electrical components that are used in amplifier design is presented in Table 4, while the electrical scheme of the amplifier is demonstrated in Figure 4. As it was mentioned earlier we used two compact component placements CP1 and CP2 (Figure 13a and 13b). The reason for this is that the operating frequency $f = 100$ MHz is in RF range and, therefore, the more compact component placement leads to less electromagnetic losses. As a result, the component placement that achieves higher gain (S_{21}) of an amplifier will be considered in an analytical modeling in Chapter 4.

The DC generator TL3035 allows setting the bias point of an amplifier (DUT). It produces the voltage $V_{CC} = 5$ V and the DC current $I_{DC} = 20$ mA, which comes to DUT through the Dual Display Multimeter Fluke 45. The value of the current I_{DC} is shown

Table 4: The list of the amplifier electrical components.

Component	Value	Specification	Note
C_1	390 pF	1830 B6 n39 J 100	DCB
C_2	390 pF	1830 B6 n39 J 100	DCB
L_1	2.2 μH	-	RFC
L_1	2.2 μH	-	RFC
R_b & R_c	-	T93 VB 20K 10%	potentiometer
BJT	DC bias: $V_{CC} = 5$ V, $I_{DC} = 20$ mA	PN3563, 2N5179, 2N5109, NTE108, BFW16, BF959	-

at the display for comfort bias point controlling, while tuning the potentiometer that is incorporated in amplifier.

3.3 S-parameter measurements: frequency sweep

The measuring of the large-signal S-parameters with frequency sweep is implemented by using the settings declared in Table 3. By considering an extremely narrow bandwidth $\Delta f = 0.2$ MHz we assure that the measured S-parameters represent accurate values at one point, i.e. at a certain frequency and a certain power level. We further measure the S-parameters for both component placements CP1 and CP2 using six different types of BJT presented in Table 4. Moreover, several transistors of the same type are tested to improve the overall accuracy of the measurements.

The universal method of S-parameter evaluation is the Smith Chart that allows visualizing the obtained results for the selected frequency range. We used the program Agilent Advanced Design System (ADS) 2009 to read in the measurement information and plot the S-parameters on the Smith Chart. Note that the markers are set at the point $f = 100$ MHz for every S-parameter S_{11}, S_{12}, S_{21} and S_{22}. Figure 18 demonstrates the obtained S-parameter presentation on the Smith Chart for transistor PN3563 and component placement CP1. The measured values of S-parameter magnitudes and phases for nine transistors of type PN3563, and their average values are presented in Table 5.

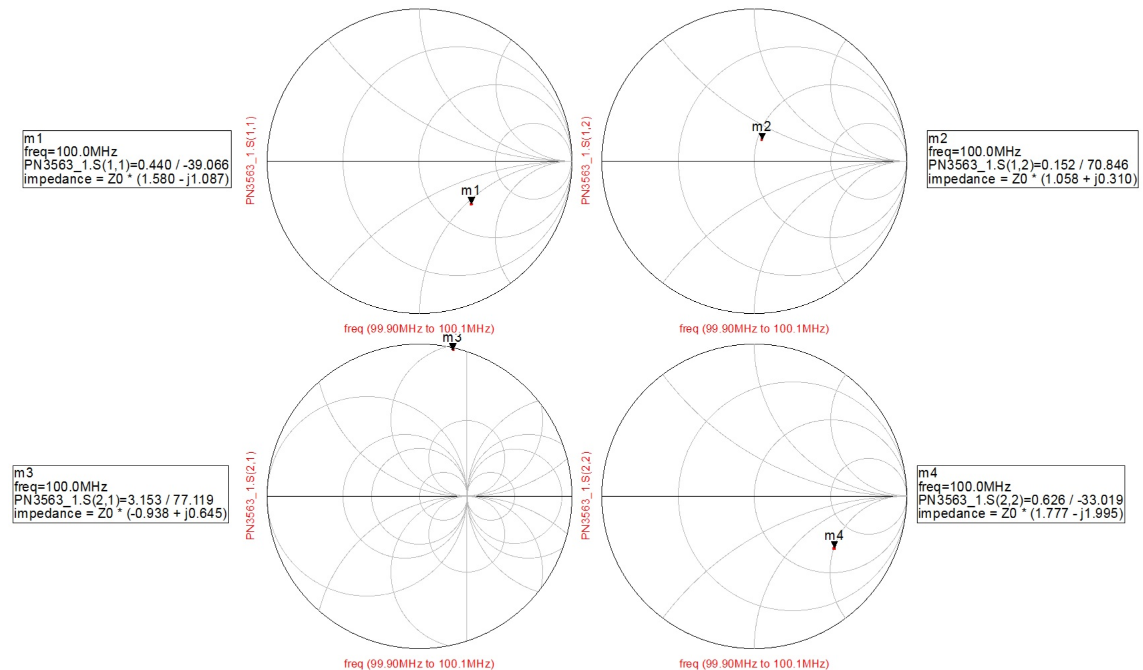


Figure 18: Measured S-parameters for BJT PN3563, CP1.

Then the measurement procedure is repeated for nine transistors of the same type using CP2. The values of the magnitudes and phases are presented in Table 6.

The S-parameters of a number of transistors specified by the parameter N are found for the rest five BJT types and both component placements CP1 and CP2. The average values of magnitudes and phases are demonstrated in Table 7. As can be seen from Tables 5–7, the gain ($|S_{21}|$) of the measured transistors for CP2 is at least 1 dB higher compared to CP1. Hence, we conclude that the component placement CP2 is more compact than CP1, leads to less electromagnetic losses.

Table 5: Measured S-parameters of nine PN3563. CP1, $f = 100$ MHz, $P = -20$ dBm.

N	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
1	0,440	-39,066	0,152	70,846	3,153	77,119	0,626	-33,019
2	0,432	-38,822	0,148	70,531	3,143	76,987	0,626	-32,579
3	0,435	-38,212	0,149	71,289	3,114	77,517	0,629	-32,650
4	0,388	-36,750	0,143	73,720	3,152	76,817	0,636	-33,789
5	0,430	-38,664	0,147	71,513	3,172	76,914	0,623	-32,862
6	0,431	-37,804	0,144	71,955	3,144	77,094	0,631	-32,623
7	0,433	-37,394	0,145	71,739	3,133	77,153	0,627	-33,073
8	0,426	-38,526	0,151	71,865	3,112	77,051	0,629	-32,458
9	0,427	-38,097	0,146	73,907	3,127	77,085	0,635	-32,632
AVERAGE	0,427	-38,148	0,147	71,929	3,139	77,082	0,629	-32,854

Table 6: Measured S-parameters of PN3563. CP2, $f = 100$ MHz, $P = -20$ dBm.

N	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
1	0,345	-93,577	0,126	68,102	4,417	86,819	0,383	-26,896
2	0,342	-94,556	0,122	71,710	4,372	86,331	0,384	-27,003
3	0,336	-95,946	0,124	69,414	4,390	86,276	0,383	-26,449
4	0,305	-103,526	0,120	71,175	4,369	86,810	0,395	-28,704
5	0,335	-93,288	0,122	68,991	4,338	86,147	0,393	-26,758
6	0,327	-91,150	0,125	69,921	4,300	85,924	0,394	-26,180
7	0,338	-92,514	0,131	70,952	4,335	86,047	0,394	-26,333
8	0,326	-93,763	0,129	71,295	4,288	85,959	0,398	-25,605
9	0,334	-96,043	0,124	68,889	4,344	86,308	0,391	-26,085
AVERAGE	0,332	-94,929	0,125	70,050	4,350	86,291	0,391	-26,668

Table 7: Measured S-parameters of NTE108, $f = 100$ MHz, $P = -20$ dBm.

N	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
NTE108								
CP1								
1	0,426	-40,165	0,154	69,107	3,008	75,898	0,626	-33,950
2	0,400	-40,848	0,151	71,997	3,023	75,059	0,630	-33,356
AVERAGE	0,413	-40,507	0,153	70,552	3,016	75,479	0,628	-33,653
CP2								
1	0,336	-94,777	0,135	67,283	4,076	85,032	0,399	-27,135
2	0,324	-98,535	0,130	68,482	4,100	84,458	0,401	-26,830
AVERAGE	0,330	-96,656	0,133	67,883	4,088	84,745	0,400	-26,983
BF959								
CP1								
1	0,413	-30,739	0,142	74,255	3,806	77,674	0,596	-31,765
2	0,423	-30,610	0,143	72,273	3,795	77,452	0,594	-31,724
AVERAGE	0,418	-30,675	0,143	73,264	3,801	77,563	0,595	-31,745
CP2								
1	0,281	-112,173	0,110	72,504	5,699	86,660	0,273	-24,543
2	0,273	-108,037	0,111	72,442	5,687	86,835	0,264	-25,880
AVERAGE	0,277	-110,105	0,111	72,473	5,693	86,748	0,269	-25,212
BFW16								
CP1								
1	0,351	-22,303	0,157	79,283	3,217	78,280	0,549	-11,062
2	0,322	-21,945	0,160	78,579	3,331	77,876	0,530	-10,692
3	0,269	-23,633	0,161	80,396	3,188	76,950	0,538	-10,568
AVERAGE	0,314	-22,627	0,159	79,419	3,245	77,702	0,539	-10,774
CP2								
1	0,350	-146,580	0,131	71,231	4,584	79,896	0,127	-40,095
2	0,325	-149,318	0,135	70,497	4,570	78,899	0,121	-27,534
3	0,379	-158,507	0,121	72,565	4,403	78,145	0,123	-33,595
AVERAGE	0,351	-151,468	0,129	71,431	4,519	78,980	0,124	-33,741
2N5179								
CP1	0,454	-30,657	0,144	73,497	3,744	78,605	0,608	-31,211
CP2	0,371	-156,452	0,12	73,196	4,47	78,437	0,129	-28,987
2N5109								
CP2	0,371	-156,452	0,12	73,196	4,47	78,437	0,129	-28,987

3.4 S-parameter measurements: power sweep

This section presents the measurement results of S-parameters measured with power sweep (the settings are declared in Table 3), which is particularly useful for investigating the power saturation (or gain compression) effects [15, pp. 294-295]. Although the NA HP 8722D uses the default power ranges, such as $P = -40 \ldots -25$ dBm or $P = -25 \ldots -5$ dBm, it is possible to set a power sweep in the NA manually. In this thesis we are interested in the widest power range that starts from $P_{start} = -20$ dBm. During the gain compression measurements we empirically found out that the actual maximum value of

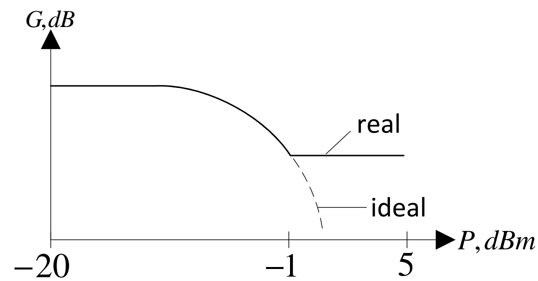


Figure 19: Ideal and real measured compression curves.

$P_{stop} = -1$ dBm when $P_{start} = -20$ dBm, as can be seen in Figure 19. Note that the NA guides [16], [17] specify the maximum output power of NA $P_{stop} = 5$ dBm.

An example of the measured S_{11}, S_{12}, S_{21} and S_{22} parameters of a transistor of the type PN3563 plotted on the Smith Chart is presented in Figure 20. As can be seen in Figure 20, markers are set at the point $P = -20$ dBm (NOTE: the ADS 2009 uses the default form “freq=-20 Hz”, which has to be interpreted as “power=-20 dBm”). The measured values of S-parameter magnitudes and phases for component placement CP1 at the point $P = -20$ dBm and operating frequency $f = 100$ MHz are presented in Table 8. The measured magnitudes and phases of S-parameters using CP2 are shown in Table 9. On comparing the values of $|S_{21}|$ taken from Table 8 and Table 9 we repeatedly ascertain that the component placement CP2 with higher magnitude value has less electromagnetic losses.

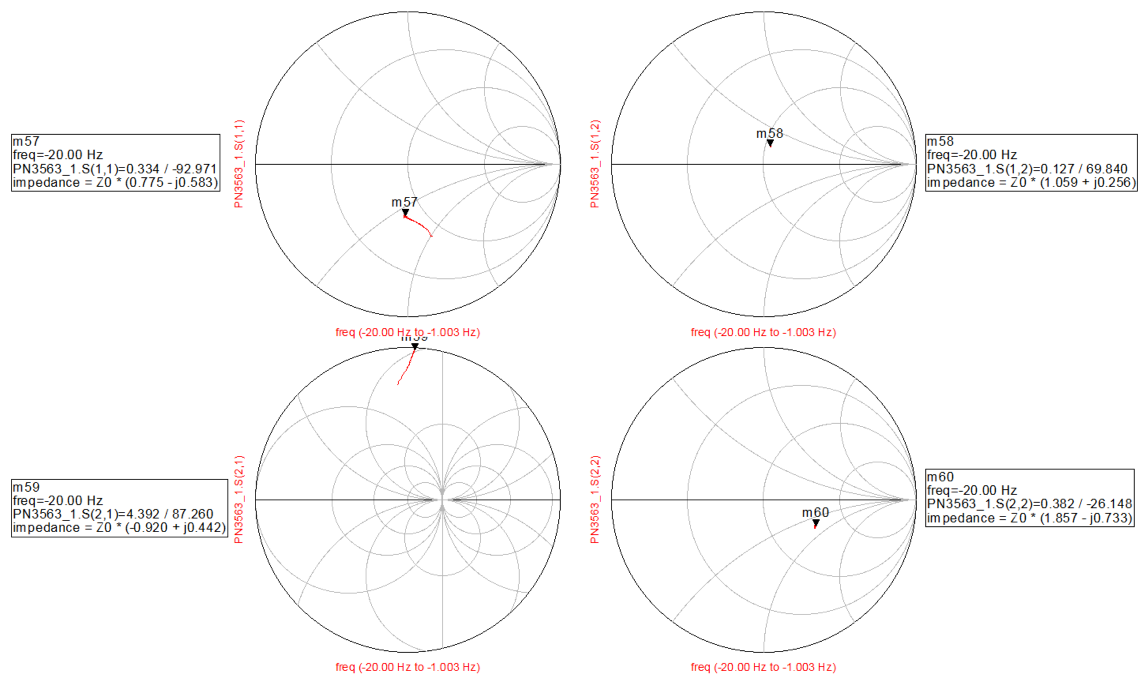


Figure 20: Measured S-parameters of one PN3563 with power sweep. CP2, $f = 100$ MHz, $P = -20 \ldots -1$ dBm.

Table 8: Measured S-parameters of PN3563. CP1, $P = -20$ dBm, $f = 100$ MHz.

N	$\lvert S_{11}\rvert$	$\angle S_{11}$	$\lvert S_{12}\rvert$	$\angle S_{12}$	$\lvert S_{21}\rvert$	$\angle S_{21}$	$\lvert S_{22}\rvert$	$\angle S_{22}$
1	0,428	-40,950	0,162	69,784	3,125	77,448	0,605	-33,363
2	0,419	-41,223	0,161	71,402	3,132	77,343	0,602	-33,041
3	0,424	-40,194	0,154	72,484	3,129	77,512	0,609	-32,920
4	0,380	-39,557	0,151	71,969	3,133	77,470	0,617	-32,944
5	0,422	-41,211	0,156	71,183	3,154	77,166	0,604	-33,130
6	0,423	-40,649	0,153	71,178	3,129	77,320	0,611	-33,000
7	0,420	-39,764	0,153	72,030	3,118	77,431	0,607	-32,961
8	0,419	-39,612	0,153	72,477	3,104	77,518	0,611	-32,568
9	0,412	-40,280	0,153	70,702	3,115	77,074	0,610	-32,968
AVERAGE	0,416	-40,382	0,155	71,468	3,127	77,365	0,608	-32,988

Table 9: Measured S-parameters of PN3563. CP2, $P = -20$ dBm, $f = 100$ MHz.

N	$\lvert S_{11}\rvert$	$\angle S_{11}$	$\lvert S_{12}\rvert$	$\angle S_{12}$	$\lvert S_{21}\rvert$	$\angle S_{21}$	$\lvert S_{22}\rvert$	$\angle S_{22}$
1	0,334	-92,971	0,127	69,840	4,392	87,260	0,382	-26,148
2	0,328	-93,374	0,124	68,781	4,348	87,136	0,389	-25,803
3	0,334	-94,512	0,124	68,219	4,355	87,121	0,395	-26,167
4	0,296	-100,450	0,121	71,426	4,340	87,214	0,396	-26,778
5	0,329	-91,686	0,127	70,950	4,339	86,904	0,396	-25,585
6	0,331	-92,988	0,130	70,762	4,321	86,930	0,400	-25,158
7	0,333	-91,666	0,124	68,900	4,327	86,526	0,389	-25,550
8	0,324	-92,985	0,124	70,195	4,316	86,621	0,397	-25,707
9	0,331	-94,799	0,122	70,101	4,326	86,998	0,394	-25,357
AVERAGE	0,327	-93,937	0,125	69,908	4,340	86,968	0,393	-25,806

The gain compression curves obtained by the NA represent the equivalent form of the power saturation [15, pp. 301-302]. Figure 21 presents the family of gain compression curves for component placement CP2 of nine transistors of type PN3563.

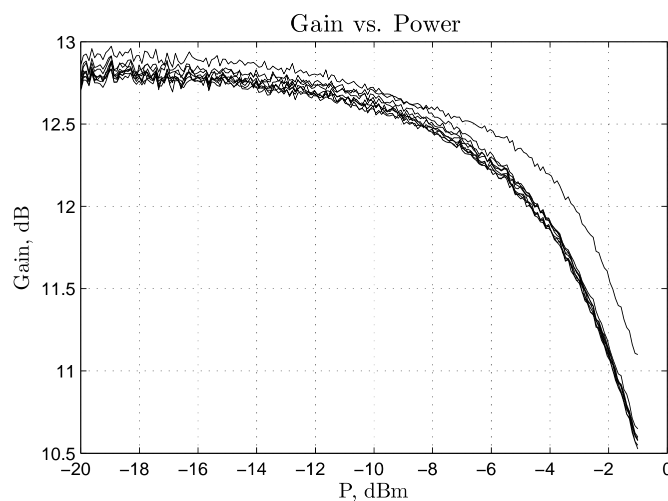


Figure 21: Family of gain compression curves. BJT PN3563, component placement CP2.

We further would like to derive the transadmittance y_{m0} from the measured S-parameters by using the following detailed steps:

1. the measured values of S-parameter magnitudes and phases are written in txt-files by exporting them from ADS 2009;

2. values from txt-files are read in MATLAB and average values for S-parameter magnitudes and phases are formed for a number of transistors of the selected type (e.g. PN3563);

3. the S-parameters in an angular form are transformed to a complex form and further converted to Y-parameters using the MATLAB RF Toolbox function `s2y(S, Z0)`, where `S` - is the 2×2 matrix that contains the S-parameters and `Z0` is a characteristic impedance $Z_0 = 50\ \Omega$;

4. the transadmittance y_{m0} is calculated

$$y_{m0} = Y_{21} - Y_{12}, \tag{20}$$

   where Y_{21} and Y_{12} are the elements of Y-matrix;

5. the voltage v_{be} is calculated

$$v_{be} = \sqrt{2}\left|\frac{Z_{in}}{Z_{in}+Z_0}\right|\sqrt{4P_{avg}Z_0}, \tag{21}$$

   where P_{avg} is equal to the NA output power $P = -20 ... -1$ dBm and impedance Z_{in} is found

$$Z_{in} = Z_0\frac{1+S_{11}}{1-S_{11}}. \tag{22}$$

6. at last, the transadmittance y_{m0} is plotted as a function of voltage v_{be} (Figure 22).

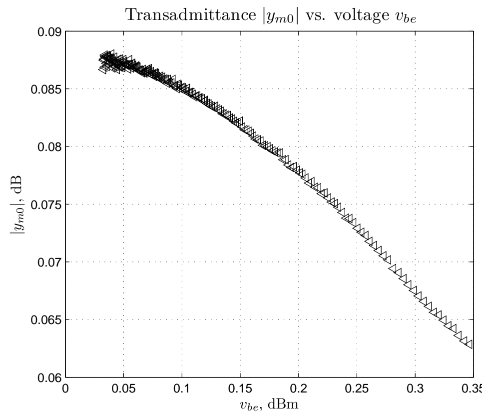
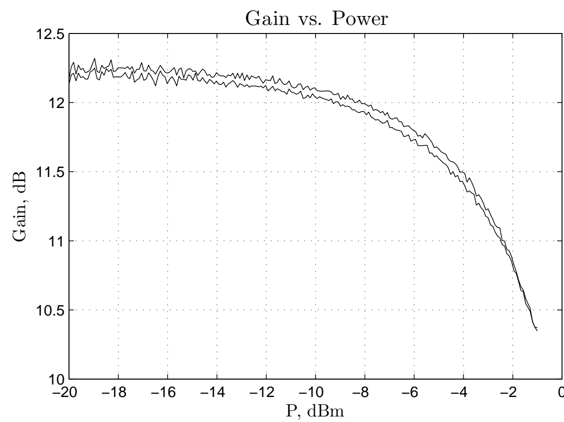


Figure 22: Transadmittance y_{m0} as a function of voltage v_{be} for BJT PN3563.

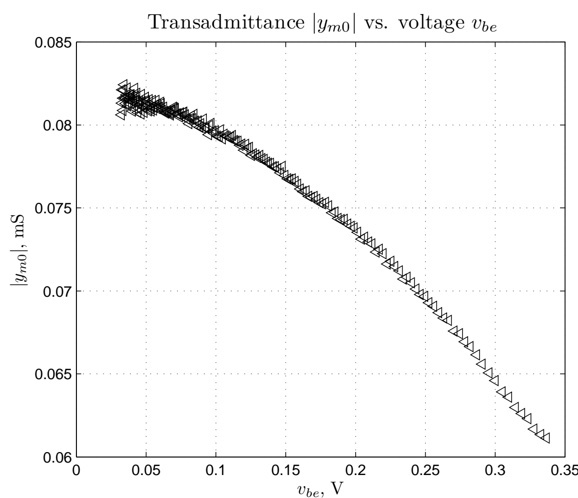
The S-parameters of a number of transistors specified by the parameter N are found for the rest five BJT types and both component placements CP1 and CP2. The average values of magnitudes and phases are demonstrated in Tables 10 – 14. The gain compression curves along with the transadmittance y_{m0} behaviors are presented in the following pages in Figures 23 – 27.

Table 10: Measured S-parameters of NTE108 for component placements CP1 and CP2.

N	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
CP1								
1	0,416	-41,627	0,162	69,443	2,980	75,958	0,613	-34,182
2	0,398	-42,821	0,160	69,267	2,996	75,328	0,608	-33,936
AVERAGE	0,407	-42,224	0,161	69,355	2,988	75,643	0,611	-34,059
CP2								
1	0,327	-93,089	0,135	70,266	4,043	85,602	0,407	-25,449
2	0,316	-98,043	0,132	69,763	4,060	84,776	0,406	-25,487
AVERAGE	0,322	-95,566	0,134	70,015	4,052	85,189	0,407	-25,468



(a)

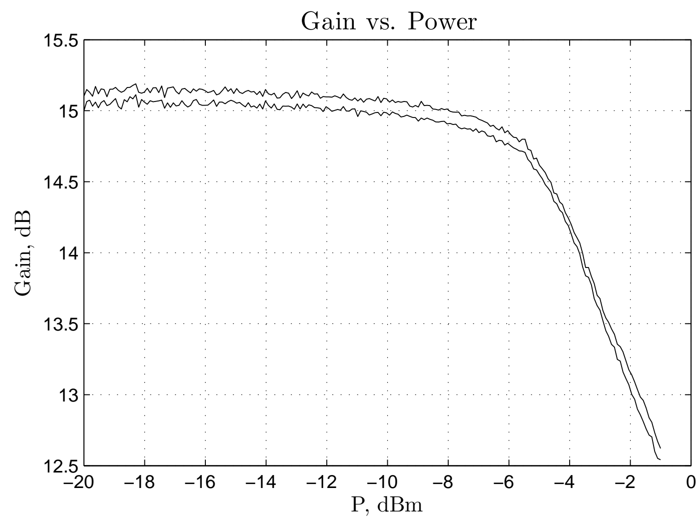


(b)

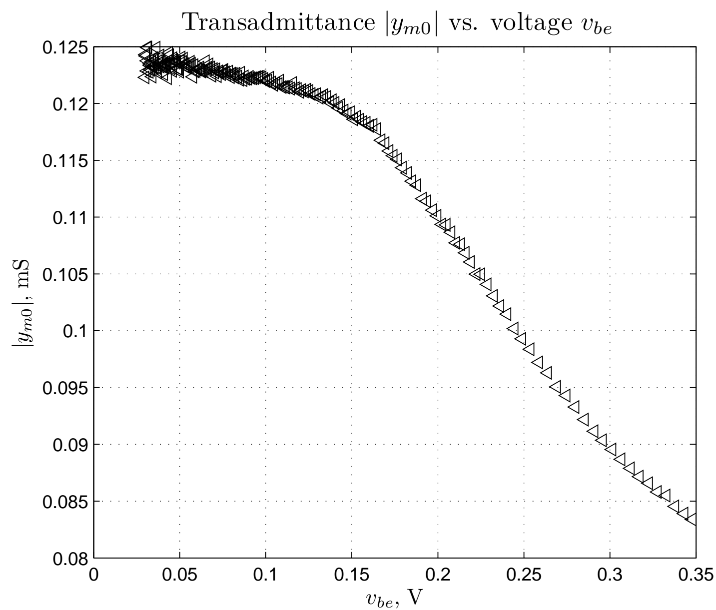
Figure 23: Measurement results for BJT NTE108: (a) the gain compression curves; (b) the transadmittance $y_{m0}(v_{be})$ behavior.

Table 11: Measured S-parameters of BF959.

N	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
CP1								
1	0,400	-32,716	0,145	73,862	3,782	77,788	0,571	-31,961
2	0,408	-31,325	0,149	72,527	3,783	77,788	0,579	-32,357
AVERAGE	0,404	-32,021	0,147	73,195	3,783	77,788	0,575	-32,159
CP2								
1	0,267	-109,415	0,112	73,526	5,623	87,352	0,283	-22,631
2	0,269	-108,293	0,108	73,521	5,691	87,571	0,272	-23,704
AVERAGE	0,268	-108,854	0,110	73,524	5,657	87,462	0,278	-23,168



(a)

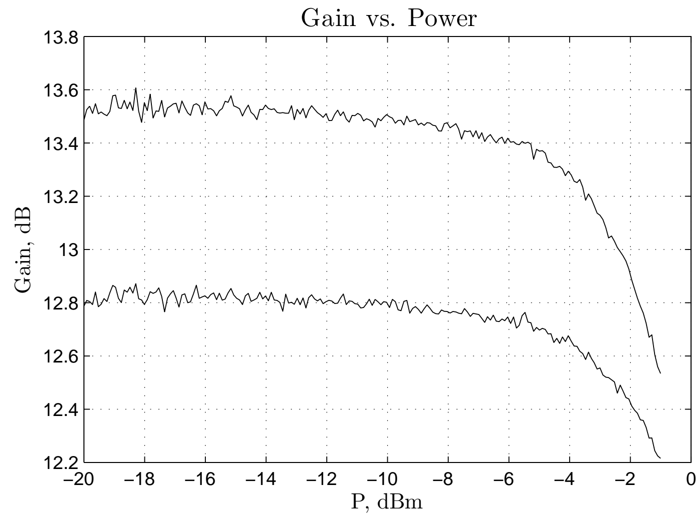


(b)

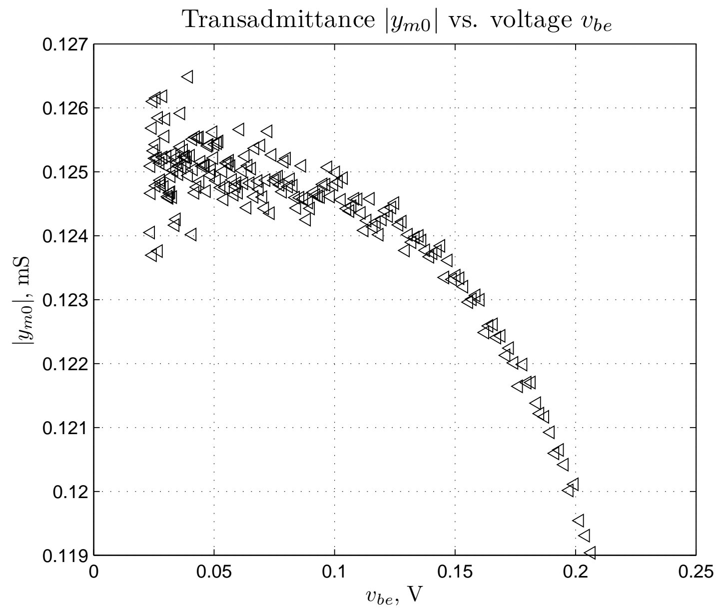
Figure 24: Measurement results for BJT BF959: (a) the gain compression curves; (b) the transadmittance $y_{m0}(v_{be})$ behavior.

Table 12: Measured S-parameters of BFW16, component placement CP2.

N	$\lvert S_{11}\rvert$	$\angle S_{11}$	$\lvert S_{12}\rvert$	$\angle S_{12}$	$\lvert S_{21}\rvert$	$\angle S_{21}$	$\lvert S_{22}\rvert$	$\angle S_{22}$
1	0,298	-138,901	0,142	68,872	4,359	79,593	0,177	-31,832
2	0,366	-152,370	0,120	71,940	4,724	80,739	0,088	-34,341
AVERAGE	0,330	-147,574	0,133	71,117	4,549	80,255	0,154	-32,705



(a)

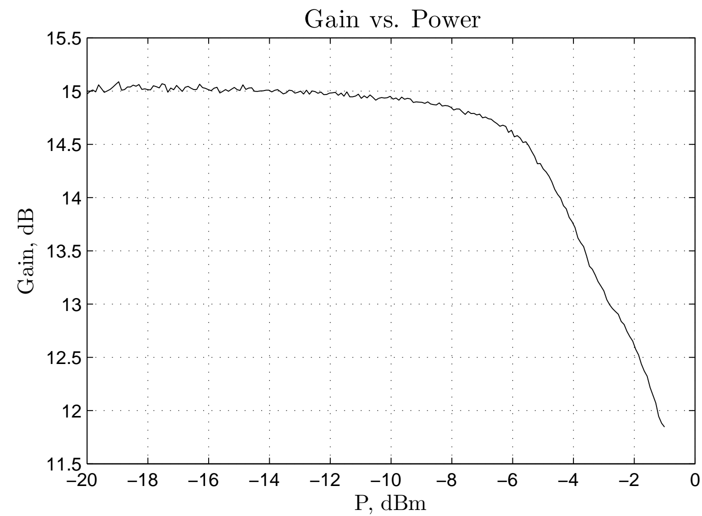


(b)

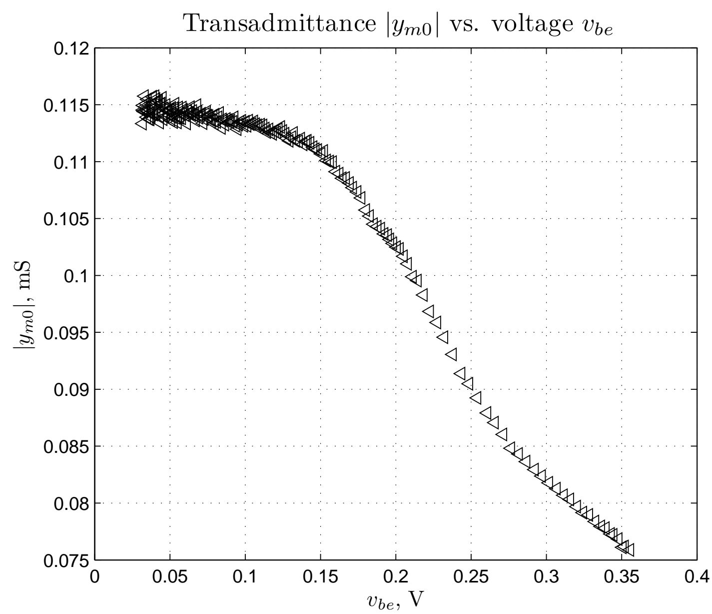
Figure 25: Measurement results for BJT BFW16: (a) the gain compression curves; (b) the transadmittance $y_{m0}(v_{be})$ behavior.

Table 13: Measured S-parameters of 2N5179.

N	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
CP1	0,439	-32,036	0,153	71,54	3,739	78,669	0,582	-31,459
CP2	0,345	-94,937	0,118	72,397	5,606	88,882	0,294	-27,007



(a)

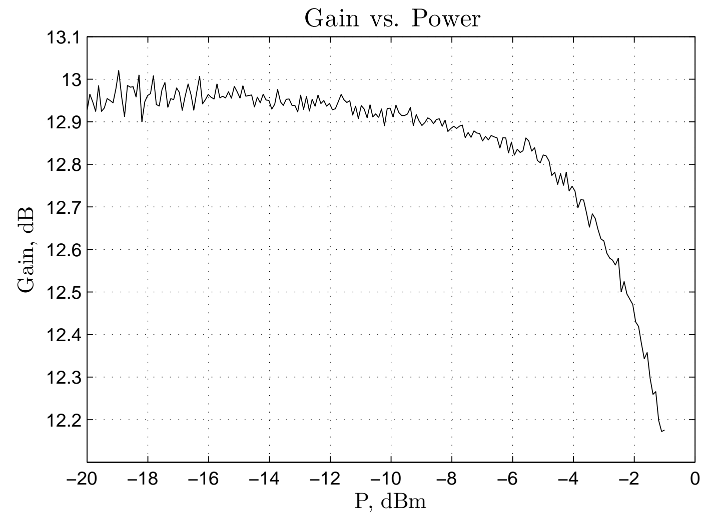


(b)

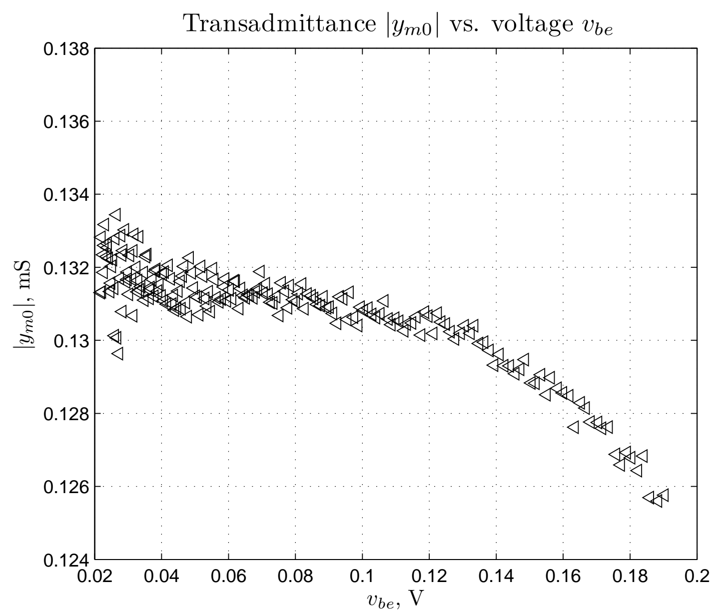
Figure 26: Measurement results for BJT 2N5179: (a) the gain compression curve; (b) the transadmittance $y_{m0}(v_{be})$ behavior.

Table 14: Measured S-parameters of 2N5109.

N	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
CP2	0,371	-156,452	0,120	73,196	4,470	78,437	0,129	-28,987



(a)



(b)

Figure 27: Measurement results for BJT 2N5109: (a) the gain compression curve; (b) the transadmittance $y_{m0}(v_{be})$ behavior.

Figure 28 shows the measured magnitudes of transadmittances of all tested transistors (presented in color), while the solid black curves are plotted using the least squares fitting [20, pp. 577-590] in the software environment “R” [21].

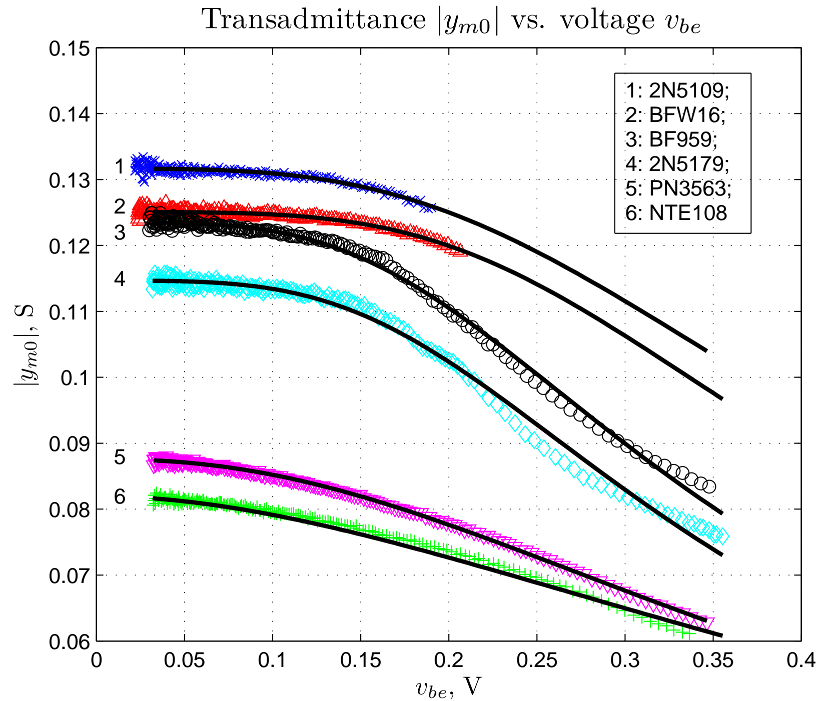


Figure 28: The measured $|y_{m0}|$ (symbols) vs. v_{be} and the fitted functions (solid lines) of the measured transistors at bias point $I_C^Q = 20$ mA, $V_{CE}^Q = 5$ V.

The procedure of finding the fitted curves by means of the least squares method is described in detail in the following steps:

1. the measured values of transadmittance magnitudes and voltage v_{be} are imported to the “R” as vectors;

2. the function `nls` is used for the least squares fitting, which input parameters comprise the following empirical equation of transadmittance

$$|y_m(v_{be})| = \frac{|y_{m0}|}{\left(1 + \left(\frac{v_{be}|y_{m0}|}{i_{c,max}}\right)^r\right)^{1/r}}, \tag{23}$$

   and the initial user-specified values of the transadmittance $|y_{m0}| = 0.1$ S, current $i_{c,max} = 40$ mA and the empirical parameter $r = 2$. The output of the function contains the target coefficient values of $|y_{m0}|$, $i_{c,max}$, r. Results for all measured transistors are presented in Table 15;

3. on plugging the values of $|y_{m0}|$, $i_{c,max}$, r into the equation (23) the fitted curves are constructed (solid black curves in Figure 28).

Table 15: The evaluated values of $|y_{m0}|$, $i_{c,max}$ and r.

N	Transistor type	$\|y_{m0}\|$ mS	$i_{c,max}$ mA	r
1	2N5109	131.64	43.04	3.37
2	BFW16	125.06	38.41	3.99
3	BF959	123.52	30	3.62
4	2N5179	114.66	27.51	3.65
5	PN3563	87.59	28.84	2.29
6	NTE108	82	33.71	1.89

In this thesis the accuracy of the measurements plays an essential role and can be verified by comparing the S-parameters with frequency and power sweeps. We state that their tolerance that do not exceed 10% corresponds to the relevant measurement results. Indeed, as can be seen in Tables 5 – 14 the given condition is fulfilled. Moreover, the power saturation graphs for transistor PN3563 are constructed for both power and frequency sweeps according to two types of component placements. As can be seen in Figure 29, the power saturation curves with power and frequency sweeps for the selected component placement are almost identical that assures the reliability of the measurement setup in an illustrative way. In addition to this, the difference between power saturation curves from different component placements is about 3 dBm that allows evaluating the role of compact electrical scheme on the breadboard. Thus, the measured S-parameters for CP2 will be used for further analytical modeling.

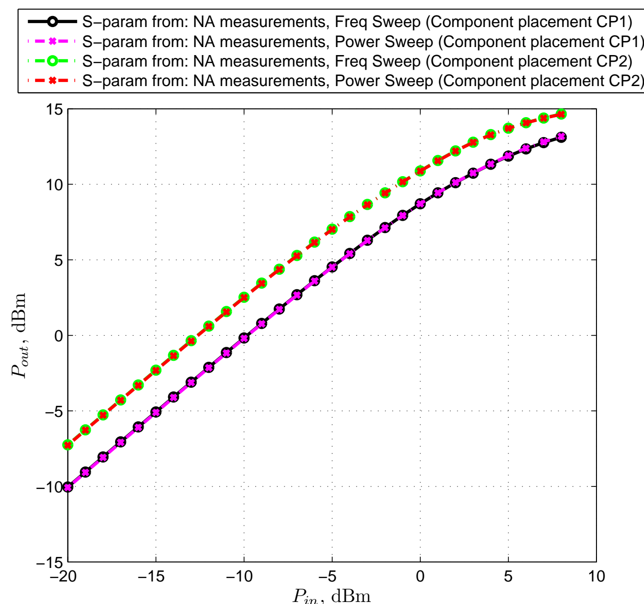


Figure 29: The power saturation graphs for BJT PN3563 for CP1 and CP2 both for frequency and power sweeps.

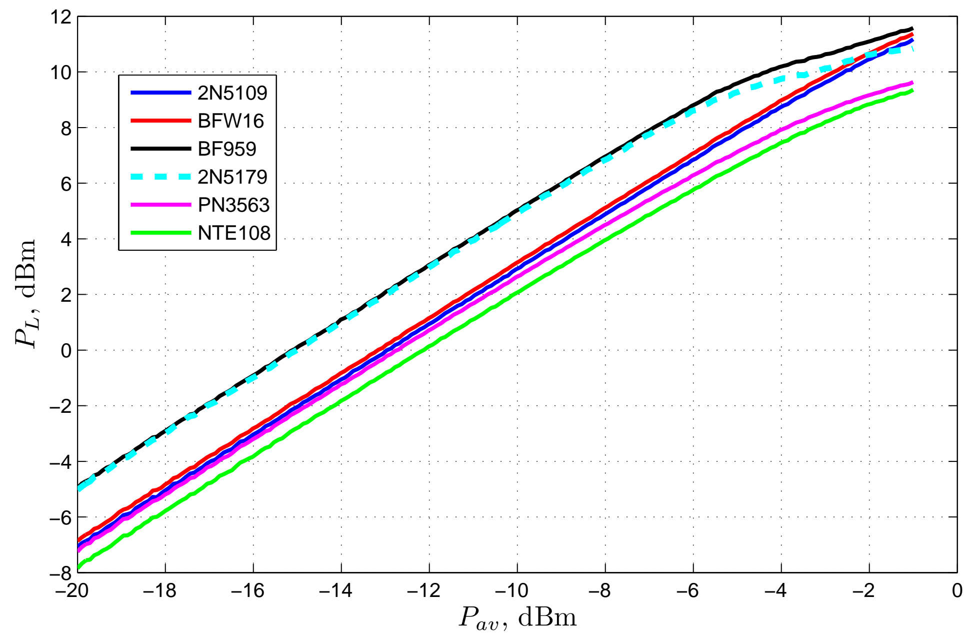


Figure 30: The power saturation curves of all measured transistors.

At last, the power saturation curves of all measured transistors for CP2 and power sweep are presented in Figure 30. The obtained results are used in the following analytical modeling presented in Chapter 4 and in Chapter 6, where the comparative analysis is held.

4 Quasi-linear analytical modeling

This chapter presents the power saturation analysis in BJT using the quasi-linear transistor model discussed in Section 2.2.3. Firstly, the extraction of the circuit element values of the quasi-linear transistor model is described for the selected transistor type PN3563. Secondly, the base-emitter voltage $\hat{v}_{be}$ and the transadmittance y_m are obtained from the measured S-parameters (Chapter 3) and, thirdly, the evaluation of the load power P_L is presented using the nodal analysis. Lastly, both the transadmittance magnitude $|y_m(\hat{v}_{be})|$ as a function of voltage $\hat{v}_{be}$ and the power saturation curves are constructed for six different types of BJT.

4.1 Circuit element values extraction

The amplifier (Figure 4) can be analyzed using the quasi-linear transistor model demonstrated in Figure 31. Here, the generator is specified by the voltage source E_g and the resistance $R_g = 50\ \Omega$, whereas the load is denoted by the resistance $R_L = 50\ \Omega$. The characteristic impedance Z_0 of the quasi-linear model is assumed to be equal to 50 Ω. The available power of a generator is the maximum power it can deliver to a load when the load impedance is to be freely selected. The expression for available power from the source in watts (W) is

$$P_{av} = \frac{|E_g^2|}{4\mathrm{Re}(Z_g)} = \frac{|E_g^2|}{4R_g}, \tag{24}$$

from which E_g is determined

$$E_g = \sqrt{4P_{av}R_g}. \tag{25}$$

Let us use the average values of the measured S-parameters for PN3563 with frequency sweep (Table 6) to express the transistor model (26). According to the measurement results (Chapter 3) the S-parameters both with frequency and power sweeps can be considered for the model description.

$$\begin{cases} S_{11} = 0.332\angle-94.9^\circ \\ S_{12} = 0.125\angle 70.05^\circ \\ S_{21} = 4.35\angle 86.3^\circ \\ S_{22} = 0.391\angle-26.7^\circ. \end{cases} \tag{26}$$

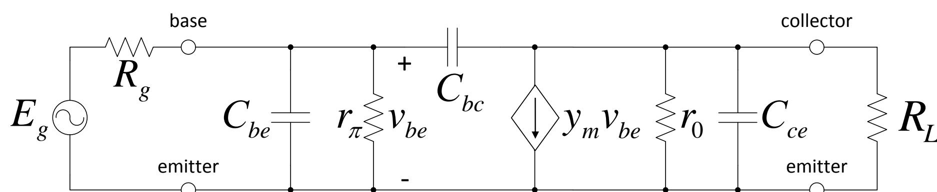


Figure 31: The quasi-linear transistor model is connected to generator and load.

The extraction of the numerical values of every element (C_{be}, r_π, C_{bc}, y_{m0}, r_0, C_{ce}) of the quasi-linear model is performed by the algorithm defined in Figure 32, which is clarified in the following steps:

1. convert the S-parameters to the admittance Y-parameters;
2. find the theoretical Y-parameters of the quasi-linear transistor model in terms of the element values (C_{be}, r_π, C_{bc}, y_{m0}, r_0, C_{ce});
3. equate the theoretical expressions and obtained Y-parameters from the measured S-parameters, and find the element values.

Let us go thoroughly through the above mentioned steps. Firstly, the conversion equations that transform S-parameters to Y-parameters are found, e.g. in [9, p. 192]

$$\begin{cases} Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{Z_0\Delta} \\ Y_{12} = \frac{-2S_{12}}{Z_0\Delta} \\ Y_{21} = \frac{-2S_{21}}{Z_0\Delta} \\ Y_{22} = \frac{(1-S_{22})(1+S_{11})+S_{21}S_{12}}{Z_0\Delta} \\ \Delta = (1+S_{11})(1+S_{22}) - S_{21}S_{12}, \end{cases} \tag{27}$$

where Z_0 is the characteristic impedance equal to $Z_0 = 50\ \Omega$.

The result of the conversion measured in milli-Siemens (mS) for transistor PN3563 is

$$\begin{cases} Y_{11} = (6.673 + j8.712) \\ Y_{12} = (0.249 - j2.566) \\ Y_{21} = (33.294 - j83.29) \\ Y_{22} = (1.017 - j2.467). \end{cases} \tag{28}$$

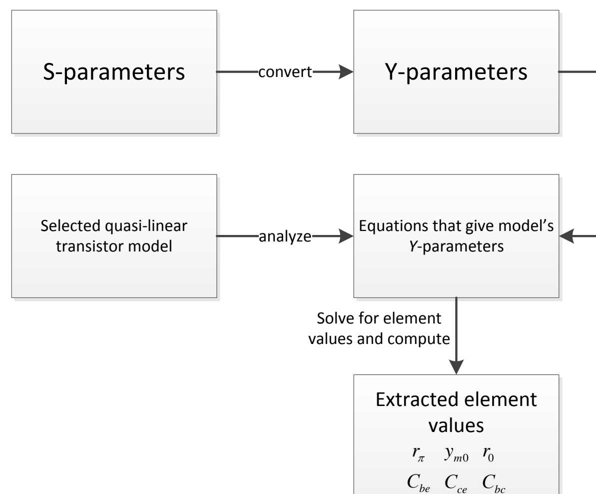


Figure 32: Algorithm of the extraction of the element values from S-parameters.

Secondly, the considered quasi-linear model is a two port network, and the general expression of the admittance matrix for a two-port network is derived from [4, p. 146-148]

$$\begin{cases} I_1 = Y_{11}V_1 + Y_{12}V_2 \\ I_2 = Y_{21}V_1 + Y_{22}V_2. \end{cases} \tag{29}$$

On applying this expression for the quasi-linear transistor model (Figure 33), currents I_1 and I_2 are changed to the base current i_b and collector current i_c respectively, whereas voltages V_1 and V_2 become v_{be} and v_{ce}

$$\begin{cases} i_b = Y_{11}v_{be} + Y_{12}v_{ce} \\ i_c = Y_{21}v_{be} + Y_{22}v_{ce}. \end{cases} \tag{30}$$

Now, shorting either the first or second port we obtain the admittance matrix elements

$$\begin{cases} Y_{11} = \frac{i_b}{v_{be}}\Big|_{v_{ce}=0} = \frac{1}{r_\pi} + j\omega(C_{bc} + C_{be}) \\ Y_{12} = \frac{i_b}{v_{ce}}\Big|_{v_{be}=0} = \frac{-j\omega C_{bc}v_{ce}}{v_{ce}} = -j\omega C_{bc} \\ Y_{21} = \frac{i_c}{v_{be}}\Big|_{v_{ce}=0} = \frac{y_{m0}v_{be} - j\omega C_{bc}v_{be}}{v_{be}} = y_{m0} - j\omega C_{bc} \\ Y_{22} = \frac{i_c}{v_{ce}}\Big|_{v_{be}=0} = \frac{1}{r_0} + j\omega(C_{bc} + C_{ce}). \end{cases} \tag{31}$$

Lastly, we derive the element values from (31)

$$r_\pi = \frac{1}{Re\{Y_{11}\}}, \tag{32}$$

$$r_0 = \frac{1}{Re\{Y_{22}\}}, \tag{33}$$

$$C_{bc} = -\frac{Im\{Y_{12}\}}{\omega}, \tag{34}$$

$$C_{be} = \frac{Im\{Y_{11}\} + Im\{Y_{12}\}}{\omega}, \tag{35}$$

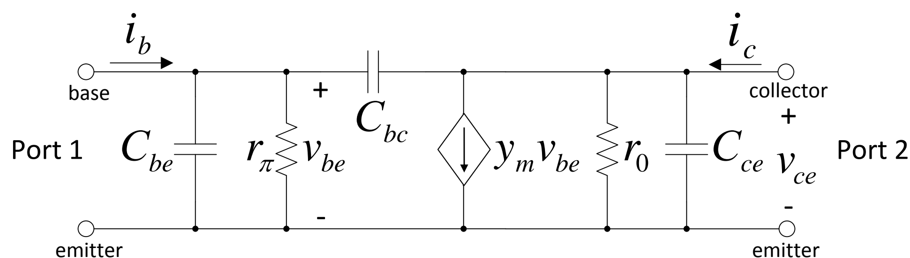


Figure 33: Quasi-linear model used for deriving the Y-parameters.

$$C_{ce} = \frac{Im\{Y_{22}\} + Im\{Y_{12}\}}{\omega}, \tag{36}$$

$$y_{m0} = Y_{21} - Y_{12}. \tag{37}$$

After substituting the numerical values for PN3563 we obtain

$$\begin{cases} r_\pi = 149.9\ \Omega, \\ r_0 = 983.18\ \Omega, \\ C_{bc} = 4.1\ \text{pF}, \\ y_{m0} = 87.3\ \text{mS}\angle -67.59^\circ, \\ C_{be} = 9.78\ \text{pF}, \\ C_{ce} = -0.16\ \text{pF}. \end{cases} \tag{38}$$

The negative value of the capacitance C_{ce} is explained either due to the uncertainty in the measured values or deficiency in the equivalent circuit. However, the value is small and does not appreciably influence the analysis.

4.2 Load power evaluation

In this section we derive the load power in the quasi-linear transistor model. Initially, the base-emitter voltage $\hat{v}_{be}$ and the transadmittance y_m that specify the voltage-controlled current source, as can be seen in Figure 31, are to be found. The base-emitter voltage $\hat{v}_{be}$ is expressed [5], [6]

$$\hat{v}_{be} = \sqrt{2}\left|\frac{Z_{in}}{Z_{in} + Z_0}\right|\sqrt{4P_{av}R_g}, \tag{39}$$

where the input impedance is obtained from the measured S-parameters

$$Z_{in} = Z_0\frac{1 + S_{11}}{1 - S_{11}}. \tag{40}$$

In its turn, the complex transadmittance (14) is derived by obtaining its magnitude and a phase angle. The transadmittance magnitude $|y_m(\hat{v}_{be})|$ is found based on (18), where the maximum collector current $i_{c,max}$ is taken from Table 15 for a certain transistor type, the small-signal transadmittance $|y_{m0}|$ is derived from the measured S-paramters ((37)) and the empirical parameter is assumed $r = 2$. The phase angle is evaluated as following

$$\phi^\circ = \arctan\frac{\text{Im}(y_m)}{\text{Re}(y_m)}\frac{180^\circ}{\pi}, \tag{41}$$

where y_m is taken based on (18).

We then derive the load power P_L that depends on the load voltage v_L based on the

nodal analysis

$$P_L = \frac{|v_L|^2}{Z_0}. \tag{42}$$

The simplified circuit of the quasi-linear transistor model demonstrated in Figure 34 is transparent way of calculating the load voltage v_L and, accordingly, the load power P_L. The following steps cover the details of the load power P_L evaluation:

1. The series connected voltage source E_g and resistance R_g are transformed into the parallel connected current source $\frac{E_g}{R_g}$ and resistance R_g based on the Norton theorem [19, pp. 113-115];

2. The parallel connected generator's resistance R_g, base-emitter capacitance C_{be} and input resistance r_π are converted into an equivalent impedance Z_1

$$\frac{1}{Z_1} = \frac{1}{R_g} + j\omega C_{be} + \frac{1}{r_\pi}. \tag{43}$$

After solving the equation for Z_1 we obtain

$$Z_1 = \frac{\frac{r_\pi \frac{1}{j\omega C_{be}}}{r_\pi + \frac{1}{j\omega C_{be}}} R_g}{\frac{r_\pi \frac{1}{j\omega C_{be}}}{r_\pi + \frac{1}{j\omega C_{be}}} + R_g} = \frac{\frac{r_\pi R_g}{r_\pi j\omega C_{be}+1}}{\frac{r_\pi R_g}{r_\pi j\omega C_{be}+1} + R_g} = \frac{r_\pi R_g}{r_\pi + R_g(r_\pi j\omega C_{be} + 1)}; \tag{44}$$

3. The parallel connected output resistance r_0, collector-emitter capacitance C_{ce} and load resistance R_L are transformed into an equivalent impedance Z_2

$$\frac{1}{Z_2} = \frac{1}{r_0} + j\omega C_{ce} + \frac{1}{R_L}, \tag{45}$$

and after solving the equation for Z_2 we get

$$Z_2 = \frac{\frac{\frac{1}{j\omega C_{ce}} r_0}{\frac{1}{j\omega C_{ce}} + r_0} R_L}{\frac{\frac{1}{j\omega C_{ce}} r_0}{\frac{1}{j\omega C_{ce}} + r_0} + RL} = \frac{r_0 R_L}{r_0 + R_L(r_0 j\omega C_{ce} + 1)}. \tag{46}$$

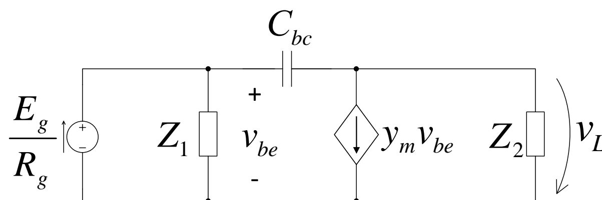


Figure 34: Simplified scheme of the quasi-linear transistor model.

4. Then, based on the Ohm's law (or Kirchhoff's current law)

$$YV = I, \tag{47}$$

where current I is the product of admittance Y and voltage V, the equations in matrix form are constructed for the given circuit

$$\overset{\mathbf{Y}}{\begin{bmatrix} \frac{1}{Z_1} + j\omega C_{bc} & -j\omega C_{bc} \\ -j\omega C_{bc} & \frac{1}{Z_2} + j\omega C_{bc} \end{bmatrix}} \overset{\mathbf{V}}{\begin{bmatrix} v_{be} \\ v_L \end{bmatrix}} = \overset{\mathbf{I}}{\begin{bmatrix} \frac{E_g}{R_g} \\ -y_m v_{be} \end{bmatrix}}. \tag{48}$$

After shifting $-y_m v_{be}$ from the current matrix into the admittance matrix we get

$$\begin{bmatrix} \frac{1}{Z_1} + j\omega C_{bc} & -j\omega C_{bc} \\ -j\omega C_{bc} + y_m & \frac{1}{Z_2} + j\omega C_{bc} \end{bmatrix} \begin{bmatrix} v_{be} \\ v_L \end{bmatrix} = \begin{bmatrix} \frac{E_g}{R_g} \\ 0 \end{bmatrix}, \tag{49}$$

and using the Cramer's rule [20, pp. 279-276], [22, pp. 119-121], the voltage at the load v_L is determined as the ratio of a determinant of matrix Y, which second column is replaced by elements of matrix I, and a determinant of matrix Y as follows

$$v_L = \frac{\begin{vmatrix} \frac{1}{Z_1} + j\omega C_{bc} & \frac{E_g}{R_g} \\ -j\omega C_{bc} + y_m & 0 \end{vmatrix}}{\begin{vmatrix} \frac{1}{Z_1} + j\omega C_{bc} & -j\omega C_{bc} \\ -j\omega C_{bc} + y_m & \frac{1}{Z_2} + j\omega C_{bc} \end{vmatrix}}. \tag{50}$$

The equation is solved

$$v_L = \frac{\left(\frac{1}{Z_1} + j\omega C_{bc}\right) 0 - \frac{E_g}{R_g}\left(y_m - j\omega C_{bc}\right)}{\left(\frac{1}{Z_1} + j\omega C_{bc}\right)\left(\frac{1}{Z_2} + j\omega C_{bc}\right) + \left(-j\omega C_{bc}\right)\left(-j\omega C_{bc} + y_m\right)} =$$

$$= \left(\frac{j\omega C_{bc} - y_m}{\left(\frac{1}{Z_1} + j\omega C_{bc}\right)\left(\frac{1}{Z_2} + j\omega C_{bc}\right) - \left(\omega C_{bc}\right)^2 - j\omega C_{bc} y_m} \right) \frac{E_g}{R_g}. \tag{51}$$

After computing the voltage at the load we determine the load power in watts using (42).

4.3 Experimental results

The quasi-linear transistor model presented in Section 2.2.3 is implemented in MATLAB as an outer function called `qltm` (Appendix 1) that calculates the load power $P_L|_{dBm}$, base-emitter voltage $\hat{v}_{be}$ and transadmittance magnitude $|y_m|$.

The evaluated graphs of power saturation and transadmittance behaviors of the transistor PN3563 are displayed in Figures 35 – 36, respectively. As can be seen in Figure 35, the power of PN3563 starts saturating roughly at $P_{av} = -7$ dBm and reaches the 1 dB compression point at $P_{av,1dB} = -2$ dBm. The dependence of the transadmittance magnitude $|y_m|$ on the base-emitter voltage v_{be} for different empirical parameters ($r = 1$, $r = 2$, $r = 3$, $r = 5$ and $r = 9$) is presented in Figure 36. Here, the roll-off of the function (18) is more rapid at low values of r compared to higher values that well agree with the theory presented in Section 2.2.3, Figure 11.

Next, we analyze the main characteristics, including the power saturation and the transadmittance $|y_m|$ as a function of input voltage $\hat{v}_{be}$, for five different types of transistors (Table 4) that are demonstrated in Figures 37 – 41. According to the given figures the quasi-linear modeling predicts the power saturation for the tested transistors. Moreover, the modeled transadmittance $y_m(\hat{v}_{be})$ behaviors for all the tested transistors are consistent with the theory.

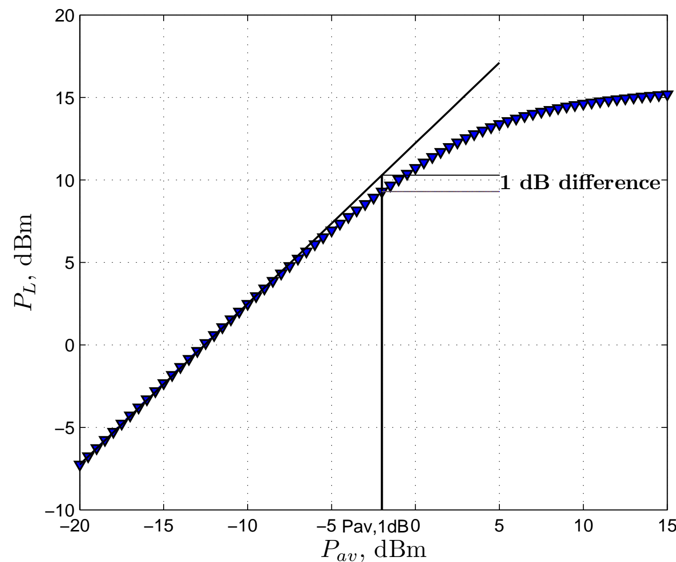


Figure 35: Power saturation for PN3563 using the analytical model.

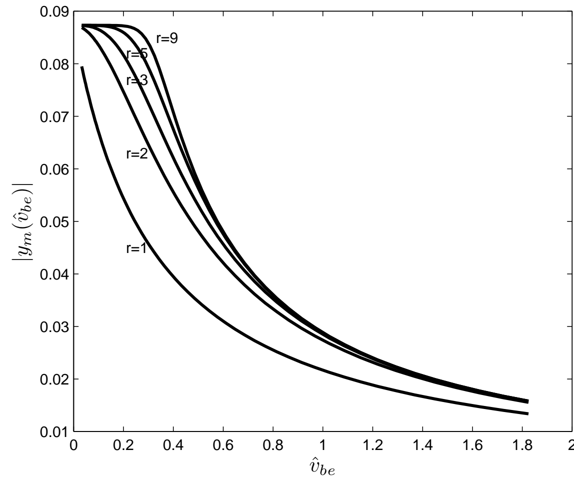
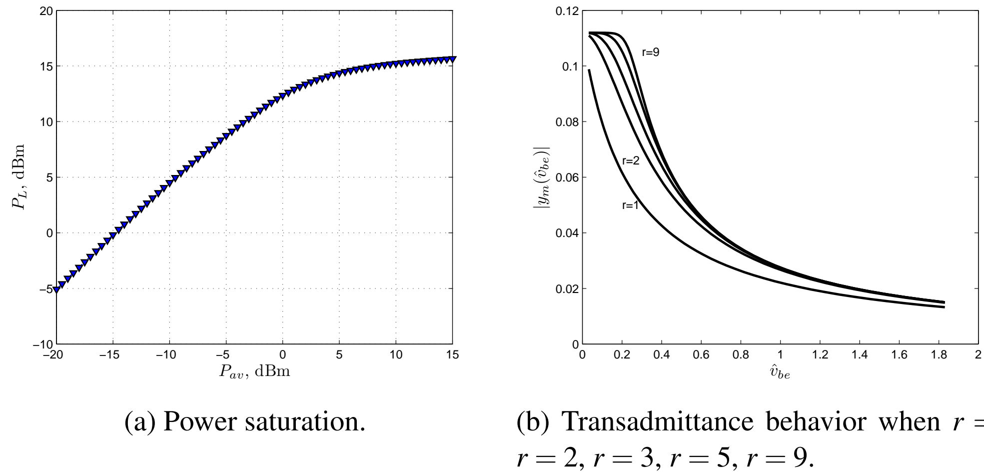


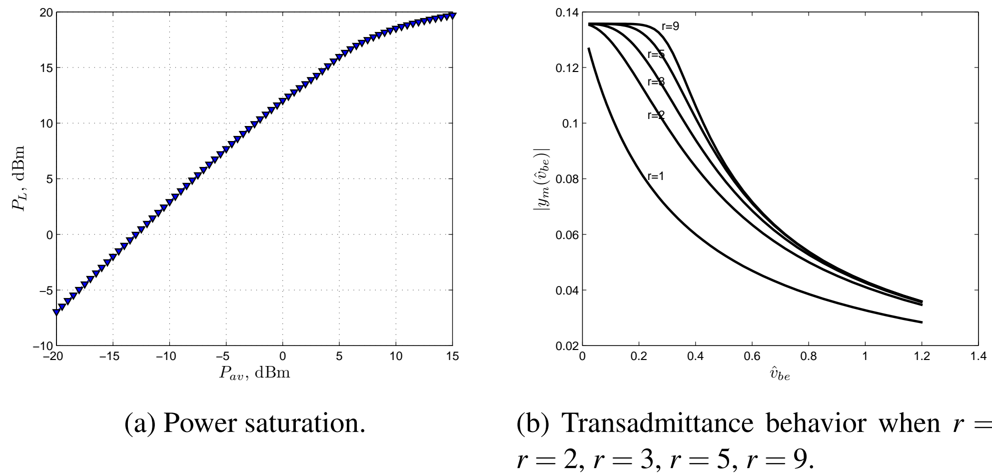
Figure 36: Obtained transadmittance behavior for PN3563 when $r = 1$, $r = 2$, $r = 3$, $r = 5$, $r = 9$.



(a) Power saturation.

(b) Transadmittance behavior when $r = 1$, $r = 2$, $r = 3$, $r = 5$, $r = 9$.

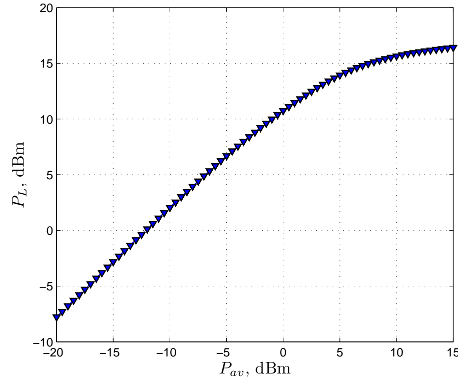
Figure 37: Obtained graphs for 2N5179 using the analytical model.



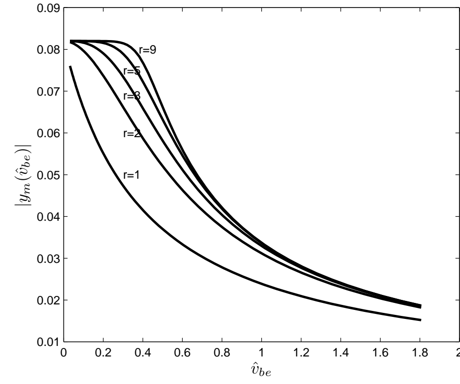
(a) Power saturation.

(b) Transadmittance behavior when $r = 1$, $r = 2$, $r = 3$, $r = 5$, $r = 9$.

Figure 38: Obtained graphs for 2N5109 using the analytical model.

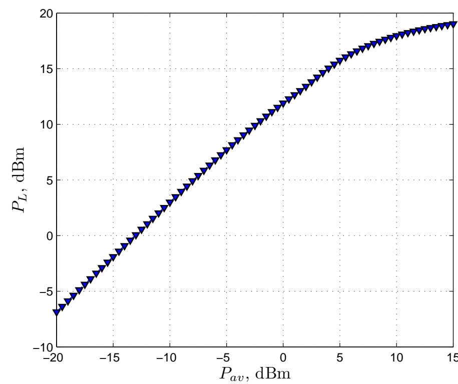


(a) Power saturation.

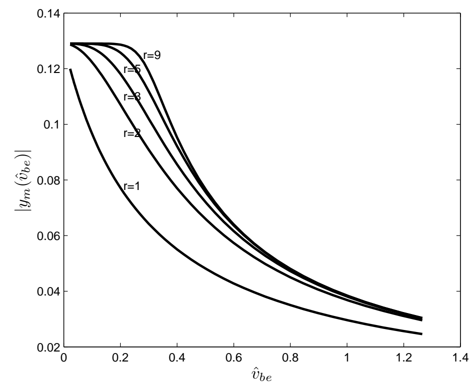


(b) Transadmittance behavior when $r = 1$, $r = 2$, $r = 3$, $r = 5$, $r = 9$.

Figure 39: Obtained graphs for NTE108 using the analytical model.

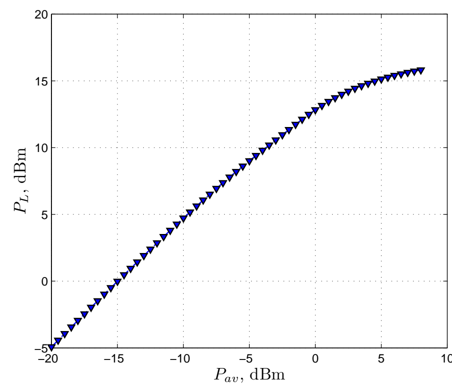


(a) Power saturation.

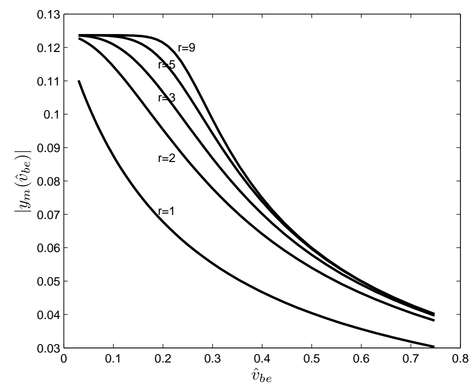


(b) Transadmittance behavior when $r = 1$, $r = 2$, $r = 3$, $r = 5$, $r = 9$.

Figure 40: Obtained graphs for BFW16 using the analytical model.



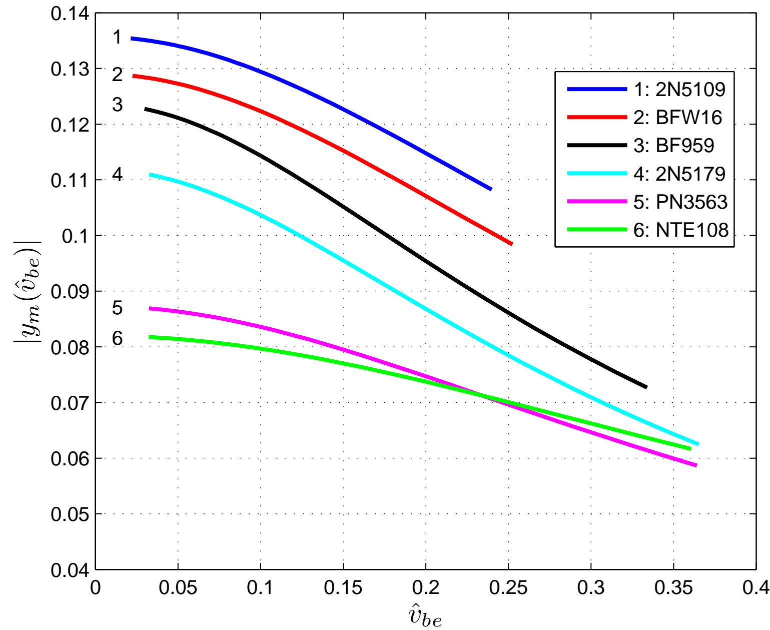
(a) Power saturation.



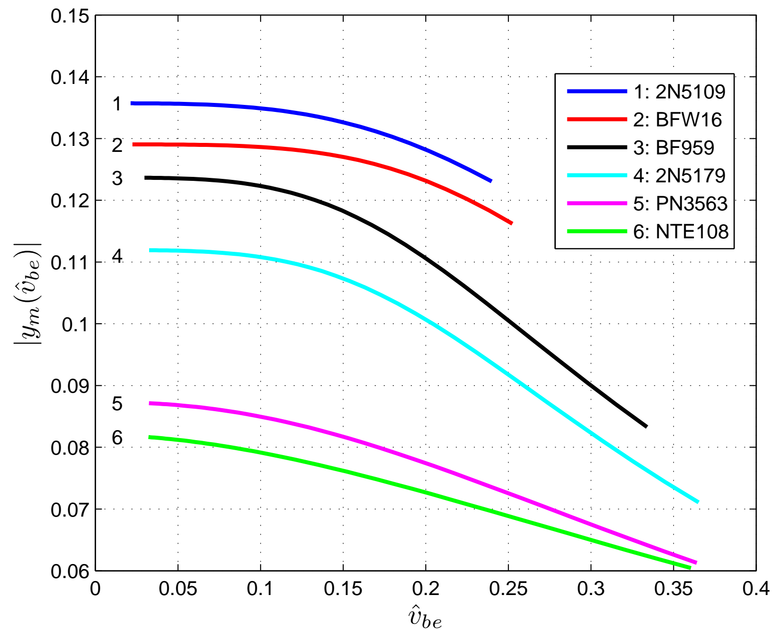
(b) Transadmittance behavior when $r = 1$, $r = 2$, $r = 3$, $r = 5$, $r = 9$.

Figure 41: Obtained graphs for BF959 using the analytical model.

Figure 42 presents two graphs on which the transadmittance behaviors are shown for all the tested transistors. Figure 42a collects the family of transadmittance magnitude curves, for which empirical parameter $r = 2$, whereas Figure 42b displays the transadmittace behaviors for the same types of transistors with r taken from Table 15. Based on the similarity of the curves for the given transistors we conclude that an approximate value of r can be used instead of the measured one.



(a) Family of transadmittance curves using $r = 2$.



(b) Family of transadmittance curves using measured r.

Figure 42: Transadmittance $|y_m(\hat{v}_{be})|$ behaviors for tested transistors.

5 Simulations

This chapter presents the simulation procedure that is done using the software Agilent Advanced Design System (ADS) 2009. The simulation results are presented for all the tested transistors (Table 4) in terms of power saturation curves. Although the ADS 2009 is the powerful design system, which contains a huge library of electric components, some types of transistors are not included in it and, therefore, the analogous transistors are used for simulations. However, the ADS 2009 has a few alternative components with different key parameters for some transistor types. All such components are simulated and the model that best suits the measurement results is used in the following discussion presented in Chapter 6.

Firstly, the simulation electrical circuit based on the common-emitter scheme (Figure 4) is presented and the simulation procedure is discussed. Then, the simulation graphs of power saturation curves are constructed for all the tested transistors.

5.1 Simulated amplifier circuit

The simulated circuit presented in Figure 43 is based on the scheme of common-emitter amplifier (Figure 4). Here, the BJT is a component that varies depending on the simulated transistor type. The resistors $R2$ and $R1$ denote the base R_b and collector R_c resistors, respectively, and on varying their values the bias point is set as $V_{CE}^{Q} = 5$ V, $I_{C}^{Q} = 20$ mA. While the inductors in base and collector operate as the RF chokes, the input and output capacitors are used as DC blocks to prevent the flow of the DC current. As can be seen in Figure 43, there are two variables, namely an input power $Pin = -20$ dBm and

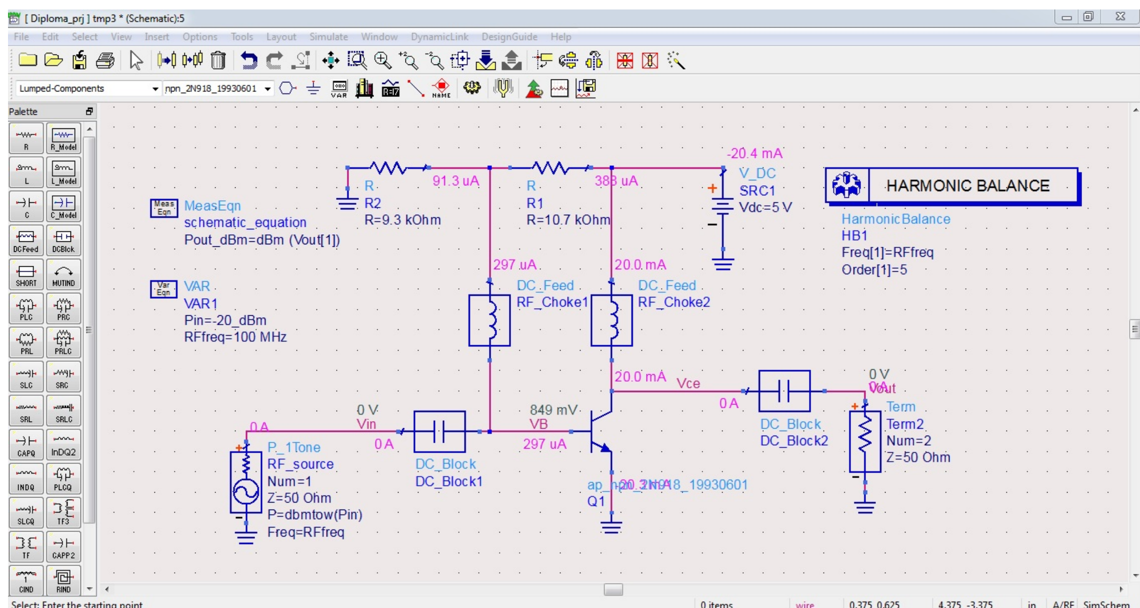


Figure 43: Simulated circuit of power amplifier in ADS 2009.

an operating frequency $RFfreq = 100$ MHz, that are used in setting up the power source and in harmonic balance. The input of the amplifier is presented by the power source "RF_source", which consists of the impedance $Z_g = 50\ \Omega$ and the harmonic source. On activating by double click the "RF_source" , the parameter window "Power Source" is opened and the following parameters are to be set:

- $Z = 50\ \Omega$ – the generator's impedance;
- $P = dbmtow(Pin)$ – the power in dBm, which is based on the input power Pin;
- $Freq = RFfreq$ – the operating frequency;
- $Pac = polar(dbmtow(0), 0)$ – the AC power in polar form.

The load is presented as a termination component "Term", which impedance is $Z_L = 50\ \Omega$. For further convenient presentation of power saturation curves, the output node of the amplifier is denoted as "Vout". Next, we specify the output power as $Pout_dBm = dBm(Vout[1])$ using the equation "MeasEqn", which converts the output voltage to the output power in dBm.

To simulate the power saturation in an amplifier, the ADS 2009 has the function of harmonic balance. After its activating the window "Harmonic Balance" is opened, in which all the necessary settings are specified:

1. In the tab "Freq" enter the operating frequency $RFfreq$ and "Order" equal to 5.
2. In the tab "Sweep" specify the variable Pin that allows changing the input power automatically. Set up the start and stop values for the sweep parameter as -20 dBm and 8 dBm respectively, while the step size is 1 dBm.

After these manipulations the simulation is done by pressing the button "Simulation". Next, the bias point, which should be $V_{CE}^{Q} = 5$ V, $I_C^Q = 20$ mA can be checked by pressing "Annotate DC Solution" in the menu "Simulate". If the current in the collector is not equal to 20 mA, then the variables of resistors $R1$ and $R2$ should be tuned till the target bias point is achieved.

5.2 Simulated power saturation curves

After all the necessary settings are set up and simulations are done, the power saturation curves are plotted. Firstly, we perform the simulation for the transistors PN3563 and NTE108, which are not included in the ADS 2009, therefore, the analogous transistor 2N918 (library name "ap_npn_2N918_19930601") with similar key parameters is used. The simulated power saturation curve for the given transistors is demonstrated in Figure 44. The resistor values of R_1 and R_2 that lead to the bias point $V_{CE}^{Q} = 5$ V, $I_C^Q = 20$ mA are defined in Table 16 for the simulated transistor types. Here, the parameter N denotes the number of alternative components for a certain transistor type.

Table 16: Resistor values for simulated transistors.

Type	N	Transistor's name	R_1, Ω	R_2, Ω
PN3563, NTE108	1	ap_npn_2N918_19930601	10.7	9.3
2N5179	3	ap_npn_2N5179	5.65	14.35
		ap_npn_Q2N5179	5.65	14.35
		pb_mot_2N5179	10.6	9.4
2N5109	2	ap_npn_2N5109	9.25	10.75
		ap_npn_Q2N5109	12.15	7.85
BF959	1	sp_sms_BF959_2_19920901	10.4	9.6
BFW16	1	ap_npn_2N5943_19930601	10.5	9.5

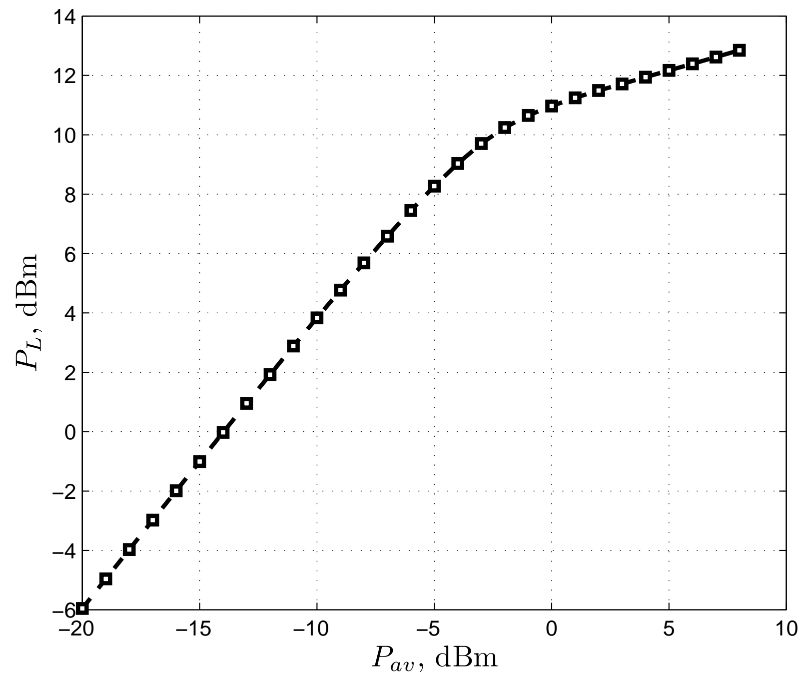


Figure 44: Simulated power saturation for PN3563 and NTE108.

We then analyze the power saturation curves obtained for the rest of the transistor types in Figures 45 – 48. According to the power saturation behavior for the transistor 2N5179 presented in Figure 45, the component ap_npn_Q2N5179 better suits the measured scenario compared to the other simulated ones. Similarly, the component ap_npn_2N5109 in Figure 46 produces more realistic results in terms of power saturation compared to the ap_npn_Q2N5109.

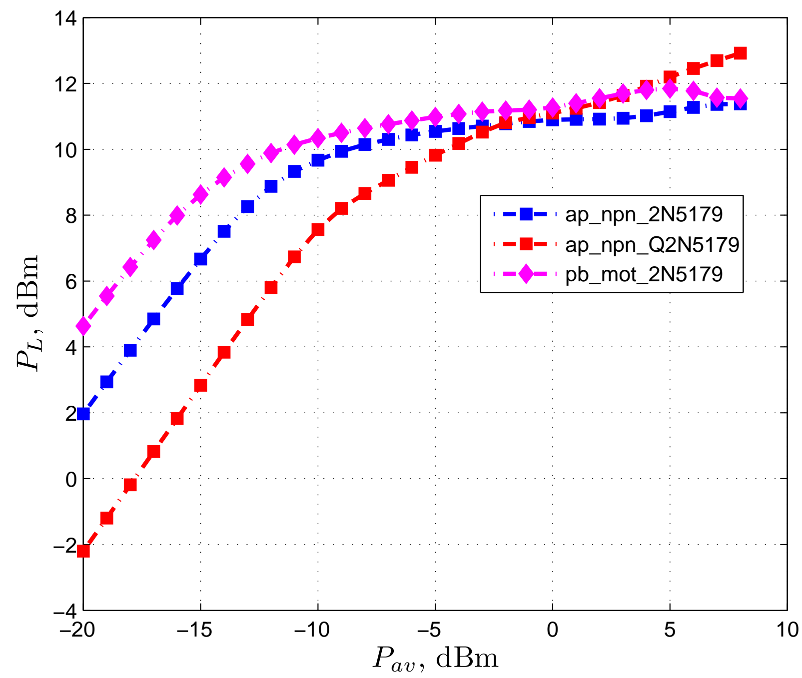


Figure 45: Simulated power saturation for 2N5179.

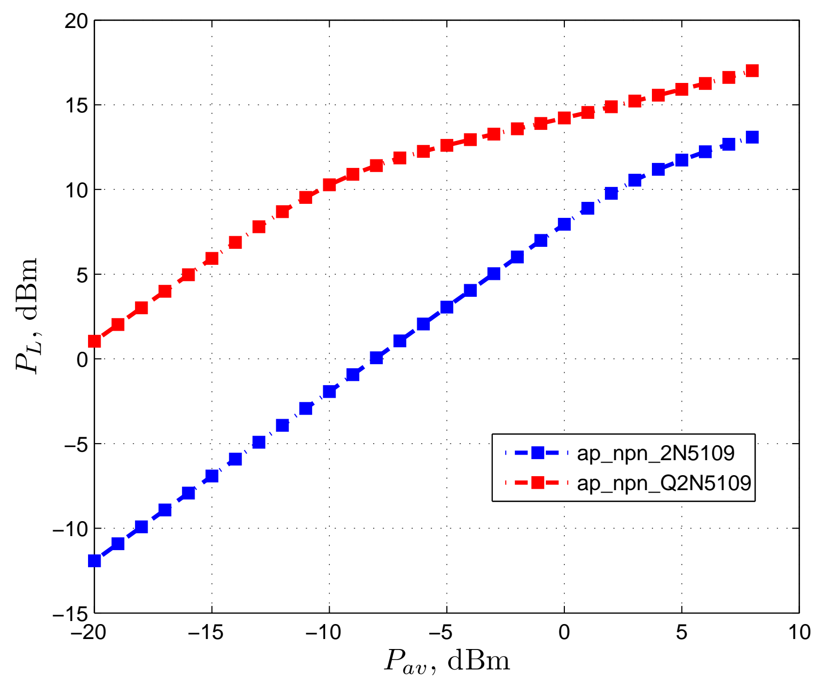


Figure 46: Simulated power saturation for 2N5109.

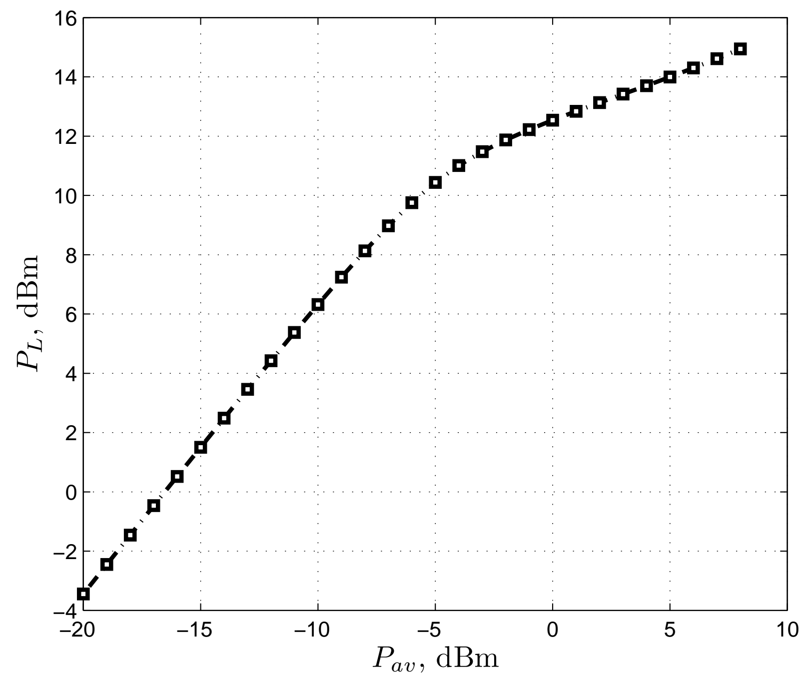


Figure 47: Simulated power saturation for BFW16.

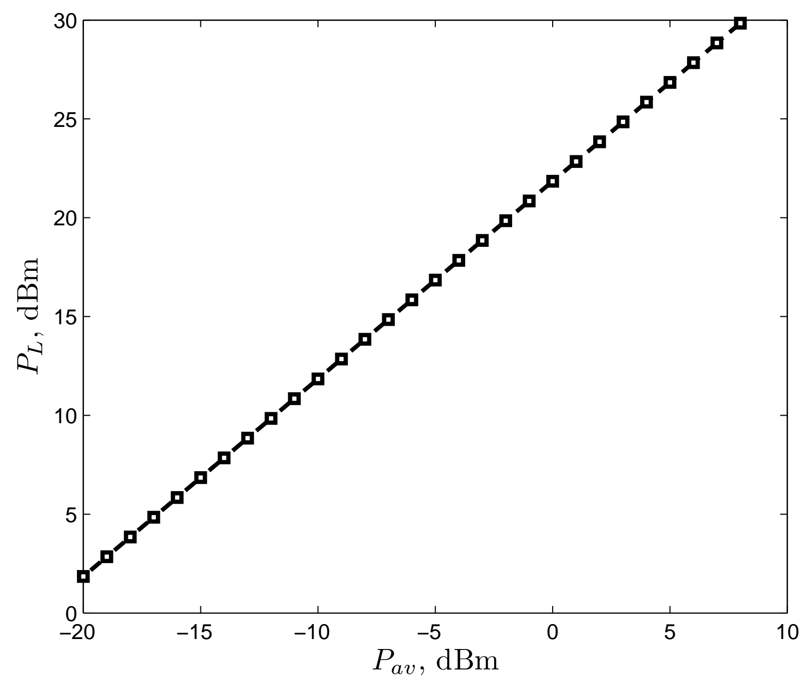


Figure 48: Simulated power saturation for BF959.

6 Discussion

This chapter presents the detailed discussion on the relevancy of the found results. Firstly, the measured transadmittance curves are compared with the ones obtained in quasi-linear modeling. Secondly, the steepness of power saturation curve is examined in accordance with the empirical parameter r. Lastly, the measured, simulated and analytical power saturation curves are compared to each other for different transistor types.

6.1 Transadmittance analysis

Figure 49 displays three transadmittance curves obtained based on the measurements (colored markers), the least-square fitting (black solid lines) and quasi-linear modeling (dashed lines) for different transistors. As can be seen in Figure 49, the quasi-linear modeled transadmittances and least-squared fitted curves are almost identical to each other for the transistors BF959, PN3563 and NTE108, and relatively similar for the transistors 2N5179, 2N5179 and BFW16. It is worth mentioning that their tolerance is less than 4%, which states that the quasi-linear transistor model is accurate in prediction of the transadmittance behavior.

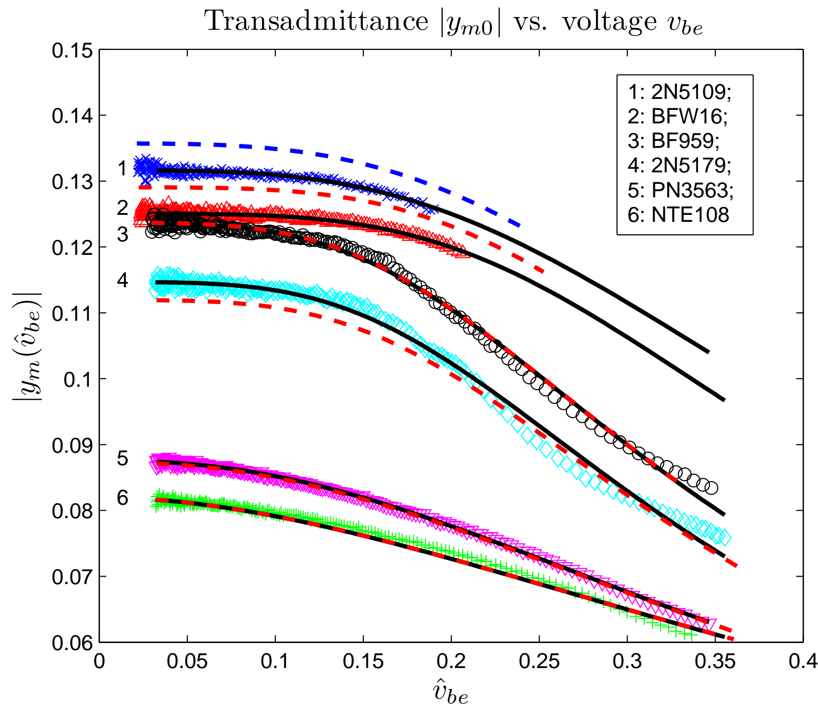


Figure 49: Transadmittance magnitude $|y_m(\hat{v}_{be})|$: measured (colored markers), fitted (black solid lines) and modeled (dashed lines) curves.

6.2 Steepness of power saturation

According to the theory (Subsection 2.2.3) the roll-off of the transadmittance (18) is controlled by the empirical parameter r. Taking into account that the transadmittance affects the power at the load, we further analyze the steepness of power saturation curve regarding the empirical parameter r.

As can be seen in Figure 50, the red solid line presents the measured power saturation results, whereas the blue lines show a family of power saturation curves for transistor 2N5179 obtained using the quasi-linear modeling. Here, the steepness of the modeled curve, or the dynamic range d_R, rises with the increase of r. Hence, we conclude that on varying the empirical parameter r we can achieve the behavior that is the closest to the measured one.

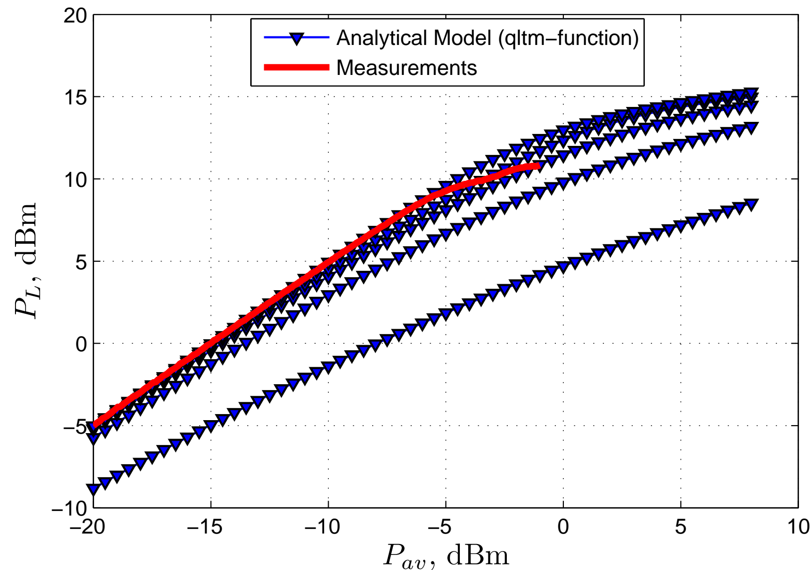


Figure 50: Measured (red line) and modeled (blue lines) power saturation curves.

6.3 Power saturation analysis

Figure 51 displays three power saturation curves for the BJT PN3563 that were found during simulations, measurements and modeling. As can be seen in this figure, the measured and the modeled curves coincide at the linear region, whereas the simulated curve shows 2 dBm difference with the realistic scenario. Moreover, both the quasi-linear model and the simulation curves start saturating approximately at the same point that is close to the measured one. However, the simulation do not always achieve accurate results in power saturation prediction, e.g. for the BJT BF959 shown in Figure 52. In its turn, in this figure the quasi-linear model demonstrates an excellent similarity of the power saturation both in linear and nonlinear regions with the measured curve.

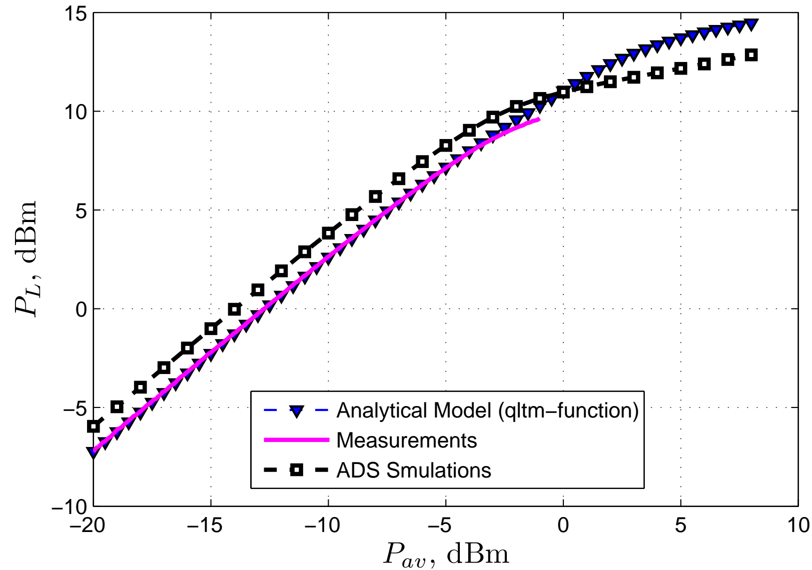


Figure 51: Simulated, measured and modeled power saturation curves for PN3563.

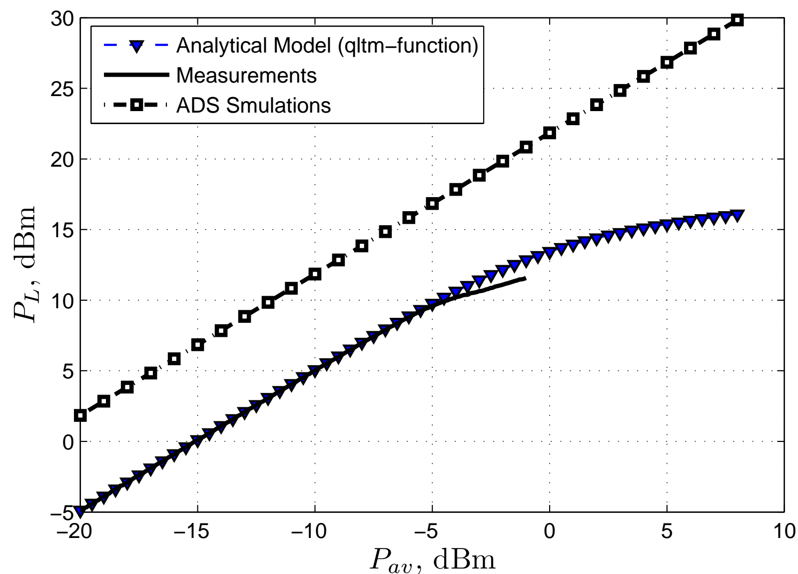


Figure 52: Simulated, measured and modeled power saturation curves for BF959.

Figures 53 – 56 display the power saturation curves for the rest of the transistor types. According to these figures the average difference between the modeled and the measured behaviors in the linear region is around 0.01 dBm, whereas the simulated curves lag behind in the range of 2 dBm – 7 dBm. Despite the steepness of the modeled power saturation concedes to the measured and simulated ones for certain transistor types, the quasi-linear model predicts the power saturation point accurately. Note that the simulations using the CAD systems with constrained possibilities do not always predict the power saturation (Figure 52).

As a summary, the quasi-linear model implies a simple and an efficient way to predict the power saturation in BJT, which has shown more accurate results compared to the ones produced by the powerful design systems, such as ADS 2009.

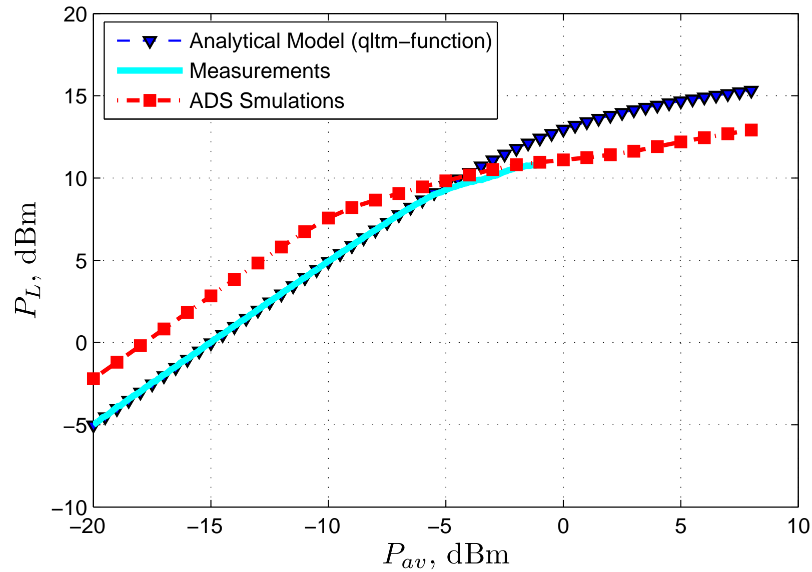


Figure 53: Simulated, measured and modeled power saturation curves for 2N5179.

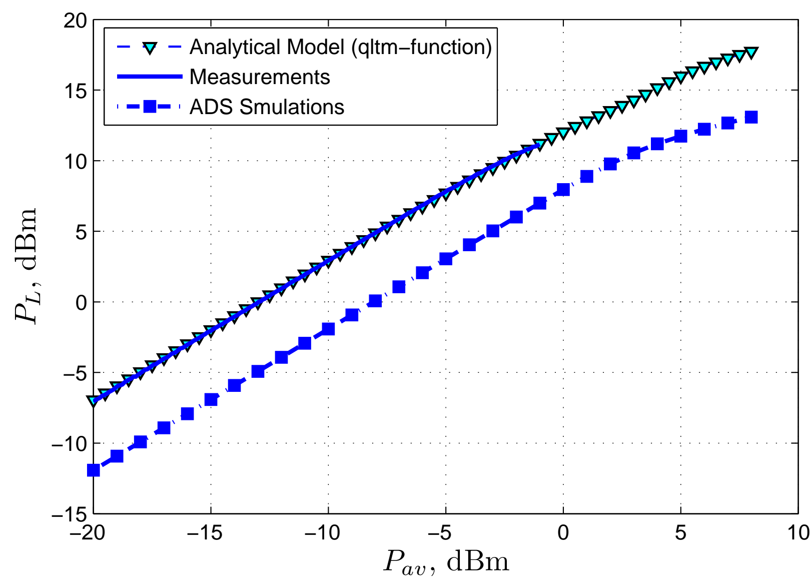


Figure 54: Simulated, measured and modeled power saturation curves for 2N5109.

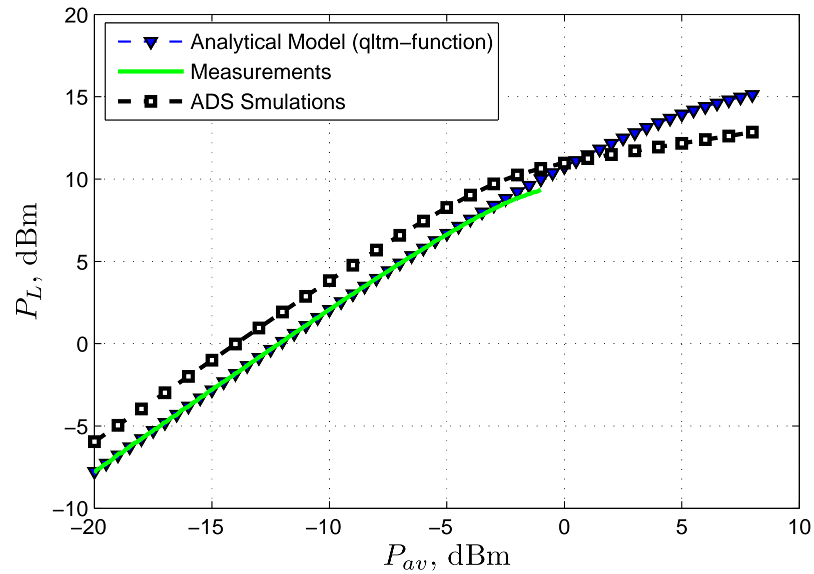


Figure 55: Simulated, measured and modeled power saturation curves for NTE108.

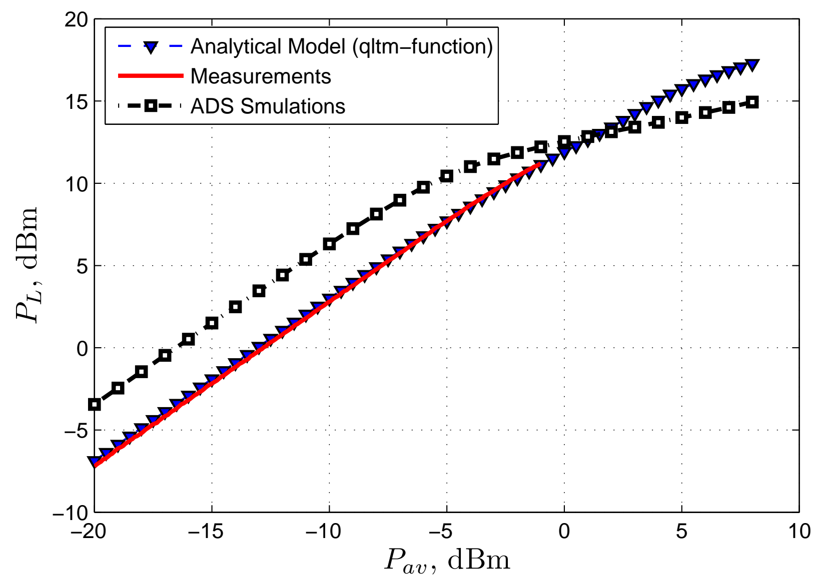


Figure 56: Simulated, measured and modeled power saturation curves for BFW16.

Conclusion

The state-of-the-art quasi-linear transistor model [5] has been initially applied for oscillation analysis. The novelty of this thesis is to investigate the model in appliance with the power saturation prediction in BJT. The quasi-linearity of the model is explained by the fact that all elements of the model are linear, while the voltage-controlled current source is nonlinear. This nonlinear element of the model is specified by the complex transadmittance y_m and the base-emitter voltage $\hat{v}_{be}$. The transadmittance y_m, which is used instead of the transconductance g_m, takes into account the phase difference between collector current i_c and base-emitter voltage v_{be}, and its magnitude $|y_m(\hat{v}_{be})|$ is a decreasing function of input voltage. Hence, the quasi-linear model can be used in specifying the BJT behavior at high frequency range.

According to the conducted measurements, we proved that more compact component placement on the breadboard at high frequencies, e.g. $f = 100$ MHz, allows reaching higher gain ($|S_{21}|$) and decreasing the electromagnetic dissipation. The relevancy of the measurement results is verified by comparing the S-parameters with power and frequency sweeps at one point ($P = -20$ dBm, $f = 100$ MHz).

The quasi-linear model allows finding the transadmittance $|y_m(\hat{v}_{be})|$, which is one of the key middle-stage parameters used for evaluating the power saturation and verifying the accuracy of the model. The maximum variation between the measured transadmittances and modeled ones was less than 4% (Chapter 6), which states that the quasi-linear model accurately evaluates the transadmittance. Moreover, the empirical parameter r influences both the roll-off of the transadmittance and the steepness of the power saturation, and can be adjusted to achieve the target power saturation behavior.

According to the comparative analysis (Chapter 6), the quasi-linear modeling of power saturation in BJT presents high accuracy in the linear region in the range of 0.01 – 0.35 dBm, whereas the simulated curves lag behind in the range of 2 dBm – 7 dBm. Despite the steepness of the modeled power saturation concedes to the measured and simulated ones for certain transistor types, the quasi-linear model predicts the power saturation point accurately. Note that the simulations using the CAD systems with constrained possibilities do not always predict the power saturation.

Thus, the proposed quasi-linear transistor model calculates the output power of the BJT amplifier accurately and predicts precisely the power saturation in bipolar-junction transistors. Despite the simplicity of the quasi-linear model, it takes into account the essential phenomena appeared in BJT, has a number of advantages compared to the hybrid-π model and can be used in RF range instead of powerful design systems, such as ADS 2009. The future research heading may include the model improvement, e.g. taking into account the inductances that appear in BJT at high frequencies.

Appendix 1: Programing code for MATLAB outer function for the quasi-linear power analysis

```
function [P_load, VBE, YM_ABS] = qltm( S11, S12, S21, S22, ic_max, r, Pav)
% KONSTANTIN RYKOV, 29.08.2013
%qltm - is a function, which analyses a Quasi-Linear Transistor Model from
%known S-parameters.
%The input parameters
% 1. S-parameters (S11, S12, S21, S22) in complex form;
% 2. ic_max - maximum collector current, obtained from measurements;
% 3. r - empirical parameter;
% 4. Pav - available power, vector form
%Firstly, S-parameters are transformed to Y-parameters
%and then transistor model resistanses,capacitances and input impedance Zin
%are computed. Secondly, the power transferd to the load is computed.
%Lastly, the 'qltm'-functiion plots the graph P_load vs. P_avg.
%% =================================================================%%
%                        S-PARAMETERS -> Y-PARAMETERS
%%==================================================================%%
S = [S11 S12; S21 S22]; % S-matrix is formed;
w=2*pi*100e6;           % MHz, operating frequency 100 MHz;
Z0=50;                  % Ohms, characteristic impedance 50 Ohms;
Rg=50;                  % Ohms, generator impedance 50 Ohms;
Rl=50;                  % Ohms, load termination 50 Ohms;
Y=s2y(S,Z0);            % forming Y-matrix by converting S-matrix.
%% ================================================================ %%
%                      FINDING TRANSISTOR MODEL PARAMETERS
%%==================================================================%%
rpi=1/real(Y(1,1));                    % Ohms, input resistance;
r0=1/real(Y(2,2));                     % Ohms, output resistance;
Cbc=real(-(Y(1,2))/(j*w));             % F, base-collector capacitance;
ym0=Y(2,1)+j*w*Cbc;                    % S, transadmittance;
Cbe=real((Y(1,1)-j*w*Cbc-1/rpi)/(j*w));% F, base-emitter capacitance;
Cce=real((Y(2,2)-1/r0-j*w*Cbc)/(j*w)); % F, collector-emitter capacitance;
Zin=Z0*(1+(S11))/(1-(S11));            % Ohms, input impedance.
%% ================================================================ %%
%                                 FINDING P_load
%%==================================================================%%
ind=1;                              % "for"-loop index used in forming a
                                    % P_load vector
for i=Pav                           % indexing Pav for 'for'-loop
i=10^((i-30)/10);                   % W, converting Pav in dBm to watts;
vbe=sqrt(2)*abs(Zin/(Zin+Z0))...    % V, base-emitter voltage;
    *sqrt(4*i*Z0);
VBE(ind)=vbe;                       % forming a vector, which consists of
                                    % all base-emitter voltages along the
                                    % whole power range;
ym_abs=abs(ym0)/(1+(vbe*abs(ym0)... % S, the transadmittance magnitude;
    /ic_max).^r)^(1/r);
ym_complex=(ym0)/((1+(vbe*(ym0)...  % S, transadmittance in complex form;
    /ic_max)^r)^(1/r));
ym_angl=angle(ym_complex)*180/pi;   % DEG, the transadmittance phase anlge;
```

```
50 ym=ang2comp(ym_abs, ym_angl);          % checking the correctness of calcula-
51                                        % tion comparing values of
52                                        % ym_complex and ym;
53 YM_ABS(ind)=ym_abs;                    % S, forming a vector of trans-
54                                        % admittance magnitudes
55 Eg=sqrt(4*i*Rg);                       % V, generator voltage
56 Z1=(1/(1/rpi+j*w*Cbe+1/Rg));           % Ohms, eq. impedance of Rg||Cbe||rpi
57 Z2=(1/(1/r0+j*w*Cce+1/Rl));            % Ohms, eq. impedance r0||Cce||Rl
58
59 % V, voltage at the load
60 vl=det([1/Z1+j*w*Cbc Eg/Z0; -j*w*Cbc+ym 0])...
61     /det([1/Z1+j*w*Cbc -j*w*Cbc; -j*w*Cbc+ym 1/Z2+j*w*Cbc]);
62 Pl=(abs(vl))^2/Z0;                     % W, P_load - power transfered to load
63 Pl2=10*log10(Pl/1e-3);                 % dBm, P_load
64 P_load(ind)=Pl2;                       % writing Pl results in a vector
65 ind=ind+1;                             % taking next vactor element
66 end
67 end
```

References

[1] Petrov, K. S., Radiomaterials, Radiocomponents and electronics. 2003, Piter, 512 p. (in Russian).

[2] Storey, N., Electronics: A System Approach. 3rd ed., 2006, Harlow, Pearson/Prentice-Hall, 704 p.

[3] Savant, C. J. Jr., Electronic Design: Circuits and Systems. 2nd ed., 1991, The Benjamin/Cummings, Inc., 831 p.

[4] Ludwig, R., Bogdanov, G., RF Circuit Design: Theory and Applications. 2nd ed., 2009, New Jersey, Pearson/Prentice-Hall, 704 p.

[5] Lundén, O.-P., Konttinen, K., Hasani, M., A Simple Closed-Form Analysis of Clapp Oscillator Output Power Using a Novel Quasi-Linear Transistor Model. To be published in Radio and Wireless Symposium, January 19-22, 2014.

[6] Konttinen, K., Nonlinear Modeling of BJT Transconductance. Bachelor's Thesis. Tampere 2012, Tampere University of Technology, Department of Electronics, 26 p. (in Finnish).

[7] Jaeger, R. C., Blalock, T. N., Microelectronic Circuit Design. 4th ed., 2011, McGraw-Hill. 1334 p.

[8] Fonstad, C. G., Microelectronic Devices and Circuits. Electronic ed., 2006, Creative Commons License 2.5. 686 p.

[9] Pozar, D. M., Microwave Engineering. 4th ed., 2011, John Wiley & Sons, Ltd, 732 p.

[10] Kazimierczuk, M. K., RF Power Amplifiers. 2008, John Wiley & Sons, Ltd, 405 p.

[11] Ebers, J. J., Moll, J. L., Large-Scale Behaviour of Junction Transistors. December 1954, Proc. of IRE, vol. 42, pp. 1761-1778.

[12] Gummel, H. K., Poon, H. C., An integral charge control model of bipolar transistors. May-June 1970, Bell System Technical Journal, vol. 49, no. 12, pp. 827-852.

[13] Warner, R. M. Jr., Grung, B. L., Semiconductor-Device Electronics. 1991, Philadelphia, Holt, Rinehart and Winston, 904 p.

[14] Yuan, J. S., SiGe, GaAs, and InP Heterojunction Bipolar Transistors. 1999, New York, John Wiley & Sons, Inc, 463 p.

[15] Hiebel, M., Fundamentals of Vector Network Analysis. 2007, M unchen, Rohde & Schwarz, 420 p.

[16] Hewlett Packard, HP 8719D/8720D/8722D Network Analyzer: Installation and Quick Start Guide. 1996, HP Part No. 08720-90291.

[17] Hewlett Packard, HP 8719D/8720D/8722D Network Analyzer: Quick Reference Guide. 1997, HP Part No. 08720-90289.

[18] National Instruments, Fundamentals of Network Analysis, 2012: http://www.ni.com/white-paper/11640/en/

[19] Nilsson, J. W., Susan, A. R., Electric Circuits. 9th ed., 2011, Pearson/Prentice Hall, 794 p.

[20] Pool, D., Linear Algebra: A Modern Introduction. 2nd ed., 2006, Thomson, 712 p.

[21] The R Project for Statistical Computing: http://www.r-project.org/

[22] Gusak, A. A., Gusak, G. M., Brichikova, E. A., Guide to Higher Mathematics. 6th ed., 2005, Minsk, TetraSystems, 640 p. (in Russian).