TAMPERE UNIVERSITY OF TECHNOLOGY

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STABILITY ANALYSIS OF A MICROWAVE POWER AMPLIFIER USING POLE ZERO IDENTIFICATION METHOD

Master of Science Thesis

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ABSTRACT

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This thesis demonstrates the use of pole zero identification method to stabilize a 2.32 - 2.37 GHz class AB power amplifier. In addition, the thesis presents a procedure to obtain values of stabilization components. Power amplifiers are used to drive transmitting antennas with high power in applications such as RADAR's, cellular base stations and RF-driven lighting. They operate at large signal level to achieve these high output power levels. This increases the risk of potential oscillations in power amplifiers, which are undetectable using conventional linear stability factors. The oscillations degrade amplifier's performance and may cause interference and transistor burnout.

Non-applicability of linear stability factors for large-signal operation has led to development of new stability analysis methods such as Ohtomo, NDF and AG. Ability to detect oscillation due to large-signal has been the priority of these methods. A drawback is that, they are either complex to use or not fully complete in stabilizing a power amplifier. A recent method based on pole zero identification is shown to be rigorous and simple to use. However, this method requires a special additional software STability ANalysis(STAN) to identify poles and zeros of power amplifiers.

This work utilized a simulation template in ADS 2011 to design the 2.32-2.37 GHz class AB power amplifier. The template requires measured load pull data of the transistor used in the amplifier design. The realized design has met maximum performance in first trial with little optimization. This design approach is useful to circumvent modeling problems in power transistors. However, the stability analysis is highly dependent on the transistor model accuracy.

The designed and constructed class AB power amplifier in this work is unconditionally stable for small-signal operation and potentially unstable for large-signal operation. The amplifier is able to deliver an output power of 140 Watts with 15.2 dB gain and 42.08% efficiency at 2.345 GHz. Load pull measurements (peak power, peak gain and peak efficiency) of the amplifier and transistor used to design the amplifier are compared for design evaluation.

PREFACE

This thesis work has been carried at NXP Semiconductors, Nijmegen, The Netherlands for product development group in the department of Product Line RF Power and Base stations. This thesis has been supervised by Jos van der Zanden (Principal RF Engineer at NXP) and Edmund Neo (Product development team leader, NXP). I would like to take this opportunity to thank Edmund Neo and Jos van der Zanden for providing me an opportunity to work on my thesis.

I would also like to thank Stephane Dellier(RF & Microwave Project leader, AMCAD Engineering, Toulouse, France) and Remi Tuijtelaars (BSW test systems) for providing me with temporary license of STAN software. I would especially like to thank S. Dellier for his kind support and comments on questions I raised during usage of the STAN software. It is a pleasure to thank Professor Juan Mauri Collantes, University of Basque country, Bilbao, Spain for his valuable comments on large-signal stability analysis using STAN.

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I would like to express my respect to my teachers and examiners Dr. Tech. Ollipekka Lundén and Dr. Tech Jari Kangas for their support, teaching and guiding throughout my Masters program. Finally I would like to thank the Department of Electrical Engineering, Tampere University of Technology for giving me admission into Masters Program in Radio Frequency Electronics.

I would like to show my gratitude to my parents for their strong support, love and motivation throughout my life.

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ABBREVIATIONS

AC	Alternating Current
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
AMCAD	Advanced Modeling for Computer Aided Design
ASCII	American Standard Code for Information Interchange
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CNES	Centre National d'Etudes Spatiales
CL	Closed Loop
DBLP	Data Based Load Pull
DC	Direct Current
DPD	Digital Pre-Distorter
FET	Field Effect Transistor
GUI	Graphical User Interface
HB	Harmonic Balance
HBT	Hetero junction Bipolar Transistor
IMD3	Third order Inter Modulation
IV	Current Voltage
KCL	Kirchhoff's Current Law
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LHP	Left Half Plane
LTE	Long Term Evolution
LTV	Linear Time Variant
MOS	Metal Oxide Semiconductor
MSG	Maximum Stable Gain
MPT	Maximum Power transfer Theorem
NXP	Next eXPerience
PCB	Printed Circuit Board
PSD	Power Spectral Density
RF	Radio Frequency
RHP	Right Half Plane
RL	Return Loss
RR	Return Ratio
STAN	STability ANalysis
UHF	Ultra High Frequency
WCDMA	Wide-band Code Division Multiple Access

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1. INTRODUCTION

An RF power amplifier is a microwave circuit used to amplify a low power RF signal to a high power RF signal. It is extensively used in surveillance and communication applications such as RADAR's (radio detection and ranging) and cellular base stations to drive transmitting antennas with large RF signals. The main difference between power amplifiers and other amplifiers is that they are forced to operate in nonlinear region of the transistor by feeding with large RF signals at input.

An amplifier (single stage) consists of an active device (transistor) and passive components. The active device is capable of amplifying the input RF signal for a given DC bias. Passive components are used to bias, stabilize and match to impedance of the active device.

The graphical representation of the transistor's measured DC output current versus voltage for increasing input DC voltage (in case of MOS transistor) is called transistor's output characteristic (For example as shown in Fig. 1.1). The output characteristic represents the operating region of the transistor and is divided into three parts, namely, active region, saturation region and cut off region [11]. Depending upon the type of application, input signal and performance requirements of the amplifier, the transistor will be biased for particular operating point (input DC voltage, output DC current and voltage) in the output characteristic.

The region of transistor operation for which the amplifier output is linearly related to its input is called linear region. To operate in this region, the input RF signal should be small enough such that its swing over a specific bias point is within adjacent bias points as shown in Fig. 1.1a. The input signal is then referred as a small-signal [1]. The transistor can be modeled by a hybrid π network in this region.

The region of transistor operation for which the amplifier's output is nonlinearly related to its input is called nonlinear region. In this case, the input RF signal is large and its swing over specific bias point cover other bias points as shown in Fig. 1.1b. The input signal is then referred as a large-signal [1]. The transistor cannot be modeled by the hybrid π network in this region.

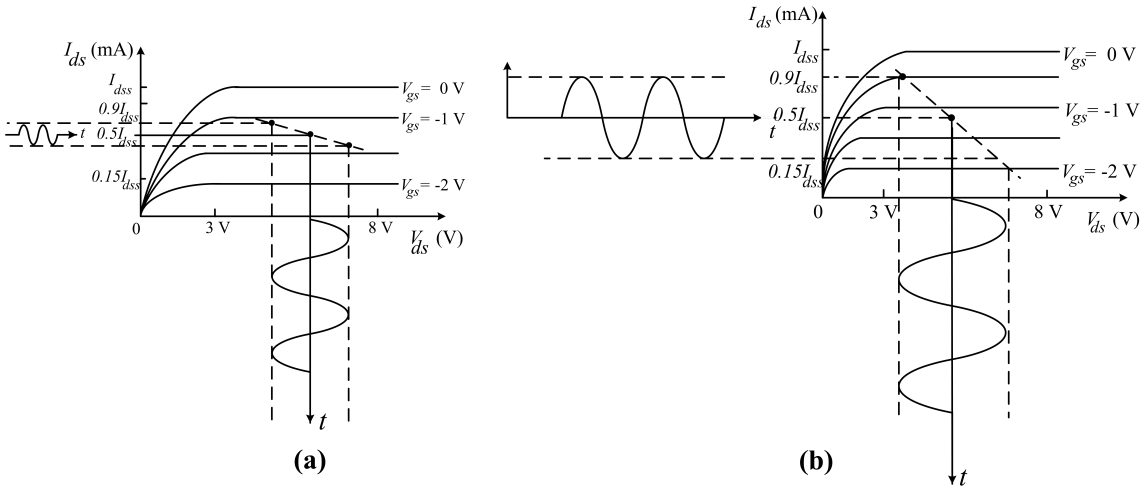

Figure 1.1: IV characteristics and load lines for (a) small-signal operation and (b) large-signal operation [1].

A transistor has two ports, input port and an output port. With appropriate termination of transistor at one port, for some region of increasing input voltage, if its output current decreases, then the transistor can exhibit negative differential resistance at the other port in this region [11]. The change in applied voltage with respect to change in output current in this region is defined as negative differential resistance [12]. It is sensitive to applied input voltage and can occur when the transistor is fed with direct current (DC) or small or large voltage signals.

A factor by which an incident signal reflects back is called reflection coefficient [13]. When a transistor exhibits negative resistance at one port, its corresponding reflection coefficient becomes greater than one [11]. The reflected signal from this port is in greater magnitude than incident signal. If this port is terminated such that its reactance resonates with termination reactance and its resistance magnitude is greater than termination resistance, then it is possible that a signal is sustained between the transistor port and the termination [11]. This process of sustaining a signal is called oscillation. The frequency at which the circuit oscillates is called oscillation frequency.

An amplifier without oscillation is a stable amplifier and an amplifier with oscillation is an unstable amplifier. An amplifier is said to be unconditionally stable if it does not oscillate for any applied passive terminations and input signal frequency, else the amplifier is said to have potential instability.

Oscillation degrades performance of an amplifier. An oscillating amplifier usually produces a strong RF signal that may interfere with the useful signals. In some cases it leads to failure of transistor [14]. Oscillation in an amplifier is undesirable and needs to suppressed.

The process of checking stability of an amplifier is referred to as stability analysis. A method that could (i) detect oscillation for all operating conditions, (ii) find

right place in the circuit for suppressing the oscillation and (iii) give the values of stabilization network is referred to as rigorous stabilization method in this work.

A transistor can exhibit negative resistance when it is fed with DC, small and large AC (alternating current) signals. This implies that oscillation is a possibility with these signals. Stability analysis of an amplifier operated on DC and small AC signals are performed with μ factor [15]. It uses small-signal S-parameters and is valid for one bias point.

Large-signal operation covers various bias points, hence it is not possible to do stability analysis with μ factor. One may think of applying μ factor analysis individually at all bias points covered by large-signal, but that does not guarantee stability. Oscillation in power amplifiers is a large-signal phenomena. It occurs due to the negative resistance exhibited by transistor when pumped with large RF signals [3] and may not be observed when pumped with small-signals at the same bias points. Therefore, small-signal μ factor indicating stable operation at all these bias points doesn't necessarily guarantee amplifier stability. Stability analysis for large-signal operation of the amplifier has to be based on large-signal simulations [15].

1.1 Thesis Motivation and Background

Motivation

This project is commissioned by NXP Semiconductors, to find a simple and effective stability analysis method for power amplifiers. The importance of a rigorous stability analysis in simulation at NXP is realized, when a customer complained about oscillation in one of its power transistors. The oscillation occurred at low temperatures for a given gate bias voltage during large-signal operation. This could have resulted in wastage of 50.000 transistor samples. However, it is solved by shifting the operating gate bias voltage with mutual agreement.

The oscillation occurred beyond nominal operating range. Measurements at such extreme temperatures require special lab sites. It is time consuming to do measurements at every stage of transistor development. Therefore, it is concluded to look for simulation methods and tools for rigorous stability check at all operating conditions. This conclusion further raised two important questions: What are the methods to perform large-signal stability analysis ? and Which is the most feasible among them ? Apart from answering these questions, this thesis includes a case design to demonstrate the use of the most feasible method. This thesis also depicts a complete design procedure for microwave power amplifiers.

Background

Power amplifiers operate at large-signals and exhibit weak and strong nonlinear effects [5]. Such circuits are efficiently simulated using harmonic balance (HB) al-

gorithms. Stability analysis of these circuits require analysis of their HB simulated solution using some analysis methods. These methods use different ways to obtain transfer function of the circuit and employs their respective criteria to decide on circuit's stability. Implementation complexity, completeness in stability analysis and giving direction on stabilization of the circuit are the factors that define a good stabilization method.

Nonlinear stability analysis methods such as Ohtomo [16] and normalized determinant function (NDF) [17, 18] are used frequently to analyze the HB simulated solution of the power amplifier for stability. They can detect and quantize unstable operating conditions but cannot provide complete information on location and values of stabilization network. Moreover, their implementation complexity and usage of high computation resources makes them unfeasible to use in a general purpose design procedure.

An alternative method based on pole zero identification [9, 19] for detection of oscillations and stabilization of linear/nonlinear circuits is utilized in this work. This method has been successfully used to detect oscillations in power amplifiers [3,20–23] and monolithic microwave integrated circuit (MMIC) power amplifiers [10]. The fact that an oscillation is associated by a closed loop [13] is utilized by this method. This method treats the amplifier as a closed loop control system and calculates its closed loop single input single output (SISO) transfer function [19]. The transfer function will be resolved into poles and zeros. Stability of the amplifier is then observed and controlled by varying these poles and zeros using control system techniques [6]. Special software called Stability Analysis tool (STAN) [24] is used to extract poles and zeros of the amplifier from its transfer function data.

1.2 Objective and Scope of the Thesis

The main objective of the thesis is to demonstrate the use of pole zero identification method for stability analysis of a power amplifier. For this, a 2.32-2.37 GHz class AB power amplifier is designed with NXP's experimental power transistor and is stabilized using pole zero identification method. A power amplifier design procedure that is standardized in development group at NXP is followed to design the class AB amplifier. One contribution of the author to design procedure is the validation of template in ADS 2011 for power amplifier design at NXP.
The scope of this thesis is limited to,

- Literature review of existing large-signal stability analysis methods and selection of a suitable method.
- Explaining concepts related to pole zero identification method.

- Demonstrating detailed intermediate steps of pole zero identification method, by stabilizing an example pre-designed push-pull amplifier using simulation tools ADS, STAN and MATLAB.
- Validation of the pole zero identification method with conventional liner stability factor for small-signal stability analysis.
- Load pull measurements of NXP's power transistor.
- Design and simulations of a class AB power amplifier in ADS made with NXP's transistor.
- Fabrication, prototyping, stabilization and performance measurements of the class AB amplifier.
- Class AB amplifier design evaluation.

1.3 Thesis Outline

The whole report is divided into 9 chapters. Chapter 1 gives introduction to large-signal stability problem, thesis motivation, background, objective, scope.

Chapter 2 is "A Brief Review of Power Amplifier Theory". In this chapter, Power amplifier's performance parameters, types of power amplifiers, their biasing requirements and performance (efficiency) differences are discussed. A brief introduction to power transistor, load pull measurements and a general power amplifier design procedure used in development group at NXP is given. Later in Chapter 7, the same design procedure is followed to design a class AB amplifier. At the end of this chapter, stability issues, common oscillation types in a power amplifier and requirements of a rigorous stabilization method are given.

Chapter 3 is "Control System Theory". In this chapter, introduction to control systems is given and related concepts such as transfer function, poles & zeros and closed loop systems are explained. The relation between stability and poles, criterion to detect oscillation and use of root locus method to get direction on stabilization of a control system is provided. This chapter gives background to understand the theory of pole zero identification method given in Chapter 5 and the stabilization procedure given in Chapter 6.

Chapter 4 is "Pole Zero Identification Method Background". This chapter presents the background and literature review of pole zero identification method. This chapters helps to understand the motivation in choosing pole zero identification method for large-signal. It clarifies the need of a detailed step by step procedure for pole zero identification method presented in this work.

Chapter 5 is "Pole Zero Identification Method Theory". This chapter presents the theoretical background and practical considerations of pole zero identification method. STAN software with its practical problems are discussed in brief. At the end of this chapter, the templates in ADS to perform small-signal and large-signal stability analysis are given. This chapter serves as a backbone to Chapter 6.

Chapter 6 is "Pole Zero Identification Method Application". In this chapter, a detailed step by step procedure in stabilizing a push-pull amplifier using pole zero identification method is given. Design of two different stability networks using root locus method is presented. The obtained small-signal stability result using pole zero identification method is compared with μ factor for validation. The effect of stability network on the amplifier's performance is also analyzed. This chapter fully utilizes the concepts, tools and procedure described in Chapters 3 & 5.

Chapter 7 is "Design and Stabilization of a Class AB Amplifier". In this chapter, a 2.32-2.37 GHz class AB power amplifier is designed and stabilized by fully utilizing concepts, tools and procedure described in Chapters 2, 3, 5 & 6.

Chapter 8 is "Performance Measurements and Design Evaluation". In this chapter, the performance measurements of the designed and stabilized class AB amplifier is reported. The amplifier design is evaluated by comparing load pull measurements of the amplifier and the transistor used in the amplifier. The performance measurements of the amplifier before and after stabilization are reported. The discrepancies observed in the results are explained. The main outcomes of the thesis are presented at the end of this chapter.

Chapter 9 is provides conclusions from the work and the suggestions for future investigations.

2. A BRIEF REVIEW OF POWER AMPLIFIER THEORY

Today, applications of RF and microwave engineering have extended to industrial, scientific and medical (ISM) fields apart from wireless communications. These applications require high RF power to be delivered. For example, a RADAR needs RF power up to few hundreds of kilo watts. In communication systems, evolution of new generations (3G, 4G & LTE) has demanded more and more RF power to be transmitted. At the same time, cost and size of transmitting equipment is also a concern. This has led to the evolution of various technologies, types and design considerations both at transistor and amplifier level.

This chapter gives a review of power amplifiers and their performance parameters. The basic power amplifier types, a general design procedure and introduction to instabilities in power amplifiers are presented.

2.1 Performance Parameters of Power Amplifier

This section presents definitions of power amplifier main performance parameters. They include efficiency, linearity, power gain and return loss (RL).

2.1.1 Efficiency

Efficiency is an important parameter in power amplifier design. High efficiency helps to reduce size and increase reliability and ruggedness of power amplifiers. For example, high efficiency of a power amplifier in base station leads to less power losses and low heat dissipation in the amplifier circuit. This reduces size of cooling equipment thereby reducing total size of the base station. Moreover, low dissipation decreases damaging effect of power transistor and allows the amplifier to operate over long period of time. This increases life of the base station. In mobile devices, high efficiency of power amplifier means less dissipation of supply voltage and longer battery life.

In general, efficiency is defined as ratio of output power to input power. This definition can be further classified based on whether the input power is considered with or without DC. The Figure 2.1 shows the flow diagram of various powers in the circuit that are useful to define efficiency.

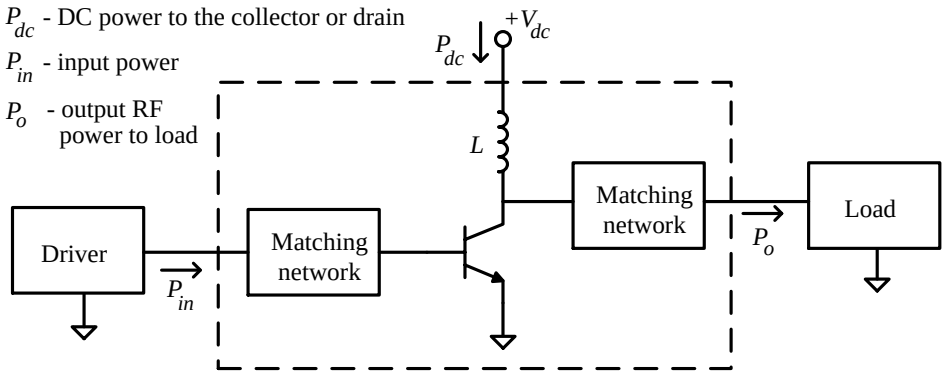

Figure 2.1: Block diagram of RF power amplifier represented with the flow of available input power (P_{in}), DC power supply (P_{dc}) and output power delivered to load (P_o) for the purpose of efficiency definition [2].

(a)Collector efficiency: Collector efficiency (Bipolar junction transistor (BJT)) or drain efficiency (Field effect transistor (FET)) is defined as the ratio of output RF power dissipated into load to DC power supply given to collector or drain [2],

$$\eta = \frac{P_o}{P_{dc}} = \frac{P_o}{V_{dc}I_{dc}}.$$

Where V_{dc} is DC supply voltage and I_{dc} is DC current that flows when the power amplifier is driven with input signal.

(b) Overall efficiency: Overall efficiency is defined as,

$$\eta_{overall} = \frac{P_o}{P_{dc} + P_{in}} = \frac{P_o}{P_{dc} + \frac{P_0}{G_P}}; G_P = \frac{P_o}{P_{in}}$$

The variable G_P in above equation represents amplifier's power gain.

(c) Power added efficiency (PAE): Power added efficiency is defined as,

$$\eta_{PAE} = \frac{P_o - P_{in}}{P_{dc}} = \frac{P_o - \frac{P_o}{G_P}}{P_{dc}}$$

2.1.2 Linearity

Linearity is the capability of a power amplifier to reproduce time domain input signal or waveform at output without having distortion in its amplitude and phase [5]. For an ideal linear amplifier, its output amplitude should increase linearly with its input amplitude and their relative phase difference should be zero. If the input and output signal peak amplitudes are not linearly related or if the phase difference between them is other than zero, then the signal is said to be distorted. This distortion is caused by the presence of strong interference signal around the desired signal.

Linearity for a base station power amplifier is sometimes characterized by using Adjacent Channel Power Ratio (ACPR) measurements. This measurement is similar to third order intermodulation distortion (IMD3) measurements [11]. ACPR specifies the amount of distortion in dBc/Hz that occurs in output spectrum side bands due to nonlinearity of the amplifier.

When an amplifier encounters interference, it produces several mixing components of input signal frequency and interference signal frequency at the output. These frequency modulated components at the output are called intermodulation products. The distortion caused by them to the carrier signal is called intermodulation distortion. The amplitude and frequency of these products depends on nonlinearity of the amplifier. Some of these intermodulation products (especially third order intermodulation products) fall in the vicinity of carrier. When the input signal (carrier) power is increased, they tend to increase in amplitude three times faster than carrier signal and ultimately lead to its distortion. The amount of distortion caused by these intermodulation products is characterized by ACPR measurements.

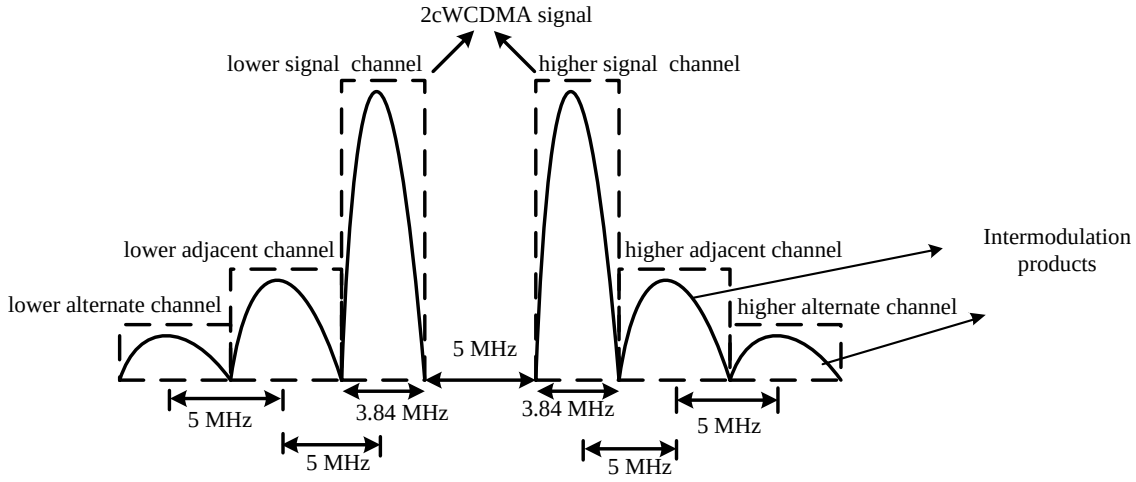

Figure 2.2: ACPR measurement signal setup.

Adjacent channel power ratio is defined as the ratio of average power in adjacent frequency channel to average power in transmitted frequency channel [25]. ACPR can also be defined as the ratio of power spectral densities (PSD) between carrier and specified offset band [26]. For base station power amplifiers, ACPR measurements are performed by feeding the input with a two tone wide band code division multiple access signal (2cWCDMA) with the adjacent channels (interference channels) placed at an offset of $\pm$ 5 MHz and $\pm$ 10 MHz as shown in Figure 2.2. The amount of distortion is calculated as the difference in power level of the carrier and the interference that fall in $\pm$ 5/10 MHz vicinity of the carrier. ACPR is used to characterize this distortion in terms of dBc/Hz. This refers to the difference in power levels of interference with respect to carrier in a 1 Hz bandwidth. Higher the ACPR of a circuit, lower is the distortion and greater is its linearity.

2.1.3 Power Gain (G_P)

Power gain is defined as the ratio of output power to input power of a power amplifier operating with a given load impedance [25]. It is expressed in dB .

$$G_P = 10\log\left(\frac{P_{out}}{P_{in}}\right)$$

P_{out} is the output power delivered to load, measured in watts and P_{in} is the available input power measured in watts.

2.1.4 Return Loss (RL)

Input return loss is the ratio of reflected power and input power of a transistor or module operating in a given load system [25]. It is expressed in dB.

$$RL = -10 * \log\left(\frac{P_{ref}}{P_{in}}\right)$$

P_{ref} is the reflected power measured in watts with given load and P_{in} is the input power measured in watts delivered into transistor. Measurement of these powers is given in Chapter 7.

2.2 Types of Power Amplifiers

Power amplifiers are classified as class A, B, AB, C, D, E, F based on their operating characteristics [27]. The operating characteristics include DC bias condition, conduction angle and output terminations at fundamentals and harmonics. These classes can be further divided into two broad categories, transconductance amplifiers (class A, B AB & C) and switch mode amplifiers (class D, E & F) [5]. Transconductance amplifiers are the general voltage controlled current source amplifiers. Further classification in transconductance amplifiers is based on their conduction angle and is discussed in the following sections.

2.2.1 Class A Amplifiers

Class A power amplifier conducts output current throughout entire RF cycle (0 to 2π). For this to happen, the transistor has to be biased at middle of the current voltage (IV) characteristics as shown in Figure 2.3.

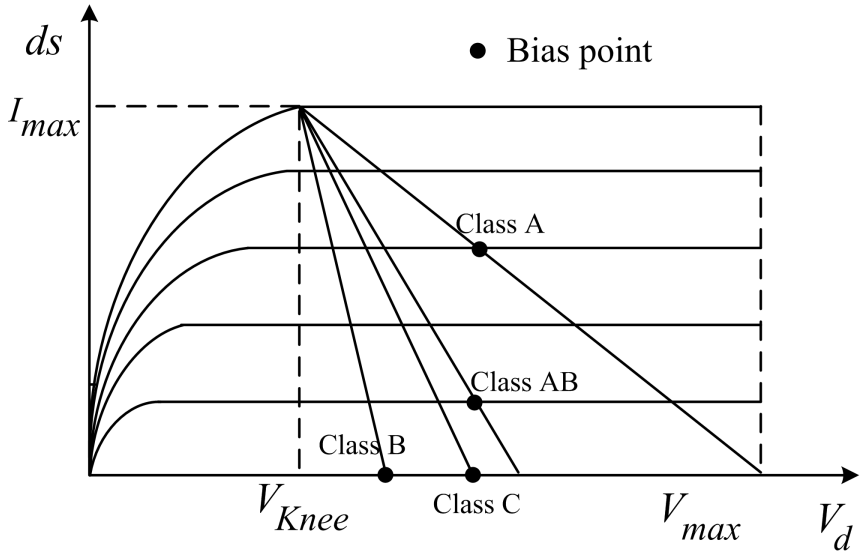

Figure 2.3: Operating classes of transconductance amplifiers and their corresponding bias points [3].

The bias point should be exactly in between knee voltage V_{knee} and maximum voltage V_{max}. Their output current waveform follows output voltage waveform as shown in Fig. 2.4. Class A amplifiers conduct for entire input RF signal period and produces a signal (time domain) with little distortion at output, hence their linearity is good. In class A amplifiers, the dissipation takes place for entire conduction period. Hence, they have an ideal efficiency of only 50% [2].

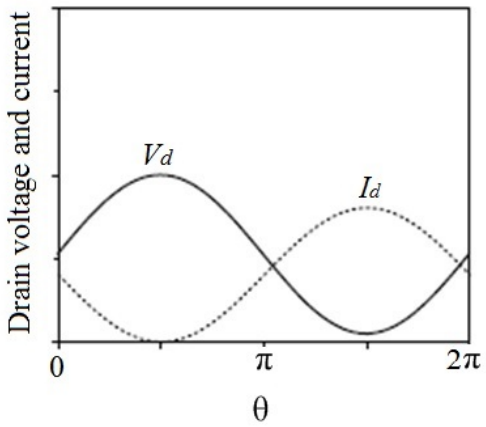

Figure 2.4: Class A amplifiers drain voltage and drain current waveforms [3].

2.2.2 Class B and Class AB amplifiers

A class B amplifier conducts during one half cycle per one RF period of input signal. For this to happen, transistor gate has to be biased such that it is ON only for half of input RF cycle. Hence the conduction angle of a class B power amplifier is π. Since dissipation is not taking place for one half cycle, class B amplifiers have an improved theoretical efficiency of 78.5 % ($\pi/4$) [2].

Popularly known push pull amplifiers [2] are made of two transistors biased for class B operation and combined at the output. The transistors are ON complementarily per half cycle for entire RF period. This helps to produce entire RF waveform with improved efficiency at output.

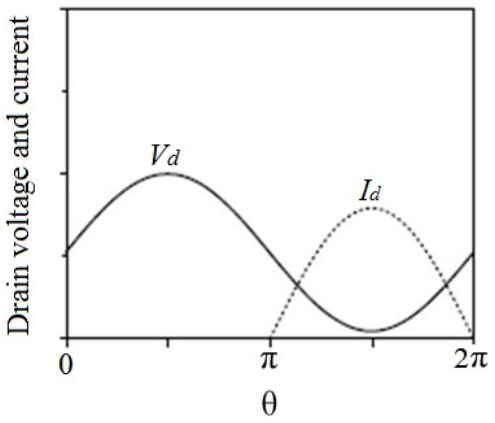

Figure 2.5: Drain voltage and drain current wave forms of class B amplifier [3].

Class AB amplifiers operation is also similar to class B amplifiers. In this case, biasing is done such that the conduction angle is in between 2π & π. Therefore, ideally their efficiency also lies in between 50 % & 78.5 % [2]. Class B amplifiers can have a good compromise in between high efficiency and high linearity. Hence, these amplifiers are highly used in communication applications. The drain voltage and current wave forms of a MOS transistor are shown in Figure 2.5.

2.2.3 Class C amplifiers

Conduction angle of class C amplifiers is less than π. Efficiency of class C amplifiers is in between 75% and 80% [2]. Ideally, efficiency can be 100% for 0 conduction angle, but this is not possible in practice. This is because, when the conduction angle is zero its corresponding output power also becomes zero.

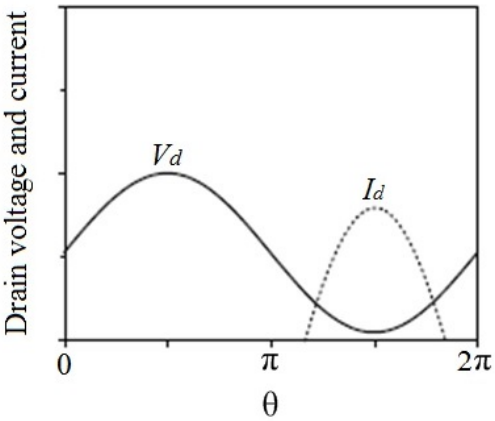

Figure 2.6: Drain voltage and drain current wave forms of class C amplifier [3].

Since these amplifiers conducts for less than half a cycle, reproduction of time domain input signal at the output is poor. Hence linearity of class C amplifiers is poor. The drain voltage and current wave forms of a class C amplifier are shown in Figure 2.6

2.3 Power Transistors

The increase of high power RF applications in Industrial Scientific and Medical (ISM) band has demanded more power to be transmitted or fed into a system. This high output power (and improved efficiency) is achieved by increasing output current and voltage of the transistor. The high output current can be achieved by increasing drain area and periphery of the transistor. As a consequence, size and cost of transistor also increases. For effective and economic power transistor design, its drain is divided into several fingers and are connected together (Fig. 2.7). This increases drain periphery for a given area of transistor die [4]. The layout of a power transistor inside package is shown in Figure 2.7.

Thickness of transistor die, type of internal matching (using bond wires and MOS capacitance as shown in Fig. 2.7) and design on the die depends on operating conditions. During transistor design, care will be taken such that its large signal source and load impedances transform to desired impedances for operating frequency. This is achieved by using a pre-internal matching in the transistor package itself. This kind of transformation helps to reduce losses and increase bandwidth when an external matching is realized to design a power amplifier [4].

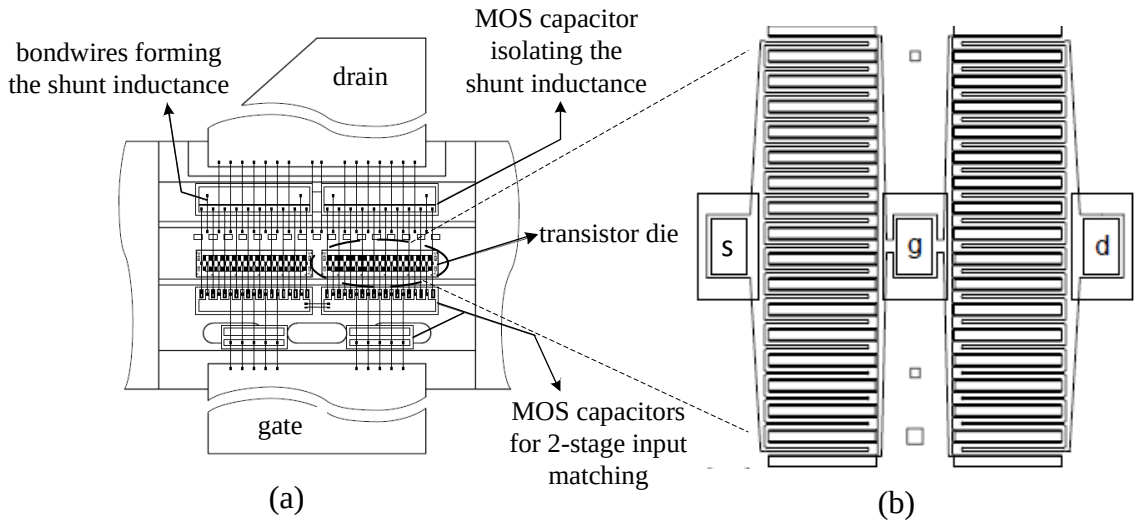

Figure 2.7: (a) Layout of power transistor. (b) Gate, drain and source arrangement on die in typical LDMOS transistors [4].

2.4 Power Amplifier Design

This section presents and discusses general steps in a power amplifier design. Fig. 2.8 shows flow diagram of a power amplifier design.

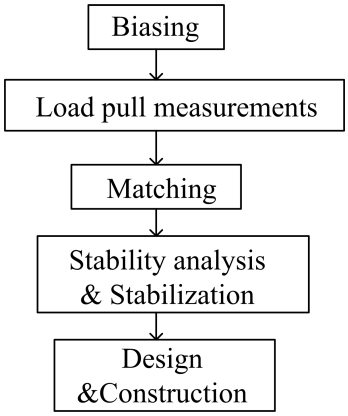

Figure 2.8: General power amplifier design flow followed in development group at NXP

2.4.1 Biasing

Biasing of a power amplifier is done according to its operating class. A class AB power amplifier bias point in the IV transfer characteristics is shown in Fig. 2.3. Biasing is done by initially applying drain to source voltage (V_{ds}) at quiescent point. Gate to source voltage (V_{gs}) is then increased till the output DC drain to source current (I_{ds}) reaches its quiescent point. Transistor used for power amplifier design in this work is biased for class AB operation with $V_{ds} = 28V$ and $I_{ds} = 1400mA$ (corresponding $V_{gs} = 2V$). Biasing at quiescent point gives maximum RF signal swing at the output. However, for a given bias condition, output signal swing also depends on termination impedance at transistor output. This will be explained in section 2.4.3

In general, for high power amplifiers operating at microwave frequencies, bias voltages (V_{gs}, V_{ds}) are applied using quarter wave micro strip transmission lines [13]. These lines are connected to ground at one end with an RF capacitor. The other end is connected respectively to gate and drain of the transistor . This RF capacitor is chosen such that it provides low impedance at the operating frequency. Therefore at this frequency, the lines are connected to ground and act as open when looked from the other side (from gate and drain terminals). This makes the useful signal not to escape into bias lines, thereby reducing possible losses. Any signal at other frequencies is grounded through RF capacitors. Next step is to find large-signal input and output impedances of the transistor for given bias.

2.4.2 Load Pull Measurements

Load pull measurements are performed to find large-signal optimum source and load impedances of power transistor. Optimum here would mean optimum power gain, optimum power and optimum efficiency of the transistor. The load selected for designing the power amplifier should be a good trade off between power, gain and efficiency. The selection is done by measuring gain, power and efficiency of the power transistor at all source and load impedances for given operating conditions.

Load pull measurements can be made easy by computer aided design (CAD) analysis of the measured results [5]. The CAD based analysis give contours of peak power, gain and efficiency for measured source and load impedance points. This helps to predict direction and location of optimum source and load in the Smith chart [28] with less effort. Block diagram of a typical load pull measurement setup is shown in Figure 2.9.

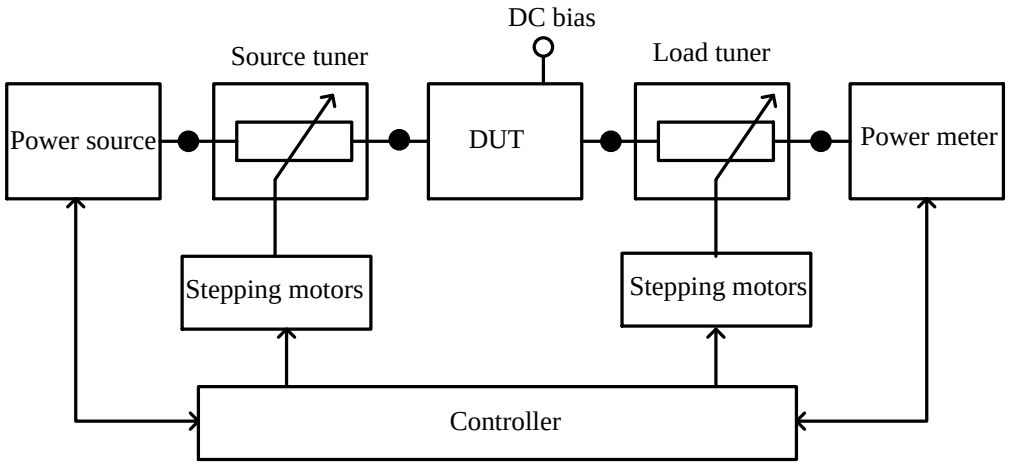

Figure 2.9: Typical load pull measurement setup [5].

Initially, source impedance is tuned to find the optimum for given operating conditions (bias, frequency) using contours. An input power required to produce average output power is used to drive the transistor for this (source pulling) measurement. For example, a power amplifier with 18 dB gain can deliver a peak power of 54 dBm at 1 dB compression point. If the average output power is 47 dBm, then the input power required to perform source pull measurement is 47 dBm - 18 dB = 29 dBm.

Next, load impedance is tuned to find the optimum for given operating conditions. An input power required to drive the transistor into compression is used to perform this measurement (load pulling). Usually, output power of a power amplifier is specified as the power at 1 dB compression point. For the same example in above paragraph, input power required to drive the transistor to perform load pulling is 54 dBm - 18 dBm = 36 dBm.

This is an iterative process between source and load pull till the optimum source is found [28]. Once the optimum source is found, it is then fixed. Next, load is tuned to find the optimum. Optimum load impedance is a trade off in between peak power, peak gain and peak efficiency. It lies on the line (load line) connecting centers of power, gain and efficiency contours. Above said measurement is for a single frequency, it has to be repeated for other operating frequencies.

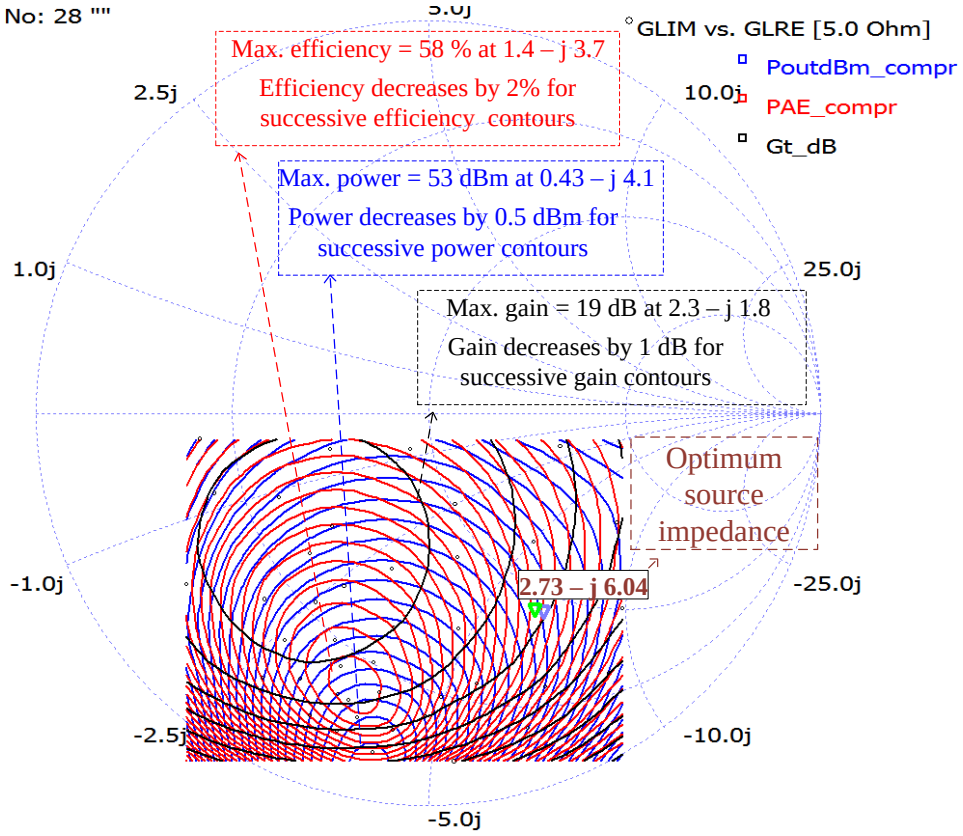

Figure 2.10: Load contours for power, gain and efficiency of NXP's power transistor at 2.3 GHz. Smith chart is normalized to 5Ω.

The optimum source and load impedances for NXP's power transistor biased for class AB operation with $V_{gs} = 2V, V_{ds} = 28V$ at 2.3 GHz are shown in Fig. 2.10. The figure shows source and load contours for power, gain and efficiency.

Load pull measurements are performed for same transistor at frequencies 2.23, 2.3, 2.4 and 2.5 GHz respectively. The corresponding optimum source and load impedances are given in appendix A1. The transistor is intended to operate in between 2.32 to 2.37 GHz. But, because of non-availability of tuner calibration files [28] exactly at those frequencies, measurements are not performed at those frequencies. The measured impedances at 2.3 and 2.4 GHz are enough to give a good estimation of impedances at frequencies in between them. Moreover new tools (Advanced design system - ADS 2011) can be used to interpolate and estimate approximately the in-band impedances.

2.4.3 Matching

Due to large-signal operation, small-signal S-parameters are not used to design a power amplifier. Instead, it is designed using measured large-signal impedances.

It is well known from maximum power transfer theorem that, power delivered from source to load can be maximized by using a conjugate termination. Then, it is logical to assume of realizing a conjugate match at input and output of the power transistor. This assumption is limited at the output in practice by two factors of amplifier's input generator, (i) the maximum current it can supply and (ii) the maximum voltage that it can sustain across its terminals.

For example, a current generator as shown in Fig. 2.11 with 100Ω output resistance can deliver a maximum current of 1 ampere. Then, by using maximum power transfer theorem to obtain maximum output power, we may terminate it with 100Ω. For simplicity, a termination with pure resistance is considered. This makes voltage across generator to be 50V. If this current generator were the output of a transistor, then it can happen that this voltage exceeds maximum rating V_{max} of the transistor. Moreover, the transistor voltage would be limited by available DC supply.

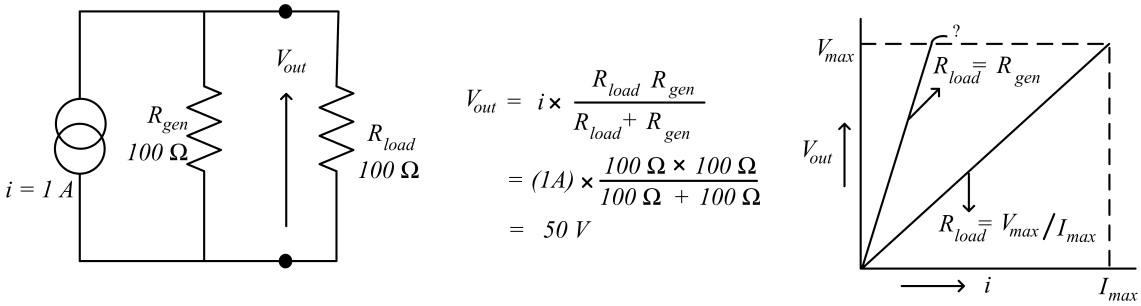

Figure 2.11: Conjugate match (simplified to show limiting action of current) and load line match [5]

In practice, with conjugate match at output, the device output current shows a limiting action before reaching its maximum (I_{max}) [5]. This is because, the maximum voltage that the device can handle is reached much before the current becomes maximum and further improvements to increase the output current leads to device breakdown. This means, the transistor is not being used to its fullest capacity. To have a maximum voltage and current swing at the output, the device has to be matched to a lower value of load resistance called R_{opt}. This is found by using load pull measurement as described in the previous subsection.

It is difficult to model a high power transistor having strong nonlinear effects [2]. This makes the power amplifier design a highly repetitive process using simulations. To overcome this, a simulation procedure that is purely dependent on transistor measured load pull data can be used. CAD design tool ADS in its new version (ADS 2011) has provided a template to design output matching network of a power

amplifier based on transistor load pull data. It is called Data Based Load pull (DBLP) template. The data file obtained from load pull measurements is loaded into the template. Matching can be done to desired load (optimum load) by tuning a predefined matching network. Performance parameters can be looked simultaneously in the data display page while tuning.

2.5 Stability issues in Power Amplifiers

This section presents and discusses oscillation mechanism and oscillation types in a power amplifier. The criterion for a rigorous stability analysis method is presented at the end of this section.

2.5.1 Oscillation mechanism in power amplifiers

Transistor parasitics are sensitive to input signal amplitude and affects flow of current through transistor channel. This makes the transistor to exhibit negative resistance at some point when terminated by an appropriate impedance [15]. For example, suppose in nonlinear region, the transistor output current (i_{out}) through channel has a relation $i_{out} = 5V_{in} - V_{in}^2$ with input signal voltage (V_{in}). The differential resistance of this transistor can be obtained as, $\frac{di_{out}}{dV_{in}} = 5 - 2V_{in}$. This differential resistance is positive for $V_{in} < 2.5$ and negative for $V_{in} > 2.5$. This means, the transistor can exhibit negative differential resistance depending on the level of input signal.

Two points can be understood from the above example. First, non-linearity provides a feasible condition to exhibit negative resistance. Second, the negative resistance condition is fulfilled by applying sufficient V_{in}. In practice, non-linearity might be different from above case and may result in negative resistance at some other range of input signal amplitude (or input signal power).

An appropriate termination at the negative resistance port of this transistor combined with termination at the other port, leads to oscillation [13]. Hence non-linearity and large-signal operation in power amplifiers easily satisfy condition to form oscillation and is the reason for increased risk of instabilities in power amplifiers.

2.5.2 Types of Oscillations

Stability problem is encountered in all microwave amplifiers. Stability problem exhibited by a power amplifier is different. Initially, power amplifier may seem to be stable for small-signal, but after reaching some level of input power, as explained above, stability problem may arise. Non-linearity in combination with input signal amplitude provides sufficient negative resistance to form oscillation. This is mainly

because of the nonlinear gate to drain capacitance of power transistor at high power (amplitude) levels. Oscillation will possibly occur at input power levels for which negative resistance triggers. This is practically observed in class AB amplifier designed with NXP's power transistor. Initially, with 50 Ω termination the amplifier is unconditionally stable. With same terminations,when the input power level to the amplifier is increased to 28 dBm, oscillation started to appear around 16.5 MHz. The oscillations disappeared when input power level is increased above 32 dBm. This is similar to the case reported in [20].

The most commonly observed oscillations in power amplifiers are spurious oscillations and sub-harmonic oscillations [15]. If an oscillation in an amplifier due to applied external conditions (frequency, bias, termination, temperature and signal level) occur at a frequency unrelated to input frequency, then it is called a spurious oscillation. These oscillations occur at a frequency lower than input frequency [15]. In most of the cases, this oscillation frequency gets mixed with input frequency and produce an output spectrum similar to mixer output spectrum as shown in Figure 2.12.

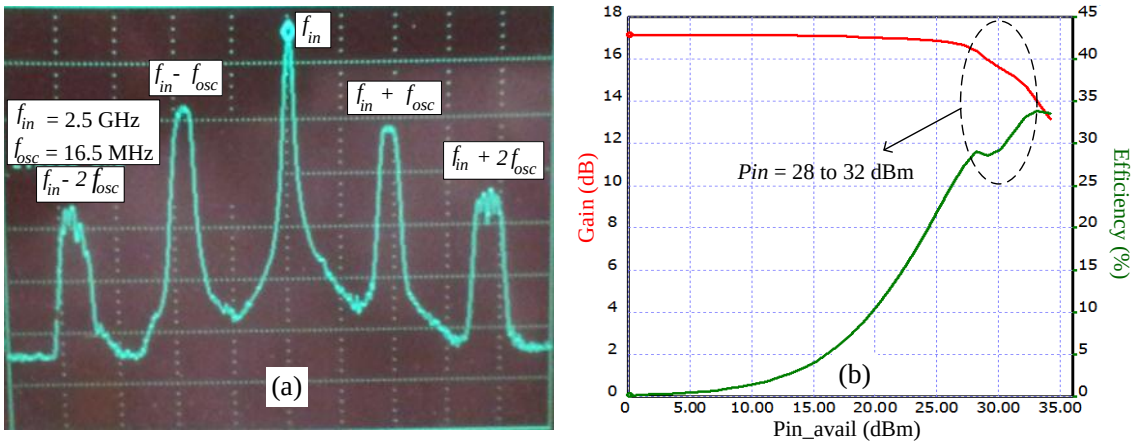

Figure 2.12: (a) Mixer like spectrum observed at the output class AB peak amplifier made of NXP's power transistor for an input frequency of 2.5 GHz. (b) Jump in gain and efficiency curves of the amplifier for 2.5 GHz at an input power level of 28 to 32 dBm.

If an oscillation in an amplifier due to applied external conditions (frequency, bias, termination, temperature and signal level) occur at a frequency harmonically related to input frequency as shown in Figure 2.13, then it is called a sub-harmonic oscillation. This type of oscillation occurs in multistage amplifiers with power combining structures.

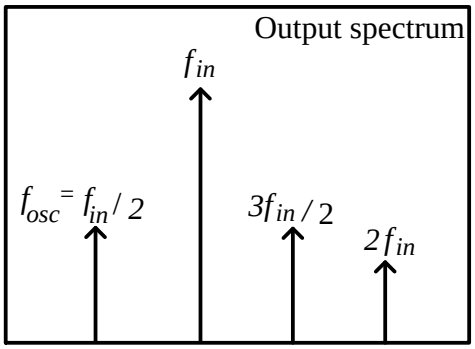

Figure 2.13: Example of a sub-harmonic oscillation spectrum [3].

Another type of oscillation that is observed during measurements is the noisy bumps [3] in output spectrum. They seem to appear as noise but actually occur due to reduced stability margins at those frequencies. In this case the feedback is not sufficient enough to form a strong oscillation. At the same time, the damping in the circuit is also not so strong to suppress the oscillation completely. In terms of control systems, it can be said that the pole of the circuit is quite close to the imaginary axis (unstable region) but is in the stable region. One such noisy bump spectrum observed during the measurements of class AB peak amplifier designed with NXP's transistor is shown in Figure 2.14. Some other instability phenomena which are specific to switch-mode (class E) power amplifiers are discussed in [3].

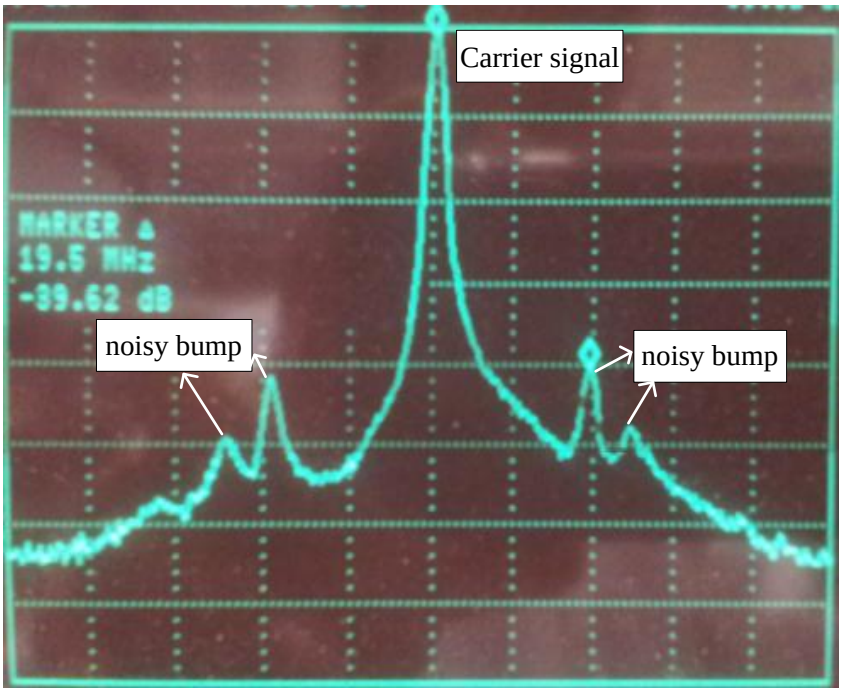

Figure 2.14: Noisy bump observed in the output spectrum of class AB amplifier around 19.5 MHz when a resistive damping is used to suppress the oscillation occurred due to 2.5 GHz

2.5.3 Stability Analysis

Oscillation in power amplifiers degrade their performance in gain, output power and efficiency. This is highly undesirable in any kind of amplifiers. Moreover, oscillations may act as strong interference to other applications operating in adjacent frequency channels. In some cases oscillation leads to very high currents and results in breakdown of the transistor. Hence it becomes important to perform stability analysis before realizing a design.

Oscillation that occur in an amplifier when it is fed with DC and small AC signals are detected by μ factor [13]. Oscillations due to large input signals are not detected by μ factor because of their non-applicability. Detection of oscillation due to large-signal is based on analyzing HB simulated solutions for stability. An appropriate large-signal stability analysis method of HB simulated solution and the accuracy of nonlinear model of the transistor is the key to detect oscillations in power amplifiers.

A rigorous stabilization method of microwave power amplifiers consists of three essential steps. They are,

1. Detection of oscillation and unstable operating conditions.

2. Identification of most feasible node/branch in the circuit to suppress oscillation with minimum performance loss.

3. Finding values of stabilization components.

3. CONTROL SYSTEM THEORY

A circuit can be considered as a black box with input and output terminals as contacts with outside world. It can be represented by a function in Laplace(s)-domain called transfer function [6]. This allows one to analyze it as a control system. The transfer function can be further resolved into poles and zeros and can be plotted onto s-plane. Stability of the circuit can be tracked with respect to location of these poles and zeros in s-plane. Conversely, stability can be controlled by moving these poles and zeros to a desired location in the s-palne using control system techniques [6]. This is an alternate way to deal with stability problem in microwave amplifiers.

This chapter presents basics of control systems required to understand pole zero identification method. Transfer function, poles & zeros, relation between stability and poles, stability criterion and root locus method are discussed.

3.1 Transfer function

Transfer function of a system is defined as the ratio of its output response to input excitation in Laplace domain [6]. It is simply a function in s-domain that transforms input to output. Lets us consider the example RLC circuit in Fig. 3.1 to understand transfer function and poles/zeros.

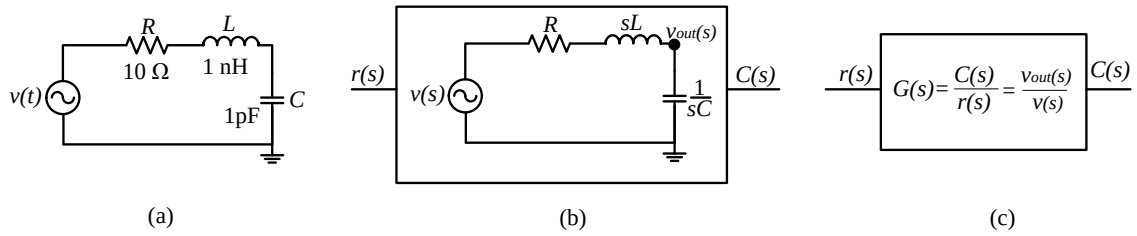

Figure 3.1: (a) RLC circuit in time domain, (b) Laplace domain (c) Transfer function.

The transfer function of the RLC circuit shown in Figure 3.1 is obtained as,

- Replace time domain elements in the circuit by their Laplace domain equivalents [6] as shown in Figure 3.1(b).
- Obtain the expression for output voltage using voltage division principle as,

$$v_{out}(s) = v(s)\frac{\frac{1}{sC}}{R + sL + \frac{1}{sC}}; (v_{out} = v_{in}\frac{\text{Impedance in output branch}}{\text{Total impedance}}) \quad (3.1)$$

- Now rewrite the above expression as the ratio of output voltage to the input voltage in Laplace domain,

$$\frac{c(s)}{r(s)} = \frac{v_{out}(s)}{v_s} = \frac{1}{s^2LC + sRLC + 1}. \tag{3.2}$$

Substituting the values of $R = 10\Omega, L = 1nH$ and $C = 1pF$ in equation (3.2) gives the transfer function, $\frac{c(s)}{r(s)} = \frac{1}{s^2*1nH*1pF+s*10\Omega*1nH*1pF+1}$. This on simplification gives,

$$\Rightarrow \frac{c(s)}{r(s)} = \frac{10^{21}}{s^2 + (2 * 0.158 * 3.16 * 10^{10}) + 10^{21}}. \tag{3.3}$$

In equation (3.3), $s = \sigma + j\omega$ is a complex variable where ω represents angular frequency. Equation (3.3) is the transfer function of the system shown in Figure 3.1(a) for $R = 10\Omega, L = 1nH$ and $C = 1pF$. This is called a second order system. It is equal to the degree of transfer function (equation (3.3)) denominator .

3.1.1 Poles and Zeros

The transfer function of a system can be represented in further simplified form by factorizing numerator and denominator as,

$$\frac{c(s)}{r(s)} = \frac{n(s)}{d(s)} = \frac{\prod_{i=1}^{n}(s + Z_i)}{\prod_{i=1}^{m}(s + P_i)}; (m \geq n). \tag{3.4}$$

In the above equation, $c(s)$ is output response and $r(s)$ is input excitation in Laplace domain, $n(s)$ is numerator and $d(s)$ is denominator of transfer function, Z_i are roots of numerator and P_i are roots of denominator. When a transfer function is represented in the form of equation (3.4), the roots of its numerator are called zeros and the roots of its denominator are called poles. These poles and zeros are plotted on complex s-plane to track various performance parameters of the system [6].

The transfer function in the equation (3.3) can be represented as,

$$\Rightarrow \frac{c(s)}{r(s)} = \frac{10^{21}}{[s - (-5 \times 10^9 + j3.12 \times 10^{10})][s - (-5 \times 10^9 - j3.12 \times 10^{10})]}. \tag{3.5}$$

Since there is no numerator polynomial in the transfer function (3.5), there are no zeros in this system. The roots of the denominator, $(-5 \times 10^9 + j3.12 \times 10^{10})$ and $(-5 \times 10^9 - j3.12 \times 10^{10})$ are the poles of this system (circuit). The poles are represented in s-plane as shown in Figure 3.2. In s-plane, horizontal axis represents real axis (σ) and vertical axis represents imaginary axis ($j\omega$). In the figure, ξ (damping factor) is the factor by which the circuit's output response is damped with respect to time and ω_n is the natural angular resonance frequency of the circuit. If

the values of R, L and C change, the location of poles also change in the s-plane. In other words, movement of poles in the $s-$plane represents variation of circuit component values.

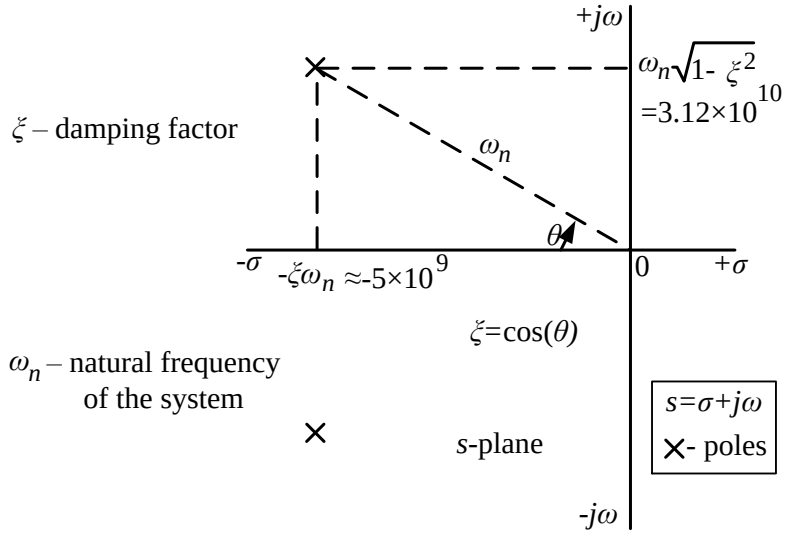

Figure 3.2: Poles of the transfer function of RLC circuit in Fig. 3.1 plotted in s-plane

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3.2 Closed Loop control System

A system with a feedback mechanism is a closed loop system. Since oscillation is associated with a feedback, considering the circuit in the form of closed loop system helps to study and solve the stability problem of a power amplifier.

Let us consider a closed loop system, the discussion is based on [6]. Any open loop system can be represented as a closed loop system by adding a feedback network. Any closed loop system can be made open by breaking the loop. Open and closed loop systems have their own advantages and disadvantages. Open loop systems are more stable and reliable but sensitive to external disturbances. Closed loop systems are less sensitive to external disturbances but have a greater chance of instability.

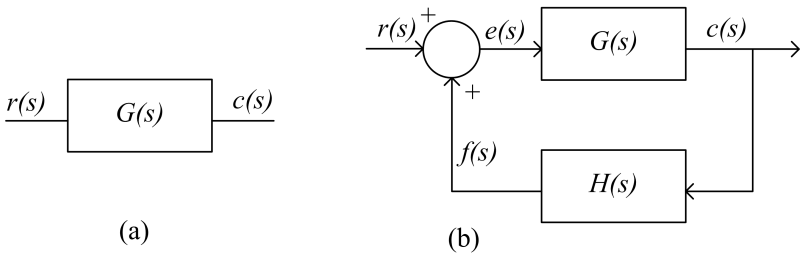

Figure 3.3: (a) Open loop control system (b) closed loop control system.

Open and closed loop control systems are shown in Fig. 3.3. In Fig. 3.3, variables $r(s)$, $c(s)$ and $f(s)$ represent the systems input excitation, output response and

feedback signal respectively. $G(s)$ is called open loop gain and $H(s)$ is called feedback gain. The variable $e(s)$ represents a corrected input signal after feedback.

Open loop transfer function (TF_{OL}) of the system in Fig. 3.3a is given as [6],

$$TF_{OL} = \frac{c(s)}{r(s)} = G(s). \tag{3.6}$$

Closed loop transfer function (CL_{TF}) of the system given in Fig. 3.3b is obtained from $e(s)$ as,

$$e(s) = r(s) + f(s),$$

$$\Rightarrow e(s) = r(s) + c(s)H(s); (\because H(s) = \tfrac{f(s)}{c(s)}),$$

$$\Rightarrow \tfrac{c(s)}{G(s)} = r(s) + c(s)H(s); (\because G(s) = \tfrac{c(s)}{e(s)}),$$

$$\Rightarrow c(s)(\tfrac{1-G(s)H(s)}{G(s)}) = r(s),$$

$$\Rightarrow TF_{CL} = \frac{c(s)}{r(s)} = \frac{G(s)}{1 + G(s)H(s)}. \tag{3.7}$$

Equation (3.7) represents closed loop transfer function of the system shown in Fig.3.3. In equation (3.7) $G(s)$ represents open loop gain and $G(s)H(s)$ is called closed loop gain. Any changes in the loop gain effects stability of the control system. If $G(s)H(s) = 0$, then $TF_{CL} = \frac{G(s)}{(1+0)} = G(s) = TF_{OL}$. This means, when loop gain is zero, closed loop transfer function of a control system is equal to its open loop transfer function.

If the closed loop gain $G(s)H(s) = 1$, then $CL_{TF} = \frac{G(s)}{(1-1)} = \infty$. This ('$\infty$') is independent of input. It means that, when loop gain is equal to 1 there will be an output even without input. Ideally, the output would be ∞ but it is limited by the system energy. This is the condition for oscillation in feedback control systems (circuits). According to Barkarhausen's criterion [29], a feedback network would oscillate when its loop gain becomes unity and when its feedback signal is in phase (0 or 360 degrees) with the input signal. In practice to start oscillation, loop gain should be greater than 1 [29].

3.3 Relation Between Stability and Poles

Transfer function of a closed loop system can be represented as,

$$TF = \frac{c(s)}{r(s)} = \frac{G(s)}{1 - G(s)H(s)} = \frac{(s - Z_1)(s - Z_2)\cdots(s - Z_n)}{(s - P_1)(s - P_2)\cdots(s - P_m)}. \tag{3.8}$$

In equation 3.8 $G(s)$ is forward gain, $H(s)$ is feedback gain, $Z_1, Z_2 \cdots, Z_n$ are

zeros and $P_1, P_2 \cdots, P_n$ are poles of the closed loop system shown in Fig. 3.3b.

It is evident form equation (3.8) that there will be a possibility of oscillation only when the denominator $(1 - G(s)H(s))$ is zero. This means stability depends on denominator and is independent of numerator. So, when a transfer function is plotted on s-plane as poles and zeros, stability can be related to location of poles, but not zeros. This means, the poles of a system lying in LHP conveys that it is stable and the poles lying in RHP conveys that it is unstable. But, the zeros lying in either LHP or RHP does not convey whether the system is stable or unstable. The relation between location of poles and system response is shown in Fig. 3.4.

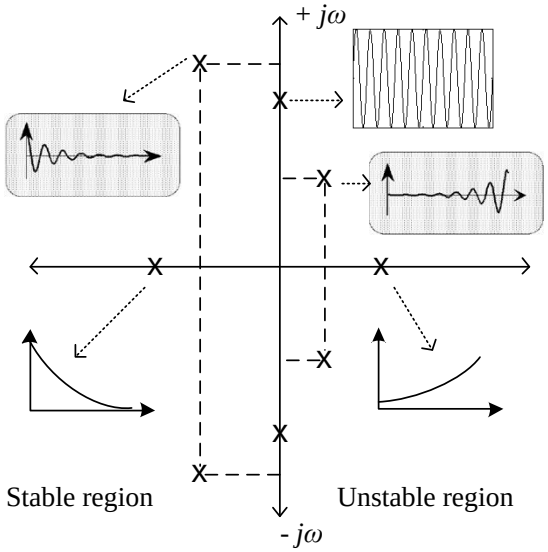

Figure 3.4: Relation between the location of the poles and the system response [6].

In brief, a closed loop control system is said to be stable if its poles are located in LHP (Left Half of s-plane). If the poles are in RHP (Right Half of s-plane) then the system is unstable [6]. A system having RHP poles would have an oscillation with increasing amplitude. Sustained oscillations occur when the poles lie on imaginary axis. In practice, a system having RHP poles sustains its amplitude at some point. Frequency of oscillation in this case is equal to the frequency at which the pole crossed imaginary axis.

3.4 Root Locus

Root locus is a locus of pole movement in s-plane for varying loop gain values [6]. Variation of any parameter in a closed loop system changes its loop gain. This parameter variation can be due to the variation of input operating conditions or due to addition of extra components into the system. For example, in case of high power MOS transistor, feedback capacitance (drain to gate) changes with input power and leads to change in loop gain. This leads to a corresponding change in position of its poles and zeros in s-plane.

It is important to know the movement of poles corresponding to varying operating conditions. This is because, initially the poles may be in stable region, but they might move to unstable region for some operating conditions. Hence to guarantee stability, movement of poles in the s-plane for varying operating conditions has to be known.

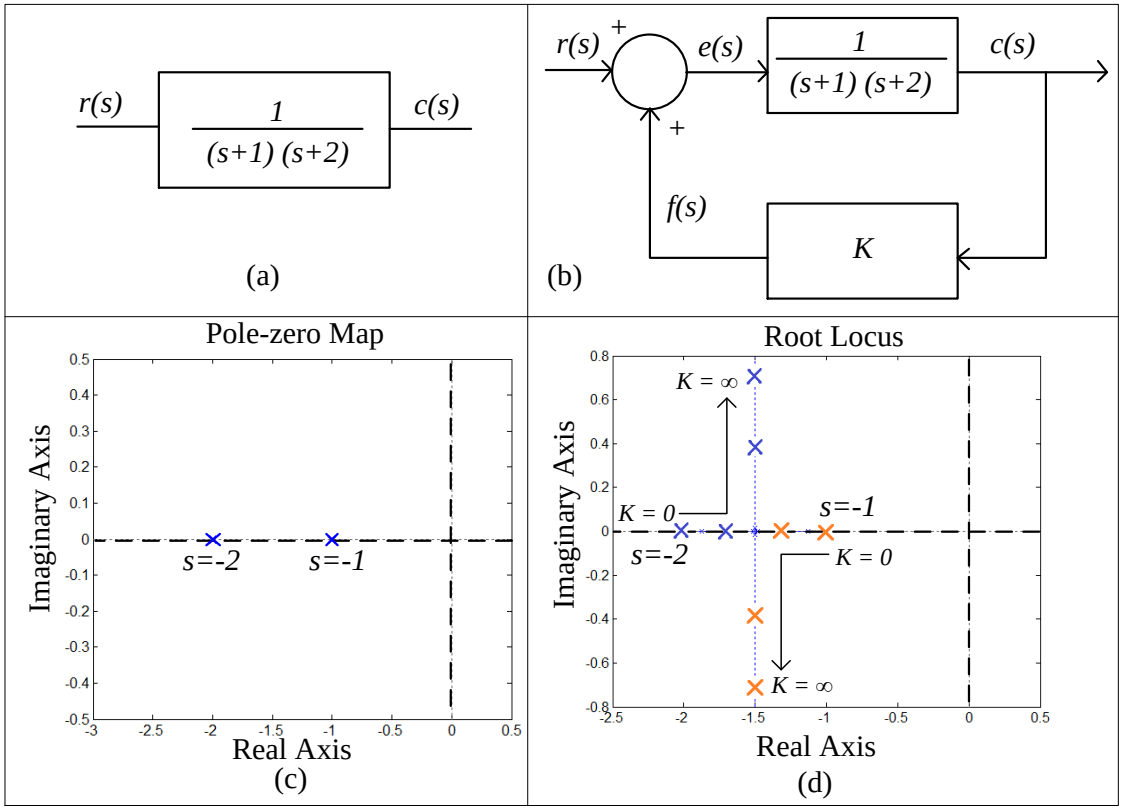

Figure 3.5: (a) Open loop system (b) closed loop system. (c) Pole zero plot of system in (a). (d) root locus plot for system in (b) [7].

Fig. 3.5a is an open loop system having poles at -1 and -2. This open loop system is converted to closed loop system by adding a feedback network having feedback gain K. Loop gain of the closed loop system is then given by $\frac{K}{(s+1)(s+2)}$. Ideally, it can have a minimum value of 0 and a maximum value of ∞. The variable K can vary in between these two values depending on input operating conditions. This makes the corresponding loop gain $\frac{K}{(s+1)(s+2)}$ of the closed loop system to vary. The poles specific to each K value also vary accordingly along the root locus path as shown in Fig. 3.5d. On the other hand, closed loop poles can be moved to a desired location on the root locus path by choosing K value and designing a feedback network accordingly. In some cases, additional feedback networks called compensators [7] would do this work. General electrical networks used for compensation are presented in appendix A2 along with their corresponding pole zero plots.

The movement of these closed loop poles can be generalized as follows,

Closed loop transfer function of the system shown in Fig. 3.5b can be represented as,

$$CL_{TF} = \frac{G(s)}{1 + KG(s)}, \tag{3.9}$$

$G(s)$ is the closed loop gain , K is the feedback gain and $KG(s)$ is the closed loop gain. Equation (3.9) can be further represented as,

$$CL_{TF} = \frac{n(s)/d(s)}{(1 + K(n(s)/d(s)))}, \text{where} G(s) = (n(s))/(d(s)). \tag{3.10}$$

$n(s)$ is the numerator corresponding to open loop zeros and *d(s)* is the denominator corresponding to open loop poles. Now if the variation of K is considered, then, when, $K = 0, CL_{TF} = \frac{n(s)}{d(s)} = OL_{TF}$. In this case poles and zeros of the closed loop transfer function are equal to that of the open loop transfer function.

When $K = \infty$, closed loop poles are then given by denominator of equation (3.10) as

$$1 + K\frac{n(s)}{d(s)} = 0 \Rightarrow K = \frac{-d(s)}{n(s)} = \infty \Rightarrow n(s) = 0 \tag{3.11}$$

But $n(s) = 0$ gives open loop zeros. This means, when K is varied from 0 to ∞, closed loop poles move from open loop poles to open loop zeros in the s-plane. This also means that the root locus path starts from open loop poles and ends at open loop zeros.

4. POLE ZERO IDENTIFICATION METHOD BACKGROUND

This chapter is divided into three sections. First section gives an introduction to harmonic balance simulation. Second section presents a review of large-signal stability analysis methods. Third section discusses previous works that used pole zero identification method. Finally, a conclusion from the discussion is presented at the end of this section.

4.1 Harmonic Balance

Harmonic balance (HB) is an efficient method to simulate microwave circuits operating at large-signal levels. It uses frequency domain description of linear lumped and distributed elements in the circuit. Nonlinear elements in the circuit are described in time domain but, Fourier/Inverse Fourier transforms are used to convert them to/from frequency domain.

HB simulation comprises of four steps [30]. The order of the simulation is as follows,

1. In the first step, initial conditions such as input power, frequency, number of harmonics, number of simulation points and error tolerance are specified.

2. In the second step, currents through linear elements and voltages across nonlinear elements in the circuit are calculated.

3. In the third step, inverse Fourier transform is used to convert the nonlinear voltages into time domain to calculate nonlinear currents. These currents are then converted back to frequency domain using Fourier transform.

4. In the fourth step, the calculated linear and nonlinear currents are checked for Kirchhoff's current law (KCL) in the circuit.

If KCL is not satisfied with error tolerance specified at the beginning of simulation, then the simulation starts iterating form step 2 to step 4 using Newton-Raphson method. This process continues until KCL is satisfied with specified tolerance in the circuit.

Mathematical representation of a circuit response after simulation is called circuit solution. It consists of a transient part and a steady-state part. There can be several transient and steady-state solutions for a circuit [15]. For example, if an amplifier is oscillating, then its solution consists of two steady states, one correspond to the oscillation and the other correspond to input generator. Since HB uses Fourier series expansion for the circuit variables, it only analyzes steady state solution [15] without considering the transient solution. This is advantageous in terms of shorter simulation time but disadvantageous in terms of stability analysis. This is because, in a HB simulation, different steady-state solutions may coexist for the same input parameters values and leads to wrong conclusion on oscillation [15]. This means the oscillation signal is undetectable. To avoid such cases, a small additional disturbance called perturbation should be added to the steady state HB simulated solution at all frequencies. Sustaining of the perturbation at any of the frequencies conforms oscillation.

The sustaining perturbation is detected using methods such as Ohtomo, NDF, AG and Pole zero identification. This complementary analysis of the HB solution is necessary to decide on oscillation in high power microwave wave circuits such as power amplifiers.

4.2 Large Signal Stability Analysis Methods - Review

This section presents a review of large-signal stability analysis methods. Advantages and disadvantages of these methods in the context of rigorous stability analysis is discussed.

4.2.1 Normalized Determinant Function (NDF) Method

The NDF method [18] [17] is used to analyze the HB simulated solution for stability. This method obtains a particular HB equation linearized over the circuits large-signal regime with respect to small-signal perturbations. The open loop transfer function of the linearized circuit is then calculated using a determinant function called return ratio (RR) [18]. This transfer function is analyzed for stability using Nyquist criterion [6].

NDF method could detect oscillations and unstable operating conditions, which is the first step towards circuit stabilization. But, it cannot differentiate between feasible and non-feasible node/branch in the circuit for stabilization, which is the second step towards stabilization. The third step of predicting stabilization component values is not fully possible with this method. It also uses much computation resources to calculate the return ratio and hence is not feasible to implement in power amplifier design.

4.2.2 Auxiliary Generator (AG) Method

In this method a small ideal external generator called auxiliary generator is connected to nonlinear circuit during HB simulation [3]. This generator is used to perturb the nonlinear circuit. Admittance as a function of frequency over this generator is calculated for stability analysis. Oscillation is detected using non-perturbation condition of the AG [3]. This condition is satisfied when the admittance function looking into the AG becomes zero [3]. By calculating the admittance function over AG for various parameter values and searching for parameters that lead to zero admittance, oscillation and unstable operating conditions are identified [31] [32].

This method is capable of detecting oscillation and the parameters that lead to the oscillation. It cannot give clear direction on feasible node in the circuit to control stability. Stabilization of the circuit using frequency selective components and finding their values is a cumbersome iterative process.

4.2.3 Pole Zero Identification Method

Pole zero identification method is another large-signal stability analysis method used to analyze HB simulated solution for stability. This method is similar to auxiliary generator method in application but different in analyzing the obtained result. It is applicable to any type of circuit (linear, nonlinear, multi device, multi-port) [30]. This method requires the closed loop single input single output (SISO) transfer function of the microwave circuit to be calculated [20]. Once the SISO transfer function is obtained, control system technique for closed loop stability [6] can be applied to analyze and control stability of the microwave circuit.

This method satisfies all the criteria for a rigorous stabilization method. It can be used to identify oscillations and parameters that lead to oscillation (first step) [22]. It can identify and differentiate between the feasible nodes/branches for stabilizing a circuit (second step) [20] [23]. It can be used to design suitable stabilization networks and to find their values (third step) [10]. Moreover, this method is simple and is feasible to implement in a power amplifier design.

The present work uses pole zero identification method. This method is developed by University of the Basque Country, Bilbao, Spain [33].

4.3 Pole Zero Identification Method - History

In [3] pole zero identification method is used to detect oscillation and unstable operating conditions in a class E power amplifier. It is mentioned that the amplifier has exhibited spurious oscillation for a particular input power range in practice. Stability analysis is performed by obtaining SISO transfer functions of the amplifier when swept with input drive power. STAN (Stability Analysis) tool is used to

identify poles and zeros from all these transfer functions. Unstable poles (RHP poles) are detected for input drive power in the range 5 to 15 W and it is shown to be in agreement with unstable operating conditions observed in practice. Stability of the circuit is achieved by placing a resistor at virtual node [3] in the circuit. The value of the stabilization resistance in this work is found using AG method. Resistance value is swept for all input power levels by connecting an AG to one of the circuit nodes. Admittance over AG is calculated and checked for non-perturbation [15] condition to conform oscillation (see section 4.2.2). A resistance that does not satisfy this condition for all input drive power levels is considered for stabilization. This process is repeated at other operating conditions to find a common resistance value that stabilizes the circuit globally.

In [18] pole zero identification method is used to detect a sub-harmonic oscillation in a monolithic microwave integrated circuit (MMIC) X band hetero junction bipolar transistor (HBT) power amplifier. In this paper two methods, NDF and pole zero identification methods are presented to detect oscillation and unstable operating conditions in the amplifier. The methods are verified by comparing the simulated unstable operating conditions with that of practical ones observed during measurements. This work is focused on detecting oscillation using these two methods. The work did not study steps 2 and 3 (mentioned in section 2.5.3) for stabilizing the circuit using these methods.

In [8] pole zero identification is used to identify oscillation and stabilize a 4 Watt ultra high frequency (UHF) power amplifier. This paper has shown a way to obtain SISO transfer function data of the amplifier. The data is identified using SCILAB software to extract poles and zeros. An RC network is used to stabilize the circuit. The values of R and C are obtained using a trial and error optimization by looking at the dominant poles of the circuit. The values of R and C that bring the RHP dominant poles to LHP are used to stabilize the circuit. In this paper, finding stabilization node in the circuit and obtaining stabilization component values relies more on practical experience rather than on a systematic approach.

In [20–24] pole zero identification method and STAN software used for identification of poles and zeros are discussed along with their practical issues. In one of these works STAN was used to identify poles and zeors of an LDMOS power amplifier. Unstable loads and input power levels are identified using this method. These works have not utilized the identified poles and zeros to obtain stabilization component values.

In [34] pole zero identification method and its application for the stability analysis of a medium power FET amplifier and a HBT re-configurable amplifier are presented. The FET amplifier was shown to be oscillating at 13.68 MHz in practice. Initially, a stabilization resistor is placed at gate bias and a Monte-Carlo

simulation [34] is run for 300 samples of resistance values. Transfer function data corresponding to each and every case is obtained in a single simulation and the data is then identified with STAN. It is shown that the identified dominant poles corresponding to lower resistance values are in RHP indicating instability. A resistance value that made the unstable dominant RHP poles to move to LHP is selected for stabilization. In the second case (HBT re-configurable amplifier), oscillation is observed at a sub-harmonic frequency in practice. Initially, unstable poles are not identified in simulation for given values of circuit components. Monte-Carlo analysis and STAN identification is performed by varying values of all components in the circuit within their tolerances. Corresponding unstable poles (RHP poles) are then shown to be identified around the oscillation frequency. In this case, instead of adding an additional stabilization resistance, the amplifier design is modified such that the oscillation does not show up even if the circuit component values vary in their tolerances.

In [35] a practical way to obtain transfer function data of an amplifier is presented. The data is then identified using STAN to observe and control amplifier's stability. An additional port in the bias line is used to connect it to vector network analyzer (VNA) in order to obtain measured transfer function data. This approach is limited to very low power amplifiers in practice. The amplifier had shown oscillation at low frequency and its stabilization is achieved by placing an additional RC network in the bias line. The values of RC network are obtained using root locus control techniques.

In [10] a systematic approach to detect oscillation in a high power MMIC power amplifier using pole zero identification method is presented. Two different ways (one using a voltage probe and the other using a current probe) to obtain transfer function data of the circuit, identifying sensitive locations for stabilization and obtaining stabilization component values using root locus control techniques are discussed in this work.

Pole zero identification method has been used successfully for stability analysis of power amplifiers in previous works as mentioned above. Most of these works are focused on detecting oscillations. Later, stability is achieved and stabilization component values are obtained using optimization based on trial and error. The identified poles and zeros of the amplifier are not rigorously used to obtain stabilization location and stabilization component values. Although, [10, 35] mentioned and used a systematic approach to obtain stabilization component values using root locus method, its detailed procedure is not given. Thus it became important at NXP to know and adopt a systematic procedure to further process STAN identified poles and zeros for the purpose of designing stability networks and obtaining their values. This work presents and uses one such procedure in chapter 6.

5. POLE ZERO IDENTIFICATION METHOD THEORY

This chapter is divided into three sections. First section presents a method to obtain closed loop transfer function data of microwave circuits. It also gives a brief introduction to STAN software that is used to extract poles and zeros from the transfer function data. In the second section, practical issues regarding the application of pole zero identification method are discussed. Third section presents templates required to perform small-signal and large-signal stability analysis in a commercial simulator like ADS.

5.1 Microwave Circuit Transfer Function

It is difficult and time consuming to calculate transfer function analytically for varying input parameters of a microwave circuit. Therefore, new simulation method is required to obtain its transfer function. The method should be fast, efficient and reasonable to implement in a general design procedure.

The control system techniques to control the stability of a SISO transfer function are applicable to linear time variant (LTV) systems. Therefore, before obtaining SISO transfer function, the microwave circuit has to be linearized around its large-signal regime to effectively apply control techniques [9]. In a commercial simulator like ADS, both linearization and transfer function data can be obtained simultaneously using a small current probe as shown in Fig. 5.1. The current probe also works as a perturbation and helps to detect oscillation.

The mechanism behind obtaining SISO transfer function of a microwave circuit can be understood from Fig. 5.1. The closed loop transfer function $H_{CL}(s)$ of the system in Fig. 5.1a, which is the ratio of output response (S_o) to its input excitation (S_i) is given by,

$$H_{CL}(S) = \frac{S_o(s)}{S_i(s)} = \frac{A(s)}{1 + A(s)B(s)}. \tag{5.1}$$

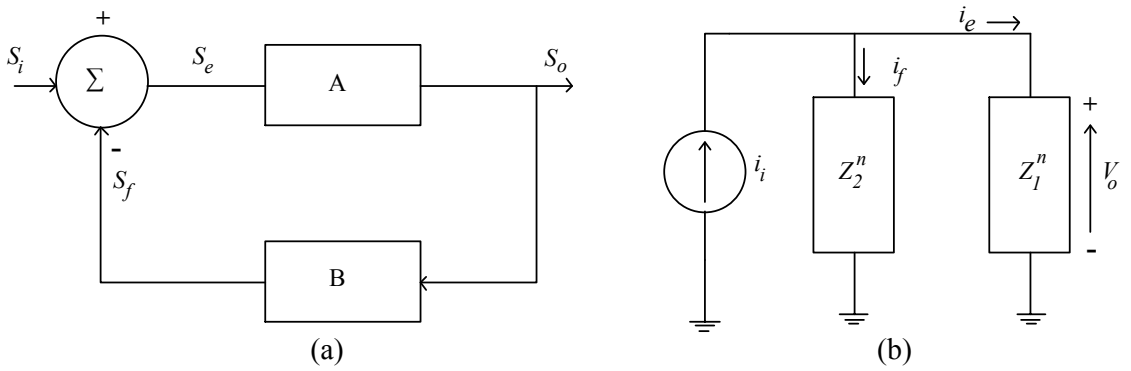

Figure 5.1: (a) Closed loop control system (b) Microwave circuit represented by its impedances and perturbed with a current probe i_i [8] [9].

The microwave circuit represented by its impedances shown in Fig. 5.1b is linearized over a particular steady state using small current probe i_i. This current probe can be connected to any node in the circuit. The closed loop transfer function can be obtained by calculating the impedance over current probe [8] as,

$$H_{CL}^{M}(s) = \frac{output\ response}{input\ excitation} = \frac{V_o}{i_i} = \frac{Z_1^n Z_2^n}{Z_1^n + Z_2^n} = \frac{Z_1^n}{1 + \frac{Z_1^n}{Z_2^n}} = Z_{eq}^n(j\omega). \tag{5.2}$$

Equations (5.1) and (5.2) resemble the same, which is closed loop transfer function. This means, impedance over a small current probe connected to a node in the circuit gives its corresponding closed loop SISO transfer function.

The probe used to obtain transfer function data performs three important tasks at a time. First, it linearizes circuit solution with respect to its amplitude for a certain steady state. Second, it introduces a small perturbation into the circuit. Sustaining of this perturbation leads to conformation of oscillation. Third, it captures the sustained oscillations into the transfer function data.

5.1.1 STAN

Once the transfer function data is obtained, it can be processed using pole zero identification tool STAN to extract poles and zeros of the circuit [22]. These poles and zeros can be plotted on to the s-plane to control and observe stability. Outcome of this process can be expressed as,

$$H_{CL}^{M}(s) \xrightarrow[STAN]{Identification\ process} = \frac{\prod_{i=1}^{N}(s - Z_i)}{\prod_{i=1}^{M}(s - P_i)}. \tag{5.3}$$

In equation (5.3), H_{CL}^{n} represents transfer function data and P_i & Z_i represents STAN identified poles & zeros. These STAN identified poles and zeros can be

imported into matlab to construct transfer function. This helps in designing suitable stabilization network using root locus method [10]. The STAN tool is developed in the IVCAD environment [36] by the University of Basque Country, Bilbao, Spain in collaboration with CNES French space agency and AMCAD Engineering [24] especially for the purpose of stability analysis.

A transfer function order estimation parameter called phase tolerance has to be specified at the beginning of pole zero identification in STAN. When higher order or tight phase tolerance than required is used for identification, over modeling problem occurs [21]. Some extra set of poles and zeros are identified to satisfy the specified phase tolerance criterion. These poles and zeros appear as pole zero cancellations in the s-plane. The pole zero cancellations lying in LHP does not change the stability information. The pole zero pair lying in RHP leads to a wrong conclusion on oscillations. These extra RHP poles appear due to over mathematical modeling [20] with higher order. Such RHP poles have to be further analyzed to avoid ambiguity on oscillations.

When lower order or loose phase tolerance than required is used for identification, under modeling problem occurs [21]. Some poles and zeros might get missed in the identification process due to under modeling of the transfer function data. If the missing poles lie in LHP, then the system stability is not affected. If they lie in RHP then there will be a loss in detecting potential oscillations. To avoid the ambiguity in oscillation detection due to over and under modeling, a systematic work flow presented in appendix A3 is used in this work.

5.2 Practical Considerations

This section presents practical considerations of pole zero identification method for stability analysis. Type of probe, sweep frequency of the probe and selection of probing location in the circuit are discussed.

5.2.1 Current (I) Probe and Voltage (V) Probe - Detection

In pole zero identification method, closed loop transfer function data can be obtained by using either a current probe or a voltage probe. If a current probe is used, it has to be placed in parallel with the node of interest to obtain transfer function data as shown in Fig. 5.2a. In this case, transfer function data is obtained as the impedance over current probe with respect to probe frequency. If a voltage probe is used, then it has to be placed in series with the branch of interest as shown in Fig. 5.2b. In this case, admittance data over voltage probe is the transfer function data.

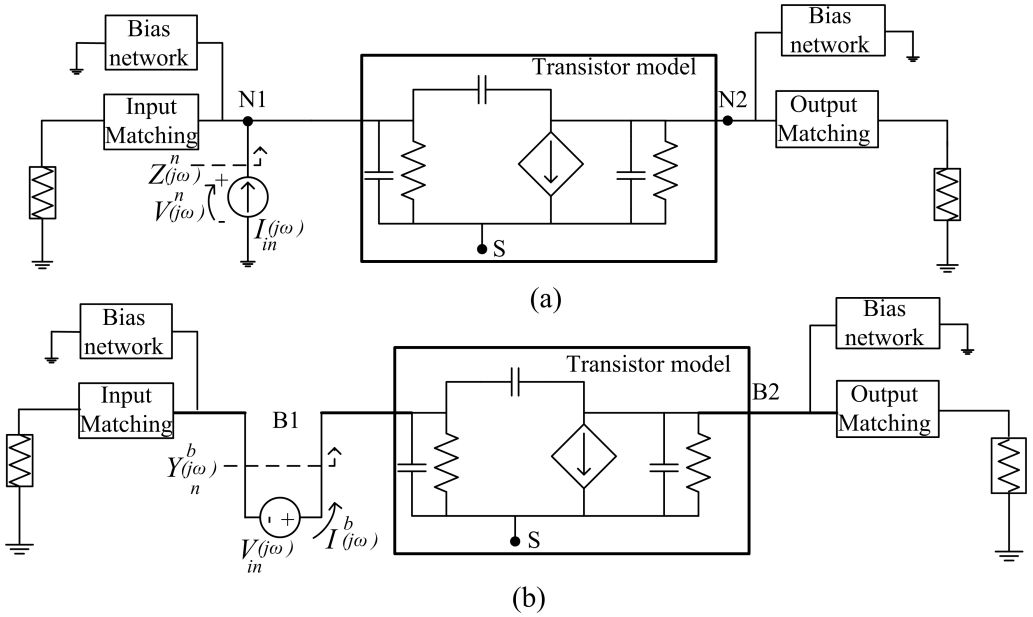

Figure 5.2: (a) Current probe placed in parallel to N1 . (b) Voltage probe placed in series with branch B1 [10].

If a stabilization component for the circuit in Fig. 5.2 is found using the transfer function data obtained from current probe, then it has to be placed in parallel to node N1 [10]. If a stabilization component is found using voltage probe, then it has to be placed in series with branch B1 as shown in Fig. 5.2 [10].

5.2.2 Node or Branch Selection for Stabilization - Location

In the context of stability, any node or branch can be used to obtain transfer function data. This is because, in a circuit (control system), transfer function obtained at any node/branch differ only in its zeros but not in poles [23]. This can be observed in Fig.5.3.

Stability of a system is decided only by its poles in s-plane (as discussed in section 3.3). This means, same stability information can be obtained by probing at different nodes or branches in a circuit. For example let's say in Fig. 5.2a, that a current probe is used at nodes N1 and N2 to obtain transfer function data. After identification of the data, the transfer functions can be represented with same set of poles as,

$$H_{CL}^{N1}(s) = \frac{(s-z_1)(s-z_2)\cdots(s-z_n)}{(s-p_1)(s-p_2)\cdots(s-p_m)}, H_{CL}^{N2}(s) = \frac{(s-z_{a1})(s-z_{a2})\cdots(s-z_{ai})}{(s-p_1)(s-p_2)\cdots(s-p_m)} \tag{5.4}$$

where, $z_1, z_2 \cdots, z_n$ and $z_{a1}, z_{a2} \cdots z_{ai}$ are the zeros obtained at nodes N1 & N2, $p_1, p_2 \cdots p_n$ are the poles obtained at nodes N1 & N2.

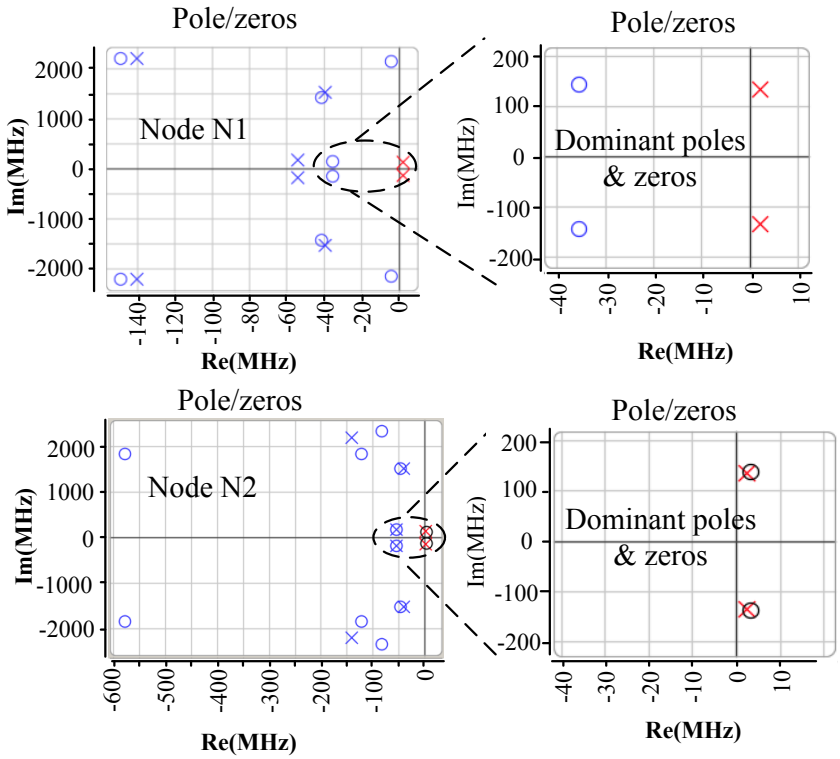

Figure 5.3: Poles zero plot of Fig. 5.2 for nodes N1 & N2 obtained using STAN. The location and number of poles in both cases is same but the location and number of zeros is different.

Even though any node can be used to obtain transfer function data with same stability information, feasibility of stabilizing a circuit from every node is not same. This means, every node in the circuit has same degree of observability of stability but not same degree of controllability [20]. Some nodes are more feasible to implement stabilization network. For example Fig. 5.3 shows dominant poles & zeros of the circuit shown in Fig. 5.2a obtained at nodes N1 & N2. Dominant poles & zeros are the pole zero set that are close to imaginary axis in s-plane. Performance of the system depends mostly on these poles & zeros. It can be observed that in both cases poles are same and are located in RHP indicating instability. The zeros in case of node N1 are in LHP and in case of node N2 are in RHP.

It is possible to stabilize this circuit from node N1 but not from node N2. This is because, according to root locus method, a pole always moves towards its nearest open loop zero following a root locus path [10] when the circuit's loop gain is varied from its minimum to a maximum value. The loop gain in the circuit is varied by varying any component in the circuit or by placing an additional component (for example a resistor). In case of node N1, there is a possibility for the RHP pole to move to LHP when loop gain is varied. The pole can at most move to location of nearest open loop zero. In case of node N2 the zero itself is in the RHP. Therefore, even after the maximum movement of the pole along root locus

path, it still remains in unstable region (RHP). This means node N1 is feasible to stabilize but not node N2. Therefore probing should be done at all nodes to know the feasibility of controlling circuit's stability from different nodes. It also helps to choose a node from the feasible nodes of the circuit that less affects its performance.

5.2.3 Sweep Frequency of the Probe

In general, oscillation due to an input signal frequency may occur at an unknown frequency. This frequency may be far away from input frequency. Therefore, it becomes necessary to know the frequency sweep length of voltage/current probe to capture the oscillation. According to [20], it is enough to sweep the frequency of current probe till half of input frequency to capture all kinds of oscillations due to input signal.

In Fig. 5.4, current or voltage probe with angular frequency ω_s is used to perturb the circuit operating at ω_o. This produces combinations of ω_s and $\omega_o, 2\omega_o \cdots n\omega_o$ at output. The transfer function data which is the impedance data over current probe is calculated at all output frequency components. These transfer functions share same denominator as shown in Fig. 5.4. Since stability depends only on poles (denominator), all the stability information due to ω_o perturbed with ω_s is obtained by calculating transfer function at any of the output frequency components.

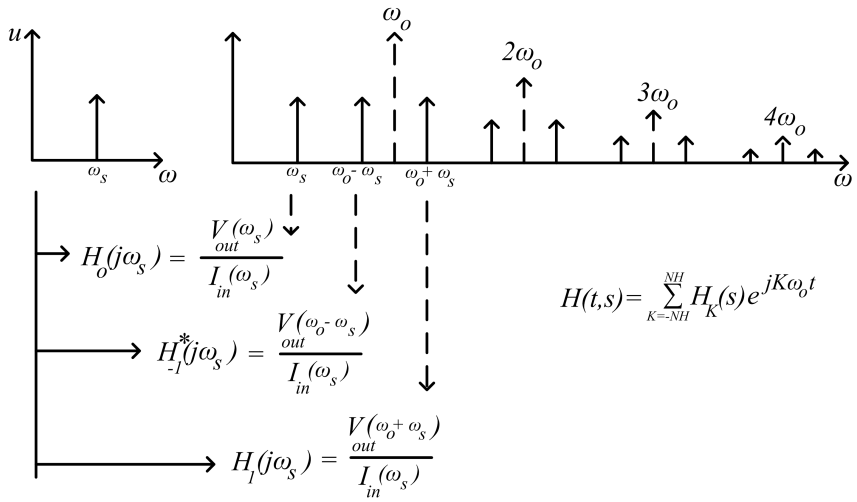

Figure 5.4: Frequency of the probe ω_s mixed with input frequency of the circuit ω_o to provide various frequency components in the output. Phase of the signal at output goes similar transformation. At the end, both amplitude and phase at respective frequencies are used by STAN to identify poles and zeros.

Now, stability due to variation of ω_s need to be considered. To capture all kinds of oscillations we may sweep ω_s from $0 \cdots \omega_o \cdots \omega_m$. The variable ω_m is the highest perturbation frequency of the probe which is considered to cover oscillation frequency due to ω_o. The total transfer function can be obtained by adding the individual

transfer functions due to each ω_s. Since we linearize the circuit with respect to the probe's amplitude (which is small-signal perturbation), the principle of superposition applies.

After the perturbation angular frequency sweep crosses $\omega_s = \frac{\omega_o}{2}$, same stability information is repeated due to periodicity of solution [20] [33]. Hence, to capture all kinds of oscillation due to ω_o, it is enough to sweep the probe or perturbation frequency till half of input frequency ($\frac{\omega_o}{2}$). This is implemented simultaneously along with simulation engine frequency sweep. Suppose, a high power amplifier is operating at 2.3 GHz then, to capture all kinds of oscillations due to 2.3 GHz, it is enough to sweep the probe from DC to 1.15 GHz. This can be done by a single simulation setting in ADS which will be shown in the following section.

5.3 Small-Signal and Large-Signal Stability Analysis

Small-signal stability analysis includes detection of instabilities that arise from DC and small-signal periodic solution. This can be done by obtaining SISO transfer function of the circuit operating in its linear region. The transfer function data can be obtained by using a small perturbation during AC simulation as shown in Fig. 5.5. The AC simulation engine frequency and the probe frequency is swept simultaneously to obtain transfer function data.

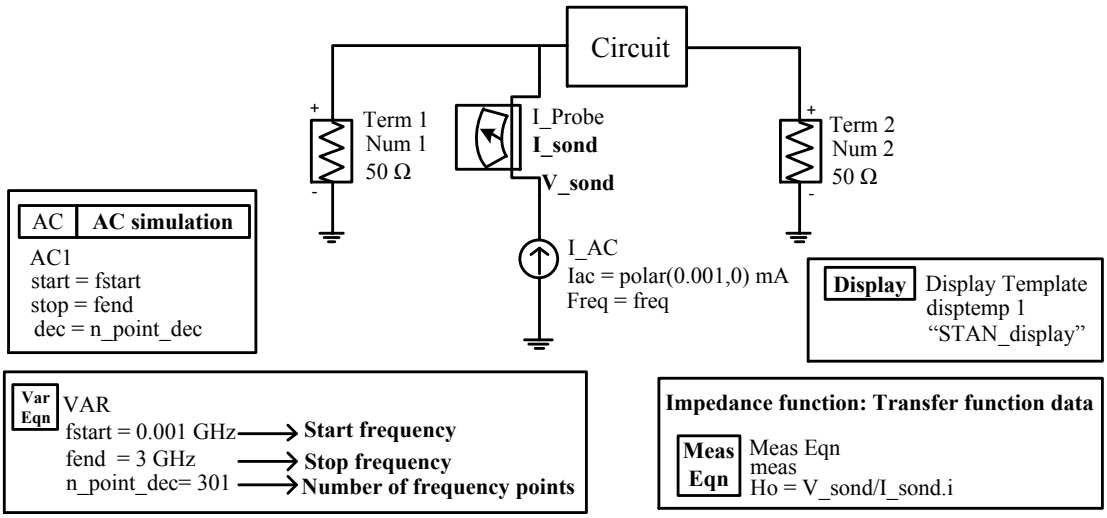

Figure 5.5: Small signal stability analysis template (ADS STAN design kit: AMCAD Engineering) using current probe.

The impedance/admittance data over current/voltage probe with respect to frequency is the transfer function data. The data is then processed through STAN for pole zero identification. The poles and zeros can be used to plot corresponding root locus on the s-plane. By applying control techniques, suitable compensators can be designed to stabilize the circuit.

The instabilities that arise from large-signal periodic solution are analyzed using large-signal stability analysis. In this case, a small perturbation can be introduced into the circuit in a HB simulation as shown in Fig. 5.6. It also helps to linearize the circuit around its large signal regime. The SISO transfer function data can be obtained by calculating the impedance/admittance data over the current/voltage probe. The data is then processed though STAN for pole zero identification and stability analysis.

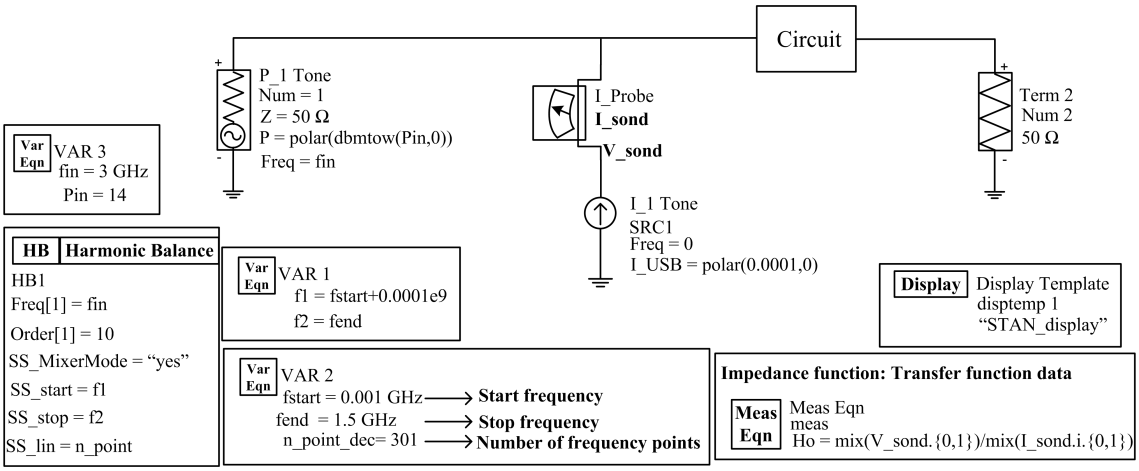

Figure 5.6: Large signal stability analysis template. It is enough to sweep fin from DC to fend/2 to capture all oscillations due to fin.

6. POLE ZERO IDENTIFICATION METHOD APPLICATION

This chapter is divided into three sections. First section shows a systematic approach for stabilization of a push-pull amplifier using pole zero identification method. Small-signal stability analysis is performed on the amplifier and suitable stabilization networks are designed. In the second section, the designed stability networks are verified using conventional μ factor. Effect of stability networks on performance of the amplifier is also discussed in this section. In the third section, large-signal stability analysis of the push-pull amplifier is presented.

The push-pull amplifier is a high power device with a peak power of 60 Watts per transistor. Total peak power of the device is 120 Watts. The transistor is intended to operate in the frequency range from 1.98 GHz to 2.2 GHz. It was designed by Jos van der Zanden (Principal RF Engineer, NXP Semiconductors, Nijmegen) on laterally diffused metal oxide semiconductor, generation 8 (LDMOS GEN 8) technology. During measurements, most of the GEN 8 transistors have shown oscillation at frequencies lower than input frequency.

6.1 Small Signal Stability Analysis

This section demonstrates the essential steps for stabilizing an amplifier using pole zero identification method. The steps include oscillation detection, finding optimum stabilization location in the circuit and obtaining stability network component values.

6.1.1 Oscillation detection

Small-signal stability analysis of the push-pull amplifier is performed by using a voltage probe perturbation as shown in Fig. 6.1. An AC simulation was performed from DC to the highest frequency (3 GHz) where the transistor's model is valid.

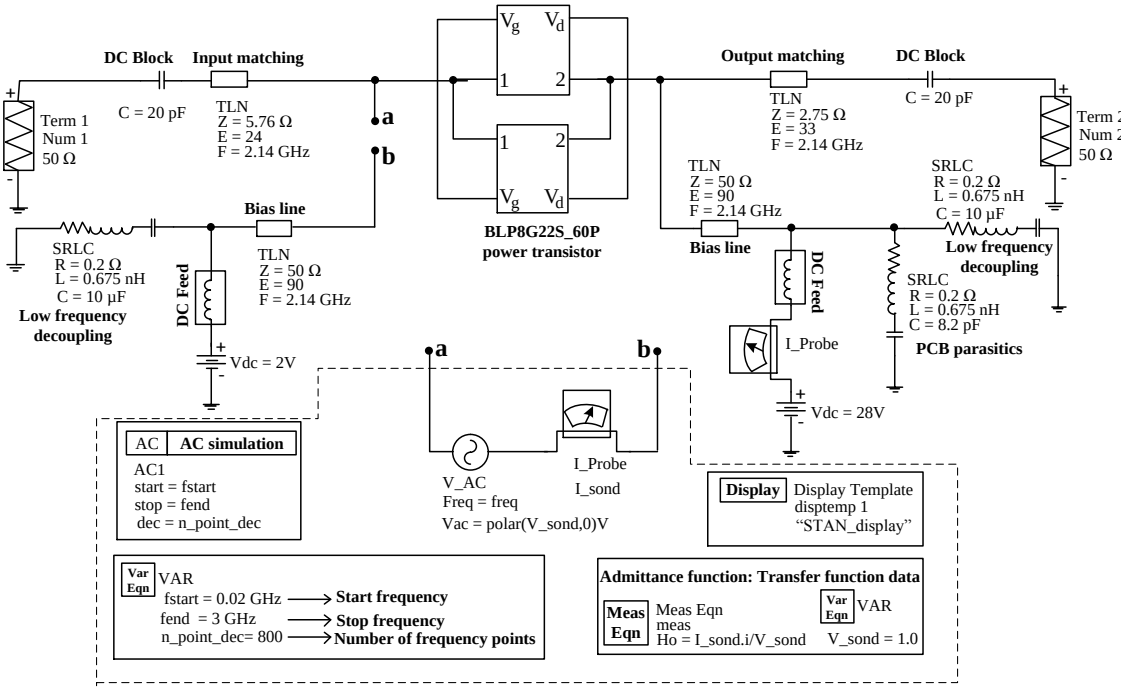

Figure 6.1: Small-signal stability analysis simulation setup of push pull amplifier.

The amplifier's transfer function data is obtained by calculating admittance function over the voltage probe with respect to its frequency as shown in measurement equation of Fig. 6.1. The data is then processed through STAN for identification of poles and zeros. The identified poles and zeros of the push pull amplifier are shown in Fig. 6.2.

RHP poles are identified around 135 MHz indicating instability. The oscillation frequency is around 135 MHz. However, the exact oscillation frequency is equal to the frequency at which the RHP pole crosses the vertical axis (imaginary axis) and will be shown later.

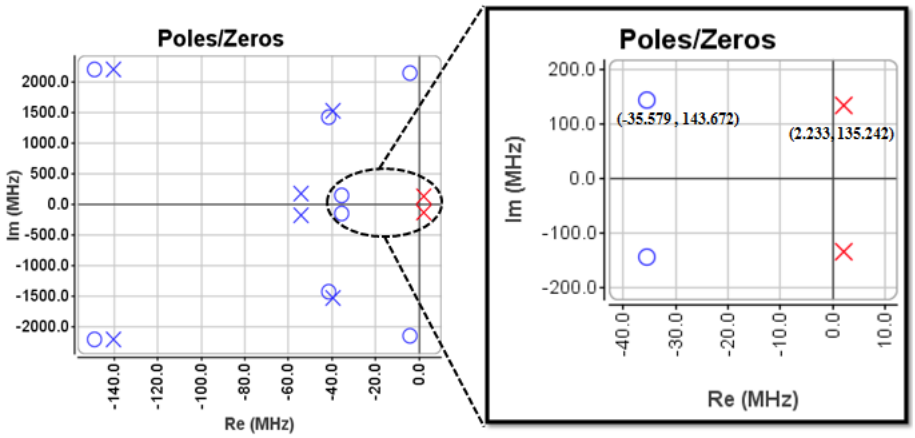

Figure 6.2: STAN identified poles and zeros of the push pull amplifier. RHP poles (red color) indicate instability.

6.1.2 Branch Selection for Stabilization - Location

Once an instability is detected, then, next step is to find a right node/branch in the amplifier circuit to control its stability. To know the most feasible branch for stability control in the circuit, probing is done in all branches at the input side of the circuit as shown in Fig. 6.3. The corresponding transfer function data is then obtained as admittance data over the voltage probe. This data is then processed through STAN for pole zero identification. Stabilization (probing) at output side of the circuit is avoided because, any kind of power dissipation at the output stage is not desirable for a power amplifier.

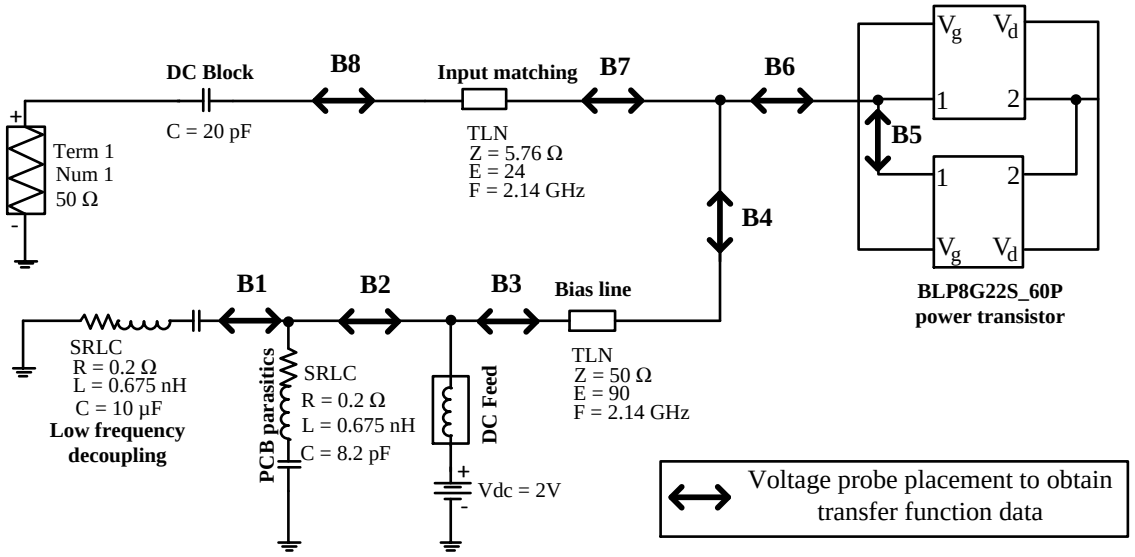

Figure 6.3: Input side of the push-pull amplifier showing branches (B1 to B8) at which the voltage probe is used to obtain closed loop transfer function data.

STAN identified dominant pole zeros corresponding to different branches are shown in Fig. 6.4. It is evident from Fig. 6.4 that the branches B1, B2, B3 & B4 have a greater degree of controllability. Branch B6 has little more degree of freedom to control stability of the circuit. This is because, a pole always moves towards its nearest open loop zero when a circuit's loop gain is varied. Farther the zero is from the pole in stable region (LHP), greater is its degree of controllability. Hence, the stability controllability order of branches in the circuit is, branch B6 $>$ branches B1, B2, B3 & B4 is $>$ B5, B7 & B8 (same set of dominant poles & zeros).

The circuit cannot be stabilized from branches B5, B7 & B8 . This is because, for any value of change in amplifier's loop gain, the RHP pole in these cases can at most move towards nearest open loop zero, which is also in RHP. The pole remains in RHP even after maximum change in loop gain. Hence, it is impossible to stabilize the circuit from these branches.

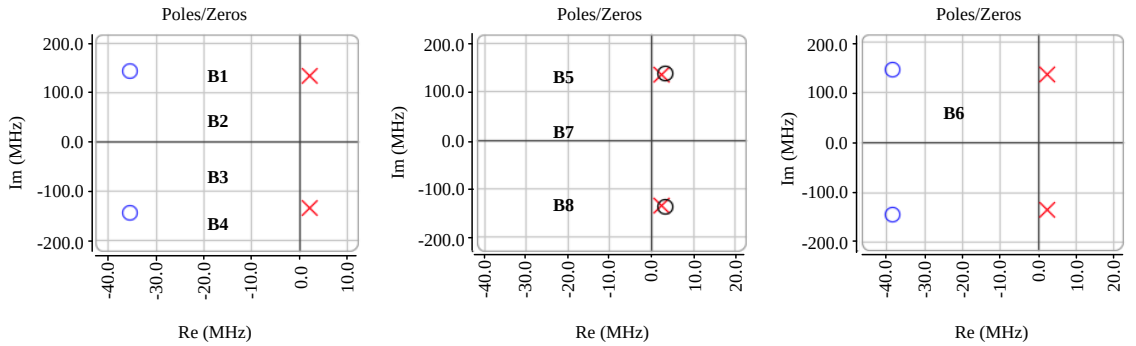

Figure 6.4: Dominant pole zero plots obtained by probing the push pull amplifier in the branches B1,$\cdots$, B8. Blue crosses indicate stable poles and red crosses indicate unstable poles.

Once feasible branches for stabilization are identified, then a branch that less affects amplifier's performance has to be selected. A stabilization component (resistor) at branch B6 would cost amplifier's power gain. Hence, this branch should be avoided for stabilization. Any of the branches B1, B2, B3 & B4 can be used for stabilization. This is because, they have a same degree of controllability and at the same time will have a less affect on amplifier's performance due to their location in bias branch. Since the bias line in this amplifier is designed to be a quarter wave transformer, a stability network placed after this line would have a less impact on amplifier's performance at operating frequency.

6.1.3 Stabilization using Root Locus Method

Once an optimum branch for stabilization is selected, the corresponding poles and zeros obtained from this branch can be further processed to design a stability network and calculate its component values [35]. STAN identified poles and zeros of the selected branch can be exported as an excel file. This excel file can be imported into MATLAB to plot a corresponding root locus of the amplifier. The code that has to be executed to plot root locus in matlab is given in appendix A.

It is important to note that a factor called normalization factor which is common to both numerator and denominator of the transfer function is not shown during STAN identification. This causes inaccurate estimation of amplifier's closed loop gain and thus the stabilization component value, when a transfer function is constructed from STAN identified poles and zeros. This can be corrected by estimating and including the normalization factor in matlab during transfer function construction. It is estimated by comparing admittance function magnitude plot in STAN window and its corresponding uncorrected bode magnitude plot in matlab. The procedure is shown in appendix A.

Corrected root locus and the dominant pole zero combination of the push-pull amplifier is shown in Fig. 6.5. It is observed that the unstable pole (RHP) moves

to stable region (LHP) along the root locus path for increasing values of loop gain. This loop gain value shown by matlab is equivalent to the stabilization component value [10]. The frequency of oscillation is the frequency at which the pole crosses imaginary axis of s-plane.

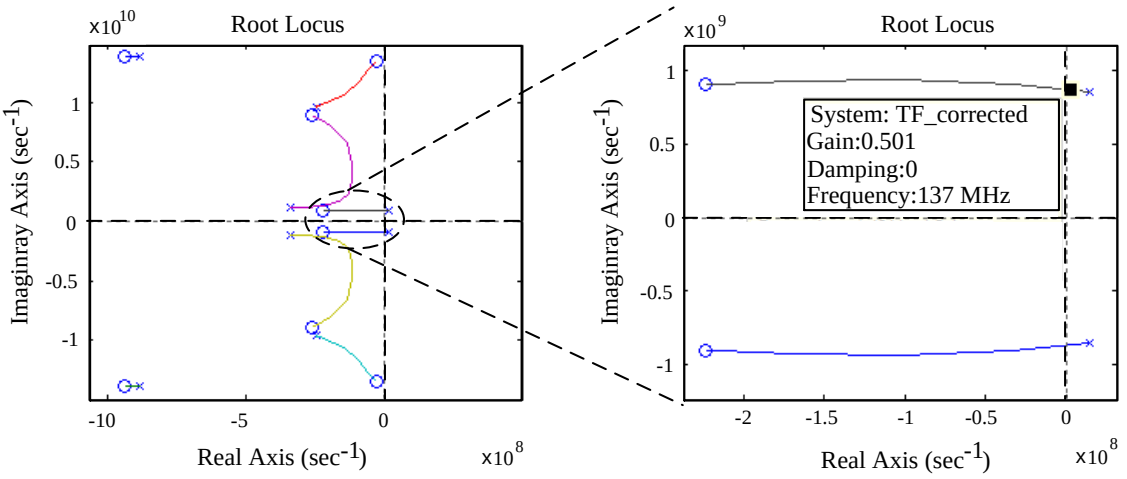

Figure 6.5: Root locus of the push-pull power amplifier circuit plotted in matlab. RHP pole crosses imaginary axis at 137 MHz (oscillation frequency) at a closed loop gain value of 0.5.

The RHP pole crossed imaginary axis and moved to LHP at a closed loop gain value of 0.5. This means, the amplifier will be stable for a closed loop gain value greater than 0.5. Therefore stability can be achieved by placing a 0.5 Ω or more value resistor in branch B3 of Fig. 6.3. To conform this, a resistor is placed in branch B3 and is swept from 0.1 to 50 Ω.

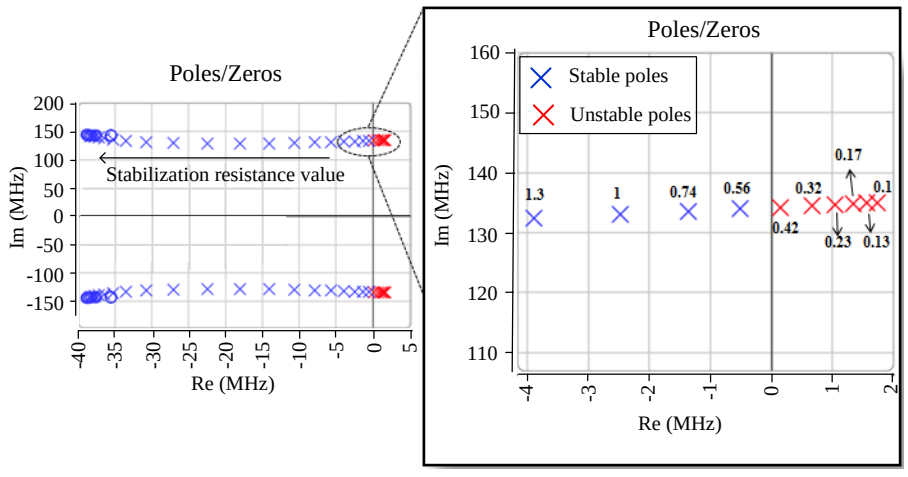

Figure 6.6: Dominant poles obtained by sweeping a stabilization resistor placed at branch B3 from 0.1 to 50 Ω. The pole crosses imaginary axis for 0.5 Ω. This is in agreement with the prediction by root locus method.

The SISO transfer functions of the amplifier for all resistance values is then calculated in a single simulation. The obtained data is then identified using STAN

for corresponding poles and zeros. The movement of the identified RHP pole for increasing resistance values exactly followed the root locus path as shown in Fig. 6.6.

6.1.4 Stabilizaton using Lag-Lead Compensator

Stability of an amplifier often can be achieved using frequency selective stabilization networks [13]. It is observed that gain of the transistor used in the push pull amplifier design is very high ($>$ 30 dB) around low frequencies (137 MHz). This high gain of the transistor contributes to achieve sufficient loop gain in the amplifier to form oscillation. It can be avoided by lagging the gain at oscillation frequency using a frequency selective network called lag compensator [6]. At the same time, any loss of gain in the operating frequency range can be compensated by using a frequency selective lead compensator [6]. Therefore, a combination of lag and lead network called lag-lead compensator (see appendix A2) is designed to stabilize and compensate for loss in performance of the push-pull amplifier.

The task of designing a lag-lead compensator (any compensator) can be made easy with the help of matlab SISO tool [37]. Input to SISO tool is the transfer function of the amplifier. The SISO tool, when invoked, simultaneously opens a root locus plot window and a compensator editor window. Different kinds of compensators can be designed using compensator editor and the resultant plots (root locus, bode, pole zero, Nyquist, step response & impulse response) can be viewed by analysis plots option in the compensator editor window. A graphical tuning option is available to tune the closed loop gain and compensator pole zero location for desired performance. An automated tuning option that use pre-programmed algorithms to achieve specified performance is also available.

Design of a lag-lead compensator using SISO tool is shown in Fig. 6.7. A lag compensator pole zero pair is placed at 137 MHz (8.6×10^8 *rad/sec*) (Fig. 6.7a) and a lead compensation pole zero pair is placed at 2 GHz (1.256×10^{10} *rad/sec*)(Fig. 6.7b). It is important to make sure that the closed loop unstable pole (RHP pole) has moved to stable region (LHP) after compensator placement. This can be viewed from the associated root locus editor window of SISO tool. The corresponding transfer function of the compensator is shown in compensator editor window (Fig. 6.7a & b). This transfer function is then compared with theoretical transfer function of a lag-lead compensator to calculate its component values as shown in Fig. 6.7. While solving for component values, one of the component values has to be chosen ($R_1 = 10\Omega$) to calculate others.

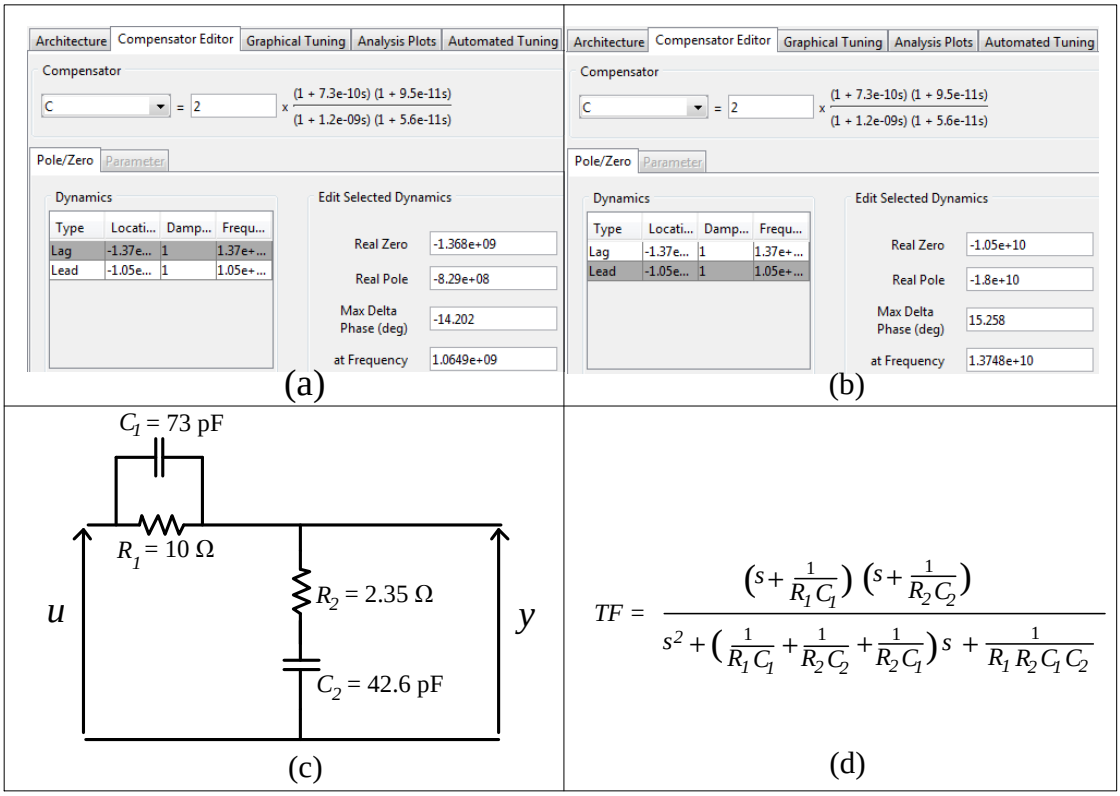

Figure 6.7: (a) Lag compensator pole zero pair placed around 137 MHz (oscillation frequency). (b) Lead compensator pole zero pair placed around 2 GHz (operating frequency). (c) Lag-lead compensator network with component values and (d) Theoretical transfer function of the lag-lead compensator.

Final position of amplifier's closed loop poles after compensation can be observed in the root locus plot associated with the SISO tool. Pole zero plot of the lag-lead compensator, its corresponding magnitude and phase plots are shown in Fig. 6.8 and 6.9.

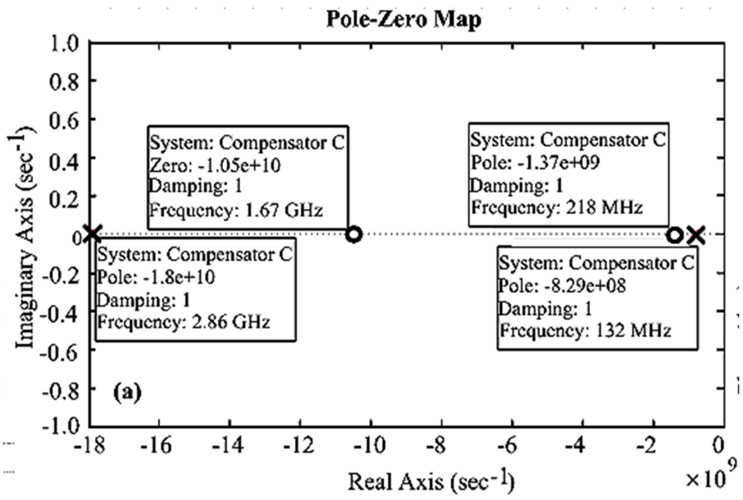

Figure 6.8: Pole zero plot of the lag-lead compensator.

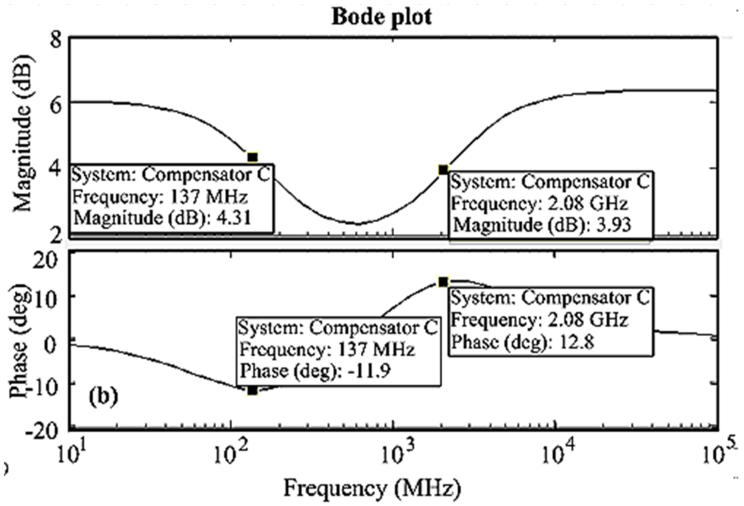

Figure 6.9: Magnitude and phase plot of the compensator. The phase lag at 137 MHz and the phase lead at 2.08 GHz can be observed.

The compensator shown in Fig. 6.7(c) is placed in series with gate bias branch (branch B3 in Fig. 6.3) and the amplifier's transfer function data is obtained using voltage probe. The data is then processed through STAN for identification. The identified poles and zeros of the amplifier after compensation are shown in Fig. 6.10. It can be observed that the amplifier's dominant closed loop poles has moved to LHP after lag-lead compensation indicating stability.

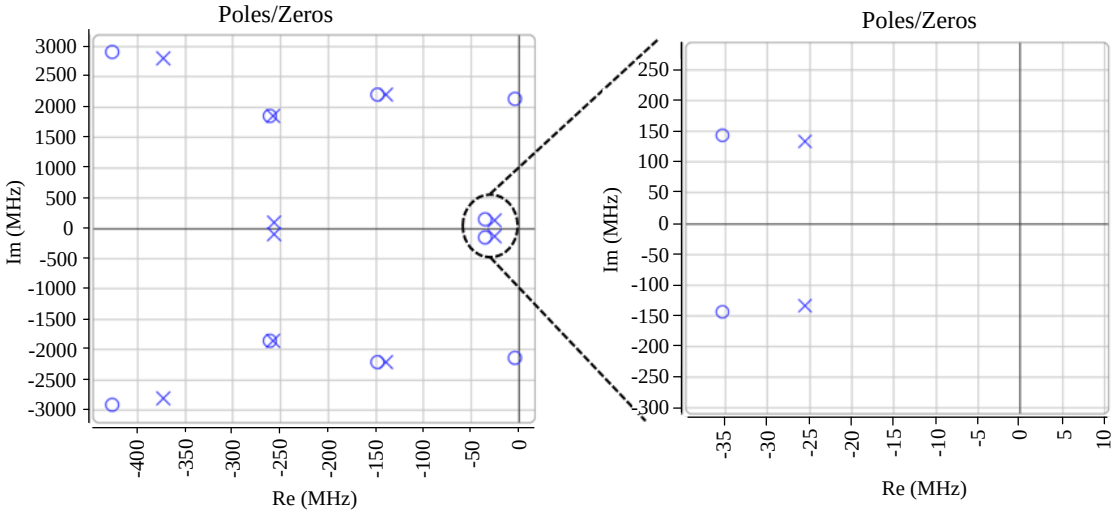

Figure 6.10: STAN identified poles and zeros of the push pull circuit after lag lead compensation.

6.2 μ factor and gain comparison

This section is divided into two sub-sections. In the first sub-section, μ factor of the push pull amplifier with and without stabilization is compared. In the second section, maximum stable gain and power gain of the amplifier with and without stabilization networks are compared.

6.2.1 Stability Factor

Stability factor (μ) of the amplifier for no stabilization, resistive stabilization and stabilization with lag-lead compensation is shown in Fig. 6.11. For an amplifier to be unconditionally stable, the μ should be greater than one at all frequencies. Failing of this at any of the frequencies results in an potentially unstable amplifier. It can be observed in Fig. 6.11 that with stability networks, the μ factor is improved (> 1) around the oscillation frequency (low frequencies) indicating unconditional stability.

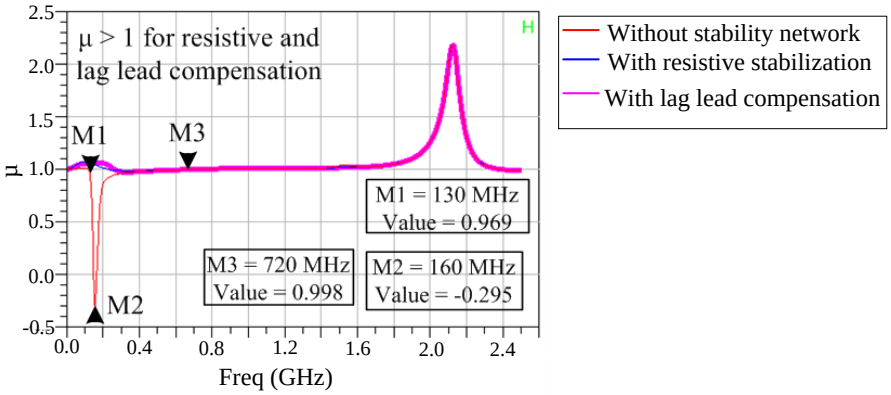

Figure 6.11: Stability factor of the push pull amplifier with no stabilization, resistive stabilization and lag lead compensation.

Clearly this shows that the stabilization network obtained using pole zero identification method is in agreement with small-signal stability factor μ. This serves as a validation of STAN tool and pole zero identification method for stability analysis, which was already proved in previous works presented in Chapter 4. The pole zero stability analysis here is shown for a single load. The analysis is repeated for multiple loads in Smith chart after stabilization and is found that the amplifier is stable for all loads inside Smith chart. The μ factor in Fig. 6.11 shows the same.

The advantage of using STAN for small-signal stability analysis is that it can detect oscillations in circuits with multi-active devices and multi-ports [38] where μ factor is not applicable [15]. The same analysis shown in this section can be used to identify instabilities in such circuits. For example, it is now possible with STAN to perform stability analysis of a mixer [15].

6.2.2 Maximum Stable Gain and Power Gain

Simulations of the push pull amplifier are performed to compare its power gain and maximum stable gain with and without stabilization networks. Maximum stable gain is the maximum gain that can be achieved from an amplifier after it is stabilized [13]. The effect of the stability networks on performance can be studied by looking at gain of the amplifier. If the amplifier's gain is unchanged in the operating frequency

region before and after stabilization, then it means that the stability network is not affecting amplifier's performance.

It can be observed from Fig. 6.12 that the device has very high gain at low frequencies. The oscillations are observed in this high gain region. The resistive stabilization and the lag-lead compensation could sufficiently damp the oscillations at low frequencies there by making the circuit stable for small signal operation.

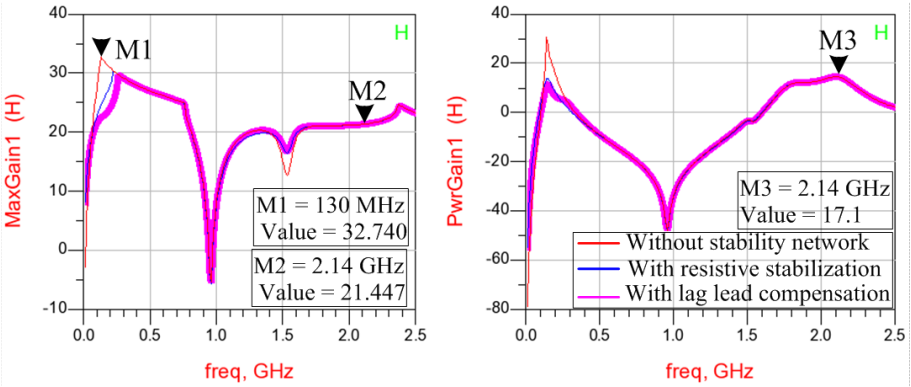

Figure 6.12: Maximum stable gain (dB) and power gain (dB) of the push pull amplifier. Gain at low frequencies is damped by resistive stabilization and lag lead compensation.

Gain of the amplifier in operating band (1.98 to 2.2 GHz) in all cases is unchanged (Fig. 6.12). This is due to the placement of stability network in bias branch (Branch B3 of Fig. 6.3). The bias line is designed to be a quarter wave transformer [39]. Since the stability network is placed after this transformer, it is not functional at RF frequency (operating frequency) and thus does not lead to additional losses in the amplifier circuit.

In practice, non functionality of the stabilization network in the operating frequency is dependent on RF grounding used to terminate the quarter wave transformer at one end. If the RF grounding is not perfect, then the quarter wave transformer deviates from its ideal behavior. This introduces additional losses thus affecting the power amplifier's performance in power, gain and efficiency.

6.3 Large Signal Stability Analysis

This section is divided into three sub-sections. In the first sub-section, large-signal stability analysis is performed to identify input power levels that lead to oscillation. In the second sub-section, the designed resistive and lag-lead compensator stability networks are used to stabilize the amplifier for large-signal operation. In the third sub-section, large-signal analysis is repeated for other frequencies in the operating band to ensure stability of the amplifier.

6.3.1 Oscillation Detection

Large signal stability analysis is performed using the template shown in Fig. 6.13. A voltage probe is placed in the same bias branch (B3 of Fig. 6.3) to obtain transfer function data during HB simulation. The data is obtained by sweeping input power of the amplifier at center frequency (2.14 GHz). It is then processed through STAN for pole zero identification. The obtained poles and zeros are then checked to find unstable RHP poles. Initially, the analysis is performed without placing any stability network.

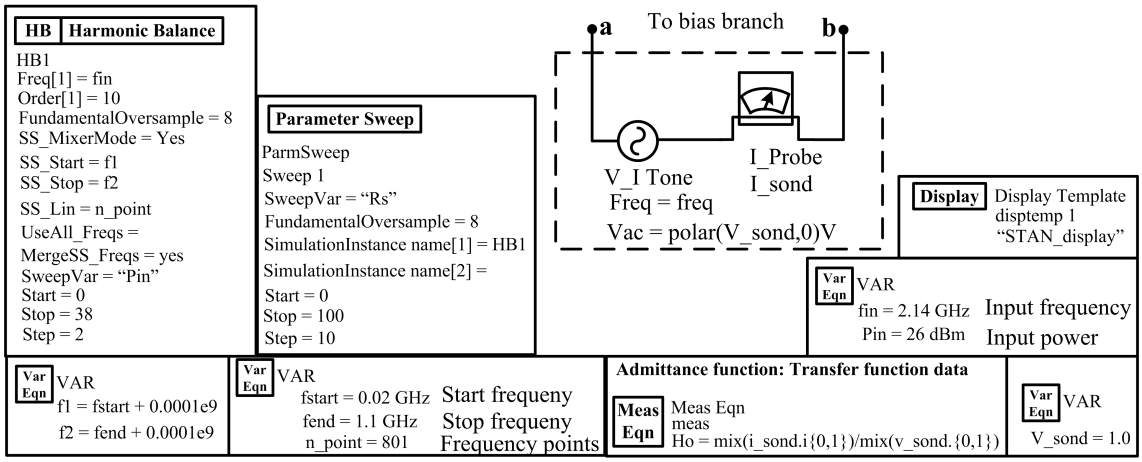

Figure 6.13: Simulation setting for large signal stability analysis. Parametric metric sweep can be used to sweep parameter of interest. Power sweep is implemented in the HB engine itself.

The frequency of the voltage probe is swept from 20 MHz to 1.15 GHz. As said earlier, it is enough to sweep the frequency of the voltage probe from DC to half of the input frequency (2.14 GHz). It can capture all kinds of oscillations due to the input frequency and also saves simulation time. The identified poles and zeros of the push pull amplifier for large-signal operation is shown in Fig. 6.14.

Unstable poles are identified for input power levels from 0 to 10 dBm. Some of the unstable poles appear as pole zero cancellations in RHP. They can be either physical pole zero cancellations [23] which lead to real case oscillations or can be due to mathematical over modeling [23] around those frequencies and power levels which lead to wrong conclusion on oscillations. To avoid ambiguity, re-identification is performed by narrowing the frequency band of identification around 137 MHz. The pole zero cancellations disappeared indicating mathematical overmodeling. It means that they are not real pole zero cancellations and can be discarded for stability analysis [21], hence, they are not shown in Fig. 6.14.

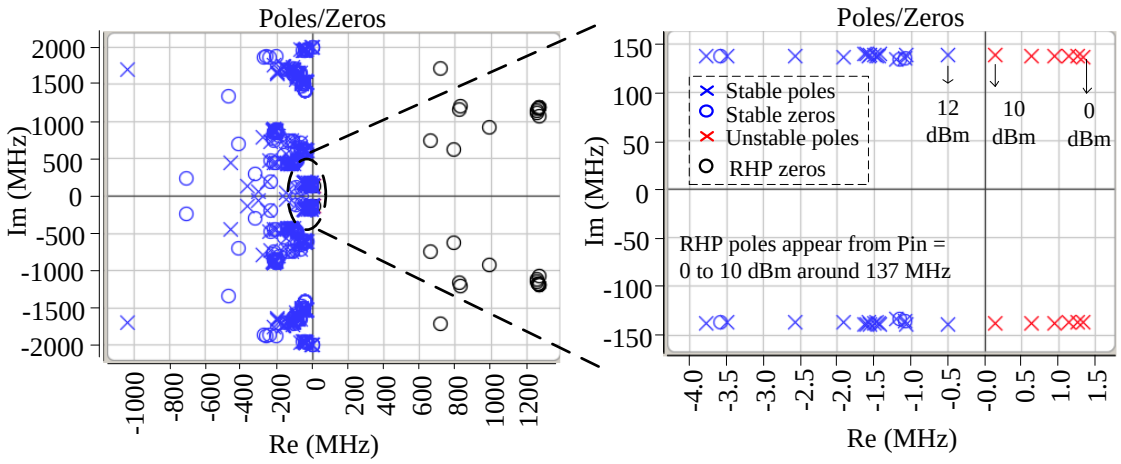

Figure 6.14: STAN identified poles and zeros of the push pull amplifier for an input frequency of 2.14 GHz and input power range of 0 to 38 dBm.

The instability shown in Fig. 6.14 is observed practically while performing load pull measurements of the transistor used in the push-pull amplifier design. The oscillation frequency observed in practice (96 MHz) is lower than the prediction by STAN analysis (137 MHz). This is because, the circuit used in load pull measurements is different from the amplifier circuit used for STAN analysis.

6.3.2 Resistive and Lag-Lead Stabilization

Stabilization components obtained in small-signal analysis are checked to see their validity for large-signal case. A resistance of 10 Ω and the lag-lead compensator designed for small-signal case are placed in the bias branch (B3) one at a time. The large signal analysis is repeated by sweeping the power levels for an input frequency of 2.14 GHz. Corresponding pole zero identifications for resistive and lag-lead compensation cases are shown in Fig. 6.15.

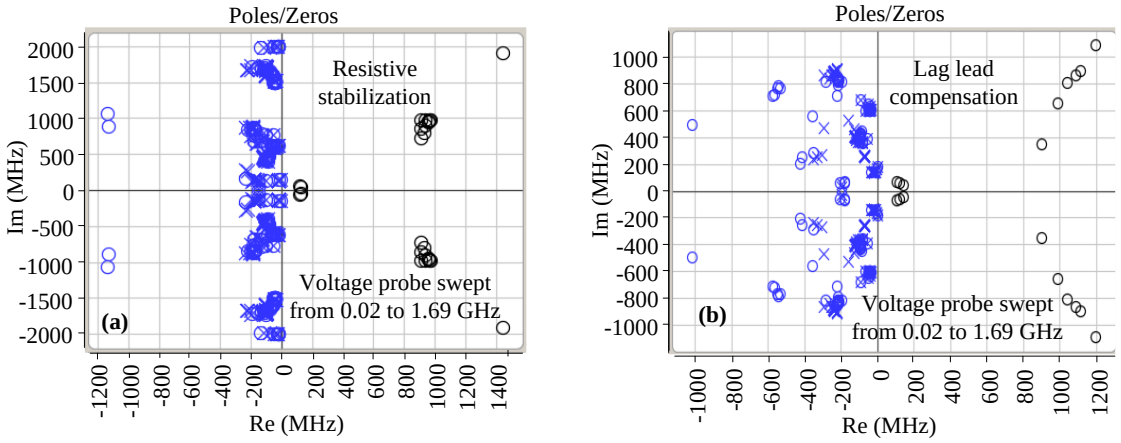

Figure 6.15: (a) STAN identified poles and zeros of push pull amplifier for an input frequency of 2.14 GHz and input power level range of 0 to 38 dBm with resistive stabilization and (b) with lag lead compensation.

Voltage probe is used and its frequency is swept from 20 MHz to 1.69 GHz to capture all oscillations due to 2.14 GHz. The plot (Fig. 6.15) indicates stable poles for all power levels. This means the designed stability networks can sufficiently suppress the oscillation due to large-signal operation. This is true for this amplifier. Suppose, if the circuit is still not stable, then a suitable stabilization component can be found by sweeping the stabilization component's value and looking at the corresponding RHP poles. The component values for which the RHP poles move to LHP should be considered for stabilization. If the circuit is not stable for any value of the stabilization component value, then the node or branch of stabilization has to be changed to next feasible node to repeat the analysis.

6.3.3 Large Signal Stability over Frequency

The designed stability networks for the push pull amplifier are able to suppress the oscillation due to large-signal operation at input signal frequency (2.14 GHz). They are able to suppress the oscillation at all frequencies for small-signal operation. The large-signal stability also has to be checked at frequencies in and little out of the operating band (1.84 to 2.2 GHz) to guarantee stable operation. Therefore the large-signal stability analysis is repeated for frequencies from 1.84 to 2.2 GHz. Fig. 6.16 shows pole zero identifications of the push-pull amplifier with lag-lead compensation in the frequency band 1.84 to 2.2 GHz.

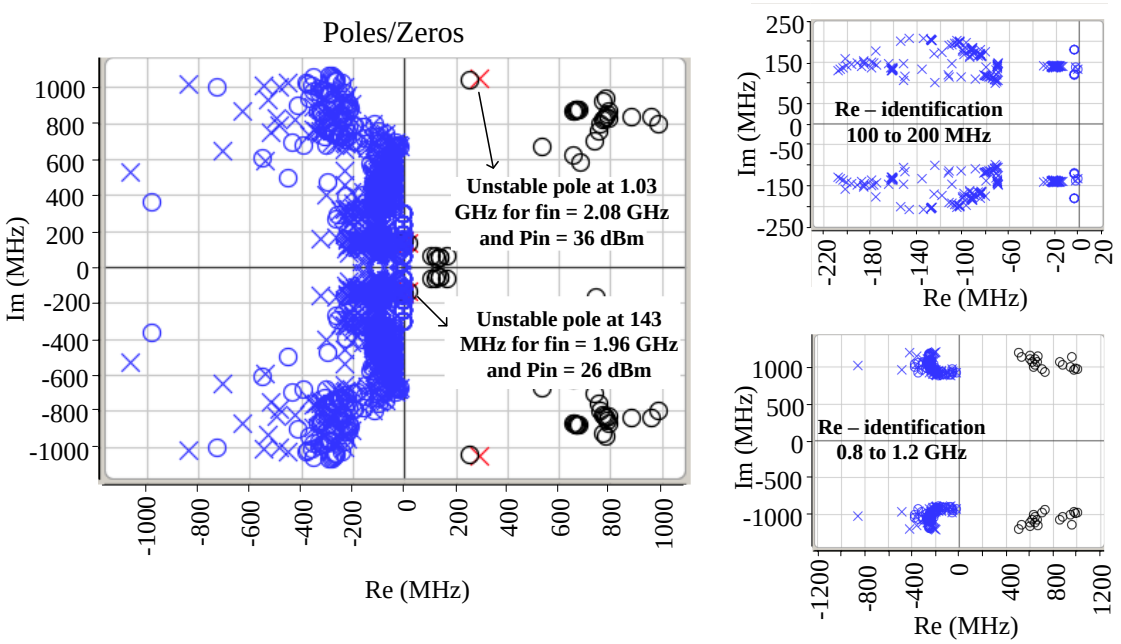

Figure 6.16: (a) Pole zero identification of the push pull amplifier with lag-lead compensation in the frequency range 1.84 to 2.2 GHz and in input power range 0 to 38 dBm. (b) Re-identification in the frequency band 100 to 200 MHz. (c) Re-identification in the frequency band 0.8 to 1.2 GHz.

Unstable poles are identified at 143 MHz for an input frequency of 1.96 GHz and input power level of 26 dBm and at 1.03 GHz for an input frequency of 2.08 GHz and input power level of 36 dBm indicating stability problem. A re-identification (Fig. 6.16 b & c) is carried around the frequency of unstable poles to conform oscillations. The re-identification shows that the identified unstable poles are due to mathematical over modeling and are not real pole zero cancellations. The same analysis has been repeated for lag-lead compensator and the circuit is found to be stable. The analysis is then repeated including out of band frequencies from 1 to 3 GHz and is found that the circuit is stable for all the frequencies for resistive and lag-lead stabilization networks.

With lag-lead compensation the large-signal analysis is repeated by sweeping the loads in the $|\Gamma| = 0.5$ circle [40] and the frequencies from 1.84 to 2.2 GHz. The transfer function corresponding to all the loads and frequencies is obtained and identified at a time using the large-signal template and STAN tool. The STAN tool is capable of performing large number of identifications with great speed. The identification results showed that the circuit is stable (no RHP poles) for all these loads and frequencies.

Oscillations at low frequency are observed in practice for some of NXP's LDMOS GEN8 transistors during load pull measurements. These are similar to the case reported in [35]. A frequency selective RC stabilization network (lag-lead compensator) is used to suppress these oscillations [35]. Large-signal stability analysis also showed that the lag-lead stabilization network is effective in suppressing low frequency oscillation. Hence a lag-lead type stability network is proposed to implement in the bias branch of a practical class AB microwave power amplifier design (using NXP's transistor) to suppress its oscillation. Design of the class AB amplifier, its oscillation problem and its suppression are shown in Chapter 7.

7. DESIGN AND STABILIZATION OF CLASS AB AMPLIFIER

The proposed lag-lead compensation type stability network is used to stabilize a high power class AB amplifier. The amplifier is made of NXP's high power transistor in an overmolded plastic (OMP) package [41]. The package inside has two transistor designs (on dies) connected in parallel with cross bonds. The design is targeted to give an output power of 140 Watts in the frequency range 2.32 to 2.37 GHz. The die thickness used for this transistor design is actually intended for a 2 GHz transistor design. This transistor design is an experiment by Albert van Zuijlen (Principal RF Engineer, NXP Semiconductors) to know the effect of die thickness on its performance, when used out of its normal operating range.

Since this transistor is in development stage, good linear and nonlinear models are not readily available. Therefore, design of the amplifier with this transistor is purely based on its measured load pull data. This is good in terms of amplifier design but not in terms of stability analysis. This is because, large-signal stability analysis using pole zero identification method depends on nonlinear model of the transistor. This chapter presents and discusses design and stabilization of a 2.32-2.37 GHz class AB power amplifier made of NXP's experimental transistor.

7.1 Class AB power amplifier design

This section presents design of input and output matching networks of the class AB amplifier. Layout and printed circuit board (PCB) of the amplifier along with purpose of the components used in the circuit is also given.

7.1.1 Input Matching Network

Input matching network is designed using measured large-signal source impedances during load pull measurements (see Appendix A1). The measurements are performed for the frequencies 2.23, 2.3, 2.4 and 2.5 GHz. Due to non-availability of source and load tuner calibration file [42] for in-band frequencies (2.32 to 2.37 GHz), measurements are not performed exactly at these frequencies. But, the impedances at 2.3 and 2.4 GHz are enough to design the input matching network.

The measured large-signal source impedances are loaded into a one port data

item in ADS. A conjugate match is then realized by looking into a 50Ω port in the frequency range from 2.32 to 2.37 GHz with center frequency 2.345 GHz as shown in Fig 7.1. The final input matching tuned with bias lines is shown in appendix A4.

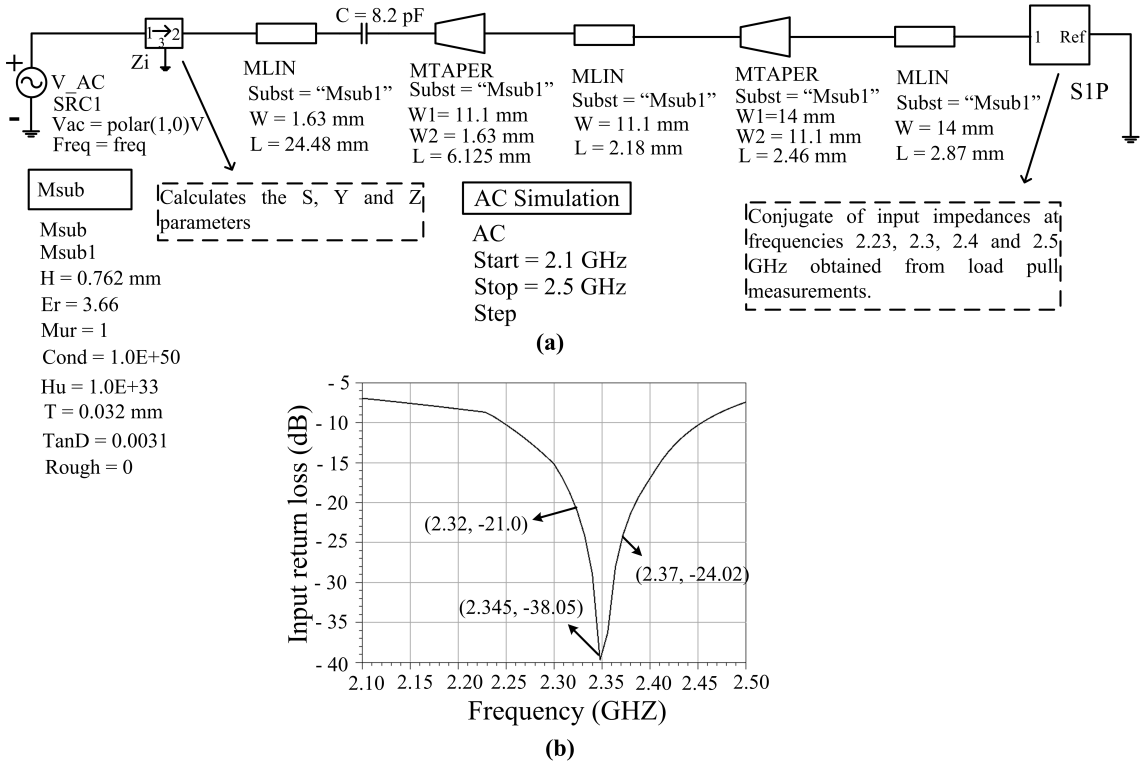

Figure 7.1: (a) Input matching network with conjugate match to large signal source impedances of the transistor in the frequency range from 2.32 to 2.37 GHz. (b) Input return loss.

It is to be noted that this is not a simultaneous conjugate match. When the output matching network is realized, the input matching may change. But this is not true for this case, since the change of input impedance due to change in load termination has been considered in the load pull measurements itself.

7.1.2 Output Matching Network

The output matching network design is purely based on measured load pull data. CAD design tool ADS 2011 [43] has a data based load pull (DBLP)template that gives feasibility to realize output matching network using transistor's load pull data.

The measured load pull data of the transistor is stored in a s2p file. This file is then loaded into the DBLP template. The template consists of two ports, one port acts as transistor's output impedance where the load pulled file is loaded. The other port is the load impedance to which the matching is realized. Matching network is realized in between these ports. The template has the capability to interpolate optimum load impedance and performance parameters for frequencies other than

measured frequencies for a given load. An associated data display page shows measured performance parameters (interpolated maximum power and efficiency for in band frequencies) of the transistor.

A matching network is realized to a 50Ω load to meet an output power of 140 W as shown in Fig. 7.2. It is tuned such that the matched load impedance of the transistor is on the measured load line (in between peak power and efficiency) as shown in Fig. 7.2b. The final output matching network tuned with bias lines is shown in appendix A5.

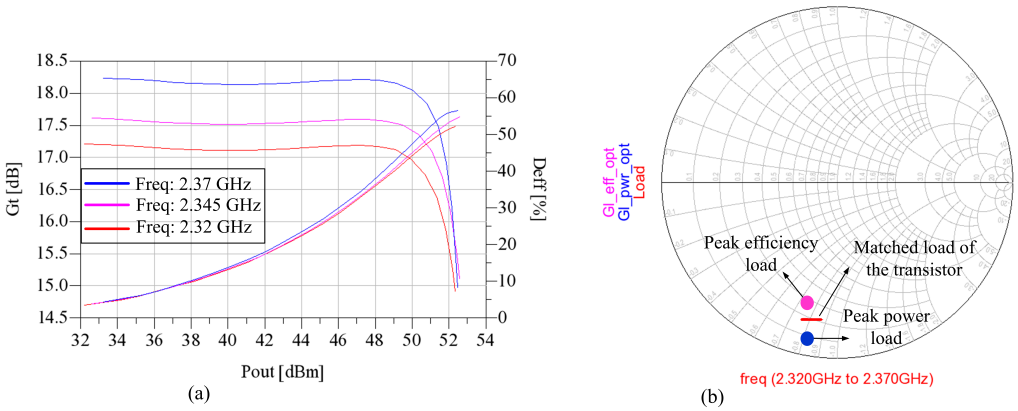

Figure 7.2: (a) Efficiency and gain of the class AB amplifier with respect to output power with ideal output matching (matching without considering losses). (b) Smith chart showing impedances of the transistor for peak power (blue) and peak efficiency (pink). The red line shows optimum output impedance of the transistor to which the matching is realized.

The output power at which the gain of the amplifier drops to 3dB from its linear gain is called 3dB compression. The power gain and efficiency of the amplifier at 3 dB compression point are given in Table 7.1

Table 7.1: Power, efficiency and gain of the class AB amplifier at 3 dB compression point.

Frequency (GHz)	Output power (dBm)	Efficiency (%)	Gain (dB)
2.32	51.51	48.84	16.13
2.345	51.72	51.20	16.41
2.37	51.63	53.90	17.18

7.1.3 Layout and PCB

The realized input and output matching networks are separately milled on Rogers Ro4350B (30 mil) PCB. The PCB has three layers, a top conductive copper layer, substrate layer in the middle and a bottom copper layer for ground. Components are connected to ground through vias from top layer to ground plane.

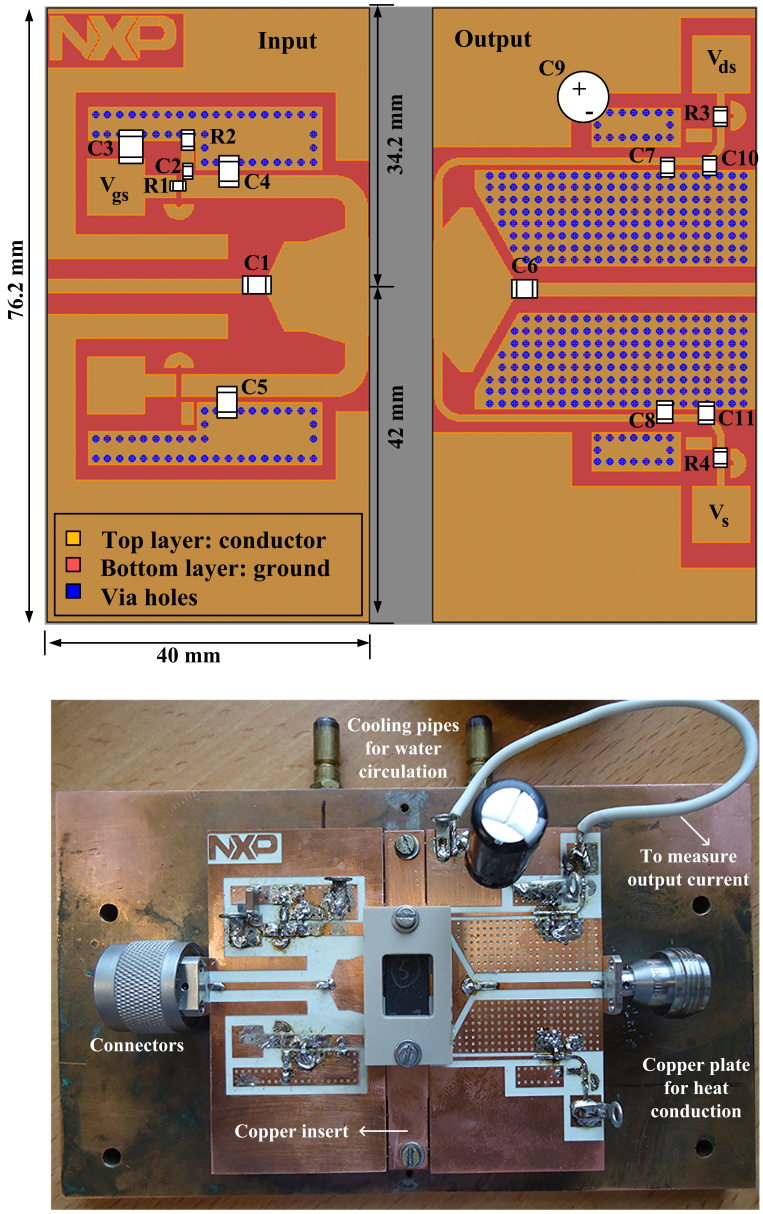

Figure 7.3: Layout and PCB of the 2.32-2.37 GHz class AB amplifier.

The PCBs are mounted on base plates made of brass. An insert made of pure copper (good thermal conductor) is placed beneath the transistor. The input, output base plates and the insert are held together using screws. The insert is used to conduct heat from the transistor to a bottom copper plate shown in Fig. 7.3. This copper base plate has two holes in it to allow water circulation for cooling purpose. Final layout and PCB of the class AB amplifier are shown in Fig. 7.3.

The layout design and construction is done by the author. The layout milling on PCB and mounting it on base plates is done by Wilfred Schmidt (RF technician, NXP).

Table 7.2: Definition of the components used in the circuit.

Component	Label	Type	Value	Purpose
Capacitors	C1, C4, C5, C6, C7, C8	SMD: ATC800A	9.1 pF	DC block and RF decoupling
	C10, C11	SMD: Murata	100 nF	Low frequency decoupling
	C2	SMD: ATC800A	24 pF	Part of stability network
	C3	SMD: ATC800A	10 μF	Low frequency decoupling
	C9	Electrolyte: 63 V	470 μF	Low frequency decoupling
Resistors	R1, R2	SMD: ATC800A	33 Ω	Part of stability network
	R3, R4	SMD: ATC800A	0 Ω	Connect supply to drain bias line

7.2 Stabilization of the Class AB Amplifier

Oscillation signals are observed on spectrum analyzer at low frequencies (16 MHz to 24 MHz) for different load terminations during load pull measurements of the transistor, biased for class AB operation. Class AB power amplifier circuit made of this transistor (Fig. 7.3) has shown oscillations at 19.2 MHz when terminated with 50Ω load.

The circuit is stable for all frequencies and loads for small-signal operation. During large-signal operation, the circuit is stable for low power levels (up to 24 dBm of input power). After 24 dBm, oscillation signal is observed at 19.2 MHz and it continued till 33 dBm. This phenomenon is observed when the circuit is fed with input frequencies 2.3, 2.4 and 2.5 GHz. Amplitude of oscillation signal at 2.5 GHz is more compared to that of oscillation signal amplitudes at 2.3 and 2.4 GHz.

The oscillation signal at low frequency got mixed with input signal and produced mixer like spectrum as shown in Fig. 7.4. The oscillation signal acted as an RF signal and the input signal acted as LO signal to produce mixing frequency components in the output spectrum.

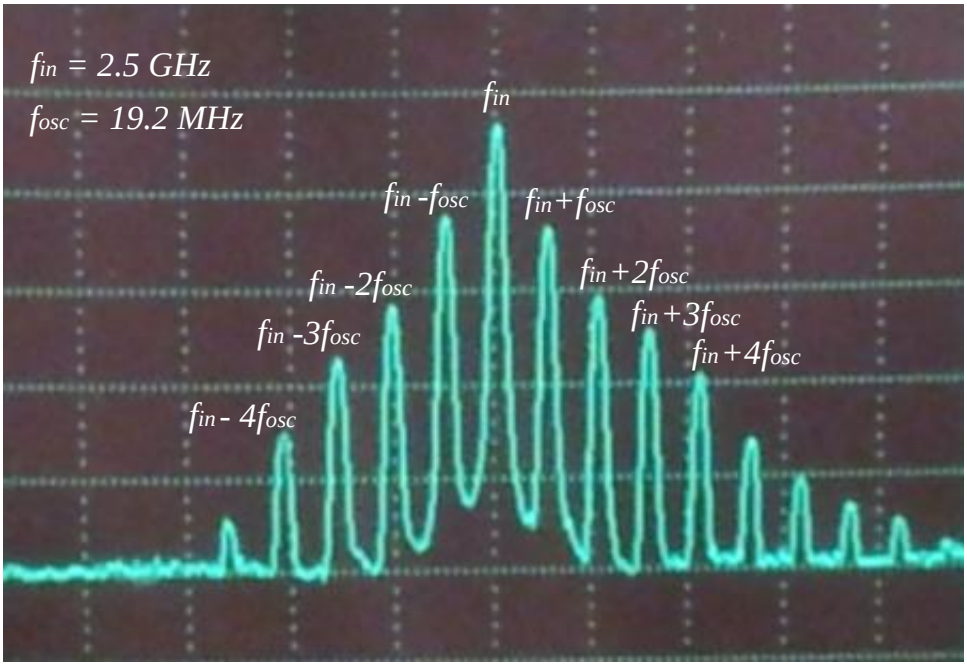

Figure 7.4: Mixer like spectrum observed at output of the class AB amplifier for f_{in} = 2.5 GHz without any stabilization network. Oscillation signal frequency (f_{osc}) is 19.2 MHz.

Pole zero identification stability analysis is purely dependent on transistor model accuracy. Since this transistor is in development stage, a good model that takes into account all parasitic effects is not readily available. Due to the transistor's high gain at low frequencies (< 400 MHz), fearing damage of measurement equipment, measurements are not performed at these frequencies by the author to build a good model.

Small-signal stability analysis using STAN on the circuit (50Ω termination) with an available transistor model has shown oscillation at 116 MHz. But in practice, oscillation occurred at 19.2 MHz for same operating conditions (biasing and termination). Large-signal analysis using STAN on available model has shown oscillations at several frequencies but are not in agreement with oscillation signal observed in practice. This is due to bad nonlinear model of the transistor especially at low frequencies.

Even though oscillation frequency observed in practice is different, oscillation mechanism is observed to be same as that of the transistor presented in chapter 6. Same oscillation phenomenon is observed for both transistors during load pull measurements. Therefore, it is decided to implement a similar kind of stability network (resistive and lag-lead compensation) in gate bias branch of the circuit. The circuit's layout is designed such that different kinds of compensation (resistive, lag, lead and lag- lead) networks can be implemented as stabilization networks when needed.

Since no good model that predicts exact oscillation frequency is available, esti-

mation of right stabilization component is also difficult. A trial and error method is used to stabilize the circuit by observing oscillating signal amplitude for change in stabilization component values. This helped to predict the direction of variation of stabilization component values. Initially, a resistor in the bias branch is used to stabilize the circuit. As expected, the resistor could decrease the oscillation amplitude but could not fully suppress it. This is true for even high values (1.3 KΩ) of resistance. This means, the effect of resistance to damp the oscillation at low frequencies is limited. This means, some part of oscillation signal that entered into bias line is damped and remaining part is undamped. Therefore, to suppress oscillation the stabilization network in combination with bias line has to provide low impedance at low frequencies such that entire oscillation signal enters into bias line. At the same time, stabilization network should damp the entered oscillation signal. This means, a frequency selective network which is significant at low frequencies such as lag-lead compensator should be used to damp the oscillation. Damping frequency and the amount of damping depends on component values in the compensator.

Parasitic of the components and their self-resonances also plays a key role in the compensator design. For some values of change in compensator components, it is observed that, oscillation signal suppression due to one input frequency (2.5 GHz) resulted in triggering oscillation due to another input frequency (2.6 GHz). This indicated that there is an optimum range of variation of stabilization components that could stabilize the circuit at all operating conditions (as indicated in [3]). By trial and error method, a lag compensator (Fig. 7.6) that could sufficiently suppress oscillations at all frequencies (2.23 to 2.7 GHz: gain is less than zero after 2.7 GHz) and all power levels (till the output power reached 3.5 dB compression point) is designed.

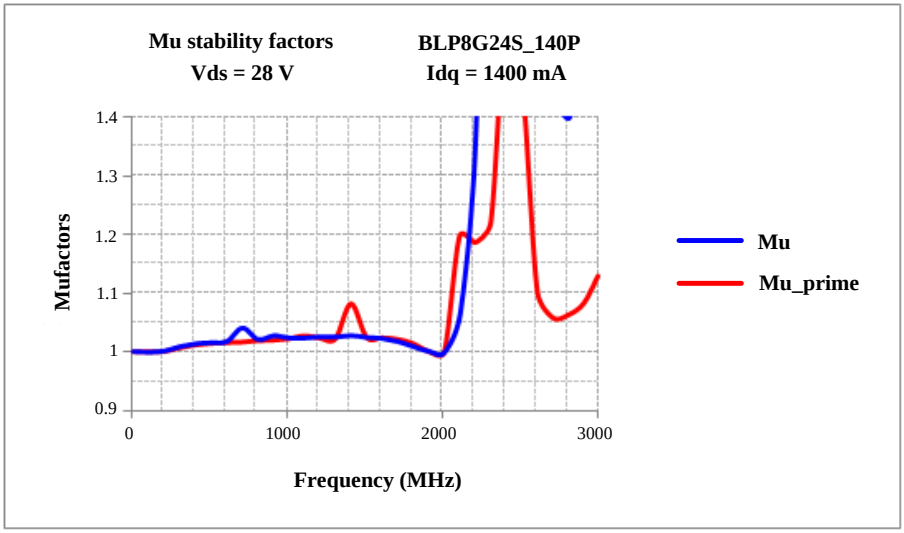

Figure 7.5: Measured μ and $\mu^{'}$ stability factors of the class AB power amplifier after stabilization, showing small signal stable operation.

Small-signal stability is verified using measured S-parameters of the power amplifier. These S-parameters are used to calculate stability factors μ and μ'. The measured stability factors μ and μ' are above 1 over frequency as shown in Fig. 7.5 indicating small-signal stability. The stability factors close to 1 at low frequencies is shown in Fig. 7.5 to ensure that they are above 1. At other frequencies, the stability factors are clearly greater than 1 and hence are clipped in Fig. 7.5.

Large-signal stability is verified using load pull measurements of the amplifier circuit. It is found that the circuit is potentially unstable for large-signal operation (Fig. 7.6). The oscillation started to trigger at high power levels (27 dBm) when the amplifier is fed with a 2.5 GHz input signal, for mismatch loads shown in Fig. 7.6. However, stability of the circuit at all frequencies and loads in $|\Gamma| = 0.5$ is checked and guaranteed. Potential instability is allowed for high power amplifiers provided the unstable loads are out of operating region [1].

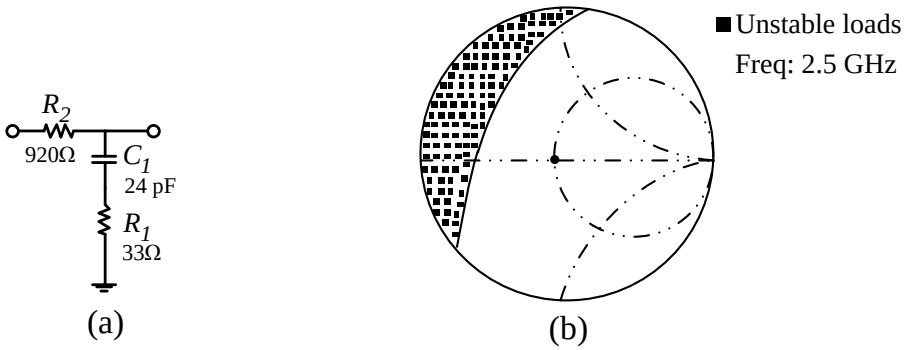

Figure 7.6: (a) Lag compensator stability network. (b)large-signal unstable loads of the class AB amplifier after stabilization, observed during load pull measurements.

8. PERFORMANCE MEASUREMENTS AND DESIGN EVALUATION

This chapter presents performance measurements of the designed and stabilized 2.32 - 2.37 GHz class AB power amplifier. Later, the measured load pull results (power, gain and efficiency) of both the amplifier and the transistor used in the amplifier are compared for design evaluation.

8.1 Performance Measurements

This section presents performance measurement results of the class AB amplifier. The performance parameters include input return loss, power gain, efficiency, output power and ACPR.

8.1.1 Input Return loss (RL)

Input return loss measurement is performed using large-signal test bench shown in appendix A6. It is obtained by measuring input power and reflected power using power sensors.

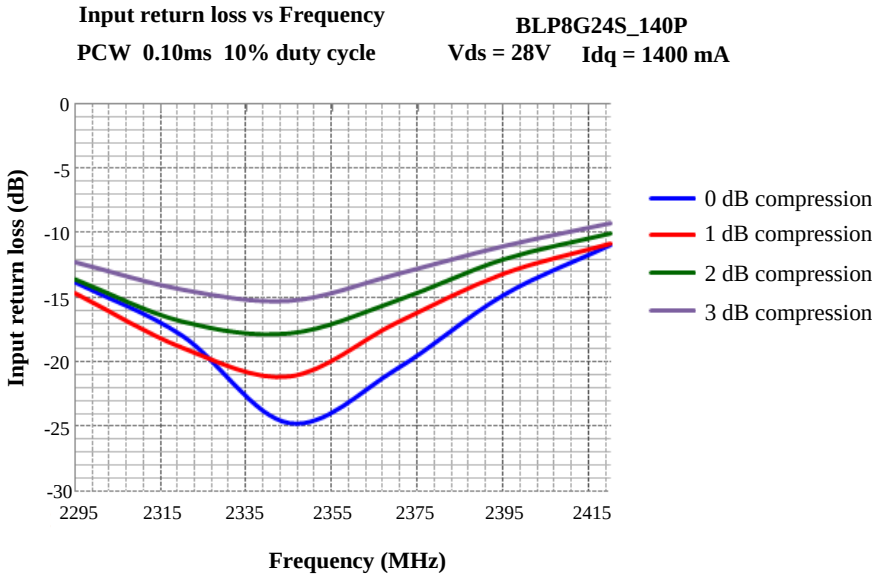

Figure 8.1: Input return loss measured when the amplifier is fed with pulsed continuous wave (PCW) signal and when the output power reached 0 dB, -1dB, -2dB and -3 dB compression points.

A coupler with 20 dB attenuation is placed at input side of the amplifier to cope for high reflections. The power sensors are placed on either side of the coupler. Calibration of whole setup setup is done by taking coupler attenuation into consideration. First power sensor before the coupler is used to measure input power from signal generator. Second one, which is after the coupler, is used to measure reflected power from input port of the amplifier. The input return loss (Fig. 8.1) is then calculated as a ratio of the reflected power to the input power and is shown in Fig. 8.1 with respect to dB scale.

It can be observed that the input return loss is good around center frequency 2345 MHz. Maximum value of the input return loss is around 26 dB for 0 dB compression point. The amplifier has a input return loss better than 10 dB from 2295 MHz to 2395 MHz at 3 dB compression point indicating good conjugate match over wide frequency range.

8.1.2 Pulsed Contiuous wave (PCW) Power Sweeps

Output power, gain and efficiency of the amplifier are measured using large-signal test bench setup shown in appendix A6. Measured gain and efficiency, plotted with respect to output power is shown in Fig. 8.2. Measurements are performed by driving the amplifier with a pulsed continuous wave of 10% duty cycle. This is a standard signal that is used to perform large-signal measurements of a base station power amplifier [44].

An output coupler and an attenuator with a total of 55 dB attenuation is connected to amplifier's output in order to avoid any damage of measurement equipment for high output power levels. Calibration of the measurement setup is done by taking this attenuation into consideration. Output power is measured using a power sensor connected to one of the output coupler's ports. Gain is then calculated as the difference of the output power in dB to that of the input power in dB. The output current is measured using a current sensor connected to one of output coupler's port. Efficiency is calculated as [44],

$$\eta_d = 100 \times \frac{P_{Load}}{\left[\frac{I_D - I_{DQ}}{\delta} + I_{DQ}\right] \times V_{DS}}. \tag{8.1}$$

In the above expression η_d is drain efficiency [%], P_{Load} is pulsed peak power [Watts], I_D is average drain current [A] and I_{DQ} is quiescent current [A]. The variable V_{DS} represents supply voltage [V] and δ is duty cycle of the PCW.

Measured gain and efficiency of the amplifier at 140 W output power is given in Table 8.1. Output power of the amplifier at 1 & 3 dB compression points read from the graph (Fig. 8.2) is given in Table 8.2.

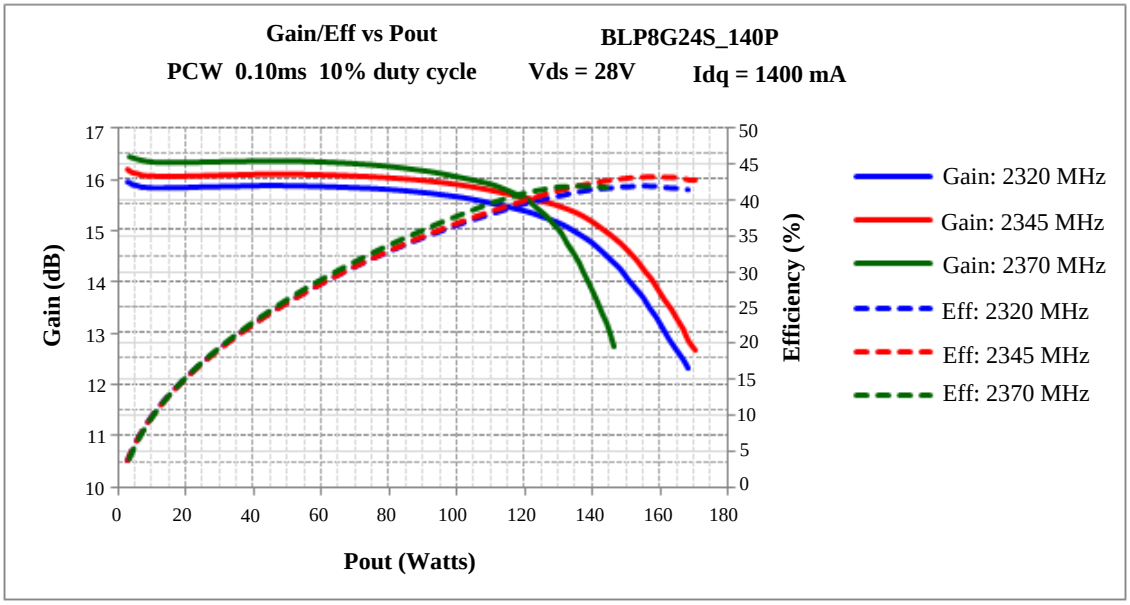

Figure 8.2: Gain and efficiency curves of the class AB amplifier plotted with respect to its output power in Watts.

Table 8.1: Gain and efficiency at peak power [140 W] @ pulsed CW

Frequency (MHz)	Gain (dB)	Efficiency (%)
2320	14.748	42.08
2345	15.21	42.08
2370	13.6	41.99

Table 8.2: Peak power (P_{-1dB} and P_{-3dB} @ pulsed CW

Frequency (MHz)	P_{-1dB} (W)	P_{-1dB} (dBm)	P_{-3dB} (W)	P_{-3dB} (dBm)
2320	133.07	51.24	162.21	52.10
2345	141	51.49	165	52.17
2370	123.5	50.92	142.69	51.54

8.1.3 Wide-band CDMA (WCDMA) Power Sweeps

Wide-band CDMA power sweeps are performed to characterize linearity of a power amplifier. The class AB amplifier is fed with a two carrier wide band CDMA signal having 3.84 MHz bandwidth as shown in Fig. 8.3. Spacing between the two carriers is 5 MHz. Adjacent channels considered for ACPR measurement are at an offset of $+/-$ 5 MHz as shown in Fig. 8.3.

Amount of non linearity or the amount of interference by adjacent channels is calculated as ACPR. It is calculated as the ratio of average power in adjacent channel bandwidth to that of average power in operating frequency band (2320 to 2370 MHz).

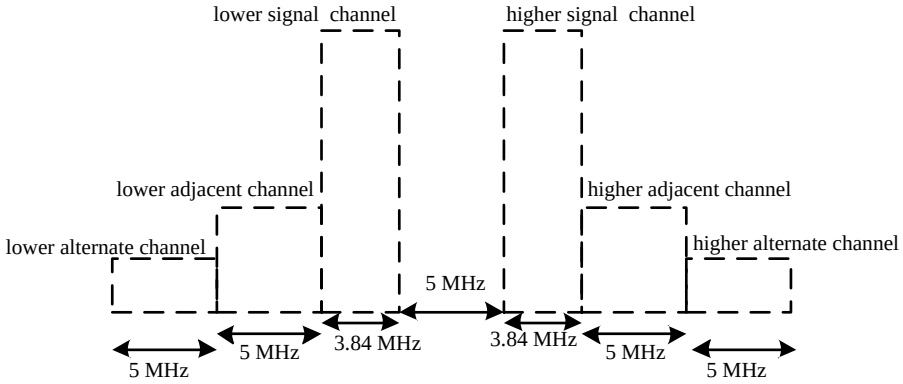

Figure 8.3: 2cWCDMA signal settings for ACPR measurements

Typical specification of the ACPR at 5 MHz bandwidth for a base station amplifier is −36 dBc at back off power. The back off power is decided by peak to average ratio (PAR) of the amplifier's output power. The −36 dBc of ACPR is from the reference class AB amplifier made of ceramic packaged transistor [45]. It has a peak power of 52 dBm at its operating frequency and a PAR of 8dB. Therefore at a back off of 8 dB from the peak power, which is 44 dBm, the ACPR is given as −36 dBc. For the amplifier in this work, peak power is 52.3 dBm and PAR is around 7.9 dB. Therefore, at a back off power of 44.4 dBm, ACPR is read as −32 to −34 dBm from the Fig. 8.4. This is a slight degradation compared to ACPR of the reference ceramic device [45].

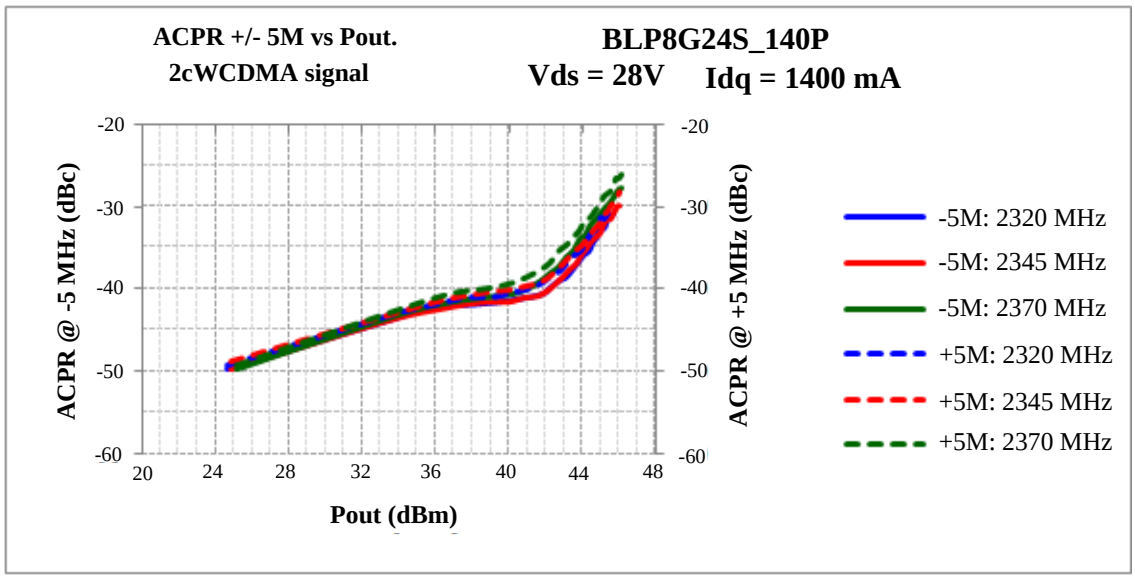

Figure 8.4: ACPR of the class AB power amplifier fed with 2c WCDMA with a 5 MHz spacing and a clipping level of 46 %, sidebands are placed at an offset of $+/-5$ MHz.

8.2 Design Evaluation and Discussion

This section is divided into two subsections. In the first subsection, load pull measurements of the class AB amplifier and the transistor used in the amplifier design are compared to evaluate amplifier's design. In the second subsection, large-signal PCW measurements of the amplifier before and after stabilization are measured and compared to know the effect of stability network on the amplifier's performance. 2cWCDMA measurements of the amplifier without stabilization are not performed in order to avoid any damage of measurement equipment due to oscillation.

8.2.1 Load Pull Measurements of Transistor versus Class AB Amplifier

Load pull measurements of the transistor and the class AB amplifier made of the transistor are performed for frequencies 2.23, 2.3 and 2.4 GHz. The intended operating region of the transistor is from 2.32 to 2.37 GHz with center frequency at 2.345 GHz. Because of non-availability of source and load tuner calibration files exactly at those frequencies, measurements are not performed for those frequencies. Measurements at 2.3 GHz and 2.4 GHz is enough to get an idea about performance at in band frequencies. Load pull measurement results of the transistor and the corresponding class AB power amplifier are shown in Table 8.3.

In practice, maximum performance that can be achieved by an amplifier is less than or equal to transistor's performance used in amplifier design. If the amplifier's performance parameters (power, gain & efficiency) are close to the transistor's parameters, then it indicates a good design.

Table 8.3: Load pull measurement comparison of peak power, peak gain and peak efficiency of NXP's transistor and corresponding class AB amplifier.

	NXP's transistor			NXP's class AB amplifier		
Frequency (GHz)	Power (dBm)	Gain (dB)	Efficiency (%)	Power (dBm)	Gain (dB)	Efficiency (%)
2.23	53.59	19.51	59.22	51.9	18.3	53.3
2.3	53.47	19.46	59.08	52.66	18.22	51.66
2.4	53.52	19.89	57.47	51.33	18.1	46.2

It can be observed from Table 8.3 that peak power, gain and efficiency of the transistor are observed to be much higher as compared to the amplifier. When an amplifier is designed out of a transistor, it is estimated at NXP by Jos van der

Zanden (Principal RF Engineer) that there would be 0.3 dB of PCB losses around 2 GHz frequency. This corresponds to a loss of around 3 to 4 % in the efficiency. These losses has been measured and characterized at NXP for rogers Ro4350B (30 mil) PCB. But, the observed loss in peak power, gain and efficiency in Table 8.3 is much more than expected. This is due to low value of real part of transistor's output impedance at peak output power. This can be observed from the Fig. 8.5.

The impedance for peak power in the Smith chart lies on Q circle with high value (9.53) as shown in Fig. 8.5. High Q at transistor's output results in high losses, when the matching network is realized. Unnecessary high reactive (inductive) currents will flow into the PCB that will not contribute effectively to power transfer, but will cause extra losses. Lowering the Q value by redesigning transistors internal matching network will improve the amplifier's efficiency.

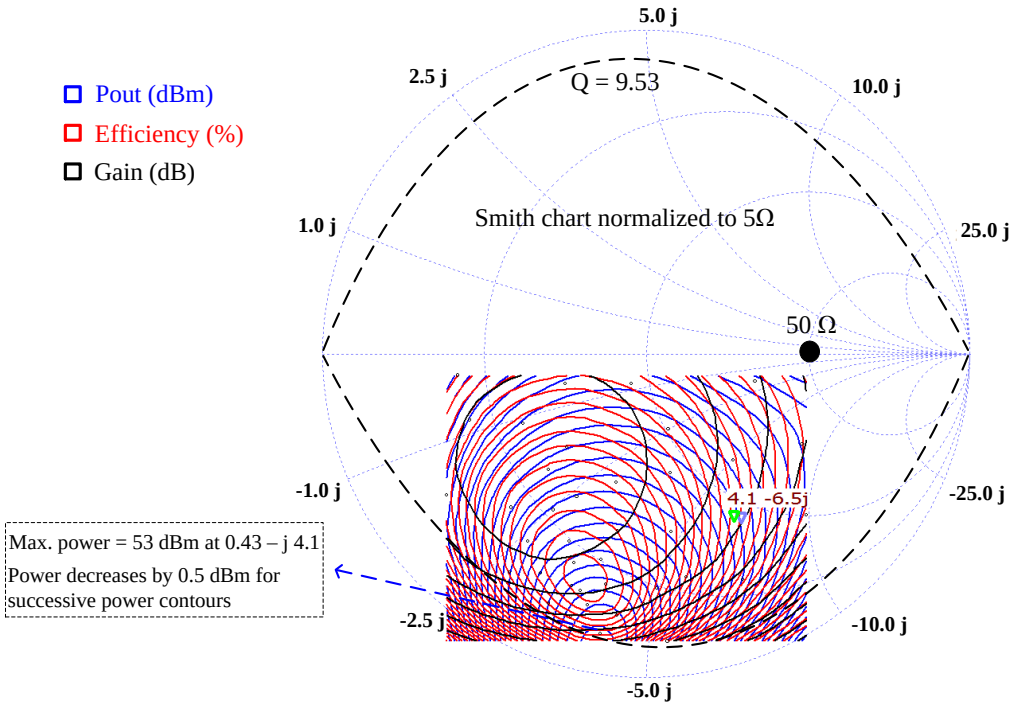

Figure 8.5: Power gain and efficiency contours of NXP's. The peak power impedance is on high quality factor (Q) circle (9.53).

One of the reasons for reduced efficiency is the change of transistor from one sample to another. The output matching network is realized based on load pull data of one (first) transistor sample. This first sample failed during the stability network tuning, due to an oscillation signal with high amplitude. It is then replaced with another (second) sample. The second sample has deviation in input and output impedances compared to first sample due to process variation and tolerances. This has caused some loss in performance. In addition to this, drain bias line could also have contributed more losses than expected due to its thin long structure. The performance can be improved little bit by realizing wider bias lines at output. All

these losses did not appear in the load pull results of the transistor because; the PCB losses of the load pull fixture (circuit) are de-embedded automatically [28] during measurements.

Table 8.4: Peak power, peak gain and peak efficiency of the class AB amplifier in the operating band obtained using large signal PCW power sweeps matched to fixed 50Ω load.

NXP's class AB amplifier			
Frequency (GHz)	Power (dBm)	Gain (dB)	Efficiency (%)
2.32	51.9	15.95	42.06
2.345	52.30	16.18	43.13
2.37	51.64	16.45	42.08

The peak power, gain and efficiency of the class AB amplifier observed in Table 8.4 are less than that in table 8.3. The measurements shown in the Table 8.3 are load pull measurements performed for out of band frequencies. The measurements shown in Table 8.4 are measured using large-signal test bench and are performed for in band frequencies. However, the performance parameters in Table 8.4 should be in between the values measured at out of band frequencies (Table 8.3). But the losses observed for the in-band frequencies seem to be more. This is because the transistor is matched to an impedance optimum for power and efficiency. Therefore the values measured in the in-band would be less than the peak values. This can be seen from the Fig. 8.6

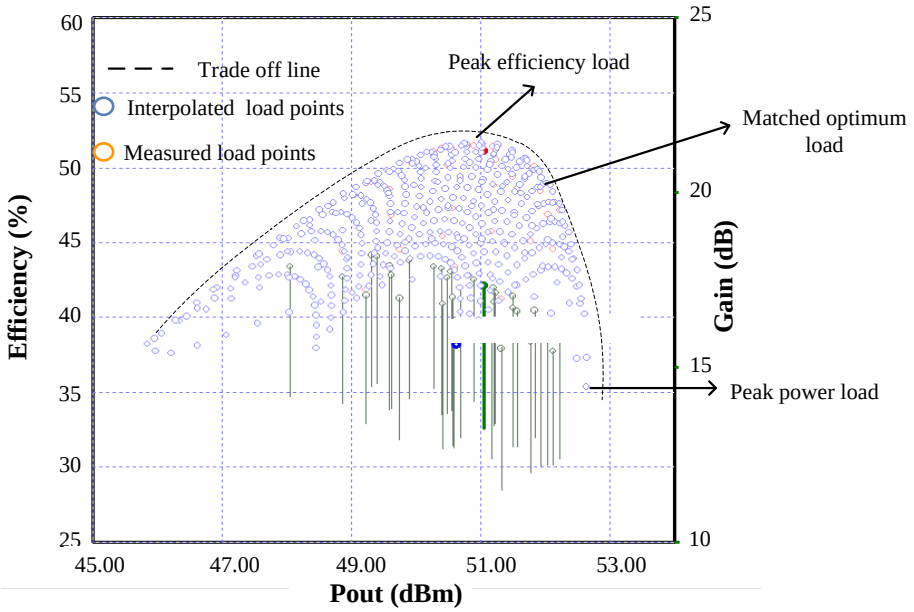

Figure 8.6: Efficiency and gain of the class AB amplifier at 2.3 GHz plotted with respect to output power for various measured and interpolated loads. The trade off line showing load boundaries at which the peak efficiency, power and gain can be achieved.

8.2.2 Pulse CW Measurements Before and After Stabilization

Large signal measurements with pulse CW signal are performed for the class AB amplifier with and without stability network. It is observed that the circuit is highly unstable for the in-band frequencies before stabilization. The gain curves have shown a strange behavior as shown in Fig. 8.7 without the stabilization network. The peak power, gain and efficiency for the amplifier with and without stabilization are shown in Table 8.5.

It can be observed from the Table 8.5 that the peak power and efficiency achieved by the amplifier before stabilization is more than the peak power and efficiency achieved by the amplifier after stabilization. The stability network is causing an average loss of around 0.3 dB in power and 2 to 3% in efficiency. This is because of non perfect RF grounding of the gate bias line. The input of the transistor is not supposed to see the stability network in the operating band but, because of the non perfect RF grounding the stability network has its effect in the operating band.

Table 8.5: Peak power, gain and efficiency of the class AB amplifier before and after stabilization.

	Without Stabilization			With Stabilization		
Frequency (GHz)	Power (dBm)	Gain (dB)	Efficiency (%)	Power (dBm)	Gain (dB)	Efficiency (%)
2.32	52.55	13.42	45.47	51.9	15.95	42.06
2.345	52.50	13.42	44.97	52.30	16.18	43.13
2.37	51.83	13.43	43.5	51.64	16.45	42.08

The peak gain of the amplifier is low before stabilization compared to its gain after stabilization. This is because, the stability network has also became a part of input matching network because of imperfect RF grounding. Therefore, the input matching network is tuned along with stability network in the operating band. When the stability network is removed, the input matching is mismatched and is the reason for decrease in linear gain (Fig. 8.7) when the measurements are performed without stabilization network. The decrease in input return loss observed when the stability network is removed is around 4.5 dB. This causes a corresponding mismatch loss of 2.5 dB, which explains the reduction in gain without stabilization.

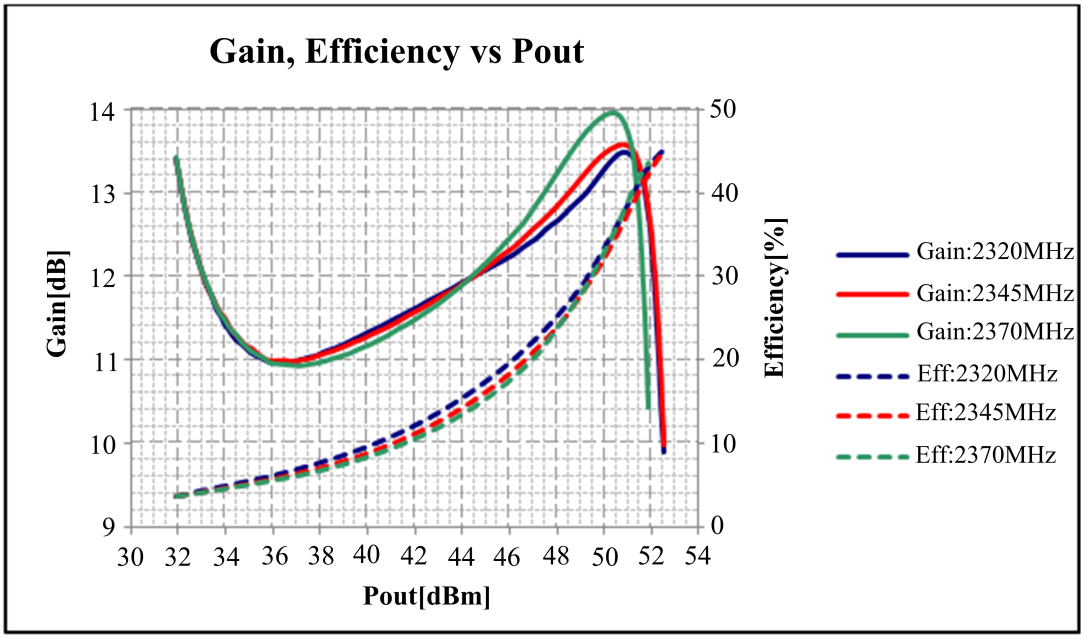

Figure 8.7: Gain and efficiency curves of the class AB amplifier without stabilization plotted with respect to output power

8.3 Thesis Outcomes

The outcomes of the thesis include,

- Demonstration of pole zero identification method for stabilization of a power amplifier.
- A procedure to obtain values of stabilization components and a flow chart to work with STAN software.
- Pointing out the need for good linear and nonlinear models for new generation NXP transistors to accurately get stability information during STAN analysis.
- Noticing the requirement of a measurement method to obtain poles and zeros of power amplifiers in order to compare with STAN identifications. Since, for now it is not possible to obtain measured transfer function data of a power amplifier, stability is checked practically using spectrum analyzer and measured gain, efficiency curves.
- Recommendation for the improvement of NXP's experimental transistor's output impedance by changing its internal output matching topology. The current matching network has high Q (9.53) and leads to more losses. Change in the matching network clearly brings improvement in output power, and efficiency of the power amplifier. Suggestion to realize wider drain bias lines in the class AB amplifier layout to minimize losses.

9. CONCLUSION

This thesis presented the design and stabilization of a 2.32-2.37 GHz class AB power amplifier. General design practice at NXP of a power amplifier is discussed and considered while designing the amplifier. Pole zero identification method for the stability analysis a microwave power amplifier is presented with its background, history, theory and application procedure. Initially, the method is used to stabilize a push-pull amplifier. Oscillation detection, stabilization node and stabilization network components are found using this method. Later, a class AB amplifier made of the same transistor family as of the transistor in push pull amplifier, but for different power level, is designed. Stabilization location and stability network selection of this amplifier is done using the information obtained from the stability analysis of the push-pull amplifier.

A frequency selective lag-lead compensator stability network is designed using root locus method for push-pull amplifier. A similar kind of network called lag compensator is designed to stabilize the designed class AB power amplifier. The designed and constructed class AB power amplifier in this work is unconditionally stable for small-signal operation and potentially unstable for large-signal operation. The amplifier can deliver an output power of 140 Watts with a gain of 15.2 dB and an efficiendcy of 42.08 %. The ACPR of the amplifier is -33 dBc at 44.4 dBm backoff power.

In addition to the power amplifier design, a step by step implementation procedure of the pole zero identification method is presented. The small signal stability analysis of the power amplifier using this method is compared with the μ factor and is verified.

Accessibility to each and every node/branch of the design to find optimum location for stabilization is the advantage of this method. Estimation of stabilization component value and the direction of variation of the components to achieve stability is another advantage of this method. Simplicity in its usage compared to other large-signal stability analysis methods is the added advantage of this method. This method is purely based on simulations. Hence, it is very important to have a good linear and nonlinear models of the transistor for small-signal and large-signal stability analysis.

Application of the pole zero identification method for stability analysis of multi

port (mixer) circuits can be considered for future work. Another line of research worth pursuing is the implementation of pole zero identification method for stability analysis at transistor level rather than at amplifier level.

REFERENCES

[1] Samuel Y. Liao. *Microwave Circuit Analysis and Amplifier Design.* Prentice Hall Inc., Englewood cliffs, New Jersy 07632, 1987.

[2] Mihai Albulet. *RF Power Amplifier.* Noble Publishing Corporation, 2001.

[3] S. Jeon. *Design and Stability Analysis Techniques for Switching Mode Nonlinear Circuits: Power Amplifiers and Oscillators.* Doctoral Dissertation: California Institute of Technology, 2006. 185 p.

[4] C. W. Bostian H. L. Krauss and F.H. Raab. *RF transmitting transistor and power amplifier fundamentals.* Phillips Semiconductors, 1998.

[5] Steve. C. Cripps. *RF Power Amplifiers for Wireless Communications.* Artech House, London, 1999.

[6] E. Kappos. *Classical Control Theory: A course in the Linear Mathematics of Systems and Control.* University of Sheffield, School of Mathematics and Statistics, January 16th 2002.

[7] M. Gopal. Compensator design using root locus plots. *http://www.nptel.iitm.ac.in/video.php?subjectId=108102043*. Accessed: 13-May-2013.

[8] A. Subramaniam and M.F. Ain. Unified approach for large signal stability analysis of 4watt uhf rf power amplifier. In *IEEE 3rd International Conference on Communication Software and Networks (ICCSN), 2011*, pages 455–459, 2011.

[9] J. Jugo, J. Portilla, A. Anakabe, A. Suarez, and J.-M. Collantes. Closed-loop stability analysis of microwave amplifiers. *Electronics Letters*, 37(4):226–228, 2001.

[10] N. Ayllon, J.-M. Collantes, A. Anakabe, I. Lizarraga, G. Soubercaze-Pun, and S. Forestier. Systematic approach to the stabilization of multitransistor circuits. *IEEE Transactions on Microwave Theory and Techniques*, 59(8):2073–2082, 2011.

[11] R. Ludwig and P. Bretchko. *RF Circuit Design Theory and Applications.* Prentice-Hall Inc., 2000.

[12] Demystifying the negative differential resistance phenomenon. *http://en.wikibooks.org/wiki/Circuit_Idea/Negative_Differential_Resistance*. Accessed: 12-May-2013.

[13] Guillermo Gonzalez. *Microwave Transistor Amplifiers, Analysis and Design.* Prentice Hall, Inc., 2nd edition edition, 1984, 1997.

[14] R. Gilmore and L. Besser. *Practical RF Circuit Design for Modern Wireless Systems, Active Circuits and Systems*, volume II. Artech House Inc., Boston, London, 2003.

[15] Almudena Suarez. *Analysis and Design of Autonomous Microwave Circuits.* John Wiely and Sons, Inc., 2009.

[16] M. Ohtomo. Stability analysis and numerical simulation of multidevice amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 41(6):983–991, 1993.

[17] T. Narhi and M. Valtonen. Stability envelope-new tool for generalised stability analysis. In *Microwave Symposium Digest, 1997., IEEE MTT-S International*, volume 2, pages 623–626 vol.2, 1997.

[18] A. Anakabe, S. Mons, T. Gasseling, P. Casas, R. Quere, J.-M. Collantes, and A. Mallet. Efficient nonlinear stability analysis of microwave circuits using commercially available tools. In *Microwave Conference, 2002. 32nd European*, pages 1–5, 2002.

[19] J. Jugo, A. Anakabe, and J.-M. Collantes. Control design in the harmonic domain for microwave and rf circuits. *IEE Proceedings - Control Theory and Applications*, 150(2):127–131, 2003.

[20] J. M. Collantes and A. Anakabe. Large-signal stability analysis through pole zero identification techniques. *European Microwave Conference*, 2005.

[21] A. Anakabe, N. Ayllon, J.-M. Collantes, A. Mallet, G. Soubercaze-Pun, and K. Narendra. Automatic pole-zero identification for multivariable large-signal stability analysis of rf and microwave circuits. In *European Microwave Conference (EuMC), 2010*, pages 477–480, 2010.

[22] A. Anakabe J. M. Collantes and A. Mallet. Large-signal stability analysis through pole zero identification. *International Microwave Symposium Workshop*, 2007.

[23] A. Anakabe G. Soubercaze Pun J. M. Collantes, N. Ayllon and S. Forestier. Expanding the capabilities of pole zero identification techniques for stability analysis. *IEE MIT-S International Microwave Symposium Workshop*, 2009.

[24] S. Dellier, R. Gourseyrol, G. Soubercaze-Pun, J.-M. Collantes, A. Anakabe, and K. Narendra. Stability analysis of microwave circuits. In *IEEE 13th Annual Wireless and Microwave Technology Conference (WAMICON), 2012*, pages 1–5, 2012.

[25] Rowena Lynn Yutuc. *RF Microwave Transistor Parameter Measurement Procedure: A presentation on all defined test parameters measured at RF Microwave transistors final test setups.* Philips, January 2002.

[26] M. Slovick. *Measuring ACPR in CDMA Amplifiers.* Helwlett Packard Co., Santa Rosa, CA, 2002.

[27] C. W. Bostian H. L. Krauss and F.H. Raab. *Solid State Radio Engineering.* John Wiley and Sons, New York, 1980.

[28] Maury-ats load pull guide. *http://web.doe.carleton.ca/\~nagui/labequip/loadpull/loadpull_brief.html\#introduction*. Accessed: 13-May-2013.

[29] N. Storey. *Electronics, A Systems Approach.* Pearson Education, 3rd edition edition, 2006.

[30] Almudena Suarez and Raymond Quere. *Stability Analysis of Nonlinear Microwave Circuits.* Artech House Inc., 2003.

[31] V. Iglesias, A. Suarez, and J.L. Garcia. New technique for the determination through commercial software of the stable-operation parameter ranges in nonlinear microwave circuits. *IEEE Microwave and Guided Wave Letters*, 8(12):424–426, 1998.

[32] A. Suarez, F. Ramirez, S. Jeon, and D. Rutledge. Stability analysis of power amplifiers. In *IEEE International Symposium on Radio-Frequency Integration Technology, 2009. RFIT 2009.*, pages 203–206, 2009.

[33] J.-M. Collantes, I. Lizarraga, A. Anakabe, and J. Jugo. Stability verification of microwave circuits through floquet multiplier analysis. In *The 2004 IEEE Asia-Pacific Conference on Circuits and Systems, 2004. Proceedings.*, volume 2, pages 997–1000 vol.2, 2004.

[34] J.-M. Collantes, N. Otegi, A. Anakabe, N. Ayllon, A. Mallet, and G. Soubercaze-Pun. Monte-carlo stability analysis of microwave amplifiers. In *Wireless and Microwave Technology Conference (WAMICON), 2011 IEEE 12th Annual*, pages 1–6, 2011.

[35] Nerea Otegi, A. Anakabe, Joana Pelaz, J.-M. Collantes, and G. Soubercaze-Pun. Increasing low-frequency stability margins in microwave amplifiers from experimental data. In *IEEE MTT-S International Microwave Symposium Digest (MTT), 2012*, pages 1–3, 2012.

[36] S. Dellier. *Stability Analysis of Microwave Circuits*. Tour Agilent ADS EMPro, 2011.

[37] Matlab. Siso design tool documentation. *http://www.mathworks.se/help/control/ug/overview-of-the-siso-design-tool.html*. Accessed: 13-May-2013.

[38] M. Jankowski, E. Limiti, and P.E. Longhi. Freitag method application to pa stability test. In *INMMIC 2008. Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits, 2008.*, pages 149–152, 2008.

[39] O. P. Lunden. Basics of rf engineering (ele - 6057): course material. Tampere University of Technology, 2011.

[40] F. Caspers. *RF Engineering Basic Concepts: The Smith Chart*. CAS, Aarhus, June 2010.

[41] NXP Semiconductors. *RF Manual 16th edition: Application and Design Manual for High Performance RF products*. NXP Semiconductors, June 2012.

[42] Maury Microwave Operating Manual. Automated tuner system, pc based application software.

[43] ADS. Advanced design system-documentation 2011. *http://edocs.soco.agilent.com/display/ads2011/Examples+of+Data+Based+Load+Pull+Simulation*. Accessed: 13-May-2013.

[44] Ji Zhao. Measurement results of a 2110 mhz - 2170 mhz class ab demo amplifier board, August 2011. NXP Semiconductors, Company internal.

[45] Power ldmos transistor blf7g24l-140 data sheet. *http://www.nxp.com/documents/data_sheet/BLF7G24L-140_7G24LS-140.pdf*, August 2011. Accessed: 13-May-2013.

A. APPENDIX

Frequency (GHz)	Optimum Source Impedance (Ω)	Optimum Load Impedance (Ω)		
		Max.Power	Max.Gain	Max.Efficiency
2.23	1.93-j5.91	0.541-j.43 (53 dBm)	3.2-j2.2 (19 dB)	1.4-j3.6 (58%)
2.3	2.73-j6.04	0.43-j4.1 (53.5 dBm)	2.3-j1.8 (20 dB)	1.4-j3.7 (58%)
2.4	4-j7.15	0.7-j4.4 (53dBm)	0.82-j2.60 (19dB)	0.91-j3.7 (56%)
2.5	7.64	0.57-j4.6 (53.5 dBm)	0.84-j4 (19dB)	0.53-j3.3 (54%)

Figure A.1: *Load pulled impedances of NXP's transistor used in the amplifier design*

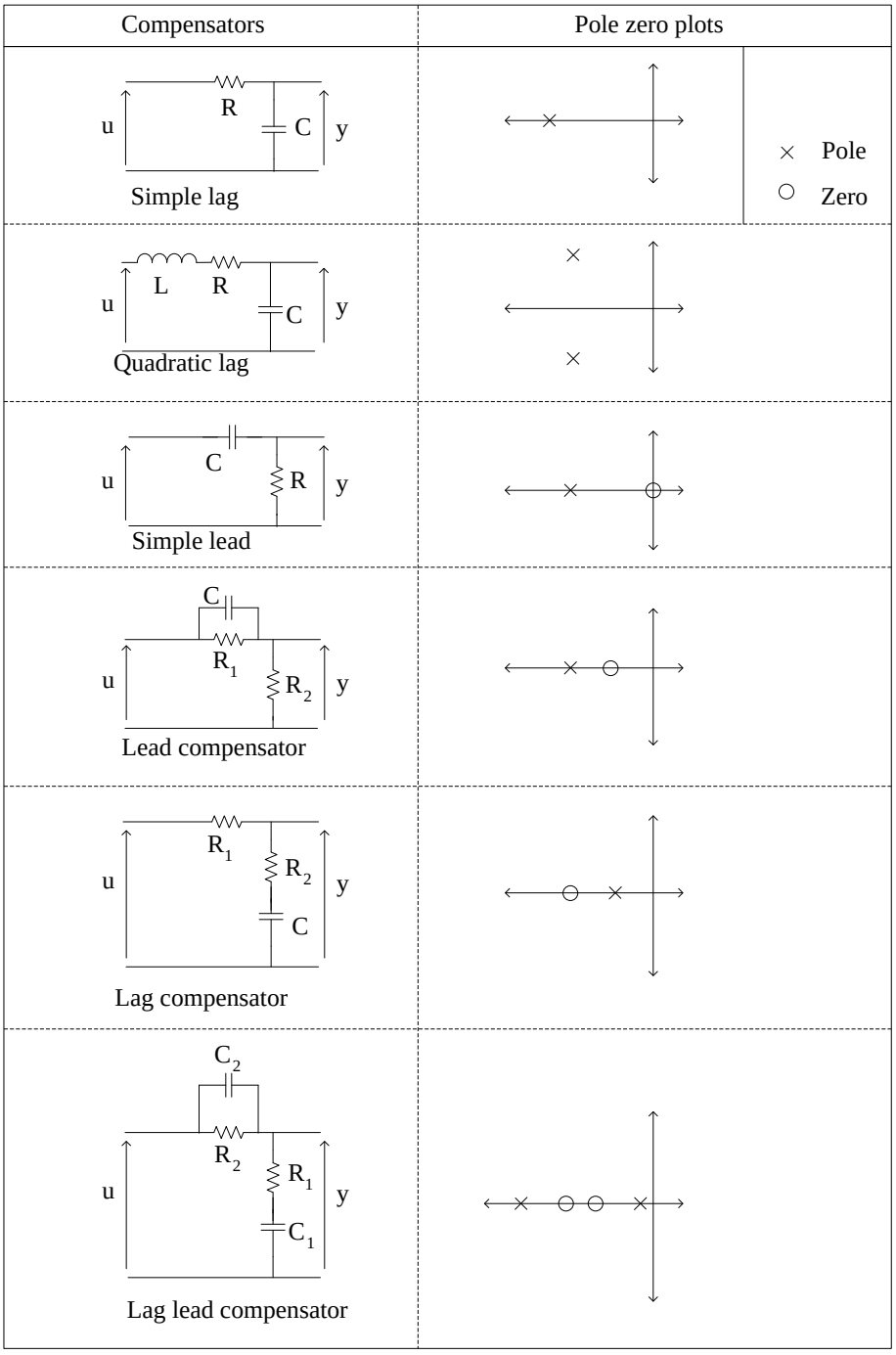

Figure A.2: *Compensator networks*

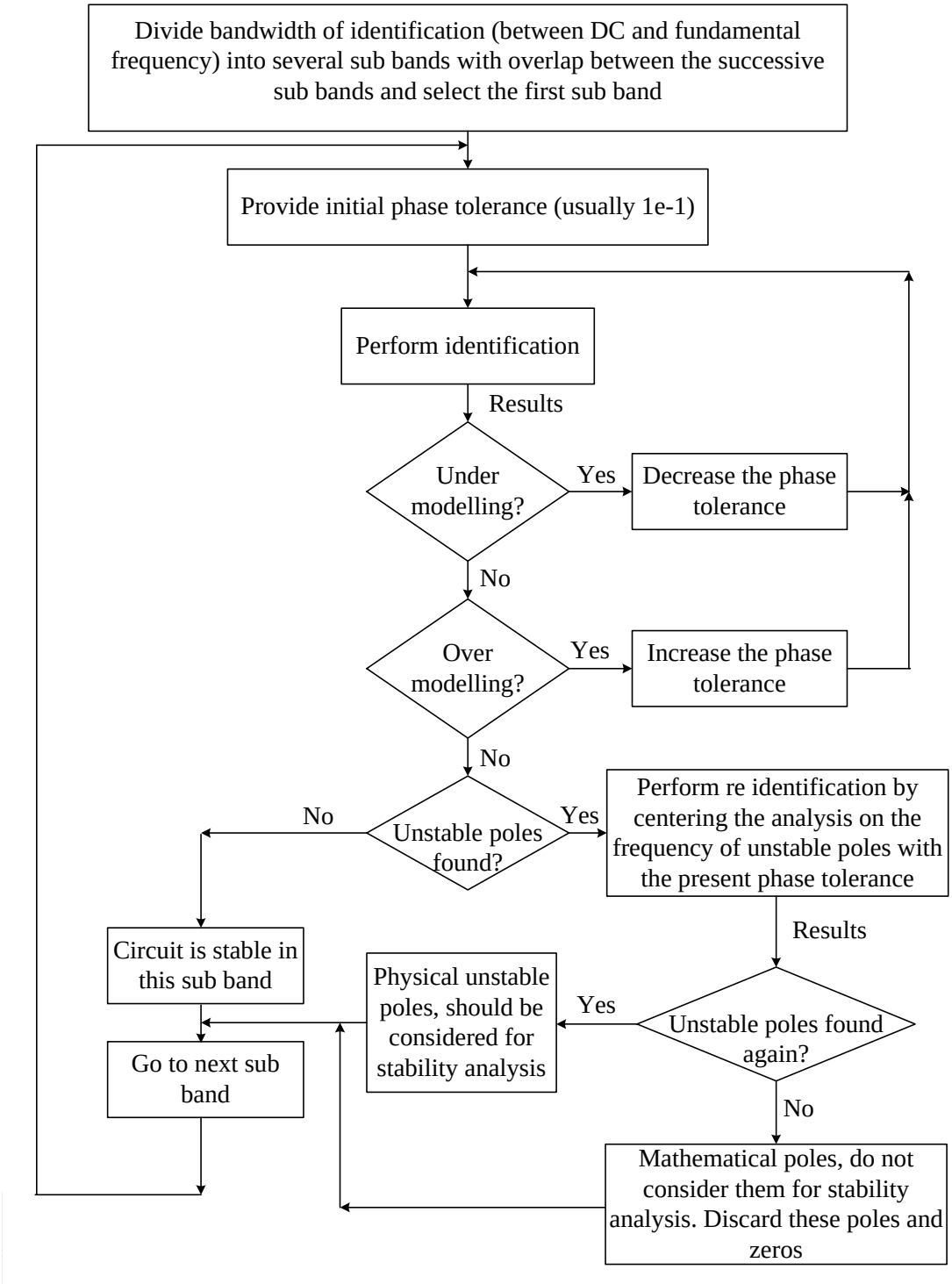

Figure A.3: *STAN working flow chart*

Root locus plot in MATLAB

% *Before starting with the code, the poles and zeros from the STAN has to be exported as an excel file using the option in STAN. After that the excel file has to be imported into matlab. The matlab imports those poles and zeros in a two dimensional workspace matrix named 'data'. The poles and zeros are stored separately in different columns as real and imaginary numbers.* %

```
clear all;
close all;

n = 10; % Number of poles
m = 8; % Number of zeros
i = 1:1:n; %Define a variable 'i' that points to poles in 'data' matrix

j = (n+1):1:m; %Define a variable 'j' that points to zeros in 'data' matrix

Poles = 2*pi*(data(i,1)+(1j*data(i,2))); % Combines the real and imaginary parts of the poles to represent as a complex pole. By default STAN gives poles with respect to frequency axis. It needs to be converted to angular frequency scale by multiplying with 2*pi.

Zeros = 2*pi*(data(j,1)+(1j*data(j,2))); % Combines the real and imaginary parts of the zeros to represent as a complex pole.

TF = zpk(Zeros,Poles,1); % returns the transfer function of the system with zeros and poles.

bode(TF); % plots the magnitude and phase plot of the transfer function

k = 8.41e-4; % corrected loop gain factor (see appendix 6B)

TF_correct = zpk(Zeros,Poles,k); % returns the corrected transfer function.

rlocus(TF); % Plots the root locus of the transfer function TF

sisotool(TF); % Opens the mat lab SISO tool which helps to design suitable compensators to control stability and performance of closed loop control systems.
```

1. Obtain the bode plot using STAN identified poles and zeros in mat lab (refer previous page).

2. Compare the magnitude at the oscillation frequency (any frequency) of bode plot with that of STAN magnitude plot.

3. Convert the magnitudes in dB scales to linear scales. While converting the bode magnitude to linear scale, use $10^{\frac{(magnitude\ in\ dB}{20}}$) instead of $10^{\frac{(magnitude\ in\ dB}{10}}$). This is because the bode plot is plotted with respect to $20\ log_{10}(magnitude\ in\ dB)$.

4. Calculate the difference between the two magnitudes. This is the correction factor.

5. If the bode magnitude is more than the STAN magnitude, then divide the transfer function obtained by the correction factor, otherwise multiply the transfer function with the correction factor.

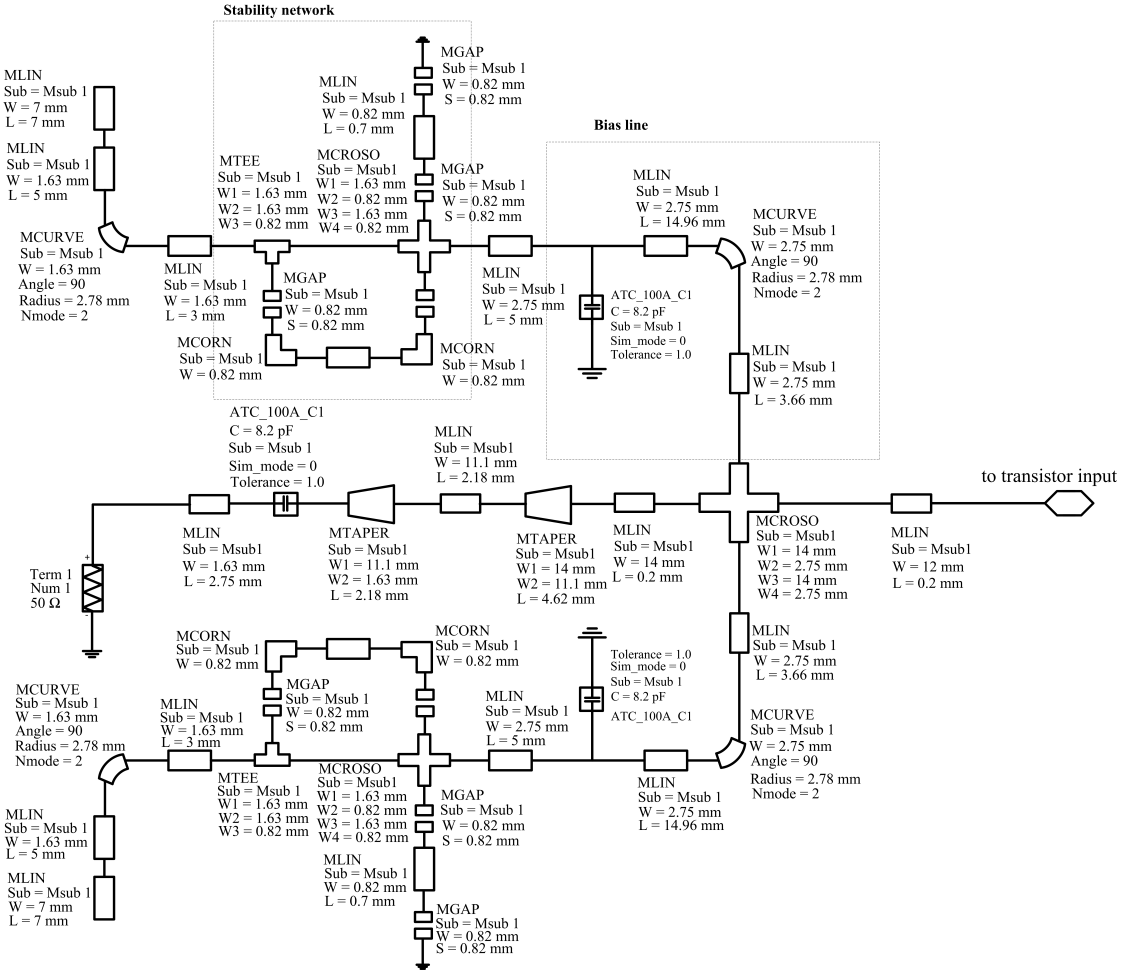

Figure A.4: *Final input matching network with bias lines*

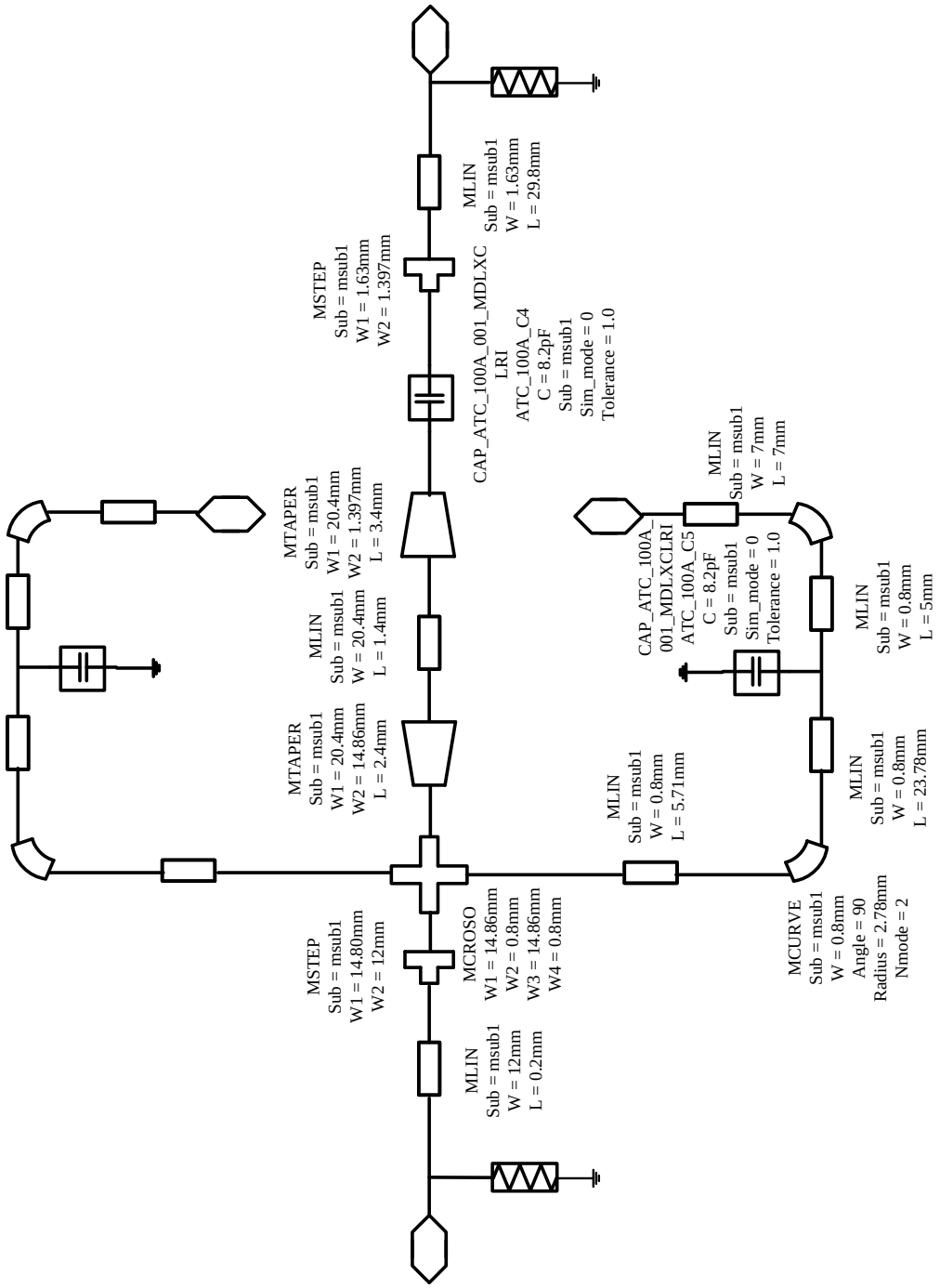

Figure A.5: *Final output matching network with bias lines. The bias lines are symmetrical.*

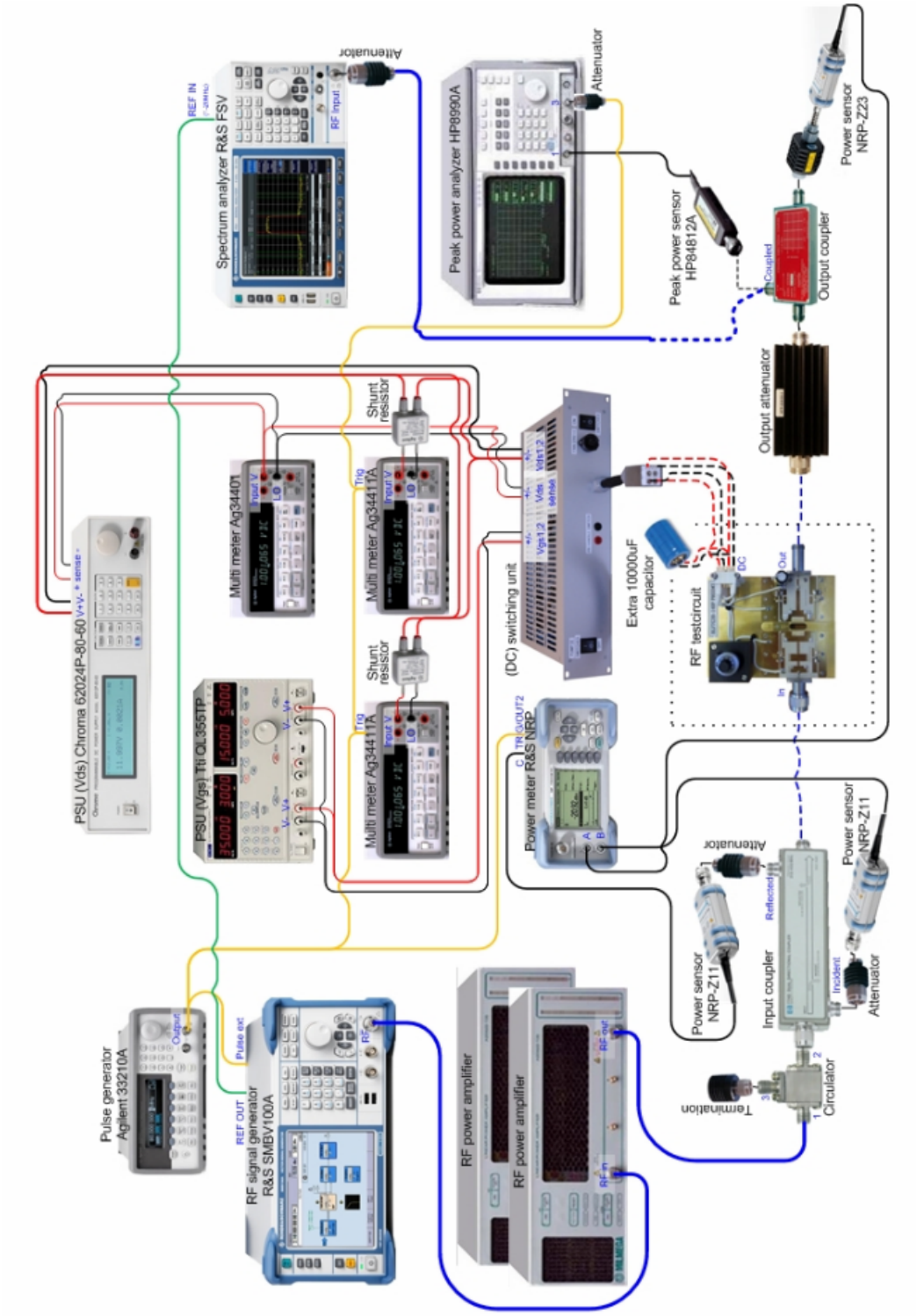

Figure A.6: *Large-signal test bench measurement setup.*