TAMPERE UNIVERSITY OF TECHNOLOGY

HANS HERZOG

HIGH FREQUENCY 65NM CMOS LC OSCILLATORS FOR INDUCTOR QUALITY FACTOR VERIFICATION

Master's thesis

Supervisor: Professor Nikolay T. Tchamov, Ph.D.
Supervisor and thesis subject approved by the Faculty of Computing and Electrical Engineering council on 7th of November 2012.

TIIVISTELMÄ

TAMPEREEN TEKNILLINEN YLIOPISTO
Tietoliikenne-elektroniikan koulutusohjelma
HERZOG, HANS: Korkeataajuisten 65nm CMOS LC oscillaattoreiden käyttö kelojen hyvyysarvon todentamisessa
Diplomityö, 53 sivua, 1 liitesivu
Kesäkuu 2013
Pääaine: Tietoliikennepiirit
Tarkastaja: professori Nikolay T. Tchamov, Ph.D.
Avainsanat: Kela, hyvyysarvo, oskillaattori, CMOS, 65nm, IC, ASIC, RF, piirisuunnittelu

Matalavaihekohinaisten LC-oskillaattoreiden suunnittelussa tarvitaan keloja, joilla on korkea hyvyysarvo. LC-oskillaattoreita käytetään erityisesti langattomien tiedonsiirtolaitteiden lähettimissä ja vastaanottimissa. Radiovastaanottimen vastaanottokyky määräytyy pitkälti vastaanottimessa käytetyn paikallisoskillaattorin tuottaman vaihekohinan mukaan. Nykyaikaisten yhdensirun täysintegroitujen lähetinvastaanottimien kannalta on tärkeää, että käytössä on hyvin mallinnettuja keloja, joilla on korkea hyvyysarvo.

Tässä työssä tutkitaan mahdollisuutta arvioida kelan hyvyysarvoa sen tuottaman vaihekohinan perusteella, silloin kun kelaa käytetään referenssioskillaattorissa. Kelojen testausta varten referenssioskillaattoriksi suunnitellaan differentiaalinen CMOS LC-oskillaattori. Oskillaattori valmistetaan 65nm:n CMOS-prosessilla käyttäen kahta eri kelavedosta, joiden simuloidut hyvyysarvot ovat 7,4 ja 10,2. Molemmat oskillaattorit keloineen ja koetinanturoineen vaativat piille valmistettuna yhteensä 680µm x 510µm -kokoisen alueen sirulta. Oskillointitaajuudet määräytyvät valittujen kelavedosten mukaan: taajuuksiksi mitattiin 3,04GHz ja 4,56GHz. Oskillaattorit tuottavat vaihekohinaa oskillointitaajuksia vastaavasti -125dBc/Hz ja -124dBc/Hz 1MHz:n etäisyydellä ja kuluttavat tehoa 14mW ja 16mW. Kunkin oskillaattorin mitattuun vaihekohinadataan sovitetaan vaihekohinamalli ja mallin toteutuneita sovitusparametreja verrataan toisiinsa. Suunniteltujen kelojen hyvyysarvoiksi saatiin simuloituja arvoja vastaavasti 8,2 ± 0,8 ja 10,8 ± 0,6. Tuloksena todetaan, että mitatut vaihekohinat vastaavat hyvin vaihekohinamallin ennustamia tuloksia ja kelojen hyvyysarvoa voidaan täten, tietyin varauksin, arvioida suhteellisten vaihekohinamittausten kautta.

ABSTRACT

TAMPERE UNIVERSITY OF TECHNOLOGY
Master's Degree Programme in Telecommunication
HERZOG, HANS: High frequency 65nm CMOS LC oscillators for inductor quality factor verification
Master of Science Thesis, 53 pages, 1 Appendix page
June 2013
Major: Communication circuits
Examiner: Professor Nikolay T. Tchamov, Ph.D.
Keywords: Inductor, quality factor, oscillator, CMOS, 65nm, IC, ASIC, RF, circuit design

High quality factor inductors are essential for the design of low phase noise LC oscillators which play an important role in the transceivers of wireless communication devices. The reception capabilities of a radio frequency receiver are to great extent defined by the phase noise performance of the local oscillator. It is therefore important for modern single chip fully integrated transceiver design that high quality inductors are available and well modeled.

In this work we investigate the possibility of evaluating the quality factor of an inductor by the phase noise it generates when used in a reference oscillator. A differential CMOS LC oscillator is designed for inductor test benching. The designed oscillator is fabricated on a 65nm CMOS process with two different inductor designs with simulated quality factors of 7.4 and 10.2. The overall combined silicon area of the two oscillators including inductors and probing pads is 680µm by 510µm. The oscillation frequencies are dictated by the designed inductors and were measured 3.04GHz and 4.56GHz. The oscillators achieve a phase noise of -125dBc/Hz and -124dBc/Hz at 1MHz offset with 14mW and 16mW power dissipation respectively. An oscillator phase noise model is fitted to the measured phase noise data of both oscillators and the model parameters are compared. The received quality factors for the designed inductors are 8.2 ± 0.8 and 10.8 ± 0.6 respectively. It was found that the measured phase noise is in good agreement with the results predicted by the model and the relative quality factor can, with certain limitations, be estimated through relative phase noise measurements.

PREFACE

The work presented in this thesis was done in Tampere, Finland while working for the RF Communication Circuits Laboratory (RFCC) at Tampere University of Technology (TUT). The silicon fabrication for the oscillators designed in this work was sponsored by Infineon Technologies AG. The work itself spawned as a side investigation from an ongoing project with Infineon. As the main project was only a little over a moth from tape-out and the designed oscillators were to be manufactured on the same chip, the time frame for this work from specification to fabrication was very short.

I would like to thank everybody at RFCC for their help and support during the design process, during the measurements and during the writing process of this work. I would also like to thank Infineon for the fabrication opportunity and the Infineon engineers who helped me out with the design tools. And last but not least I thank my family and friends who kept encouraging me to finish this thesis.

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TERMS AND DEFINITIONS

A/D	Analog-to-Digital
BB	Baseband
D/A	Digital-to-Analog
DC	Direct Current
DC-DC	DC to DC converter
DCO	Digitally Controlled Oscillator
FET	Field Effect Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
MIM	Metal Insulator Metal
MOSFET	Metal Oxide Semiconductor FET
PA	Power Amplifier
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
VCO	Voltage Controlled Oscillator
VPP	Vertical Parallel Plate
W/L	MOSFET channel width to length ratio
1L-CMOS	Differential Single-inductor CMOS LC oscillator
2L-NMOS	Differential Two-inductor NMOS LC oscillator
2L-PMOS	Differential Two-inductor PMOS LC oscillator

1 INTRODUCTION

The consumer electronics business is driven by the never ending competition for better performance, higher number of features, lowest power consumption and lowest cost while keeping device size small. The lowest cost is usually achieved via mass production which implies an integrated circuit (IC) implementation. To meet all the requirements for performance and features and still deliver a product that is also small and consuming little power, state of the art integrated circuit technologies with smallest feature size must be used. Who ever adopts the new technology first, has the advantage being the first on the market with the state of the art products.

Adopting a brand new technology is very challenging. Only few device models might exist and modeling accuracy is poor. As the technology matures more process options might become available, device options increase and more accurate models are developed. However, technology maturing takes time and hence early adoption might include taking risks with uncertainty regarding modeling accuracy and actual performance. These experiments might become very expensive, as the development costs on a new integrated process are high. It is not by coincidence that design houses use the phrase “first time success” in their marketing slogans.

A key point for first time design success is modeling accuracy. In this work we focus on the verification of inductor quality factor modeling. High quality factor inductors are essential for the design of low phase noise LC oscillators which play an important role in the transceivers of wireless communication devices [1][2]. The reception capabilities of a radio frequency receiver are to great extent defined by the phase noise performance of the local oscillator. It is therefore important for modern single chip fully integrated transceiver design that high quality inductors are available and well modeled. In this work we investigate the possibility of evaluating the quality factor of an inductor by the phase noise it generates when used in a reference oscillator.

The work is divided into four main parts. First, in Chapter 2 we show the state of the art transceivers and the oscillator topologies used in those transceivers. In Chapter 3 we re-express a known phase noise model by externally measurable quantities. The model will be used as a tool for inductor quality factor estimation. Next, in Chapters 4, 5 and 6 we design and simulate two oscillators with different inductors to be measured. Finally, in Chapter 6 we put the derived model under test and estimate the quality factors of the used inductors through the measured phase noises of the oscillators.

2 STATE OF THE ART

This chapter shows the state of the art transceiver architectures used in modern wireless communication devices and that the oscillator plays a central role in all these transceiver topologies. Although there are several ways to realize an oscillator, not all can satisfy the performance requirements imposed by nowadays transceivers. The industry developments have shown that differential LC oscillators are best suited for today's requirements. We compare the most commonly used LC oscillator topologies and the inductors used in these oscillators.

2.1 Wireless transceiver architectures

Oscillators are used, for example, in transceivers for up and down conversion of signals. Considering receivers first, the oscillator has a certain frequency of oscillation which is usually close to the frequency of the radio frequency (RF) signal to be received. When the oscillator signal is mixed together with the received signal from the antenna, the resultant signal includes a component that has very low frequency. This frequency is called the intermediate frequency (IF) signal or baseband (BB) signal depending on the receiver architecture. The low frequency signal is now much easier to process for the following receiver blocks than the high frequency RF signal. This basic concept is still valid in today's modern receivers.

In addition to the oscillator a transceiver needs a selection of other blocks to function. Typical receiver blocks are, starting from the antenna, a low noise amplifier (LNA) to boost the antenna incident signals, a mixer together with a local oscillator (LO) for frequency down conversion, image rejection and channel selection filters to filter out undesired components and select the wanted channel, a programmable gain amplifier (PGA) to adjust the signal level for the following processing blocks and finally the analog-to-digital (A/D) conversion block. For decades the dominating receiver architecture was the Superheterodyne receiver architecture, but its short comings in low integration level (mainly due to the need for high-Q off-chip channel selection and image rejection filters) and high power consumption for the on/off-chip buffering have lead to more modern designs.

Figure 2.1 below shows a zero-intermediate-frequency (zero-IF) receiver architecture, which removes the need for any off-chip components. The desired signal is translated directly down to the baseband and the image is eliminated through signal cancellation rather than filtering. Since the image is the desired channel itself, the demanded I/Q matching is practically achievable for most applications. The fundamental limitation of

the zero-IF receiver is its high sensitivity to low-frequency interference, i.e., dc-offset and 1/f noise. [2]

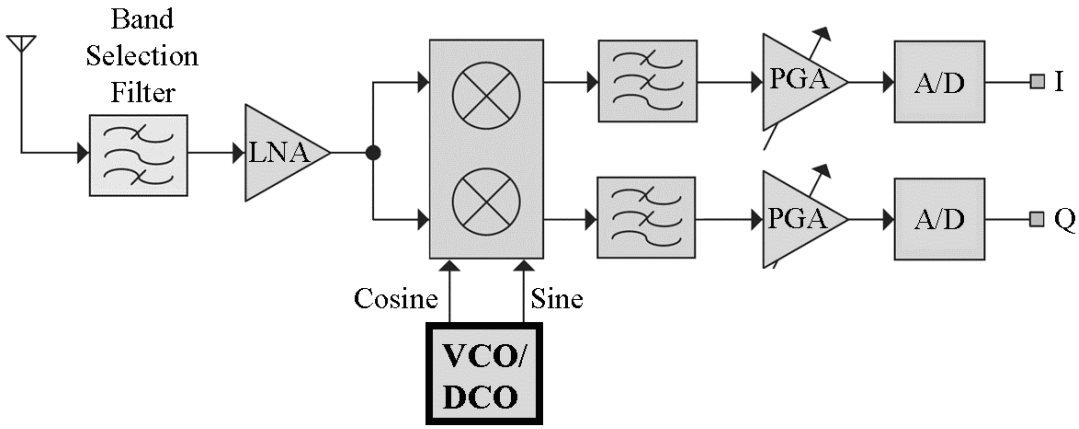

Figure 2.1. *The direct conversion receiver topology employs an oscillator to down convert radio frequency (RF) signals from the antenna directly to baseband.*

The low-intermediate-frequency (low-IF) receiver features similar integratability as the zero-IF one but is less susceptible to low-frequency interference. The desired channel is down converted to a very low-frequency bin around DC, typically ranging from a half to a few channel spacings. Unlike the zero-IF receiver, the image is not the desired channel itself. The required image rejection is normally higher as the power of the image can be significantly larger than that of the desired channel. A low-IF receiver can be realized in multiple different ways, one of which is shown in Figure 2.2. The shown architecture positions an analog IF-to-BB down converter prior to the analog-to-digital converters (A/D) so that the conversion rate of the A/Ds can be minimized. Comparing with the zero-IF receiver, the low-IF receiver is less sensitive to 1/f noise and DC-offset at the expense of a higher image-rejection requirement. [2]

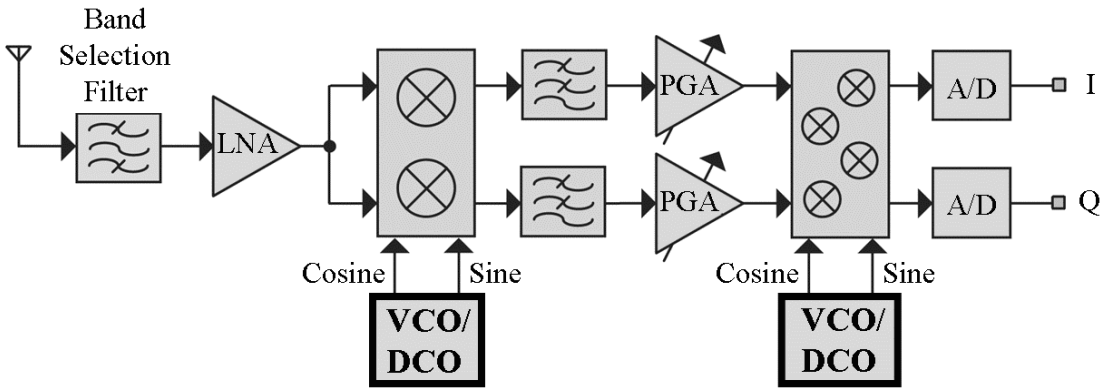

Figure 2.2. *The low-intermediate-frequency (IF) receiver topology employs two kinds of oscillators; the first high frequency oscillator down converts radio frequency (RF) signals from the antenna to IF and the second oscillator converts the low frequency IF signal to baseband.*

Architecturally, transmitters are essentially performing the reverse operation of their receiver counterparts with the A/D conversion replaced by a digital-to-analog (D/A) conversion and LNAs replaced by power amplifiers (PA). However, they are very different in the design specification. For instance, in transmission, only one channel will be up converted in the transmitter. The power levels of a transmitter are well determined throughout the transmitter path, whereas in receivers the power of the incoming signals is variable and the desired channel is surrounded with numerous unknown-power in-band and out-of-band interferences. Thus, PGAs are essential for receivers to relax the dynamic range of the A/D converter, but can be omitted in the transmitter if the power control could be fully implemented by the PA. Similarly, since the channel in the transmitter is progressively amplified toward the antenna and finally radiated by a PA, the linearity that ensures spectral purity of the whole transmitter is dominated by the PA. Whereas it is the noise contribution of the LNA that dominates the noise figure of a receiver. [2]

The direct-up transmitter in Figure 2.3 features equal integratability as the zero-IF receiver, but is limited by the well-known local oscillator (LO) pulling. LO pulling is caused by high power cross-talk from the on-chip PA being injected back into the oscillator causing oscillator spectral impurities and frequency shift towards the PA output frequency. To meet the standard required modulation mask, techniques such as offset VCOs and LO-leakage calibration are necessary. Again, it is noteworthy that although the functional blocks in the receiver and transmitter are identical, their design specifications are largely different. For instance, the receiver's low-pass-filter (LPF) has to feature a high out-of-band linearity due to the co-existence of adjacent channels, whereas it is not demanded from receivers LPF. [2]

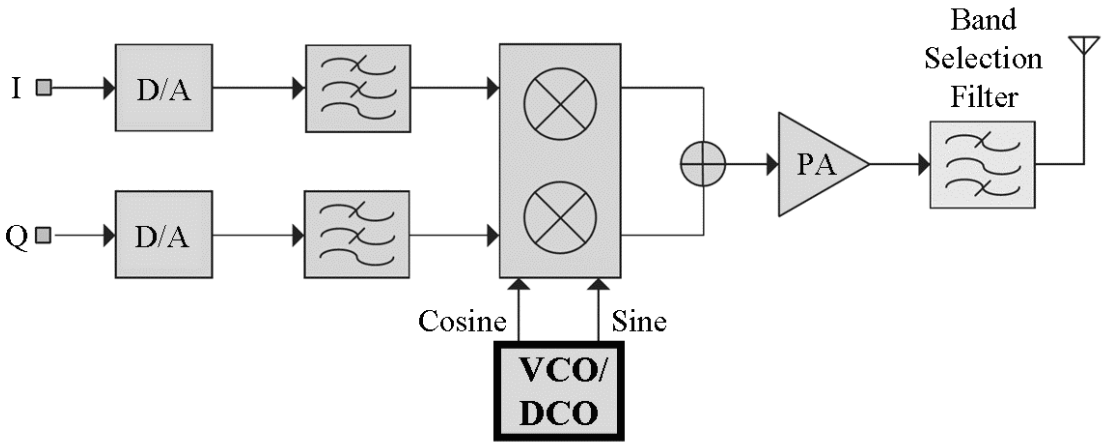

Figure 2.3. *The direct-up transmitter employs an oscillator to up convert the baseband signal directly to radio frequency (RF).*

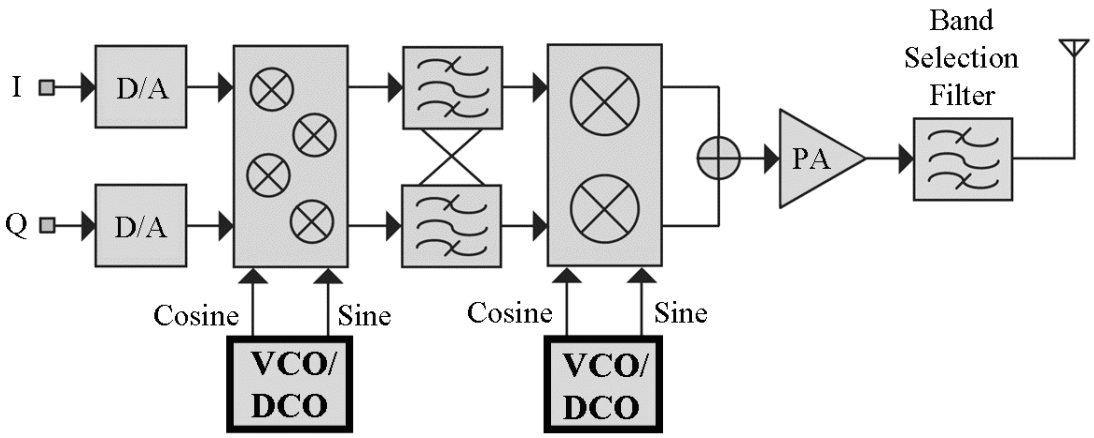

Figure 2.4. *The two-step-up transmitter employs two kinds of oscillators; the first low frequency oscillator up converts the baseband signal to intermediate frequency (IF) and the second high frequency oscillator up converts the IF signal to radio frequency (RF).*

Similar to the low-IF receiver, two-step-up transmitters can be structured into multiple different ways. The two-step-up transmitter in Figure 2.4 locates the analog BB-to-IF up converter between the D/A converter and complex filters, delivering doubled image rejection and allowing a capacitive coupling between the up converter and filter, and between the filter and IF-to-RF up converter. One key advantage of this scheme is the allowance of independent DC-biasing for each block. Compared with the direct-up transmitter, the LO feed through is reduced (of course, the amount depends on the selected IF and port-to-port isolation) as the first and second VCOs can be offset from each other i.e. the final LO signal is generated as a mixing product of two VCOs. The overheads are the additional power and area consumption required for the mixing, filtering and frequency synthesis. [2]

2.2 Oscillator topologies in modern transceivers

There are several different ways to realize oscillators. Usually the frequency of an oscillator needs to be tunable in order to receive (or transmit on) different channels. The oscillation frequency is typically controlled either by an analog voltage (VCO) or a digital control word (DCO). The most important parameters of an oscillator are its phase noise performance, tuning range, power consumption and consumed silicon area. Phase noise is a measure of the short term instability of the oscillator's frequency of oscillation. It is the most important parameter of the receiver's oscillator defining to great extent the reception sensitivity and channel selectivity of the receiver. Phase noise will be discussed more in detail throughout this work.

Figure 2.5 shows three state of the art low phase noise oscillator topologies typically used in the low-GHz to high-GHz range wireless transceiver applications [3]: (a) Top-biased 2L-PMOS oscillator with top filtering, (b) Top-biased 2L-NMOS oscillator with bottom filtering and (c) Top-biased 1L-CMOS oscillator with top and bottom filtering.

The common nominator of the shown oscillators is that they are all differential LC oscillators built using CMOS technology. All three oscillator types employ differential pairs formed by either NMOS or PMOS or both types of transistors for producing gain. The differential topology is well suited for integration due to its differential layout and common mode interference rejection capability [4]. The MOS transistor based structure makes the circuit suitable for fabrication on the standard CMOS processes.

The positive feedback is provided by the resonance tank formed by C_0 and L_0. The resonance tanks capacitance C_0 typically consists of a bank of capacitors and voltage tuned capacitors called *varactors*. The varactors are typically built from MOS transistors. Depending on the tuning method the capacitors and varactors are switched either by an analog voltage (VCO) or digital control word (DCO). All the shown oscillators are top-biased, since this way the oscillator is more immune to substrate noise because the current source is placed in an n-well, rather than in the substrate [5].

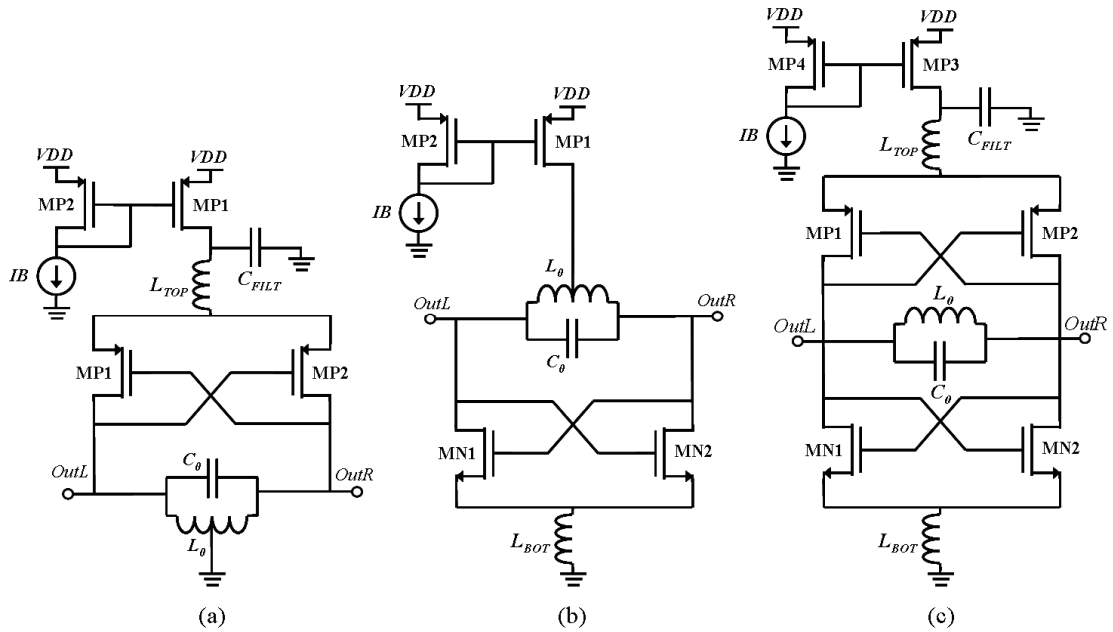

Figure 2.5. *Three state of the art oscillator topologies: (a) Top-biased 2L-PMOS oscillator with top filtering, (b) Top-biased 2L-NMOS oscillator with bottom filtering and (c) Top-biased 1L-CMOS oscillator with top and bottom filtering.*

Going into the specifics of the three shown oscillators, the main difference between the 2L and 1L topologies is the needed voltage supply *VDD* and bias current *IB*. The 2L topologies can operate with smaller supply voltages but require a larger bias current to produce the same voltage swing as the 1L topology having two differential pair gain stages. The over all power consumption of both topologies is approximately equal and they typically achieve approximately equal phase noise performance. [3]

Figure 2.6 below shows an example of the importance of good oscillator phase noise performance. Considering that a practical oscillator signal exhibits power spectral density with bell-like shape, and the receiver (such as the low-IF receiver in Figure 2.2)

incident signals are mixed with this oscillator signal, the product of the mixing will have a bell like shape as well. In practice this means that in addition to the desired signal the oscillator may down convert undesired interferers which are in the vicinity of the desired signal. These interferers will degrade the carrier to noise ratio (CNR) observed at the intermediate frequency and impose reception problems. Phase noise will be discussed more in detail throughout the work.

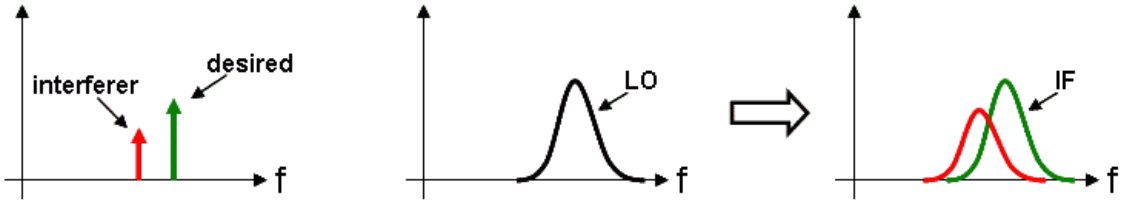

Figure 2.6. *The phase noise of the first oscillator of a low intermediate frequency (IF) receiver can cause poor carrier to noise ratio (CNR) at IF when the desired signal has an interferer at close offset.*

In the shown LC oscillator topologies, phase noise is formed by the up conversion of the noise created in the channels of the active devices and in the series resistance of the resonator [6]. The up conversion can be understood by considering an ideal oscillator that has a stable oscillation period i.e. the signal crosses zero at a fixed point. If noise is added to the oscillators signal, the zero crossing point becomes time variant creating frequencies around the ideal oscillation frequency. This translates into a bell-like spectral density of the oscillator signal as shown in Figure 2.6. In other words, the real oscillator acts as an up/down converting mixer for noise.

It has been shown that in LC oscillators the noise around the second harmonic of the oscillation frequency is one of the largest contributors to phase noise (higher harmonics are filtered by the LC-resonator) [5][6]. In the 2L-PMOS and 1L-CMOS oscillators a large capacitor in parallel with the current source shunts noise frequencies around the second harmonic to ground. However, a filter inductor must be inserted at the common source point of the differential pairs to resonate in parallel with the capacitance at that node. This blocks second-harmonic current from flowing through the grounded junction capacitors comprising the resonator, and through the switching FETs to ground. The produced high impedance at the tail node also prevents resonance tank quality factor degradation by loading from the active devices entering triode region. [5]

As described in [5], even the state of the art filtering techniques shown here do not remove the requirement for a high quality factor resonator when targeting good LC oscillator phase noise performance. The quality factor of an LC-resonator is typically dominated by the low quality factor of the inductor when considering CMOS processes. This topic is discussed in the next chapter.

2.3 On-chip inductors in LC oscillators

The integrated inductor has become a commonly used passive component in high-frequency oscillator topologies. Although the quality factors of on chip inductors have always been modest, the trend towards smaller feature sizes imposes further limits to these already low in quality factor values. One major quality factor limit is imposed by the high conductivity substrates of deep sub-micron technologies [7]. This has lead to different system-in-package (SiP) solutions where the inductor is manufactured into the chip package instead of the chip itself [8][9]. Due to the complexity of such solutions, it might be difficult to estimate the actual quality factor of the designed inductor, which also justifies inductor verification using oscillators.

Table 2.1 shows a list of inductor used in recent VCO publications. The last row shows the used topology using the same naming convention as in the previous chapter. The inductor in [8] was made using integrated passive device (IPD) thin-film technology which allows high quality inductors and filters to be fabricated in-package. The work in [9] uses an inductor in an embedded wafer level ball-grid-array (eWLB) package. The work in [10] compares the VCO performance when using an on-chip inductor versus the case of an external flip-chip connected inductor, the on-chip square shaped inductor displays typical low quality factor even though the process feature size is quite high. The octagonal on-chip inductor presented in [11] demonstrates a typical good on silicon inductor with a modest simulated quality factor of 12.8. On the other side, the inductor shown in [12] acts as a good example of the more rarely used 8-shaped inductor, which typically features a low quality factor due to long trace length. Employing 8-shaped coils in LC-VCOs has been recently invoked mainly due to their low magnetic coupling characteristics against LO pulling. The good quality factor of the inductor in [12] can be partly explained by the better substrate resistance of the BiCMOS process.

Table 2.1. *List of inductors in recent VCO publications.*

	[10]	**[12]**	**[8]**	**[9]**	**[11]**
Year	2012	2010	2011	2011	2011
CMOS Process	0.35µm	0.25µm*	0.18µm	65nm	0.18µm
Technology	On-chip	On-chip	IPD	WLB	On-chip
Inductor shape	Square	8-shape	Octagonal	Octagonal	Octagonal
L	5.0nH	0.95nH	0.6nH	1.2nH	2.0nH
Q at F	5.1	25	>20	28	12.8
F	2.45GHz	3.8GHz	5.76GHz	6.5GHz	2GHz
VCO topology	1L-CMOS	2L-NMOS	1L-CMOS	2L-NMOS	2L-NMOS

*BiCMOS

On chip inductors are predominantly realized as planar spirals or concentric-ring structures with a hollow middle. Usually the top most metal is used for inductor windings due to its largest distance from the substrate and because it typically features the

highest conductivity due to largest thickness. Additional metal layers may be needed for creating underpasses or symmetrical inductors. Most widely used inductor shapes are octagonal and rectangular. Figure 2.7 below shows an example of a differential rectangular and differential octagonal inductor. Despite its naturally high quality factor, the approximation of circular shape is less often used due to photolithography limitations. The major concern about inductors implemented on silicon is the low quality factor caused by high substrate losses, low conductivity of metal interconnects (aluminum-copper is typically used) and thin metal layers. [13]

When operating on high frequencies, the inductors quality factor is affected by additional factors such as skin effect and the proximity effect, which are discussed later. Given all the mentioned factors the typical maximum quality factor obtained for an integrated inductor lies between 10 and 20 [14][15]. Practically obtainable inductance values on chip range from 0.1 to 20nH. The quality factor of an inductor is typically expressed through its impedance:

$$Q = \left| \frac{\mathrm{Im}\{Z_{ind}\}}{\mathrm{Re}\{Z_{ind}\}} \right| \tag{1}$$

where the imaginary part of the inductors total impedance describes the energy stored into the magnetic field of the inductor and the real part the ohmic losses of the inductor.

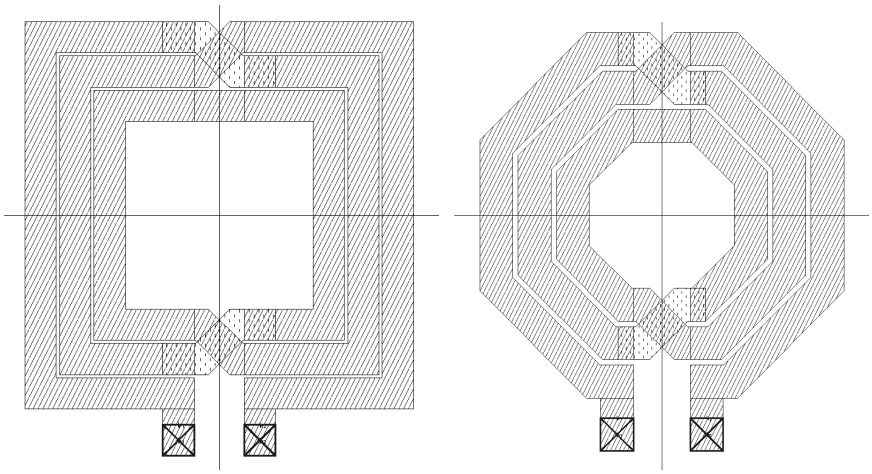

Figure 2.7. *Most common inductor shapes for on-chip inductors are rectangular and octagonal. Both inductors shown here have differential layout.*

The parameters of an inductor including the various effects on quality factor can be described using a lumped-element circuit model such as the popular single-π inductor model [14] shown in Figure 2.8. In this model L_s and R_s model the inductance and series resistance caused by the winding and interconnects, C_s models the total inter-winding capacitance i.e. the capacitance between the individual turns of the inductor, C_{ox} is the capacitance between the inductor and the top of the substrate and C_{sub} and R_{sub} are the substrate capacitance and resistance respectively. As more turns are added to the inductor the produced magnetic field and inductance increases. On the other hand, more

turns also increase series resistance and surface area which relates to substrate capacitance.

Substrate losses are caused by part of the useful signal being coupled to the substrate i.e. energy is lost instead of stored in the inductor. Both capacitive and inductive substrate losses exist. Inductive substrate loss happens by induced swirl currents (eddy-currents) running through the substrate resistance and can be extensive if substrate resistivity is low. Since even symmetrically designed inductors are usually not perfectly symmetric (e.g. due to underpasses) the substrate related model components are divided for both terminals.

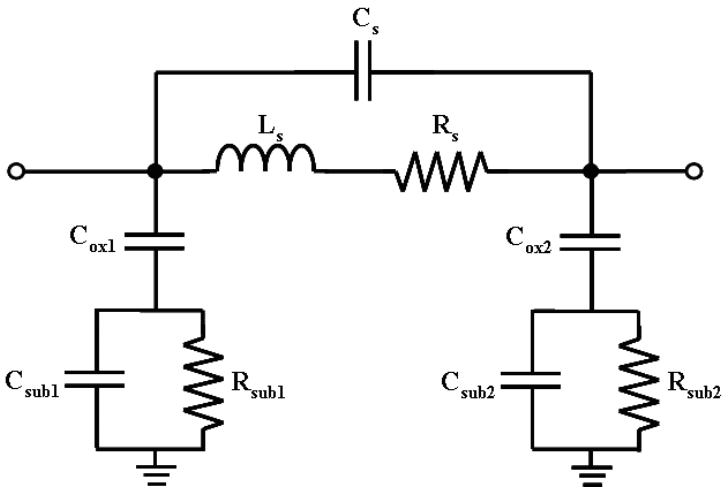

Figure 2.8. *Single-π inductor circuit model.*

Each of the lumped-element model components accounts for a physical parameter of the inductor and the quality factor is a sum of these parameters. It is important to note that changing one physical property usually affects many components of the lumped model. For example in order to lower the series resistance of an inductor, multiple shunted metal layers can be used for the inductor windings. This lowers the series resistance but increases substrate capacitance. The maximum Q value is increased and the frequency of maximum Q and the self-resonance frequency are decreased. The self resonance frequency is the frequency where the inductors inductance and parasitic capacitances become equal i.e. the reactance is zero. At frequencies higher than the resonance frequency the inductor acts as a (low quality factor) capacitor.

As discussed earlier, additional losses become apparent at high frequencies. Skin effect is caused by the internal magnetic field of the inductor which moves the current flow towards the outer edges of the conductor. The current has hence a narrower path to move along which translates into a higher series resistance and more dissipated energy. As operating frequency increases further, the magnetic field from the neighboring conductor starts to push the current towards the inner edge of the conductor causing current crowding. This is described as the proximity effect and has a greater impact than the skin effect on the increase of resistance and degradation of in present-day spiral inductor designs. These high frequency effects are not modeled in the single-π inductor model, but more complex models have been developed to incorporate these effects. [15]

3 INDUCTOR TESTING USING OSCILLATORS

In this chapter we show the differential single-inductor CMOS LC oscillator (1L-CMOS) specific theory, we define phase noise and show Leeson's model for phase noise, together with the 1L-CMOS specific parameters. Finally, we express the 1L-CMOS specific phase noise model with help of externally measurable quantities and summarize the obtained results.

3.1 Differential CMOS LC oscillator

The oscillator used in this work is a simple version of the differential single-inductor CMOS LC oscillator [17][18]. This design was chosen, because it does not limit the inductor choice to center-tapped inductors and it can be easily implemented on a CMOS process. One of the main parameters for the oscillator in this work is simplicity – the oscillator performance should be affected as little as possible by anything else except the inductor under test. Using a current mirror would create extra noise which would require filtering. On the other hand, the available silicon area is insufficient for filter inductors. Due to this and in order to reduce design variables the oscillator does not utilize top- nor tail biasing. Also the voltage control using varactors was omitted.

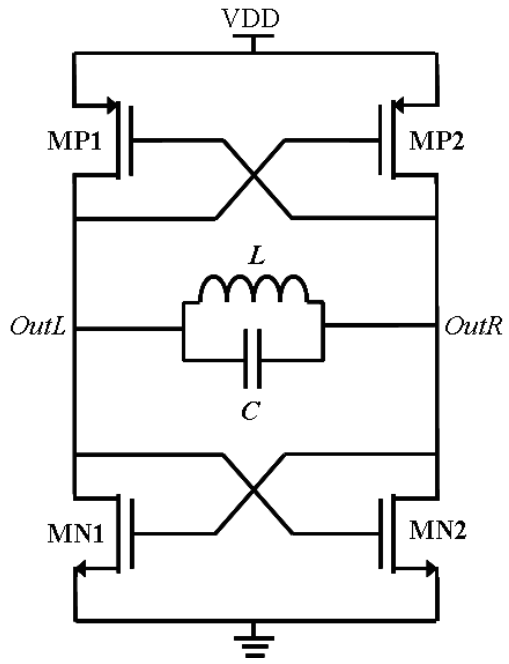

Figure 3.1 *Simple differential 1L-CMOS LC oscillator for inductor evaluation.*

In the case of LC oscillators the gain needed for oscillations is provided by a negative transconductance stage and the positive feedback path is made frequency selective by an LC tank. A simple steady-state LC oscillator model is shown in Figure 3.2. The losses of the LC tank are modeled by R_{eq}. The oscillation frequency of the LC oscillator is equal to the resonance frequency of the LC tank and is given by the well known Thomson formula:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2}$$

However, in practical oscillators the oscillation frequency may be lower; this is discussed in the next chapter.

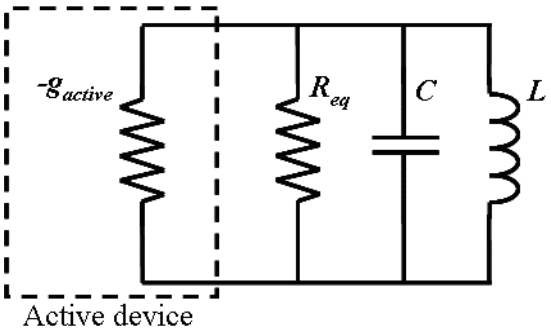

Figure 3.2. *Steady-state LC Oscillator model.*

The gain to overcome the losses in the tank and achieve oscillations is provided in the 1L-CMOS topology via the NMOS and PMOS total average transconductance. The gain requirement is hence:

$$\left|-g_{active}\right| \geq \frac{1}{R_{eq}} \tag{3}$$

This means that in steady-state the transconductance provides an average negative resistance which has an absolute value that can overcome the loss R_{eq} of the resonance tank. Start-up requires the loop gain to be higher than unity and steady-state output requires nonlinear characteristics of the loop gain. Resonators are considerably linear so the non-linearity stems from the gain stage.

As the differential output voltage over the LC tank swings between positive to negative voltage the current through the tank reverses. When the output voltage is at its maximum or minimum all of the supply current I_{tail} is flowing through the LC tank in one direction. Hence the oscillator can be modeled as an RLC tank with a current source $i(t)$ switching between I_{tail} and $-I_{tail}$. The model is shown in Figure 3.3. The waveform of $i(t)$ depends on the transistor switching time and gain which can be limited at high oscillation frequencies. [17]

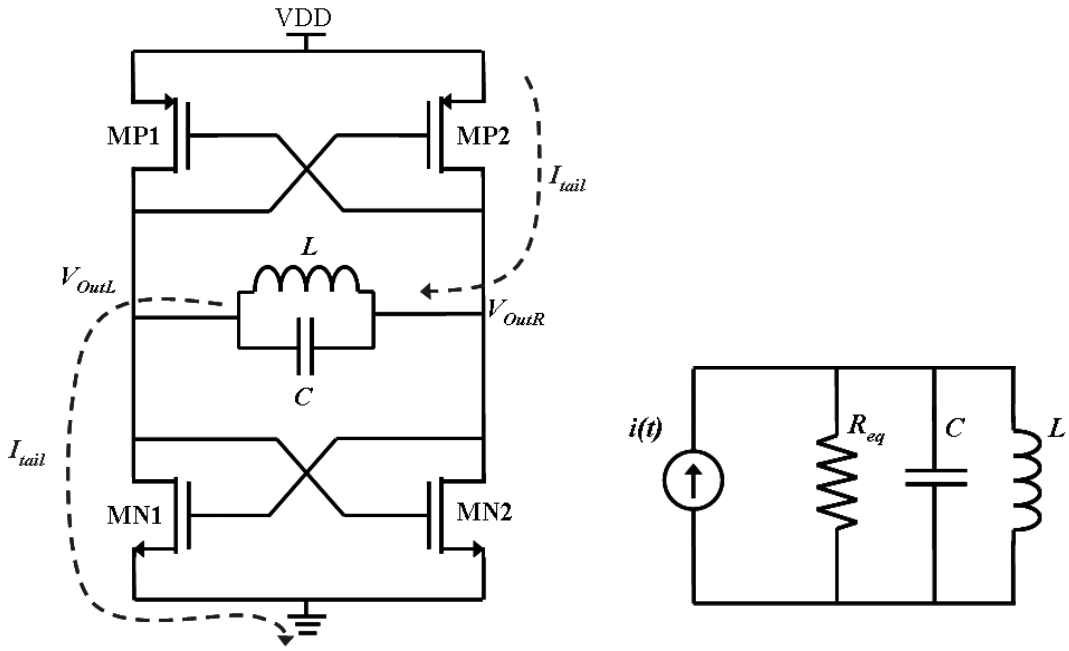

Figure 3.3 *Differential LC oscillator and its equivalent model.*

At the resonance frequency of the RLC tank the admittances of L and C cancel out leaving only R_{eq}. If the transistor gains are high and the tail current is "hard switched" i.e. the current waveform assumes a rectangular shape, then the tank voltage is expressed as:

$$V_{tank} = \frac{4}{\pi} I_{tail} R_{eq} \tag{4}$$

It should be noted that the rectangular current waveform contains harmonics which are filtered by the LC tank producing a near sinusoidal voltage waveform. The tanks capacitor presents low impedance for these harmonics and consumes them. In order to compensate for the energy imbalance between the capacitor and inductor the oscillation frequency must shift down. The frequency shift $\Delta\omega$ is equal to:

$$\frac{\Delta\omega}{\omega_0} = \frac{1}{2Q^2} \sum_{n=2}^{\infty} \frac{n^2\left(1-n^2\right)}{\left(1-n^2\right)^2 + n^2/Q^2} \cdot m_n^2 \tag{5}$$

Where Q is the quality factor of the tank and m_n is the normalized level of the n^{th} harmonic. $\Delta\omega$ is the sum of all negative terms, which means oscillation frequency shifts down with more harmonic content. [6]

If the oscillation frequency is high enough so that the drain current waveform resembles a sinusoid the oscillator is said to be in the "current limited" region of operation.

$$V_{tank} \approx I_{tail} R_{eq} \tag{6}$$

This relation is valid only as far as the NMOS and PMOS pairs are not entering triode region due to limited supply voltage. [17]

3.2 Quality factor estimation through phase noise

Short-time instability in the phase of the signal is described in terms of phase noise. It can be observed as noise modulated phase $\varphi(t)$ of the oscillator signal:

$$v_{OSC}(t) = A_{OSC}\cos\left(2\pi f_{OSC}t + \varphi(t)\right) \tag{7}$$

The change of phase yields a respective change of oscillation period duration (jitter in time domain) i.e. the oscillation frequency changes every time a change in phase occurs. The phase noise process leads to a bell-like shape of the power spectral density, instead of an ideal impulse in frequency domain.

The ratio of the power P_{SB} within a single-Hz wide sideband f_{offset} away from the carrier versus the power P_{fund} in the carrier measures the spectral purity of the oscillator. The measure of spectral purity is called phase noise and expressed as:

$$L(f_{offset}) = \frac{P_{SB}}{P_{fund}} = P_{SB,dB} - P_{fund,dB}[dBc/Hz] \tag{8}$$

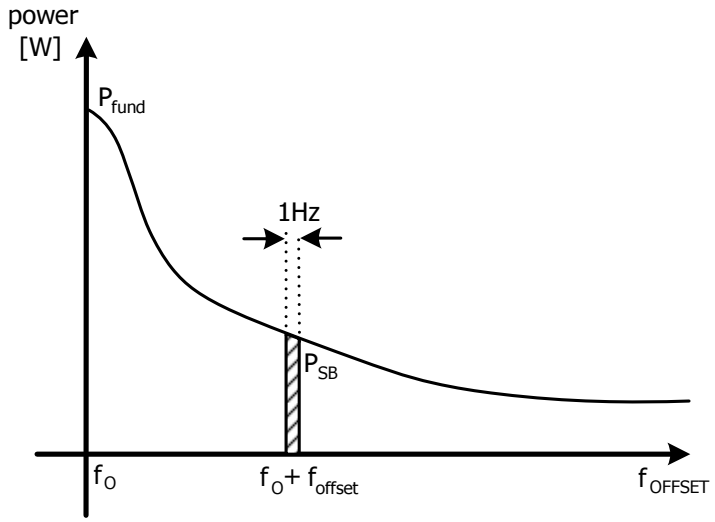

Figure 3.4. *Phase noise is measured in a single-Hz band relative to the carrier.*

Usually several noise contributions add to the rise of phase noise. They can also be distinguished in the spectrum. The region closest to the fundamental oscillation frequency is the *1/f³ region*, the name describing the relationship of the noise on offset frequency. This noise is caused by the up conversion of *flicker noise* produced in field effect transistors. Flicker noise is hence very visible in CMOS designs, but not a big

problem in bipolar VCOs. Next in frequency is the *1/f² region*, which is caused by the thermal noise within the oscillator i.e. the resonator loss and finally the *thermal noise floor*, which is due to thermal noise of circuits connecting to the oscillator.

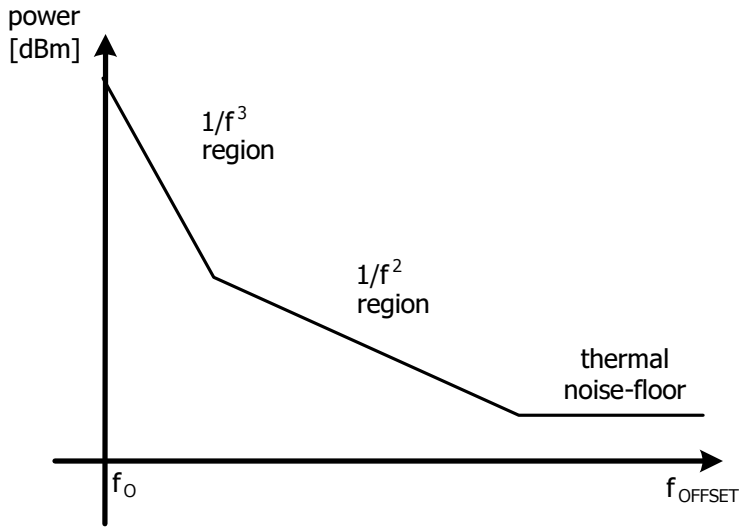

Figure 3.5. *Three regions of phase noise included in Leeson's phase noise model.*

D. B. Leeson published one of the most famous phase noise models in 1966 [20]. Leeson's model includes the mentioned above three regions. Leeson's model for phase noise:

$$L(\Delta\omega) = 10 \cdot \log\left\{\frac{2FkT}{P_{sig}} \cdot \left[1 + \left(\frac{\omega_0}{2Q_{tank}\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{9}$$

Where F is the oscillator noise factor, an empirical fitting parameter that usually needs to be measured, k is the Boltzmann constant, $\Delta\omega_{1/f3}$ is the frequency offset that separates the $1/f^3$ and $1/f^2$ regions (also often a non-deterministic fitting parameter) and Q_{tank} is the loaded quality factor of the resonator tank.

From this model, it can be concluded that the loaded quality factor of the tank needs to be maximized to reduce phase noise. The integration of a high Q tank is not easy because of the low resistivity of silicon substrate. Also, the voltage swing across the resonator needs to be maximized while minimizing the duration in the triode region of the switching transistor. Additional factors affecting phase noise are the frequency tuning arrangement and layout. [18]

Although the noise factor F is typically an empirical fitting parameter, design parameter dependent expressions have been developed. According to [21] the minimum noise factor for a differential CMOS LC oscillator can be expressed as:

$$F_{\min} = 1 + \gamma \tag{10}$$

where γ is the noise factor of a single FET, classically 2/3 for long channel devices [19][6]. The equation assumes hard switched current and equal noise factors for the PMOS and NMOS devices. If the device noise factors are not equal the averaged value of both is a good approximation. This expression for the minimum noise factor can only be obtained if the tank capacitance appears only between the output terminals. Capacitance, parasitic or otherwise, from the output terminals to ground offers a path for high frequency noise in the PMOS devices and this can degrade the phase noise factor significantly. [21]

The actual noise factor of the differential CMOS LC oscillator shown here is influenced by loading, the loading is caused by the time varying conductance of the core transistors as modeled in Figure 3.6. The resulting expression for the loaded noise factor is:

$$F = (1+\gamma)(1+G_{DS}R_{eq}) \tag{11}$$

where G_{DS} is the combined effective conductance responsible of loading the tank and R_{eq} is the equivalent parallel resistance of the tank. Since the loaded noise factor takes tank loading into account, the loaded quality factor in (9) can be replaced by the unloaded quality factor. [21]

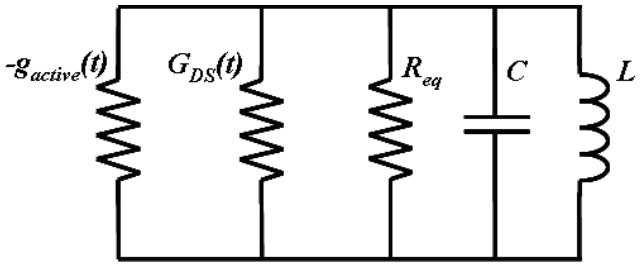

Figure 3.6. *Oscillator equivalent model including tank loading by G_{DS}.*

As discussed before, the oscillator's resonance tank can be modeled as a simple RLC-tank as shown in Figure 3.3. The quality factor of a simple parallel RLC-tank can be expressed as:

$$Q_{tank} = R_{eq}\sqrt{\frac{C}{L}} \tag{12}$$

Solving the equation for R_{eq} and inserting the result into (11) yields:

$$F = (1+\gamma)\left(1+G_{DS}Q_{tank}\left(\frac{C}{L}\right)^{-\frac{1}{2}}\right) \tag{13}$$

In this tank it is assumed that L is the simulated inductance of the inductor at the oscillation frequency, C is the capacitor bank total capacitance including parasitic wiring capacitance at oscillation frequency.

Since G_{DS} is the combined effective conductance loading R_{eq}, G_{DS} can be thought as the total voltage needed to produce I_{tail}. Also, in order to express G_{DS} we need to use an effective tank voltage. Assuming V_{tank} is nearly sinusoidal, we use $V_{tank}/\sqrt{2}$ to represent its effective value, giving G_{DS} the form:

$$G_{DS} = \frac{I_{tail}}{V_{DD} - V_{tank}/\sqrt{2}} \tag{14}$$

where V_{tank} can be expressed with the help of I_{tail} and Q_{tank}.

Assuming that the designed capacitor bank and the parasitic capacitances can be reliably modeled and looking at Leeson's phase noise model in (9), we can see that we have now expressed all Leeson's model variables by known or externally measurable quantities. The signal power P_{sig} is assumed equal to $V_{tank} \cdot I_{tail}$. The remaining fitting parameters are L, $\Delta\omega_{1/f3}$ and Q_{tank}. The inductance of the inductor can be estimated from the measured oscillating frequency, taking into account a possible frequency shift due to tail current harmonics. The 1/f border offset frequency $\Delta\omega_{1/f3}$ can be visually estimated from the measured phase noise plot, where the phase noise turns from a -30dB/dec slope to -20dB/dec. This leaves Q_{tank} as the only real fitting parameter.

Taking the analysis further, if we can reliably characterize the oscillators capacitor bank together with the parasitic capacitances so that we know their total quality factor, we can solve the inductors quality factor by knowing that [1]:

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{15}$$

where Q_L is the quality factor of the inductor and Q_C is the total quality factor of the capacitor bank and parasitic capacitance. It is important to note that the analysis method shown so far allows the empirical characterization of the inductor only at the oscillation frequency it produces. Since the final oscillation frequency depends on the designed inductor, the capacitor bank must be characterized for a frequency range that covers the final oscillation frequency of the oscillator under test. In other words, in order to use (15) the capacitors quality factor should be known at the frequency that is produced by the inductor under test. Also, in order to characterize and inductor at a certain specific frequency the capacitor value must be chosen so that the oscillation frequency falls into this frequency. In this case the inductance value of the inductor under test must be known.

3.3 Summary of conclusions

To summarize the conclusions of this work so far, we can say that the differential LC type oscillators are the main topology used in today's transceiver applications due to their superior phase noise performance. The quality factor of the used inductor is a major parameter in defining the phase noise performance of these modern LC VCOs. Hence, the differential LC type of oscillator is a suitable vessel for testing not only inductor quality factor, but also to directly see the phase noise impact of a certain designed inductor versus other inductors.

As the VCO core continues to become smaller with decreasing feature sizes of the bulk CMOS process, the inductor quality factor suffers from the high substrate conductivity of the deep sub-micron process. This has partially led to system-in-package (SiP) inductor solutions which can impose new difficulties for reliable inductor modeling. Both, the difficulty of implementing high-Q on-chip inductors and the modeling uncertainty of new inductor technologies justify the need for quality factor verification.

Verifying inductor quality factor is important also from the point of view of other high-Q inductor applications such as filters or integrated direct-current-to-direct-current (DC-DC) converters.

The quality factor verification method shown here is conducted by first designing a differential LC oscillator and characterizing its capacitor bank. Next, a reference inductor is placed into one of these oscillators and a new inductor design in another. Both oscillators are manufactured and measured. The measured phase noise plot of the known inductor is fitted with a phase noise model expressed by the active device noise factor, tank quality factor and externally measurable parameters (mainly oscillation frequency, supply voltage and bias current). Keeping the device noise factor constant, the model is fitted to the oscillator under measurement by changing only the externally measurable parameters and using the tank quality factor as a fitting parameter. The inductor quality factor can now be calculated, by knowing the quality factor of the tank capacitor.

4 ELECTRICAL DESIGN

The design was divided into the following modules: The oscillator core, which consists of the active NMOS and PMOS gain stages; capacitor bank; output buffer; open drain stage. These modules were combined to form the oscillator without the inductor. The inductor constituted for its own top-level module. This enables quick implementation of several oscillators by simply changing the inductor. In this work two oscillators are fabricated. The oscillator schematic is shown in Figure 4.1. Due to the limited silicon area there was not enough space to fit the output pads for the differential outputs of both oscillators, hence the decision was made to ground the second open-drain stage of both oscillators and measure the oscillators by single-ended output. This choice makes the oscillator more vulnerable to supply noise, and will be taken into account during measurements.

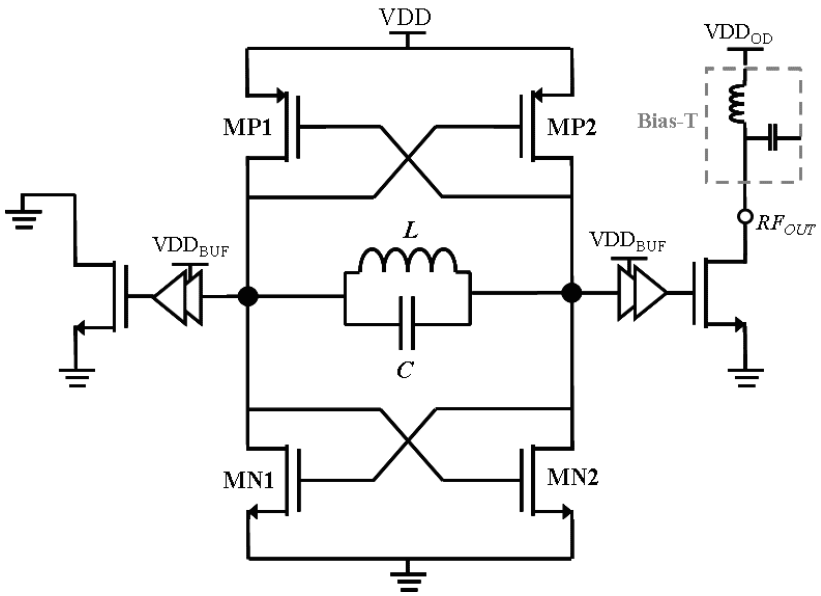

Figure 4.1 *Differential CMOS LC oscillator with CMOS inverter buffers and single-ended open-drain output.*

Figure 4.2 shows how the chip containing the two designed oscillators will be interfaced. Both oscillators will have their individual core supply pad, but joint buffer supply. The output from the open-drain stage will be taken through a bias-t block providing also the supply voltage for the stage. Both oscillators will be powered up and measured individually to avoid interference.

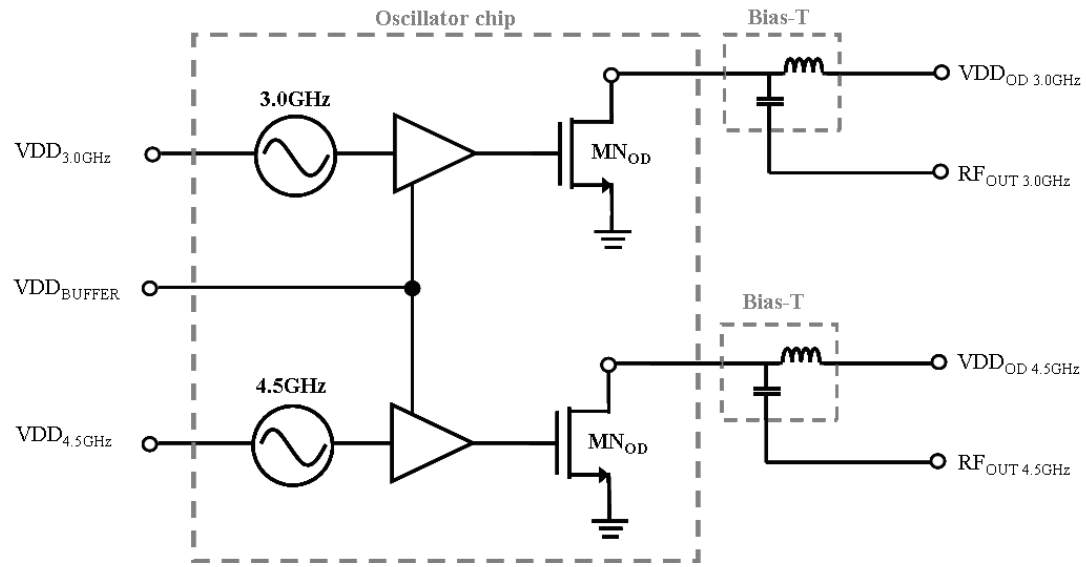

Figure 4.2. *The two designed oscillators have individual core supplies but joint output buffer supply. The oscillators will be powered up and measured individually to avoid interference.*

Because the target application does not require certain precise oscillation frequencies, the resonator components were not optimized during simulations to meet exactly the target oscillation frequencies. The final oscillation frequencies were hence a result of the inductor design choices and were accepted as they came.

The target oscillation frequencies for the two oscillators are 3.0GHz and 4.5GHz hence the characterization of the resonance tank components was performed for these two frequencies. The 3.0GHz frequency was chosen, because it allowed a feasible sized resonator tank to be implemented on the silicon area available. The higher target oscillation frequency 4.5GHz was a result of inductor choice. The inductor was chosen to have roughly half of the inductance of the 3.0GHz oscillator inductor, hence resulting in an oscillation frequency of 4.5GHz. This choice was made because the second oscillator should use the same components as the first one, but a smaller inductor in order to fit the same silicon area.

4.1 Oscillator core

The core transistors where chosen to have W/L ratios of 120µm/120nm (63 gate fingers) for the PMOS devices and 40µm/120nm (21 gate fingers) for the NMOS devices as shown in Figure 4.3. The size ratio of 3 between NMOS and PMOS devices is a design rule of thumb which originates from the different carrier mobility of n-type and p-type of silicon. In NMOS devices where the channel is formed through free electrons the carrier mobility is typically between 2-3 times higher than in p-channel devices [22]. The chosen device sizes give an average simulated current consumption of 11.1mA and 11.3mA on 3.055GHz and 4.717GHz respectively. The nominal break down voltage of the used devices is 1.2V.

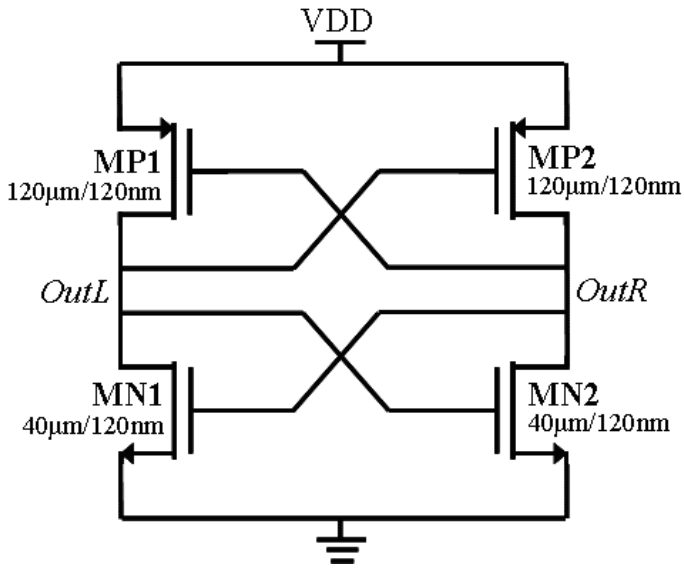

Figure 4.3 *Core transistor sizing.*

The channel length was chosen to be higher than the minimum of 65nm in order to decrease quality factor degradation caused by the transistors entering the triode region [5] and loading the resonance tank. A longer gate will also be less prone to channel length modulation and thereby appear as larger impedance.

4.2 Capacitor bank

The capacitor bank has two 6.6pF vertical parallel plate (VPP) metal-insulator-metal (MIM) capacitors laid out against each other making the total capacitance 3.3pF as shown in Figure 4.4. The series connection wastes chip area but ensures layout symmetry.

MIM-capacitors usually have quite low capacitance density compared to polysilicon capacitors due to the larger insulator thickness between metal layers and because of thin metal layers (concerning lateral capacitors). Special shapes can be adopted for increasing the capacitance density. Usually MIM-capacitors have the highest Q-value (due to small resistivity of metals) amongst capacitors and are therefore suitable for RF-applications.

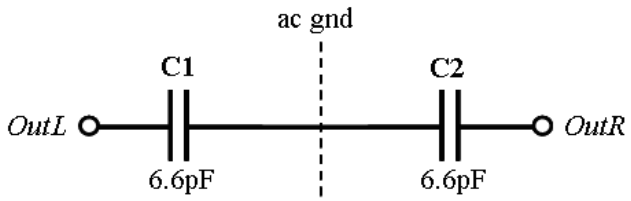

Figure 4.4 *Capacitor bank.*

The simulated quality factor of the capacitor bank together with its associated parasitic capacitance is 30.1 at 3.0GHz and 18.1 at 4.5GHz.

4.3 Output buffer

The output buffer shown in Figure 4.5 consists of a chain of two inverters. At the input of the buffer we have a 300fF coupling capacitor together with two 8kΩ biasing poly-resistors, which bias the input of the inverter to $VDD_{BUFFER}/2$. The input MOS transistors have a W/L ratio of 40µm/65nm for PMOS and 20µm/65nm for NMOS. The fan-out has a value of 1.2, making the output transistors 48µm/65nm and 24µm/65nm for PMOS and NMOS respectively. All transistors use 21 gate fingers. The output buffer was originally designed for a different purpose and is sub-optimal for the oscillators designed here.

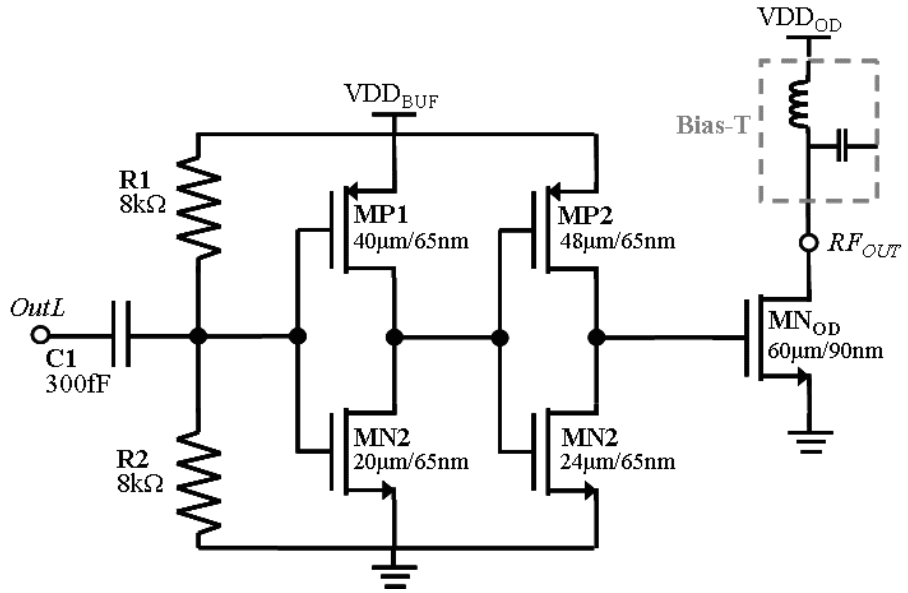

Figure 4.5 *Output buffer schematic.*

The open-drain stage was selected to have a W/L ratio of 60µm/90nm in order to drive the output pads. This creates a quite high ratio of 2.5 for the width of the last buffer NMOS device and the open-drain device.

4.4 Inductors

Two different inductors where designed for the oscillator to produce two different oscillation frequencies. First Cadence Virtuoso Passive Component Designer (VPCD) [23] was used to generate the initial inductor layouts. VPCD allows extracting a schematic model of the designed inductor (shown in Figure 4.6). However, the VPCD tool was not tuned to the process design rules, i.e. it did not generate some specific layers needed by the process for inductor layouts. Because of this the VPCD generated layouts needed to be modified by hand after generation and of course the VPCD generated circuit models would not take these modifications into account.

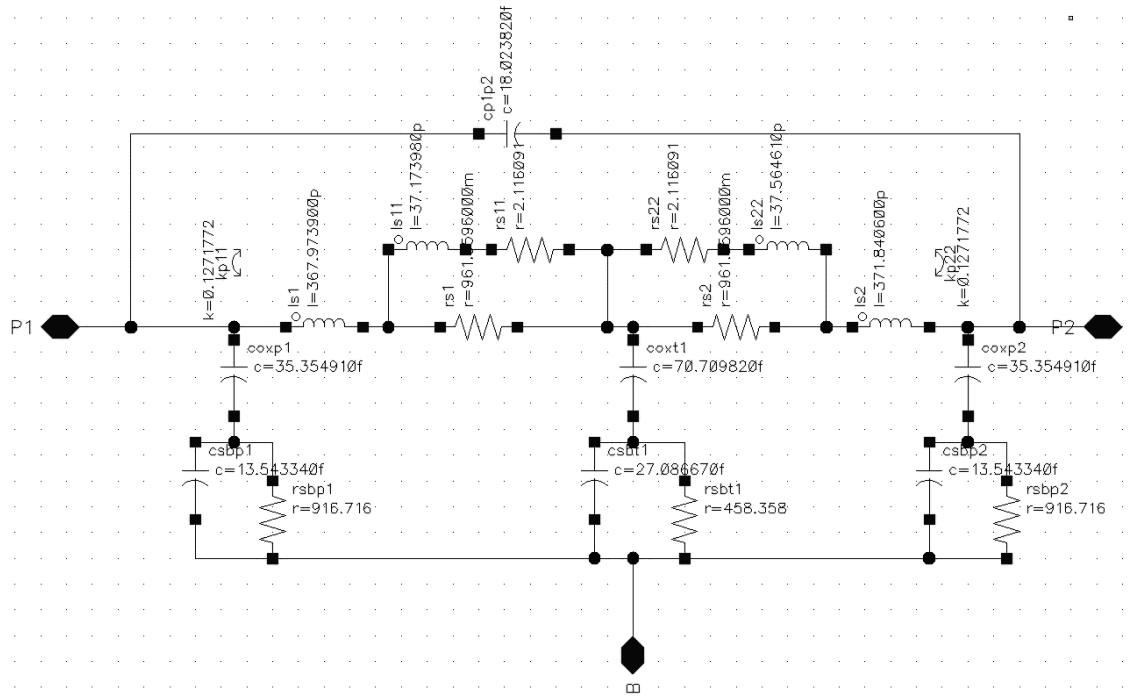

Figure 4.6 *The inductor model created by Virtuoso Passive Component Designer (VPCD) takes skin and proximity effects into account.*

Next the generated layouts were modified so that they fit the design rules of the process and pass layout vs. schematic checks (LVS). After the modifications the layouts were analyzed for inductance and quality factor using the Sonnet electromagnetic (EM) field solver software [24]. Based on the received results a circuit model was generated from Sonnet (shown in Figure 4.7). The models are optimized for the target oscillation frequency of each inductor and accuracy is therefore not guaranteed on other frequencies. All the simulations were carried out using these Sonnet generated models. One can see that the VPCD model is more complex than the model extracted from Sonnet e.g. it takes skin and proximity effect into account, however as mentioned before the VPCD generated layouts were modified after generation so the generated circuit models could not be used.

The first designed inductor is a two-turn single layer octagonal inductor with a modeled inductance of 702pH and Q-factor of 7.4 at 3.0GHz. The general views of the models generated by Sonnet and VPCD for this specific inductor are shown in Figure 4.7 and Figure 4.6 respectively. The inductance and quality factor values given by the Sonnet model differ slightly from the obtained EM simulation results shown in Figure 4.8 below i.e. the circuit model generated by Sonnet does not match exactly the Sonnet EM simulation result.

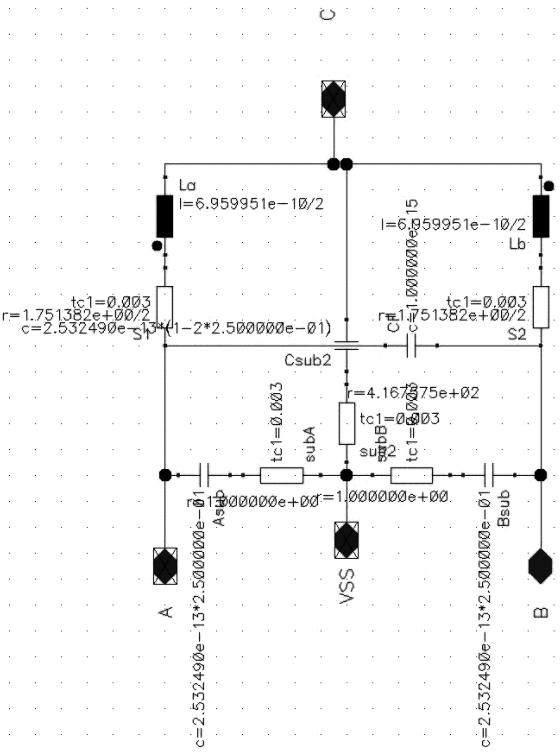

Figure 4.7 *Inductor model generated from Sonnet.*

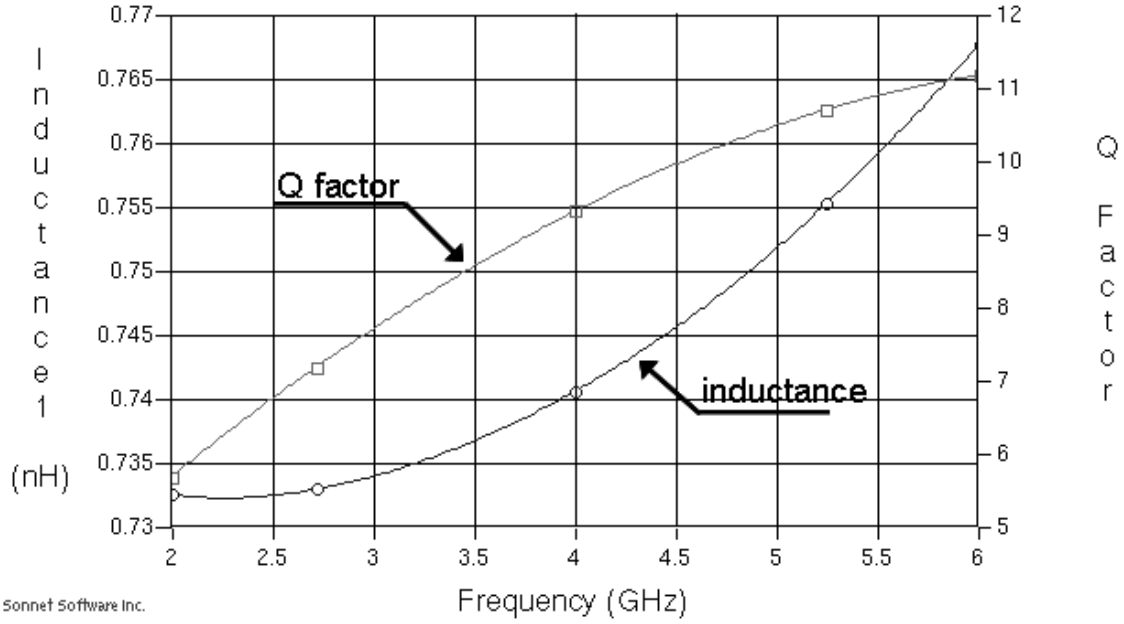

Figure 4.8. *Sonnet electromagnetic (EM) simulator evaluated inductance 735pH and Q-factor 7.5 at 3.0GHz.*

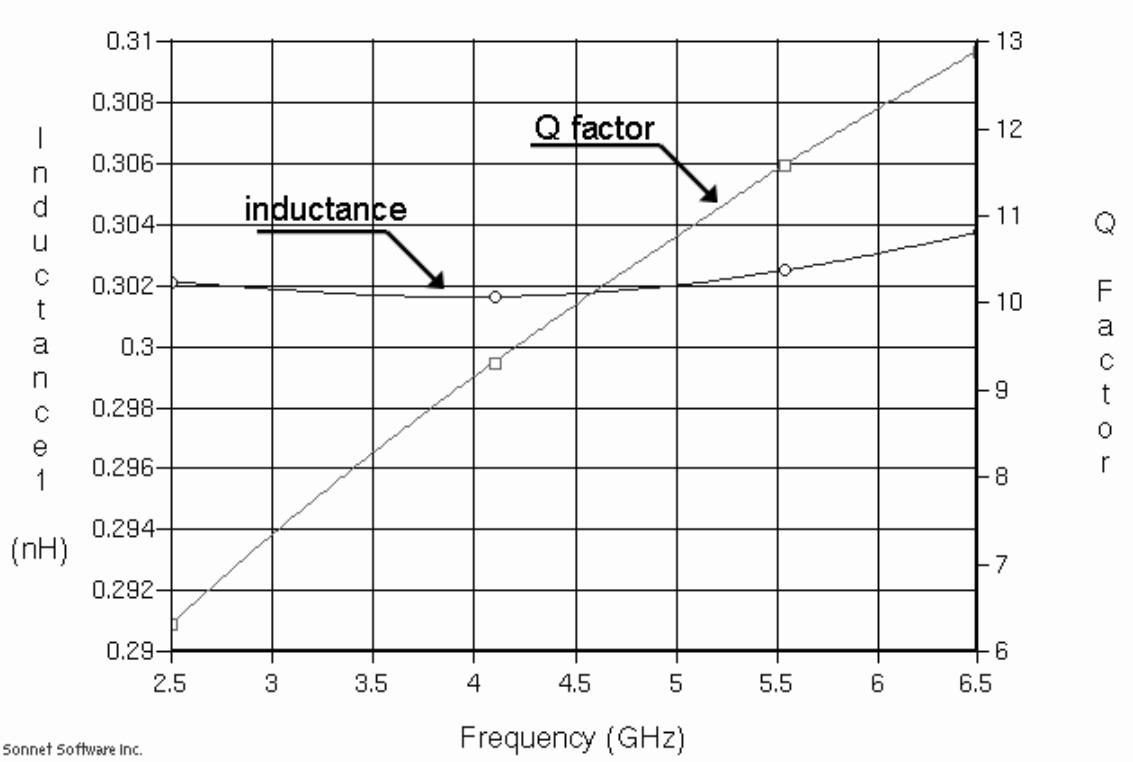

Figure 4.9. *Sonnet electromagnetic (EM) simulator evaluated inductance 302pH and Q-factor 10.0 at 4.5GHz.*

The second inductor is a single-turn single layer octagonal inductor with modeled inductance of 293pH and Q-factor of 10.2 at 4.5GHz. Again, the values differ slightly from the obtained EM simulation results shown in Figure 4.9.

5 LAYOUT DESIGN

The finished layout including both oscillators is shown in Figure 5.1 below and Figure 5.2 shows the corresponding fabricated chip. The two oscillator layouts are identical with the exception of the used inductor. The blue line in Figure 5.1 shows the border between the oscillators, the 3.0GHz oscillator is on top and the 4.5GHz oscillator is at the bottom. The overall silicon area of the design is 680µm x 510µm, which includes the probing pads.

In order to ensure that the two oscillators do not disturb each other during measurements only one oscillator is measured at a time. Both oscillators have their own VDD pad allowing the oscillators to be powered up individually. The output buffers of both oscillators share a common supply pad. The used pad size had to be quite small due to space limitations; on the other hand the measurement equipment required pads with 150µm-pitch. To fulfill these requirements small 100µm-pitch pads were re-spaced to 150µm-pitch to fit in the available silicon area, trading off skating length.

The 702pH inductor uses a second metal layer for the crossing from outer turn to inner turn. Due to a design rule limitation regarding the maximum width of paths drawn on this layer the crossing had to be made from two separate pieces in order to maximize the total width of the crossing. The amount of vias used for the under pass was limited by the shape of the inductor. The need for an under pass and the limited amount of vias increase the series resistance of the two turn inductor compared to the single turn inductor. The single turn inductor also uses a larger metal width. However, the actual quality factors of course depend on the produced inductance versus series resistance.

The capacitor bank has a horizontal shape in order to conserve silicon area in the vertical direction. This choice had to be made in order to fit the two oscillators in the silicon area available. The vertical shape of the capacitor bank creates a very short path from the inductor to the oscillator core, but at the same time it requires lower conductivity metal layers to be used for the interconnection of the two opposite capacitors. The low conductivity connection was compensated by adding several lower metal layers in parallel together with an extensive amount of vias. In a tunable oscillator this would increase the amount of constant capacitance and decrease the tuning range, but since tunability was not a concern in this effect was not of importance.

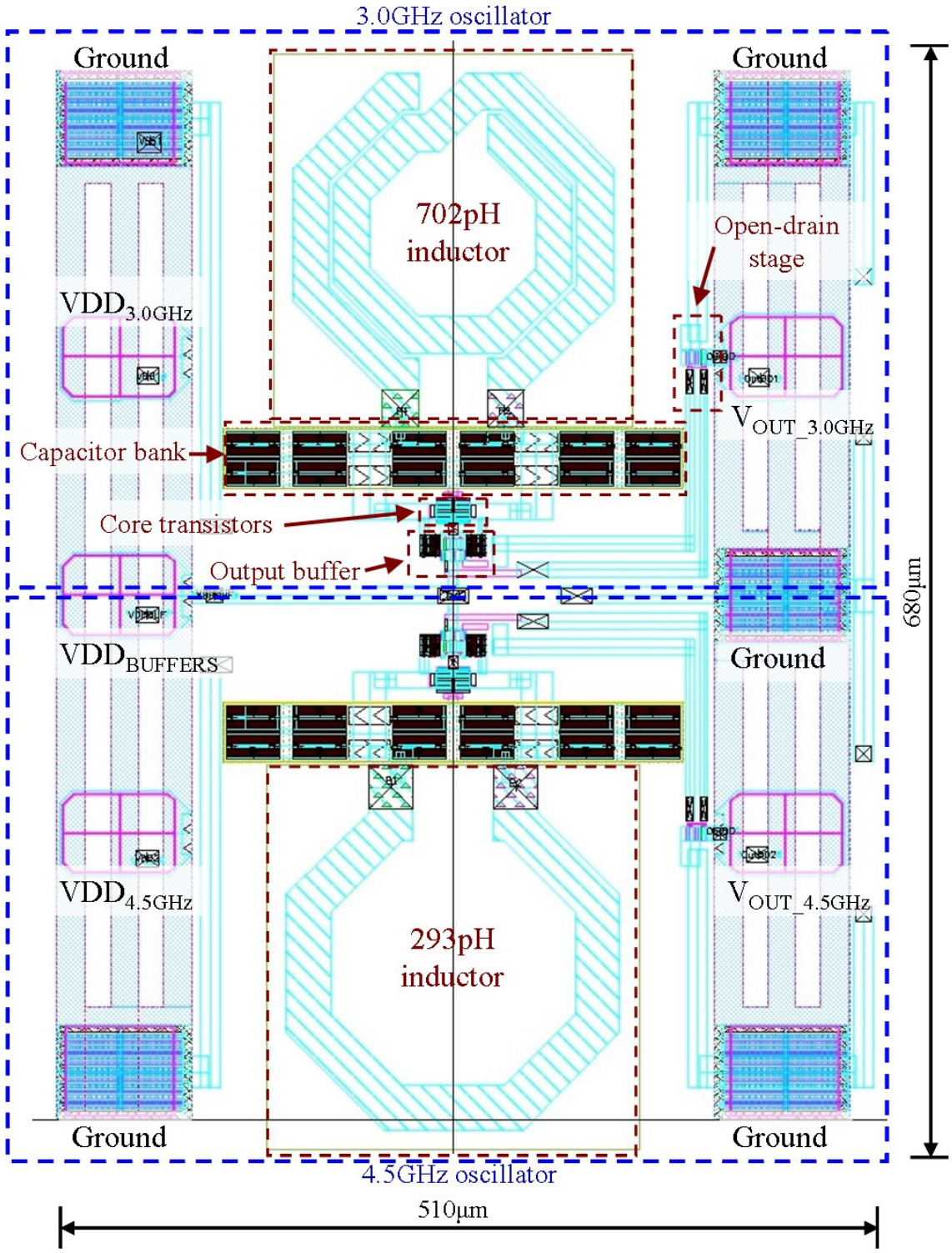

Figure 5.1 *Finished layout design (only top most metal layer is shown). The two oscillators have identical layout excluding the used inductor. The top half represents the 3.0GHz oscillator and the lower half the 4.5GHz oscillator. The total chip area is 680µm x 510µm.*

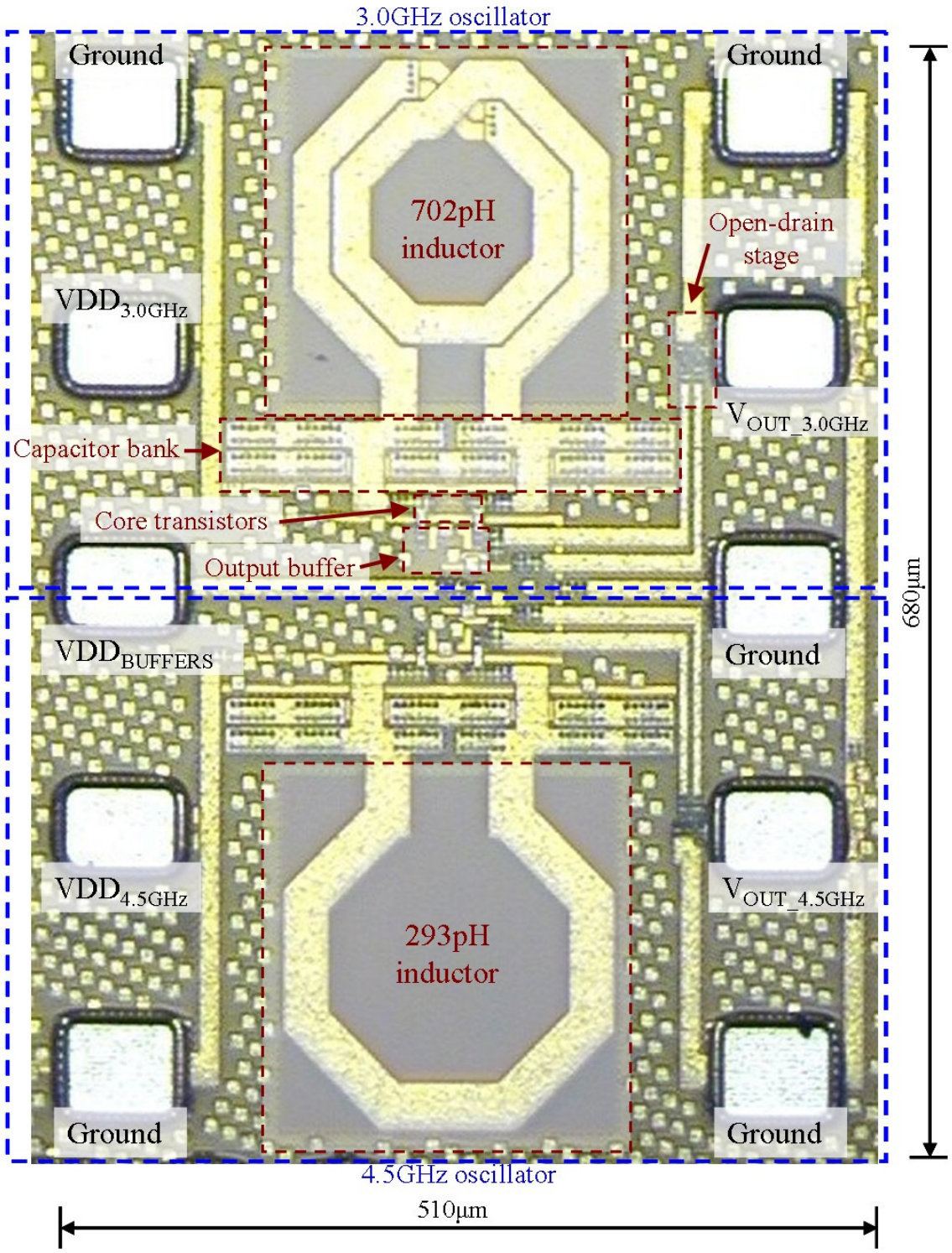

Figure 5.2 *Photograph of the layout on a fabricated chip. The two oscillators have identical layout excluding the used inductor. The top half represents the 3.0GHz oscillator and the lower half the 4.5GHz oscillator. The total chip area is 680µm x 510µm.*

The output buffer was placed near the oscillator core output to avoid additional loading of the core from the wiring capacitance. Again the same technique of stacking metals together with an extensive amount of vias was used to decrease series resistance of the connection between the capacitor bank, core transistors and output buffer. The

bias resistors for the output buffers input were split into smaller sections and those sections were laid out in an interleaved manner in order to equalize the effect of process variations. Also, dummy resistors were added to the edges of the resistors to ensure a symmetrical environment for the actual resistors and to protect against uneven etching around the edges of the resistors. [4]

The oscillator core transistors were laid out in a “common-centroid” configuration which is suitable for the matching of large differential pair transistors. The layout effectively cancels first order process gradient variations. The matching is further improved by gate finger interleaving. [4]

6 SIMULATIONS

Simulations were performed using the SpectreRF simulator from Cadence [25]. The simulations shown here are divided into two main parts: Oscillator simulations and resonance tank simulations. The oscillator simulations show the general performance of the designed oscillator including simulated values for the derived phase noise model parameters. The resonance tank simulations show the derivation of an RLC equivalent circuit for the oscillators at their oscillation frequencies.

6.1 Oscillator simulations

A test bench schematic view as shown in Figure 6.1 was created to facilitate simulations. The oscillator phase noise was measured with single-ended output. The test bench included the voltage sources for the oscillator core and output buffer. The 1mΩ resistors are for current probing. Parasitic capacitances were included for faster simulations after parasitic extraction. These capacitors were set to 1fF whenever they were not used. Additionally, the capacitor between the left and right oscillator output node was used to set an initial condition for quicker oscillation startup and shorter total simulation time. The test bench also included the external bias-T and a load resistance of 50Ω. The oscillator itself was embedded into the test bench as a block not including the inductor, this way the inductor could be easily changed on top level.

After the layout was generated for each design block, a parasitic extraction tool was used to compute additional wiring resistance and capacitance for all nodes of each block, including the top level wiring and probing pads. The final oscillator simulations were carried out using these parasitic extracted versions of the blocks (av_extracted view in Cadence terminology). The simulation results are shown in the Table 6.1 and the figures below.

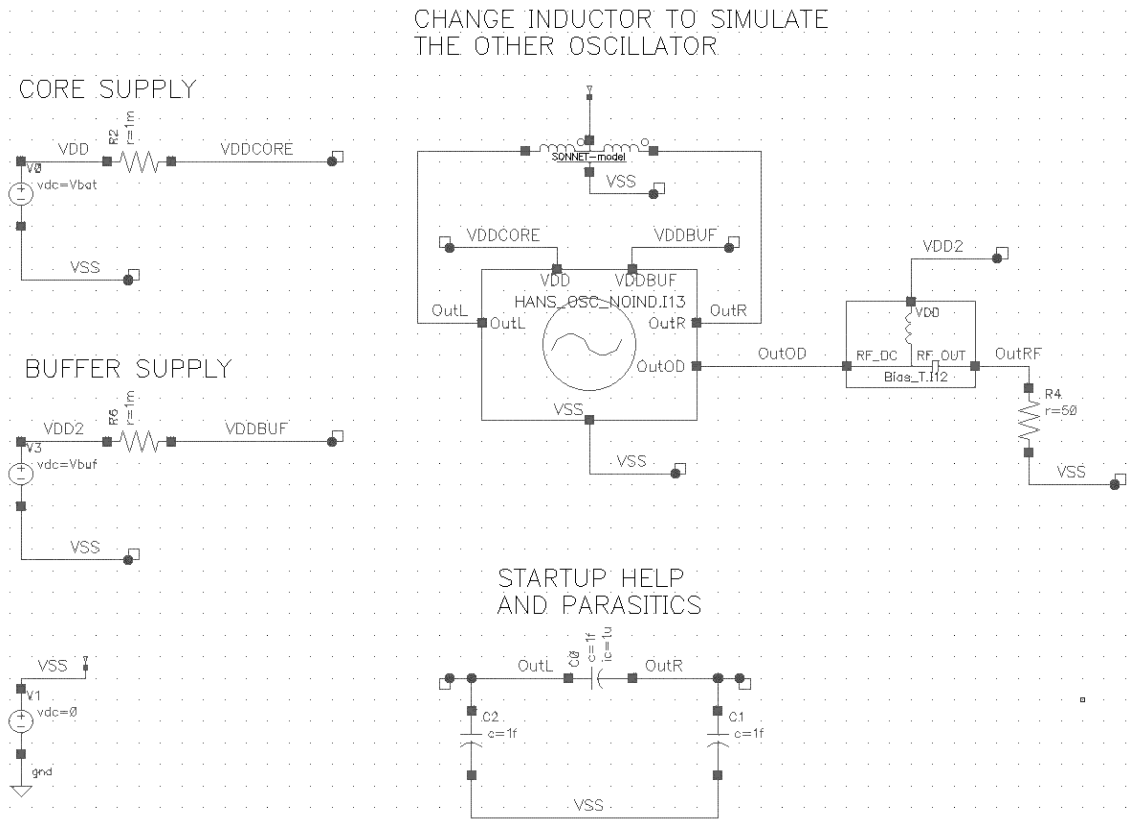

Figure 6.1 *Oscillator simulation test bench in Virtuoso Schematic editor.*

Table 6.1 *Simulation results. Simulation conditions are listed first (gray background) followed by simulation results.*

	3.0G	**4.5G**
V_{DD_Core} [V]	1.5	1.5
V_{DD_Buffer} [V]	1.2	1.2
$V_{DD\_Open\text{-}drain}$ [V]	1.2	1.2
R_{Load} [Ω]	50	50
F_{osc} [GHz]	3.055	4.717
$I_{core,\ avg}$ [mA]	11.06	11.25
$V_{p\text{-}p}$ [V]	1.06	0.72
Ph.N. @ 100kHz [dBc/Hz]	-102.7	-100.4
Ph.N. @ 1MHz [dBc/Hz]	-124.8	-121.5
Ph.N. @ 3MHz [dBc/Hz]	-134.6	-131.1
Ph.N. @ 10MHz [dBc/Hz]	-145.0	-141.5

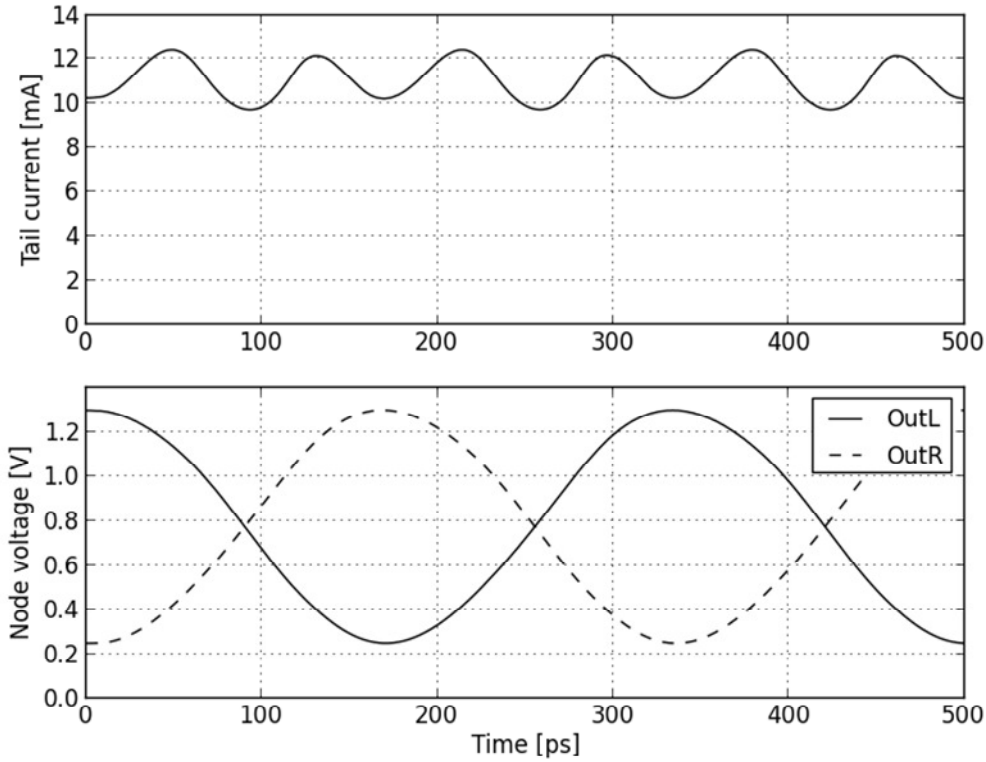

Figure 6.2 *Oscillator core tail current and node voltages for 3.055GHz.*

Note that since the tail transistor is omitted, the tail current does not stay constant. Thus, the drain-source voltage of the differential NMOS transistors can drop significantly, resulting in a large drop in their drain current, this can be seen as a drop in the tail current like in the figure above. This means that the 3.055GHz oscillator is operating close to the voltage-limited region. [17]

The average current consumption of the 3.055GHz oscillator is 11.06mA and the output voltage is 1.06Vp-p for the single-ended output and 2.12Vp-p for the differential output.

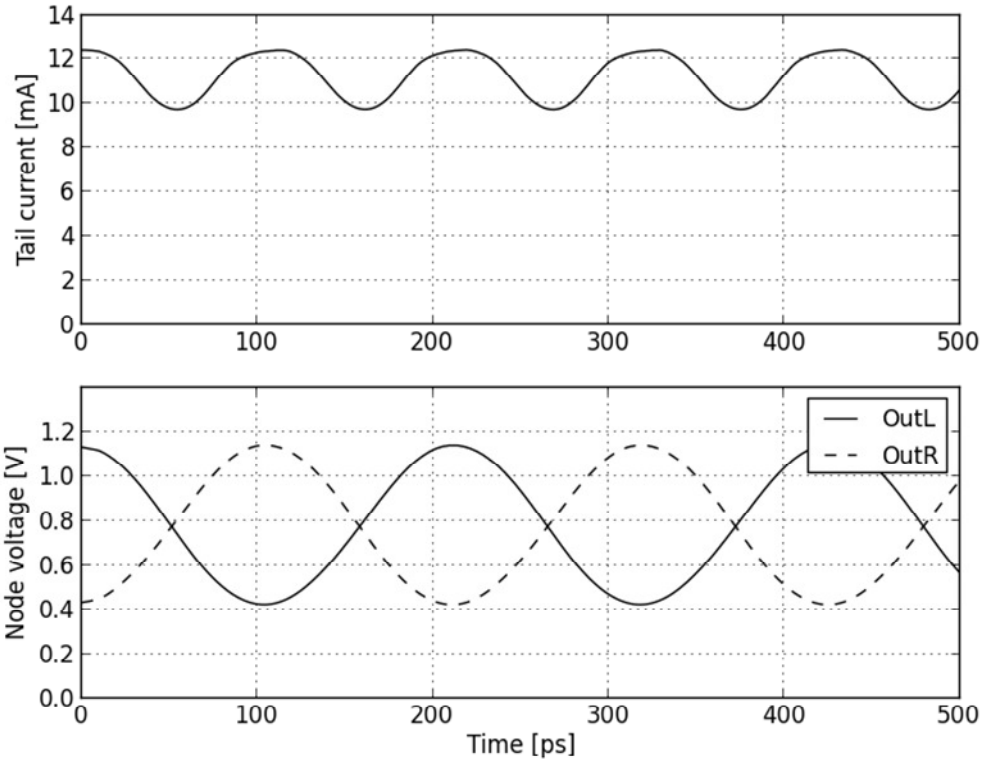

Figure 6.3 *Oscillator core tail current and node voltages for 4.717GHz.*

The 4.717GHz is showing a much smaller voltage swing for approximately the same tail current as the 3.055GHz oscillator. This is due to the smaller equivalent parallel resistance of the resonance tank which is caused by the smaller series resistance of the single turn inductor used. Evidently the 4.717GHz oscillator is operating in the current limited region. Usually the current is limited by the biasing tail current source, but since it has been omitted in this design, the current is in this case limited by the core transistors.

The average current consumption of the 4.717GHz oscillator is 11.25mA and the output voltage is 0.72Vp-p for the single-ended output and 1.44Vp-p for the differential output.

6.2 Resonance tank simulations

In order to simplify the quality factor calculations an equivalent RLC parallel resonance tank (as shown in chapter 2) was created for both oscillators. The impedances of the RLC tanks were matched to the impedances received when simulating the parasitic extracted capacitor bank and inductor models together. The results are shown below. At the resonance frequency of each tank the reactive parts of the impedance cancel out and

only the resistive part remains. The quality factor of a parallel resonance tank is directly proportional to its parallel resistance.

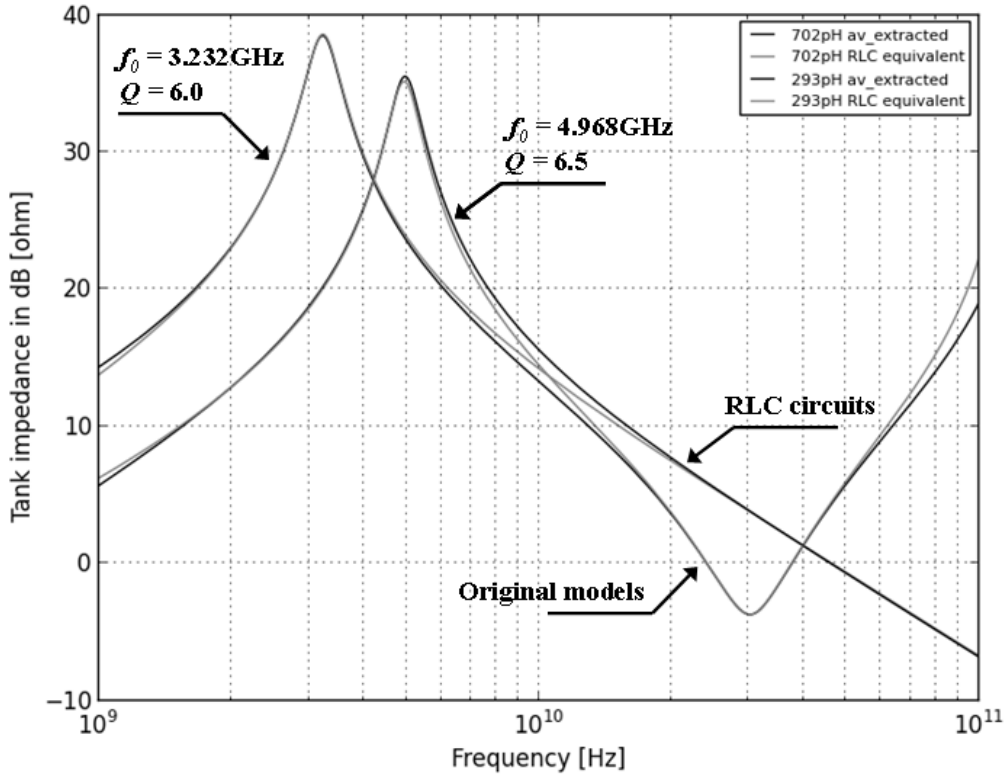

Figure 6.4 *The parasitic extracted resonance tanks have simulated quality factors of 6.0 and 6.5 for the 3.0GHz and 4.5GHz oscillators respectively. The maximum quality factors occur at 3.23GHz and 4.97GHz accordingly. Equivalent RLC parallel tanks were matched for both resonance tanks at the expected oscillation frequency.*

The received RLC circuits achieving best match with the parasitic extracted resonance tank are shown in Figure 6.5 below. Since the resonance frequencies of these two tanks match exactly the resonance frequencies of the extracted tanks but differ from the simulated oscillation frequencies, it can be assumed that difference is caused by load capacitance. The additional load capacitance was evaluated to be 0.41pF for the 3.055GHz oscillator and 0.38pF for the 4.717GHz oscillator. The small difference may be due to the fact that the designed inductors and capacitor were characterized at 3.0GHz and 4.5GHz and not at the oscillation frequencies.

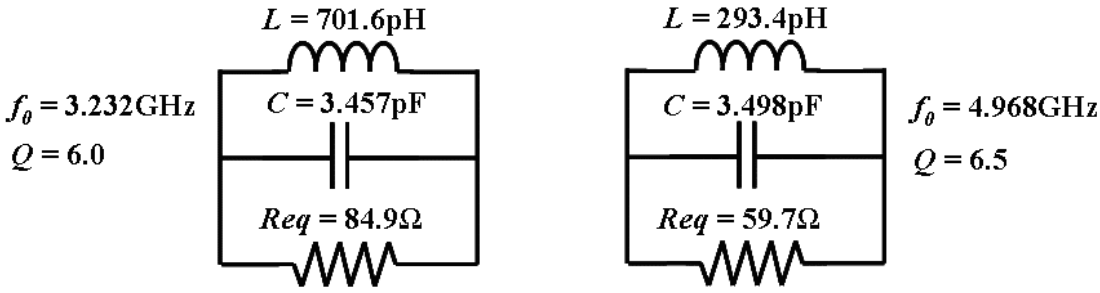

Figure 6.5 *Received component values for 3.0GHz tank (left) and 4.5GHz tank (right).*

When comparing the received equivalent resistances to the node voltages received in the time domain simulations of the two oscillators, it can be seen that in both oscillator cases the produced voltage over the resonance tank matches quite well the voltage which would be produced when the corresponding tail currents were fed through the received equivalent resistances. Because of this and since the additional loading capacitance is small we will assume the loaded quality factors Q_L of the tanks to be approximately equal to the unloaded quality factors.

7 MEASUREMENTS

The measurements were carried out at the RF-Communication Circuits (RFCC) Laboratory's IC measurement facility. The measurements were performed on a Cascade Microtech 9000 Probe Station with a HP 4352B VCO/PLL Signal Analyzer with capability to measure signals up to 3GHz. HP E3631A power supplies were used for DC voltage generation and HP 34401A multimeters for current measurements.

Because of the frequency limitation of the VCO/PLL measurement system, a Picosecond 5650 frequency divider block is used to drop the oscillation frequencies to half for measurement. This division by two drops the phase noise by 6dB throughout the carrier offset frequency range [1].

The measurement plan is shown in Figure 7.1 below. The plan shows the chip as it is seen under the microscope. The chip is contacted through a GSGSG probe from the left hand side and through a GSSSG probe from the right hand side. The use of five legged probes allows all measurements to be carried out with one single landing for each probe. In order to switch between oscillators it is necessary only to change the oscillator supply voltage cables and open-drain output cables (after bias-t). Due to the single ended measurement setup additional bias-t blocks were placed on all supply lines for additional supply voltage filtering.

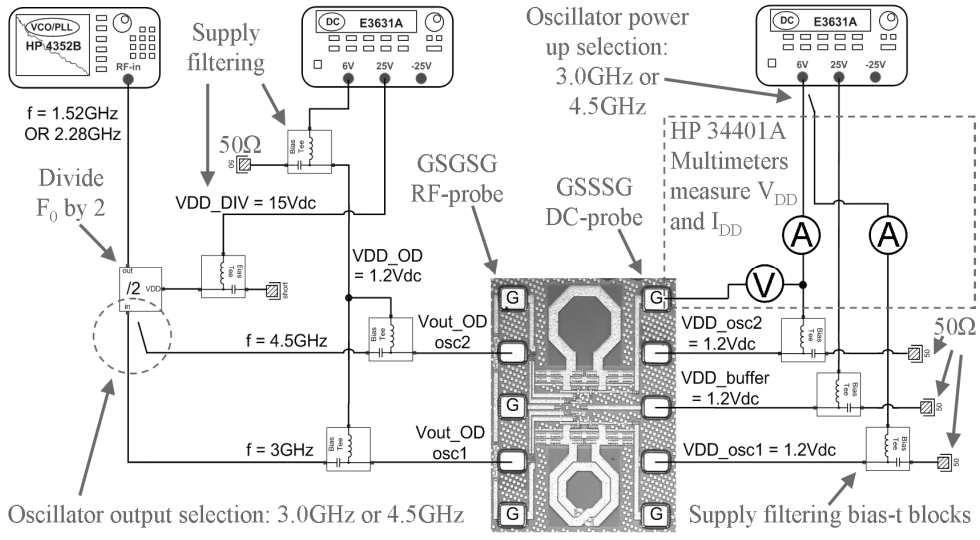

Figure 7.1. *Thumbnail of the measurement plan in Appendix A. The plan shows initial startup voltages and connections to measurement equipment. The core supply voltage is connected to one oscillator at a time and the oscillators are measured through the divider individually by switching output cables. Additional bias-t blocks are used in all supply lines for supply filtering.*

After the measurement plan was finished all needed cables and components were gathered and duct taped to the probe station to prevent cable movement.

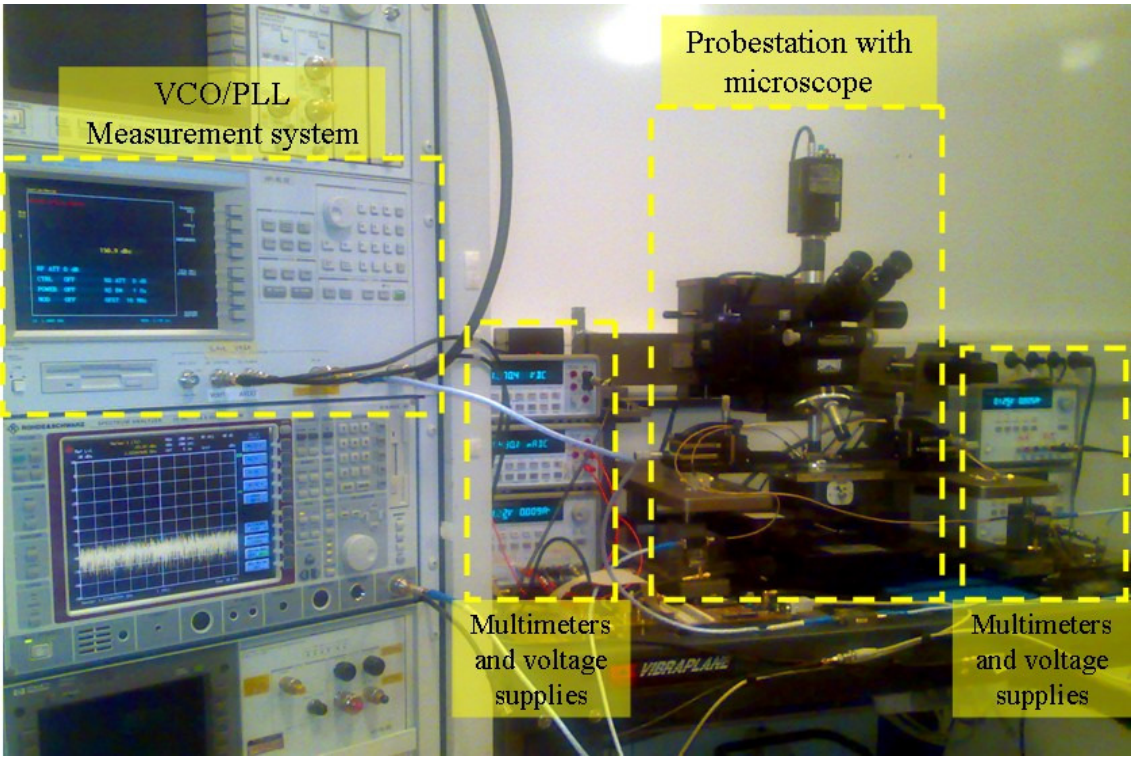

Figure 7.2 *The measurement setup in place according to the measurement plan. All cables are duct-taped to the measurement table to prevent movement. The multimeters are used to measure current consumption and supply voltages at the chip end.*

Four samples of the manufactured chip were glued onto a thin glass plate. This glass plate was then placed under the microscope on the suction plate which uses a vacuum pump to suck air through small holes on the plate to hold the glass plate still.

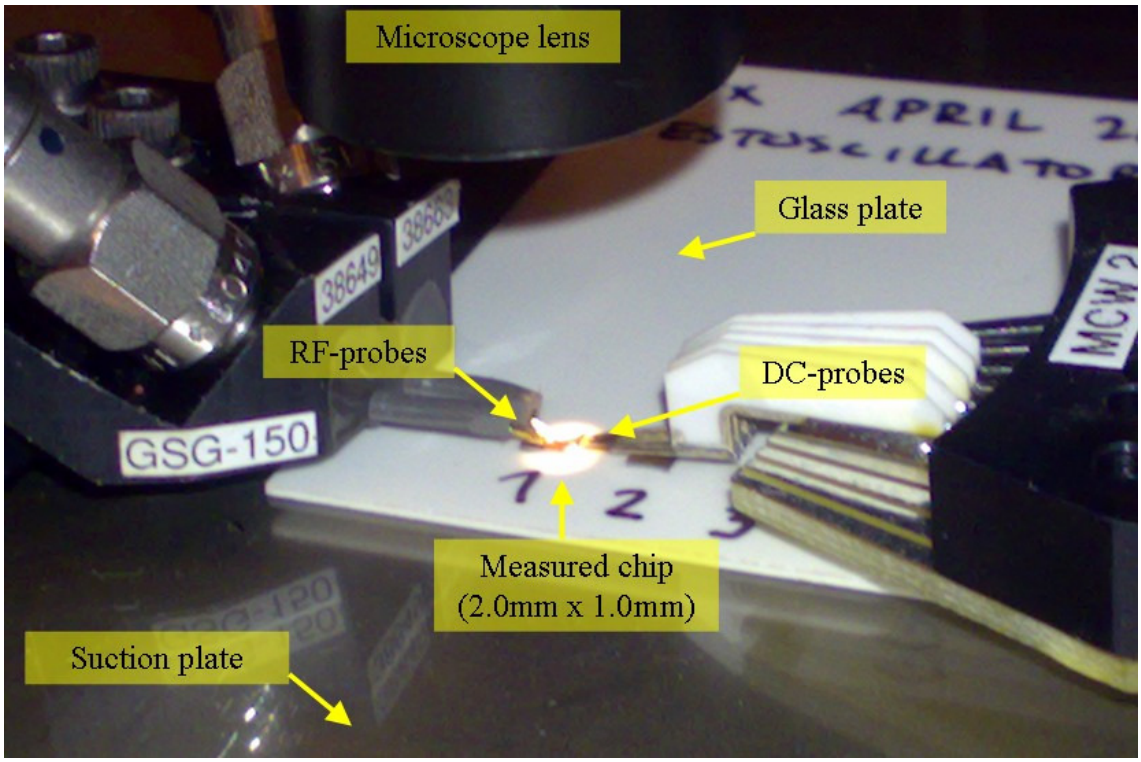

Figure 7.3. *Four samples of the measured chip are glued to a glass plate which is held in place by the suction plate operated by a vacuum pump. The chip is oriented so, that the RF-probes are landed from the left and DC-probes from the right side.*

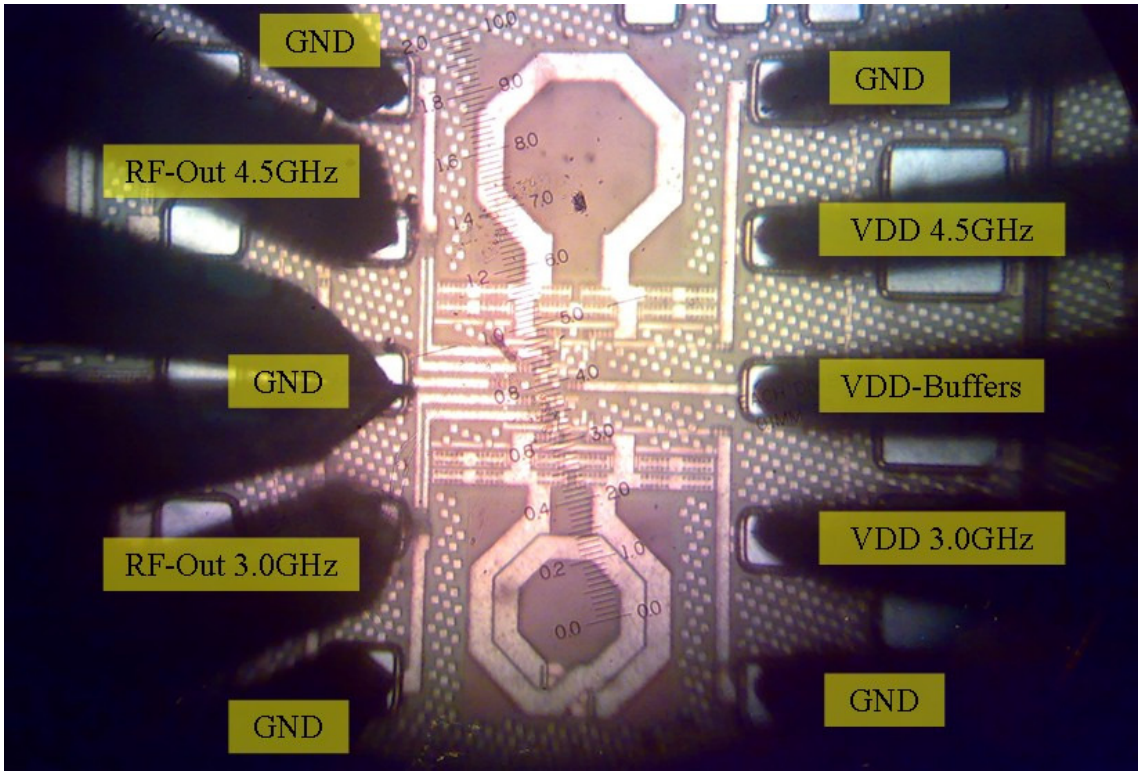

Figure 7.4 *A view through the microscope with probes landed. The RF-probes are on the left hand side and DC-probes on the right hand side.*

Landing the probes is the last step before powering up the chip and starting to gather measurement data. The probes (as well as the chip) are very fragile and need to be landed carefully. As the probes are lowered towards the chip surface the microscope focus needs to be adjusted continuously. When the probes are near the surface of the chip the probes are moved to the outer edge of the landing pads and focus is adjusted to the chip. The probes are lowered so that they just touch the pads and then lifted up again. As the probes leave marks on the pads the need for probe tilt adjustment can be judged from these marks. When the probe leaves equal sized marks on all pads it is landing evenly and all probe tips have contact. As the probes are lowered they bend and skate along the pad. Lowering is stopped when the probes reach the inner edge of the pads and give maximum contact.

7.1 Initial results and observations

The first oscillator to be measured was the 3.055GHz oscillator. The supply voltages of the oscillator core, buffer and open-drain stage were all set to 1.2V for initial start up. After the chip was powered up it was observed that the VCO/PLL system had trouble to lock its second PLL to the oscillator output signal. It was found that this was caused by a bump in the oscillators phase noise curve between the carrier offset frequencies from 900kHz to 3MHz. The same behavior was later observed with the 4.717GHz oscillator. The phenomenon is shown in Figure 7.5 below. Note that the measured frequencies are now 1.522GHz and 2.279GHz due to the frequency divider. Since the divider is dropping the phase noise by 6dB, the simulated phase noise values are corrected by the same factor.

After investigating the PLL locking issue it was found that reducing the output buffer supply voltage and open drain supply voltage made the bump disappear and allowed the VCO/PLL measurement equipment to properly lock on to the oscillator signal. It is assumed that the output buffer used in the design was loading the oscillator core too much at nominal. Further more, it is assumed that the output buffer input exhibits a reactive load that has a resonance frequency around the carrier offset frequency at which the phase noise bump was observed.

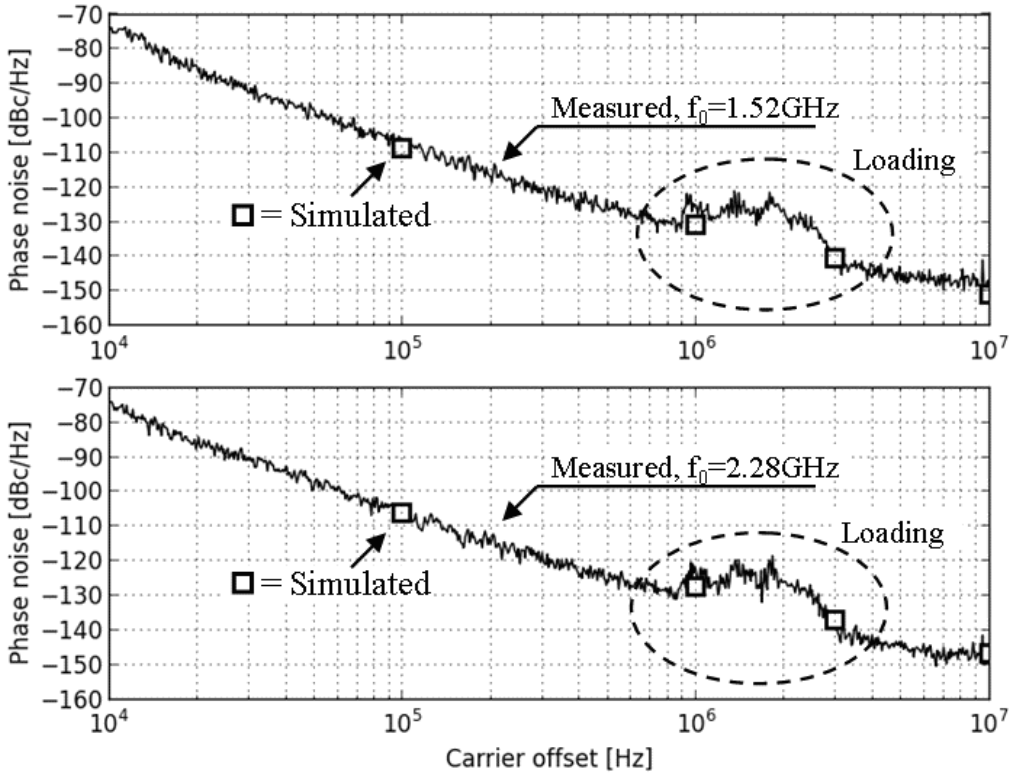

Figure 7.5 *The initial measurements with all voltage supplies set to 1.2V revealed a bump in the carrier sideband between carrier offsets of 900kHz and 3MHz causing PLL locking difficulties for the measurement equipment. The bump was removed by relaxing the core loading by decreasing the buffer and open-drain supply voltages.*

The same loading effect as described above was also observed when the supply voltage of the core was decreased while keeping the buffer supply voltage constant, this is shown in Figure 7.6 below for four different carrier offset values. In this figure the phenomenon is especially visible at the higher carrier offsets. The buffer supply voltages are 0.8V and 1.0V for the 1.52GHz and 2.28GHz output signals respectively.

It was decided that all measurements should take place in such operating conditions that the measurement equipment remains properly locked to output the signal. The oscillator core voltage was at the simulated value of 1.5V and the output buffer and open-drain supply voltages were set to the maximum value which would still give a proper PLL lock. These values are shown together with the corresponding measurement results in Table 7.1 below.

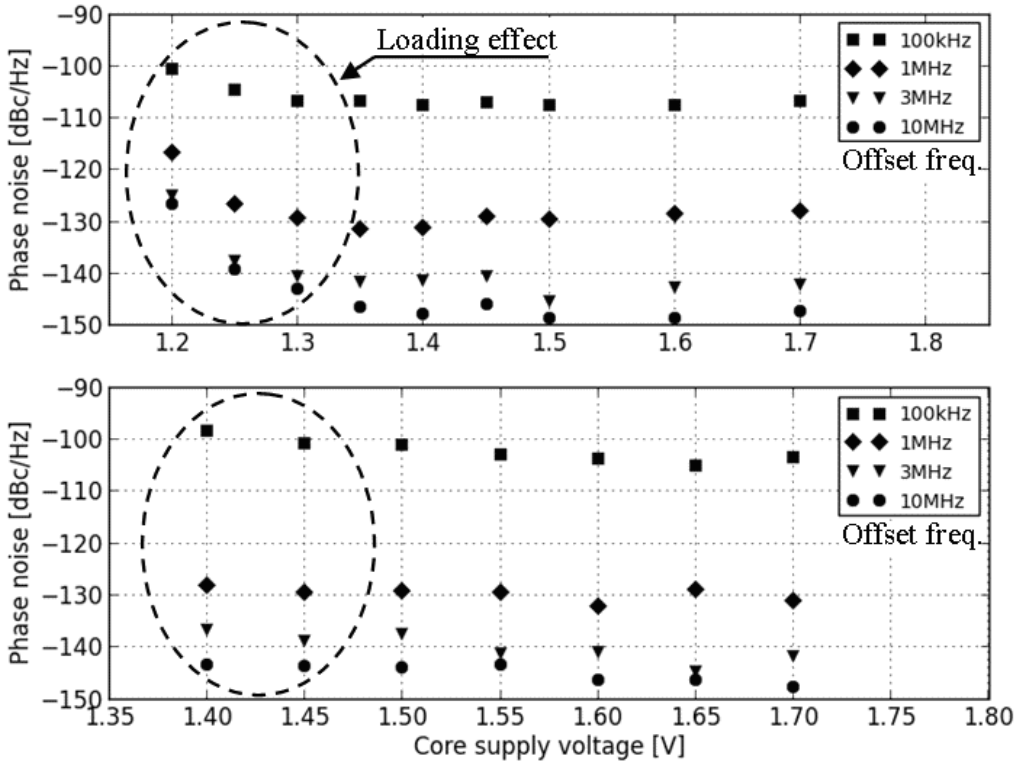

Figure 7.6 *The buffer loading effect was also observed when keeping the buffer and open-drain voltages fixed at their reduced values and varying the core supply. The measured phase noise increased rapidly for core voltages below 1.3V with both oscillators; 1.52GHz (top) and 2.28GHz (bottom).*

Table 7.1 *Measurement results under maximum load operating conditions. Measurement conditions are listed first (gray background) followed by measurement results.*

	3.0G	**4.5G**
V_{DD_Core} [V]	1.50	1.50
V_{DD_Buffer} [V]	0.7	1.0
$V_{DD\_Open\text{-}drain}$ [V]	0.6	0.6
R_{Load} [Ω]	50	50
F_{osc} [GHz]	3.044	4.559
$I_{core,\ avg}$ [mA]	9.4	10.7
P_{in} [mW]	14.1	16.1
Ph.N. @ 100kHz [dBc/Hz]	-107.7	-102.9
Ph.N. @ 1MHz [dBc/Hz]	-131.1	-129.5
Ph.N. @ 3MHz [dBc/Hz]	-140.4	-141.2
Ph.N. @ 10MHz [dBc/Hz]	-143.1	-143.6

7.2 Measurement results versus modeling

Since the operating conditions where the fabricated oscillators can be reliably measured differ from the operating conditions used in simulations, the measurements shown here are not compared to simulations. Instead, the two oscillators are compared against each other. Figure 7.7 below shows the measured phase noise of both oscillators for the operating conditions in Table 7.1.

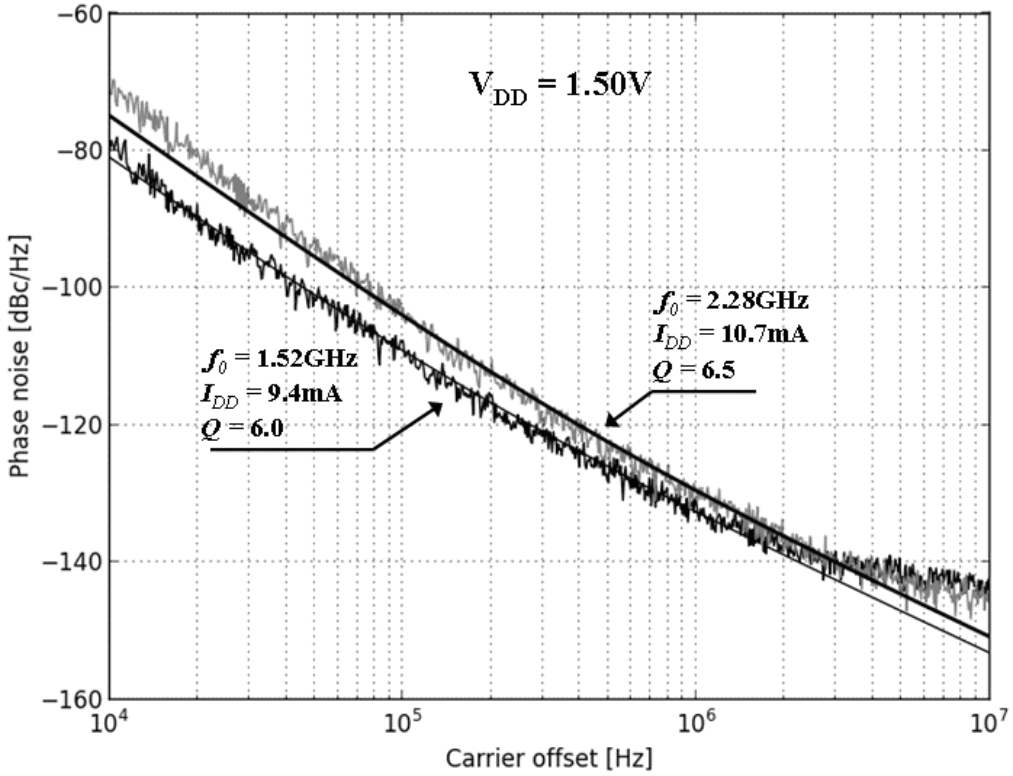

Figure 7.7 *The fitted phase noise model matches extremely well with the measured phase noise of both oscillators. The best fit is achieved with the same tank quality factor values which were received in simulations.*

Figure 7.7 shows also modeled phase noise curves using derived phase noise model which is fitted to the measured phase noise of both oscillators. Since the measurements were taken after a divide-by-two frequency divider and original oscillating frequencies were used for the modeling plot a 6dB subtraction was made from the model values. The modeled phase noise equation does not take into account the increased noise floor caused by the divider circuit.

The individual parameters of derived model, including the noise factor parameters, were set according to the results received from the measurements. Only the resonance tank capacitance was set to the value received in simulations. In practice, this means that first the oscillation frequency was measured together with the tail current. Then using the Thomson formula the inductance value was estimated. The estimated inductance values are 791pH and 348pH with 13% and 19% increase from simulated values

respectively. This is a rough estimate and does not take into account the drop in oscillation frequency due to tail current harmonics i.e. the estimation could be improved. However, this difference did not seem to affect the quality factor estimation significantly. After this the 1/f corner frequency was visually estimated from the point where the phase noise slope turns from -30dB/dec to -20dB/dec. The measured and estimated values were inserted into the model and the model was plotted on top of the measured data. Finally, the quality factor was adjusted to align the model with the measurement data. The phase noise model plot aligned best with the 3.04GHz oscillators measured phase noise when the tank quality factor was set to a value between 6.0 and 7.0. For the 4.56GHz oscillator the corresponding quality factor resulted in a value between 6.5 and 7.0. The received values are matching quite well the simulated tank quality factors which are 6.0 and 6.5 for 3.055GHz and 4.717GHz respectively. If we choose the most pessimistic fitted quality factor values to represent the resonance tanks Q-factors, then the measurement results match the simulations exactly. This means, that after we subtract the impact of the capacitor banks Q we receive the exact same quality factors for the inductors as in the simulations. Taking the middle value and tolerances we receive inductor quality values of 8.2 ± 0.8 and 10.8 ± 0.6 respectively.

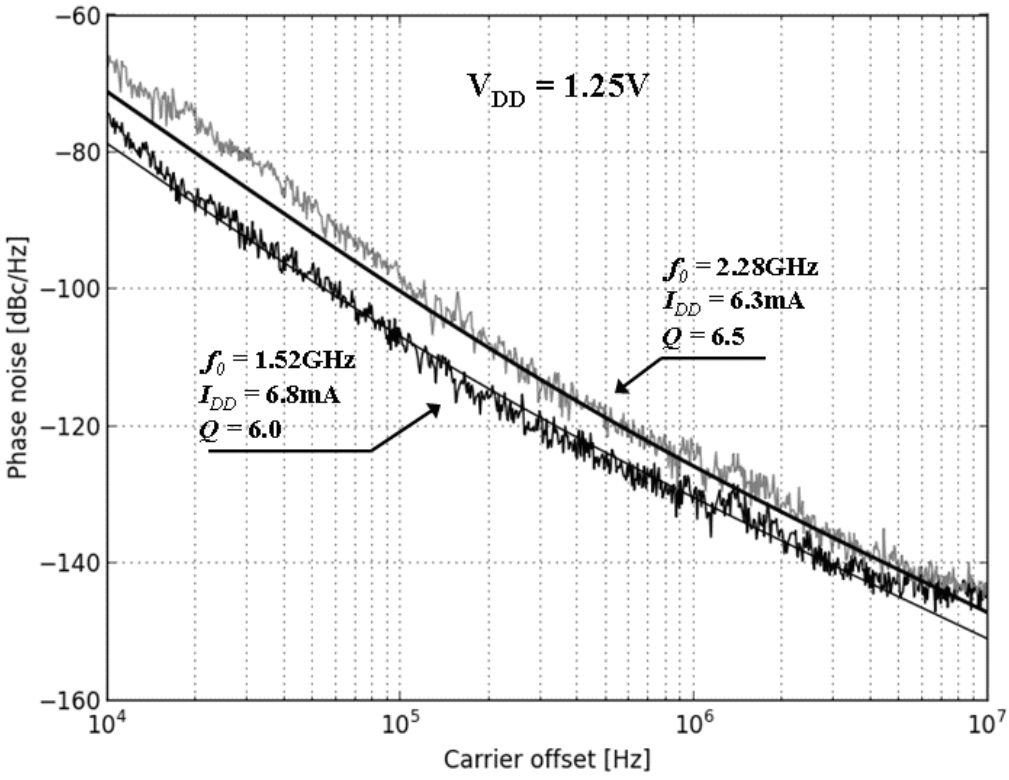

Figure 7.8 *The phase noise model fits the measured phase noise of both oscillators also with lowered V_{DD}. The model uses the measured current consumption to take into account the change in oscillation amplitude. Best fit is again achieved with the simulated quality factor values.*

The model fitting is repeated for different measurement points with good results. Figure 7.8 shows the same oscillators now operating at V_{DD} = 1.25V. We have adjusted the model parameters V_{DD} and I_{DD} to match the new measurements settings. Again the model fits the measurement data very well.

It can be seen in Figure 7.7 and Figure 7.8 that as we get closer to the carrier in the $1/f^3$ region the measured phase noise for the 4.56GHz oscillator starts to rise more rapidly than the model predicts. As it was shown in the simulations the 4.56GHz oscillator is operating in the current limited region i.e. its gain is not high enough to enable hard switching as it is required by the model. According to [6] the phase noise resulting from up conversion of the differential pairs flicker noise is inversely proportional to the gain, which explains the observed behavior.

8 CONCLUSIONS

Conclusion I: We have shown that it is possible to estimate the quality factor of an inductor by the phase noise it creates when used in an oscillator. The quality factor estimation is performed indirectly through a phase noise model which is fitted to measured phase noise data. Two differential CMOS LC oscillators (1L-CMOS) oscillating at 3.04GHz and 4.56GHz were fabricated and measured for this purpose. The measured phase noise was compared to the 1L-CMOS specific phase noise model shown in this work. Both oscillators show good agreement with the phase noise predicted by the model giving inductor quality values of 8.2 ± 0.8 and 10.8 ± 0.6 for the corresponding simulated values of 7.4 and 10.2. The expression of the model requires that the LC resonators capacitance including parasitic capacitance is known, all other model parameters can be evaluated by external measurements. The inductor quality factor is received from the resonators loaded quality factor Q_{tank} by first using Q_{tank} as a fitting parameter in the phase noise model. The model assumes a hard switched oscillator tail current.

Conclusion II: The shown phase noise model can be calibrated for a certain process and core transistor type by using a reference oscillator with a well modeled reference inductor. The reference inductor can be designed so that its shape is optimal for model generation using electromagnetic field solver software. Also, the method shown here can be used for quick quality factor verification against earlier verified reference inductors.

Conclusion III: It must be noted that the method for inductor quality factor estimation shown here is narrow band only, giving an estimate of the inductors quality factor at the oscillation frequency of the test oscillator. If quality factor estimation is needed for a certain specific frequency, the inductance of the inductor under test should be known and the test oscillator's capacitor value should be selected accordingly.

Conclusion IV: The possibility to characterize an inductor for its quality factor and inductance over a larger frequency range requires the implementation of frequency tuning for the test oscillator. The varactors used for frequency tuning need to be well characterized for capacitance and quality factor throughout the entire frequency range of interest and with all control voltage values. Again, the frequency range for which characterization can be performed depends on the used varactor bank. Broad band inductor characterization using oscillators is left to be investigated in future works.

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APPENDIX A: FULL-SIZE MEASUREMENT PLAN