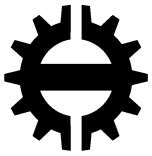

TAMPERE UNIVERSITY OF TECHNOLOGY

Mohammad Moakhkhrul Islam

Two-Phase DC-DC Buck Converter for Power Amplifier Modulation

Master of Science Thesis

Examiners: Professor Nikolay T. Tchamov, Jani Järvenhaara.
Examiners and subjects were approved in the Faculty of Computing and Electrical Engineering Council meeting on 05-10-2011.

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Tampere on April, 2012

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Abstract

This thesis presents the theory, design, layout and a proposal for measurement set up of a synchronous DC-DC buck converter. This converter will be used as the supply modulator of power amplifier of mobile phones. The design is done using 45nm CMOS technology. Pmos and nmos switches are synchronously turns on and off for DC voltage conversion. Second order LC type filter is used to filter out the ac component from output. Two phase interleaving is done to reduce the output ripple voltage. Pulse Width Modulation (PWM) method is used for generating the control signal. Several techniques like dead time control mechanism, reduced gate drive voltage for switches are applied for improving the efficiency of the converter.

The operating voltage range of the converter is 3.3-4.2V and it can produce 0.5-3V output voltage with 2W of maximum output power. It has maximum load current of 700mA. The switching frequency of the converter can be varied from 10MHz to 100MHz. The ripple voltage is less than 10mV for 50MHz switching frequency. The converter shows good results in terms of power density and simulated efficiency which are 1.65W/mm^2 and 88.5%.

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Tiivistelmä

Tässä diplomityössä esitetään synkronisen buck -tyyppisen tasajännitemuuntimen teoria, suunnittelu ja mittauskytkentä ehdotus. Piiri on suunniteltu 45nm CMOS teknologialla, ja sen käyttökohteena on tehovahvistimen käyttöjännitteen modulointi. Ulostulojännite muodostetaan kytkemällä pmos ja nmos kytkimiä synkronisesti päälle ja pois. Ulostulojännitten ac komponentin, rippelin, suodattamiseen on käytetty toisen asteen LC-suodatinta. Lisäksi lomittamis (interleaving) tekniikkaa on käytetty vähentämään ulostulojännitteen rippeliä. Ohjaussignaali kytkimille muodostetaan pulssin leveys modulaatiota (PWM) käyttäen. Suunnittelussa on käytetty useita menetelmiä hyötysuhteen parantamiseksi, kuten säädettävä dead time ja madallettu ohjaussignaalin jännite.

Tasajännitemuunnin toimii jännitealueella 3.3-4.2V ja se tuottaa ulostulojännitteen välillä 0.5-3V. Maksimi ulostuloteho on 2W ja kuormavirta 700mA. Kytkentätaajuus voidaan valita väliltä 10-100MHz. Ulostulojännitteen rippeli on alle 10mV 50MHz taajuudella. Simulaatioissa saavutettu tehotiheys on 1.65W/mm^2 ja hyötysuhde 88.5%.

Abbreviations

AC	Alternating Current
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DRC	Design Rules Check
EGDE	Enhanced Data rates for Global Evolution
EMI	Electro Magnetic Induction
GSM	Global System for Mobile Communications
IC	Integrated Circuit
IMD	Inter Modulation Distortion
LTE	Long Term Evolution
LVS	Layout vs. Schematic
LDO	Low Dropout Regulators
MOS	Metal Oxide Semiconductor Transistor
NMOS	N-type Metal Oxide Semiconductor
PA	Power Amplifier
PCB	Printed Circuit Board
PFM	Pulse Width Modulation
PWM	Pulse Frequency Modulation
PMOS	P-type Metal Oxide Semiconductor
RF	Radio Frequency
RFI	Radio Frequency Interference

SMD	Surface Mounted Device
SC	Switched Capacitor
UMTS	Universal Mobile Telecommunications System
WiMAX	Worldwide Interoperability for Microwave Access

Symbols

C	Capacitance
C_{ox}	Capacitance of the MOS transistor Oxide Layer
Cgs	Gate to source capacitance of mosfet
Cdb	Gate drain overlap capacitance
Cgd	Wiring capacitance and stray capacitance
dB	Decibel
dBC	Decibels relative to the carrier
L	Inductance (in schematics)
P	Power
Q	Quality Factor (ratio of reactance to the resistance)
V_{BAT}	Battery voltage
V_{SS}	Negative Supply Voltage
f	Frequency
f_{switch}	Switching frequency
f_{cutoff}	Cut off frequency of filter
Ω	Ohom, unit of resistor
η	Efficiency

1 Introduction

Portable electronics have significantly advanced in the last decades. Most of these equipments have Li-Ion batteries as their power supply. The output voltage of the Li-Ion batteries changes from 4.2 to 2.6 [1]. Due to this reason Li-Ion batteries can not be used directly as a power supply for different IC's in the electronic system [1]. The IC's used in the system, need a constant power supply for proper operation. A power management unit is used between the battery and the system to provide a constant power supply to different IC of the system. DC-DC converter is the major component of the system. DC-DC converter gives a regulated output voltage while the input voltage and load current are varying widely.

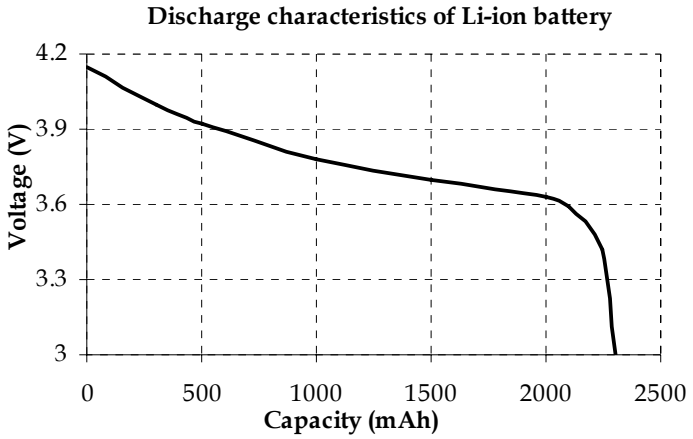


Figure 1-1. Discharge characteristics curve of Li-ion battery. [1]

The electronic equipments are consisting of the analog, digital and mixed-signal systems. They are becoming more complex to meet the challenges of increased demand for different features and due to continuous pressure on size reduction. The trend in minimizing the cost and power consumption of portable electronic devices are forcing to implement different system in a single IC. But these systems need good isolation and independent power supplies [3]. DC-DC converter can work as power supply unit for different system with isolation from each other. Beside this the design of converter is dependent on application. As for example, for a Power Amplifier (PA) using Polar Modulation techniques needs a DC-DC converter with variable voltage and current for increasing the overall efficiency of the system.

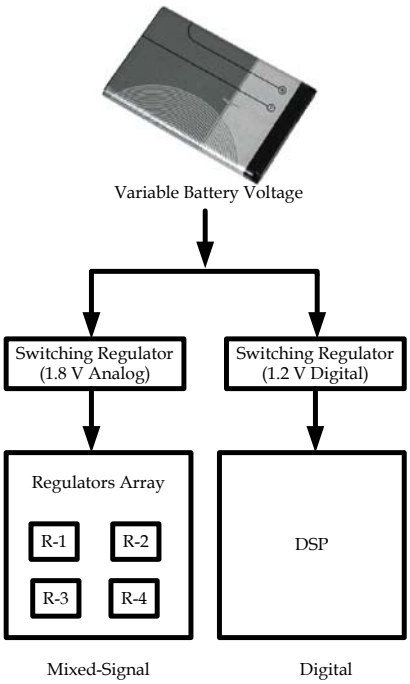


Figure 1-2. DC-DC converter in different part of a portable electronic system

This thesis presents the design procedure of a high efficiency low ripple DC-DC converter, targeted for mobile phone transmitter. In the first chapter design background and different types of DC-DC converters are described. In the second chapter some state of art DC-DC converters are reviewed along with the specifications. Theory of the buck converter is explained in chapter three. Design and Layout of the converter are covered in chatter four and five. Chapter six includes the proposed measurement set up. Concluding remarks and comments for future works are included in chapter seven.

1.1 Background study

First generation mobile phones in mid-90s were used only for voice communications. But in late-90s the emphasis on data services using mobile networks stars to increase. In the Figure 1-3. [32] the increment of data speed of the mobile communication system is shown. For voice communication and lower data rate, constant-envelope modulation is used. In constant-envelope modulation techniques power amplifier have good efficiency. In case of GSM constant-envelope modulation technique is used for sending the information, which allowed the power amplifiers to operate in the saturation region, results high efficiency for the power amplifiers, normally more than 50%. [3] But in the late-90s new modulations techniques are applied for increasing the data speed. The envelopes of these modulated signals are not constant, which reduce the efficiency of the power amplifier. The amount of efficiency reduction of the power amplifier depends on the crest factor of the modulation techniques [3]. Peak to average ratio of the signal known as the crest factor increases with data speed. Increment of the crest factor decreases the power amplifier efficiency. For EGDE, UMTS AND CDMA2000 the crest factor is about 3.2 dB which reduces the power amplifier efficiency below 25% [3]. The latest telecommunication standards like LTE and WiMAX have even higer crest factor due to the higher data rate. LTE has a crest factor of 6.5dB and WiMAX has the uplink crest higher than 12dB [3]. Due to the low efficiency of PA, it is not suitable to use the same techniques in the system for transmitting modulated signal. New techniques such as use of supply modulators in the system are developed to increase the efficiency of the PA. Moreover the PA of the mobile phone consumes most of the power of the battery. The supply modulator of the PA needs to be efficient to have a good over all efficiency of the system. And at the same time it should not add extra noise to the information signal. There are several ways to improve the efficiency of the system by using a high efficiency DC-DC converter in the system as supply modulator. Some of the methods are: slow tracing, envelop tracking and polar modulation techniques.

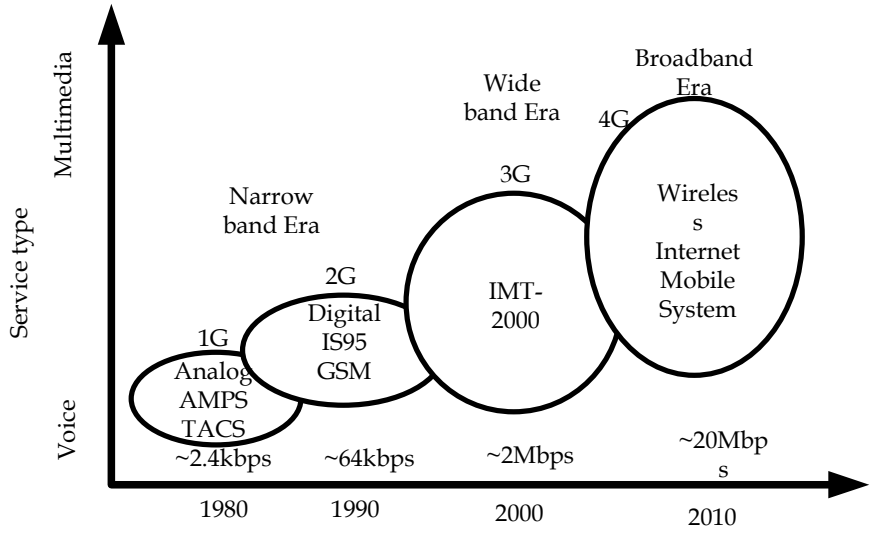


Figure 1-3. Increment of mobile data speed with the evolution of mobile communication system. [32]

In the Figure 1-4 slow tracking, envelope tracking and polar modulation techniques are shown for transmitting information using a supply modulator. In slow tracking process, the PA is supplied by slightly higher voltage than the largest peaks of the envelope. This process tracks the comparatively slow changes in the average transmitter output power and recovers lost efficiency due to power-control back off. The second process named as envelope tracking, refers supplying the PA with a voltage which tracks the instantaneous changes in the envelope due to the modulation. Hence, this process offers the benefit to recover lost efficiency due to both modulation and power-control back off. But the problem is that the bandwidth of the tracking signal increases a lot. In this method the gain does not compressed too much thus the noise at the PA output decreased by several decibels. In case of polar modulation the PA worked in the saturation region. The noise and bandwidth increases a lot but the efficiency is much higher than the previous two cases, because the power supply of PA is same as the highest peak of the modulated signal. The efficiency increased significantly due to the virtue of the saturation and good RF filter is needed before transmission of the signal [3].

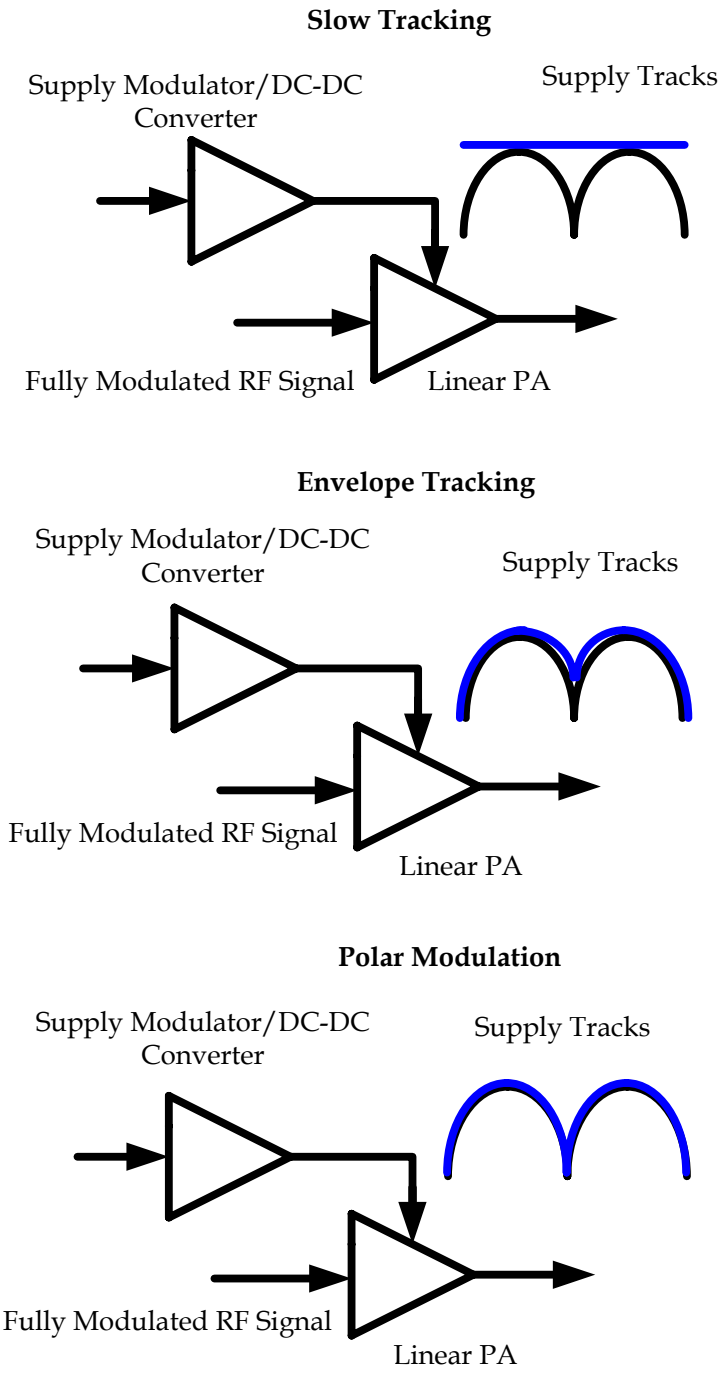


Figure 1-4. DC-DC converter used as a supply modulator in different tracking regime for increasing the efficiency of PA [3].

1.2 Converter types

DC-DC converters can be divided into different categories depending on the properties of the converters. They can be divided into linear and switching converters depending on circuit operation. There are several different topologies for designing converters with in each group. Switching converters can be divided in to LC type converter and switched capacitor type converter. In the Figure 1-5 the classification of the converters are shown. DC-DC converters can also be divided in to buck, boost and buck-boost types depending on the output voltage options. Buck converter has lower output voltage compare to the input voltage, and boost converter provides higher output level compare to input level. Buck-boost converter can give both lower and higher level of output.

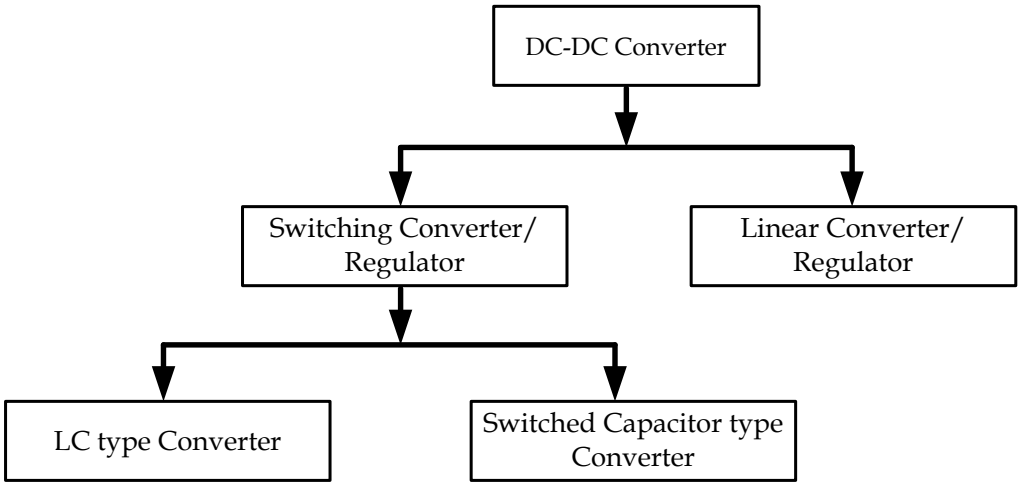


Figure 1-5. Classification of DC-DC converter depending on working principle.

In linear converter or regulator transistors are operated in the active region. They are small in size and easy to design. But linear regulators are limited by their efficiency, as it works by taking the differences between the input and output. The efficiency of these regulators is in the range of low to medium (<81%) [33], [65]. The amount of heat production increases with the increment of difference. The efficiency of theses regulators are limited by the ratio of output to the input voltage. Maximum efficiency is achieved when output is equal to input. A scaled down output signal is compared with internally generated reference signal to give a constant output. There is no switching component in linear regulators. These types of regulators are more popular where size is more important compare to efficiency. Linear regulators have lower settling time and ripple. They generate less noise compare to switching regulators. These regulators are also known as Low Dropout Regulators (LDO). Linear regulator can only be buck types.

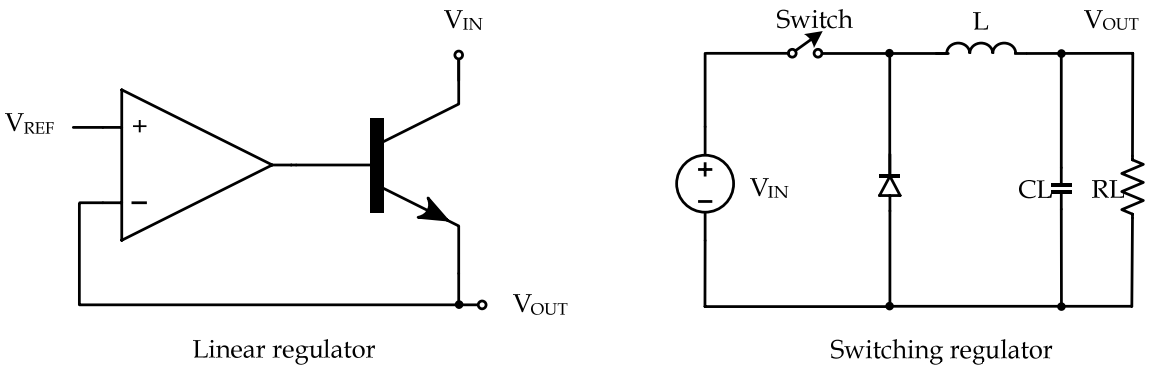


Figure 1-6. Simplified diagram of linear and switching regulator.

The transistors of the switching regulator work in saturation or cut off region. Switching regulators work by transferring energy in discrete packets from input to output. This is done by a low-resistance switch and controlling the rate of energy transfer. When the switch is off, current through it is zero. And when the switch is on voltage over it is zero. Therefore the power losses are small, ideally zero. Therefore high efficiency can be achieved using switching regulator. Switching regulators can be buck, boost and buck-boost types. These regulators use capacitor or inductor as an energy transferring element from input to output. Depending on the charge transfer elements switching regulators can be divided into switched capacitor (SC) type and LC type. These two types of converters are more popular in modern analog and mix-signal design in CMOS and Bi-CMOS process.

Table 1-1. Comparison of linear and switching regulator

Property of comparison	**Linear Regulator**	**Switching Regulator**
Transistor operating region	Transistors are operated in active region.	Transistors are operated either in cut off or saturation region
Efficiency	Linear regulators have lower efficiency [33], [65].	Switching regulators have higher efficiency (70-95%) [33].
Out put voltage options	Only step down operation.	Both step-up and step-down operation.
Noise	It generates little noise at the output.	Switching regulators may produce considerable noise at output.
Size	Small	Bigger compare to linear regulator
Design complexity	Simple	Complex in design

1.2.1 SC type converter

In SC type converter, capacitor works as energy transferring element. Capacitors are easier to integrate in CMOS design compare to inductors. Fully integrated switched-capacitor (SC) converters have recently received increased attention form both academic and industrial researchers. As for example in the paper [4] and [6] two fully integrated switched capacitor converters are describes, where multi-phase interleaving is done for ripple reduction. The size of the capacitor depends on the frequency of operation. Higher frequency operation allows smaller valued capacitor to use. But the losses in the capacitors especially the losses in the bottom plate restrict to attain very high efficiency in fully integrated SC type DC-DC converters. There are several other advantages of using switched capacitor converters, some of them are [7]:

- No inductor needed
- Minimum EMI
- More than 90% efficiency is achievable.
- Low cost and compact.

1.2.2 LC type converters

LC type switching converter can achieve 80% efficiency easily, which makes them most popular types of DC-DC converter. With carefully analysis of the loss components of the LC type converter and by optimizing them more than 90% efficiency can be achieved. In the modern CMOS technology LC type converters are widely used due to this reason and a lot of research work is going on this topic. Higher efficiency increases the battery life and longer battery life makes portable electronic goods more popular in the market. This thesis work is on LC type DC-DC converter. Though LC type converters have higher efficiency compare to other converters, they have several disadvantages such as:

- Electro-Magnetic Interference,
- Complexity in design,
- External inductor is needed, which increases the size and costing,
- In some CMOS process internal inductor is used but the quality factor of the inductors is low. High series resistance of the inductor degrades the efficiency of the converter. They also need lot of silicon area.

1.3 Conclusions

DC-DC converter is one of the important elements of the power management unit. In the mobile phones, as the numbers of features are increasing, the power consumption is also increasing. These results lower operating time of the mobile phones. The high efficiency DC-DC converter can increase the operating time by decreasing the power consumption. The efficiency of the PA of mobile phones is decreasing as the peak to average ratio is increasing, with higher data rates. For increasing the efficiency of power amplifier supply modulators are used. High efficiency DC-DC converter can be used as the supply modulator. There are different kinds of DC-DC converter. SC type and LC type are most suitable for modern CMOS technology. Both of them have their own advantages and disadvantages. SC type converters are smaller in size and LC type converters have higher efficiency. The choice of the converter depends on the application.

2 Review of LC-type DC-DC converter

In this chapter some of the recently published LC type DC-DC converters for power amplifier amplifiers are reviewed. High efficiency DC-DC converters with low output ripple are needed for the supply modulator of PA. Higher efficiency is achieved by minimizing the losses in different sections. The operating frequencies of the converters are made higher to decrease the inductor size of the converters. Most common method for reducing ripple is to interleave the output.

2.1 State of art LC-type DC-DC converter

In recent year's lot of state of art LC-type DC-DC converter are designed, for different applications. Comparing DC-DC converters are not straight-forward, some properties need to specify for comparing. This converter will be used as the supply modulator of power amplifier of mobile phones. So it would be more suitable to compare the designs by comparing the specifications of DC-DC converter used for PA modulation. Table 2-1 presented some recently published LC-type DC-DC converter implemented in submicron CMOS technologies.

Table 2-1. Comparison of LC type DC-DC converter .

Ref. #	V_{IN} [V]	V_{OUT} [V]	f_{switch} [MHz]	L [uH]	η [%]	Output ripple [mV]	I_{Load} (max) [mA]	P_{OUT} [W]	Si-area [mm²]	Tech.	Application
[9]	4	2-3	5-10		89	<4	1100	3.2	1.5	0.25 μm CMOS	GSM/ EDGE/ UMTS
[11]	3.3	0.3-3	10	30		<2	750	2	4.62	0.35 μm CMOS	CDMA
[12]	2.7-4.3		130	2× 0.11	83	-60dBc	750	2	0.86	0.25 μm LDMOS	WCDMA
[13]	3.3	0.3-3	2.12/2.88 /3.75	2.2			0-750	2		0.13 μm CMOS	EDGE/ WCDMA/ WiMax
[14]	3.6/ 3.3	0-2.9	10	5.3	75.5		420	1.2	4.2	0.25 μm CMOS	GSM900
[15]	1.2	0-1.15	118	0.80		<4.3		0.186	1.32	65nm CMOS	WLAN
[16]	3.3	0-1.15	3.4/1.6/ 7.1				700			65nm CMOS	EDGE/ WCDMA / LTE
[17]	3.4	0.5-4.5	3-6					0.525/0.4 07	4.42	65nm CMOS	LTE
[18]	3.3	0.4-2.8	10	2×0.5		<40	725	2	3.09	0.35 μm CMOS	WCDMA

A high efficiency power supply modulator for PA for GSM, EDGE and UMTS is presented in [9]. This supply modulator combines a high-bandwidth class-AB linear regulator and an efficient DC-DC converter in a master slave configuration. The DC-DC converter is designed based on current mode control topology and optimized for 1MHz to 25MHz switching frequency. Maximum efficiency 89% is achieved at 600mA load current. The output ripple is suppressed by a third order dual inductor LCR filter. The peak output power of the circuit is 3.2W and has current ripple less than 4mV. The supply modulator is fabricated in 0.25 μm CMOS process and has an active area of 1.5 mm².

The PA regulator described in [11] has output ripple less than 2mV and it designed for CDMA transmitter. This converter has also master slave configuration like previous one with maximum efficiency of 82%. The low frequency content of the envelope of the modulated signal is provided by a synchronous DC-DC converter while high frequency content is

supplied by the rail-to-rail class-AB amplifier. A low loss output current sensing circuit is used for output ripple and extending the overall bandwidth. This modulator is fabricated in 0.35µm CMOS process and has an active area of 4.62mm^2. This regulator has a bandwidth of 10MHz, with less than 0.2% envelops error which makes it suitable for CDMA applications.

A 130MHz PWM mode DC-DC converter is described in the publication [12] by V. pinon et al. from STMicroelectronics for WCDMA. A polar modulation technique is used for high efficiency, which is 83% at maximum 2W output power. Careful PCB design can keep the switching harmonies below -60dBC. The test chip area is 0.86mm^2, fabricated in 0.25µm RF-CMOS process.

A DC-DC converter for multi-standard applications is described by [13]. A hybrid switching supply modulator with programmable hysteric comparator enables multimode operation of this supply modulator. The maximum efficiency of this modulator is 89% and capable of provide 2W of power. The test IC is fabricated in 0.13um CMOS process.

In the paper [14] combined delta-modulated switch-mode PA supply modulator is presented. The circuit is implemented in 0.25µm CMOS process and has an area of 4.2mm^2. The maximum efficiency is 75.5% for 30.8dBm output power.

A wideband modulator is described in the paper [15] which has a bandwidth of 285MHz. The highest efficiency of the IC is 87.5%. It is realized in 65nm CMOS process having an area of 1.32mm^2. The modulator is based on cascaded miller compensated linear amplifier and a class D switching amplifier. The modulator has a bandwidth of 20MHz and designed for polar modulated PA. It has maximum ripple of 4.3mV at 118MHz switching frequency.

Another multiband supply modulator for PA applications is explained in the paper [16]. Here multimode operation is achieved by an envelope tracing techniques with a programmable hysteresis control and automatic switching current adaptation. A linear broadband class E amplifier is used here for output. Maximum efficiency of this converter is 90%. The IC is fabricated in 65nm CMOS process.

In [17] a high efficiency and wideband envelope tracking power amplifier with sweet spot tracking is presented. Sweet spots are local minimums of inter modulation distortion (IMD) and occurred by cancellation of harmonics. The efficiency is maximized by modulating supply voltage of PA and linearity is improved by envelope tracking and sweet spot tracking. Maximum achieved efficiency for this IC is 75%. The IC is fabricated in 65nm CMOS process and the total silicon area is 4.42mm^2.

A hybrid supply modulator with interleaving the outputs for low ripples, wideband and high efficiency class AB linear amplifier is described in [18]. Two–phase switching is implemented to lower the inductor current ripple. The IC is fabricated in 0.35µm CMOS process and the total silicon area is 3.09mm². The test IC has a good efficiency of 89%, which is usually 9% higher than conventional converters.

From these reviewed paper, DC-DC converter in [18] is chosen as a reference paper for further investigation and development. The goal of the development is to implement a DC-DC converter for WCDMA application with low ripple, high efficiency and small silicon area.

2.2 Specifications

Depending on the above state of art DC-DC converters, competitive specifications are proposed for the converter design targeted for the PA of the transmitter of WCDMA. In the table 2.2 the list of the specifications are given where the peak efficiency is more than 90%.

Table 2-2. Specification of the DC-DC converter

V_{IN} [V]	V_{OUT} [V]	f_{switch} [MHz]	L [uH]	η [%]	Output ripple [mV]	I_{Load} (max) [mA]	P_{OUT} [W]	Si-area [mm²]	CMOS Tech.	Application
3.3	0.5-3	10-100	0.1-1	>90	<10	700	2	<1	45 nm	WCDMA

2.2.1 Efficiency

Efficiency is the measure of how much energy is transferred from the input to the output. It is defined as the ratio of output power to the input power and represent in terms of percentage. Theoretically 100% efficiency is achievable for switching DC-DC converter, but different losses in the circuits limits the efficiency. The input power is the product of input current and input voltage. The DC-DC converter in this thesis has three different inputs or power supply, two supplies for two drivers and one battery power supply. So for calculating the efficiency all the inputs are considered. Similarly, output power is the product of output current and output voltage which are shown by the equations 2.1-2.3.

$$P_{IN} = V_{BAT} I_{BAT} + V_{PMOS\_driver} I_{PMOS\_driver} + V_{NMOS\_driver} I_{NMOS\_driver} \quad (2.1)$$

$$P_{OUT} = V_{OUT} I_{OUT} \quad (2.2)$$

$$efficiency, \eta = \frac{P_{OUT}}{P_{IN}} \tag{2.3}$$

The current flowing form the battery and the current at the output are switching. So the equations of the input power and the output power are modified and the average of the voltage and current are taken for calculating the efficiency.

2.2.2 Output ripple

It is expected that the output of the DC-DC converter is clean DC. But due to the switching operation, the output voltage varies over time. The ripple is like a small ac signal is imposed on DC signal. A typical example picture is shown in the Figure 2-1. Here ΔV represents the amount of ripple voltage, where V_{avg} is the average of the voltage.

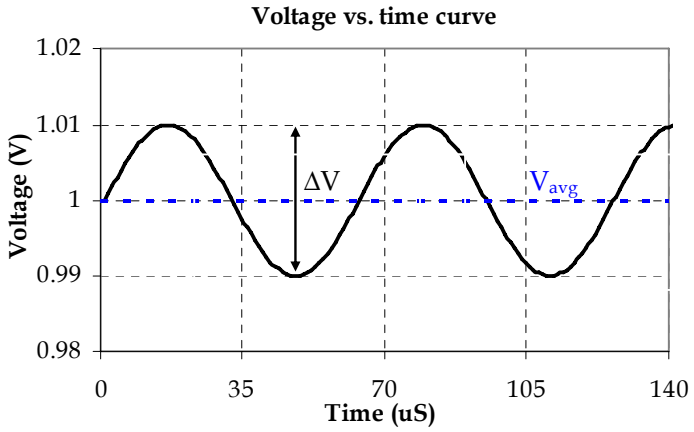


Figure 2-1. voltage vs. time curve for showing the ripple..

The ripple requirement is small for WCDMA, GSM, EGDE, 3G and other wireless communication standards. State of art DC-DC converters which are presented here have less than 40mV output ripple voltage.

2.2.3 Output power

Output power is the measure of the maximum amount of power than can be deliver to the load by the DC-DC converter. And the equation for measuring the output power is already given by equation 2.2. The output power rating for a WCDMA application a mobile phone PA is 2W.

2.2.4 Frequency of operation and inductor sizing

There is a simple relationship between the switching frequency and inductor size. Higher switching frequency allows using lower valued inductor. But higher switching frequency increases switching loss and degrades the efficiency. Smaller valued inductor increases the output current ripple. There is a trade off between the ripple, inductor sizing and switching frequency. The switching frequency of a the supply modulator of a RF PA must be roughly ten times the maximum frequency of the envelope the output ripple does not degrade the performance of operation of the whole system [21],[22].

2.3 Conclusions

The state-of-the-art LC type DC-DC converters are reviewed in this chapter. All the state of art DC-DC converter in this chapter has good efficiency, low ripple and lower silicon area. The specifications of this work is set competitive, like the state of art DC-DC converters. For achieving good efficiency, low ripple new techniques are applied in design, but this increases the complexity in the circuit and increases the silicon area. Thus trade offs are needed among these parameters.

3 Basic Theory of DC-DC Converter

This chapter discusses the DC-DC converter circuit topology and design consideration that is chosen for implementation. The basic theory of synchronous switching DC-DC converter is explained in the first part of the chapter. Then the design procedures of different sections are given. Finally in the last part of the chapter, different considerations for maximizing efficiency are explained which will be implemented in this design.

3.1 Basic concept

A buck converter has lower output voltage than input voltage. In Figure 3-1 a) the block diagram of a LC type synchronous DC-DC buck converter is shown. The converter gives a regulated output V_{OUT} from the unregulated V_{BAT} power supply. Here the inductor works as an energy transferring element. Two switches Sw-1 and Sw-2 are synchronously controlled. When Sw-1 is conducting, V_X is connected the input of the low pass filter. At this time the switch Sw-2 off and the input V_{BAT} is providing energy to the inductor. When Sw-2 is on, the inductor current flows through it, and the stored energy in the inductor transfer to the load. These two switches chop the battery voltage into square pulses which have an average output voltage equal to the desired output voltage [19]. A pulse width modulation technique is used to control the width of the chopped voltage that has an average value equal to the expected output level. The switches can be designed either BJT or MOSFET. In the Figure 3-1 b) MOSFET implementation of synchronous DC-DC converter is shown. A low pass filter consists of an inductor and a capacitor attenuates the harmonics and gives a DC output voltage with acceptable AC ripples. The cut-off frequency of the filter is chosen much lower

than the switching frequency for ripple reduction. In the Figure 3-2 the timing diagram of the DC-DC converter is shown.

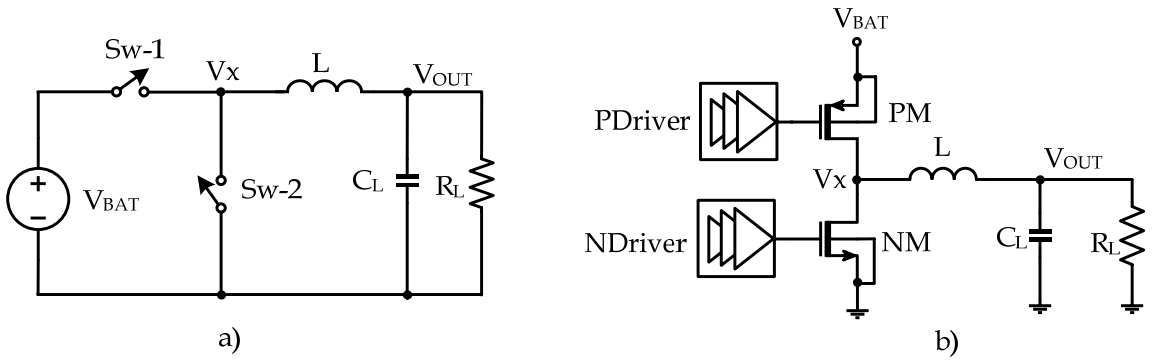


Figure 3-1. a) Simplified block diagram of a buck DC-DC converter, b) MOSFET implementation of buck DC-DC converter

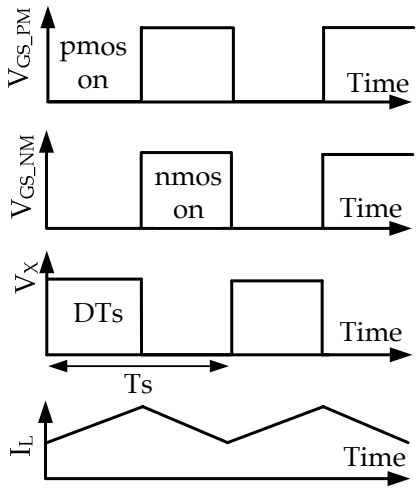


Figure 3-2. Timing diagram of gate drive voltages, switching node voltage and inductor current.

The output voltage level of a buck converter depends on the duty cycle of the gate drive voltage. In steady state operation the integral of the inductor voltage over the switching period is zero. The relationship between the input and output voltage can be shown by the following equation 3.1, when the system is ideal. For practical case the losses are added and the V_{OUT} voltage is lower than this calculated value.

$$V_{OUT} = D \times V_{BAT} \tag{3.1}$$

Where, D is the duty cycle of the switching pulses.

DC-DC converter design stars with the sizing of the switches for maximum efficiency. The driver stages for the switches and the filter stages are design once the switches are optimized. The losses in all the stages are minimized for maximum efficiency.

3.1.1 Converter losses and efficiency

Theoretically switching DC-DC converter can achieve 100% efficiency, if the converter is made of ideal components. But due to several losses the efficiency decreases. For a switching DC-DC converter more than 75% efficiency can be achieved easily, but with careful analysis of losses and by minimizing them more than 90% can be achieved [20]. The main losses of switching converters are: conduction loss, gate drive loss, capacitive switching loss, short circuit loss and body diode reverse recovery loss [20]. The driver stages losses are consist of conduction loss, switching loss, short circuit loss etc. The filter element losses are mainly conduction loss due to the inductor parasitic resistance.

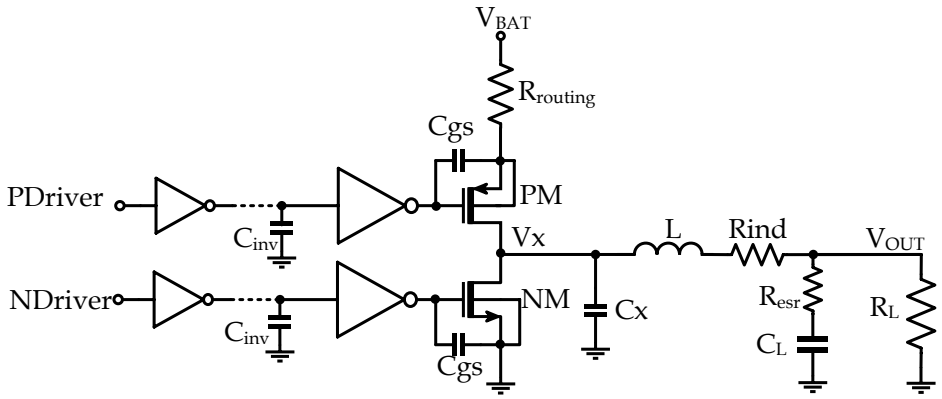


Figure 3-3. DC-DC converter with loss components in the practical circuits [20].

Conduction loss: Conduction loss in the switches occurs due to the resistive component of non-ideal switches and parasitic resistance of interconnections. Conduction loss represented by [20],

$$P_{cond} = i_{rms}^2 R \tag{3.2}$$

Gate-drive loss: When the gate drive voltages of mosfets changes their states, they dissipates an average power. The amount of the power dissipation increases with the increase of the mosfets size. The dissipated power can be expressed as [20],

$$P_g = E_g f_s \tag{3.3}$$

Where, E_g is directly proportional to the gate energy transferred per cycle, and this also include energy losses due to the miller effect and losses in the drive circuitry.

Capacitive switching loss: Due to the charging and discharging of the parasitic capacitance of the mosfets PM and NM, power dissipates in each cycle. The parasitic

capacitance will include drain to body junction capacitance C_{db}, gate drain overlap capacitance C_{gd}, wiring capacitance from their interconnections and stray capacitance associated with the filter capacitance. The loss can be found by the following equation [20].

$$P_C = C_{parasitic} V_{in}^2 f_s \tag{3.4}$$

The parasitic capacitance, $C_{parasitic}$ will also include the capacitance of bonding pads and off- chip bonding wire, if the external inductor is used. In the case of soft switching the power loss reduced to half of P_C.

Short circuit loss: A short circuit path exits temporarily between the battery and ground when the switch gate drive voltages change their stages, like the inverter transition period. Because at that time both the switch are on for a small amount of time and short circuit current flows directly from the supply to the ground. But this phenomenon can be stopped introducing dead time between the switch transitions, which is explained later in this chapter.

Body diode reverse recovery loss: If the duration of the dead time is high, then the body diode of the NM are forced to forward bias to pick up the inductor current for a fraction of time in each cycle. And if the forward biased body diode voltage is comparable to the output voltage then a significant amount of current flows to the ground causes the conduction loss given by the equation 3.5. When the mosfet PM is turned on, it removes the excess minority carrier stores in the body diode of the PM and dissipate an energy given the equation [20],

$$E_{rr} = Q_{rr} V_{in} \tag{3.5}$$

Where Q_{rr} , is the stored charge in the body diode.

Driver loss: The driver stage loss consists of all the losses explained earlier in this section. But the loss is small comparing to the losses of transistor PM and NM. Because PM and NM are considerably big compare to the driver stages.

Filter-element loss: Resistive element of the inductor causes the conduction loss in the filter. In addition to this the filter elements have dielectric loss in the capacitor, charging and discharging loss of capacitor in each cycle and inductor core losses. At higher switching

frequency the conduction loss increases, because the resistance of the inductor increases due to the skin effect and proximity effect [34].

3.1.2 Synchronous switch design

The efficiency of the converter can be improved by designing the switches for low losses. The current flowing through these switches of this converter is high, 700mA for maximum output. The on resistance of the mosfets should be as low as possible to reduce the dissipation loss, which is one of the main losses for efficiency reduction. The on resistance of mosfetes is calculated using following equation [35].

$$r_{on} = \frac{L}{\mu C_{ox} W (V_{GS} - V_T)} \tag{3.6}$$

For decreasing the on resistance the width of the mosfets is made as big as possible, but bigger mosfets has higher parasitic capacitance. In each cycle there will be loss for charging and discharging of parasitic capacitance. A trade off is required between the resistive loss and capacitive loss of the mosfets [19]. The expressing for the optimum values for the widths of the nmos and pmos transistors are as follows, considering all the losses in the mosfets [36] [19].

$$W_{NMOS} = \frac{I_L}{V_{BAT}} \sqrt{\frac{1}{(b+1)\frac{\mu C_{ox}}{2} f_s (V_{BAT} - V_t)}} \tag{3.7}$$

$$W_{PMOS} = b W_{NMOS} \tag{3.8}$$

Where, I_L is the current through the inductor, V_t is the threshold voltage of the mosfet, b is the ratio between the electron and hole effective motilities, f_s is the switching frequency, V_{BAT} is the battery voltage, μ is the electron or effective mobility, C_{ox} is the gate oxide capacitance per unit area.

3.1.3 Output filter design

The square wave generated by the synchronous switch is passes through filter to suppress the harmonics of the square wave. The filter is a second order LC type low pass filter, which passes the DC component of the switching node (V_x) and attenuates the AC component to an acceptable ripple voltage [20]. For a dynamic power supply of PA, the filter response is expected to critically damped (ξ=0.707), for which the step response is well

damped and the 3dB cutoff frequency coincides with the undammed natural frequency. The cut off frequency of the filter and the damping ratio are given by the following equations [19].

$$f_{cutoff} = \frac{1}{2\pi\sqrt{LC}} \tag{3.9}$$

$$\xi = \frac{1}{2}\sqrt{\frac{L}{C}}\frac{1}{R_L} \tag{3.10}$$

The inductor current of Figure 3-2 can be found by integrating the voltage over the inductor, for the time period on or off time of the switching. This is shown by the equation 3.11 [33]. The DC component of the inductor current flows through the load and the AC component flow through the capacitor. The magnitude of the AC voltage of the load can be determined using the equation 3.12 [33].

$$\Delta I_L = \frac{V_X D(1-D)}{Lf_s} \tag{3.11}$$

$$\Delta V = \frac{\Delta Q}{C} = \frac{V_{OUT}(1-D)}{8LCf_s^2} \tag{3.12}$$

The output voltage ripple is a function of L, C, duty cycle and output voltage. By increasing the value of L and C output ripple can be decreased. By using the equations 3.9 and 3.10 the value of L and C can be found in the following way [19].

$$C = \frac{1}{4\pi\xi R_L f} \tag{3.13}$$

$$L = \frac{1}{4\pi^2 f^2 C} \tag{3.14}$$

For attenuating the AC component of the switching voltage, the cut off frequency of the filter is chosen as low as possible compare to the switching frequency. But if the cut off frequency is lower the inductor and capacitor size increases. High switching frequency allows using lower valued inductor and capacitor for miniaturizing the DC-DC converter.

3.1.4 Driver design

The sizes of the switch mosfets are usually big, in the rage of mm. To drive them cascaded drivers are needed. Driver stage is consisting of 3-5 stages of inverters connected one after another, with a gradual increment of size of the inverter stages. The ratio of the

width of nmos and pmos is kept 2, as the electron mobility is more than 2 times than the holes mobility [9]. And the ratios of two consecutive stages are kept 4 [38]- [39], to have enough driving power for the next stage and to optimize the propagation delay.

3.2 Design considerations

Beside the design issues explained in the previous sections, there are several other techniques to maximize the efficiency of the converter. When design techniques are applied for efficiency maximization, the cost and the physical size of the converter are also considered. In following sections some design methods such as: high frequency operation, dead time control, zero voltage switching are explained for maximizing the efficiency.

3.2.1 High frequency operation

The inductor in the low pass filter is the biggest component in LC type DC-DC converter. The size and value of the inductor is inversely proportional to the frequency of operation. For lower valued inductor, the operating frequency is higher and it miniaturizes the converter. But higher operating frequency increases the losses in the switches roughly by the square root of the switching frequency, ($\sqrt{f_s}$) and ideally the size of the component decreases by a factor of f_s^{-1} [20]. In the following Figure 3-4 the relation ship between the losses in the switches and the size of the converter is shown. Depending on the design targets the size of the inductor can be chosen which will determine the size, efficiency and cost of the converter.

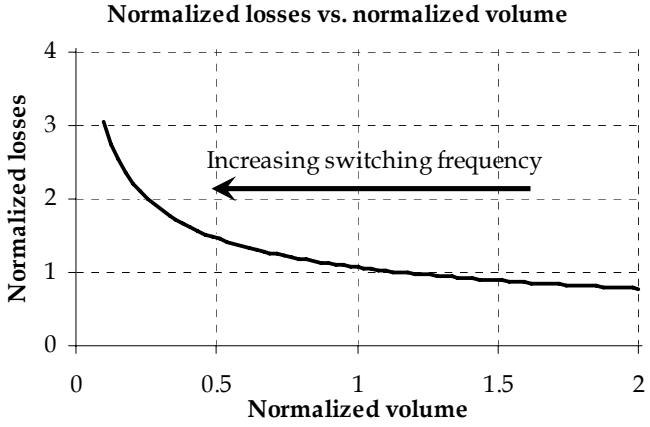


Figure 3-4. Theoretical relationship between the losses in the switches and the volume of the DC-DC converter [20]

There are several factors affect the selection of an inductor. Some of the factors are: DC resistance, quality factor, resonance frequency and the maximum current carrying capability of the inductors. By trade offs among theses parameters the converter can be optimized for high efficiency, while using higher operating frequency.

3.2.2 Zero voltage switching

Pmos and nmos switches of the converter turn on and off synchronously. When nmos is turning on the pmos is turning off in one edge of the gate drive switching voltage and in other edge of the gate drive voltage the opposite phenomena takes places. In case of hard switching, P_C amount of energy dissipates in every cycle and in case of soft switching $0.5 \times P_C$ amount of energy dissipates in each cycle. In addition to that there is short circuit current loss in every cycle, because there is a small amount of time for which the nmos and poms both are partially conducting. This can be stop by introducing a dead time between the pmos and nmos gate voltage pulses, where both the mosfets are forced to enter in off condition for a shot period of time. If the time is small there will be short circuit loss. If the time is big there will be reverse recovery loss, becasue when both the nmos and pmos are off, the magnetic energy stored in the inductor forced the body diode of the nmos to conduct and a path created to ground. In case of soft switching circuit the filter inductor works as a current source to charge and discharge the $C_{parasitic}$ capacitor in a lossless manner. This charging current is the inductor current which normally flows to ground, when the nmos is on. But instead of going to ground this current charged the capacitor. This capacitor is discharged to the load and thus recovers some energy. More capacitor can be added to V_X node to regain all the energy which is going from inductor to ground, but the extra capacitance will slow down the V_X node. At this charging and discharging time of the capacitor appropriate dead time can be set, to set the switching voltage of power transistors zero (V_{ds}=0) [20]. This will eliminate the associated switching loss. In the paper [40] the efficiency of a synchronous buck converter improved by 7% for using zero voltage switching. In this design only the concept of dead time is applied to recover the lost energy. In future work zero voltage switching will be applied. The Figure 3-5 shows the concept of dead time. Two conditions are shown in the figure. In the Figure 3-5 a) there is no dead time introduced, so there is a short period of time when both the mosfets are conduction. In b) there is a small amount of time when both the mosfets are off at the transitions and stops the short circuit current.

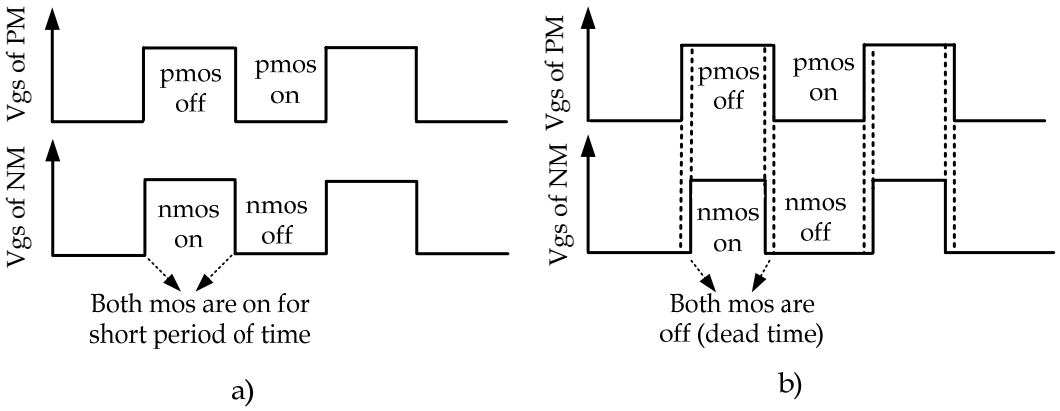


Figure 3-5. DC-DC converter gate drive voltage a) without dead time b) with dead time

3.2.3 Supply voltages of drivers

The gate drive loss of converter increases significantly in higher frequencies. There are several ways to decrease or recover this lost energy in the gates. One of the popular methods for recovering this lost energy is to use resonator circuits, which are explained in the reference [23]–[25]. However, this method increases the complexity of the design. There is another simple approach to reduce the gate drive dissipation loss, by lowering the gate energy consumption per cycle [20]. This is achieved by lowering the voltage swing of gate drive voltage. The gate swing V_{gs} set between zero (V_{gs} =0, for off condition) and some other gate voltage V_g (for on condition) for nmos, for which the condition $V_{gs}>>V_t$ is satisfied. In the case of pmos, V_{gs} set between V_{BAT} (V_{gs} = V_{BAT}, for off condition) and some other gate voltage V_g (for on condition), for which the condition $V_{sg}>>V_t$ is satisfied. Where V_t is the threshold voltage. But lowering the gate drive increases the on resistance of the switch which is shown by the equation 3.6. As a result the conduction loss increases. The gate drive voltages of the switches are optimized for minimum total loss to obtain maximum efficiency.

3.2.4 Cascode devices

According to Moore's low the number of transistors in an integrated circuit, which can be fabricated in the same area in silicon, is getting doubled in every two years [41]. Several measures in integrated circuit design like size, cost, density and speed of the components are also following this law [41]. The gate length sizes and oxide thickness of the transistors are also decreasing to increase the density of the transistors in the integrated circuits. With the decrement of the oxide thickness the supply voltage of the devices

decreases with the ratio of scaling factor [42] [46], because the breakdown voltage of the mosfets decreases with oxide thickness. In the Table 3-1 the decrement of the supply voltage of the integrated circuits is shown. The standard battery voltage of Li-Ions did not change last few years, same 3.7V Li-Ions battery is used in today's mobile phones and other portable electronics. As a result previous CMOS design techniques are not implementable to modern integrated circuits. New methods are developed to use the latest CMOS technology with same battery voltage. LDMOS technology and use of cascode device are two methods for overcoming this problem. Here the cascode device approach is followed to solve the problem.

Table 3-1: Reduction of supply voltage with the technological node advancement.[43]

Year of Production	**2004**	**2007**	**2010**	**2013**	**2016**
Technology node (nm)	90	65	45	32	22
Supply voltage(V)	1.2	1.1	1.1/1	1.1/0.9	0.9/0.8

In the following Figure 3-6 cascode structure is shown. PMC works as pmos cascade and NMC works as nmos cascade. The cascode devices prevent the power mosfets from break down voltage.

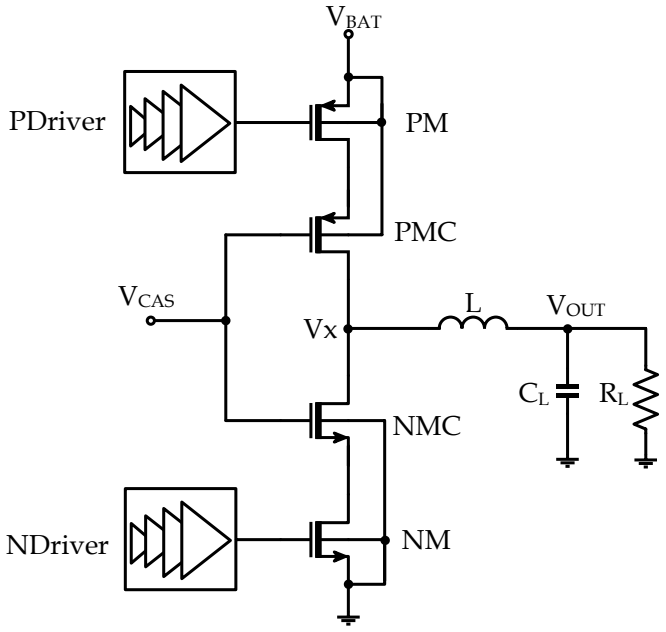


Figure 3-6. DC-DC converter with cascade device

3.2.5 Interleaving

Interleaving is the method where single phase converters are placed in parallel between the input and output. Each of the phases is turned on at equally spaced intervals over the switching period [26]. Thus the output ripple decreases significantly. In the Figure 3-7 pictures are shown for load current for single and two phases. In two phase the ripples are varies with the duty cycle of the gate drive voltages of the converter. For 50% duty cycle the inductors current are 180° phase shifted and load current is ripple free. And the output voltage is directly proportional the load current.

Another advantage of multiphase converter can respond to rapidly changing loads. In multiphase converter the output settled faster than a single phase converter. The load current is distributed among the phases, which allows for using inductors having lower current ratings. But the numbers of the inductors are increased proportionally with the increase of phases. This will result higher cost and larger space in the circuit. Normally in the DC-DC converters for mobile phone applications the two phase interleaving are used. In the Figure 3-8 a DC-DC converter with two phase interleaving is shown. Here phase-1 and phase-2 works in parallel and the load currents are between L_{P1} and L_{P2}.

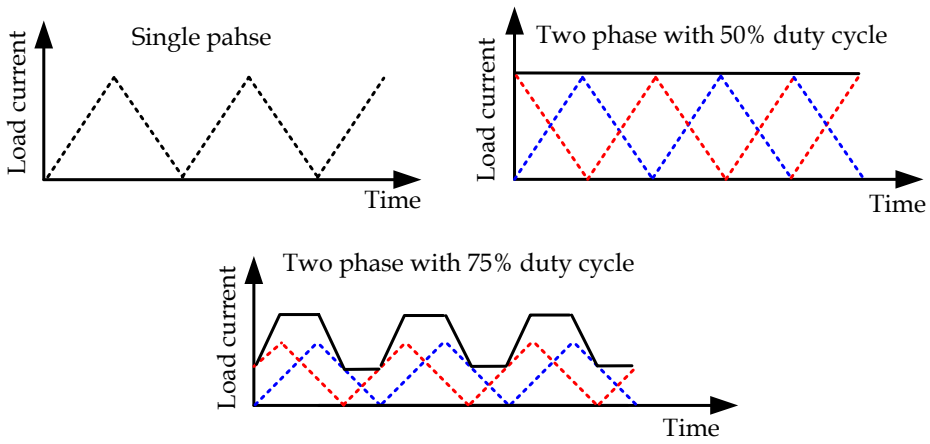


Figure 3-7. Output current curves of single phase and two phase DC-DC converter.

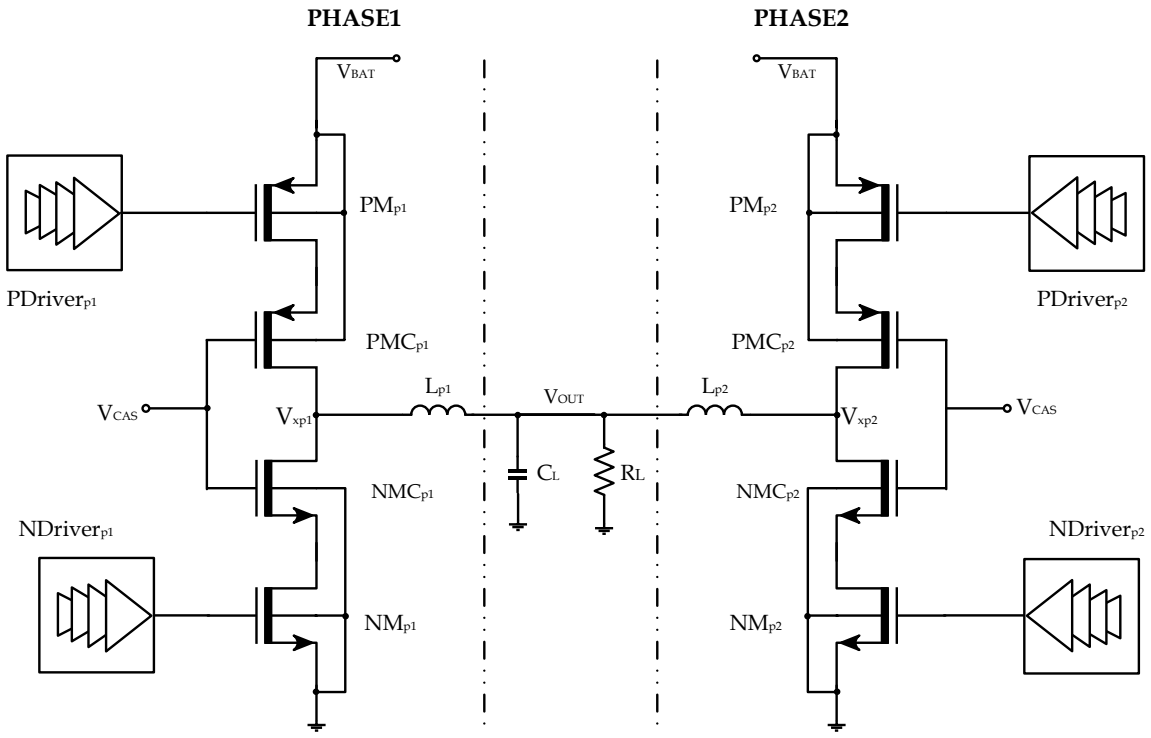


Figure 3-8. 2-phase interleaving for DC-DC converter for decreasing the ripple.

3.3 Conclusions

High efficiency DC-DC converter design needs lot of considerations. Applying the basic theory for designing DC-DC buck type converter more than 75% efficiency can be achieved. But for higher efficiency different losses in the converter like conduction losses, gate drive losses and losses in the driver stage should be minimized. Along with theses considerations applying the concepts of high frequency operation, interleaving, zero voltage crossing switching and optimized gate swing voltage can make the efficiency more than 90%.

4 DC-DC Converter Design

This chapter includes the design procedure of the DC-DC converter. The circuit is designed based on the theory presented in the previous chapter. The electrical design is made utilizing Cadence IC 6.1.3 with SpectreRF tool. Design of the DC-DC converter is done step by step. First the design and simulation is done without the control circuits. Then the control circuits are introduced and simulation is done again with the control circuits.

4.1 Design steps

The converter design is done in four steps. First step is about the transistor sizing and optimizing it considering the efficiency. The second step is about designing the low pass filter. Then the gate drivers are designed and optimized for high efficiency. In the last step the control circuits are designed for generating two phases signal with dead time. In the following sections the design procedure and simulation results are given.

4.1.1 Power mosfet sizing

The widths of the mosfets are calculated using the equations 3.2 and 3.3. Then the values of the widths are optimized using the simulation tools. This design is made for 45nm CMOS process technology. In the library of this process there is no special high voltage mosfets. The break down voltage of the available nmos and pmos are 1.2V and 2V. As the supply voltage for this converter varies form 3.3V to 4.2V, the mosfets having higher breakdown voltage is chosen. One pmos and one nmos cascade are introduced in the design

which is shown in the following Figure 4-1. PMC and NMC works as coscode device in Figure 4-1.

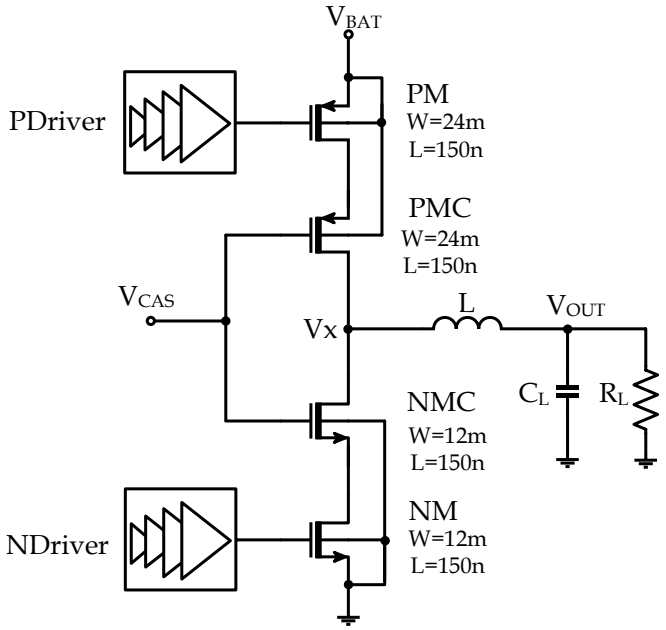


Figure 4-1. Schematic diagram of DC-DC buck converter with cascade devices.

The cascode devices have the same width and length of the synchronous switches. The widths of the devices are optimized for the best efficiency. The optimum width of the transistor is a function of operating frequency which is known from the equation 3.7. The performance of the bigger transistor will be good in terms of on resistance but the parasitic capacitance will increase. So the size is made not too big and not to small.

For calculating the optimum widths of the switches 50 MHz switching frequency is used. Then the calculated values are optimized using simulation, which is shown in the following Figure 4-2. Efficiency of the converter for different width of the transistors are shown in the figure. Considering the efficiency the widths of the pmos and nmos transistors are set 24mm and 12mm.

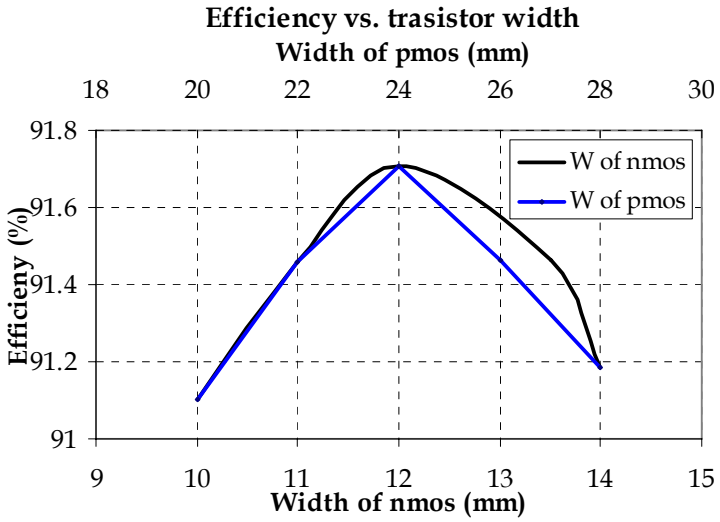


Figure 4-2. Efficiency of the converter for different nmos and pmos width at 50MHz switching frequency. All the simulation is done for 1.8V output voltage and 3.6V battery voltage.

4.1.2 Filter design

The values of the component of the second order low pass filter are calculated using the equation given in equations 3.9 to 3.14. The cut off frequency of the filter is assumed five times lower the lowest switching frequency. The calculated value is justified using simulation. Choosing the inductor for the filter is a critical issue, because the DC resistance of the inductor greatly affects the efficiency. So the inductor having minimum DC resistance should be chosen. For smaller valued inductor DC resistance is lower. But if the inductor having lower inductance is used, in the filter the cut off frequency of the filter is higher and the output ripple increased. If higher value of inductor is used, the DC resistance is higher and the efficiency of the converter drops. For good operation of the inductor the self resonance frequency of the inductor should be at least five times higher than the cut off frequency of the filter. For finding a suitable inductor for the filter the following parameters are considered.

- Inductance
- DC resistance of the inductor
- Quality factor of the inductor
- Resonance frequency of the inductor
- Current conducting capability of the inductor.

Depending on these parameters the following Table 4-1 is made to compare different SMD inductors available in the market. Most of the inductors have current capability of 400-500mA. But the maximum load current of the converter is 700mA. And for single phase converter the output ripple of the converter is higher than the specifications. Both of these problem leads to the solution of interleaving, which is explained in the previous chapter. Interleaving allows to use lower valued inductor by splitting the load current and the same time decreases the output ripple. Comparing all the parameters a 150nH [29] inductor (Model: B82422T) is chosen for the design. The choice of the inductor is justified by simulation.

Table 4-1: Comparison of different SMD inductors available in the market

L [nH]	**R_{max} [mΩ]**	**Q_{min}**	**$F_{resonance}$ [MHz]**	**Current [mA]**	**Core Material**	**Reference**
47	130	45	1900	500		[27]
100	260	40	1310	350		[27]
47	300	26	1200	450		[28]
100	440	28	700	450		[28]
120	220	30	500	450		[28]
47	200	26	1300	450	Ceramic	[29]
100	310	28	900	450	Ceramic	[29]
120	150	30	900	450	Ferrite	[29]
150	**180**	**30**	**700**	**450**	**Ferrite**	[29]
180	190	30	500	450	Ferrite	[29]
47	220	25	1600	470		[30]
100	300	30	1000	400		[30]
47	190	26	1350	510		[31]
100	260	25	1000	440		[31]

In the Figure 4-3 simulation results are shown for different DC resistance of the inductor. With the increment of DC resistance the efficiency drops. For 500mΩ resistance the efficiency drops by more than 5% compare to 200mΩ DC resistance of the inductor. All these simulation is done for 3.6V battery voltage and 1.8V output voltage. The load current for every simulation is 400mA. Lower DC resistance of the inductor will give better results in terms of efficiency. But in that case the inductance will be lower. This will increase the output

ripple voltage. In the Figure 4-4 output ripple voltage vs. frequency curve is plotted for 1-phase and 2-phase. Ripple voltage decreases a lot for 2-phase converter. For less than 25MHz switching frequency ripple voltage of two phase converter is less then 10mV. But in case of 1-phase the ripple is more than 30mV for all frequency. Same simulation condition is used hare like previous case.

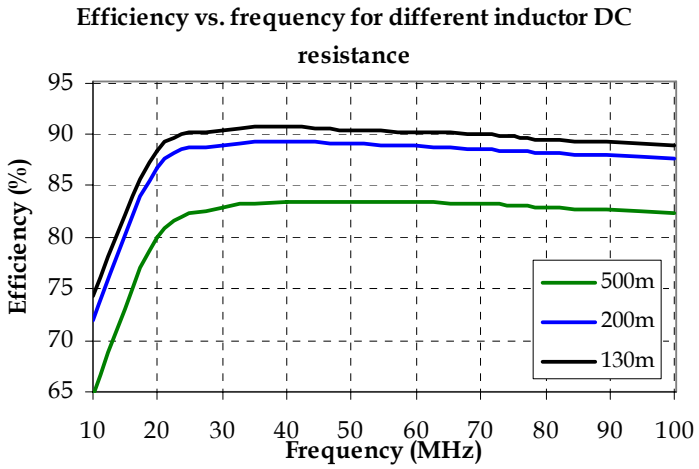


Figure 4-3. Efficiency of the converter for different inductor DC resistance. The efficiency decreases with the increment of DC resistance. The efficiency does not vary too much when inductor DC resistance is less than 200m. All the simulation is done for 1.8V output options.

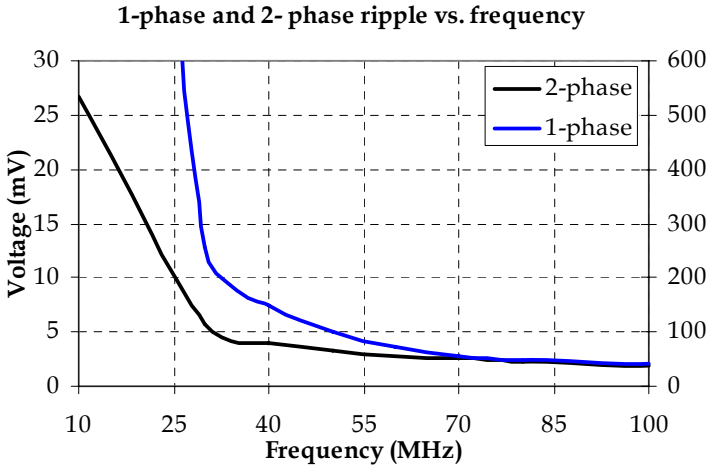


Figure 4-4. Output ripples voltage for 1-phase and 2-phase interleaving. Both the curves are for 1.8V output. The out ripple voltage decreases rapidly for 2-phase inter- leaving.

4.1.3 Driver stage design

A cascaded four stage inverter is used to drive the power mosfets PM and NM. The sizes of the inverter stages increased by four times to maximize the gate drive power and minimize the propagation delay. The pmos and nmos drivers are designed for same propagation delay. To reduce the gate drive losses of the converter the supply voltages of the drivers are reduced. But the on resistance of the mosfet increases when the gate drive is decreased. So the optimum supply voltages for the drivers are selected when total loss is smallest. The optimum supply voltage is found from the simulation. In the Figure 4-5 the driver circuit for the pmos, PM is shown. And in the Figure 4-6 efficiency for different driver supply voltage is shown. The supply voltage is varied to find out the maximum efficiency. When the difference between the supply and ground voltage is 1.2V, the efficiency is maximum and this voltage is chosen for the drivers.

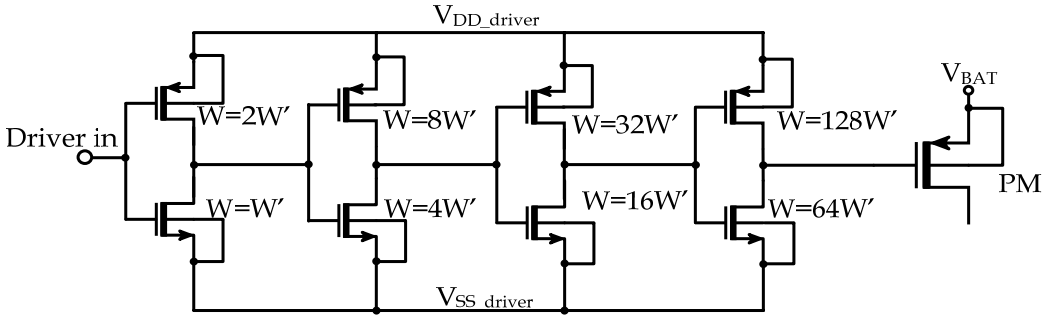


Figure 4-5. Schematic diagram of the pmos driver, showing the sizes of the inverter stages.

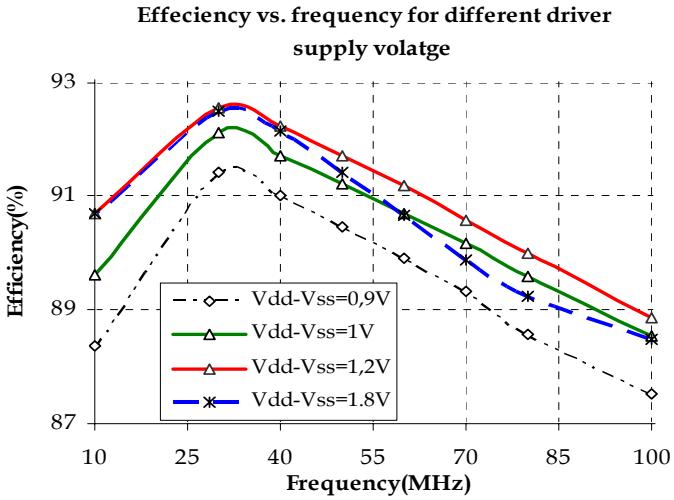
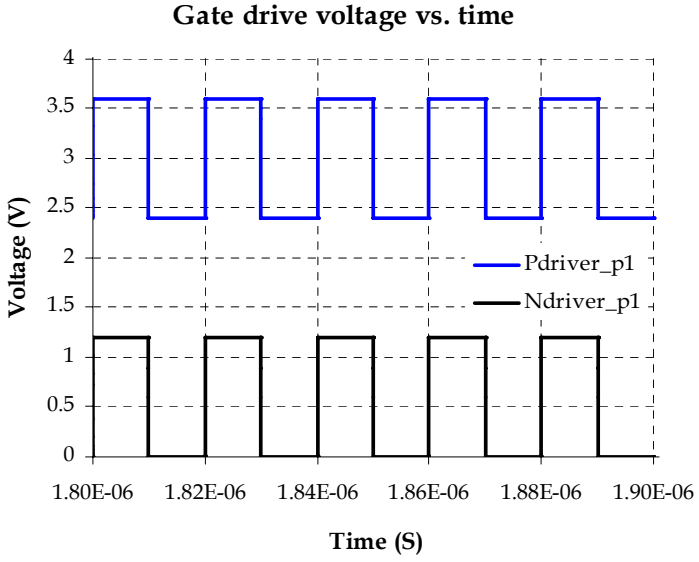


Figure 4-6. Efficiency for different driver voltage. The maximum efficiency is achieved for 1.2V driver supply voltage (V_{supply} – V_{ground} of driver).

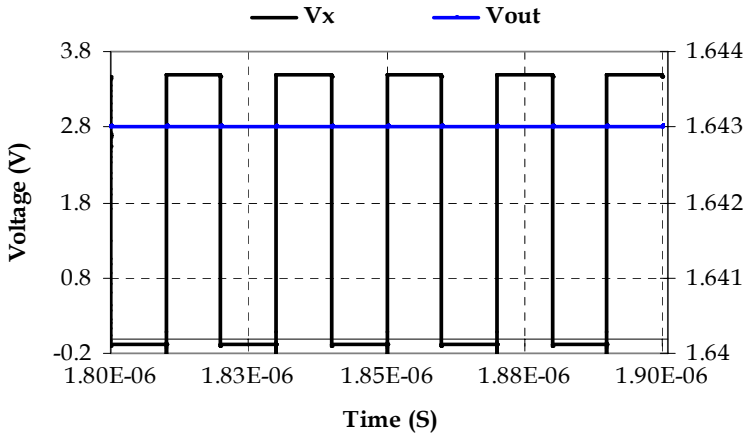
The simulations for the Figure 4-6 is done for 3.6V battery voltage and 400mA load current when the output is settled at 1.8V. After the simulation, the voltages of Figure 4-5 are finalized. V_{dd_driver} voltage for pmos driver is set same as the battery voltage and V_{ss_driver} voltage is set to 1.2V down from the battery voltage. In case of nmos driver supply voltage is 1.2V and ground voltage is zero.

4.2 Simulation results without control circuits

In this following section different simulation results are shown. First few results are related with the timing diagram of the converter. These figures show the behavior of gate drive voltages, the switching nodes, output voltage and the currents through the inductors. Three scenarios are chosen to show the behavior of these curves. In the first case, the duty cycle of the switching frequency is 50% and the frequency is 50MHz. In the second scenario, the duty cycle of the switching frequency is smallest and the frequency is 10MHz. In the third the duty cycle of the switching frequency is more than 90% and the frequency is maximum, 100MHz. Different simulation results related to efficiency vs. frequency for different output voltage, battery voltage and output power are shown after the timing diagrams.



a)



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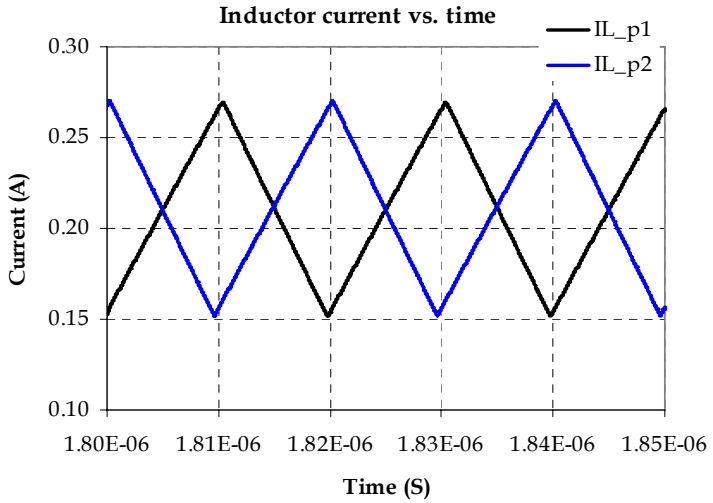
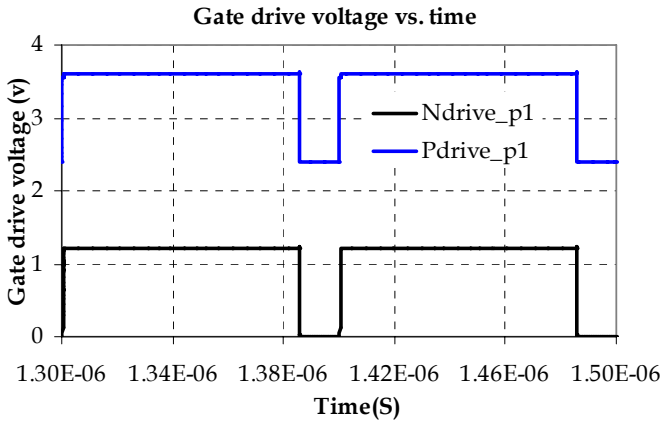


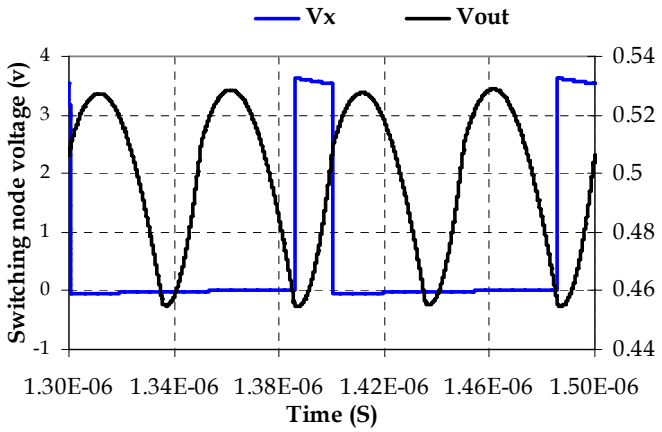
c)

Figure 4-7. Figure showing different timing diagrams of the converter for 50MHz switching frequency when the out put is settled at 1.65V. The simulation is done for the battery voltage 3.6V and load current of 700mA.

In picture Figure 4-7.a) the gate drive voltages for pmos and nmos are shown. The dead time concept is applied here to stop the short circuit losses. In the figure b) the switching node voltage and output voltage are shown in different axis. The output ripple voltage is less than 1mV as the duty cycle is 50%. In the picture c) the behavior of inductor currents are shown. The inductor currents are out of phase resulting very low ripple voltage in the output.



a)



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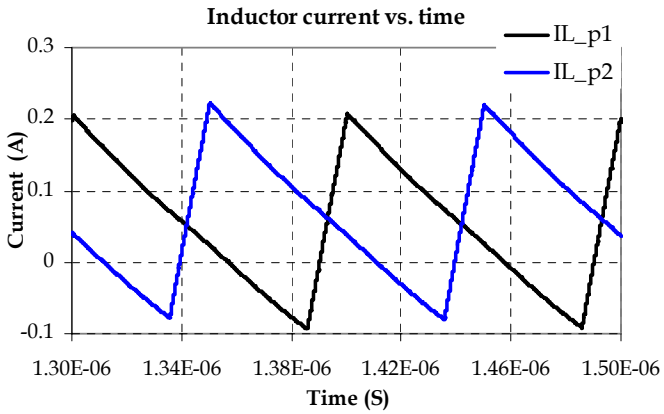
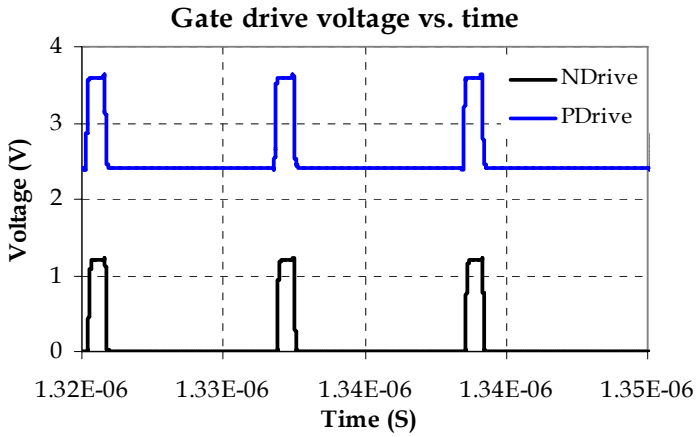


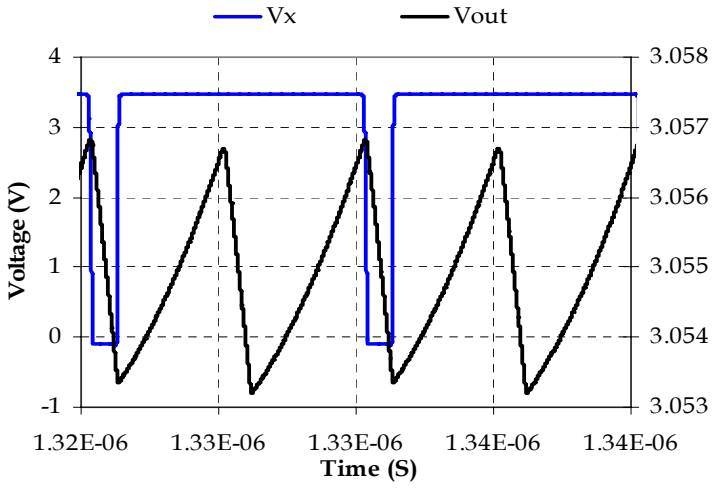
c)

Figure 4-8. Different timing diagrams of the converter for 10MHz switching frequency and 0.5V output voltage are shown in the previous pictures. This is one of the worst conditions in terms of voltage ripple and efficiency because the duty cycle and output power is very low.

In Figure 4-8 a) the gate drive voltages for pmos and nmos are shown where, zero dead time concept is applied like previous picture. In the figure b) the switching node voltage and output voltage are shown in different axis. The voltage at the switching node has an average of 0.5V. The output ripple voltage is 73mV. In the picture c) the behavior of inductor currents are shown.



a)



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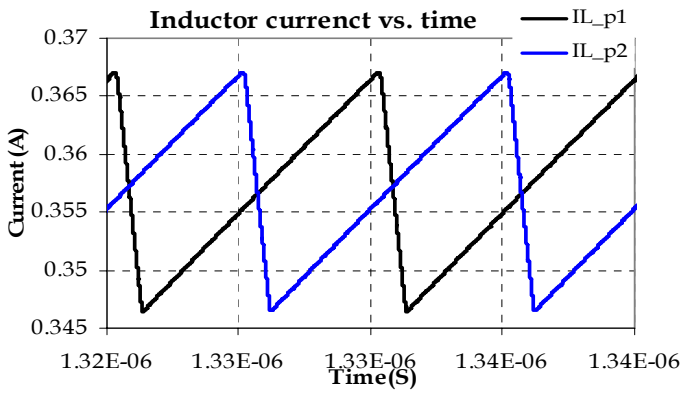


c)

Figure 4-9. Different timing diagrams of the converter for 100MHz switching frequency and 3V output voltage. This is one of the best conditions in term of output power and efficiency but worst conditions in terms of voltage ripple.

In this configuration the pmos is on most of the time and nmos is on for very small amount of time which is understood by the gate drive voltages from Figure 4-9 a) the gate drive voltages for phase-1, b) the switching node voltage goes lower than zero voltage when the current in the inductor gets a path to ground through nmos. The output ripple voltage is 3.6mV. Though the current in the inductors are not perfectly out of phase, the ripple is not very high, because the frequency is high here. In the picture c) the behavior of inductor currents are shown. The timing diagrams shown in the previous sections are done for the 3.6V battery voltage and in all the cases the load current is 700mA.

4.2.1 Efficiency vs. frequency for different output voltage

The size of the power mosfets are optimized for 50MHz switching frequency. But the maximum efficiency is achieved at 30MHz frequency, because the mosfets are sized without considering the losses in other blocks of the design. When losses from different blocks are added the peak efficiency shifted to lower frequency. In the Figure 4-10 curves are plotted efficiency vs. frequency for different output voltage. Efficiency increases with the output voltage level. Maximum efficiency is achieved for 30MHz switching frequency for output voltage level 3V. With the increase of frequency the efficiency increases at first and after a 30MHz switching frequency efficiency starts to drop again. Because, initially conduction loss is high and switching loss is low for lower frequency. When the frequency increases the conduction loss decreases and switching loss increases [45]. And efficiency starts to rise

because overall loss decreases. The efficiency vs. frequency curve is also varies for output voltage level. For higher output voltage level the efficiency is higher. For the output voltage level 3 and 2.5, the converter has more than 90% efficiency for whole frequency range form 10-100MHz. For 0.5V output voltage the efficiency is less than 80% for all frequency. Here all the simulation is done for 3.6V battery voltage.

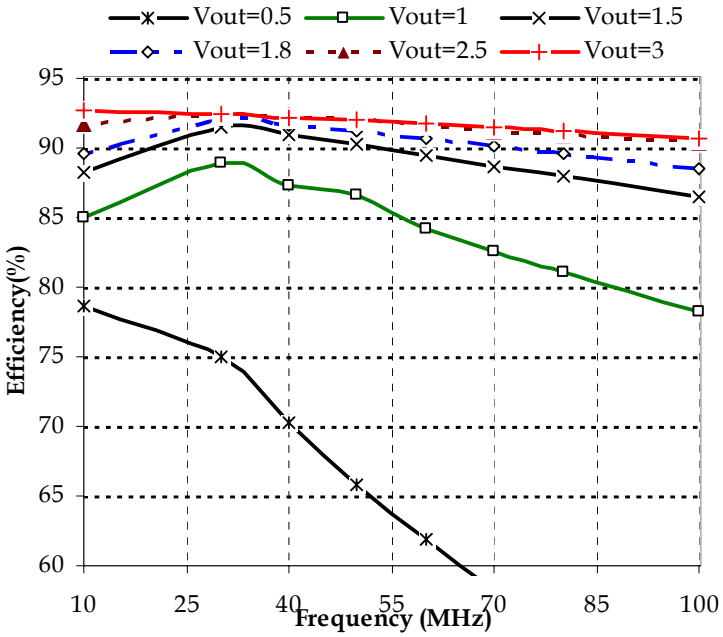


Figure 4-10. Efficiency vs. frequency curves for different output voltage. Maximum efficiency 93% is achieved for 3V output and 30MHz switching frequency.

4.2.2 Efficiency vs. frequency for different battery voltage

The voltage of the Li-Ion batteries used in the mobile phones changes over time due to uses and aging. The efficiency of the converter varies with the change of battery voltage. In the following Figure 4-11 efficiency vs. frequency curves are plot for different battery voltage. The efficiency increases with the decrement of the battery voltage, because the ratio of the input by output decrease. The simulation results shown in the Figure 4-11 are for 1.8V output. For this output voltage options maximum efficiency reached 92.1%. When the battery voltage drops below 3.3V, output voltage 3V is not guaranteed.

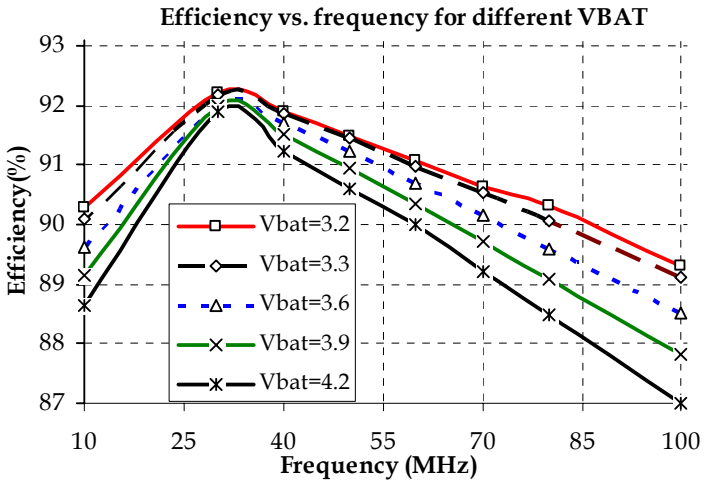


Figure 4-11. Efficiency vs. frequency plots for different battery voltage. Maximum efficiency 92.1% is achieved for battery voltage 3.3. All the simulation is done for output voltage 1.8V and 400mA load current.

4.2.3 Efficiency vs. output power

The efficiency increases as the output power of the converter increases, because the loss of the converter does not increase proportionally with the increment of output power. In the following Figure 4-12 efficiency vs. output power curves are plotted for different switching frequency. For output power less than 400mW, the efficiency decreases rapidly, because the total loss becomes comparable with the output power. For output power more than 750mW the efficiency does not change significantly. The converter gives more than 90% efficiency in all switching frequency for more than 1.25W output power. For this simulation 3.6V battery voltage and a 4.28Ω load resistor are used. The output power is changed by changing both the current and voltage. As a fixed load resistor is used, with the change of output voltage level the output current also changed. The efficiency of the converter drops for light loads, because the pulse width modulation techniques (PWM) used here for varying the duty cycle is not good for light load management. Pulse frequency modulation techniques provide higher efficiency in light load condition [62] .A combination of PFM and PWM techniques will result high efficiency in all loading condition. From the figure it is observed that efficiency also depends on the switching frequency. When the switching frequency of the converter is 30MHz it gives maximum efficiency in all load conditions. At 100MHz switching frequency it gives the worst results because switching loss is high.

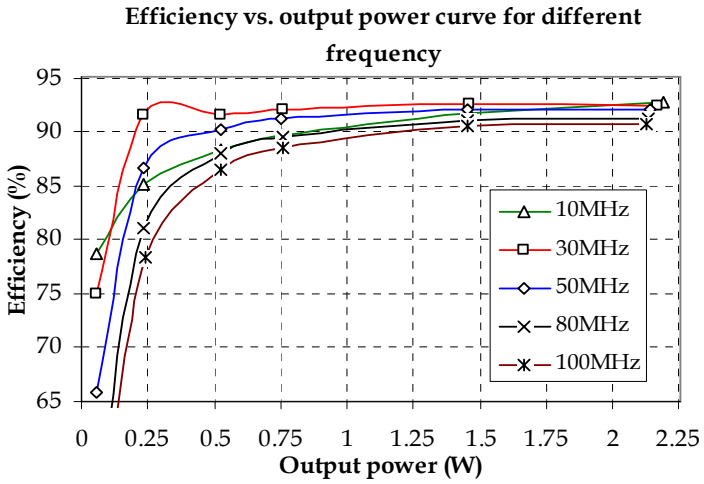


Figure 4-12. Efficiency vs. output power curves for different frequencies. For switching frequency 30MHz the efficiency is maximum for low to high output power. More than 90% efficiency is achieved for all the switching frequency at 2W output power.

4.2.4 Ripple voltage vs. frequency

The ripple voltage is inversely proportional to the frequency. With the increment of switching frequency the ripple voltage decreases. In the following Figure 4-13, output ripple voltage vs. the frequency curves are plotted for different output voltage level. The ripple voltage is related with the duty cycle. For 50% duty cycle the ripple voltage is minimum, theoretically zero. Because at 50% duty cycle the inductor currents cancel each others. With increment or decrement of duty cycle the ripple voltage decreases.

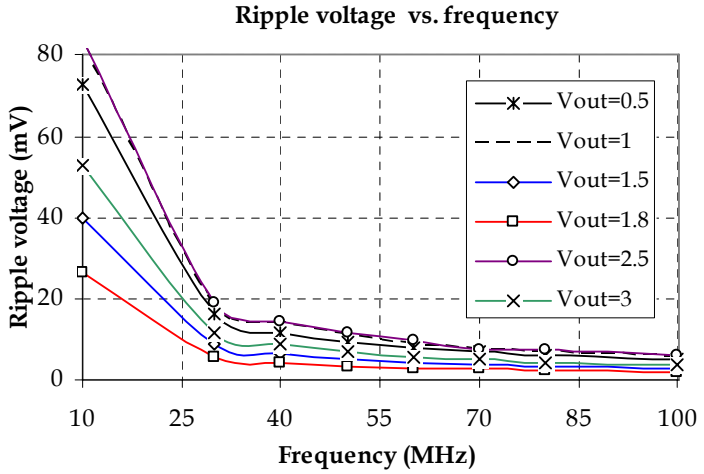


Figure 4-13. Ripple voltage vs. frequency plot for different output voltage.

4.2.5 Efficiency vs. dead time

The efficiency of the converter is increased more than 1% by optimizing the dead time. Dead time restricts the short circuit path from battery voltage to ground. If the dead time is too much, then the body diode of the nmos starts to conduct and the energy stored in the inductors goes to ground. In the Figure 4-14 efficiency vs. dead time curves is plotted. The dead time for rising edge and falling edge is different. Maximum efficiency is achieved for 30pS falling edge delay and 150pS rising edge delay.

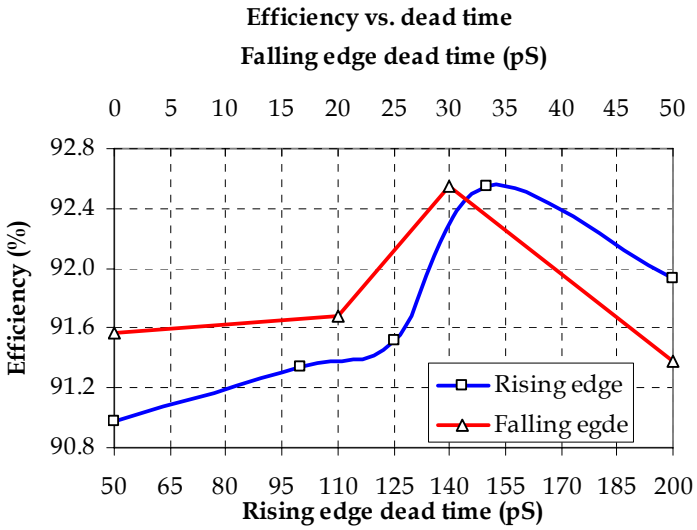


Figure 4-14. Efficiency vs. dead time curves for rising and falling edge of gate drive pulses. All the simulation is done for 3.6V battery voltage, 1.8V output voltage level, 400mA load current and 50MHz switching frequency.

4.2.6 Frequency vs. efficiency when body of nmos of pmos driver is grounded

In this design the bodies of all the nmos, of the pmos driver are considered as higher potential than ground. In the simulation it is considered that both the body and source of the mosfet are in same potential. But usually all the p-substrates are connected to ground. But in some process it is possible to split the substrate. As this process does not allow substrate separation, simulation is done with the body all the nmos, of pmos driver grounded. In this case, the overall efficiency of the converter decreases by 3%.

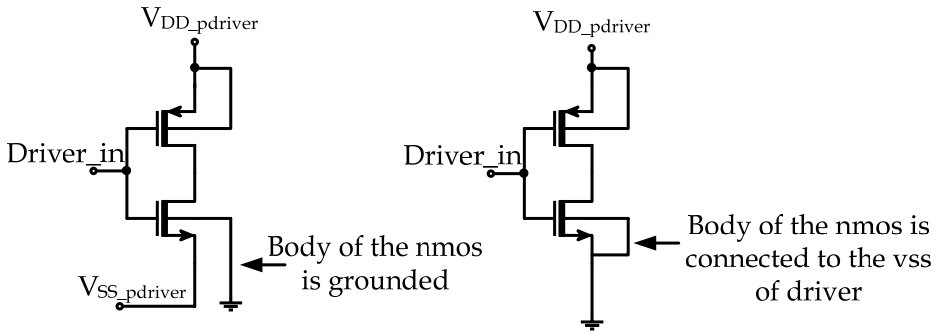


Figure 4-15. Figure showing the body connection of the nmos of the pmos driver. In actual design the body of the nmos is not grounded, rather it is same potential with the source of the nmos.

4.3 Control circuit design

This DC-DC converter does not have any feedback circuit. It takes an input sinusoidal with a dc offset voltage as its control signal. The control circuit consists of a Schmitt trigger, one 180° phase shifter, two level shifters and two dead time controllers. Schmitt trigger generates pulse wave from the sinusoidal signal. The frequency of the pulse wave and the sinusoidal signal are same. The duty cycle of the pulse wave is determined by the offset voltage of the sinusoidal signal. The pulse wave then passes through the 180° phase shifter circuit, which produces two identical pulse waves having 180° phase shift. But the switching frequency of these two signals is half of the input pulse wave. These two signals then pass through the dead time controller circuits, level shifters and driver circuits before driving the power mosfets.

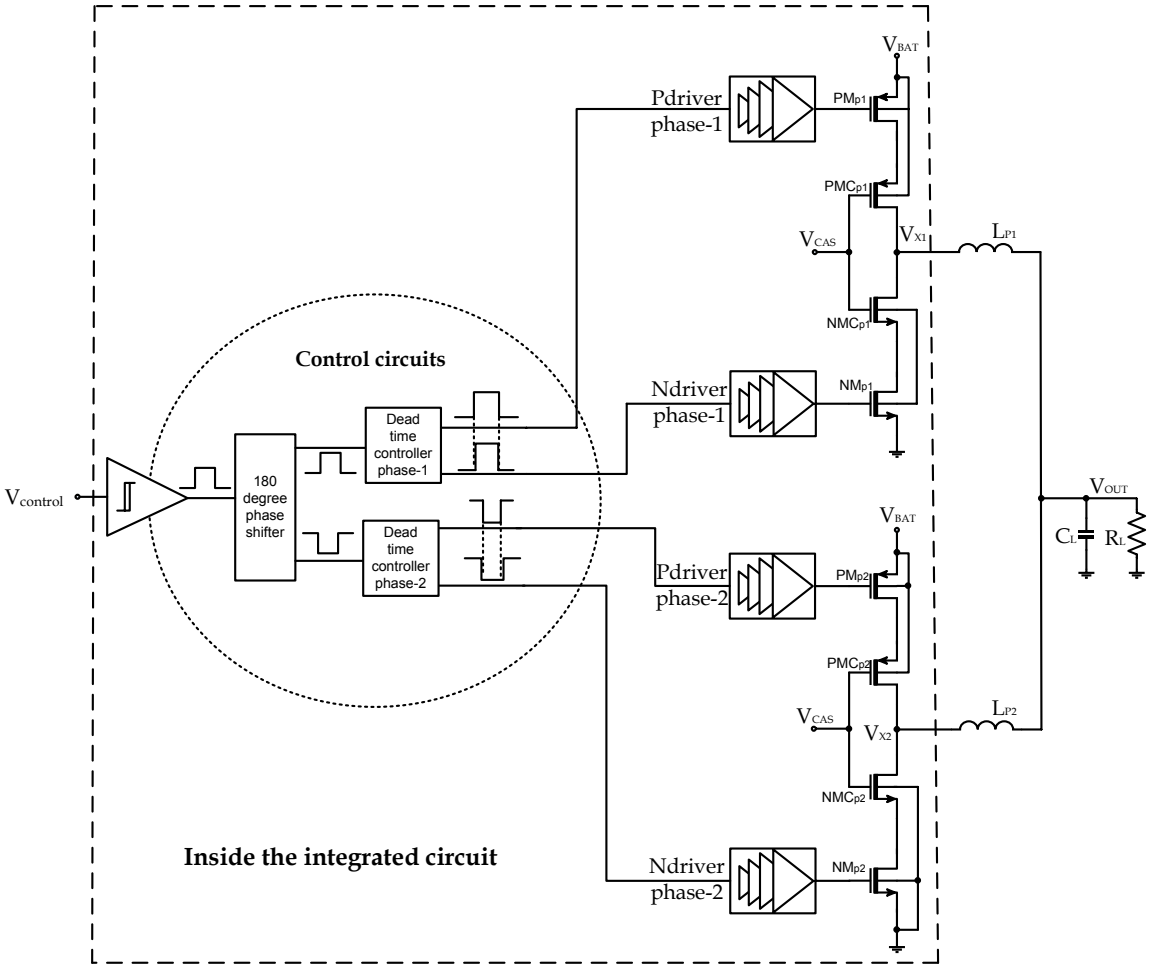


Figure 4-16. Signal flow graph of the DC-DC converter with the control circuits.

4.3.1 Schmitt trigger

Schmitt trigger detects the level of an input signal and gives a pulse wave as output. In the paper [47]-[50] different Schmitt trigger are described. A simple Schmitt trigger without hysteresis is chosen for this design. In this work, the Schmitt trigger is used to convert input sinusoidal into pulse wave. Depending on the amplitude and offset voltage of the sinusoidal signal the duty cycle is determined. In the Figure 4-17 the schematic diagram of the Schmitt trigger is shown. Maxim 1V offset voltage with 400mV V_{PP} sine wave can be used as V_{IN}. The input output curves of the Schmitt trigger is shown in Figure 4-23. Three different scenarios are shown in the picture for different duty cycle. The duty cycle of the V_{OUT} pulse increases with the increase of V_{offset}. Simulation results of the Schmitt trigger is shown by the Figure 4-19.

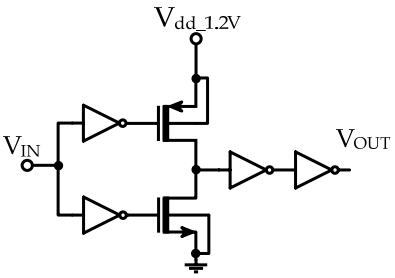


Figure 4-17. Schematic diagram of Schmitt trigger.

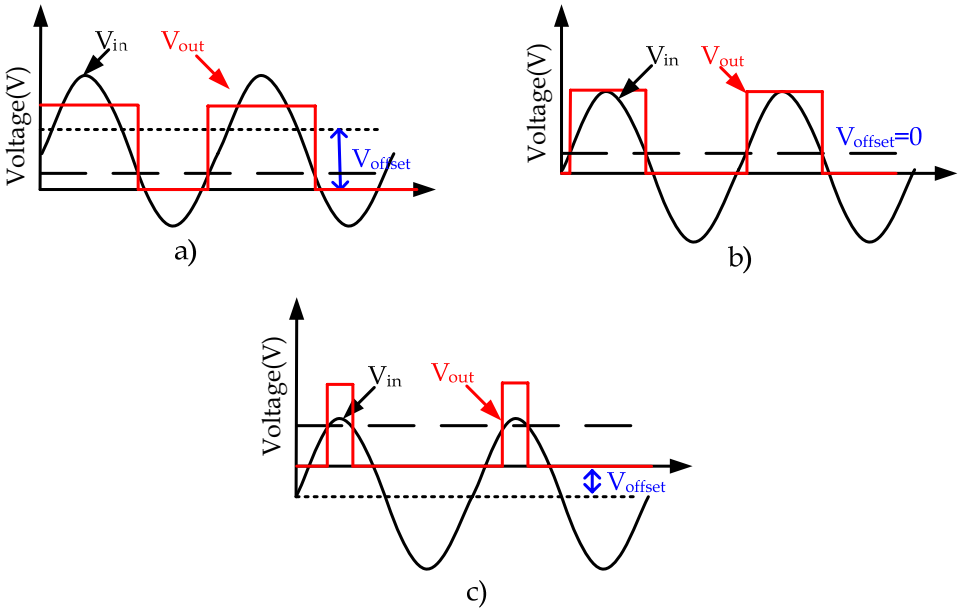


Figure 4-18. Input and output curve of the Schmitt trigger. a) V_{offset} >0, b) V_{offset} =0 and c) V_{offset} <0

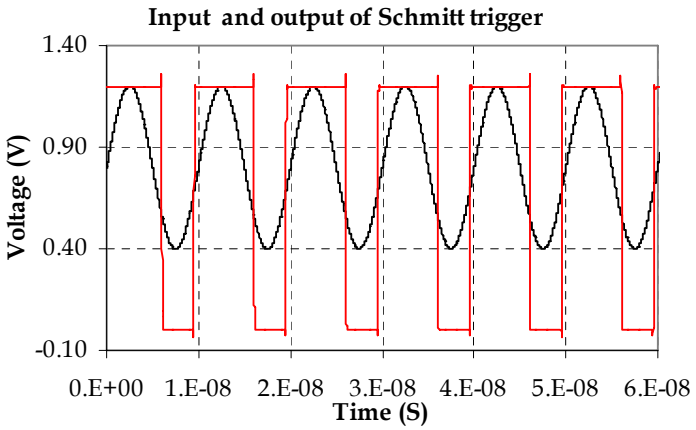


Figure 4-19. Simulation results of the Schmitt trigger. The Schmitt trigger is producing more than 50% duty cycle.

4.3.2 180° phase shifter

Two pulse signals separated by 180° degree are needed for driving two interleaved stages of the DC-DC converter. In the paper [51] and [52] two different techniques are explained for generating two phase signal form one phase signal. In the reference [51] a D flip–flop and two NAND gates are used for generating the signals. In the reference [52] a J-K flip-flop along with other circuitry are used for generating two phase signal. For this implementation the circuits of reference [51] is chosen for generating two phases signal. In the following Figure 4-20 a) the diagram of the circuit is given. In the Figure 4-20 b) the input output curve of the phase shifter is shown. In the Figure 4-20 PWM is the input signal; PWM1 and PWM_2 are the output signals. There are two drawbacks of this circuit. First the switching frequency of the new signal is half of the original signal. And secondly this circuit can not produce more than 50% duty cycle theoretically. First problem is solved by increasing the frequency of PWM signal by a factor of two. And for solving the second problem a controlled transmission gate is used. When the controlled voltage is zero it directly passes the pulses and when the controlled voltage is one it passes the inverter pulses. In this way the whole range of the duty cycle is covered. A typical simulation result of the phase shifter is shown in the Figure 4-21. The simulation results matches with the Figure 4-22. (b. In the Figure 4-22 the schematic diagram of the transmission gate is given. If the V_{CNT} is low then PWM_1 passes through the transmission gate but if V_{CNT} is low then $PWMB_1$ appears at the output.

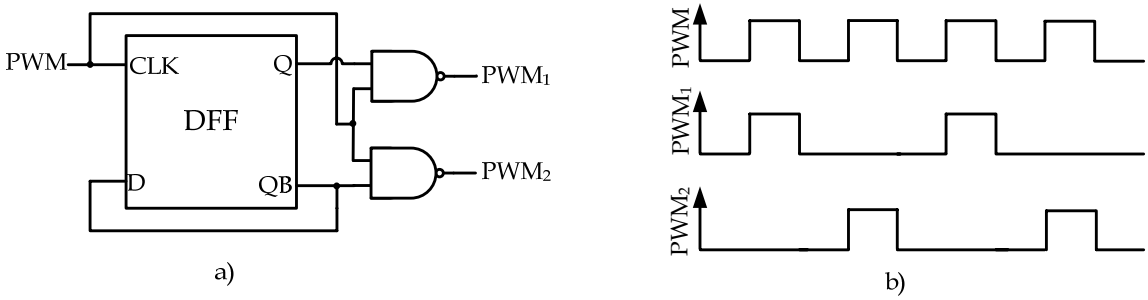
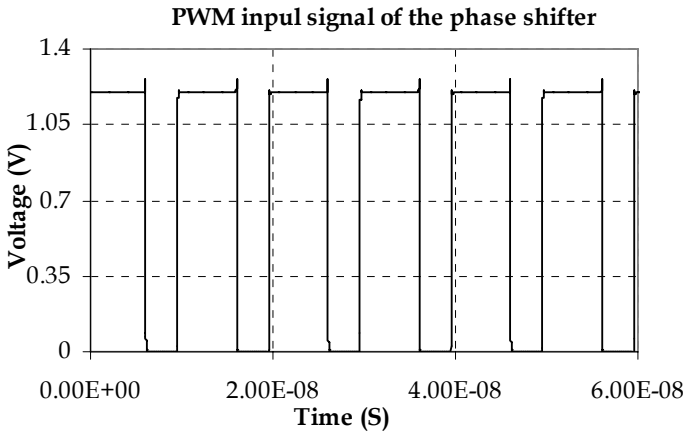
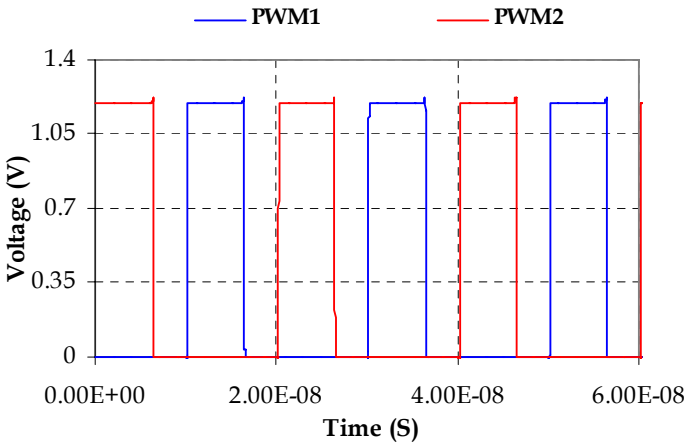


Figure 4-20. a) Schematic diagram of two phase generator and b) input output signal of two phase generator



a)



b)

Figure 4-21. Simulation results of the 180° phase shifter. a) Input signal b) output signals of the phase shifter.

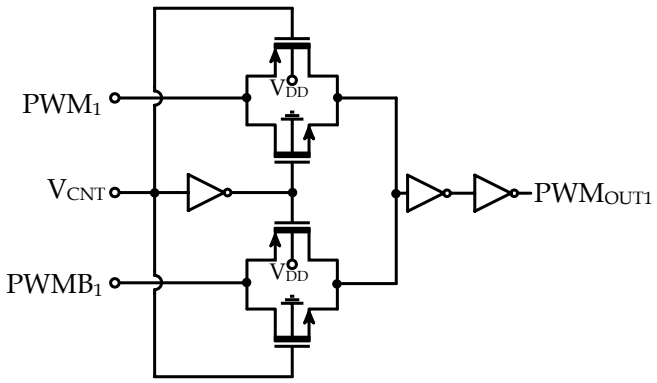


Figure 4-22. Schematic diagram of transmission gate for controlling the two phase signal.

4.3.3 Dead time controller

Dead time is used for zero voltage switching to stop the short circuit current from battery to ground. In the paper [51] dead time controller circuit is described. In the Figure 4-23 the dead time controller circuit is shown. The dead time for both the rising and falling edge can be controlled externally for maximum efficiency. The supply voltage of the feed back inverter chain controls the delay. When the supply voltage is higher then the inverter works very fast and the delay is minimum. When the supply voltage is low then the delay is higher, because for lower supply voltage the inverter chains produce maximum delay. In the Figure 4-24 control voltage vs. delay curve is shown both for the rising and falling edge delay. Falling edge delay is changed form 20pS to 600pS for the control voltage 1V to 0.5V and rising edge delay is changed from 40pS to 640pS for the same voltage range. In the figure $V_{control}$ voltage refers to the rising and falling edge control voltage. When the V_{C_RISING} is varied $V_{C\_FALLING}$ is fixed to 1V, when $V_{C\_FALLING}$ is varied V_{C_RISING} is fixed to 1V. The maximum efficiency of the converter is achieved for 150pS rising edge delay and 30pS of falling edge delay. The default supply voltages of the inverters and NAND gates are 1V DC and all the inverters and NAND have common ground.

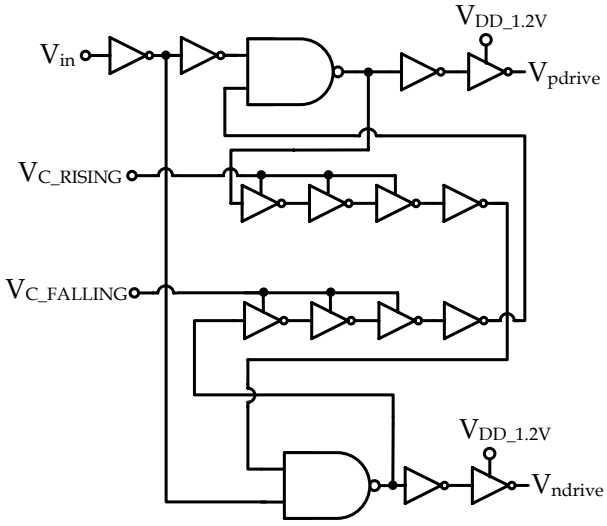


Figure 4-23. Schematic diagram of dead time controller

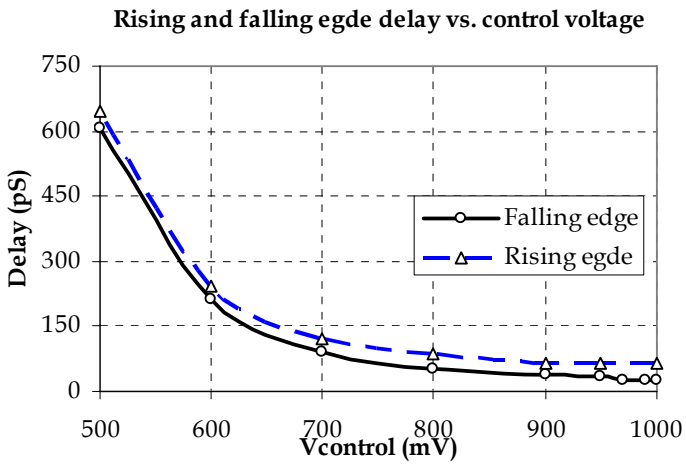


Figure 4-24. Rising and falling edge delay of the dead time control circuits for different control voltage.

4.3.4 Level shifter

Level shifter is needed to convert the low voltage PWM signal to high voltage PWM signal for driving the gate of pmos switch. Lowering the swing of the gate drive voltage increases the efficiency of the converter [20]. In the paper [54]-[58] different types of level shifter are presented for different applications. For this DC-DC converter, a level shifter is needed with very low rise time and fall time. And the low level switching pulses generated by 180° phase shifter need to convert high switching pulses with out duty ratio compression. The dead time of the circuit will be affected by the compression of the duty cycle, which will decrease the efficiency of the converter.

A folded cascode based level shifter is designed to solve this problem. Folded cascode amplifiers have higher gain compare to other amplifiers, which will help to reduce the rise and fall time of output pulses of the level shifter. This type of amplifier need higher power supply compare to other amplifier, which is an advantage of this application. As this is a direct battery powered circuit and cascode devices are used to protect the mosfets form breakdown.

Figure 4-25 the schematic diagram of the level shifter is shown. 0-1.2V pulses coming in the input, V_{IN} of the level shifter are converting into 2.4-3.6V output signal V_{OUT}. R_{bias} select the biasing current and controls the rising and falling time of the level shifter. V_{BAT} sets the high level of the switching pulse and V_{SS_PDRV} sets the low level of the level shifter. It has rise and fall time of 25pS when an inverter is used as a load. The level shifter is simulated for

10MHz-100MHz switching pulses for all corner variation with temperature variations. This level shifter can convert any low switching pulse of 5-95% duty cycle into high switching pulses. In the Figure 4-26 the input and output curve of the level shifter is shown. The simulation is done for 50MHz switching frequency and 50% duty cycle.

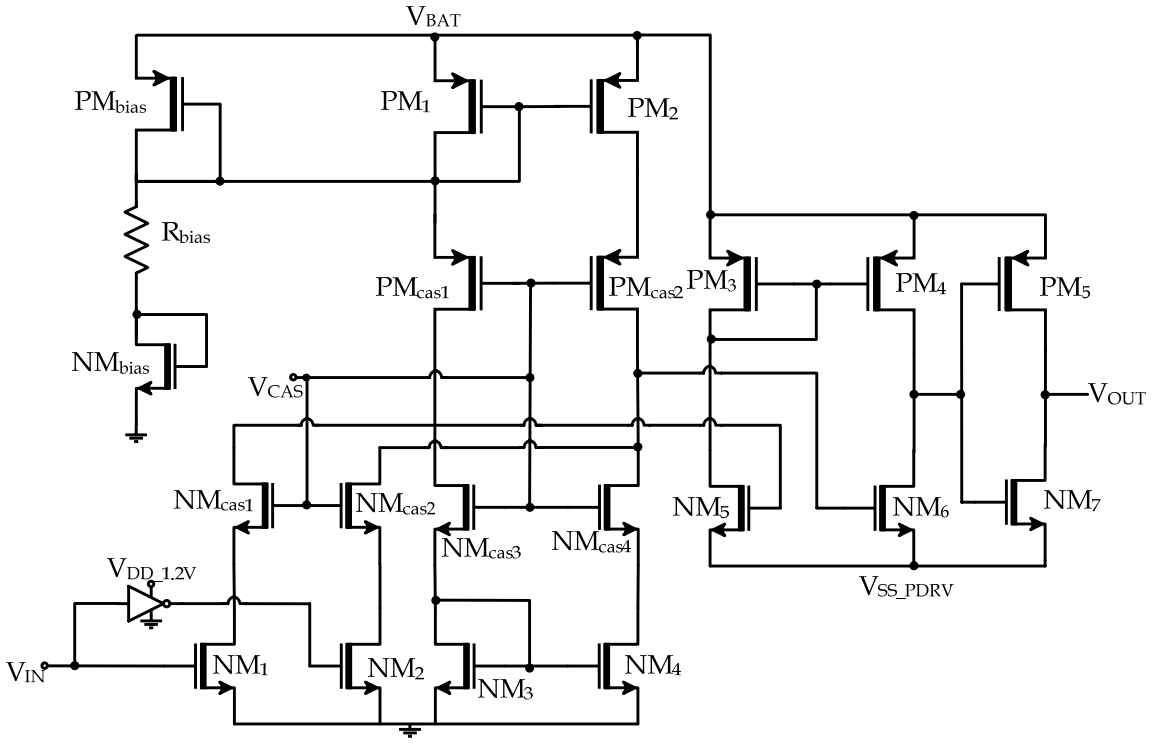


Figure 4-25. Schematic diagram of level shifter

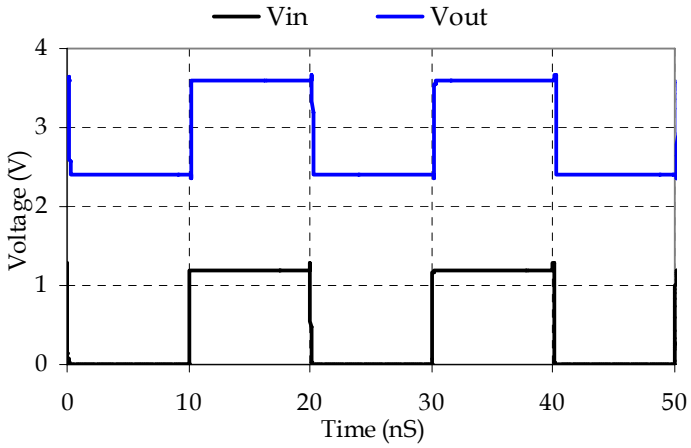


Figure 4-26. Input output curve of the level shifter.

4.4 Simulation results with control circuits

In the following sections simulation results of the DC-DC converter is shown with the control circuits. These results are similar like the results are presented in the previous section of this chapter. The losses in the control circuits are added with the other losses of the converter and decrease the efficiency. When the output power is high these losses are insignificance compare to the output power. Thus the maximum efficiency of the converter does not change. When the output power is low then the efficiency drops by more than 0.5% due to the losses in the control circuits.

4.4.1 Efficiency vs. load current

In the Figure 4-27 efficiency vs. load current curves are plotted for different output voltage. Maximum efficiency 93% is achieved for 3V output for 450mA load current. The efficiency is less than 60% for load current less than 150mA and the output voltage is 0.5V. Efficiency decreases further for lower load currents.

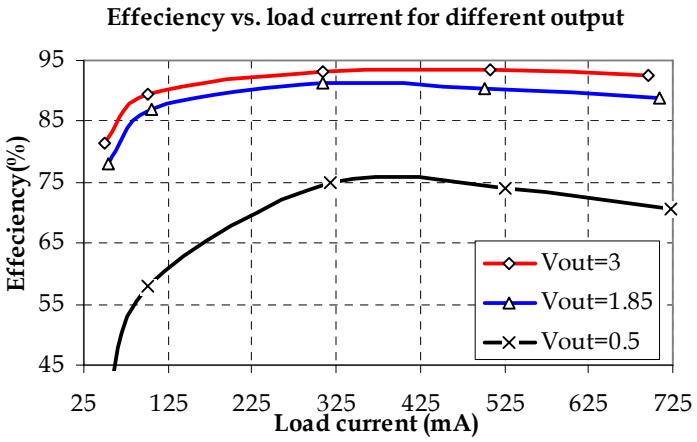


Figure 4-27. Efficiency vs. load current curve for different output voltage. Al the simulation is done for 50MHz switching frequency 3.6V battery voltage.

4.4.2 Efficiency vs. frequency for different output voltage

Efficiency vs. frequency curve for different output voltage option is shown by the Figure 4-28. For higher output voltage options the efficiency is almost constant in all the frequency, but at lower output voltage option the efficiency drops rapidly at high frequency. At high frequency the switching losses increase significantly and the efficiency drops.

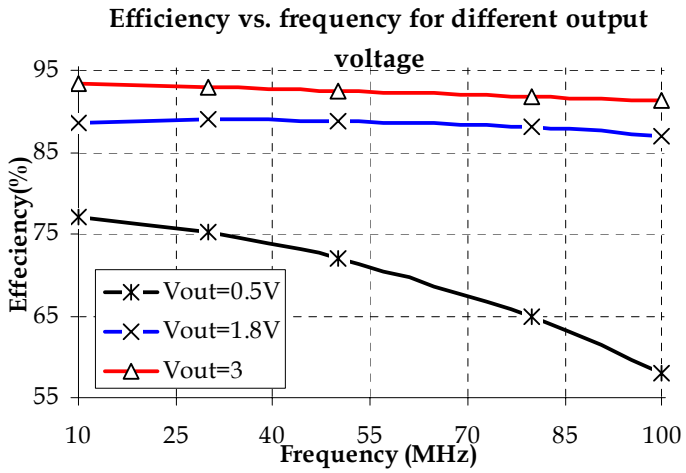


Figure 4-28. Efficiency vs. frequency curve for different output voltage. Here the input voltage is 3.6V and the load current is 700mA

4.4.3 Efficiency vs. frequency for different battery voltage

In the following Figure 4-29 efficiency vs. frequency curve is shown for different battery voltage. The efficiency increases when the difference between the battery voltage and the output voltage decreases. Maximum efficiency is achieved for maximum output voltage option when the battery voltage is 3.3V.

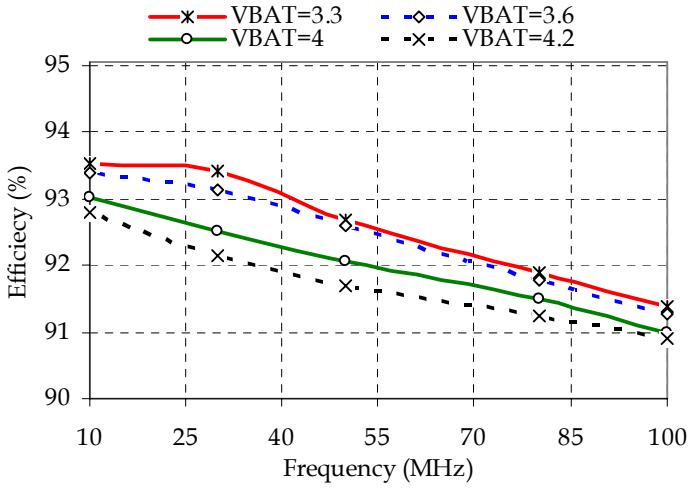


Figure 4-29. Efficiency vs. frequency curve for different battery voltage. Here the output voltage is 3V and the load current is 700mA.

4.4.4 Efficiency vs. output power for different frequency

Efficiency vs. output power curve is shown by the Figure 4-30. Efficiency is increased with the increment of output power. At light load condition total loss becomes comparable with the output power, so the efficiency drops rapidly at low load condition. Efficiency also varies with frequency. Switching loss increases with the increment of switching frequency which results in the reduction of efficiency at high frequency. At 100MHz switching frequency the efficiency decreases by 1.5% at maximum load condition shown by the green curve in the figure.

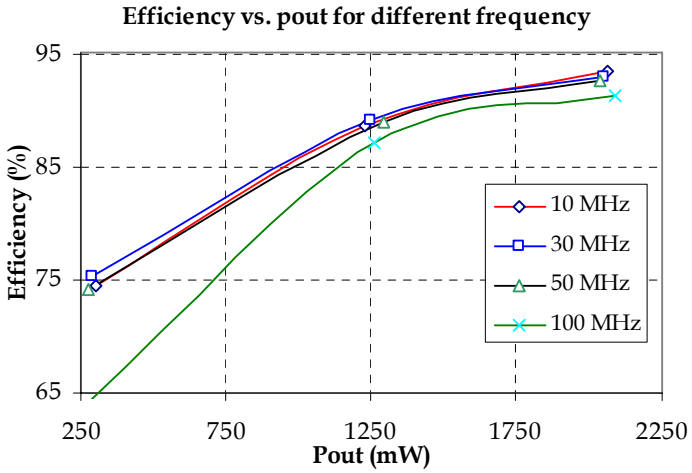


Figure 4-30. Efficiency vs. output power curve for different frequency. Here the battery voltage is 3.6V.

4.4.5 Efficiency vs. dead time

Efficiency vs. dead time curve is shown by the Figure 4-31, which is similar like the Figure 4-14. But here the dead time is generated by the control circuit. Maximum efficiency is achieved for 30pS falling edge delay and 150pS rising edge delay.

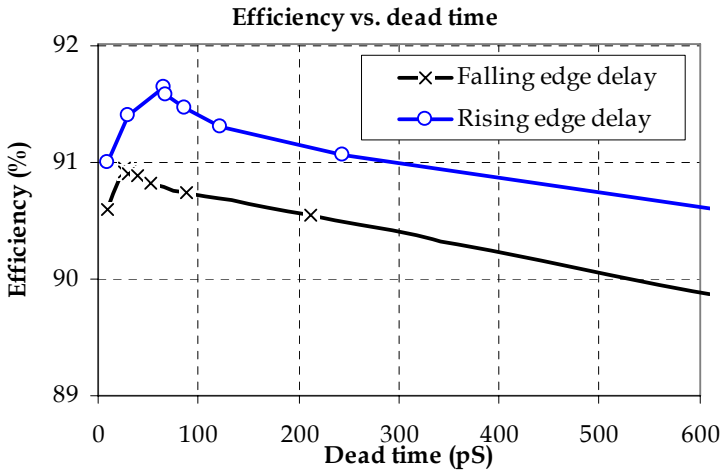


Figure 4-31. Efficiency vs. dead time curve.

4.4.6 Summary of efficiency

In the following Table 4-2 the efficiency of the converter is shown for different corner conditions. Maximum efficiency is found for 3V output when the load current is 400mA. For 100mA load current the efficiency is less than 60%, when the output voltage level is 0.5V. The efficiency is higher than 75% for more than 300mA load current for the output voltage 0.5-3V.

Table 4-2: Efficiency of the converter for different conditions

F_{Switch}	V_{BAT}	V_{OUT}	I_{Load}	Efficiency
[MHz]	[V]	[V]	[mA]	[%]
10	3.3	3	400	93.5
10	4.2	0.5	100	58
50	3.3	1.8	700	92.5
100	3.3	3	700	91
100	4.2	0.5	100	56

4.5 Conclusion

Design procedure and simulation results of the DC-DC converter are explained in this chapter. The design starts with optimizing the pmos and nmos switch for single phase DC-DC converter and ends with two phase converter with complex control circuit. First the converter is optimized without the control circuit. Two phase interleaving is done for reducing the output ripple voltage, but it needs two external inductors. Digital control is used for generating two phases control signal form a single phase signal. Dead times are introduced to stop the short circuit current, when the gate drive vlotage of the pmos and nmos are changing their states. The dead time can be controlled externally for maximum efficiency. Level shifter is used for pmos drive to decrease the gate drive loss. In the end the converter ends up with maximum efficiency of 93.5% for 3V output options at 30MHz switching frequency when the supply voltage is 3.3V.

5 DC-DC Converter Layout

This chapter includes the layout procedure of the DC-DC converter. The layout is done using Cadence Virtuoso tools. DRC and LVS checks and parasitic extraction are performed with Cadence Assura RCX. The first part of the chapter includes the layout considerations and the second part describes the layout design of the converter.

5.1 Layout consideration

The converter has 2W output power at 3V output, which represents 700mA current flows from battery to load at maximum condition. So the routing of the current paths is considered carefully. The signal path having switching frequency of 10-100MHz needs also special considerations for routing, because the signal can be easily distorted by the high current and noisy path. When the layout is done the following things are taken into consideration [59],

1. Wiring for the high current path is made short and wide, so that the series resistance of the current path is as small as possible.
2. Multiple metal layers are used in V_{BAT} and V_{SS} paths to decrease the series.
3. For interconnecting the metal layers maximum number of via's are used.
4. The control signal path is made also wide a small to minimize the parasitic resistance.
5. This is a two phase DC-DC converter. First the layout for one phase is done. Then by copying this layout the second phase is made. As a result an axis of symmetry is present in the layout.

6. Place big bypass capacitor near to DC power supply pads.
7. Place ESD protection circuits.

5.2 Floor plan

Floor plan is the preliminary sketching of the layout of the circuit, which is done prior to the layout. Floor plan actually shows the placing of different blocks of the circuit and interconnections among them. When the floor plan of the DC-DC converter is done, all the points of previous section are considered very carefully. In the Figure 5-1 the floor plan of the DC-DC converter is shown. V_{BAT} and V_{SS} bus line is placed in the middle and two outputs are taken from two sides of the IC. V_{BAT} and V_{SS} bus creates the symmetric line of the IC. Each phase is placed vertically in two sides of the V_{BAT} and V_{SS} bus lines. The control units are placed in the bottom of each phase. All the pins are placed for minimum distance form the block to the pin.

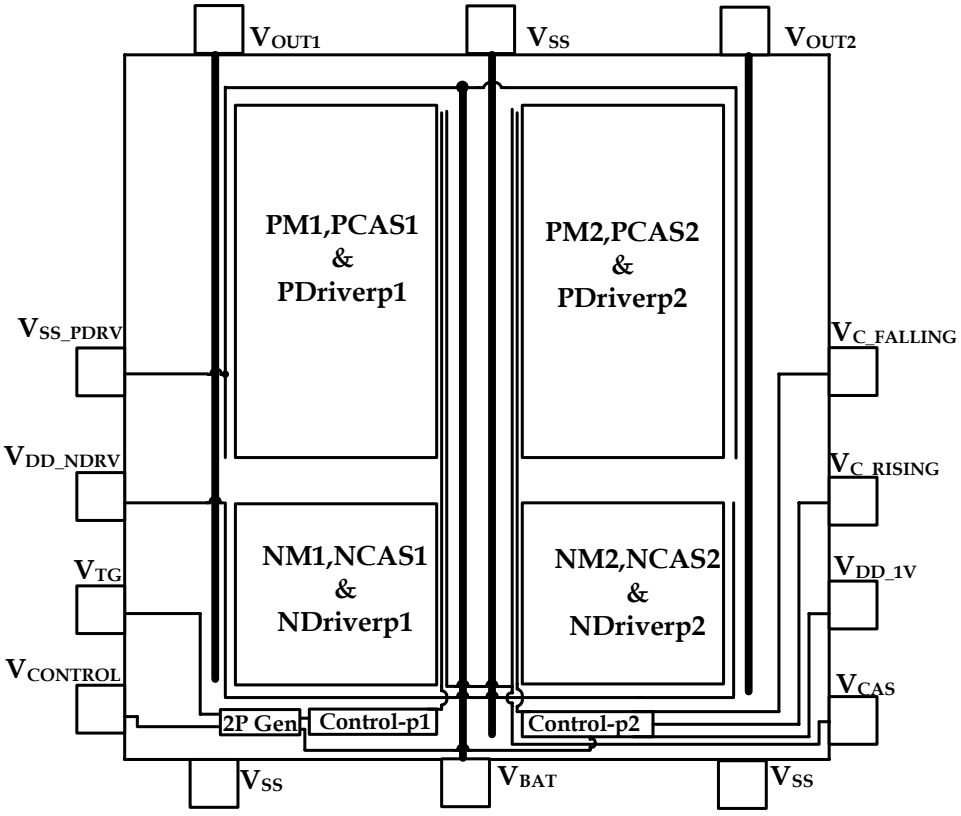


Figure 5-1. Floor plan of the converter.

5.3 Layout design

The power mosfets and cascodes take most of the places of the IC. They are divided into small segments for the easiness of the layout. Small segment of the switch and cascode device are placed together. The drivers are also divided into small segments. Thirty small segments of the switches, cascodes and a driver segment make a unit cell for both nmos and pmos. Forty unit pmos and twenty unit nmos cell creates one phase of the converter.

Choosing the shape of cells are very important. Because depending in the size of them the size and shape of the converter will be determined. Different sized cells with different finger width are tried to make the whole converter square shaped. In the end MOS having total width of 10u and 10 fingers are chosen for small cells for switches and cascodes.

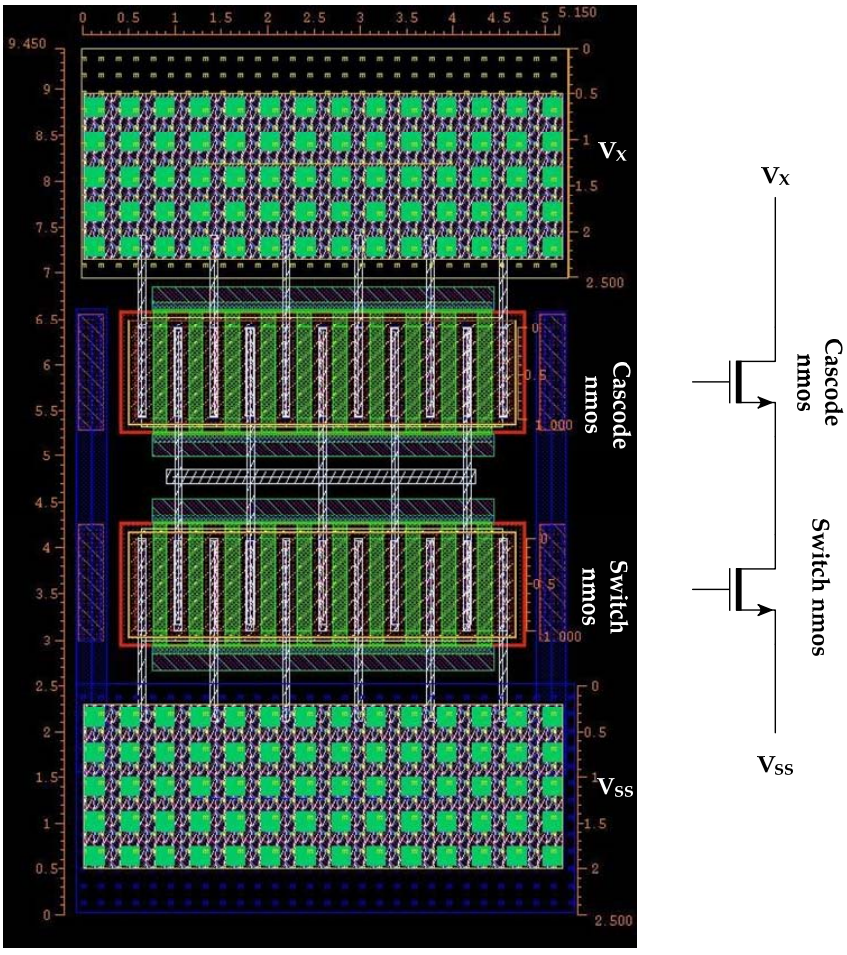


Figure 5-2. Small segment of switch nmos and cascode nmos.

In the Figure 5-2 picture of a small segment of power nmos and cascode are shown. The drain (V_X) and source (V_{SS}) connecting wires are made wide to reduce parasitic resistance. Multiple metal layers are also used for decreasing the parasitic resistance. The gates are connected in the both sides of the mosfet. Same configuration is followed for the pmos.

In the Figure 5-3 the layout diagram of the nmos unit cell is shown. Six small cells of nmos cascode and nmos switch are placed in a row and five of them are placed in a column. The driver for the unit cell is placed in the bottom of the unit. In one side of the unit cell the gate connections are given and in the other side of the unit cell the gate connections of the cascade devices are given.

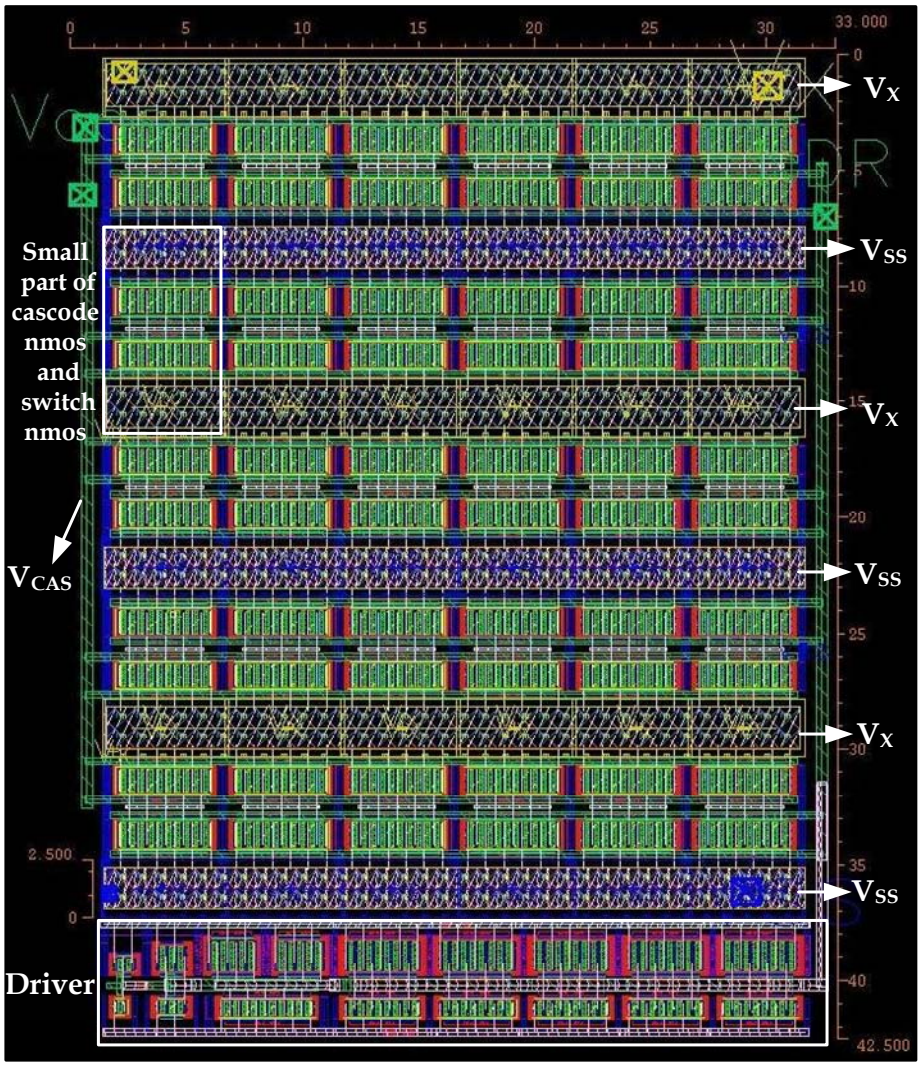


Figure 5-3. Figure showing a unit cell of nmos.

Each phase is consisting of forty pmos unit cells and twenty nmos unit cells. V_{BAT} and V_{SS} bus lines are placed in between two phases. Two phase generator and the dead time control circuit are placed in the bottom of the layout. The control signal generator circuits for phase-1 and phase-2 are placed in the bottom of each phase. The detailed layout of the converter with all blocks is shown in the Figure 5-4 and the top level layout is shown in Figure 5-5. Metal layers 11 and 10 are used for V_{BAT} connection and metal layers 9, 8, 7 and 6 are use for V_{SS} connection. Metal layers 11, 10 and 11 are used for connecting the outputs. Total current capability of the bus lines,

$$V_{BAT}=\frac{8mA}{\mu m}\times 6\mu m\times 16\times 2=1536mA \text{ and } V_{SS}=\frac{2mA}{\mu m}\times 6\mu m\times 16\times 4=768mA$$

Where, 8mA/µm is the current density of metal 10 and M1, 6µm is the metal width of each line, 16 is the total number of metal lines, 2m/µm is the current density of metal 6 to 9 [60].

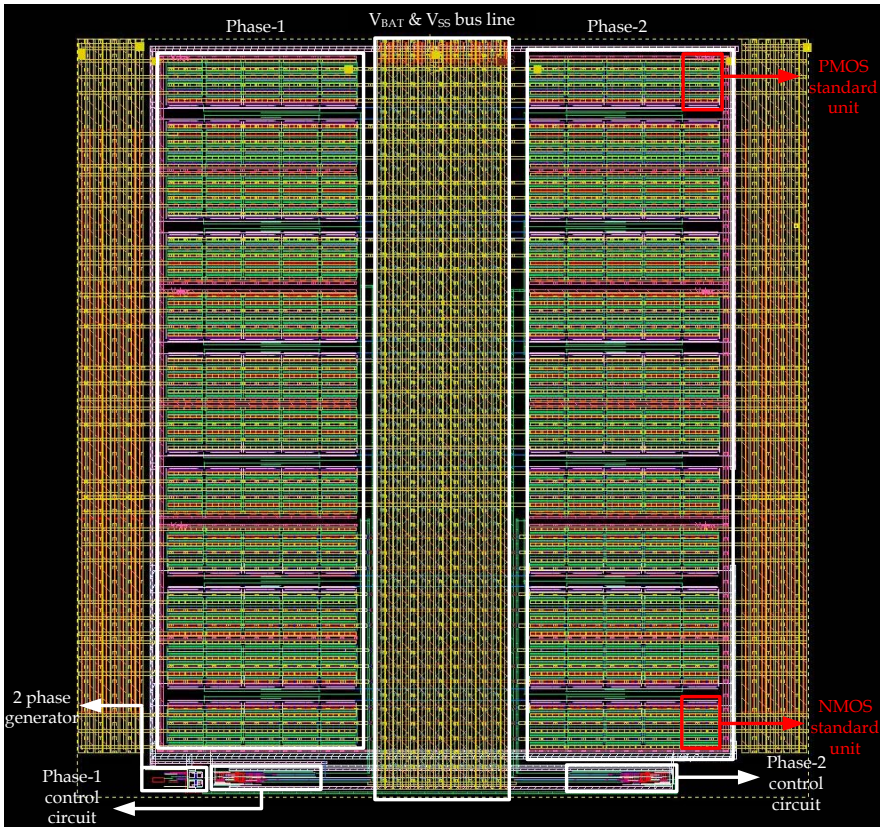


Figure 5-4. Layout of different blocks of the DC-DC converter.

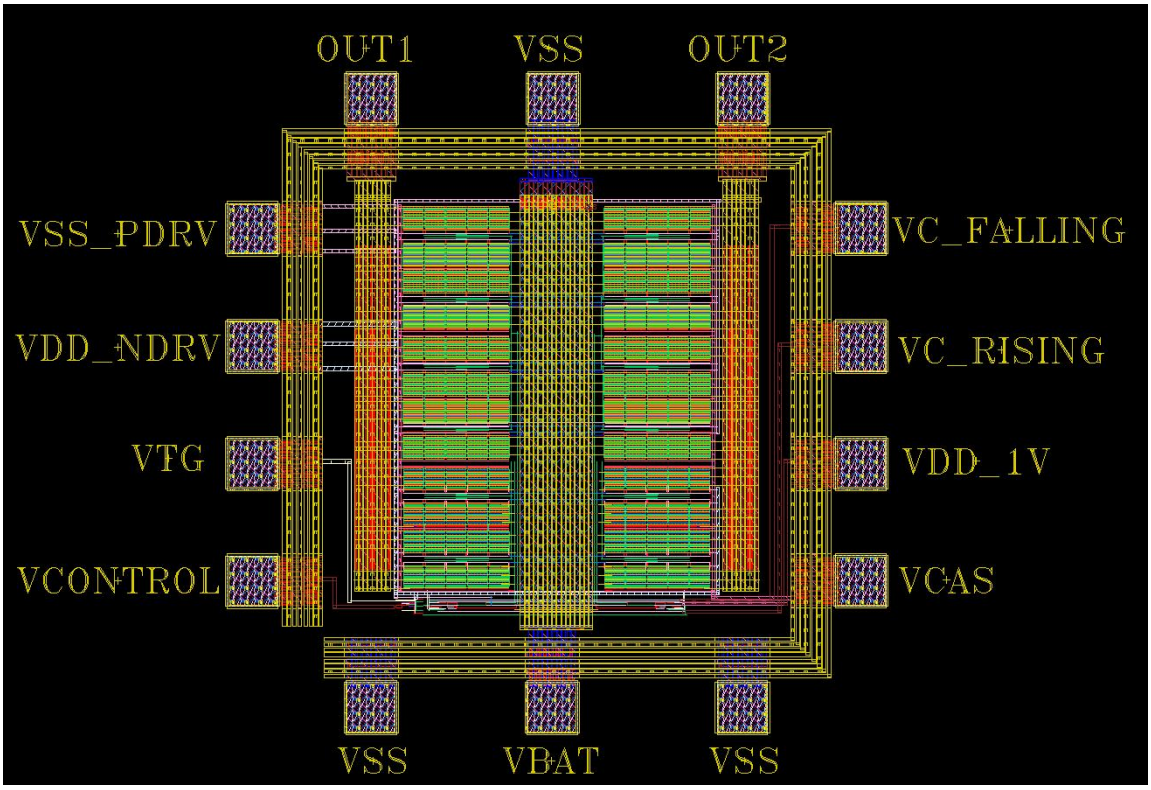


Figure 5-5. Top level of the DC-DC converter.

5.4 Conclusion

In this chapter the layout of the converter is explained. At first basic rules of layout and the floor plan is described. The layout is done maintaining the rules. The width of the high current lines is chosen for minimum 700mA current and staked metal layer is used for reducing parasitic resistance.

6 Proposed Measurement Set up

In the first part of this chapter the calculations of load and other resistances are shown. Then a typical set up for efficiency and ripple measurement are described in the later part of the chapter. With this set up efficiency for different load current and battery voltage can be found. In the later part of this chapter expected practical results are given. The simulation is done by introducing main parasitic components of the converter and PCB.

6.1 Load resistor calculations

Six load resistors are placed in parallel in the output to change the load currents of the converter. The value of the load resistors are 24.9 and 30.1. In the Figure 6-1 combination of load resistors are shown and in the Table 6-1 load currents for different combinations of load resistors are shown.

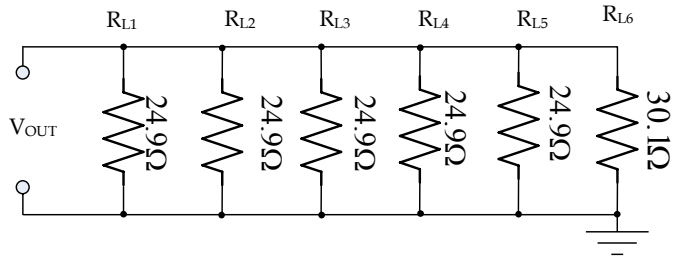


Figure 6-1. Load resistor combination for varying the load current from 100mA to 700mA.

Table 6-1: Load resistor and load current combinations

Resistor	Overall Resistance(Ω)	Load Current (mA) for 3.0V output
30.1	30.1	100
24.9	24.9	120.5
24.9‖24.9	12.45	240
24.9‖24.9‖24.9	8.3	360
24.9‖24.9‖24.9‖24.9	6.2	480
24.9‖24.9‖24.9‖24.9‖24.9	4.98	602
24.9‖24.9‖24.9‖24.9‖24.9‖30.1	4.27	702

6.2 LM38511 voltage regulator: bias voltage calculations

In this DC-DC converter there are four different bias voltages and three variable voltages are needed. For generating these voltages seven different LM38511 voltage regulators are used. In case of fully functional DC-DC converter this regulator is not needed. These bias voltages will be generated internally. As it is not a complete DC-DC converter theses constant bias voltages are generated externally for test purpose. The bias voltages are 2.4V, 1.8V, 1.2V, 1V and the variable voltages are 1.8/0 V, 550-1000mV, 550-1000mV. For calculating the bias voltages Figure 6-2 used as a reference picture and the formulas are taken from the datasheet of the regulator.

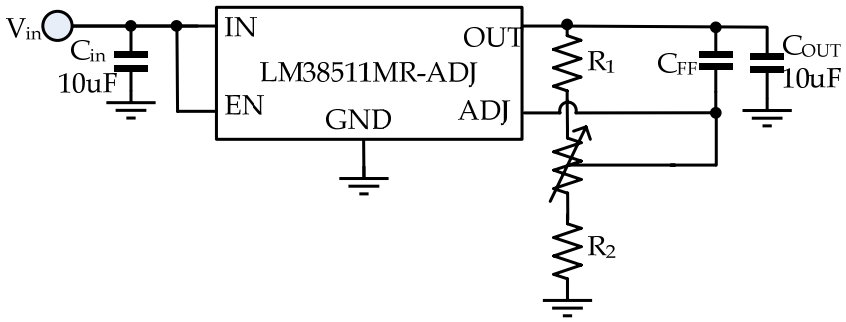


Figure 6-2. Bias voltage calculation for using LM38511MR-ADJ [61]

$$V_{OUT}=V_{ADJ}\times(1+\frac{R_1}{R_2}),\ \text{where}\ V_{ADJ}=0.5V$$

$$C_{FF}=\frac{1}{2\pi R_1 F_Z},\ \text{where}\ F_Z=20\text{-}40\ \text{kHz}$$

Based on these equations the values of the resistor and capacitor are calculated. A variable resistor is used to tune the output voltage of the regulator. In the Table 6-2 the calculated values are shown.

Table 6-2: Bias voltage calculations

V_{OUT}(V) of regulator	R_1(Ω)	R_2(Ω)	R_{TRIM}(Ω)	Voltage Range (V)	C_{FF}(pF)
2.4	2K	499	0-100	2.17-2.6	2700
1.8	1.24K	453	0-100	1.62-1.98	3300
1.2	1.21K	845	0-100	1.14-1.28	3300
1	1K	1K	0-100	0.95-1.05	4700
1.8(0)	3.01k	1.31K	0-100	1.72-1.88	2400
0.55-1	100	1K	0-1K	0.525-1.05	47000
0.55-1	100	1K	0-1K	0.525-1.05	47000

6.3 Pin description

The converter has twelve pins, six of them are input DC voltage, four control signal and two output voltages. In the following table the descriptions of the pins are given.

Table 6-3: Description of the pins of the converter

Pin name	Pin description
V_{BAT}	Input voltage of the converter
V_{CAS}	Cascode bias voltage for the cascode devices
V_{SS_PDRV}	Ground voltage for pmos driver and level shifter
V_{DD_NDRV}	Supply voltage for the nmos driver
V_{DD_1V}	Supply voltage of the dead time generator circuit
V_{OUT1}	Output voltage of phase one
V_{OUT2}	Output voltage of phase two
$V_{CONTROL}$	Input sine wave for controlling the output voltage
V_{C_RISING}	Control voltage for controlling rising edge relay
$V_{C\_FALLING}$	Control voltage for controlling falling edge relay
V_{TG}	Control voltage of the transmission gate for duty cycle control
V_{SS}	Ground pin

In the following Figure 6-3 the pin configuring of the converter is shown. The blue lines in the diagram represent the high current path and the green line represents the control signal path of the converter.

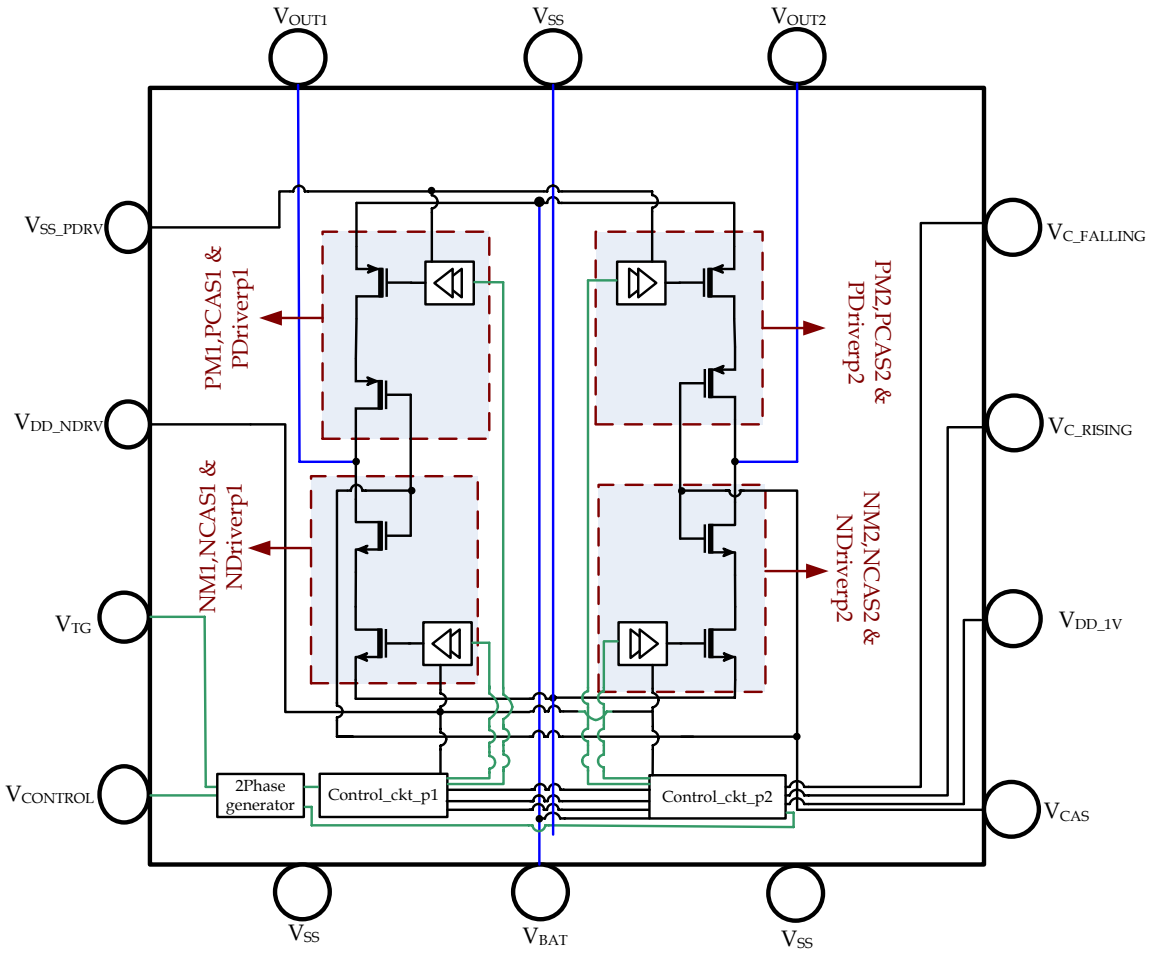


Figure 6-3. Pin configuration of the DC-DC converter.

6.4 Electrical characteristics and proposed measurement set up

A typical measurement set up for efficiency and output ripple measurement of the DC-DC converter is shown on the following figure Figure 6-4. The input signals of the set up are V_{BAT}, V_{SS_PDRV}, V_{CAS}, V_{DD_NDRV}, V_{DD_1V} and V_{SS}. The control signals are $V_{CONTROL}$, V_{TG}, V_{C_RISING} and $V_{C\_FALLING}$. The output signals are V_{OUT1} and V_{OUT2}. The load current is control by six resistors R_{L1} to R_{L6}. The efficiency for different load current can be measured by changing these load resistances. As for example for 3V output options the load can be varied from 100mA to 700mA. By changing the frequency of $V_{CONTROL}$ the switching frequency can be

changed. The switching frequency of the synchronous switches is half of the $V_{CONTROL}$ signals frequency. The dead time can be changed by changing the voltage levels V_{C_RISING} and $V_{C\_FALLING}$. With this set up the efficiency for different battery voltage can also be measured by changing V_{BAT}.

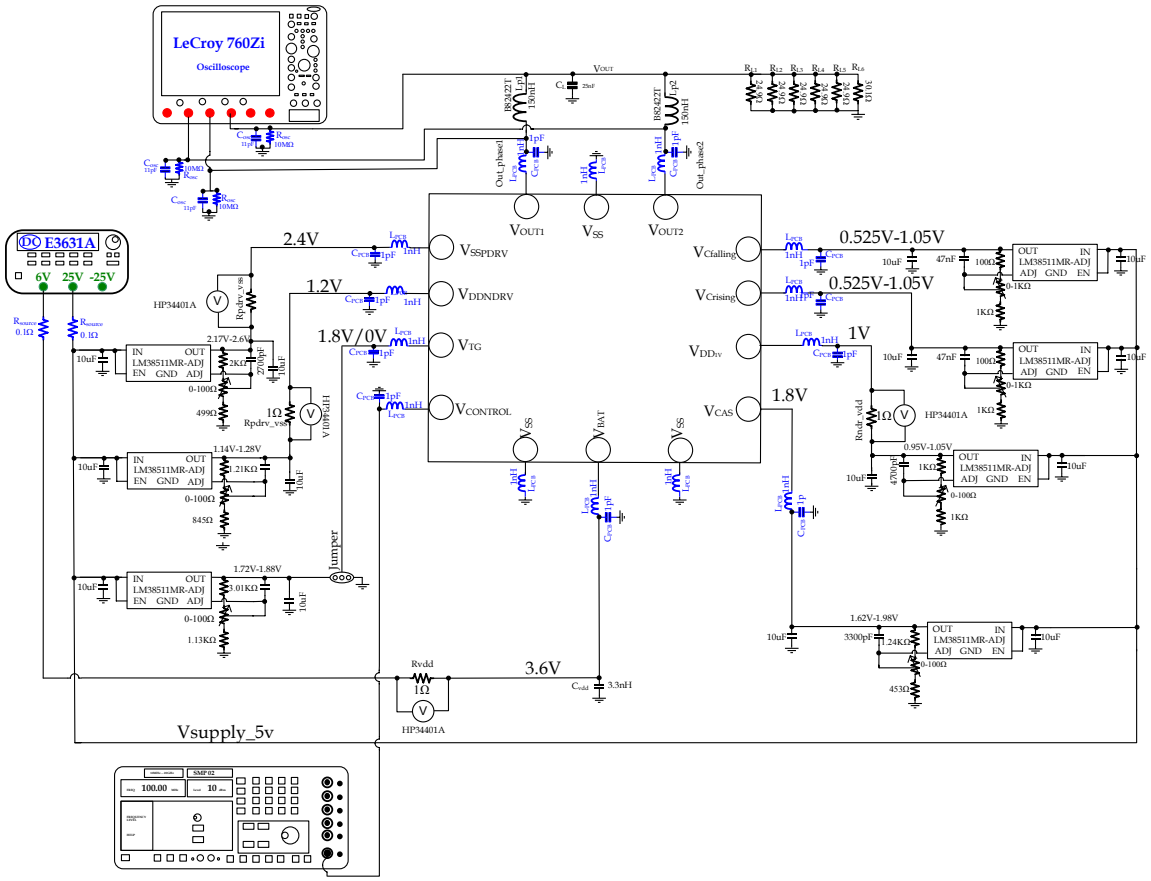


Figure 6-4. Proposed measurement setup of the DC-DC converter.

Figure 6-5 shows the efficiency vs. load current curve. The simulation is done including the major parasitic components, which are parasitic resistances of the V_{BAT}, V_{SS}, V_{SSPDRV}, V_{DDNDRV} and the parasitic components of the PCB. Maximum efficiency drops by 5 % due to the losses in the parasitic components of circuits. But the patters of the curves are similar like the Figure 4-27, where the simulation results are shown without the parasitic effects. In the end the electrical characteristics of the DC-DC converter is shown in the Table 6-4.

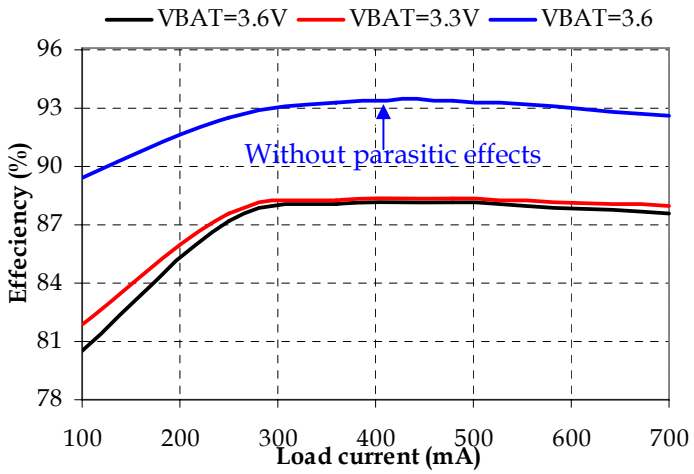


Figure 6-5. Efficiency vs. load current curve for different battery voltage.

Table 6-4: Electrical characteristics of the DC-DC converter.

Pin Name	Min	Typ	Max	Unit
V_{BAT}	3.3	3.6	4.2	V
V_{OUT}	0.5		3	V
I	50		700	mA
$F_{CONTROL}$	20	100	200	MHz
$F_{SWITCHING}$	10	50	100	MHz
$V_{PP\_CONTROL}$			400	mV
V_{OFFSET}	300		1000	mV
V_{CAS}		$V_{BAT}/2$		V
V_{SS_PDRV}		V_{BAT}-1.2		V
V_{DD_NDRV}		1.2		V
V_{TG}		0/1.8		V
V_{C_RISING}	550	900	1000	mV
$V_{C\_FALLING}$	550	950	1000	mV
V_{DD_1V}		1		V
Efficency			88.5	%

6.5 Conclusion

In this chapter a proposal is given for measuring the efficiency of the DC-DC converter is presented. Six resistors are used for changing the load current from 100mA to 700mA for 3V output. The DC bias voltages are given using the voltage regulator LM38511. For this test set up simulation is done for efficiency calculation at 50MHz switching frequency including the major parasitic effects. The peak efficiency drops by 5 % due to the effects of internal and PCB parasitic.

7 Conclusions and future works

Designing high efficiency DC-DC converter is always challenging. DC-DC converter with high output power and lower silicon area makes it more complex. In this work a high efficiency LC type DC-DC converter is designed using Cadence 45nm generic design kit. The design procedure with considerations for high frequency, simulation results, layout and proposed measurement set up are explained in different chapter.

This circuit operates for the voltage range 3.3V to 4.2V and can produce a variable output from 0.5V to 3V. The converter has 2W output power and designed for WCDMA mobile phones. Different state of art techniques are applied for improving the performance of the converter. Dead time control circuits and reduced gate drive voltage of the switches are used to improve the efficiency of the converter. The losses of the converter are minimized for the switching frequency range 10-100MHz. Simulated maximum efficiency is 88.5% for 3V output. Two phase interleaving is done to reduce the output ripple.

In the Table 7-1 comparison of this work and some recently published LC-type DC-DC converter is shown. Due to different technology it is not possible to compare the converters in the straight forward manner. But they can be comparable in terms of parameters like efficiency, silicon area, ripple voltage and output power. From the table it can be conclude that this design shows good performance in terms of efficiency and silicon area.

Table 7-1. Comparison of this work and other LC type DC-DC converter

Ref. #	V_{IN} [V]	V_{OUT} [V]	f_{switch} [MHz]	L [uH]	η [%]	Output ripple [mV]	I_{Load} (max) [mA]	P_{OUT} [W]	Si-area [mm²]	Tech.	Application
[9]	4	2-3	5-10		89	<4	1100	3.2	1.5	0.25 µm CMOS	GSM/ EDGE/ UMTS
[11]	3.3	0.3-3	10	30		<2	750	2	4.62	0.35 µm CMOS	CDMA
[12]	2.7-4.3		130	2×0.11	83	-60dBc	750	2	0.86	0.25 µm LDMOS	WCDMA
[13]	3.3	0.3-3	2.12/ 2.88/ 3.75	2.2			0-750	2		0.13 µm CMOS	EDGE/ WCDMA/ WiMax
[14]	3.6/ 3.3	0-2.9	10	5.3	75.5		420	1.2	4.2	0.25 µm CMOS	GSM900
[15]	1.2	0-1.15	118	0.80		<4.3		0.186	1.32	0.35 µm CMOS	WLAN
[18]	3.3	0.4-2.8	10	2×0.5		<40	725	2	3.09	0.35 µm CMOS	WCDMA
This Work	**3.3-4.2**	**0.5-3**	**10-100 (50)**	**2×0.15**	**88.5**	**10**	**700**	**2**	**1.21**	**45 nm CMOS**	**WCDMA**

There are some limitations of design which can be improved. First of all, the circuit operates in open loop condition. There is no feedback circuit inside the converter. External signal is needed to control the output voltage level. A feedback circuit with oscillator and error amplifier can be designed to control the output voltage level internally. The dead time of this converter is controlled by external signal. But it is possible to design adaptive dead time control circuit, where no external voltage needed for controlling the dead time.

This converter shows poor performance in light load condition. For generating control signal PWM techniques is used here which is good for higher load current management. PFM mode control is good for light load management. So combination of both PFM and PWM mode control can be implemented which will increase the efficiency at light load condition.

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