Analog Integrated Circuits and Signal Processing (2024) 118:187–197
https://doi.org/10.1007/s10470-023-02232-1

An 18–28 GHz dual-mode down-converter IC for 5G applications

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Received: 4 July 2022 / Revised: 25 November 2023 / Accepted: 14 December 2023 / Published online: 21 January 2024

Abstract
Emerging spectrum trends require a higher integration of 5G New Radio Frequency Range 1 (FR1) and Frequency Range 2 (FR2) bands to enhance the availability of spectrum and spectrum-sharing opportunities. To enable the reception of both FR1 and FR2 bands in a seamless hardware entity, we propose combining homodyne and heterodyne architectures. This necessitates the incorporation of a down-converter module that transfers the incoming signals from FR2 bands down to FR1, ensuring compatibility with an FR1 direct-conversion receiver (DCR) for the final signal reception. The primary focus of this paper is the design and implementation of the required integrated down-converter. The module includes an integrated balun, a low-noise amplifier (LNA) with a bypass mode, a dual-mode mixer, and an intermediate frequency (IF) amplifier. The introduced bypass mode helps to further elevate the linearity performance compared to the nominal mode. The bypass mode is designed for joint communication and sensing operation to avoid the compression of the receiver. This work also incorporates a local oscillator (LO) signal distribution network with phase tuning elements using a mixed-signal approach. The circuit is implemented in a 22-nm CMOS process, and the active die area is 0.6 mm^2. The measurements demonstrate that the implemented chip can efficiently perform the required frequency conversion over a wide frequency range of 18–28 GHz. Conversion gain of 4.5–7.5 dB, noise figure of 15–19.7 dB, 1 dB compression point (IP1dB) of − 16 to − 10 dBm, and input third-order intercept point (IIP3) of − 5 to 0 dBm are achieved. The measured IP1 dB and IIP3 for the bypass mode are +0.5 to +4.5 dBm and +8.5 to +10 dBm, respectively.

Keywords 5G · Down-converter · Frequency converter · Heterodyne · Joint communication and sensing · Millimeter wave · Modular receiver · New radio (NR)

1 Introduction

5 G communication brings new features and applications to the users, such as high data-rate communication, sensing and security, industrial 5G, health and medical, and transceivers requiring ultra-low latency and high reliability. Millimeter wave frequency operation together with array transceivers will be widely utilized in future products. Within 3GPP standardization, first step is to shift to the FR2 band at 24.2–52.6 GHz [1]. Although several receiver front-ends have been published in the literature for either FR1 [2–4] or FR2 [5–16], none of them can cover both FR1 and FR2 bands in one system. In the context of emerging spectrum trends, the combination of FR1 and FR2 bands increases the availability of spectrum and spectrum-sharing opportunities. This provides deployment flexibility, enhanced coverage (through the low frequency band FR1), and higher data rates (through the mmWave band FR2) for a 5G communication system. Therefore, developing hardware-efficient methods to enable communication over both FR1 and FR2 bands within a seamless hardware entity is a valid research direction for future 5G systems.

Our solution to cover both FR1 and FR2 bands is illustrated in Fig. 1. In this approach, the down-converter module converts the signal from FR2 bands down to the FR1 band in such a way that an FR1-compatible direct-conversion receiver (DCR) will follow for the final signal reception. In our approach, we convert the FR2 band signal down to 1–7 GHz which enables wideband signal

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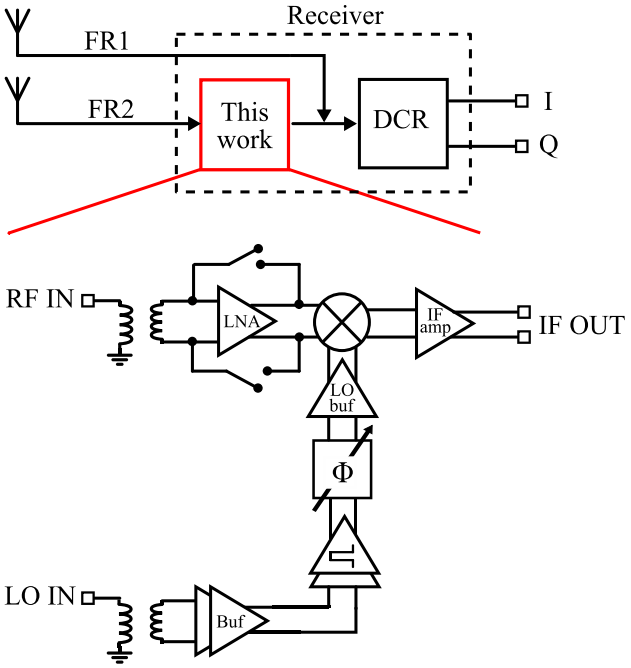

Fig. 1 Concept of a 5G receiver for both FR1 and FR2 bands, and the structure of the implemented FR2 down-converter module

feed to the output. The module is a frequency converter consisting of an integrated balun, an LNA with a bypass mode, a dual-mode mixer, an IF amplifier, and an LO signal chain. The module has intentionally low gain and thus high linearity, to enable operation with a lower probability of compression in a hostile radio environment. Furthermore, it incorporates a bypass mode, as depicted in Fig. 1, in which the LNA is bypassed to further elevate linearity, and the dual-mode mixer is configured for passive operation. The bypass mode is used to avoid the compression of the receiver due to strong transmitter leakage during radar full-duplex operation for joint communication and sensing systems [17, 18].

We have designed a proof-of-concept IC for the down-converter module, fabricated on a 22-nm CMOS process. The circuit occupies an active die area of 0.6 mm^2 and operates over a frequency range of 18–28 GHz. Conversion gain of 4.5–7.5 dB, noise figure of 15–19.7 dB, 1-dB compression point (IP1dB) of − 16 to − 10 dBm, and input third-order intercept point (IIP3) of − 5 to 0 dBm are achieved. The measured IP1 dB and IIP3 for the bypass mode are +0.5 to +4.5 and +8.5 to +10, respectively. In Chapter II we describe the down-converter architecture in detail and Chapter III covers the circuit implementation. Chapter IV represents the measurement results and finally, Chapter V concludes the paper.

2 Architecture

Figure 1 presents the overall system-level concept as well as the structure of the implemented down-converter module including the RF, LO, and IF blocks. The module is designed to work at 5G NR FR2 bands with a heterodyne operation, where the down-converted FR2 signals along with the received FR1 signals will be processed through a direct conversion receiver. The single-to-differential transformer and LNA are the first two stages of the implemented structure. The intention for employing an integrated transformer is to decouple the bonding pads from the gate terminals of the input transistors without using any electrostatic discharge (ESD) diodes. The LNA is followed by a double-balanced Gilbert-cell based mixer for down-converting the RF input signal to the desired IF. Finally, the last stage of the designed structure is a super-source-follower type IF-amplifier that provides a matched impedance for the IF output of the down-converter. This work also represents an inverter-based LO chain. Such a circuitry is usually designed by analog techniques for operation above 10 GHz, see e.g. [12, 19]. However, the deep submicron CMOS technology offers transit frequencies and maximum oscillation frequency of several hundreds of gigahertz [20], promoting the operation of the digital circuits above 10 GHz. The presented LO signal chain is designed by applying the mixed-signal techniques to explore this opportunity.

While operating at the highly occupied radio spectrum of modern urban environment, a radio receiver can potentially be affected by hostile signals from the nearby transmitters that can compress the signal path [21]. Furthermore, during radar-mode operation in joint sensing and communications scheme, strong signal may enter the receiver and the receiver needs to avoid compression. On the other hand, in this scenario sensitivity is not a major issue and we can tolerate high noise figure. As a counter-action for this issue an additional operating mode is implemented that can bypass the amplification stages and improve the linearity of the receiver. The mode control functionality of the proposed mixer is accomplished by switching between the resistive and capacitive loads in the IF outputs as well as whether or not to bypass the input transconductance stage of the mixer. In the nominal mode, the bypass switches around the LNA shown in Fig. 1 are open and the LNA can provide its nominal amplification. The next stage mixer is also configured to operate as an active mixer. In the bypass mode of operation, on the other hand, the bypass switches around the LNA are enabled and the input signal is directly applied to the common source nodes of the mixer's switching quad and in this way, the preceding gain stages including the LNA and the

transconductance stage of the mixer are both bypassed. The LNA employs a reconfigurable bias current using an IDAC and therefore it can be turned off in this mode so that the LNA's input and output nodes are sufficiently isolated. The mixer has also the capacitor loads enabled, and since the transconductance has already been bypassed, the mixer operates in passive mode with a good linearity as expected from the bypass mode.

3 Implementation

3.1 LNA

Figure 2 presents the structure of the LNA. The LNA is based on the capacitively cross-coupled common gate input stage structure [22, 23], and wideband gain response is achieved with a shunt-peaked load. Digital current control is utilized for tuning the bias current.

A transformer at the LNA input converts the input signal from single-ended to differential. In addition, the transformer provides ESD protection for the input transistor gates, and thus ESD protection diodes are avoided. The phase error of the differential signal was minimized with a center tap capacitor C_b. The transformer has a significant impact on the LNA operation, especially on the noise figure (NF) and input matching. The losses add to the total NF directly, since the transformer is the first stage in the chain. In this case, a stacked structure provided strong coupling and consequently minimized losses, and the EM-simulated transformer losses are 1.4–2.1 dB. The effect of the transformer on the input impedance was included in the LNA simulations by first

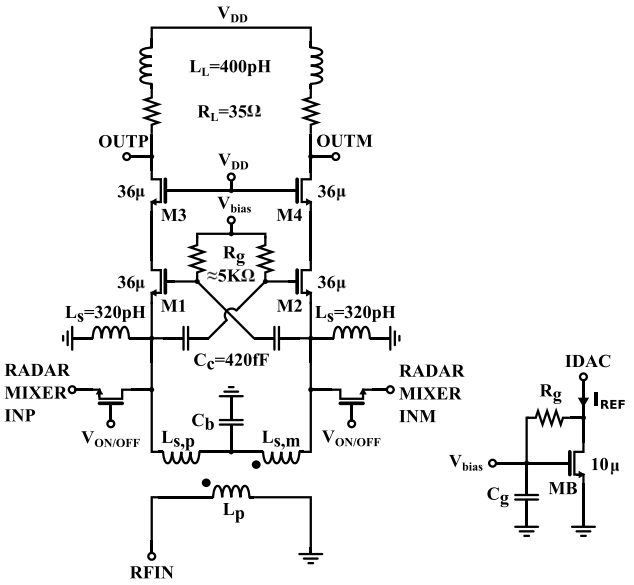

Fig. 2 The schematic of the LNA with the transformer at the input

EM-simulating the transformer and embedding the S-parameters to the LNA top-level simulations. The input matching circuit was designed by first tuning the transformer to the input frequency band. Then L_s and C_c were adjusted to provide the correct impedance.

The common-gate structure has a relatively high minimum NF, which is here decreased by a g_m-boosting method implemented with capacitive cross-coupling technique. The effective transconductance of the input transistors M_1 and M_2 is increased, and consequently their NF decreases. Furthermore, the structure provides wideband input matching together with the transformer. The wideband gain response was achieved with a shunt-peaked load implemented with a load inductor L_L, load resistor R_L, and the input capacitance of the following stage. L_L creates an additional zero to the transimpedance so the decreasing effect of the load capacitance is reduced [24]. The mixer input defines the load capacitance, and the frequency band of the gain response was tuned with the load inductor.

The LNA required configurable biasing because the LNA must be turned off in the bypass mode. The bypass switches were included in the LNA simulations, and in the off-state they degrade the LNA gain with less than 0.5 dB. IDAC provides the reference current I_{REF} for the current mirror visible in Fig. 2. Thus, I_{REF} can be tuned with control bits, and the LNA performance can be adjusted.

3.2 Dual-mode mixer

The overall structure of the implemented down-conversion mixer is shown in Fig. 3. The proposed mixer utilizes a well-known double-balanced Gilbert-cell based structure as the mixer core. The mixer is designed to enable both nominal and bypass modes. The mode control function is accomplished by switching between the resistive and capacitive loads in the IF outputs as well as whether or not to bypass the input transconductance stage of the mixer. The LNA is also bypassed via the M11 and M12 switches. As a specific design detail, the resistors in the gates of these switches improve the linearity by suppressing the fluctuations of the gate-drain and gate-source voltages [25, 26]. The achieved IIP3 improvement by employing this technique in the proposed structure is in the range of 3–5 dBm based on the simulation results.

3.2.1 Nominal mode

By enabling the nominal gain mode according to the requirements mentioned in Table 1 and neglecting the ON and OFF resistances of the configuration switches, the structure of the mixer can be redrawn as shown in Fig. 4. In this mode, resistive loads are in use and there will be a DC current flowing through the switching quad

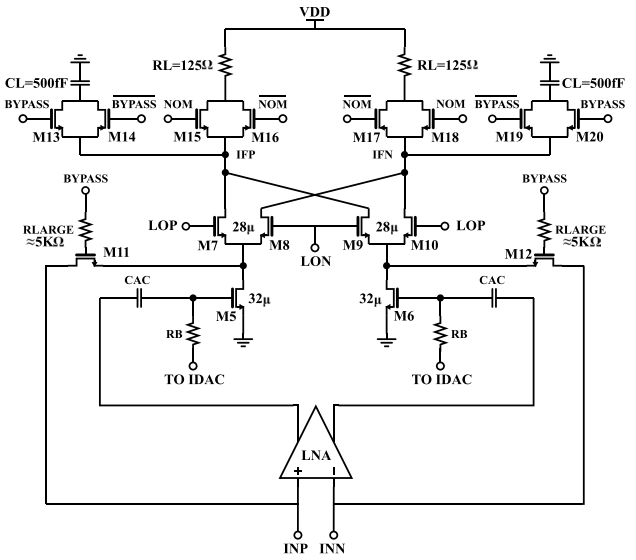

Fig. 3 Overall structure of the dual mode mixer

Table 1 Configuration of the switches

Switch	Nominal mode	Bypass mode
NOM	ON	OFF
$\overline{\text{NOM}}$	OFF	ON
BYPASS	OFF	ON
$\overline{\text{BYPASS}}$	ON	OFF

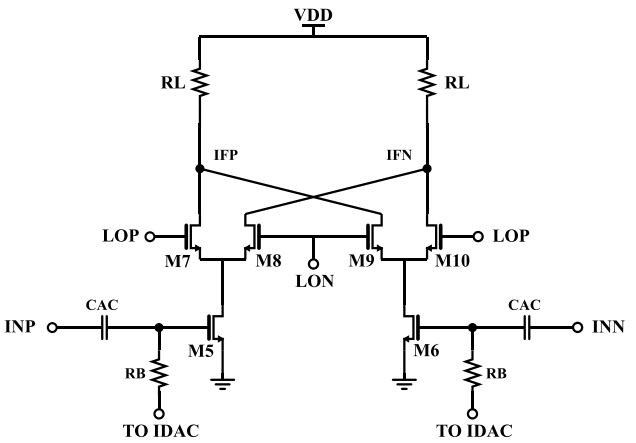

Fig. 4 Down-conversion mixer: nominal mode

and consequently, the mixer operates as an active mixer. The implemented mixer in the nominal mode involves three main stages: input transconductance stage (M5, M6), switching stage (M7, M8, M9, M10), and load stage (RL). Resistive loads are preferred over the active load counterparts to provide a wider bandwidth for the mixer in the nominal mode. Transistors M5 and M6 are biased in the saturation region to provide enough gain for the input signal. On the other hand, the switch transistors, M7–M10, are all biased to conduct but near the pinch-off region to act as switches [27].

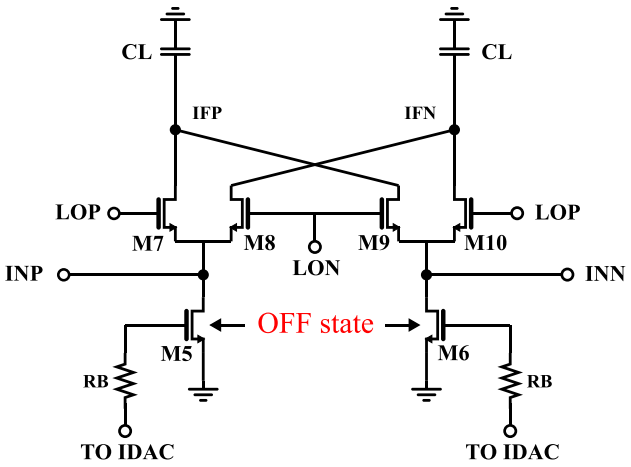

Fig. 5 Down-conversion mixer: bypass mode

3.2.2 Bypass mode

By enabling the bypass mode according to the requirements mentioned in Table 1, the structure of the mixer can be redrawn as shown in Fig. 5. In the bypass mode, the input signal is directly applied from the output of the integrated transformer to the common-source nodes of the switching quad and in this way, the preceding gain stages are all bypassed. This will relax the saturation challenge of the down-converter in the presence of strong interferer. The mixer will also have capacitor loads enabled in this mode and since the transconductance has already been bypassed, there is no DC current flowing through the mixing quad. As a result, the mixer will operate in the passive mode with a good linearity performance as required in the bypass mode.

Passive mixers can operate in either ON or OFF overlap region depending on the dc gate bias of the switching quad. The ON overlap operation is preferred in the proposed structure since it is the desirable region from a linearity perspective [28]. In addition to the linearity performance, the input matching is another important parameter that should be taken into account since with the LNA bypassed the mixer is the first stage of the down-converter in the bypass mode. The required input matching is provided by a series combination of ON resistance of the switch transistors and scaled version of IF impedance formed by the implemented load capacitors (CL). These IF capacitors will also improve the linearity performance of the mixer by attenuating the out-of-band blockers [29, 30].

3.3 IF amplifier

The last circuit block of the implemented down-converter is the IF amplifier stage, which is shown in Fig. 6. This stage provides the required output matching for the implemented module. It also provides IF gain for the desired IF band as well as a sufficient suppression for the out-of-band interferences by the low-pass behavior. The proposed IF amplifier has a two-stage configuration composed of a super source follower followed by a self-biased inverter stage. The super-source follower is selected as the input stage because it provides wider bandwidth compared to the conventional common drain structure. The high input impedance of the super-source follower stage also prevents any loading effect and signal degradation on the mixer's output side. The output stage of the proposed IF amplifier is a self-biased inverter that provides few dB IF-signal amplification and a driving capability to external load. During the design phase the high-frequency non-ideal effects imposed by the chip pads, bonding wires, PCB pads, and PCB traces were taken into account while designing the proposed IF amplifier stage to be matched to a 50Ω load.

3.4 LO chain

Figure 7 illustrates the block diagram for the LO signal chain. It was designed by applying mixed-signal techniques, and it serves as a step to analyze the feasibility of digital circuits operating above 10 GHz. The LO chain targets to provide

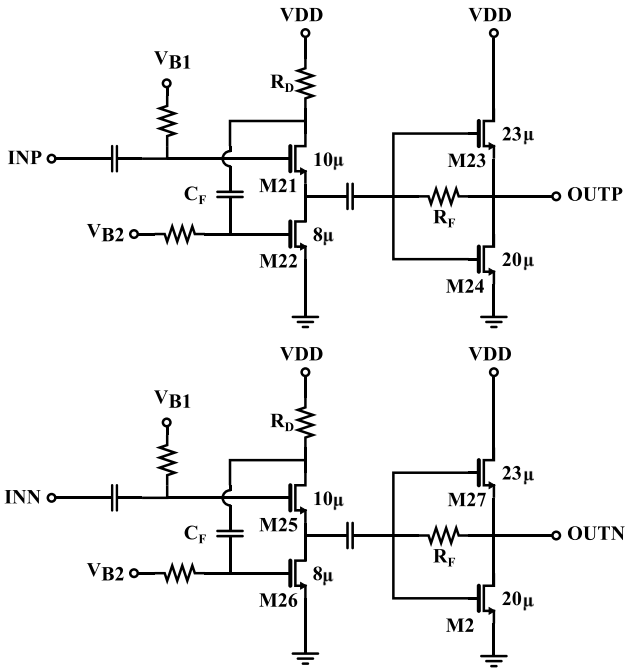

Fig. 6 Overall structure of the IF amplifier

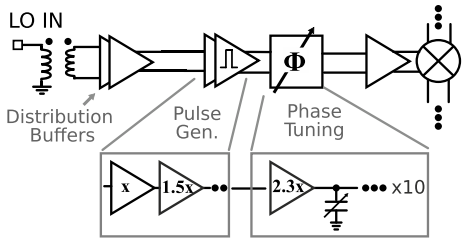

Fig. 7 LO-signal chain

rail-to-rail signals for switching of mixers operating between 12 and 25 GHz LO frequency. It also incorporates varactor-based phase-tuning, to calibrate phase mismatches and study the possibility of LO phase-tuning for phased arrays.

The reference LO signal is fed in through a single-to-differential transformer and distributed across the chip with buffers. Located close to the mixers, pulse generation is the first block in the LO chain. At frequencies above 10 GHz, rail-to-rail signal generation and propagation requires special design considerations. The RC time-constant contributed by the load, interconnect and transistor parasitics limits the driving capability of CMOS circuits. Inverters are chosen as the building block for the LO signal chain as they present the smallest possible load. Pulse generation consists of a chain of inverters, and each inverter drives a load of 1.5 times its size. The inverter loading has been limited to allow amplification of the LO signal to create required waveforms.

The pulse generator is followed by a phase-tuning element, which is composed of a series of 10 inverter-varactor pairs. The varactors are driven by 2.3 times the minimum-sized inverter to maintain signal integrity at the highest frequency of the range, as well as drive the mixers. Digital controls (0,1) enable 1-bit of tuning control in each pair. The varactor-tuning block can calibrate phase mismatches between LO_P and LO_N signals or can serve phase-tuning for possible beamforming application. Figure 8 shows the post-layout simulation results at for the presented LO chain to demonstrate its phase-tuning capability. Here, one of the differential input signal LO_P is phase-tuned by progressively changing varactor controls from V_{DD} to ground. Overall delay tuning is 13 ps. This would correspond to a 30° beamsteering angle in a typical 2 × 2 sub-array antenna at 28 GHz. These results indicate that the mixed-mode design methodology is feasible, yet the performance of this demonstration calls for improvements.

4 Measurements

Figure 9 presents layout and microphotograph of the chip fabricated on a 22-nm CMOS process with a size of 1.25 mm × 1.25 mm including pads. RF transformer, LNA, mixer, IF

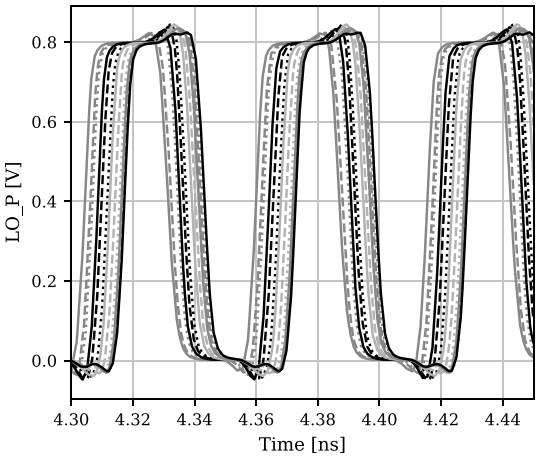

Fig. 8 Simulated time-domain waveforms for phase-tuning at 18 GHz

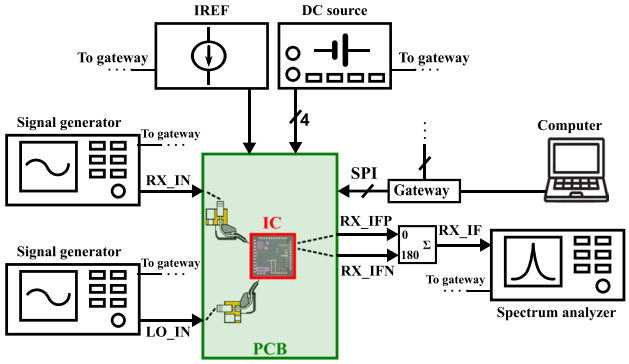

Fig. 10 Simplified measurement setup (CG)

amplifier, and LO related blocks are the main elements of the receive path and are specified using red colored rectangles on the die microphotograph. Active die area is 0.6 mm^2. The implemented IC also includes two TX up-converting elements that are not the subject of this paper. The simplified measurement setup of the implemented down-converter is depicted in Fig. 10. The RF and LO inputs are provided using ground-signal-ground (GSG) probes through the custom designed low-parasitic pads. The EM-simulated parasitic capacitance of these mmw pads are only 20 fF. The IF outputs, on the other hand, are wire-bonded to the PCB and a micro-strip transmission line pair is employed to route them to the edge SMA connectors. Other lower frequency signals, including reference current, DC power supplies and SPIs are also provided through the PCB traces.

The functionality of the implemented down-converter module in both nominal and bypass modes was investigated through various measurements. Figure 11 shows the measured return loss at the RF input. The implemented on-chip transformer along with the input matching network of the nominal mode can preserve S11< −10 dB in a wide range of frequencies starting from 20 GHz up to 30 GHz. On the other hand, the input matching in the bypass mode is mostly defined by the on-chip transformer and the input impedance of the passive mixer. The measured S11 of the bypass mode verifies that the input power in this mode can also be efficiently transferred into the chip in a wide range of frequencies as nominal mode.

The measured conversion gain and noise figure of the module with an IF frequency of 7 GHz are shown in Fig. 12. The receive path can provide a conversion gain of 2.5–7.5

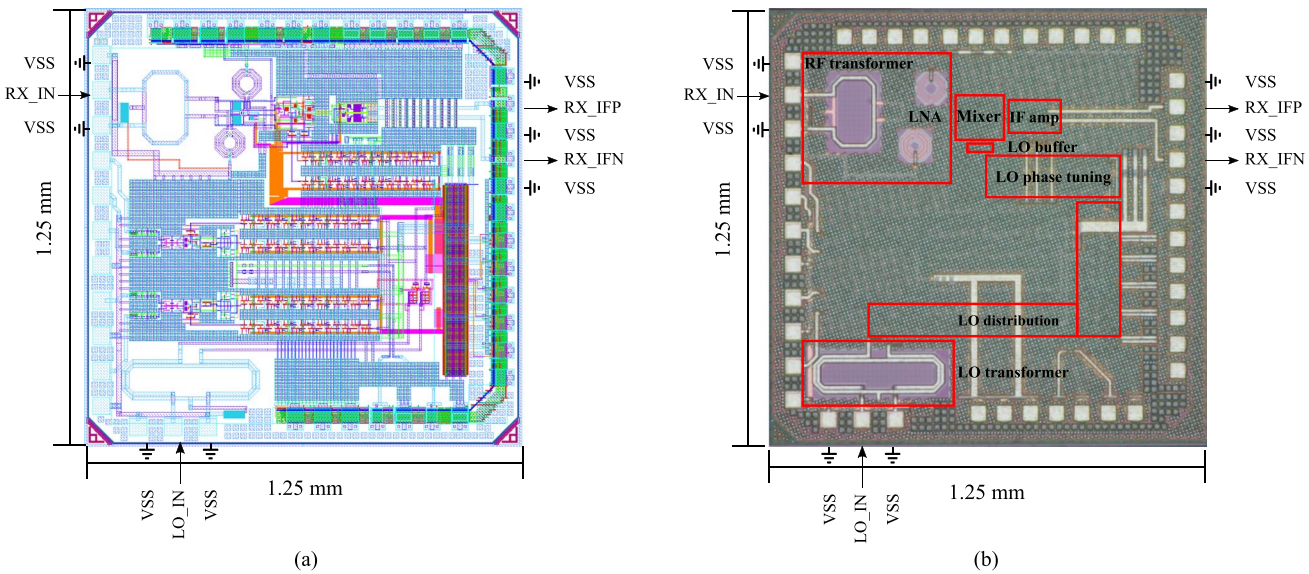

Fig. 9 Layout of the implemented down-converter IC (**a**), microphotograph of the implemented down-converter IC (**b**)

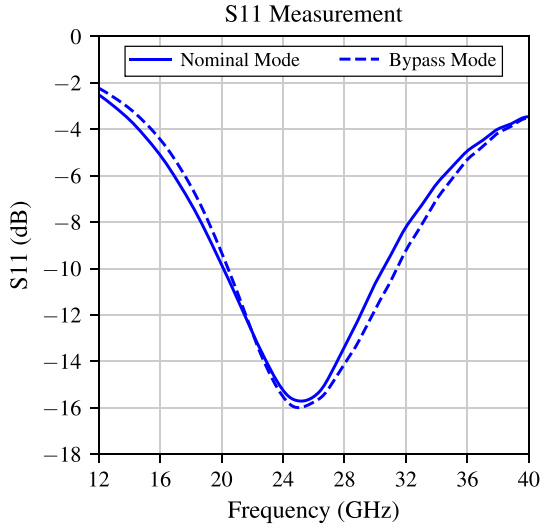

Fig. 11 Measured S11 in both modes of operations

dB and a noise figure of 15–20 dB over the frequency range in the nominal mode of operation. By enabling the bypass mode, the LNA and transconductance stage of the mixer are disabled and in this way, a good linearity performance at the cost of lower gain and higher noise figure is achieved from the bypass mode. As can be seen from Fig. 12, the bypass mode reduces the nominal conversion gain of the down-converter by about 18dB over the frequency range.

Finally, Fig. 13 presents the measured linearity performance of the implemented module, where the IIP3 is measured using a two-tone separation of 100 MHz. The input P1dB is − 16 to − 10 dBm and the in-band IIP3 is − 5 to 0 dBm at 18–28 GHz for the nominal mode of operation. For the bypass mode of operation, the input P1dB is +0.5 to +4.5 dBm and the in-band IIP3 is +8.5 to +10 dBm at 18–28 GHz. Performance summary and comparison with other down-converters in the same frequency range are provided in Table 2. As it can be seen, the implemented chip can achieve state of the art level performance metrics while providing a dual-mode operation at millimeter wave ranges.

5 Conclusions

In this paper, a modular receiver architecture to enable the reception of input signals from both FR1 and FR2 bands using an hardware-efficient approach is presented. As the main requirement to achieve this goal, we have designed and implemented a proof-of-concept down-converter module that converts the signal from FR2 bands down to FR1. The measurement results show that the required frequency conversion is successfully implemented and a CG of 4.5–7.5 dB, NF of 15–19.7 dB, IP1dB of − 16 to − 10 dBm, and IIP3 of − 5 to 0 dBm were achieved for the proposed down-converter module over a wide frequency range of 18–28 GHz. The module also offers a bypass mode in addition to the nominal mode where even a higher linearity is achieved by bypassing the gain stages of the structure. The measured IP1dB and IIP3 for the bypass mode are +0.5 to +4.5 and +8.5 to +10, respectively.

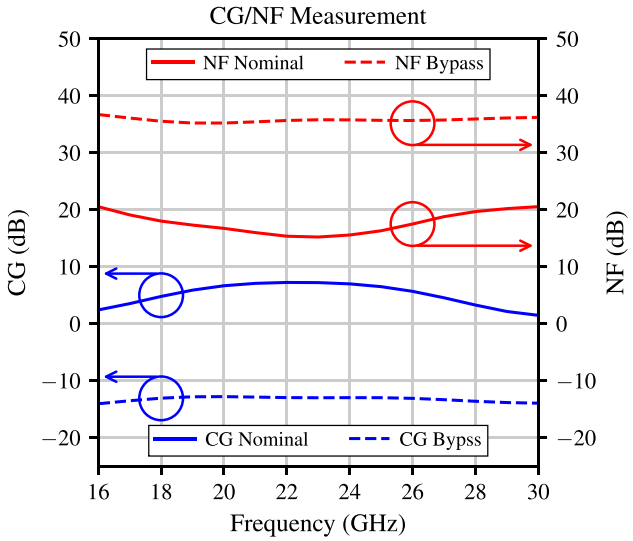

Fig. 12 Measured conversion gain and noise figure in both modes of operations

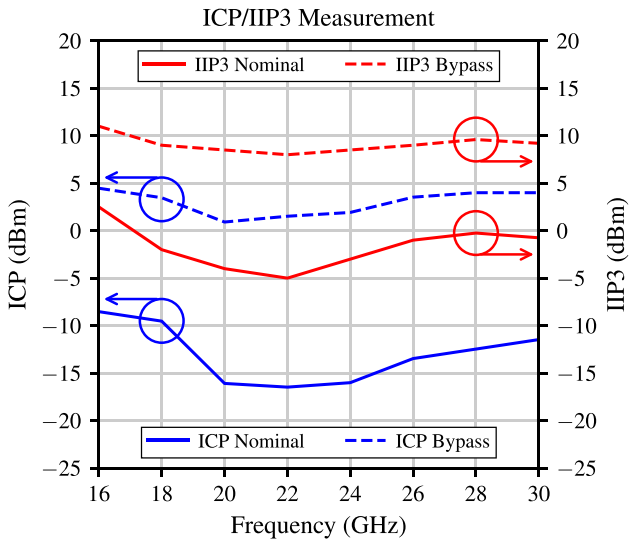

Fig. 13 Measured 1-dB compression point and IIP3 in both modes of operations

Table 2 Performance summary and comparison with millimeter wave down-converters

	This work	[31] ICMMT 2022	[32] AICSP 2022	[33] EuMIC 2022	[34] IMS 2021	[35] RFIC 2021	[36] TCAS-II 2021	[37] TVLSI 2017
Process (CMOS)	22 nm	65 nm	180 nm	65 nm	130 nm	130 nm	65 nm	65 nm
Supply (V)	0.9	1.1	1.8	1	1.5	2.7	1	1.2
RF Freq (GHz)	18–28	20–55	5	30–38	23–25	24–30	24–40	21.5–32.5
IF Freq (GHz)	1–7	2	0–0.1	1	0.1	2–5	N/A	0.001
CG (dB)	4.5 –7.5	2.41	6[2]	4.3	1.3–3	− 1	7.2[3]	15.5
NF (dB)	15–20	12.6–14.7[2]	21[2]	21	15.2−19.3	< 15	12.3[3]	11–20.5
S11 (dB)	< − 8	N/A	N/A	N/A	< − 10	< − 10	N/A	< − 10
IP1dB (dBm)	− 11 ± 4[1]	−11.3	+1.9[2]	− 1	−0.6–0	N/A	−6.1[3]	N/A
IIP3 (dBm)	− 1 ± 10[1]	N/A	+10.6[2]	+ 4	N/A	> + 14.5	−2.5[3]	(− 1.9)–(+8.8)
Integration	LNA + Mixer + IF buf + LO	Mixer + IF buf + LO	Mixer	Mixer + IF buf + LO	Mixer + IF buf + LO	T/R SW + Mixer +IF buf+LO	Mixer + IF buf	LNA + Mixer + IF buf
Power (mW)	RX = 14.8/6.5[1]	7.48	6.64[2]	10.4	10.5	210	10.3	7.1
Area (mm^2)	0.6	0.25	N/A	0.44	0.6	N/A	0.4	0.88

[1]Nominal mode result/Bypass mode result

[2]Simulation result

[3]Measured at 28 GHz RF frequency

Author Contributions SN: Mixer Design, Top-level arrangements, Tape-out activities, IC measurements kaisa ryynanen: LNA design, Transformer design, Tape-out activities MZ: LO design, Tape-out activities AK: IF amp design, Tape-out activities KS: Senior designer for microwave support, System design, Top-level arrangements, Tape-out activities MK: Senior designer for digital support (SPI, IO ring), System design, Top-level arrangements, Tape-out activities vishnu unnikrishnan: System design, Top-level arrangements. LA: System design (communication aspects) MV: System design (communication aspects) JR: Main supervisor of the project

Funding Open Access funding provided by Aalto University.

Declarations

Conflict of interest The authors declare no competing interests.

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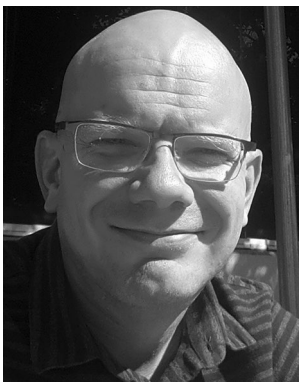

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