High-Precision Time-to-Digital Conversion for Calibration of Outphasing Radio Transmitters

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***Abstract*—Wireless transceivers for 5G NR FR2 frequencies around 30 GHz support signal bandwidths up to 400 MHz to achieve ambitious data rates. The Phase Modulators (PMs) in the FR2 outphasing transmitters generates delays with delay steps of about a few hundred femtoseconds. To calibrate and linearize the PMs, time-to-digital converters (TDCs) that measure delays with higher accuracy in the order of a few femtoseconds are required. To this end, this work explores two synthesizable time interval averaging (TIA) TDCs which employ averaging to achieve high accuracy with low-precision hardware. The results show that the delay quantization step of the converter has an effect only on the time taken to achieve the required accuracy, presenting opportunities to reduce area and power consumption. Simulation shows that a TDC with quantization step of 12.5 ns achieves an accuracy of 0.3 fs by averaging 2^{28} samples. For a 32 GHz 7-bit PM producing a minimum delay step of 244 fs, this implies a TDC of 8-bit precision for each time step. The hardware synthesized towards a 22 nm FDSOI process occupies 0.0004 mm^2 area and consumes 0.3 mW power.**

***Index Terms*—quantization,time-to-digital converter (TDC), delay measurement, random sampling, digital circuit.**

I. Introduction

To meet high data rate requirements, the 3GPP 5G NR FR2 standard [1] utilizes spectral efficient signals with large peak to power ratio at high frequencies of 30 GHz. This makes it challenging for transmitters with linear power amplifiers (PAs) to achieve high efficiency. Hence, the outphasing transmitters [2]–[5], that combine two constant envelope phase-modulated signals to generate the output (See Fig. 1), is an attractive candidate as it allows the use of efficient non-linear PAs on individual signal paths to achieve a linear amplification [6]. The signal component separator (SCS) converts baseband I/Q signal into polar form and separates it into two phase modulating components, Φ_1 and Φ_2. The Phase Modulator (PM) delays the local oscillator (LO) signals based on Φ_1 and Φ_2 and produces the outphasing signals. They are then amplified by non-linear PA and combined. The PM is subjected to non-linearity causing performance degradation. An accurate delay measurement hardware such time-to-digital converter (TDC) with precision in femtoseconds is required to characterize and calibrate away the non-linearity. The measurement time available for the TDC to estimate the generated delay of PM is relatively large, allowing the use of time interval averaging (TIA) [7]. TIA refers to a technique where high-precision estimation of time interval is obtained by averaging large number of measurements in the presence of random measurement errors [8], [9]. Traditionally, a high-precision TIA TDC is designed with a full-custom mixed-signal design flow, where high accuracy is achieved with carefully designed components [10]–[13] and consumes larger area and power. Further, they require a high design effort, and are not easily portable across different semiconductor technologies. In this work, we explore all-digital TIA TDCs that are synthesized with a digital design flow, leading to low area, low design effort, and better cross-technology portability. Two TDC circuits, one with a small and the other with a large quantization time step (T_Q) are designed and evaluated for characterizing a 7-bit PM operating at 32 GHz. The effect of T_Q on the accuracy and measurement time is studied. Simulation of the behavioral and hardware models shows that a TDC with a T_Q of 12.5 ns achieves accuracy of 0.3 fs after a measurement time of 1.2 s (2^{28} samples), which implies 8-bit pecision for a 32 GHz PM with a delay step of 244 fs. The converter synthesized for a 22 nm FDSOI process occupies 0.0004 mm^2 area and consumes 0.3 mW power.The paper is organized as follows. Section II describes the precision requirements for the TDC. Section III presents two TDC circuits. Section IV-A and IV-C analyzes the simulation results from the behavioral model. Section IV-D presents the implementation for the TDC with larger T_Q and section V concludes the paper.

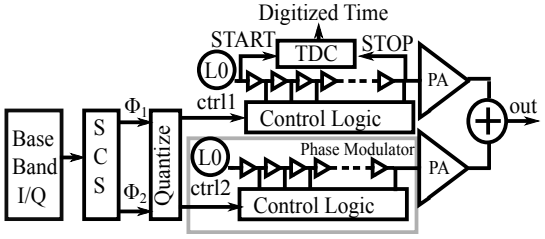
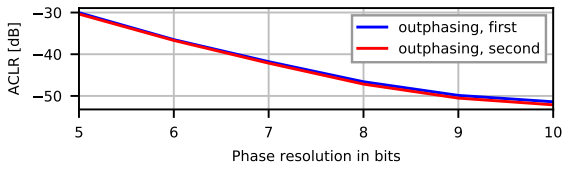


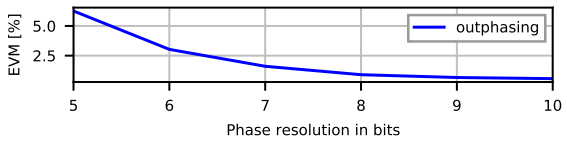
Fig. 1: Outphasing Transmitter

II. Precision Requirement for PM

The phases Φ_1 and Φ_2 (Fig. 1) are in the range [0, 2π] relative to the carrier frequency, and are quantized to a certain resolution before being fed to the control logic of PM, while still meeting performance requirements. This resolution is estimated using system-level model of a configurable transceiver model written in Python programming within our open-source development framework called TheSydekick [14]. In this

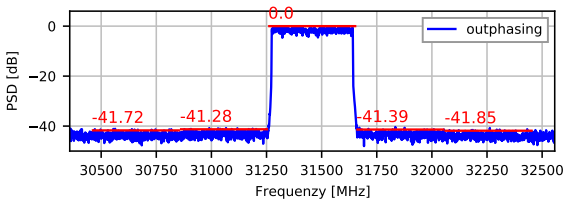


(a)

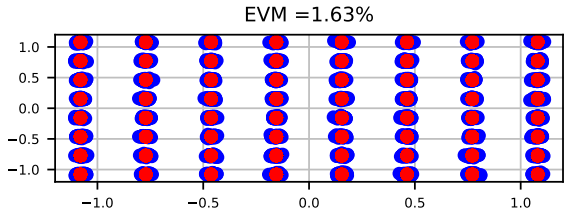


(b)

Fig. 2: a) ACLR & b) EVM for different resolutions of ideal PM



(a)



(b)

Fig. 3: a) ACLR & b) EVM performance of Outphasing Transmitter with 7-bit phase resolution

work, we set the carrier frequency to 32 GHz and bandwidth to 400 MHz. The variation of Adjacent Channel Leakage Ratio (ACLR) and Error vector Magnitude (EVM) of an ideal transceiver chain as a function of resolution of PM is plotted in Fig. 2(a) and (b) respectively. The minimum ACLR and EVM requirement for FR2 [1] is −28 dB and 8 % respectively. However, due to performance degradation that may arise from non-idealities at the analog front-end, we set a conservative design margin of −40 dB and 2%. From Fig. 2(a) and (b), a 7-bit resolution is required implying a 244 fs delay quantization step for a 32 GHz PM. The corresponding Power Spectrum Density and constellation plot is shown in Fig. 3, where the ACLR and EVM are around -41dB and 1.63% respectively. The TDC (Fig. 1) estimates the delay T_{d} produced by the PM by measuring the time interval between the rising edge of LO (START) and the phase modulated RF_out (STOP).

III. Time-to-Digital Converter Design

The individual delay measurements that are averaged in the TIA circuits are obtained by observing the number of quantization time steps (T_{Q}) present between each rising edge

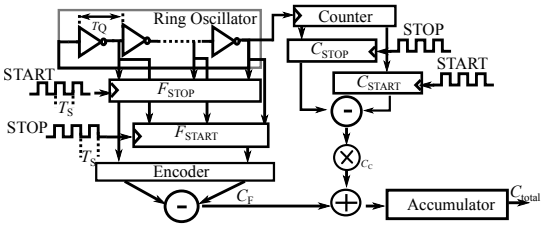


Fig. 4: TDC with small quantization step ($T_{\mathrm{Q}} \ll T_{\mathrm{S}}$)

of START and STOP signals occurring with a periodicity T_{S} (larger than LO period for practical convenience during calibration). In this work, we use T_{S}=4 ns. Further, we allow T_{Q} to be smaller or larger than T_{S}. To avoid individual measurements yielding the same value and to ensure averaging leads to increasing precision, a necessary condition is that T_{S} is not divisible by T_{Q} or vice versa depending on which one is larger. This is ensured by setting $\zeta = T_{\mathrm{S}}/T_{\mathrm{Q}}$ or $T_{\mathrm{Q}}/T_{\mathrm{S}}$ to an irrational number. In this work, we set $\zeta = K\pi$ and $K \in Z$. Two different TDC designs are explored, which are described in the following subsections.

A. TDC with inverter delay as T_Q: $T_Q \ll T_S$

Fig. 4 shows a design where T_{Q} is defined by the delay of an inverter in a Ring Oscillator (RO). A single measurement of T_{d} is obtained by counting the total number of RO transitions (C_{d}) elapsed during T_{d} and mapping it to T_{Q}. C_{d} in turn is obtained by finding the difference between the numerically encoded states of the RO recorded by registers clocked with START and STOP signals as shown in Fig. 4. To deal with errors that are likely within picosecond range T_{Q}, the encoding includes error mitigation techniques to minimize the impact of bubble errors, besides mapping the states of the RO to a numerical value [15]. A counter clocked by RO is added along with respective registers to increase the range of the time interval that can be measured unambiguously, as shown. C_{START} and C_{STOP} are respectively the numbers recorded by the registers connected to the counter triggered by START and STOP, and $C_{\mathrm{C}} = C_{\mathrm{STOP}} - C_{\mathrm{START}}$ gives the integer RO cycles recorded during T_{d}. Similarly, fine measurement C_{F} is obtained from numbers recorded by registers connected to the multi-phase output of RO as $C_{\mathrm{F}} = F_{\mathrm{STOP}} - F_{\mathrm{START}}$. The individual estimate in terms of count is obtained as follows, where N_{osc} is the number of inverters in the RO.

$$C_{\mathrm{d}} = 2 \times N_{\mathrm{osc}} \times C_{\mathrm{C}} + C_{\mathrm{F}} \quad (1)$$

To implement TIA, multiple values of C_{d} obtained by continuously sampling at the rate T_{S} are cumulatively added to obtain C_{total}, which is averaged to yield the final estimate $T_{\mathrm{d\_avg}}$ as

$$C_{\mathrm{total}} = \sum_{n=1}^{N} C_{\mathrm{d}n}, n = 1, 2, 3....N \quad (2)$$

$$T_{\mathrm{d\_avg}} = \frac{C_{\mathrm{total}}}{N} \times T_{\mathrm{Q}} \quad (3)$$

B. TDC with $T_Q > T_S$

To reduce the power consumption, hardware complexity we explore another circuit shown in Fig. 5. Here, we push the TIA by using a T_Q larger than T_S and T_d, that is, we measure the target delay with a quantization step size much larger than the delay being measured. A large T_Q in the range of several nanoseconds is obtained from a single tap of a RO with a large number of inverters. The circuit consists of a measurement counter and a reference counter, both clocked by the RO output. The time interval T_d to be measured is given as an enable pulse at the rate of T_S (extracted from the rising edges of START and STOP) to the measurement counter clocked by RO. The count recorded by the measurement counter during the observation interval of N sample cycles (total time of NT_S) is denoted with C_meas. The reference counter is enabled during the entire measurement time NT_S, and yields the count C_ref. The delay estimate is obtained from the ratio of C_meas to C_ref. The ratio ranges between [0,1] and directly maps to a single period of T_S, with 0 being no delay and 1 being the maximum delay equal to T_S. This method has the advantage that the estimate is agnostic to the absolute value of T_Q and gives a measure in relation to T_S, and is thus resilient to PVT variations. Further, a separate accumulator is not required since the count from measurement cycles is inherently accumulated in the counters. The averaged delay $T_\mathrm{d\_avg}$ can be obtained as

$$C_\mathrm{meas} \approx \frac{N \times T_\mathrm{d}}{T_\mathrm{Q}} \tag{4}$$

$$C_\mathrm{ref} = \frac{N \times T_\mathrm{S}}{T_\mathrm{Q}} \tag{5}$$

$$T_\mathrm{d\_avg} = \frac{C_\mathrm{meas}}{C_\mathrm{ref}} \times T_\mathrm{S} \approx T_\mathrm{d} \tag{6}$$

IV. Simulation and Analysis

The two TDCs described in Section III are characterized for performance based on T_Q and the required number of samples to be averaged (N) using a test input $T_\mathrm{d} = 87.6\,\mathrm{p}s$ and $\zeta = \pi$. The performance metrics, which include the convergence time and accuracy of measurement, are obtained with behavioral models developed using Python programming. Models include non-ideal effects like jitter, making the simulations realistic. Transistor-level simulations are not done due to the exhaustive computational complexity involved with multiple simulations each with millions of samples. Based on the analysis of the simulation results, one of the proposed converters is implemented in hardware and the performance from RTL simulation is reported together with area and power estimates. The values of T_Q for the TDCs are set as follows for the simulations, where $T_\mathrm{S} = 4\,\mathrm{ns}$.

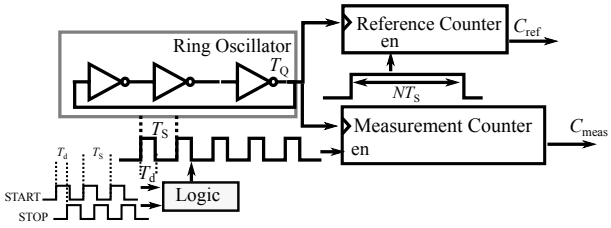
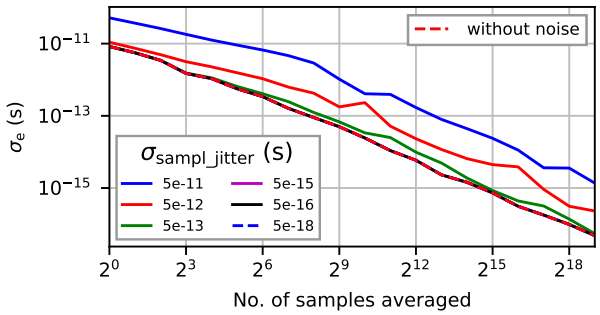
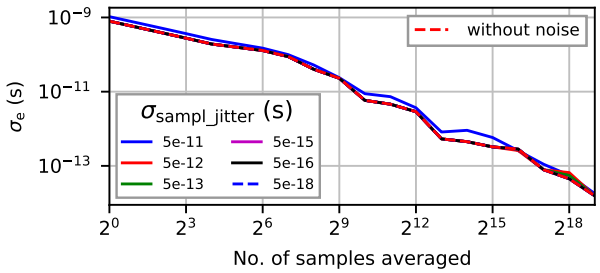


Fig. 5: TDC with large quantization step ($T_\mathrm{Q} > T_\mathrm{S}$)



(a) TDC with $T_\mathrm{Q} \ll T_\mathrm{S}$



(b) TDC with $T_\mathrm{Q} > T_\mathrm{S}$

Fig. 6: σ_e of estimated delays vs. number of samples in the presence of different levels of sampling clock jitter

$$T_\mathrm{Q} \ll T_\mathrm{S} \rightarrow \zeta = K\pi = \frac{T_\mathrm{S}}{T_\mathrm{Q}} \rightarrow T_\mathrm{Q} = \frac{T_\mathrm{S}}{45\pi} \approx 28\,\mathrm{ps} \tag{7}$$

$$T_\mathrm{Q} > T_\mathrm{S} \rightarrow \zeta = K\pi = \frac{T_\mathrm{Q}}{T_\mathrm{S}} \rightarrow T_\mathrm{Q} = \pi T_\mathrm{S} \approx 12.6\,\mathrm{ns} \tag{8}$$

A. Behavioral Modelling of TDCs in Python

The TIA-TDC is modeled by defining three vectors of successively increasing time values that represent T_Q, START, and STOP signals. The step between each time value in the START vector is determined by T_S. The same is applicable for the STOP vector but an offset of T_d is added. The time values of vector T_Q is determined by (7) or (8) depending on which TDC is modeled. Each pair of time values in START and STOP vectors represent a sample, which is quantized by the vector T_Q. The respective quantized output from START is subtracted from STOP vectors to yield individual estimates of T_d. They are then averaged to yield the final delay estimate.

1) Jitter Modeling: To make the behavioral models realistic, we model sampling jitter and oscillator jitter in the circuit. The sampling jitter arises due to the timing variations in the START or STOP causing variations in T_d, and it is modeled by adding Gaussian noise to the START. The Gaussian noise has mean ($\mu = 0$) and standard deviation ($\sigma_\mathrm{sampl\_jitter}$). The oscillator jitter arises due to timing variations of the transitions in the ring oscillator, which accumulates over time. It is modeled by adding Gaussian distributed noise with $\mu = 0$ and $\sigma_\mathrm{osc\_jitter}$ to the ring oscillator output transitions cumulatively.

B. Simulation of the Behavioral Models

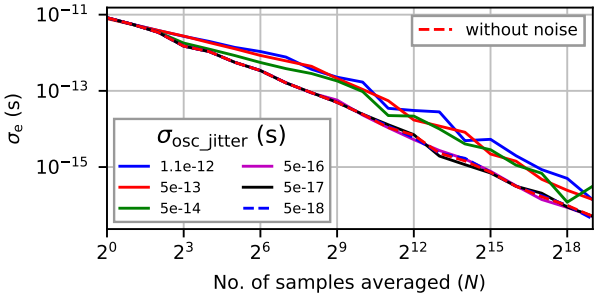
The models are simulated and the performance is determined by plotting the standard deviation of error (σ_e) against the number of samples averaged (N), as shown in Figs. 6 and 7 for the two designs. It shows the variation of the estimated delay from the actual delay. The effect of different levels of $\sigma_{\text{sampl\_jitter}}$ on performance is shown in Figs. 6(a) and 6(b) for $T_Q \ll T_S$ and $T_Q > T_S$ respectively. Similarly, the effect of varying $\sigma_{\text{osc\_jitter}}$ is shown in Figs. 7(a) and 7(b). In Figs. 6 and 7, it can be seen that irrespective of the level of jitter, σ_e reduces with increasing N for both designs, implying that the accuracy of both the TDCs increases with the extent of averaging and the error steadily approaches zero. The effect of jitter is more in the TDC with $T_Q \ll T_S$ as can be seen when comparing Figs. 6(a) & 7(a) with Figs. 6(b) & 7(b). Despite that, this converter with $T_Q \ll T_S$ still requires lesser N to achieve higher accuracy due to its finer T_Q when compared with $T_Q > T_S$. Note that accuracy in the range of femtoseconds is obtained after 1 ms for $T_Q \ll T_S$ at $N = 2^{18}$, whereas $T_Q > T_S$ achieves an accuracy of only picoseconds. Therefore, a larger N and consequently a measurement time that is approximately thrice its counterpart is required for $T_Q > T_S$ to provide the same accuracy.

C. Hardware Implementation of TDC with $T_Q > T_S$

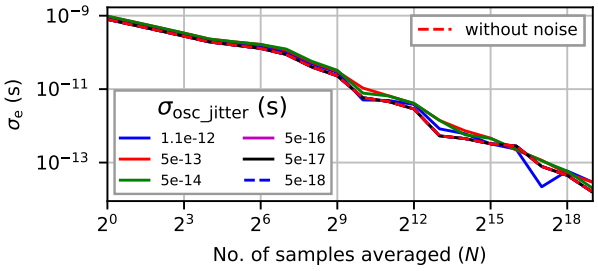
Although the TDC with $T_Q \ll T_S$ requires lesser measurement time for higher accuracy, it is challenging to design due to sampling-induced errors associated with small T_Q. The converter with $T_Q > T_S$ is more efficient in terms of area, power and design effort despite the longer measurement time required for a given accuracy and therefore, is selected for hardware implementation. The measurement and reference counter of the implemented TDC are 31 bits for longer measurement ranges. The metastability at the measurement counter due to the asynchronous enable pulse is reduced by providing the enable pulse through flip-flops clocked by RO. The area and power values obtained after place-and-route for 22 nm FDSOI technology are 0.0004 mm^2 and 0.3 mW respectively. The static delay does not affect the delay measurement, as linearity characterization requires only relative time measurement for different codes, and the effect of static delay is removed.

D. RTL Simulation

The largest delay produced by the PM is 31.25 ps. Considering its internal static delay T_t of 1 ns arising due to placement and routing, the maximum delay to be digitized by the TDC is 1.032 ns. With T_Q=12.6 ns, the maximum measurement time possible without the reference counter (clocked by T_Q) overflowing is 26 s. Simulations show the possibility of achieving sub-femtosecond accuracy using this TDC. In Fig. 8, the TDC is provided with an array of inputs with delay steps of 1 fs, and the output is plotted. It is seen to resolve these delay steps with an accuracy of 0.3 fs after a measurement time of 1.2 s and a total of 2^{28} samples were used for each delay estimate. For 32 GHz PM with a minimum delay step of 244 fs, the TDC approximately has an 8-bit precision for each LSB of the PM.



(a) TDC with $T_Q \ll T_S$



(b) TDC with $T_Q > T_S$

Fig. 7: σ_e of estimated delays vs. number of samples in the presence oscillator jitter

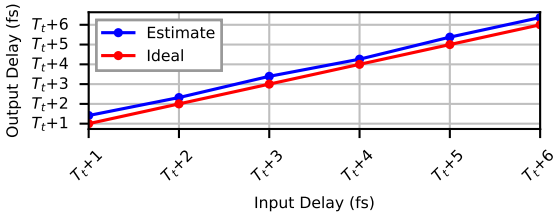


Fig. 8: Delay estimated by TDC vs. the actual delay with $N = 2^{28}$ at each input and T_Q = 12.6 ns

V. Conclusion

Two synthesizable TIA based TDCs were introduced in this paper. Comparison of both the architectures based on their quantization step size, T_Q, showed that both can achieve arbitrary precision with increasing number of samples averaged. The TDC with smaller T_Q approaches zero error relatively faster. Yet, considering the long measuring time availability for calibration, the low complexity TDC with larger T_Q is chosen for synthesis in a 22 nm FDSOI. The total area and power obtained were 0.0004 mm^2 and 0.3 mW respectively. Hardware simulation results showed that accuracy in the range of 0.3 fs can be obtained even with a quantization step of 12.6 ns when averaging 2^{28} samples, allowing the TDC to have approximately 8-bit precision for measuring each delay step of the 7-bit PM operating at 32 GHz.

VI. Acknowledgement

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