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OPTIMIZATION OF InP ETCHING USING INDUCTIVELY COUPLED PLASMA

Bachelor's thesis
Faculty of Engineering and Natural Sciences
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ABSTRACT

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The etching of semiconductor components is one of the most critical process steps in the manufacturing process of semiconductor devices, as the desired pattern can be transferred into the semiconductor wafer with lithography and etching steps. In this Bachelor's thesis, plasma etching of InP-based semiconductor wafers is optimized in cooperation with Modulight Corporation. The goals are to transfer the etching process from reactive ion etching (RIE) equipment to inductively coupled plasma (ICP) RIE equipment, decrease the etching time, and improve the etching profile. In the future, the process is planned to be used in production.

A total of five 3" InP-based wafers were etched, one reference wafer with RIE and four wafers with ICP-RIE, varying the etching time. Etch depths were measured with a contact profilometer and scanning electron microscope (SEM) to compare the etch depths and the profiles of the ridges. The etch depth next to the ridge was also looked at because it is significant for the operation of semiconductor devices. The etching process used gave reliable results. It was observed from the results that the etch rate increased, and the etch profile was better in ICP-RIE processes than in the RIE reference. In addition, a profile with undercutting was not formed. It was also found that the etch rate was up to 500 nm/min in ICP-RIE processes, which was 15 times faster than in the RIE reference. On the other hand, the footing value was higher in ICP-RIE etchings when compared to the RIE reference. Moreover, it was observed that possibly the hard mask ran out from the edges of the pattern during longer ICP-RIE etchings, which was caused by mask erosion. Still, after all, the profiles were smoother.

Overall, the results were promising, and the etching process can be transferred from RIE to ICP-RIE. In the future, a thicker hard mask could be tested to see if the same etch depth can be reached with a mask surviving the whole etch time. In addition, the process parameters could be optimized to decrease the footing. Also, other InP-based compound semiconductors could be tested to see if similar results can be achieved with them.

Keywords: contact profilometry, ICP-RIE, InP, plasma etching, semiconductor device, SEM

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TIIVISTELMÄ

Mira Säe: InP-pohjaisten puolijohteiden plasmaetsauksen optimointi
Kandidaatin työ
Tampereen yliopisto
Tekniikan ja luonnontieteiden kandidaattiohjelma
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Puolijohdekomponenttien syövytys on yksi keskeisimpiä prosessivaiheita puolijohdelaitteiden valmistusprosessissa, sillä haluttu kuvio voidaan siirtää puolijohdekiekolle litografian ja syövytyksen avulla. Tässä opinnäytetyössä optimoidaan InP-pohjaisten puolijohdekiekkojen plasmasyövytystä yhteistyössä Modulight Oyj:n kanssa. Työn tavoitteet ovat siirtää syövytysprosessi reaktiivinen ionisyövytys (RIE) -laitteelta induktiivisesti kytketty plasma (ICP) RIE -laitteelle sekä lyhentää syövytysaikaa ja parantaa syövytysprofiilia. Prosessi on tarkoitus ottaa myöhemmin käyttöön tuotannossa.

Yhteensä viisi 3"InP-pohjaista kiekkoa prosessoitiin, yksi referenssikiekko RIE:llä ja neljä kiekkoa ICP-RIE:llä muuttaen syövytysaikaa. Syövytyssyvyyttä ja -profiilia arvioitiin kontaktiprofilometrillä ja pyyhkäisyelektronimikroskoopilla. Harjanteen kulmassa olevaa syövytyssyvyyttä tarkasteltiin myös, koska sillä on mahdollisesti merkitystä puolijohdelaitteiden toiminnan kannalta. Käytetty syövytysprosessi antoi luotettavia tuloksia. Tuloksista havaittiin, että syövytysnopeus kasvoi ja syövytysprofiili oli parempi ICP-RIE-syövytyksissä kuin RIE-syövytyksessä. Lisäksi ICP-RIE:llä prosessoitaessa ei muodostunut alileikkausta, mikä paransi profiilia. Syövytysnopeus ICP-RIE:llä oli jopa 500 nm/min, mikä oli noin 15 kertaa nopeampi kuin referenssiprosessissa. Toisaalta ICP-RIE-syövytyksen footing-arvo oli suurempi kuin RIE-syövytyksessä. SEM-kuvista havaittiin myös, että maski loppui mahdollisesti kesken pidempien ICP-RIE-syövytysten aikana, mikä aiheutti maskin eroosiota. Silti profiilit olivat tasaisempia ICP-RIE-syövytyksissä.

Kaiken kaikkiaan tulokset olivat lupaavia ja syövytysprosessi voidaan siirtää RIE:ltä ICP-RIE:lle. Jatkossa prosessia voitaisiin parantaa käyttämällä paksumpaa syövytysmaskia, jotta nähtäisiin, voidaanko sama syövytyssyvyys saavuttaa niin, että maski ei lopu kesken harjanteen reunoilta. Lisäksi prosessiparametreja voitaisiin optimoida footing-arvon pienentämiseksi. Syövytysprosessia voisi myös kokeilla muille InP-pohjaisille puolijohteille, jotta nähtäisiin, voidaanko niilläkin saavuttaa vastaavia tuloksia.

Avainsanat: ICP-RIE, InP, kontaktiprofilometria, plasmaetsaus, puolijohdelaite, SEM

Tämän julkaisun alkuperäisyys on tarkastettu Turnitin OriginalityCheck -ohjelmalla.

PREFACE

This Bachelor's thesis was carried out in Modulight Corporation. First, I would like to thank my supervisors, Adj. Prof. Jukka Viheriälä, R&D Engineer Timo Aho and R&D Engineer Riina Ulkuniemi, who guided me during this writing process. They all helped me through these experiments and offered me guidance, especially for narrowing down the topic of this thesis and in perspective observations.

I would also like to thank the whole Laser family of Modulight, with whom I have had many unforgettable moments during the past year. Special gratitude belongs to Timo Aho and Riina Ulkuniemi, who have guided me in my professional and personal life. Finally, I would like to thank my family for their help and encouragement at different stages of this project and my friends for their peer support and motivation during spring 2023.

In Tampere, 3rd May 2023

Mira Säe

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LIST OF SYMBOLS AND ABBREVIATIONS

A	anisotropy
R_a	center line average
R	etch rate
S	selectivity
ρ	resistivity
BOE	buffered oxide etchant
BSE	backscattered electrons
HAR	high aspect ratio
IC	integrated circuit
ICP-RIE	inductively coupled plasma reactive ion etching
LED	light-emitting diode
LSI	large scale integration
PECVD	Plasma Enhanced Chemical Vapor Deposition
RF	radio frequency
RIE	reactive ion etching
SE	secondary electrons
SEM	scanning electron microscope
UV	ultraviolet

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1. INTRODUCTION AND BACKGROUND

The semiconductor device industry is a fast-growing industry in which the driving principle has been Moore's law. It was stated by Intel cofounder Gordon Moore in 1965, and it sounds as follows: the number of transistors and resistors on an integrated circuit (IC) chip doubles every 18 months. [1, p. 1435]

Dry etch patterning of semiconductor devices is interesting for different applications, from bipolar transistors to lasers. The requirements for the etching of high aspect ratio (HAR) patterns via selective etching have accelerated the development of versatile high-density plasma tools capable of operating over many ion densities. This feature enables flexibility in designing etch processes for requirements like high etch rate and low damage. [2]

In the manufacturing process of semiconductor devices, plasma etching technology systems, such as reactive ion etching (RIE) and inductively coupled plasma (ICP) RIE, are currently widely used. These manufacturing technologies make it possible to remove, i.e., dry etch, really thin layers of material in a controlled way. [1, p. 1435] The most used high-density plasma reactor type is ICP-RIE because of its ease of scalability, plasma tuning, and that there are no expensive water-cooled magnets in ICP reactor. [2]

Plasma etching technologies have enabled the introduction of technological innovations, especially in manufacturing large-scale integration (LSI) devices [1, p. 1452]. An LSI device is fabricated through many depositions and etching steps, so the etch processing accuracy will determine the device performance and yields [3, p. 9]. Smooth and vertical sidewalls are desirable for applications in photonic circuits [4] and are an important factor in controlling device dimensions [5]. Many plasma etching techniques, like electron cyclotron resonance plasma etching, ICP etching, and ion beam etching, have been used to fabricate anisotropic etch profiles. However, they tend to engender damage to the active and contact layers. The damage can be reduced by using low-energy ion bombardment during the etch process. [5, p. 1130]

Often etched materials are, for instance, Si, GaAs, Ge, and InP. In this Bachelor's thesis, the focus is on the etching of InP. The most used etching chemistry for In-based semiconductors is CH_4/H_2, which produces a smooth pattern transfer. However, these processes have low etch rates, hydrogen passivation of near-surface dopants, and polymer deposition and contamination of the chamber and the InP wafer. [6]

This Bachelor's thesis aimed to transfer CH_4/H_2 etching processes from RIE to the ICP-RIE system. In addition, other aims were to achieve a smoother profile and to decrease the etching time. The etching process was done to four 3" InP wafers by changing the etching time and adding chlorine. In addition, the etch profiles of etched ridges were studied with scanning electron microscopy (SEM) equipment and a contact profilometer. First, the basics of semiconductor materials and semiconductor fabrication processes are introduced. Then, methods and equipment are presented, focusing on RIE and ICP-RIE plasma etching reactors. Lastly, results are introduced, and conclusions are discussed.

2. SEMICONDUCTOR MATERIALS

Semiconductors are materials that have some properties similar to insulators and some similar to conductors. Nevertheless, there are many physical properties in which semiconductors differ from other materials significantly, one of which is resistivity ρ. Resistivity is an ability of a material to resist an electric current. A good conductor has a low resistivity, whereas a good insulator has a high resistivity. In semiconductors, the resistivity is highly dependent on temperature and usually decreases with increasing temperature. [7, p. 60]

Many semiconductor materials in the table of the elements, such as silicon (Si) and germanium (Ge), appear in group IV and are called elemental semiconductors. There are also many compounds of two or more elements, called compound semiconductors. They can be formed from groups III and V, such as GaAs and InP; the II-VI compounds, such as CdS and ZnSe; the III-VI compounds, such as GaS and InSe; and the IV-VI compounds, like PbTe and PbS. Also, the properties of these semiconductor materials depend on the presence of impurities such as boron and arsenic. Adding impurities is called doping, and the deviations from stoichiometry are adequate for the properties of semiconductor devices. [8, pp. 1-2] The groups in the periodic table for frequently used semiconductor materials are presented in Table 2.1.

Table 2.1. *Common semiconductor materials [9, p. 22].*

II	III	IV	V	VI
	B	C	N	
	Al	Si	P	S
Zn	Ga	Ge	As	Se
Cd	In		Sb	Te

In n-type (or negative-type) semiconductors, there are free electrons in the conduction band made by adding donor impurities. In p-type (or positive-type) semiconductors, there are free holes in the valence band made by adding acceptor impurities. [8, p. 90]

2.1 Bandgap

One another fundamental difference between a semiconductor and other materials is the bandgap. Each atom has its orbital structure, varying between semiconductors, conductors, and insulators. Electrons orbit around the nucleus in a 3D shell, which is why electron orbits are called shells. An electric current is not conducted in a valence shell, but if an electron escapes the constriction of the nucleus and leaves the valence shell, it can conduct an electric current as a free electron.

When atoms bond to make solid materials, their orbits overlap and form bands. In conducting bands, electrons can move freely and conduct electric currents when an electric field is applied. In the valence band, electrons cannot move freely because they are bound to the nuclei. Also, the valence band has a lower electric potential, so electrons tend to stay there.

For most metals, the conducting and valence bands have a very small bandgap so that electrons can jump across even at room temperature. Therefore, the conducting band has many electrons, making them great electrical conductors. For insulators, the situation is different: the gap is too large for electrons to jump across, so the conducting band has just a few electrons to conduct electric currents. For semiconductors, the bandgap is somewhere between insulators and conductors. [7, pp. 59-62]

For light-emitting semiconductor devices, such as light-emitting diodes (LED)s and lasers, the bandgap determines the wavelengths of light that the semiconductor can absorb or emit. For instance, the band gap of GaAs is about 1.43 eV, a wavelength in the near infrared. [9, p. 22]

2.2 Semiconductor devices

A discrete device is an electronic device such as a resistor, diode, capacitor, or transistor. On the other hand, an IC device is a functional circuit built on a single substrate and exists in many electronic products. [7, p. 19] IC chip technology has been growing for over 50 years, and they have developed in complexity and usefulness. They are widely used in automobiles, televisions, digital cameras, smartphones, and many other appliances. [7, p. 1]

Many interesting and useful device functions are based on the interaction of photons in semiconductors. The devices provide optical sources and detectors, enabling broadband communication and data transfer via optical fibers. The field is called optoelectronics. Some devices detect photons, some emit them, and some convert optical energy into electrical energy, such as photodiodes and solar cells. Emitters of photons have incoherent sources like LEDs and coherent sources like lasers. [9, p. 430]

3. FABRICATION PROCESS OF SEMICONDUCTOR DEVICES

The semiconductor industry has continued developing in higher density and higher performance devices through the evolution of lithography, pattern transfer and process technology. Further improvements for cost-effective semiconductor devices are becoming even more challenging. [10] High-quality devices require lots of raw materials for wafer processing, ultra-high purity and extremely low particle density. In addition, many used process materials are also poisonous, flammable, explosive, or corrosive, which requires employees to receive special training to ensure proper handling. [7, p. 12] On the other hand, if the wafer size is increased, more chips can be made on a wafer. Assuming that the research and development costs stay manageable, manufacturing IC chips can be quite profitable. [7, p. 20] In this chapter, it is represented how a transition of a pattern occurs through lithography and etching.

3.1 Optical lithography

Optical lithography is the main method for cost-effectively replicating small, micrometer-scale patterns on the sample's surface. In optical lithography, the pattern replicates to the substrate with light shone through a photomask with transparent and opaque areas. A photosensitive thin polymer film, photoresist, is deposited onto the substrate surface. This photoresist is exposed to the light through the photomask. [11] To perform this process step, the photoresist needs a good adhesion to the wafer surface. [10].

In optical lithography, the exposure can be done by electromagnetic radiation in the ultraviolet (UV) or X-ray region. UV light is efficient because it can expose wide areas at once. Although, the feature size is limited by the wavelength of light, which in UV-lithography, is as low as 1 µm. [12, p. 78] That is due to the Rayleigh diffraction limit for any electromagnetic radiation twice the wavelength. [13, p. 108]

Exposed areas in photoresist will transform to either soluble (positive) or nonsoluble (negative) photoresist, depending on the chosen chemistry. Further steps are taken to transfer the copied patterns to the substrate. Other options for the lithography step are, for instance, interference lithography, electron beam lithography and nanoimprint lithography.

[11]

3.2 Etching

The pattern fabricated to photoresist by lithography can be etched into the semiconductor materials. Etching can either be done by a chemical reaction or physical sputtering. [1, p. 1440] In chemical etching, the material can be etched with a spontaneous chemical reaction [13, p. 127], while in physical etching, sputtering is done with by-products that are generated on the surface by chemical reactions [1, p. 1440].

Etching can be done with wet etching or plasma etching. Wet etching is usually done in baths or tanks [13, p. 127] while plasma etching needs a vacuum chamber by reactive gases that are excited or ionized by radio frequency (RF) fields [13, pp. 132]. In this thesis, the focus is on plasma etching.

Many wet and dry etching processes utilize hard masks because resists are not tolerant enough under harsh etch conditions [13, p. 134]. The hard mask material is etched with a photoresist mask, the photoresist is then stripped, and the etch process is performed using the hard mask only [13, p. 135].

3.2.1 Etching effects

One of the most important characterization ways for etching is etch rate R. It is a way to measure how fast material is removed during the etch process. [13, p. 127] Etch rate is defined as thickness change caused by the etch process divided by etch time. Etch depth is the difference between the bottom and top values of the etched pattern and can be determined by step height using a stylus profilometer [14] or imagining a cross-section of the etched sample by SEM measurement [15, p. 317-318].

Etch rate differs between chemical and physical etching and depends on the chemistry used [13, p. 127]. It is essential to have a uniform etch rate across the wafer [15, p. 318]. Also, the etch rate ratio between the material and hard mask must be considered. It can be characterized as selectivity S as

$$S = \frac{R_1}{R_2} \tag{3.1}$$

where values R_1 and R_2 are the etch rates of the hard mask and material [15, p. 320]. High selectivity enables deep etch depths and the possibility to etch with etch stops [13, p. 135].

Also, etch profile is one of the most important characteristics of etch. It affects the following processes and can impact the device's performance. It can also be defined with SEM.

[15, p. 320] One factor in measuring the etch profile is to compare the lateral and vertical etch rates of the etching process, also called anisotropy. Anisotropy A can be given by

$$A = 1 - \frac{R_L}{R_V} \tag{3.2}$$

where R_L and R_V are the lateral and vertical etch rates. The etching process is anisotropic if the equation equals 1 (lateral etch rate is 0). The etching process is isotropic if the equation equals 0 (etch rates are the same). Isotropic etching also causes undercutting, or in other words, lateral etching under the etch mask. Usually, for semiconductor devices, anisotropic etching is a desirable feature. [16, pp. 283-284] In Figure 3.1, the basic etching profiles are presented.

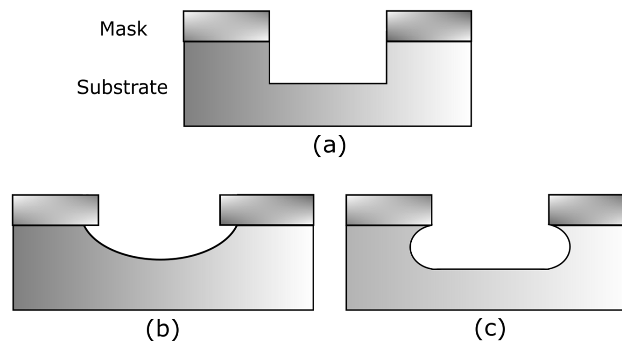


Figure 3.1. *Basic etching profiles (a) anisotropic profile, (b) isotropic profile, and (c) undercut profile. Adapted from [15, p. 320]*

In physical etch, the etch rate depends mainly on the flux and energy of the ion bombardment and, thus, is very low. Although, the direction of ion bombardment is the reason for the anisotropic etch process. [15, p. 331]

3.2.2 Plasma etching

Plasma etching processes use gaseous etchants to chemically or physically react with etched materials [15, p. 330]. A condition where one or multiple gases are held at a certain pressure and submitted to an electrical potential, which causes partial ionization of the gas atoms, is called a plasma state. In plasma, positive ions, radicals and electrons co-exist. [17, p. 1] [15, p. 330] Both electron density and ion density are equal and also referred to as plasma density [3, p. 11].

In plasma, particles can collide due to either change in energy or particle transformation where a neutral particle becomes ionized or vice versa. In a noble gas, for example, argon, discharge, if an electron hits an ion, the electron loses energy. However, if an atom collides with an ion, the energy is exchanged, and a charge can be transferred. [17,

p. 2]. Ion-assisted plasma conditions are needed due to the strong bond strengths in materials, making it harder to choose a suitable mask to avoid, for instance, mask erosion and micro-masking issues. Also, desirable etch rates can be hard to achieve without damaging the patterned surface. [18]

Plasma also has a conductive property because electrons can move freely in there. When RF power is applied to the electrodes, the electric field causes the acceleration of electrons that acquire kinetic energy and then collide with atoms and molecules, which makes more ions and electrons. Eventually, the number of ions and electrons exceeds a threshold level, resulting in a plasma discharge. [3, pp. 11-12]

If the etching is only chemical, chemically reactive free radicals are generated to increase the etch rate of the process [15, p. 330] In addition, plasma etching can be only physical. For instance, the physical part can be sputtering with energetic particles of plasma, which can either remove materials from the surface or break the chemical bonds between atoms on the surface. [15, p. 330]

Usually, plasma etching is both chemical and physical reaction. In that case, it is called RIE [1]. Figure 3.2 shows the basic etching mechanisms. The etch rate can be very high or fairly low for chemical etch, depending on the chosen etch chemistry. In addition, it always has an isotropic profile and good selectivity. For the physical etch process, the etch rate can be low and mainly depends on ion bombardment and flux energy. The selectivity is also usually very poor. However, the etching profile is very anisotropic, which can be the desired characteristic for the etch process. [15, p. 330] One advantage of plasma etching over wet etching is anisotropy [18].

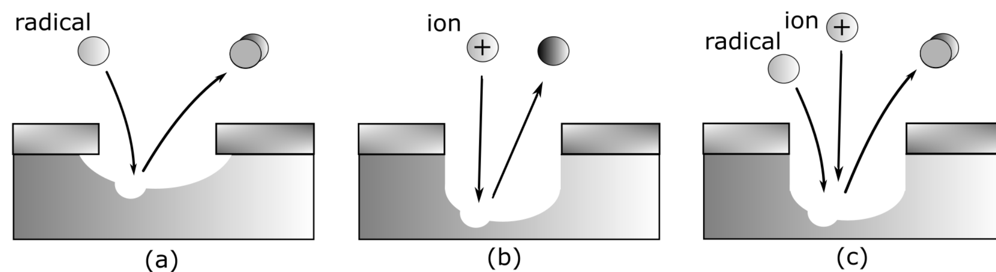


Figure 3.2. *Three etching mechanisms, (a) chemical reaction, (b) physical sputtering, and (c) RIE. Adapted from [1]*

In the plasma etching process, first, reactive species are generated. Then, they are transported and absorbed on the wafer. Then, etching reactions occur on the wafer surface, creating etch byproducts. Then, etch byproducts desorb from the wafer surface. [3, p. 21]

For etchant selection, one important criterion is the volatility of reaction products. To estimate volatility, boiling points of reaction products are needed. [13, p. 133] Another essential consideration is surface reactions and desorption of etch byproducts. The chem-

ical sputtering yield and the vapor pressures of etch byproducts are also important to be compared. [3, p. 27]

3.2.3 Plasma etching effects

One plasma etching effect is called the RIE lag effect, which is a qualification given to the difference in etching depth that results from the feature size. Different opening sizes cause the etch depth to vary in the chosen mask: the etch depth can be much larger in large, open areas than in smaller openings, causing non-uniform etching results. The difference is related to the diffusion processes of etching reactants, and smaller size requires a longer time to be etched. [17, p. 3]

Another plasma etching effect is micro-masking. Micro-masking is usually a non-desired phenomenon that occurs under certain conditions. It happens most frequently when a metal mask is used. In micro-masking, re-deposition of non-volatile particles may be re-deposited to the sample, leaving randomly positioned etched structures, for instance, dispersed nano-pillars. Then physical sputtering of small metal particles may be re-deposited elsewhere on the sample due to being non-volatile. Micro-masking can also be caused by slowly volatile etching products or lithography errors. [17, p. 3]

An effect that describes how the etching depth and etch rate may vary with the total surface area etched is called the loading effect. RIE processes cause the loading effect and can be clarified by the faster depletion of reactants with larger surface areas to be etched. [17, p. 2] Loading effect can be divided into two subsections: macro-loading and micro-loading. In macro-loading, the etch rate of a wafer with a larger open area differs from a wafer with a smaller open area. In micro-loading, smaller holes usually have a lower etch rate for contact and via hole etch processes than larger holes. [15, p. 321] Nevertheless, the effect is also dependent on the chosen chemistry, chamber configuration, and the material forming the lower electrode [17, p. 2].

3.2.4 Damage caused by plasma etching

Plasma-induced damage can be divided into physical damage, contamination by metal components, and electrical damage or charge-up. Physical damage is primarily induced by energetic ion bombardment during etching but also due to plasma surface modification. Contamination on the sample surface can be replicated to the underlying surface and cause damage. Electrical damage relates to the RF electric field, nonuniform plasma, bias voltage, and electron-shading effect. [1, p. 1450]

There can also be some RIE effects, such as surface residues or roughness. Surface residues are related to the chemistry discharge or due to the involatile products formed when etching. Surface roughness is usually related to micro-masking or etching of the

rough overlayer, which replicates the underlayer. These material changes affect the performance of electronic devices. [19, pp. 216-271]

Because the processes use plasma, the LSI devices are susceptible to different kinds of damage due to high energy and charged particles. The damage might lower the LSI yields and reliability. Also, dry etching damage includes the creation of crystal defects and wafer charging. The problems resulting from these damages are, for instance, increased contact resistance due to the damage on the Si surface and gate oxide breakdown caused by wafer charging. [3, p. 73]

For ICP-RIE, the ion energy and density can be decoupled more efficiently than in RIE, so the plasma-induced damage can be more readily controlled. Thus, faster etch rates can be achieved with only low damage. Anisotropy is attained by superimposing RF bias on the wafer. [18]

Because substrate temperature control is also an essential factor during RIE, it must be considered. It can be done indirectly through thermal contact between the lower electrode, which is temperature-controlled, and the sample backside. The electrostatic chuck stays at a specific temperature by a coolant circulating from the chiller. Since the physical contact between the wafer and electrostatic chuck does not ensure enough heat transfer, the space is filled with He gas to promote thermal conduction. [3, pp. 70-71].

4. METHODS AND EQUIPMENT

This section focuses on the principles and equipment used in this thesis, with a specific emphasis on RIE and ICP-RIE reactors. Afterward, the methodology of the study is described.

4.1 Plasma etching reactor

In this Bachelor's thesis, RIE is one of the used equipment to etch a sample. RIE uses chemical and physical components in etching processes which can lead to anisotropic profiles and high etch rates. Plasma is usually generated with RF power applied between two parallel electrodes. The wafer is placed on an electrode where a potential is induced, and ion energies are some hundred electron volts. Anisotropic etching is caused by low pressures, which enables an increased mean free paths and reduces collisional scattering of ions accelerated in the sheath. [20, p. 410] An illustrative picture of the RIE chamber is shown in Figure 4.1.

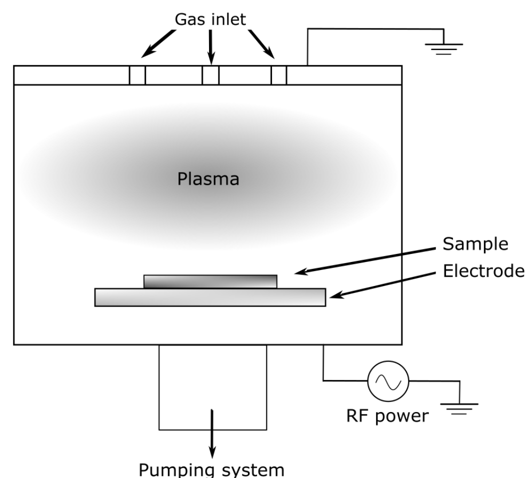
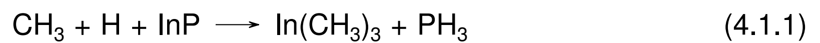


Figure 4.1. *RIE chamber. Adapted from [20]*

When etching with RIE, the etch chamber is first pumped down to a high vacuum. Then, the etching gas is applied, and the plasma can be generated by applying a 13.56 MHz RF power to a pair of electrodes facing each other. The etch gas dissociates in this plasma to form reactive species like radicals and ions. These reactive species are transported to the wafer surface and react with the material to be removed. Then, the underlying

semiconductor wafer is etched through the interaction with radicals. An etching reaction happens, and deposition takes place near the wafer. Then, the byproducts desorb from the sample surface and etching continues. The etch byproducts are eventually removed from the etching chamber. [3, p. 3]

Hydrogen gases, such as methane and ethane, have been used for etching InP with RIE due to the smooth surface morphology and good anisotropy, which can be applied to semiconductor devices [21]. In a CH_4/H_2 plasma discharge, the free radicals to etch InP are CH_3 and H, while the reaction products are $In(CH_3)_3$ and PH_3 that are volatile at room temperature. The reaction is



$$CH_3 + H + InP \longrightarrow In(CH_3)_3 + PH_3 \tag{4.1.1}$$

Although low etch rates are typical for CH_4/H_2 etching chemistry, which causes mask erosion and polymer deposition during long etching processes, which requires repeated cleaning of the chamber walls [22, p. 169] [17, p. 10]. Without a hydrogen supply, the plasma-excited hydrocarbon atoms do not etch InP but react with one another to deposit the polymer film [21]. The polymer formation can be avoided by adding chlorine as one etch gas. It also increases the etch rate of the etching process. Nevertheless, the chlorine reacts with indium to form $InCl_x$, an involatile gas at room temperature. Due to that, the temperature needs to be risen to 200℃ or over. [23]

4.2 Inductively coupled plasma etching reactor

Another etching equipment in this Bachelor's thesis is the ICP-RIE reactor. ICP plasma is formed in a dielectric vessel and surrounded by an inductive coil where RF power is applied. The changing electric field induces a changing magnetic field which focuses the electrons in the center of the chamber and generates a high-density plasma. Since plasma density and ion energy can be decoupled, uniform energy and density distributions can be transferred to the wafer while the ion and electron energies are kept low. [20, p. 411] The bottom electrode, also used as the sample holder, is connected to another RF generator [24]. The magnitude of the ion flux determines the etch rate but not the efficiency of the reaction. The efficiency is more dependent on the ion energy. When comparing two different etching equipment, the efficiency can be the same, but the etch rates might differ. [18] An illustrative figure of ICP-RIE chamber is presented in Figure 4.2.

ICP-RIE discharges occur at lower pressures, and the power coupling is not directed to the lower electrode but through a dielectric window or wall (made of quartz). As a result, there is a low voltage across plasma sheaths at electrodes and walls. For instance, rising ICP power leads to lower DC bias and higher plasma density. For that reason, ICP-

RIE reactors can achieve anisotropic etching at a high rate and do not induce that much damage to the etched surface. [17, p. 2] [20, p. 411] In RIE systems, the etch profiles could result in slanted sidewalls due to plasma being formed only with DC bias [17, p. 3]. Thus, in RIE, it is possible to control the plasma density independently of the DC bias, unlike in RIE, where plasma is formed only with DC bias [17, p. 1].

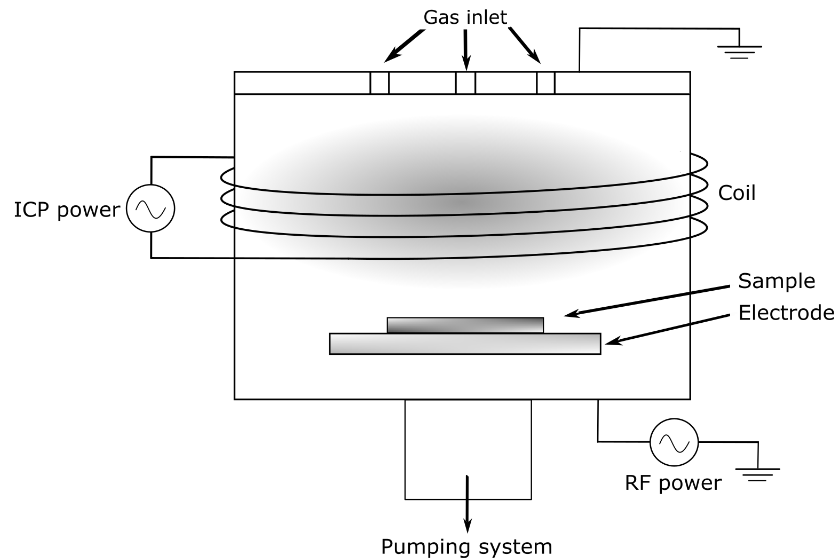


Figure 4.2. *ICP chamber. Adapted from [20]*

4.3 Scanning electron microscopy

To analyze the etch depth and sidewall profile of an etched sample, one efficient method is SEM. It is used to collect structural and chemical composition information. Compared to a conventional light microscope, the light source is replaced with a high-energy electron beam. The imaging resolution can be as small as 1 nm and is mainly limited by the electrons and sample interactions. In addition, high-resolution imaging with a large depth of field can be achieved due to the wavelengths of electrons that can be focused with electromagnetic lenses.

Various signals are formed from the electrons and sample interactions to gain information on materials' morphology, chemical composition, phase, and crystallography. X-rays depend on the atoms so the sample composition can be determined with X-ray spectra. They are secondary electrons (SEs), low-energy electrons which are leaving the sample surface as a result of the primary beam-caused collision sequence; backscattered electrons (BSEs), high-energy electrons that have escaped from the sample surface; and characteristic X-rays that are generated by bringing the excited atoms back to ground state. The image of a specimen under study can be formed by collecting SEs and BSEs. [25, p. 103-104]

4.4 Contact profilometry

A traditional method of inspecting a sample surface's profile and coarse roughness is called contact profilometry. In contact profilometry, a stylus runs over the sample in contact and is moved across the surface. The contact profilometer drags the stylus across a gap and outputs a 2D line profile. The profile is analyzed with statistical methods that produce different surface parameters. Etch depth can be measured by checking the etched pattern's top and bottom from the measured 2D line profile.

The center line average, R_a, the average deviation of the mean line, can be calculated to measure a sample's roughness. Contact profilometer can also be a destructive method, which needs to be considered when planning the measurements. [14] [26]

4.5 Process description

This thesis aimed to optimize InP etching using ICP-RIE equipment. The optimization was done with five 3" InP-based wafers. At first, it was decided to etch one of them with a RIE plasma etching system using $\mathrm{CH_4/H_2}$ etching chemistry and the other four wafers with an ICP-RIE system using $\mathrm{CH_4/H_2/Cl_2}$ etching chemistry. Adding chlorine was due to the slow etch rate of $\mathrm{CH_4/H_2}$ plasma caused by polymerization on the sample surface. Adding chlorine to the etch chemistry removes the polymer from the sample surface, which increases the etch rate and reduces chamber cleaning [4, p. 81].

Each of these five wafers was prepared identically. At first, 100 nm of SiN_x was deposited with Plasma Enhanced Chemical Vapor Deposition (PECVD) as the hard mask. The pattern was generated with RIE after the photolithography steps to the hard mask, and straight lines, ridges, were used as an etching mask. Then, the pattern was transferred to the underlying wafer with etching, RIE for the first one and ICP-RIE for the other four wafers. After the etching step, the rest of the hard mask was removed with buffered oxide etchant (BOE) to measure the etch depths and etch profile with a contact profilometer and SEM.

The profiles of the ridges were studied with SEM imaging, where etch depth, etch depth next to the ridge, ridge top width, ridge bottom width, and ridge angles were measured. The etch depth was measured with a contact profilometer from 5 points across the wafer. Before etching with RIE, the etch recipe was run in an empty chamber. On ICP-RIE, the etch recipe was run to a chamber with only the quartz disk in the chamber each time before the first etching with chosen chemistry. After the etch process, the wafer was removed, and a cleaning process with $\mathrm{O_2}$ was run to an empty chamber for RIE and ICP-RIE with the quartz disk.

The reason to measure two different etch depth values with SEM was to see the difference

between these two etch depths, which is also called footing. The cause of footing might be due to the geometry of ion bombardment in etching, and it may affect the performance of semiconductor devices.

5. RESULTS AND DISCUSSION

In this chapter, the results are presented, starting with etch depths measured with a contact profilometer and SEM. Then, time dependence and repeatability are looked at.

5.1 Etch depth measurements

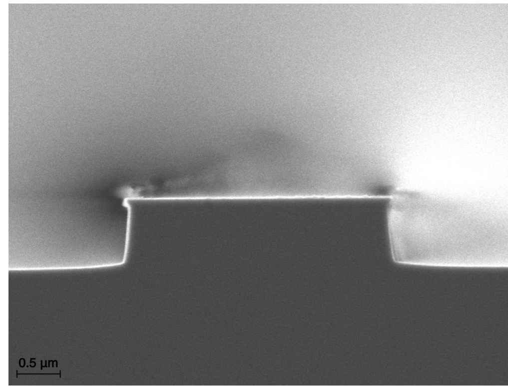
To obtain knowledge of the time dependence on InP-based material etching using ICP-RIE with $CH_4/H_2/Cl_2$ etching chemistry, a total of four wafers were measured. In addition, one wafer was etched using RIE with CH_4/H_2 etching chemistry as a reference. The RIE etching process was 25 minutes, and the ICP-RIE etching processes were 0.5, 1, 1.5 and 2 minutes, respectively.

The profile and etch depths were examined with a contact profilometer and SEM for each wafer. Etch depths next to the ridge were also measured because they are significant for the operation of semiconductor devices. In Table 5.1, average values of etch depth next to the ridge, etching time, footing, which is the difference between etch depth and etch depth next to the ridge, and etch time are presented. Examples of the SEM images of the ridges are presented in Figure 5.1.

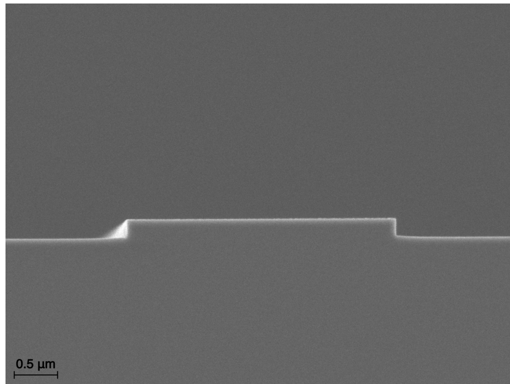
Table 5.1. *Etched sample, etch depth next to the ridge, footing, and etch time of etched samples. Values are an average of the measured ten ridges, and the footing value is calculated as the difference between the etch depth and etch depth next to the ridge.*

Etched sample	Etch depth next to the ridge [nm]	Footing [nm]	Etch time [s]
25 min RIE etch	723.6	42.2	1500
0.5 min ICP etch	191.5	30.5	30
1 min ICP etch	434.9	55.4	60
1.5 min ICP etch	674.8	74.2	90
2 min ICP etch	923	82.9	120

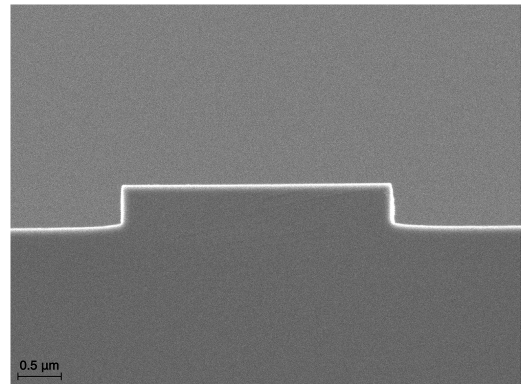
It can be seen from the etch depths next to the ridge that the etch time for the ICP etching processes is much faster compared to the RIE reference. The same etch depth as in the RIE reference lies between 90 s and 120 s. Although, the footing increased when time increased, which was not a desired feature. In 120 s etching, the footing was almost twice



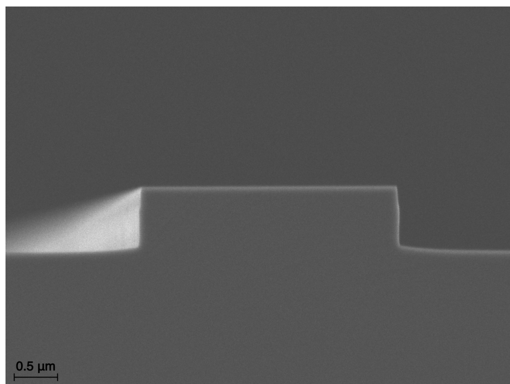
***(a)** RIE reference.*



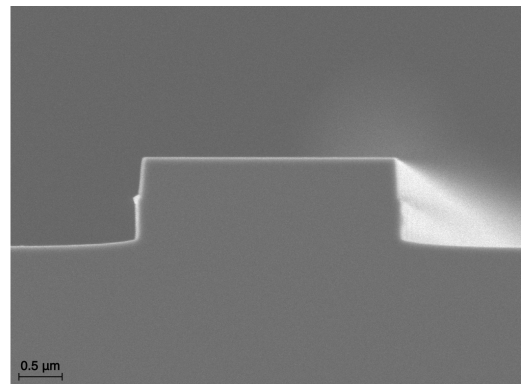
***(b)** 1st ICP etch*



***(c)** 2nd ICP etch*



***(d)** 3rd ICP etch*



***(e)** 4th ICP etch*

***Figure 5.1.** SEM images of the etched samples.*

as much as for the RIE reference. Still, the etching time was much faster with ICP-RIE than with RIE.

When it comes to the profile of the ridges, the wafers etched with ICP-RIE were more anisotropic and smoother. For instance, in RIE reference, the little details caused by undercutting, which in this case means a different etch rate between the contact layer and other layers, were not formed when etching with ICP-RIE. Those details are usually taken off with another process step, which is not needed when etching with ICP-RIE.

5.2 Time dependence

In this chapter, the results of time dependence on etching are presented. Five points were measured with the contact profilometer for each wafer to obtain knowledge about the etch depth around the wafer. The measurement points were as far apart as possible on the wafer. As a function of etching time, the etch depth is plotted in Figure 5.2.

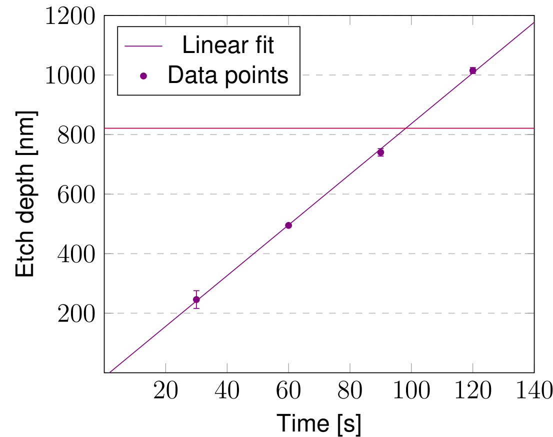


Figure 5.2. *Etch depth as a function of time measured with a contact profilometer. The purple line exemplifies the RIE reference value. The error has been evaluated using standard deviation. The error bars are so small that they are hidden under the markers.*

In Figure 5.2, R^2 value for linear fit was 0.99. It can be seen that the etch rate is constant. The etch rate was about 510 nm/min, which is about 15.5 times faster than with RIE.

A small piece was cleaved for each wafer to image it with SEM. A total of ten points were measured to obtain knowledge about the etch depth next to the ridge and profile. In Figure 5.3, the etch depth next to the ridge, as a function of etching time, is plotted.

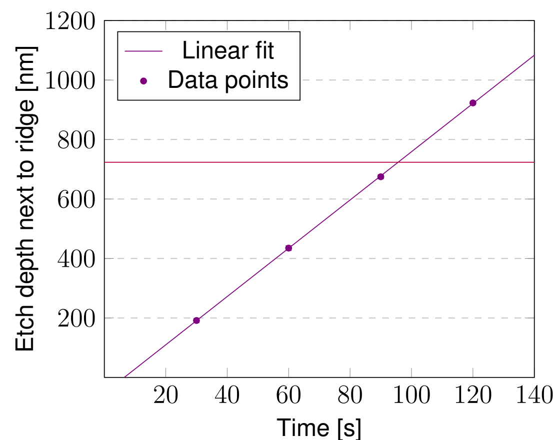


Figure 5.3. *Etch depth next to the ridge as a function of time measured with SEM. The purple line exemplifies the RIE reference value. The error has been evaluated using standard deviation. The error bars are so small that they are hidden under the markers.*

In Figure 5.3, R^2 value for linear fit was 1. It can be seen that the etch rate was nearly

constant with each ICP-RIE process. The etch rate was about 480 nm/min, about 15 times faster than with RIE. The results were surprising because the role of chlorine in the etching was more significant than anticipated. All in all, the etch rate was around 500 nm/min.

Even though the profile was much better compared to RIE, the footing value was observed to be higher in ICP processes. In Figure 5.4, the footing, as a function of etch depth, is plotted.

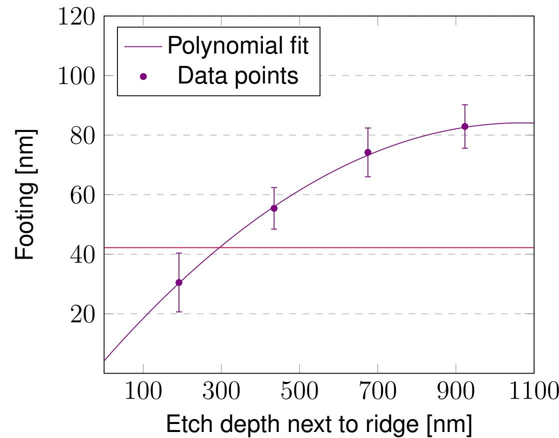


Figure 5.4. *Footing as a function of etch depth next to the ridge. The purple line exemplifies the RIE reference value. The error has been evaluated using standard deviation.*

In Figure 5.4, R^2 the value for the polynomial graph plot was 0.99. It can be seen that the footing increased when the etching time increased and is almost twice as much as for the reference with the same etch depth. The increase in footing might be due to different etch chemistry. The footing might possibly affect the performance of a semiconductor device destructively, so the process parameters might require further optimization to decrease the footing in the future.

5.3 Process reliability

Changing the etch depth between processes was extremely linear: when the etch time rose, the etch depth rose linearly. That was not expected due to the polymer formation on the sample surface. It was chosen to add chlorine to remove the polymer from the sample surface, which might be why the etch rate remained the same when the etching time increased.

There was mask erosion in the top corners of the ridge when the etching time was over a minute. That can be seen from the SEM images of the last two ICP-RIE processes, in which the ridge's shape is curved on the top of the ridge. In the future, a thicker hard mask could be used to achieve a smoother ridge.

Regarding the etch depth measuring equipment, measuring with both SEM and contact

profilometer gave much more reliable results than measuring with one. The standard deviation was smaller with SEM measurements than when measuring the etch depths with a contact profilometer. On the contrary, the accuracy of the SEM measuring tool is only about tens of nanometers per pixel, so the change of one pixel on SEM changes the measured length by up to tens of nanometers. Also, the results from SEM were from a specific location of the wafer. When measuring with the contact profilometer, the measurements can be done all over the wafer, which means that the variation over the wafer can be seen. In addition, the contact profilometer is less prone to human errors because the measurement is done by equipment.

6. CONCLUSIONS

In the semiconductor industry, InP is one of the used materials. Currently, the etching of InP takes a long time, and a shortening of etching time and higher quality are needed. This Bachelor's thesis aimed to transfer CH_4/H_2 etching processes from RIE to the ICP-RIE system. In addition, other aims were to achieve a smoother profile and to decrease the etching time. Five 3" InP-based wafers were etched, one with RIE as a reference and four with ICP-RIE, varying the etching time. Etch depths were measured with a contact profilometer and SEM to compare the etch depths and the etch profiles. The etch depth next to the ridge was also looked at because it is significant for the operation of semiconductor devices.

The etch rate with ICP-RIE was up to 500 nm/min, which is over 15 times faster than when etching with RIE. However, the footing was larger for the etch depth required, and possibly the hard mask ran out from the edges of the pattern during longer ICP etchings, which was caused by mask erosion. Still, the profiles were smoother, and the effect on the top of the ridge, which was caused by undercutting, did not occur in the ICP etching processes.

All in all, the processes were successful, and the etching process can be transferred from RIE to the ICP-RIE system. This way, processing time can be saved, and undercut profiles can be avoided, which will leave the following process steps out and shorten the processing time even more. All four etchings gave a smooth profile. In the future, a thicker hard mask could be tested to see if the same etch depth can be reached so that the mask would not run out. In addition, the process parameters could be optimized to decrease the footing. Also, other InP-based compound semiconductors could be tested to see if they gave similar results.

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