Delta-Sigma Modulator-Embedded Digital Predistortion for 5G Transmitter Linearization

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***Abstract*—This article presents two novel digital predistortion (DPD) based architectures that jointly mitigate the in-phase/quadrature (IQ) modulator impairments and the power amplifier (PA) nonlinear distortion in wireless transmitters. The proposed architectures are multibit cartesian and complex delta-sigma modulator-based joint DPDs, called CDSM-JDPD and CXDSM-JDPD, respectively, which enable using low-cost digital-to-analog converters (DACs) while offering versatile linearization capabilities to combat the coexisting distortions of the PA and the IQ modulator. The proposed approach alleviates the need for reverse modeling and implementation of extra hardware to separately deal with frequency-dependent IQ impairments. Moreover, the CXDSM-JDPD enhances the linearization performance and relaxes the high oversampling ratio (OSR) requirement by quantizing the signal more efficiently. Furthermore, the presented concepts inherently support the use of low-resolution DACs, which offers a tremendous advantage in designing and implementing low-cost and energy-efficient radio transmitters. Extensive set of hardware-in-the-loop RF verification measurements with a commercial PA are provided, including two timely 5G New Radio (NR) scenarios at NR bands n3 and n78, while covering channel bandwidths up to 100 MHz and varying the OSR and the DAC bit resolution. The obtained results demonstrate the excellent linearization capabilities of the proposed solutions and their superiority compared to other DSM-based DPD approaches.**

***Index Terms*—5G New Radio, delta-sigma modulator, digital predistortion, IQ imbalance, linearization, nonlinear distortion, power amplifier, quadrature modulator, wireless transmitter**

I. Introduction

THE wireless communication systems are continuously advancing to support ever-increasing numbers of users and wide variety of high-quality services. These advances require more and more complex signal modulation and access techniques such as orthogonal frequency division multiplexing (OFDM) that provide higher spectral efficiency and robustness over broadband propagation channels. However, the new digitally modulated signals have a strongly dynamic envelope with high peak-to-average power ratio (PAPR) [1], [2]. Under these conditions, the power amplifier (PA) of the transmitter is highly constrained to operate within a complex tradeoff between power efficiency and linearity. Traditionally, this constraint leads to over-dimensioning the PA with respect to the required output power so that it operates in its linear region with a high input back-off (IBO) resulting in poor energy-efficiency [3]–[6].

To overcome such trade-off, applying a linearization technique to the PA presents a very interesting solution that enables the PA to be employed as close as possible to its saturation region which increases its efficiency while maintaining a relatively linear behavior [7]–[9]. Digital predistortion (DPD) has emerged as the most preferred technique for PA linearization due its flexibility and efficiency gained from the technical advances of digital electronics [1], [2]. Digital predistortion consists of preceding the PA with a predistorter whose nonlinear function is ideally the inverse of that of the PA. Thus, the cascading of the predistorter and the PA leads to a linearized amplification system [2], [5], [8]–[18]. However, several difficulties, such as complexity, numerical stability, convergence problems or the coexistence of multiple RF impairments can arise which challenge the extraction and the inversion of the PA model.

A relatively simple yet effective DPD technique based on a mixture of a delta-sigma modulator (DSM) [19]–[22] and a linearization module has been introduced in [23], [24]. This solution consists on inserting a PA behavioral forward model in the feedback loop of a multibit DSM in a way that the resulting closed-loop transfer function of the system is the inverse model of the PA. This approach allows using directly the forward model without the need for the reverse model identification, which improves the system robustness compared to conventional DPD solutions. DSMs have previously been introduced in RF transmitters/receivers thanks to their advantages in terms of resolution and noise shaping capabilities [19]–[22].

However, these existing architectures still have a severe limitation. Specifically, none of the DSM-based linearizers published so far take into account the signal distortion due to the impairments of the IQ modulator [25]–[29]. Indeed, direct conversion principle is commonly used to reduce the circuit complexity and cost of the transmitter, but these systems are sensitive to the imbalance between the I and Q branches which is unavoidable in any practical implementation. The IQ impairment can severely compromise the performance of the DPD and make the predistorted signal totally inaccurate by biasing the estimated coefficients. The effects of this

This work was supported by the Academy of Finland under the grants #319994, #338224, and #332361, and by the Finnish Funding Agency for Innovation under the ENTRY-100GHz project.

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type of impairments become more severe in multiple-input multiple-output (MIMO) systems as each channel has its own independent IQ imbalance. In the case of conventional DPD architectures, different methods have been applied to compensate for the IQ modulator impairments and thus to achieve a better linearization performance [25]–[29]. However, significant extra hardware might be required due to the separate processing of the PA and the IQ modulator impairments. An effective method has been published in [30], [31], presenting an enhanced IQ memory polynomial model (EIQMPM) that can predict simultaneously the behavior of the PA and the imperfections of the IQ modulator. Consequently, the usage of this model in the conventional DPD has led to a robust linearization even in the presence of input signal IQ impairments. However, none of the existing methods has been used in the DSM-based predistorters.

Another issue that system designers can face is the constraints of the digital-to-analog converter (DAC) that converts back the digital signal to the analog form. In fact, the DAC needs to provide high precision with low noise level. The high performance of the DAC keeps the noise at minimum levels and maintain the accuracy of the predistorted signal. Therefore, high-resolution DACs are commonly employed to ensure the required signal quality. However, the trend of designing low-cost and energy-efficient yet flexible radio transceivers makes the use of high-resolution DACs not very practical as they are more complex, costly, and power-hungry. In MIMO systems, the total power consumption would be even higher when using high resolution DACs since multiple transmission chains are used.

In this article, we propose two new multibit DSM-based joint DPD (DSM-JDPD) architectures able to simultaneously compensate for the dynamic nonlinear behavior of the PA and the IQ impairments caused by the IQ modulator. They also inherently support the use of low-resolution DACs while maintaining the desired performance. The first architecture is a multibit joint digital predistorter that uses a conventional cartesian DSM (CDSM-JDPD) with real quantizers. In the second architecture, the first one is further enhanced by introducing a new multibit complex DSM-JDPD (CXDSM-JDPD). The latter employs the concept of complex DSM (CXDSM) that exhibits higher efficiency and reduced quantization noise level, and relaxes the oversampling ratio (OSR) requirements [32], [33]. In this modified version, we are able to improve the linearization performance by reducing the quantization error produced by the quantizer. The proposed architectures are based on inserting an EIQMPM in the DSM's feedback path to create the inverse nonlinearity of the PA even in the presence of IQ impairments arising from the IQ modulator stage, thus offering a more robust and effective system to be used in wireless communications. The proposed topologies perform the PA linearization without the need of reverse modeling and the associated problems as the nonlinearity is intrinsically inverted by the feedback loop of the circuit, leading to lower complexity and increased robustness. Moreover, there is no need for additional circuits or complexity to compensate the effect of the IQ impairments. Beside the compensation of the PA and IQ modulator impairments, the proposed topologies

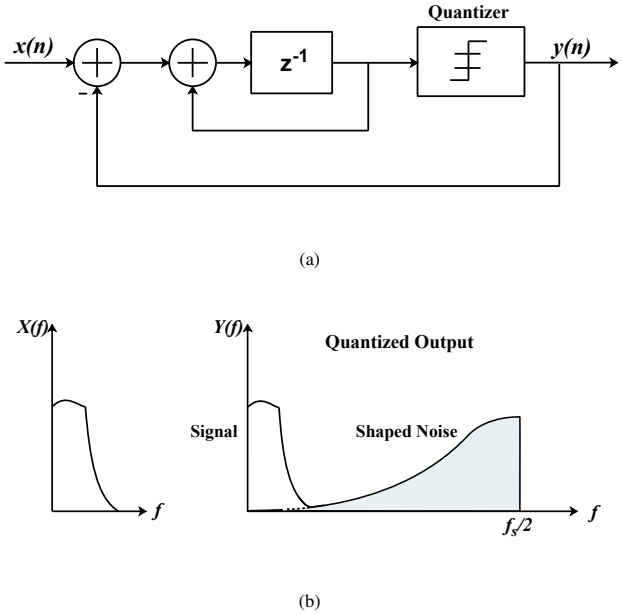


Fig. 1. Principle of a typical first-order DSM. (a) Block diagram. (b) Typical signal spectrum before and after a DSM.

re-quantize the input signal to a shorter word length and shape the resulting quantization noise before the digital to analog conversion, which enables using low- or medium-resolution DACs while maintaining the desired linearization performance. In this article, the proposed concepts are defined and theoretically studied while are also supported by extensive RF measurement results in 5G New Radio (NR) context with true hardware-in-the-loop experiments. Overall, the proposed architectures stand as promising solutions for flexible, programmable, digitally-intensive radio transmitters in the existing and emerging networks, particularly 5G and beyond.

The rest of this article is organized as follows. Section II describes the utilization of the DSM as a nonlinearity inverter. In Section III, the employed PA forward model is presented and elaborated. In Section IV, the proposed DSM-based linearization concepts and architectures are described and detailed. Section V presents the experimental validation and performance assessment of the proposed DPDs through extensive 5G RF measurements. Finally, conclusions are provided in Section VI.

II. Using a Delta-Sigma Modulator for Nonlinearity Inversion

A. Delta-Sigma Modulators

Fig. 1(a) shows the simplified diagram of a first-order DSM. It comprises a direct path containing an integrator followed by a quantizer; and a feedback path. The concept of the DSM consists of quantizing the input signal to a certain number of levels and shaping the quantization noise produced by the quantizer outside the band of interest. The input signal is oversampled at a sampling frequency f_s in order to reduce

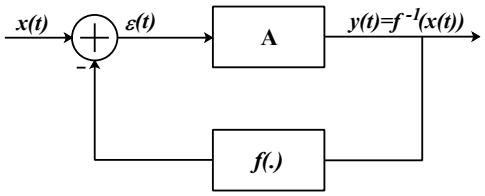


Fig. 2. Nonlinearity inversion concept using the feedback technique.

the in-band noise by distributing it over a wider range of frequencies. The OSR is defined as follows:

$$\text{OSR} = \frac{f_s}{2f_B} \tag{1}$$

where f_s is the sampling frequency and f_B is the maximum frequency component of the signal. The order of the DSM can be increased in order to achieve a better performance and relax the constraint on the OSR value. However, the higher the order, the more the system is vulnerable to instability issues.

In order to evaluate the performance of a DSM, two common figures of merit can be used: the signal to noise and distortion power ratio (SNDR), and the coding efficiency (CE). The SNDR is used to evaluate the linearity of the DSM, and it is defined as the ratio between the in-band signal power and the in-band noise and distortion power expressed as:

$$\text{SNDR} = 10\log_{10}\left(\frac{\text{In-band signal power}}{\text{In-band noise and distortion power}}\right) \tag{2}$$

The CE is the ratio of the desired signal power to the total power, which is the sum of the signal power and the out-of-band quantization noise. It can be defined as follows:

$$\text{CE}\% = \frac{\text{Signal power}}{\text{Signal power} + \text{Quantization noise power}} \times 100 \tag{3}$$

B. Delta-Sigma Modulator as a Nonlinearity Inverter

In the proposed DPD systems, the DSM is employed to invert the PA nonlinearity by placing its *forward model* in the DSM *feedback loop*. Fig. 2 depicts a typical simplified diagram of a closed-loop system, where A is the forward gain and $f(\cdot)$ is a nonlinear function. If we consider, for a stable system, that the feedback and forward gains are sufficiently high, we can assume that the error $\varepsilon(t)$ is much smaller than the input $x(t)$, the output $y(t)$ and $f(y(t))$. Thus, $x(t)$ would be approximately equal to $f(y(t))$, and consequently $y(t)$ would be approximately equal to $f^{-1}(x(t))$. The higher the A is, the more accurate the approximations are, which keeps the feedback system stable. This familiar property of the inversion concept of closed-loop systems is exploited in the DSM, where the function $f(\cdot)$ is tailored towards a PA forward model so that the feedback of the DSM integrates the nonlinear behavior of the PA. It is worth mentioning that $f(\cdot)$ is a general nonlinear expression used here for the purpose of notational simplicity. A different model with memory characteristics will be used in the following sections when actual PA inversion is pursued.

III. Enhanced IQ Memory Polynomial Model

A. Basic Memory Polynomial Model

The memory polynomial model (MPM) is a simplified version of the Volterra-series model which has established itself as one of the most widely used models for both PA behavioral modeling and predistortion [1]–[3], [34]. MPM is an effective way to predict PAs' behavior including nonlinearity and memory effects. Its well-known formulation is given as follows:

$$y(n) = \sum_{k=1}^{K}\sum_{m=0}^{M} a_{k,m}x(n-m)|x(n-m)|^{k-1} \tag{4}$$

where $x(n)$ and $y(n)$ are the complex envelopes of the input and output signals, respectively; K represents the nonlinearity order; M stands for the memory depth; and $a_{k,m}$ are the complex coefficients of the model. The basic MPM serves as a well-known reference method.

B. Enhanced IQ Memory Polynomial Model

MPM was used in the DSM context in [24] and it showed better performance compared to the previous DSM linearizers in terms of signal bandwidth. However, in a real direct-conversion transmitter, the PA will be driven by a signal distorted by the impairments of the IQ modulator. This presents one of the major difficulties in the predistortion process that all the published DSM-based predistorters fail to cope with, which degrades significantly the quality of the transmitted signal. The model used in the proposed DPDs is defined directly in the IQ domain allowing the possibility to handle jointly the IQ imbalance and the PA nonlinearity and memory effects. By using this enhanced model in the DSM-based digital predistorter, the total distortion will be compensated at the PA output. To this end, the expression of the EIQMPM reads

$$\begin{aligned} y(n) = &\sum_{\substack{k=2\\ k\ \text{even}}}^{K}\sum_{m=0}^{M} b_{k,m}x(n-m)\,|x(n-m)|^{k-1} \\ &+ \sum_{k=0}^{K}\sum_{t=0}^{k}\sum_{m=0}^{M} c_{k,t,m}{x_I}^{k-t}(n-m)\,{x_Q}^{t}(n-m) \end{aligned} \tag{5}$$

where $x_I(n)$ and $x_Q(n)$ are the real and imaginary parts of the complex envelope of the input signal $x(n)$, respectively; $b_{k,m}$ and $c_{k,t,m}$ are the complex coefficients; K represents the nonlinearity order; and M is the memory depth.

Let us next define

$$\phi_k(x) = x\,|x|^{k-1} \tag{6}$$

and

$$\gamma_{k,t}(x) = x_I^{k-t}x_Q^t \tag{7}$$

Equation (5) then becomes

$$\begin{aligned} y(n) = &\sum_{\substack{k=2\\ k\ \text{even}}}^{K}\sum_{m=0}^{M} b_{k,m}\phi_k(x(n-m)) \\ &+ \sum_{k=0}^{K}\sum_{t=0}^{k}\sum_{m=0}^{M} c_{k,t,m}\gamma_{k,t}(x(n-m)) \end{aligned} \tag{8}$$

Given the PA input and output measurements, the coefficients $b_{k,m}$ and $c_{k,t,m}$ can be estimated. First, we define the $N\times 1$ input and output data vectors $\mathbf{x} = [x(n),\ x(n-1),\ \ldots,\ x(n-N+1)]^T$, and $\mathbf{y} = [y(n),\ y(n-1),\ \ldots,\ y(n-N+1)]^T$, respectively. The parameters of this model are defined by the $L_b\times 1$ vector $\mathbf{b} = [b_{2,0},\ b_{4,0},\ \ldots,\ b_{K_b,0},\ b_{2,1},\ \ldots,\ b_{K_b,M}]^T$ and the $L_c\times 1$ vector $\mathbf{c} = [c_{0,0,0},\ c_{1,0,0},\ \ldots,\ c_{K,K,0},\ c_{0,0,1},\ \ldots,\ c_{K,K,M}]^T$, where

$$K_b = \begin{cases} K, & K \text{ even} \\ K-1, & K \text{ odd} \end{cases} \tag{9}$$

$$L_b = \left\lfloor \frac{K}{2} \right\rfloor (M+1) = \frac{K_b}{2}(M+1) \tag{10}$$

$$L_c = \left(\sum_{i=1}^{K+1} i \right)(M+1) = \frac{1}{2}(K+1)(K+2)(M+1) \tag{11}$$

In the identification procedure, we consider the $L_h\times 1$ total parameter vector $\mathbf{h} = [h_1,\ h_2,\ \ldots,\ h_{L_h}]^T = \begin{bmatrix}\mathbf{b}^{\mathrm{T}} & \mathbf{c}^{\mathrm{T}}\end{bmatrix}^{\mathrm{T}}$, where $L_h = L_b + L_c$. Next, we define the $N\times L_b$ matrix

$$\mathbf{\Phi} = \begin{bmatrix} \boldsymbol{\phi}_{\mathbf{k}}(x(n)) & \boldsymbol{\phi}_{\mathbf{k}}(x(n-1)) & \cdots & \boldsymbol{\phi}_{\mathbf{k}}(x(n-M)) \\ \boldsymbol{\phi}_{\mathbf{k}}(x(n-1)) & \boldsymbol{\phi}_{\mathbf{k}}(x(n-2)) & \cdots & \boldsymbol{\phi}_{\mathbf{k}}(x(n-M-1)) \\ \vdots & \vdots & \ddots & \vdots \\ \boldsymbol{\phi}_{\mathbf{k}}(x(n-N+1)) & \boldsymbol{\phi}_{\mathbf{k}}(x(n-N)) & \cdots & \boldsymbol{\phi}_{\mathbf{k}}(x(n-M-N+1)) \end{bmatrix} \tag{12}$$

and the $N\times L_c$ matrix

$$\mathbf{\Gamma} = \begin{bmatrix} \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n)) & \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-1)) & \cdots & \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-M)) \\ \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-1)) & \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-2)) & \cdots & \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-M-1)) \\ \vdots & \vdots & \ddots & \vdots \\ \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-N+1)) & \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-N)) & \cdots & \boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x(n-M-N+1)) \end{bmatrix} \tag{13}$$

where

$$\boldsymbol{\phi}_{\mathbf{k}}(x) = \left[x|x|^1,\ x|x|^3,\ \ldots,\ x|x|^{K_b-1} \right] \tag{14}$$

$$\boldsymbol{\gamma}_{\mathbf{k},\mathbf{t}}(x) = \left[x_I^0 x_Q^0,\ x_I^1 x_Q^0,\ x_I^0 x_Q^1,\ \ldots,\ x_I^0 x_Q^K \right] \tag{15}$$

By considering then the $N\times L_h$ composite data matrix $\mathbf{\Psi} = \begin{bmatrix}\mathbf{\Phi} & \mathbf{\Gamma}\end{bmatrix}$, we can now rewrite (5) as

$$\mathbf{y} = \mathbf{\Psi}\mathbf{h} \tag{16}$$

The least-squares (LS) solution for $\mathbf{h}$ reads then

$$\mathbf{h}_{\mathrm{LS}} = \left(\mathbf{\Psi}^H\mathbf{\Psi}\right)^{-1}\mathbf{\Psi}^H\mathbf{y} \tag{17}$$

where $\left(\mathbf{\Psi}^H\mathbf{\Psi}\right)^{-1}\mathbf{\Psi}^H$ is the Moore-Penrose pseudo inverse of $\mathbf{\Psi}$ and $\mathbf{\Psi}^H$ is its Hermitian transpose.

IV. Proposed DSM-based Joint Digital Predistortion Architectures

In this section, the actual joint DPD schemes are presented. It is generally important to determine the expressions of the system in order to have an in-depth knowledge of the operations which are performed by the proposed linearization systems. We thus start by describing and further analyzing a second-order DSM system with EIQMPM in the feedback path, while then present the actual corresponding CDSM-JDPD and CXDSM-JDPD architectures.

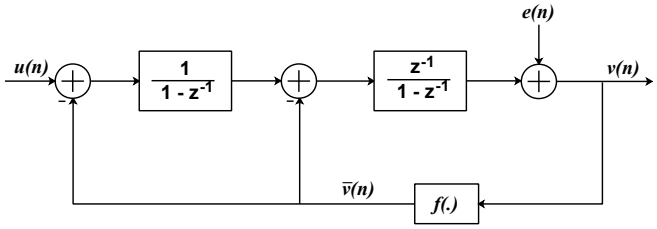


Fig. 3. Discrete-time equivalent block diagram of a second-order DSM-based DPD.

A. Second-Order DSM-Based DPD Using the EIQMPM

Fig. 3 shows the discrete-time block diagram of a second-order DSM with a nonlinear function in its feedback. This architecture uses two integrators, which means the integration is done twice instead of once. The quantizer is assumed to introduce additive white noise, which means its output is the sum of its input and the error signal, $e(n)$. The nonlinear function in the feedback path, $f(.)$, represents the EIQMPM described in the previous section. The input of the system is $u(n)$; $v(n)$ is its output; and $\bar{v}(n)$ is the output of the nonlinear function. We consider $G(z) = 1 - z^{-1}$ and $D(z) = z^{-1}$, where z^{-1} represents the unit backward shift operator. Then the system in Fig. 3 can be described as

$$v(n) = \frac{D(z)}{G(z)}\left[\frac{1}{G(z)}u(n) - \left(\frac{1}{G(z)}+1\right)\bar{v}(n)\right] + e(n) \tag{18}$$

or equivalently, as

$$\begin{aligned}(G(z))^2 v(n) = D(z)\ u(n) - [D(z) + D(z)G(z)]\,\bar{v}(n) \\ + (G(z))^2 e(n)\end{aligned} \tag{19}$$

Stemming from above, we can write

$$\begin{aligned}v(n) = \left[1 - (G(z))^2\right] v(n) + D(z)\ u(n) \\ - [D(z) + D(z)G(z)]\,\bar{v}(n) + (G(z))^2 e(n)\end{aligned} \tag{20}$$

Therefore, by using the properties of the shift operator, we eventually get

$$\begin{aligned}v(n) = 2v(n-1) - v(n-2) + u(n-1) - 2\bar{v}(n-1) \\ + \bar{v}(n-2) + e(n) - 2e(n-1) + e(n-2)\end{aligned} \tag{21}$$

The expression in (21) shows that the output signal $v(n)$ depends on the delayed but unchanged input, the previous two output samples, the previous two output terms affected by the nonlinearity of $f(.)$, and the noise term that depends on the previous two errors – not just only on the previous error – which is the reason of using the double integration in order to lower the in-band quantization noise in the DSM concept. If we assume that the feedback loop of the system is linear, then $2v(n-1) = 2\bar{v}(n-1)$, and $v(n-2) = \bar{v}(n-2)$. Therefore, the expression (21) leads to a typical difference equation of a conventional second-order DSM, that is

$$v(n) = u(n-1) + e(n) - 2e(n-1) + e(n-2) \tag{22}$$

Next, by considering the EIQMPM, the expression of the nonlinear function output reads

$$\begin{aligned}\bar{v}(n) &= f(v(n)) \\ &= b_{2,0}\phi_2(v(n)) + \ldots + b_{K_b,0}\phi_{K_b}(v(n)) + \ldots \\ &+ b_{K_b,M}\phi_{K_b}(v(n-M)) + c_{0,0,0}\gamma_{0,0}(v(n)) + \ldots \\ &+ c_{K,K,0}\gamma_{K,K}(v(n)) + \ldots + c_{K,K,M}\gamma_{K,K}(v(n-M))\end{aligned} \tag{23}$$

Noting that $\bar{v}(n-1) = f(v(n-1))$ and $\bar{v}(n-2) = f(v(n-2))$, the expression of the overall system is thus

$$\begin{aligned}v(n) &= 2v(n-1) - v(n-2) + u(n-1) - 2f(v(n-1)) \\ &+ f(v(n-2)) + e(n) - 2e(n-1) + e(n-2) \\ &= 2v(n-1) - v(n-2) + u(n-1) \\ &- 2\sum_{\substack{k=2 \\ k \text{ even}}}^{K}\sum_{m=0}^{M} b_{k,m}\phi_k(v(n-m-1)) \\ &- 2\sum_{k=0}^{K}\sum_{t=0}^{k}\sum_{m=0}^{M} c_{k,t,m}\gamma_{k,t}(v(n-m-1)) \\ &+ \sum_{\substack{k=2 \\ k \text{ even}}}^{K}\sum_{m=0}^{M} b_{k,m}\phi_k(v(n-m-2)) \\ &+ \sum_{k=0}^{K}\sum_{t=0}^{k}\sum_{m=0}^{M} c_{k,t,m}\gamma_{k,t}(v(n-m-2)) \\ &+ e(n) - 2e(n-1) + e(n-2)\end{aligned} \tag{24}$$

Considering the $1\times L_b$ vector $\boldsymbol{\phi}(v(n)) = [\boldsymbol{\phi}_{\mathbf{k}}(v(n)),\ \boldsymbol{\phi}_{\mathbf{k}}(v(n-1)),\ \ldots,\ \boldsymbol{\phi}_{\mathbf{k}}(v(n-M))]$, the $1\times L_c$ vector $\boldsymbol{\gamma}(v(n)) = [\boldsymbol{\gamma}_{\mathbf{k,t}}(v(n)),\ \boldsymbol{\gamma}_{\mathbf{k,t}}(v(n-1)),\ \ldots,\ \boldsymbol{\gamma}_{\mathbf{k,t}}(v(n-M))]$, and the $1\times L_h$ vector $\boldsymbol{\psi}(v(n)) = \begin{bmatrix}\boldsymbol{\phi}(v(n)) & \boldsymbol{\gamma}(v(n))\end{bmatrix}$, the system output can be expressed also as

$$\begin{aligned}v(n) &= 2v(n-1) - v(n-2) + u(n-1) - 2\boldsymbol{\phi}(v(n-1))\,\mathbf{b} \\ &- 2\boldsymbol{\gamma}(v(n-1))\,\mathbf{c} + \boldsymbol{\phi}(v(n-2))\,\mathbf{b} + \boldsymbol{\gamma}(v(n-2))\,\mathbf{c} \\ &+ e(n) - 2e(n-1) + e(n-2) \\ &= 2v(n-1) - v(n-2) + u(n-1) - 2\boldsymbol{\psi}(v(n-1))\,\mathbf{h} \\ &+ \boldsymbol{\psi}(v(n-2))\,\mathbf{h} + e(n) - 2e(n-1) + e(n-2)\end{aligned} \tag{25}$$

B. Proposed Cartesian DSM-Based Joint Digital Predistorter

The overall concept and architecture of the proposed CDSM-JDPD is described in the block diagram of Fig. 4. The architecture includes a multi-bit DSM with an EIQMPM and a gain/phase adjustment block in its feedback path. To this end, the block A in Fig. 2 is replaced by a CDSM with a multi-bit real quantizer, and the EIQMPM is adopted in the feedback path.

Additionally, in order to obtain the optimal DPD performance, a gain and phase adjustment block is added to the system. This block helps to control the gain level and phase in the feedback when needed. To avoid any stability issues, gain normalization and phase alignment are essential. In fact, during PA modeling, a phase offset could appear in the captured data. Such phase offset should be subtracted in order to capture the phase excursions that represent the PA's phase distortion properly. This phase offset can be tracked by simply averaging all phase responses of the PA. It is worth mentioning that including the phase distortion in the modulator's feedback will not cause issues for the proposed system as long as the phase offset is eliminated. In addition, in a second-order DSM, the input signal level should be smaller than the feedback level. Specifically, the boundary of the input needs to be limited to 0.7 times the feedback level in order to prevent saturation in the integrators and system instability [19].

In general, it is noted that although second-order topologies are employed in this work for the nonlinearity inversion, higher orders can be used to relax further the OSR factor. However, the DSM will also be more vulnerable to saturation and stability issues [23]. Therefore, higher order architectures are left for future work and investigations.

C. Proposed Complex DSM-based Joint Digital Predistorter

In order to further improve the DSM-based predistortion capabilities, we next propose and formulate a new multi-level complex DSM-based joint digital predistorter. The CXDSM-JDPD uses a complex DSM as it allows having better performance in terms of overall efficiency by decreasing the power level of the generated quantization noise [32], [33].

The CXDSM is based on processing the input signal directly using only one DSM with a complex polar quantizer instead of employing two DSMs for the decomposed I and Q components of the signal. In this approach, all the building blocks of the CXDSM need to be designed to handle complex data. The used quantizer allows mapping the amplitude and phase of its input envelop signal to N_r and N_θ different quantization levels, respectively. The complex polar quantizer maps the data more efficiently, and in the context of DPD, this is expected to offer better linearization accuracy.

To shortly analyze and illustrate the effect of N_r and N_θ on the SNDR and CE, a second-order CXDSM with an OSR of 16 was designed and tested using different values of N_r and N_θ. It is worth mentioning that by changing the number of phase quantization levels, the magnitude quantization thresholds ρ_i should be adjusted to optimum levels, i.e., when N_θ is high, the magnitude quantization thresholds are reduced. In this study, the values of the magnitude thresholds were swept for each case of N_θ, and the lowest values that do not saturate the modulator are considered. Moreover, the values of ρ_i are a function of the statistical characteristics of the signal and therefore should be different from one signal to another.

Fig. 5(a) shows the SNDR versus N_r for the cases of N_θ = 8, 16, 32 and 64; while Fig. 5(b) shows the CE versus N_r for the same cases. The SNDR and CE versus N_θ are presented in Fig. 5(c) and Fig. 5(d), respectively, for the cases of N_r = 8, 16, 32, and 64. The performance of the CXDSM is improved by increasing the phase and amplitude quantization levels. It is noteworthy that N_r and N_θ can be different. However, in this work, we are going to use the same quantization levels for both amplitude and phase.

The overall architecture of the proposed CXDSM-JDPD is presented in Fig. 6. Compared to the CDSM-JDPD, this archi-

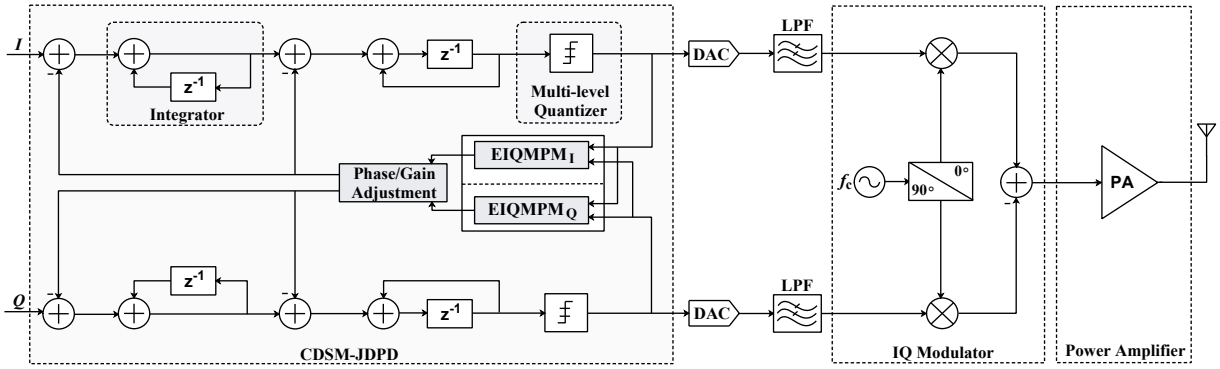


Fig. 4. Proposed multi-bit CDSM-JDPD architecture.

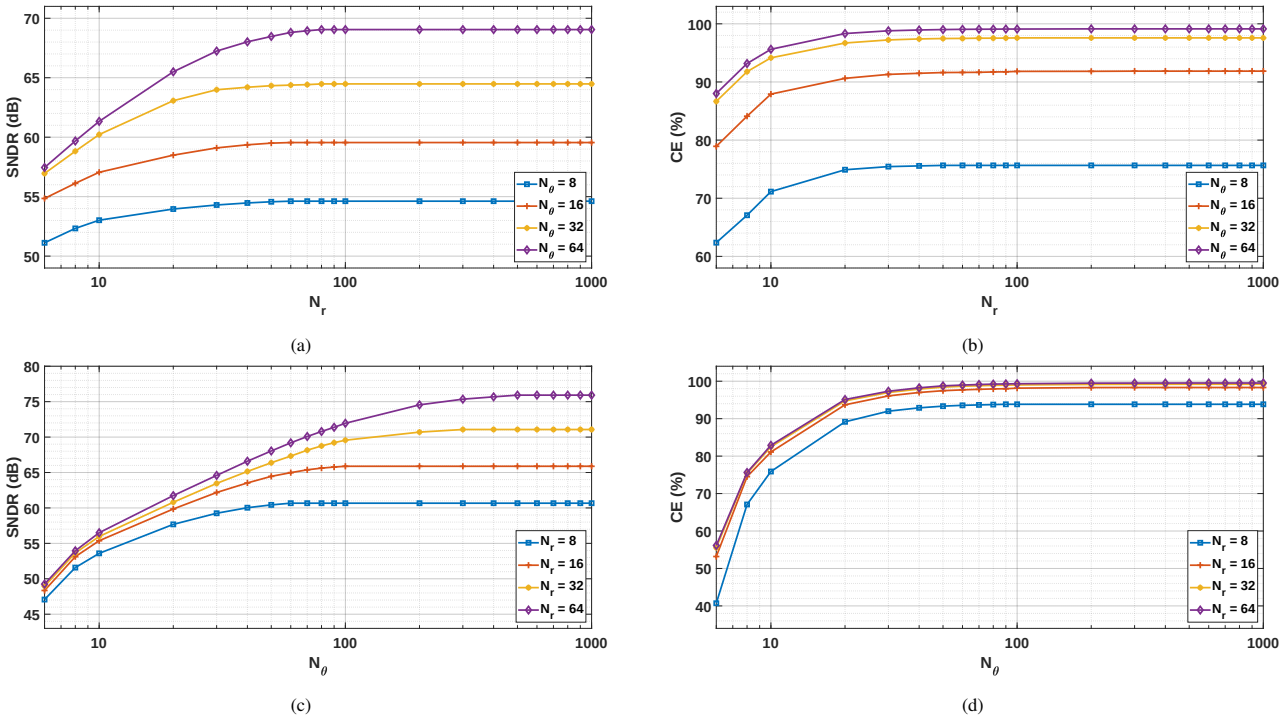


Fig. 5. Effect of the magnitude and phase quantization levels on the performance of the CXDSM. (a) $SNDR\ (dB)$ versus N_r. (b) $CE\ (\%)$ versus N_r. (c) $SNDR\ (dB)$ versus N_θ. (d) $CE\ (\%)$ versus N_θ.

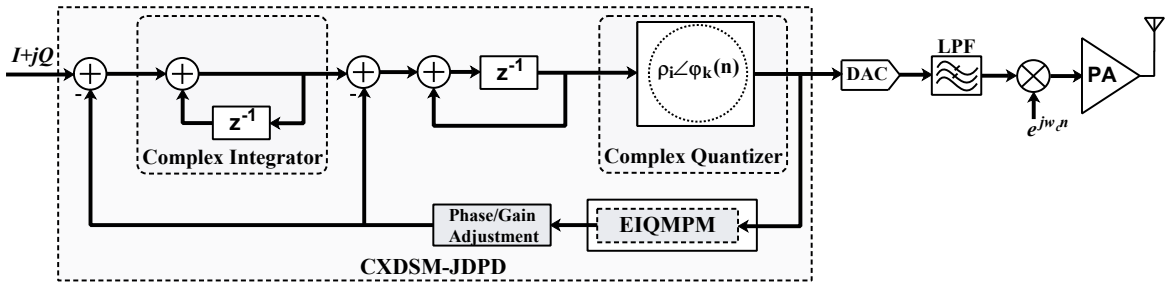


Fig. 6. Proposed multi-bit CXDSM-JDPD architecture.

tecture consists of one CXDSM, where the signal's quadrature components are processed as complex data. The EIQMPM is then integrated into the complex feedback loop of the CXDSM in order to obtain the inverted model at the output.

D. Overall Transmitter System with Low- or Medium-Resolution DAC

The overall transmitter systems with low- or medium-resolution DACs are high-lighted and summarized in Fig. 7. Specifically, Fig. 7(a) shows a classical transmitter system with separate DPD and IQ imbalance correction modules, while Fig. 7(b) illustrates the proposed approach. In general, the DAC nonlinearity and the word-length of the digital input are mutually proportional. In addition, the power consumption of DACs increases significantly with the increase in the number of bits. On the other hand, using a low-resolution DAC preceded by a standalone quantizer alone leads to a high level of generated noise. A solution is to precede the DAC with an oversampled DSM in order to reduce the word-length in an effective manner. The DSM not only re-quantizes the digital input but also spectrally shapes the resulting quantization noise.

In our overall transmitter system, this approach motivates us not only to use the DSM as a digital-to-digital converter, but also as a DPD and IQ impairments compensator as described above. Consequently, and considering the fact that our transmitters eliminate the need for reverse modeling and additional IQ impairments compensation circuits, the overall system would be less complex than conventional systems that require separate processing for each RF impairment.

V. Experimental Evaluation of The Proposed Architectures

In order to validate and evaluate the proposed concepts, three separate linearization experiments are carried out in 5G NR context. The first two experiments are intended to the 5G NR Band n3 (1805-1880 MHz), where the carrier frequency is centered at 1.85 GHz. The third experiment is related to the 5G NR Band n78 (3300-3800 MHz) with a carrier frequency centered at 3.5 GHz. Additionally, two different scenarios are considered. The *first scenario* is for the compensation of the PA nonlinearity and memory effect assuming no IQ impairments. The *second scenario* is for the compensation of PA distortion in the presence of a non-ideal IQ modulator leading to a co-existing IQ imbalance of 5% and 10 degrees in amplitude and phase, respectively.

In all the experiments, we utilize 5G NR Release-15 standard-compliant OFDM waveforms. The PAPR of the generated waveforms is limited to 8.0 dB through the iterative clipping and filtering (ICF) processing technique, and the inherent OFDM signal sidelobes are suppressed via additional time-domain windowing.

A. RF Measurement Setup

The RF measurement setup is presented in Fig. 8. The device under test (DUT) is a general-purpose PA (Mini-Circuits ZHL-4240) that has a frequency range of 700-4200 MHz and a gain of 40 dB. To perform the RF IQ modulation and demodulation, we utilize a National Instrument PXIe-5840 vector signal transceiver (VST) that includes a vector signal generator (VSG) and a vector signal analyzer (VSA). The VST has a frequency range from 9 kHz to 6 GHz and 1 GHz of instantaneous bandwidth. The VST includes an additional host processing-based computing environment that performs digital waveform generation and executes the system's functions and it is embedded through an NI PXIe-8880 controller. The low-resolution DACs are implemented in the host processing environment, with different effective bit resolutions.

The digital waveforms are generated in the host processor. Then, the data is divided into 8 blocks with the size of 10 k samples to be transferred iteratively to the VSG for the IQ modulation. The resulting RF signal leaves the transceiver to feed the amplification unit. The PA output is then connected to the transceiver input through an attenuation block. The observed PA output signal is then demodulated to obtain the baseband signal. Lastly, the host processor aligns the observed signal with the data generated locally and estimates the coefficients of the PA behavioral model. After model identification, the host processor performs the digital predistortion and sends the predistorted data to the PA.

B. Modeling Process and Evaluation Metrics

The EIQMPM is evaluated using the normalized mean square error (NMSE) that allows estimating the deviations between the measured and modeled output of the PA. Its expression in dB is given by:

$$\text{NMSE} = 10\log_{10}\left(\frac{\sum_{n=1}^{N}\left|y_{\text{measured}}(n) - y_{\text{model}}(n)\right|^2}{\sum_{n=1}^{N}\left|y_{\text{measured}}(n)\right|^2}\right) \quad (26)$$

where $y_{\text{measured}}(n)$ and $y_{\text{model}}(n)$ are the measured and modeled PA output signals, respectively, while N is the length of the waveforms in the discrete time domain.

In forward modeling, a very common approach to select the parameters of the model is by performing a systematic NMSE study, in which the nonlinearity order K and the memory depth M are increased until sufficiently high performance is obtained [1]–[3]. In this work, this approach was used to determine the values of the nonlinearity order and memory depth of the model described in (5). Determining suitable values for K and M is important to have an accurate model with the minimum computational cost. In our architectures, the nonlinearity order and memory depth of the EIQMPM were set to 7 and 3, respectively. Once an accurate model with a very low NMSE better than -42 dB is obtained, we can insert it into the feedback path of the developed DSMs as described in the previous sections.

In order to quantify and measure the performance of the overall proposed DPD architectures, the adopted figures of merit are the SNDR to evaluate the in-band signal quality and the adjacent channel power ratio (ACPR) to measure the out-of-band emissions. The ACPR is defined as the ratio of the

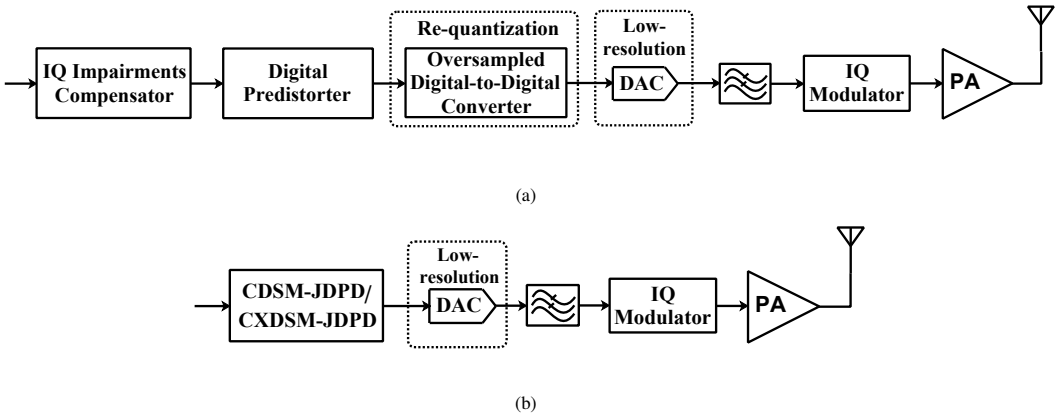


Fig. 7. Overall transmitter systems with low-resolution DACs. (a) A traditional approach. (b) The proposed approach.

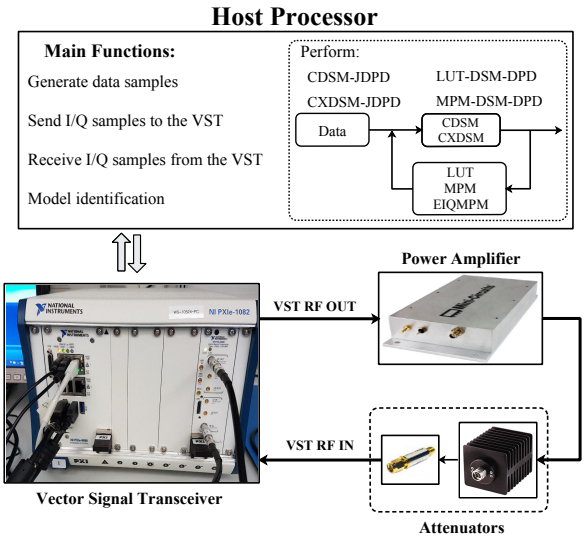


Fig. 8. RF measurement setup used in this work for experimentation and validation.

powers within the desired channel (P_{desired}) and the right or left adjacent channel (P_{adjacent}), expressed as

$$\text{ACPR (dBc)} = 10\log_{10}\left(\frac{P_{\text{desired}}}{P_{\text{adjacent}}}\right) \tag{27}$$

C. RF Experiment 1 – 5G Band n3 (1.8 GHz)

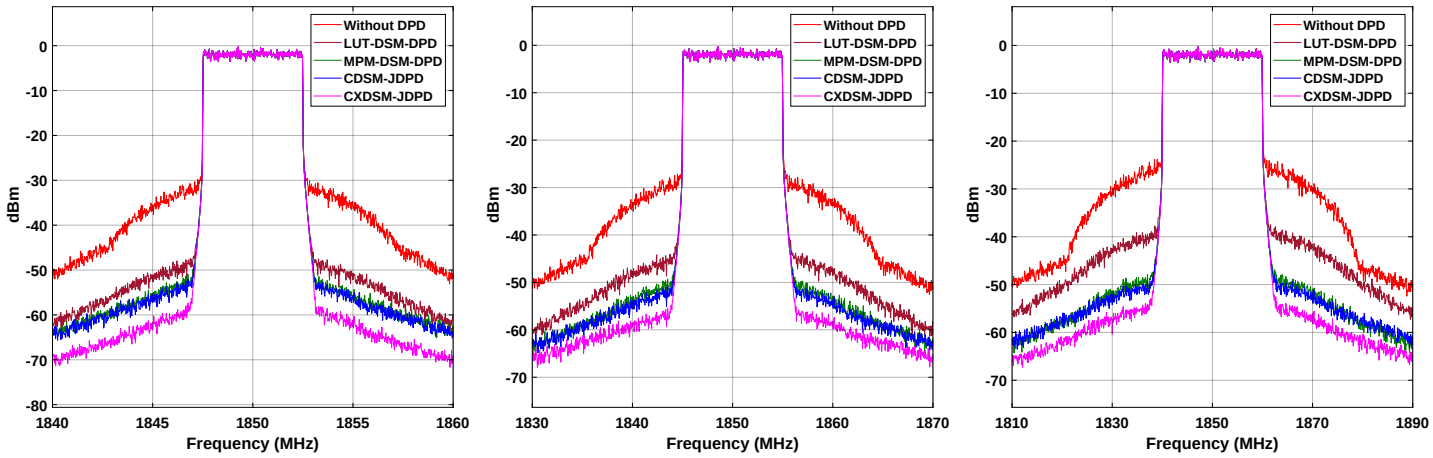
In this experiment, the proposed CDSM-JDPD and CXDSM-JDPD are tested using three different channel bandwidths of 5, 10, and 20 MHz at the 1.8 GHz band. The DPD architectures use 4-bit quantizers, and OSRs of 16 and 32. For comparison purposes, we also used and tested two DSM-based DPDs incorporating look-up tables (LUTs) and memory polynomial models.

1) Scenario 1: No IQ Impairments: Fig. 9 shows the spectra of the PA output signals obtained with the CDSM-JDPD and CXDSM-JDPD while also comparing to those obtained using the LUT and MPM-DSM based predistorters. Overall, all the architectures provide good linearization performance, especially the CXDSM-JDPD. Specifically, the CDSM-JDPD and the MPM-DSM-DPD show comparable performance while the CXDSM-JDPD exhibits a significant improvement. This is explained by the fact that the CXDSM is an improved version of the cartesian DSMs used in the other architectures. It generates less quantization noise, and therefore better performance is achieved. More details can be found in Table I which summarizes the measured SNDR and ACPR results of the four DPD topologies using three different bandwidths of 5, 10, and 20 MHz, and two OSRs of 16 and 32. Firstly, it is clear that the CXDSM-JDPD has the best performance in terms of SNDR and ACPR in all the cases. It is also worth mentioning that the differences in the ACPR and SNDR values between the LUT-DSM-DPD and the other architectures are significantly increased when expanding the bandwidth of the signal. This is explained by the reason that the LUT model is static, which means that it is unable to handle memory effects that, in turn, cannot be neglected when the bandwidth of the signal gets wider.

2) Scenario 2: With IQ Impairments: In order to have a more realistic environment and performance assessment, similar measurements are next reported under the non-ideal IQ modulation conditions. Fig. 10 presents the obtained PA output spectra of the evaluated DPD topologies and Table I again summarizes the obtained measurement results in terms of SNDR and ACPR. As can be observed, the CDSM-JDPD and the CXDSM-JDPD are able to very effectively compensate for the distortions, whereas the LUT-DSM-DPD and the MPM-DSM-DPD are clearly falling short. This can be seen through the significant drop in their performance as they are unable to compensate for the nonlinearity of the PA in the presence of IQ impairments. Thus, when the distortion is caused by the joint contribution of the coexisting IQ modulator and PA impairments, it is clear that the proposed CDSM-JDPD and the CXDSM-JDPD clearly outperform the other DSM-based predistorters.

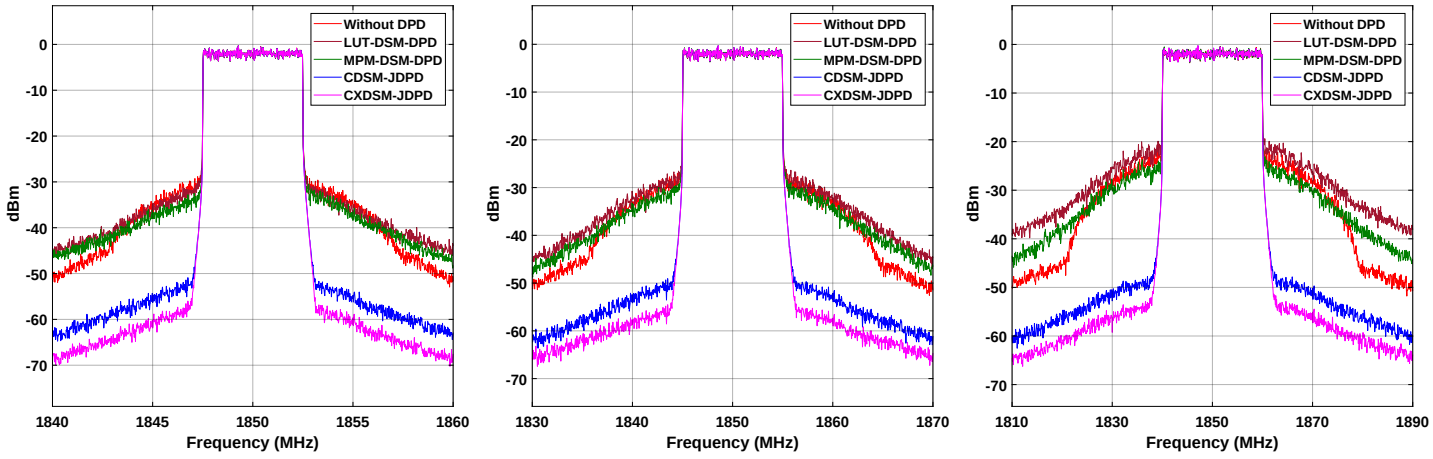
D. RF Experiment 2 – 5G Band n3 (1.8 GHz), Varying DAC Resolution and Reduced OSR

The goal of this second experiment is to evaluate the introduced CDSM-JDPD and CXDSM-JDPD using different



(a) (b) (c)

Fig. 9. Measured PA output spectra of the CDSM-JDPD and the CXDSM-JDPD in comparison with the LUT and the MPM DSM-based linearizers, at NR band n3, when using 5G NR signals *without IQ impairments*. (a) 5 MHz. (b) 10 MHz. (c) 20 MHz.



(a) (b) (c)

Fig. 10. Measured PA output spectra of the CDSM-JDPD and the CXDSM-JDPD in comparison with the LUT and the MPM DSM-based linearizers, at NR band n3, when using 5G NR signals *with IQ impairments*. (a) 5 MHz. (b) 10 MHz. (c) 20 MHz.

number of bits for the DACs, i.e., 4, 8, and 12 bits. This evaluation was carried out again at the 1.8 GHz band and using a transmission bandwidth of 20 MHz, while the applied OSR is now reduced to 8 compared to the previous Experiment 1. The two scenarios of no IQ impairments and with IQ impairments are also considered in this experiment. In general, although this work offers the benefit of using low-resolution DACs, it is important to show the effect of different resolutions to evaluate the effectiveness of the architectures in various applications, while also demonstrating the proper operation and good performance with reduced OSR.

1) Scenario 1: No IQ Impairments: Table II presents the measured results of the CDSM-JDPD and CXDSM-JDPD. As it can be observed, the proposed transmitters provided good SNDR and ACPR values for all the different cases. These results show that the linearization performance increases with the increase in the number of bits. It is worth mentioning that the increase in the SNDR and ACPR from the 8-bit case to 12-bit case is smaller than the increase from 4-bit to 8-bit. This is also explained by already approaching the practical linearization performance limit as in any linearization system.

2) Scenario 2: With IQ Impairments: Table II summarizes also the measured SNDR and ACPR performance when IQ impairments are present. We can observe that for all the different cases in terms of the numbers of bits, the CDSM-JDPD and CXDSM-JDPD are maintaining a good linearization performance despite the presence of IQ impairments. In addition, as in the first scenario, the SNDR and ACPR improve with the increase in the number of bits. The difference when moving from 4-bit case to 8-bit case is higher than the difference between the 8-bit to 12-bit cases. Overall, the results in Table II also demonstrate that the proposed linearization systems can offer good performance also with the reduced OSR of 8.

E. RF Experiment 3 – 5G Band n78 (3.5 GHz)

In our next experiments, in order to provide more complete evaluations, the proposed topologies are further assessed

TABLE I
SUMMARY OF THE MEASURED LINEARIZATION PERFORMANCE AT 1.8 GHZ BAND WITH DIFFERENT CHANNEL BANDWIDTHS AND OVERSAMPLING RATIOS WHEN APPLYING 5G NR SIGNALS, AND CONSIDERING TWO DIFFERENT SCENARIOS

Bandwidth (MHz)	OSR	Architecture	Scenario 1 (no IQ impairments)		Scenario 2 (with IQ impairments)	
			SNDR (dB)	ACPR (dBc)	SNDR (dB)	ACPR (dBc)
5	16	Without DPD	28.65	-34.53/-34.32	27.55	-33.76/-33.58
		LUT-DSM-DPD*	42.32	-46.58/-46.47	27.10	-33.42/-33.65
		MPM-DSM-DPD**	47.13	-50.98/-50.92	28.11	-34.02/-34.15
		CDSM-JDPD	47.35	-51.50/-51.46	46.19	-50.42/-50.38
		CXDSM-JDPD	52.21	-57.27/-57.24	52.12	-55.79/-55.75
	32	Without DPD	30.32	-36.23/-36.03	29.61	-35.44/-35.24
		LUT-DSM-DPD	47.25	-51.57/-51.45	30.64	-35.75/-35.83
		MPM-DSM-DPD	51.65	-55.47/-55.51	31.50	-37.47/-36.85
		CDSM-JDPD	52.38	-56.28/-56.23	51.45	-55.23/-55.18
		CXDSM-JDPD	57.75	-62.05/-62.02	56.87	-60.51/-60.48
10	16	Without DPD	25.21	-31.64/-31.39	24.32	-30.67/-30.45
		LUT-DSM-DPD	38.55	-43.56/-43.27	22.63	-29.07/-29.19
		MPM-DSM-DPD	46.28	-50.92/-50.84	23.68	-29.65/-29.47
		CDSM-JDPD	46.69	-51.80/-51.65	44.53	-48.65/-48.50
		CXDSM-JDPD	52.50	-56.52/-56.43	50.40	-54.60/-54.47
	32	Without DPD	28.20	-34.01/-33.72	27.71	-33.82/-33.55
		LUT-DSM-DPD	43.97	-48.42/-48.12	26.56	-32.50/-32.20
		MPM-DSM-DPD	49.59	-53.66/-53.62	28.74	-34.75/-34.48
		CDSM-JDPD	50.70	-54.74/-54.62	49.39	-53.23/-53.10
		CXDSM-JDPD	55.56	-58.91/-58.85	54.32	-58.14/-58.07
20	16	Without DPD	21.51	-27.83/-27.57	20.68	-27.12/-26.88
		LUT-DSM-DPD	34.36	-39.61/-39.10	17.39	-22.30/-22.09
		MPM-DSM-DPD	44.52	-49.20/-48.05	21.96	-27.68/-28.14
		CDSM-JDPD	45.62	-50.02/-49.90	42.81	-46.94/-46.81
		CXDSM-JDPD	51.39	-54.91/-54.95	48.75	-52.52/-52.49
	32	Without DPD	24.67	-30.87/-30.52	22.39	-28.94/-28.65
		LUT-DSM-DPD	37.96	-43.15/-42.60	20.15	-27.14/-26.82
		MPM-DSM-DPD	47.26	-51.92/-51.84	23.68	-29.83/-30.37
		CDSM-JDPD	48.85	-52.80/-52.71	47.52	-51.31/-51.20
		CXDSM-JDPD	53.52	-57.14/-57.25	52.29	-56.11/-56.18

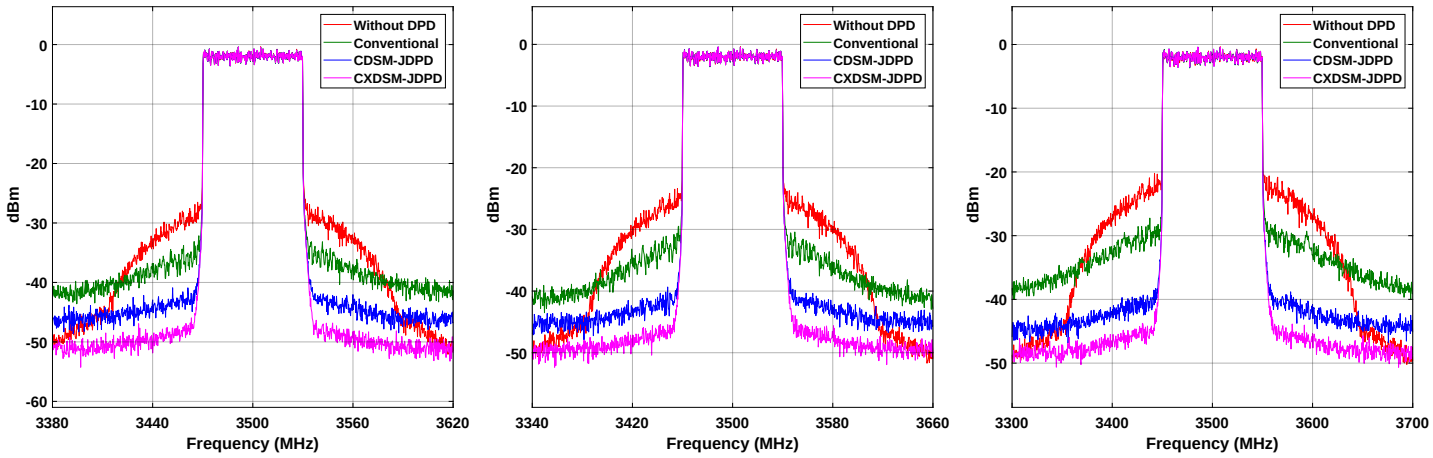
* DSM-based DPD using an LUT model
** DSM-based DPD using an MPM

TABLE II
SUMMARY OF THE MEASURED LINEARIZATION PERFORMANCE AT 1.8 GHZ BAND WITH DIFFERENT NUMBERS OF BITS WHEN APPLYING 5G NR SIGNALS WITH AN OVERSAMPLING OF 8, AND CONSIDERING TWO DIFFERENT SCENARIOS

No. bits	Architecture	Scenario 1 (no IQ impairments)		Scenario 2 (with IQ impairments)	
		SNDR (dB)	ACPR (dBc)	SNDR (dB)	ACPR (dBc)
4	Without DPD	19.89	-26.01/-25.84	19.16	-25.48/-25.12
	CDSM-JDPD	42.51	-46.93/-46.55	38.23	-42.38/-42.56
	CXDSM-JDPD	48.32	-51.87/-51.92	44.40	-48.35/-48.28
8	Without DPD	22.12	-28.63/-28.46	21.50	-27.95/-28.03
	CDSM-JDPD	50.72	-53.98/-54.18	46.73	-50.31/-50.72
	CXDSM-JDPD	56.71	-60.14/-60.19	53.15	-56.64/-56.81
12	Without DPD	23.16	-29.43/-29.66	22.53	-28.90/-28.72
	CDSM-JDPD	51.84	-47.21/-47.83	48.12	-51.51/-51.36
	CXDSM-JDPD	57.95	-61.68/-61.56	54.51	-58.05/-57.98

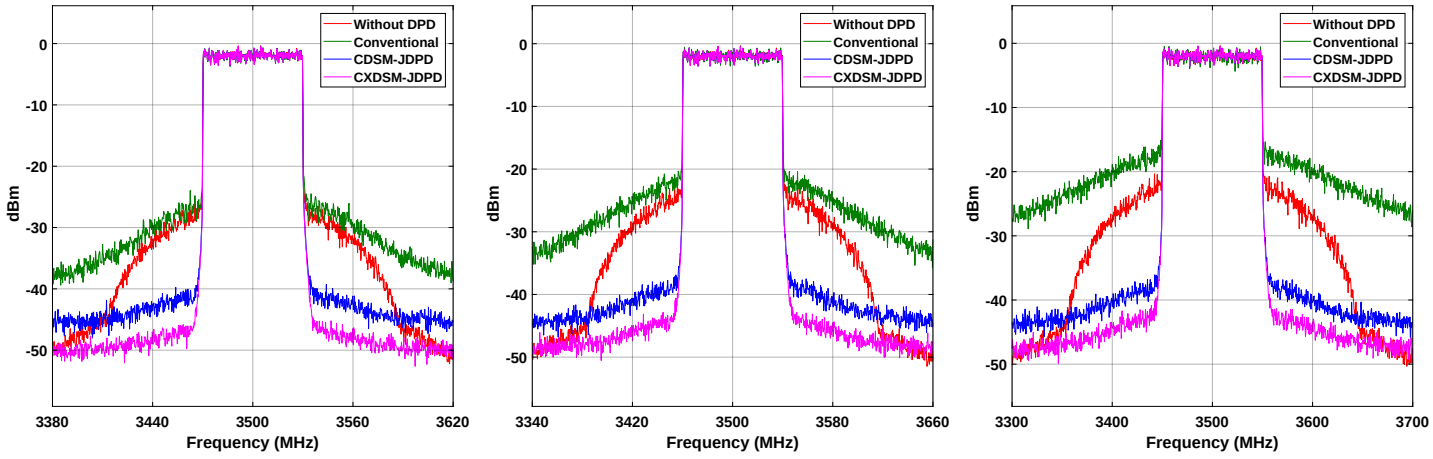
and compared to a conventional memory polynomial-based DPD system. For a fair comparison, all the architectures are followed by a 6-bit DAC. In addition, the input data is oversampled by a factor of 8 for all the evaluated DPD architectures. Therefore, the quantizer number of bits for the CDSM-JDPD and CXDSM-JDPD are set to 6. Furthermore, wider channel bandwidths of 60, 80, and 100 MHz are chosen for this experiment, and the measurements are performed at the 3.5 GHz band. Like in the prior two experiments, the measurements cover the two scenarios – without and with IQ impairments.

1) Scenario 1: No IQ Impairments: Fig. 11 presents the PA output spectra of the CDSM-JDPD and CXDSM-JDPD while also comparing to the conventional MP-based DPD. Furthermore, Table III provides the measured SNDR and ACPR of these architectures for the three different channel bandwidths. We can observe that the CDSM-DPD and CXDSM-JDPD clearly outperform the reference MP DPD. This is explained by the usage of the same low-resolution DAC for all the architectures. To this end, one of the advantages of the proposed architecture is that it supports low-resolution DACs by doing the so-called digital-to-digital conversion that performs the requantization of the digital signal to a lower granularity and also predicts and corrects the future quantization noise of the DAC, which mitigates the inband deviation and maintains the accuracy of the predistorted signal. On the other hand, the conventional DPDs require higher resolution DAC to prevent their linearization performance from being affected. This can be clearly observed in Table III.



(a) (b) (c)

Fig. 11. Measured PA output spectra of the CDSM-JDPD and the CXDSM-JDPD in comparison with a conventional memory-polynomial DPD using a 6-bit DAC, at NR band n78, when applying 5G NR signals *without IQ impairments*. (a) 60 MHz. (b) 80 MHz. (c) 100 MHz.



(a) (b) (c)

Fig. 12. Measured PA output spectra of the CDSM-JDPD and the CXDSM-JDPD in comparison with a conventional memory-polynomial DPD using a 6-bit DAC, at NR band n78, when applying 5G NR signals *with IQ impairments*. (a) 60 MHz. (b) 80 MHz. (c) 100 MHz.

2) Scenario 2: With IQ Impairments: The measured PA output spectra and the summary of the SNDR and ACPR values when the practical IQ modulator impairments are also included, are presented in Fig. 12 and Table III, respectively. As expected, these results show the capability of the CDSM-JDPD and the CXDSM-JDPD to provide the desired linearization even in the presence of the IQ impairments, whereas the performance of the conventional DPD has significantly dropped. It can also be seen that the CXDSM-JDPD outperforms again the other topologies.

Overall, these results confirm the capability of the proposed concept to provide a robust and complete DPD system that is able to compensate for the nonlinearity and memory effects of the PA, the nonidealities of the IQ modulator, while at the same time supporting the usage of low-resolution DACs and operating at an implementation feasible OSR.

F. Comparative Assessment Against Related Works

In this section, we compare the proposed approach to other related transmitter systems reported in the literature, specifically those described in [23], [24], and [31], from an operational complexity point of view. Table IV summarizes the comparison, building on the below discussion.

Regarding the DSM-based DPD systems, [23] focuses on using a LUT-based model to describe the PA nonlinear behavior, while neglecting IQ impairments. The architecture uses a high oversampling of 128, a 4-bit DAC, and a LUT with a size of 16 × 16. Employing a LUT model helps in reducing the number of arithmetic operations in the system, but larger memory would be required in order to store the instantaneous complex gain values of the PA. In addition, only memoryless nonlinearity is taken into account, which makes the DPD only suitable for narrowband applications. The work also focuses only on a first-order DSM. This will offer more simplicity to the system as only one integration loop is required. However, in this case, high oversampling rates are required to reduce

TABLE III
SUMMARY OF THE MEASURED LINEARIZATION PERFORMANCE AT 3.5 GHZ BAND WITH DIFFERENT CHANNEL BANDWIDTHS WHEN APPLYING 5G NR SIGNALS WITH AN OVERSAMPLING OF 8, AND CONSIDERING TWO DIFFERENT SCENARIOS

Bandwidth (MHz)	Architecture	Scenario 1 (no IQ impairments)		Scenario 2 (with IQ impairments)	
		SNDR (dB)	ACPR (dBc)	SNDR (dB)	ACPR (dBc)
60	Without DPD	27.53	-33.54/-33.21	26.46	-32.81/-32.49
	Conventional MP	33.58	-37.52/-37.43	25.02	-29.99/-29.38
	CDSM-JDPD	41.26	-43.65/-43.69	39.89	-42.39/-42.25
	CXDSM-JDPD	46.57	-48.78/-48.70	45.30	-47.58/-47.40
80	Without DPD	24.01	-30.59/-30.30	23.03	-29.66/-29.40
	Conventional MP	31.16	-35.60/-35.65	20.45	-25.15/-24.98
	CDSM-JDPD	40.03	-42.68/-42.39	37.53	-40.61/-40.52
	CXDSM-JDPD	45.15	-47.34/-47.19	42.79	-45.46/-45.31
100	Without DPD	21.05	-27.60/-27.38	20.11	-27.69/-27.47
	Conventional MP	28.64	-32.10/-32.05	15.73	-19.79/-19.56
	CDSM-JDPD	38.92	-41.62/-41.39	36.21	-39.85/-39.76
	CXDSM-JDPD	43.74	-46.08/-45.95	41.12	-44.12/-43.89

the level of the generated noise in the band of interest.

The transmitter in [24] differs by upconverting and amplifying the quantized data and only uses the low-pass filter (LPF) after the PA. The reason for this is to amplify directly the predistorted, upconverted quantized signal. However, this approach will cause a reduced efficiency in the system as both the useful signal and the out-of-band noise will be amplified. The actual DPD in [24] focuses on implementing an MPM with a nonlinearity order of 12 and a memory depth of 3, which enables describing the dynamic nonlinear behavior of the PA. However, the transmitter development is focusing on narrowband systems, with a maximum of 4 MHz channel bandwidth reported in the measurements, while neglecting the IQ impairments.

Finally, in [31], joint mitigation of IQ impairments and PA nonlinearity is pursued. The approach utilizes EIQMPM basis functions in an ordinary DPD setup, building on least-squares -based indirect learning architecture (ILA), with nonlinearity order of 3 and memory depth of 3. Relatively high oversampling rate of around 10 is adopted. The ILA based learning for post-inverse model imposes clear additional complexity, compared to forward modeling based approaches, as the EIQMPM basis functions must be calculated from the observed PA output in the learning phase, while being then also separately calculated from the digital transmit signal in the actual linearization phase. Such inverse model calculations are completely avoided in the proposed methods.

In our work, the two DSM-based architectures are based on second-order modulators. This increases the complexity to some extent by adding one more integration loop, but the noise shaping operation is more efficient, and therefore the OSR requirement is relaxed. As mentioned earlier, embedding the PA forward model in the feedback does not cause stability issues as far as phase alignment and gain normalization are performed. The nonlinear behavior of the PA is described by an EIQMPM with a nonlinearity order of 7 and a memory depth of 3. The implementation of this model is straightforward in digital hardware. The CXDSM-JDPD is a new approach, in which, the DPD is applied using a complex polar quantizer in order to reduce the generated noise by quantizing the phase and noise separately, relaxing therefore, the OSR requirement. Both methods have built-in capability for joint IQ and PA impairment mitigation, and the adopted OSR values as low as 8 are very similar to the oversampling factors of conventional DPD systems.

G. Further Discussion on Benefits and Limitations

In general, one important advantage that the proposed architectures offer is the generation of the inverse behavior of the PA without the need for the reverse modeling – as is conventionally done in DPD systems. The fact that only the PA forward model is required makes it possible to overcome model inversion stability and precision issues. Furthermore, in addition to the PA nonlinearity and memory effects, the imperfections of the IQ modulator should in general be taken into account. These impairments are known to cause the appearance of more distortions at the PA output, and to cripple the linearization performance of the DPD by heavily biasing the estimated coefficients – which in turn can make the spectral regrowth even more severe. To this end, all the previously reported DSM-based DPDs allow compensating for the PA nonlinearity, but they do not handle the distortions of the IQ modulator. Thus, the ability of the presented CDSM-JDPD and CXDSM-JDPD architectures to jointly mitigate the PA nonlinearity and the corresponding memory effects, and also the co-existing IQ impairments arising from the IQ modulator without extra hardware or algorithms, is one clear benefit.

Furthermore, considering the importance of maintaining the accuracy of the predistorted data, and considering the fact that high resolution DACs are costly, more complex, and power-hungry, the conversion from the digital domain to analog domain has always been a challenge for system designers. However, the proposed architectures inherently support low-resolution DACs while preserving the desired precision of the predistorted data. Specifically, the presented topologies not only re-quantize the digital signal to a lower granularity but also predict and correct the future quantization error values, mitigating therefore the in-band deviation and preparing to the conversion more efficiently.

One practical limitation that should be noted and considered, related to the DSM-based transmitters, is the potentially high sampling rate required for achieving the desired performance. High OSR and sample rates can be challenging issues, particularly with wideband signals. However, new software defined

TABLE IV
COMPARISON OF THE PROPOSED TRANSMITTERS WITH RELATED WORKS REPORTED IN THE LITERATURE

Ref.	BW (MHz)	f_s/BW	Quantization bits	Quantization type	Compensation
[23]	3.4	128	4	Conventional (real)	PA nonlinearity
[24]	4	16	3	Conventional (real)	PA nonlinearity Memory effects
[31]	3.84	10.42	–	–	PA nonlinearity Memory effects IQ impairments
Proposed CDSM-JDPD	100	8	6	Conventional (real)	PA nonlinearity Memory effects IQ impairments
Proposed CXDSM-JDPD	100	8	6	Complex polar	PA nonlinearity Memory effects IQ impairments

radio (SDR) type systems are more and more using fast yet low- or medium-resolution DACs in order to reduce the cost and power consumption of transmitters, while often utilizing also means to shorten the word length and shape the quantization noise before the DAC. Such schemes are well inline with the concept proposed in this work, and exploiting such synergies and benefits are likely to offer more opportunities for new SDR systems. Furthermore, in this article, OSR values as low as 8 were shown to be feasible, while the proposed architectures demonstrated excellent linearization performance with channel bandwidths in the order of 100 MHz. Moreover, the complex polar quantization enhances the performance of the overall system by reducing the generated quantization noise without the need of high OSRs, thus leading to more accurate linearization capabilities compared to the previous alternatives.

VI. CONCLUSION

This article proposed two new digital predistortion schemes, based on multibit cartesian and complex DSMs, for the joint mitigation of RF transmitters' impairments, specifically the PA nonlinearity and the IQ impairments generated by the IQ modulator. The linearization schemes also support the use of low-resolution DACs, which provides clear implementation benefits for wireless transmitters. The concept behind the proposed architectures is to use a properly constructed forward EIQMPM in the feedback path of multibit CDSM and CXDSM. To validate the proposed DPD architectures, extensive collection of RF measurements at 5G NR bands n3 and n78 was reported, covering both narrowband and wideband signals with channel bandwidths ranging between 5 to 100 MHz, while also varying the oversampling ratio and bit widths. The linearization performance of both proposed topologies were extensively assessed and compared to those of other DSM-based linearization approaches. The RF measurement results demonstrate very encouraging linearization performance, with the proposed architectures being shown to efficiently compensate for the PA nonlinearity even in the presence of severe IQ impairments, while the reference DSM-based DPD approaches were shown to fall short in that regard. The proposed architectures are thus promising and versatile solutions for future digitally-intensive radio transmitters, with applications ranging from lower-cost narrowband to high-end wideband wireless systems.

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