

RESEARCH ARTICLE

A New DeadBeat-Based Direct Power Control of Shunt Active Power Filter With Digital Implementation Delay Compensation

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ABSTRACT Active Power Filter (APF) can significantly compensate the current harmonics produced by nonlinear loads. To do this feature, harmonic detection reference current generation play vital role. Direct Power Controller (DPC) has great harmony with instantaneous power compensation (PQ) algorithm as well as the ability to eliminate internal current loops. In addition, DeadBeat Controller (DBC) has high compatibility for digital implementation, superior control performance and fast dynamic response. However, DBC suffers from time delay linked to control action calculation and digital implementation. In this paper, a new deadbeat-based DPC method is proposed firstly to generate reference current and control of APF. Secondly, a simple and robust compensation method is proposed to eliminate aforementioned deadbeat delay thanks to the online/offline predictions. Several simulations are conducted in MATLAB/SIMULINK verified by experimental tests obtained from a DSP-based active power filter to illustrate the effectiveness and superior performance of the proposed control method. By employing the proposed control method, the Total Harmonic Distortion (THD) of grid current is decreased from 22% to 3% under steady state condition. While the dynamic response with proposed delay compensation validates significant transient response improvement.

INDEX TERMS Active power filter (APF), direct power control (DPC), deadbeat control.

I. INTRODUCTION

Nonlinear loads such as power converters, motor drives, and Uninterruptible Power Supplies (UPS) and diode rectifier are abundantly used in power system [1]. This type of loads causes the flow of harmonic currents to the AC power system. Harmonics cause severe problem and have adverse effects on distribution power loss and communication lines due to electromagnetic interference [2]. Hence, harmonics filtering is an emerging issue in modern power system.

One of the conventional methods for harmonics filtering in power system is the use of passive filters which suffers from several drawbacks such as resonance problem, limited

capability and flexibility. To overcome passive filters drawbacks, Active Power Filters (APFs) were introduced. APFs can compensate harmonics in power system by power electronics based devices [1]. The field is enriched with several advancement such as APF topologies called hybrid topologies. Enhancing the passive filter performance and power-rating reduction of the active filter are the main characteristics of hybrid topologies [3], [4].

Among different APFs configuration, Shunt configuration has been the most studied topology in which, the APF is connected parallel to the load [5]. Shunt Active Power Filter (SAPF) not only compensates the current harmonics but also, it can compensate the reactive power. Hence, the SAPF must be able to detect and generate the compensation current instantaneously without any delay even under sudden variation of load and harmonics current. Therefore, SAPF

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should be designed with very simple as well as very high dynamic response and accurate control system.

Active power filter control systems consist of two parts: 1) current harmonics identification and 2) current harmonics injection.

A. CURRENT HARMONICS IDENTIFICATION

Different identification methods are grouped into time domain and frequency domain ones [6]. Several frequency domain methods are found in literatures such as the windowing-wavelet based technique [7], Discrete Fourier Transform (DFT) [8], Fast Fourier Transform (FFT) [9] and Artificial Neural Network (ANN) techniques [10]. Among various time domain methods [11], [12], instantaneous power theory which is known as PQ method which uses instantaneous power allowing excellent dynamics is the widely use technique [11].

B. CURRENT HARMONICS INJECTION

Different algorithms have been developed in recent years to control APFs. Hysteresis current control is the first candidate because of simplicity and easy implementation [13]. The main drawback is variable switching frequency [14]. Another solution is repetitive control or dual repetitive control which strongly suffers from very low dynamic response [15]. In addition, these methods are current-based methods which is not compatible with PQ identification method. Another solution is a Lyapunov function based controller which provides high tracking accuracy [16]. But, it again suffers from variable switching frequency, high sampling frequency for good operation and high calculation burden. Also, it just provides simulation results without any experimental validation.

Direct Power Control (DPC) method offers decoupled active and reactive power control without the inner current loop [17]–[19]. This method is highly applicable for SAPF with simple PQ theory identification algorithm. The conventional DPC is based on predefined switching table [19]. This method offers simplicity as well as fast dynamic response but, it suffers from variable switching frequency and model dependency. The hysteresis controllers and the switching table are substituted by two controllers from the robust H_∞ control (that minimized the disturbance rejection gain defined as $\sup_{w \neq 0, w \in L_2} \|z\|_2 / \|w\|_2$ where z is desired output and w is disturbance), and a Space Vector Modulation (SVM) block, thus ensuring a constant switching frequency [20]. However, the control method requires high sampling frequency, tedious parameters tuning and model dependency. Due to the several benefits of Model Predictive Control (MPC) such as, fast tracking response and simple inclusion of system nonlinearities, this type of controller has been recently adopted for power electronics converters control [21]–[23]. Finite Control Set MPC (FCS-MPC) is a model based control strategy which presented for shunt active power filter control [23]. However, all of these methods mainly force very high calculation and computational burden.

In addition, they are converter-based and not general solution only applicable for one converter topology. Recently, sliding mode-based DPC are also proposed for control of SAPFs with fast dynamic response and low chattering [24]. However, most of the developed methods impose high computation burden beside laborious control parameter tuning.

On the other hand, a DeadBeat Controller (DBC) is a digitally-compatible method which has been used for power converters' control. It provides high dynamic response and guarantees robustness of the control system under a wide range of model parameter changes [25], [18]. It is also used for current control of APF because of the advantages such as high control accuracy and fast dynamic response with fixed switching frequency as it is proposed in [26]. Also, DPC method with DeadBeat concept was also proposed for three phase rectifiers [18]. But, this paper used deadbeat concept in which the control system calculates the zero and non-zero vector times that will set the active and reactive powers at desired value at instant $k + 2$ with two sampling delays. Hence, the way of DB implementation is more conceptual not DB logical procedure. However, the DBC method faces the problem raised by the control delay and also the current tracking error. Hence, an improved DBC with current tracking error compensation is introduced for APFs [27]. Moreover, the conventional DBC suffers from the effects of sampling errors on current control performance. This problem can be improved by control variable prediction which already proposed in [28].

In order to overcome the drawbacks of the DBC method, an appreciate delay compensation is essential which should be considered carefully.

C. CONTRIBUTIONS AND ORGANIZATION

To sum up, DPC is an attractive, fast dynamic response control algorithm highly compatible with PQ identification theory. However, complicated structure, variable switching frequency and model dependency are the main drawbacks. In addition, a simple structure with fixed switching frequency and perfect coordination for digital implementation are the advantages of DBC method but, an appreciate delay compensation is essential. In this paper a new DB-Based DPC method is proposed to control the SAPF to have the merits of both DBC and DPC methods for SAPFs. In the proposed control method, the simplicity and superior performance of the DPC is accompanied by highly digitally compatible, high dynamic response and robust (against model parameters and load variations) DBC. Moreover, an offline delay compensation method is proposed to improve the sampling delay issue associated with DBC. To sum up, the contribution of the paper can be listed as follow:

- New DB-Based DPC method is adopted for SAPF,
- New optimized offline prediction unit based on RLS method for delay compensation is proposed,
- Periodic reference active and reactive powers tracking capability with high dynamic response is ensured,

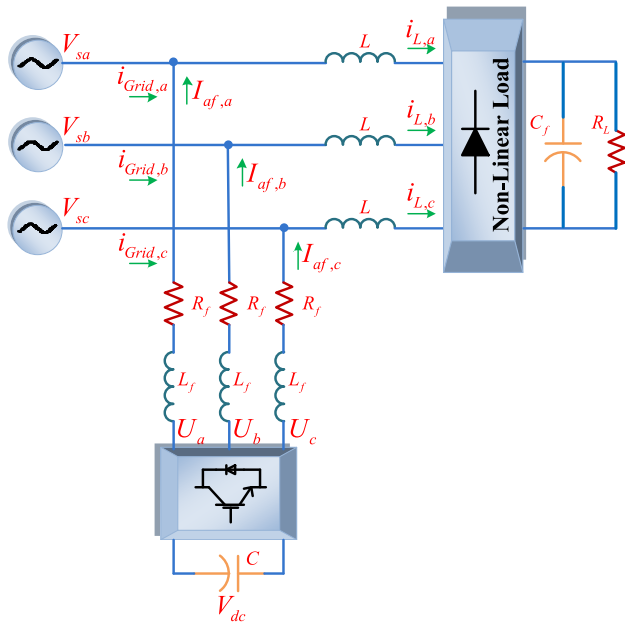


FIGURE 1. Shunt active power filter.

- High robustness against wide model parameter mismatches is verified,
- High simplicity with very low computational burden is assured,
- General high performance of proposed method through different quality factors such as THD% is validated.

The rest of the paper is organized as follow. In section II, the structure of SAPF is described. Section III and IV are regarded to the proposed DB-Based DPC method and delay compensation procedure. Simulation and experimental results are presented in section V and VI while the conclusion is included in section VII.

II. SHUNT ACTIVE POWER FILTER

SAPF acts as a controllable current source. A Voltage Source Inverter (VSI) which is connected to the Point of Common Coupling (PCC) through a series inductor forms a SAPF. The DC bus is supported only by a capacitor therefore, this filter can only produce non-active power. For this reason, this type of active filter can compensate any harmonics and reactive power which is caused by nonlinear loads. Fig. 1 shows the configuration of SAPF supplying a nonlinear load represented by diode rectifier followed by capacitive filter and resistive load. The filter equations in *abc* reference frame are obtained as follows:

$$\frac{di_{af,abc}(t)}{dt} = \frac{1}{L_f} V_{s,abc}(t) - \frac{R_f}{L_f} i_{af,abc}(t) - \frac{U_{abc}(t)}{L_f} \quad (1)$$

where $V_{s,abc}$, i_{af} and U_{abc} stand for grid voltage, APF current and APF output voltage, relatively. L_f and R_f are APF series inductor and resistor.

DC link voltage can be related to ac side current as below:

$$\frac{dV_{dc}}{dt} = \frac{1}{C} [S_a i_{af,a}(t) + S_b i_{af,b}(t) + S_c i_{af,c}(t)] \quad (2)$$

where V_{dc} is APF DC voltage. S_a , S_b and S_c stand for each leg state including 1 or 0 either a positive or a negative voltage is produced at the leg output with respect to the DC-Link midpoint. Equation (1) in vector notation can be expressed as (3).

$$L_f \frac{d\vec{i}_{abc}(t)}{dt} = R_f \vec{i}_{abc}(t) + \vec{u}_{abc}(t) - \vec{v}_{s,abc}(t) \quad (3)$$

A. REACTIVE AND HARMONIC CURRENT EXTRACTION

According to instantaneous power theory, for power calculation, three phase voltages and currents are transferred to dq frame and the active and reactive powers are calculated as follow:

$$P = v_d i_d + v_q i_q \quad (4)$$

$$Q = v_q i_d - v_d i_q \quad (5)$$

It is worth to be mentioned that active and reactive powers will remain constant if three phase voltages and currents are balanced and harmonics free. If three phase currents are unbalance and contain harmonics, the instantaneous power is combination of a steady state average term and ripple term.

$$P = \bar{P} + \tilde{P} \quad (6)$$

$$Q = \bar{Q} + \tilde{Q} \quad (7)$$

In (6) and (7), \bar{P} and \bar{Q} are the powers free of any harmonics providing sinusoidal currents. The active and reactive ripple powers (\tilde{P} , \tilde{Q}) are caused by unbalanced and harmonics currents. In desirable condition of grid voltage, only absorbing active power is permitted and the other power harmonics components should be compensated or reduced to standard range.

Ripple components of active and reactive power which correspond to current harmonics, should be compensated in order to have pure sinusoidal current. To reduce absorbed reactive power from grid and increasing power factor, load reactive power should be compensated by SAPF. As a result, reference active and reactive power will be defined as:

$$P_{APF}^* = \bar{P} \quad (8)$$

$$Q_{APF}^* = \tilde{Q} + k\bar{Q} \quad (9)$$

These values are the input of control system for generating harmonic components. In order to produce power components, proposed DPC is presented that has maximum compliance with harmonics recognition algorithms in term of digital implementation.

B. DC LINK CONTROLLER

The DC link capacitor provides a constant DC voltage for the SAPF. It is also responsible for reactive power generation and converter switches losses compensation which leads to capacitor discharge. To recharge capacitor with active power absorbed from grid, a PI controller with anti-windup compensator is utilized which is shown in Fig.2.

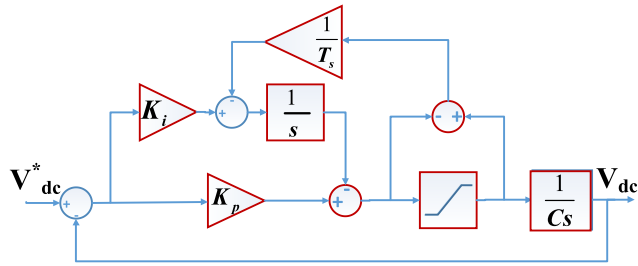


FIGURE 2. Block diagram of anti-windup controller.

The transfer function of anti-windup compensator is determined as follow [24]:

$$\frac{V_{dc}}{V_{dc\ ref}} = \frac{K_p s + K_i}{Cs^2 + K_p s + K_i} \quad (10)$$

Close loop transfer function can be reform as a second order transfer function:

$$\frac{V_{dc}}{V_{dc\ ref}} = \frac{\omega_n^2}{s^2 + 2\omega_n \xi s + \omega_n} \quad (11)$$

Then, the K_p and K_i can be formulated as follow:

$$\begin{aligned} K_p &= 2\omega_n \xi C \\ K_i &= \omega_n^2 C \end{aligned} \quad (12)$$

The output of PI controller is multiplied to dc voltage (V_{dc}) to form the active power reference for maintaining the constant DC-Link voltage.

III. PROPOSED DB-BASED DPC CONTROL METHOD

A. PROPOSED DB-BASED DPC METHOD

The complete equations of the SAPF in the abc reference frame are given in (2) and (3). According to three wire configuration, coordinate transformation from three-phase to the synchronous reference frame is performed on (3) and obtained as follows:

$$\frac{d}{dt} \vec{i}_{af,dq} = \left(\frac{R_f}{L_f} + j\omega \right) \vec{i}_{af,dq} + \frac{1}{L_f} \vec{u}_{dq} - \frac{1}{L_f} \vec{v}_{s,dq} \quad (13)$$

Using Euler discretization, the left side of (13) can be discretized by (14). It should be noted that this approximation is confirmed for even low frequencies as ($\frac{F_{sampling}}{f} \gg 20$).

$$\begin{aligned} \frac{d\vec{i}_{af,dq}}{dt} &= \frac{\vec{i}_{af,dq}(k+1) - \vec{i}_{af,dq}(k)}{T_{ps}} \\ &= \left(\frac{R_f}{L_f} + j\omega \right) \vec{i}_{dq} + \frac{1}{L_f} \vec{u}_{dq} - \frac{1}{L_f} \vec{v}_{s,dq} \end{aligned} \quad (14)$$

Decomposing (13) into d and q components results in (15) and (16).

$$\begin{aligned} i_{af,d}(k+1) &= \left(1 - \frac{T_s R_f}{L_f} \right) i_{af,d}(k) + T_s \omega i_{af,q}(k) \\ &\quad + \frac{T_s}{L_f} (u_d(k) - v_{sd}(k)) \\ i_{af,q}(k+1) &= \left(1 - \frac{T_s R_f}{L_f} \right) i_{af,q}(k) + T_s \omega i_{af,d}(k) \end{aligned} \quad (15)$$

$$+ \frac{T_s}{L_f} (u_q(k) - v_{sq}(k)) \quad (16)$$

Based on the power equations mentioned in (8) and (9), the discrete form of active and reactive powers in dq reference frame are given in (17) and (18).

$$P(k+1) = v_d(k+1)i_{af,d}(k+1) + v_q(k+1)i_{af,q}(k+1) \quad (17)$$

$$Q(k+1) = v_q(k+1)i_{af,d}(k+1) - v_d(k+1)i_{af,q}(k+1) \quad (18)$$

In (17) and (18), if dq reference frame is perfectly synchronized with grid voltage due to proper operation of phase locked loop (PLL), so $v_q = 0$ and also $v_{sd} = |v_{sd}| = cte$. Therefore, it can be concluded pretty much that $v_{sd}(k+1) = v_{sd}(k)$. Hence, Equations (17) and (18) are simplified as follows:

$$P(k+1) = v_d(k)i_{af,d}(k+1) \quad (19)$$

$$Q(k+1) = -v_d(k)i_{af,q}(k+1) \quad (20)$$

By substituting (15) and (16) in (19) and (20), active and reactive power equation can be obtained:

$$\begin{aligned} P(k+1) &= \left(1 - \frac{T_s R_f}{L_f} \right) \underbrace{i_{af,d}(k)v_d(k)}_A \\ &\quad + T_s \omega \underbrace{i_{af,q}(k)v_d(k)}_B + \frac{T_s}{L_f} (u_d(k)v_d(k) - v_d^2(k)) \end{aligned} \quad (21)$$

$$\begin{aligned} Q(k+1) &= \left(1 - \frac{T_s R_f}{L_f} \right) \underbrace{i_{af,q}(k)v_d(k)}_C \\ &\quad + T_s \omega \underbrace{i_{af,d}(k)v_d(k)}_D + \frac{T_s}{L_f} (u_q(k)v_d(k)) \end{aligned} \quad (22)$$

Comparing terms (A) and (B) in (21) with (19) and (C), (D) terms with (20), power equations $P(k)$ and $Q(k)$ are obviously seen in (21) and (22).

In other words and according to deadbeat control theory, in k_{th} step and with respect to the measured and reference values, switching signals is calculated for $(k+1)_{th}$ step. Thus, the control variables will meet their references at the end of $(k+1)_{th}$ period. As a result, it can simply concluded that $(k+1)_{th}$ values are equal to k_{th} reference values as given in (23) and (24):

$$P(k+1) = P^*(k) \quad (23)$$

$$Q(k+1) = Q^*(k) \quad (24)$$

Calculation of APF switching signals is a final goal in the proposed DB-Based DPC control system with constant switching frequency. Therefore, advanced modulators can be used for switching power semiconductors with constant frequency.

By substituting (23) and (24) in (21) and (22) and after solving and simplification in order to retrieve U_{dq} , below equations are obtained:

$$U_d(k) = V_d(k) + \frac{L_f}{T_s V_d(k)} [P^*(k) - P(k)] + \frac{R_f}{V_d(k)} P(k) - \frac{L_f \omega}{V_d(k)} Q(k) \quad (25)$$

$$U_q(k) = \frac{L_f}{T_s V_d(k)} [Q^*(k) - Q(k)] + \frac{R_f}{V_d(k)} Q(k) - \frac{L_f \omega}{V_d(k)} P(k) \quad (26)$$

Proposed DPC equations (25) and (26) are simple and contain only few additions, subtraction and multiplication. This ensures high simplicity as well as very low computational burden of the proposed control method. Considering the PWM and sampling delays that are the limitation of digital control implementation, this controller will be the most compatible with digital implementation.

B. DELAY COMPENSATION OF THE PROPOSED DB-BASED DPC METHOD

In the conventional deadbeat, beside one sample delay caused by control algorithm and calculation of control signals, there is another delay related to the digital implementation. These delays dramatically deteriorate the controller performance such as current oscillation and inaccurate APF compensation. In addition, these delays may affect the controller instability. As a result, delay compensation algorithms should be evaluated to remove or decrease the aforementioned effects. In this section, simple and enhanced procedure is proposed to compensate the control algorithm delay.

Values at the $(k + 1)$ th time instant are used as references for k th time instant. This procedure leads to one step delay associated with control law. Therefore, injected powers are one step back at least. To overcome this limitation, values at the $k + 1$ th time instant must be present at the k th time instant. In this case we can predict $(k + 1)$ th control laws in k th time instant and control law delay will be compensated. This delay compensation method significantly improves the performance of controller. Unlike conventional prediction methods [29], [30], proposed method has simple structure with linear model and offline coefficient calculations.

According to equations (25) and (26), five variables (V_d , P , Q , P^* , Q^*) have been used. These variables are classified into reference, measured and control categories. Since sampling frequency is much higher than the grid frequency in APFs, grid voltage variations can be considered as a linear approximation in one sampling period. So, V_d is estimated by means of k th and $(k - 1)$ th samples for next period:

$$v_d(k + 1) = c_0 v_d(k) + c_1 v_d(k - 1) \quad (27)$$

Measured parameters $P(k + 1)$ and $Q(k + 1)$ are estimated from equations (21) and (22) using current (k th) values. Since

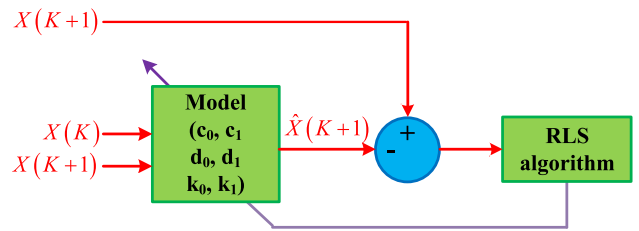


FIGURE 3. The structure of estimation procedure of prediction coefficients.

these estimations are extracted from real model of the system, it is expected to have minimum prediction error.

Reference powers in APF include low frequency variation of load current and consequently, load powers. Therefore, linear approximation can be utilized to predict power references:

$$P^*(k + 1) = d_0 P^*(k) + d_1 P^*(k - 1) \quad (28)$$

$$Q^*(k + 1) = k_0 Q^*(k) + k_1 Q^*(k - 1) \quad (29)$$

Now, the problem is to find the prediction coefficients (c_0 , c_1 , d_0 , d_1 , k_0 , k_1). The estimation procedure of the prediction coefficients used in (27), (28) and (29) is depicted and illustrated in Fig. 3. These values are obtained offline by recursive least square (RLS) algorithm based on different loading condition. For grid voltage estimation, a set of voltage values are used to estimate next sample. Afterward, according to the real value and estimation error, the coefficients are changed. Since the error estimation is used to revise the coefficients, the accumulation error is avoided, definitely.

For reference power estimation, the set of data under different loading conditions (25%, 50%, 75% and 100%) are used for coefficients estimation which result in high accuracy estimation for different condition.

Since these values are calculated offline, not only the prediction method does not impose high computational burden but also, it has very simple structure as well as good accuracy. Consequently, the proposed DB-Based DPC with prediction algorithm will imply high performance controller. General structure of the proposed DB-Based DPC with delay compensation is depicted in Fig. 4.

IV. SIMULATION RESULT

Simulation tests have been performed to validate the proposed control method and investigate its effectiveness by means of MATLAB simulation. The system parameters are listed in Table. 1.

It is worth to mention that almost all the implementation limitations such as sampling effect, control delay, deadtime and quantization effect are included in the simulations. Fig.5 shows the performance of SAPF with the proposed control method including grid voltage and current, load current, SAPF current and DC link voltage. Accordingly, the load currents are highly harmonic polluted, but the SAPF effectively compensates the harmonics. In addition, synchronized grid voltage and current ensures complete

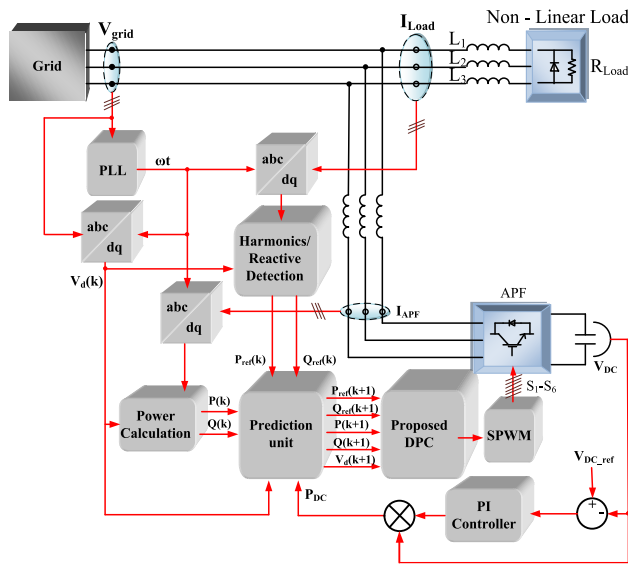


FIGURE 4. The structure of the proposed DB-Based DPC with delay compensation algorithm.

TABLE 1. The system parameters.

Grid Voltage (Vs)	70V(rms)
Grid Frequency	50Hz
Series Inductor Filter (L_f)	1mH
Series Resistance (R_f)	10m Ω
DC-Link Capacitance (C)	2200uF
Switching Frequency	10kHz
Sampling Frequency	10kHz
K_p (DC-Link controller)	2
K_i (DC-Link controller)	10
c_0, c_1	2,1
d_0, d_1	2,1
k_0, k_1	2,1

reactive power compensation with unity power factor. Also, the DC-Link controller effectively regulates and maintains the DC voltage at desired value with very low ripple (<0.25%). Based on this figure, it is evident that the injected current ripple is low compared to the peak grid current. It is worth to mention that the maximum permitted current ripple is assumed about 25% of peak grid current to both satisfy low current ripple and high dynamic response and current compensation at sharp and sudden load changes. The FFT analysis of the grid current without and with SAPF operation are depicted in Fig. 6. The grid current THD% is decreased from 21.59% to 1.68% in which dominants 5th and 7th harmonic orders are highly attenuated.

The power analysis of SAPF covering active and reactive load power, grid power and APF power are shown in Fig. 7 in the same timeframe, respectively. It is worth mentioning that in dq domain analysis the variables with grid frequency are DC. When the grid currents contain harmonic components which have multiple grid frequency, this parameter have both DC and oscillating components. Therefore, the active and

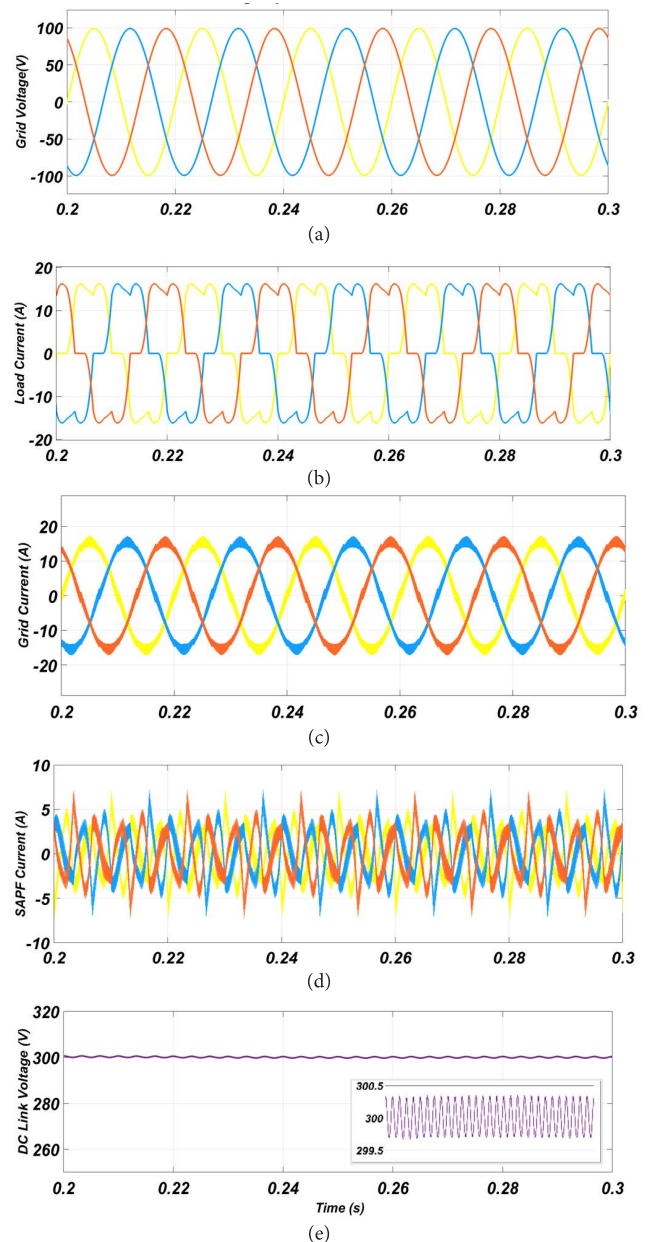


FIGURE 5. Performance of SAPF with proposed control method: a) Grid voltage, b) Load Current, c) Grid current, d) APF current, e) DC link voltage.

reactive powers which is the production of voltage and current will have oscillating components, too.

As it can be seen from Fig. 7(c), the high amplitude active power oscillation of load is highly compensated by SAPF at grid side results in sinusoidal grid currents. On the other hand, reactive power absorbed from grid is minimized to almost zero in order to have unity power factor.

To evaluate the dynamic response of the proposed method, sudden activation of SAPF harmonic and reactive compensation is conducted and the results are shown in Fig. 8. Clearly appears that the control methods track the changes and compensation immediately with very low delay in range

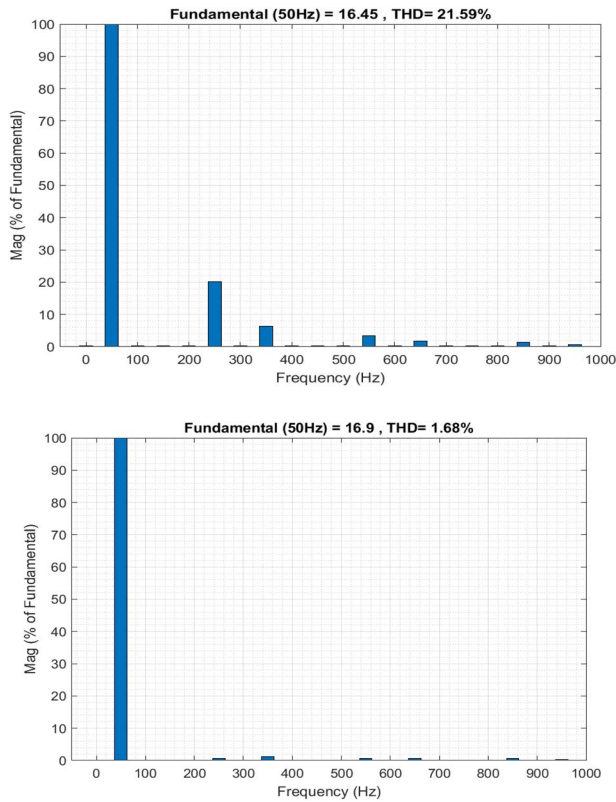


FIGURE 6. FFT analysis of the grid current a) without and, b) with SAPF operation.

of few milliseconds. This validates high dynamic response of the proposed control method. Also, Grid reactive power is compensated quickly as SAPF start operation.

For further dynamic response investigation of SAPF, load changes from 100% to 50% in $t = 0.3s$ and after in $t = 0.45s$ from 50% to 100% and the results are depicted in Fig. 9. SAPF controllers have appropriate dynamic response under load changes. As a result of SAPF dynamic behavior, normal 3% undershoot and 5% overshoot are observed in DC link voltage while the compensation is performed very fast (below 3ms). In addition, power description under this test is also added in Fig. 10 in which the simulation results clarify the high dynamic reactive power compensation of proposed control method. It is worth mentioning that very low power ripples related to the very low harmonic switching ripples in grid currents which is unavoidable.

Since the SAPF is connected to the grid at PCC, the grid voltage may meet some non-ideality conditions such as voltage drop or unbalanced condition which will affect the SAPF performance. Hence, simulation results under one phase voltage drop as well as unbalanced condition is conducted, and the results are shown in Fig. 11. Phase ‘a’ is 20% decreased at instant 0.3s and come back to normal condition at 0.4s.

Accordingly, the proposed control method compensates the harmonic components and provide sinusoidal current.

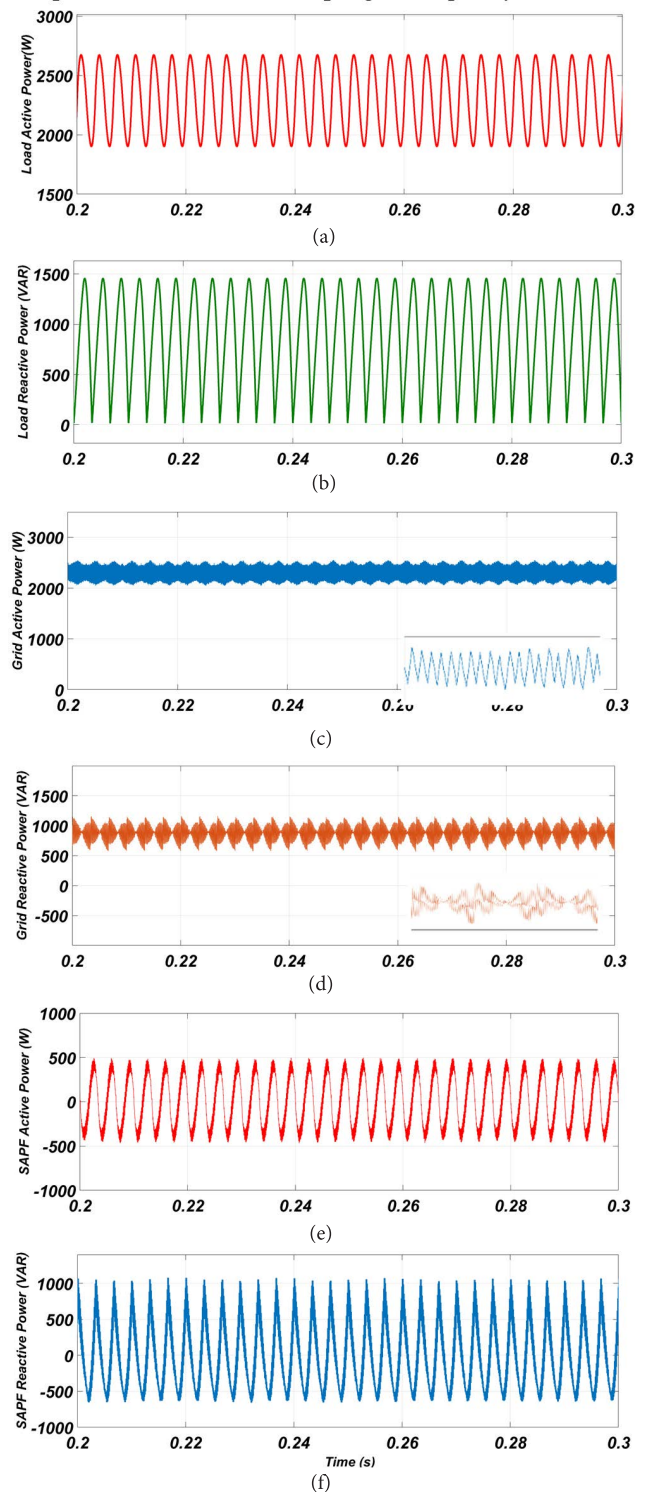


FIGURE 7. Power analysis of SAPF with proposed control method: a) Load active power, b) Load reactive power, c) Grid active power, d) Grid reactive power, e) APF active power, f) APF reactive power.

However, unbalanced grid current condition is existed where the DC-Link voltage experiments some low fluctuation. But, the controller performance is still maintain its normal operation.

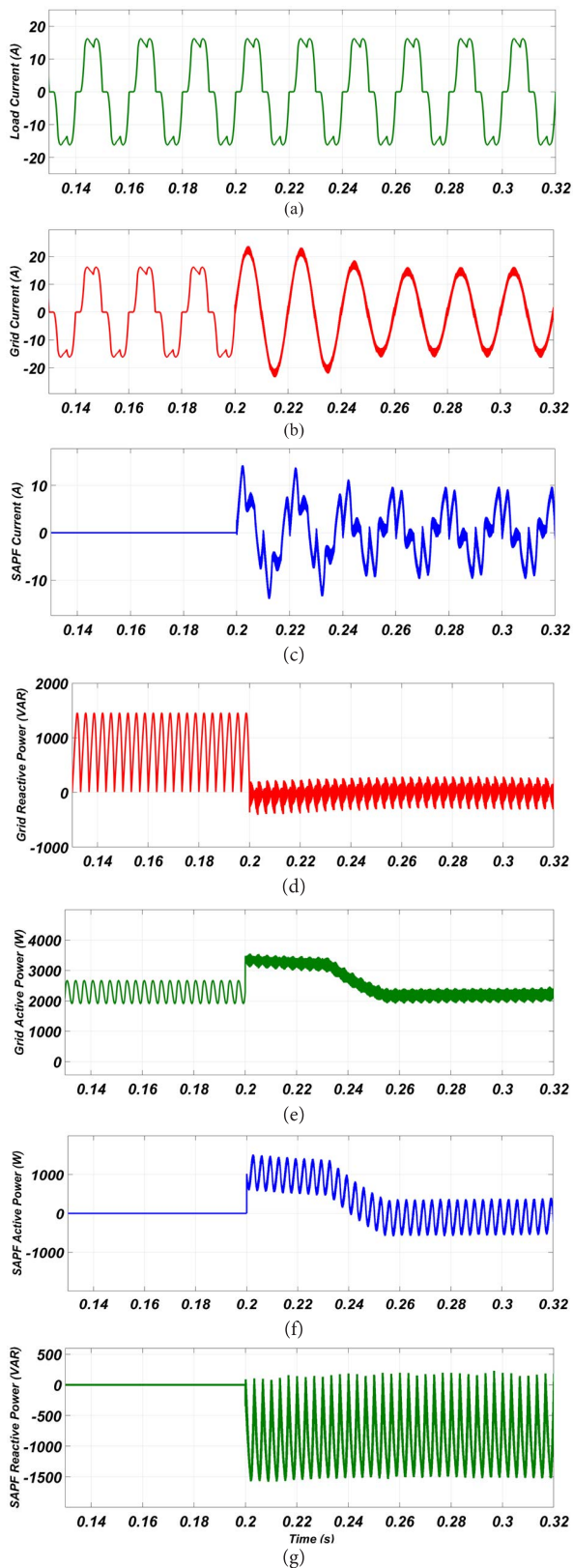


FIGURE 8. Performance of SAPF with proposed control method at SAPF startup operation in $t = 0.2s$: a) Load current, b) Grid current, c) APF current, d) Grid reactive power, e) Grid active power, f) SAPF active power, g) SAPF reactive power.

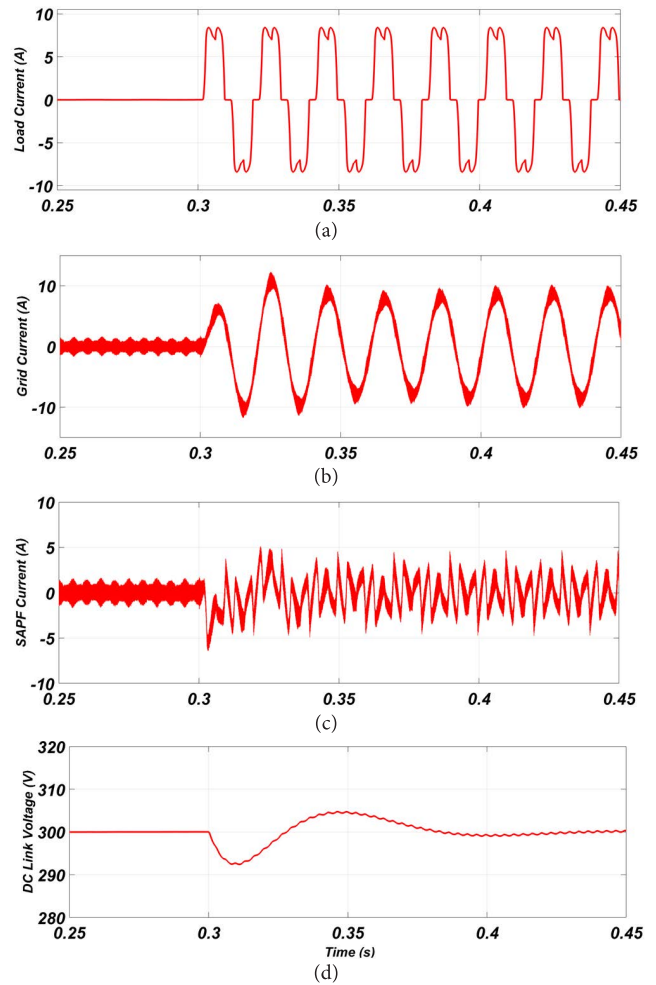


FIGURE 9. Performance of SAPF under load change from 100 to 50% and vice versa at $t = 0.3s$ and $t = 0.45s$. (a) Load current, (b) Grid current, (c) APF current, (d) DC link voltage.

V. EXPERIMENTAL RESULT

To verify the effectiveness of the proposed control method and to validate the simulation results, a prototype of three-phase APF is built, as shown in Fig. 12. The control system is implemented through DSP TMS28F335 from TI. The power semiconductors are SKM100GB12T4 with prototype driver is used as the main control board. In addition, three phase diode bridge rectifier with output resistance load is used as nonlinear load. On the other hand, a LA55P LEM current sensors are used in order to measure line, load and SAPF currents. Also, voltage transformers are utilized to sense voltages.

Firstly, steady state performance of proposed DB-Based DPC with and without delay compensation are shown in Fig. 13. Accordingly, both methods show ability for both harmonic and reactive power compensation. The THD% of grid current which is quality factor shows tracking performance of the methods are 3% and 6.2% with and without delay compensation, relatively. However, without delay compensation not only precise compensation is not

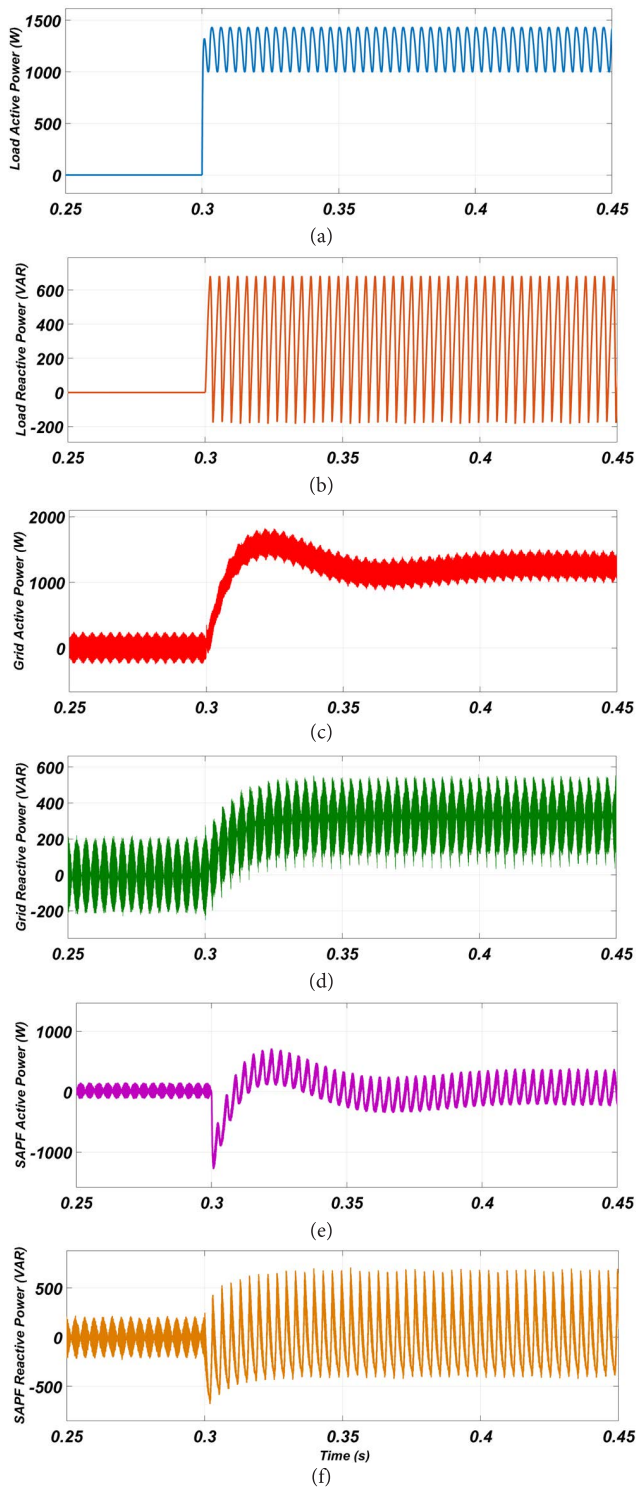


FIGURE 10. Performance of SAPF under load change from 100 to 50% and vice versa. (a) Load active power, (b) Load reactive power, (c) Grid active power, (d) Grid reactive power, (e) APF active power, (f) APF reactive power.

performed but also, the current ripple of the injected current and consequently grid current is higher. Hence, it can be concluded that the overall performance of proposed DB-Based DPC with delay compensation is very much

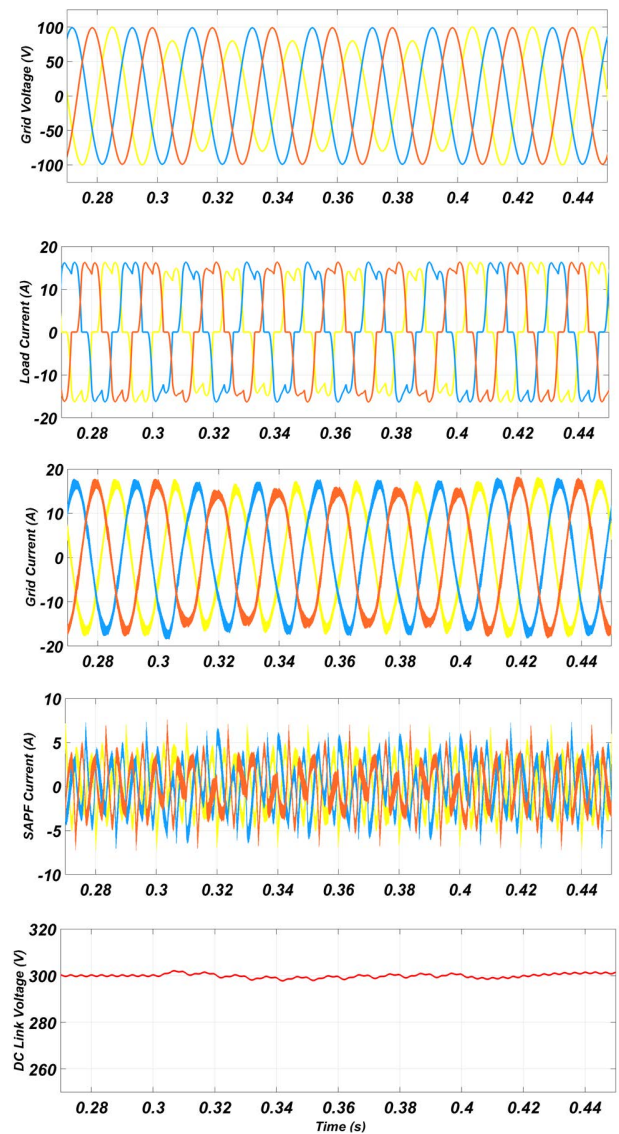


FIGURE 11. Simulation results under one phase voltage drop and unbalanced condition: a) grid voltage, b) load currents, c) grid currents, d) SAPF currents, e) DC-Link voltage.

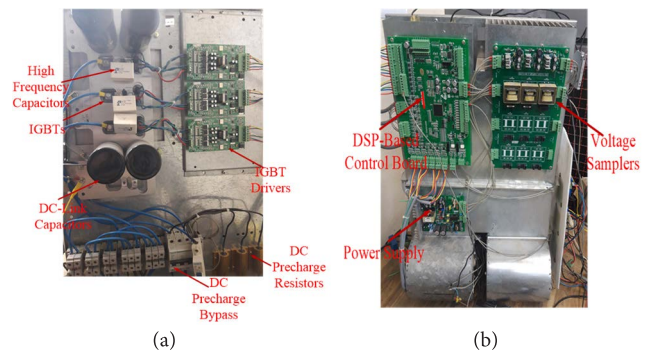


FIGURE 12. The graph of the experimental prototype: a) front view, b) back view.

improved. Thus, the performance of this method will be evaluated in the following.

The experimental results under steady state condition are shown in Fig. 14. For the brevity and clarity purpose only one phase signals are represented for some experimental results where other phase have the same shape but only proper phase shift, and they do not reflect additional information to be reported. These include load, grid and SAPF currents in which the load harmonics are precisely detected and compensated by the SAPF. Also, the reactive power is fully compensated which results in synchronized sinusoidal current with grid voltage. These results absolutely verify the performance of the proposed control method.

The harmonic components of the load and grid current after compensation with active and reactive powers are given in Fig. 15. It can be seen that THD% of grid current is improved by using proposed strategy in SAPF from 22% to 3%. This data is approved by FFT analyzer in Fig. 15 (c). Also, the power factor at grid side is improved and closed to 0.99. According to this fact that one step delay is eliminated from deadbeat controller, reference tracking is highly achieved which experimental results confirm this claim.

To better evaluate the performance of the proposed method, the results under transient response with 50% step change in the load are presented in Fig. 16. Accordingly, the controller identifies and compensates the reactive and harmonic components with few milliseconds (<5ms) delay. This ensures the fast transient response of the whole control system. It is worth mentioning that the transient response is decided by low pass filter in harmonic detection section and also, control system section. However, the low pass filter is implemented digitally with very low order and low cut-off frequency filters. Thanks to the high sampling frequency of the control system and low order of filters, the filtering delay and transient response is very low. Hence, it can be concluded that the transient response is mostly affected by the control system performance and filtering effect can be minimized.

The aging problem refers to the change of inductor and capacitor values over time, wearing out and increasing internal resistance, inductor value changes is inevitable. Hence, the robustness of the model-based control methods is one of the main challenges. The proposed DB-Based DPC control method is evaluated under model parameter mismatches. According to (26) and (27), the inductor filter value (L_f) is the main model parameter in the final control signals. Hence, the robustness of the proposed method should be evaluated with L_f mismatches. Accordingly, different variation from -40% to +40% in model are conducted and the THD% of the grid current and P.F at grid side as the main performance indexes are depicted in Fig. 17. As evidently appears, the THD% and P.F changes are very low and slight. This confirms that the proposed method is highly robust against model mismatches. Also, according to Fig. 9 and 10, the proposed method is robust against external disturbances even 50% step load changes.

To make a good comparison, the proposed method is compared with DPC-SVM based on super twisting sliding

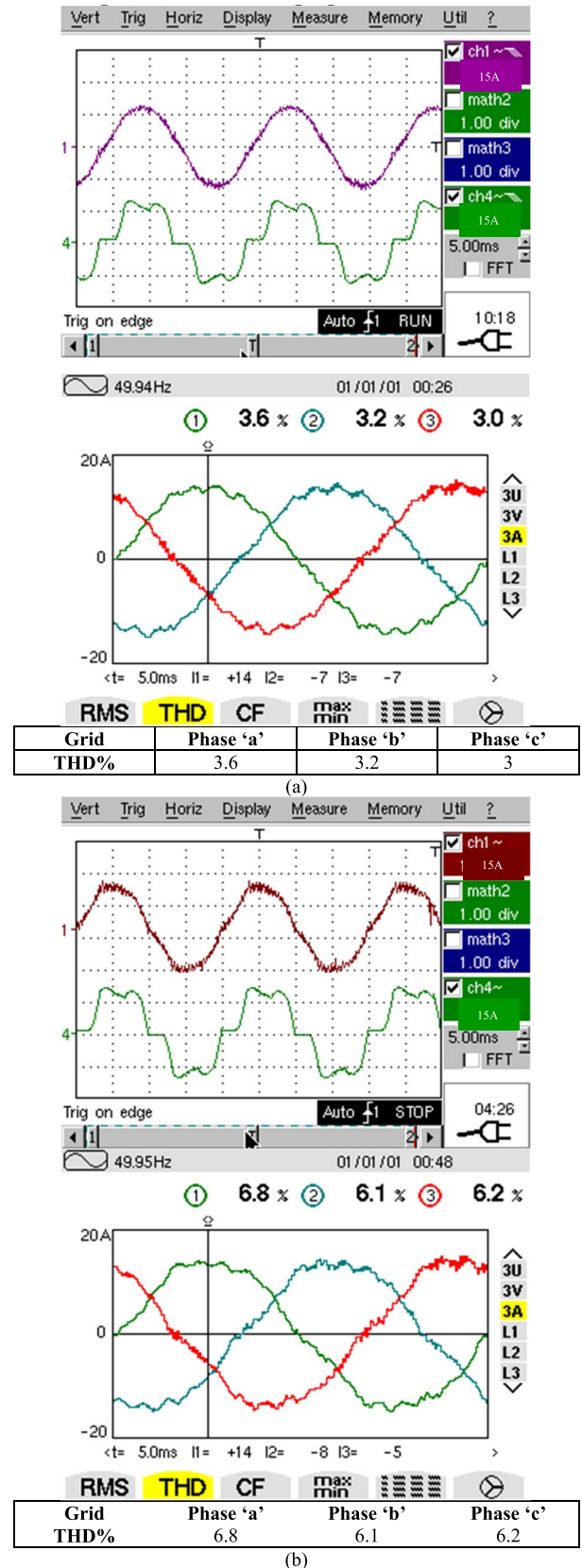


FIGURE 13. Performance of SAPF with proposed DB-Based DPC: a) with, b) without delay compensation; ch1:grid current, ch4: load current.

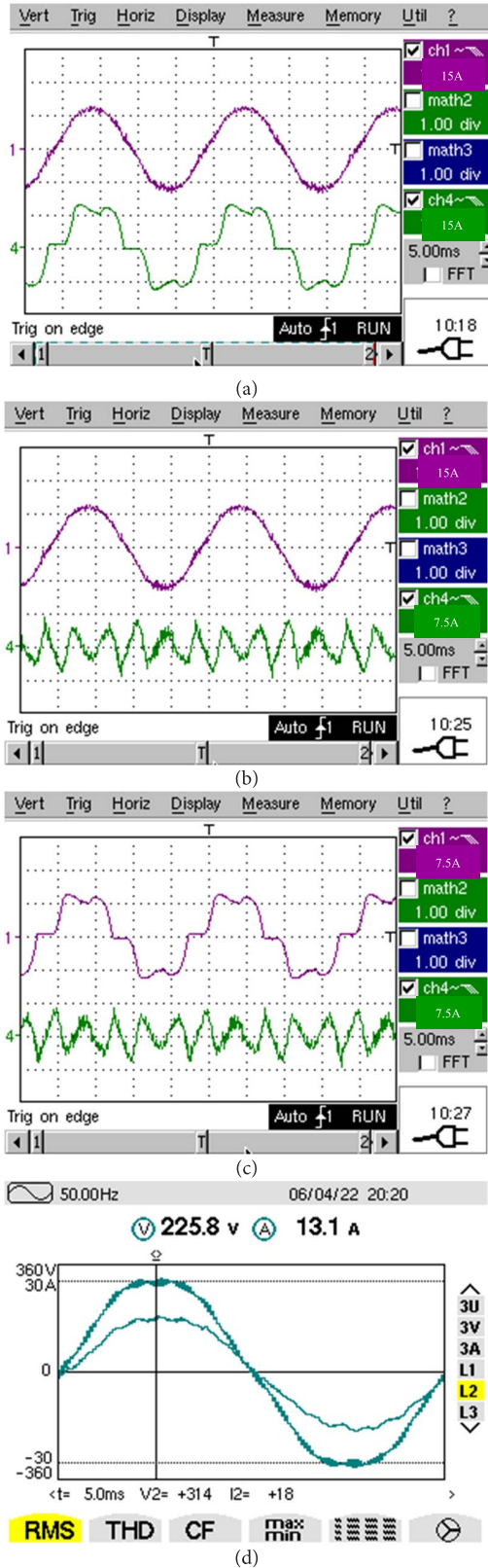


FIGURE 14. The experimental results of the proposed DB-Based with delay compensation under steady state condition: a) ch1: grid current; ch4:load current (15A/div), b) ch1: grid current (15A/div); ch4: SAPF current (7.5A/div), c) ch1: load current (15A/div), ch4: SAPF current (7.5A/div), d) Synchronized grid voltage and current.

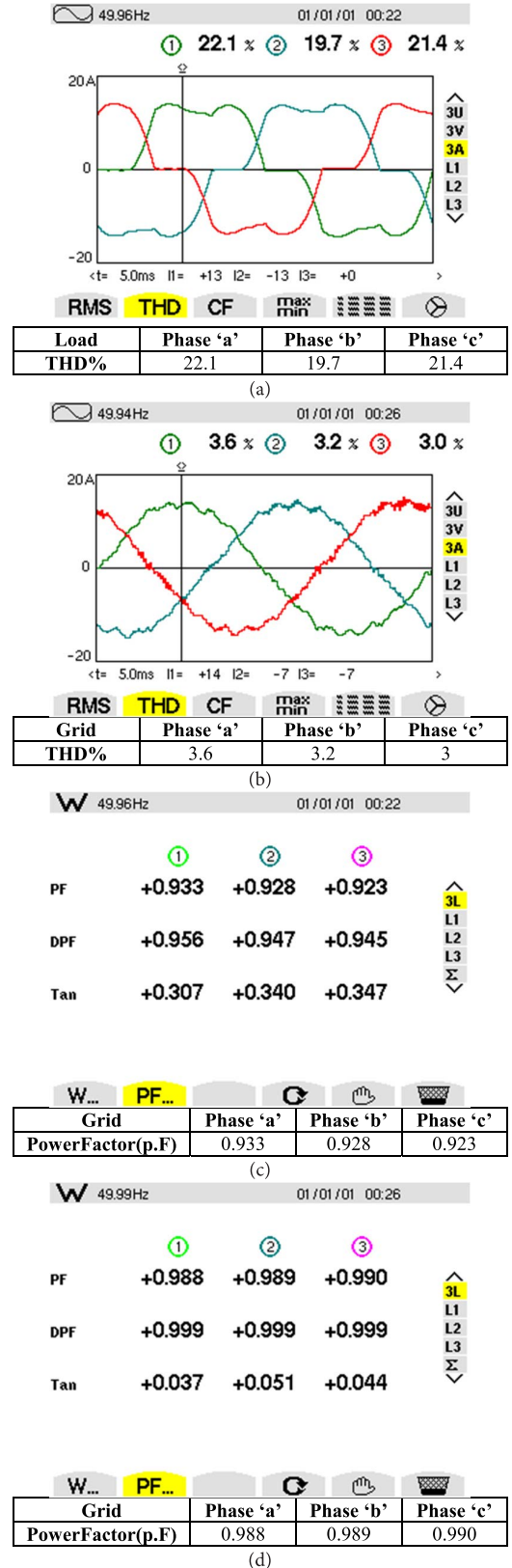


FIGURE 15. The Harmonic and power factor analysis: a) the THD% of load currents, b) the THD% of grid currents with compensation, c) the FFT analysis of the load and grid currents, d) the power factor at grid side for phase 'a'

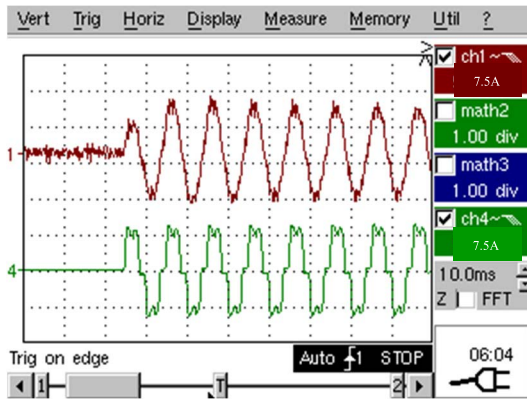


FIGURE 16. The performance under transient response with 50% rising load changes: ch1: grid current (7.5A/div), ch2: load current (7.5A/div).

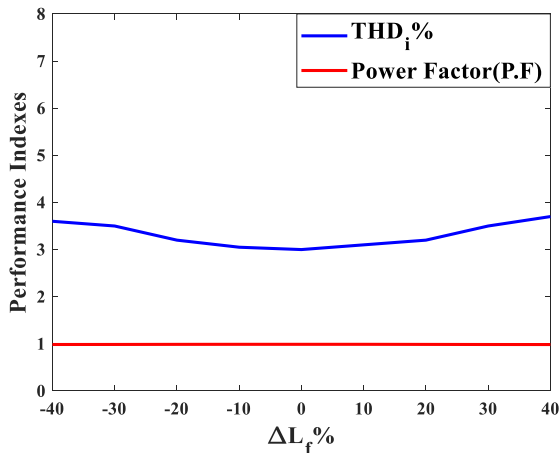


FIGURE 17. Robustness evaluation of proposed DB-Based DPC under model parameter mismatches (L_f).

mode control method [24]. This comparison is conducted through different performance indexes like THD%, P.F and two additional indexes defined as follow [24]:

$$\text{Integral Absolute Error(IAE)} = \int_0^t e(t)dt \quad (30)$$

$$\text{Power Ripple(rip\%)} = \frac{P_{\max} - P_{\min}}{P_{\text{avg}}} \quad (31)$$

It is noteworthy that the IAE is defined for SAPF output current while $rip\%$ is calculated at grid side. The comparison results are given in Table. 2.

Accordingly, the proposed method with lower inductor filter value not only provides lower THD% but also, it provides lower IAE which emphasize high reference tracking capability of the proposed method. Although both methods provide very high robustness against model parameter mismatches and external disturbances but, the structure of proposed method is evidently simpler. Furthermore, the chattering phenomena which is evident in grid current of [23] is not considerable as shown in Fig. 13. To sum up, the main benefits of the proposed method which are confirmed are simplicity, high robustness, good compatibility for digital

TABLE 2. Comparison results.

	Proposed DB-Based DPC without delay compensation	Proposed DB-Based DPC with delay compensation	DPC-SVM based on super twisting sliding mode control [24]
Grid Voltage (V)	70	70	53
Filter Inductor (mH)	1	1	1.32
Sampling Frequency (kHz)	10	10	10
Switching Frequency (kHz)	10	10	N.A
THD%	6.2	3	3.37
P.F	> 0.96	> 0.99	> 0.99
IAE	0.612	0.592	0.596
rip%	2.23	1.55	1.43
Robustness	very high	very high	very high
Complexity	simple	simple	high
Chattering effect	No	No	Yes

implementation providing low THD% and unity power factor at grid side.

VI. CONCLUSION

Harmonic pollution is one of the main challenges of power quality issue. Among different solutions, shunt active power filter (SAPF) can provide sinusoidal grid current at unity power factor. However, the control of SAPF is critical issue since it should detect and compensate the harmonic current simultaneously. A new DeadBeat(DB)-Based direct power control of active power filter was proposed in this paper. In addition, an enhanced and simple delay compensation is also proposed. The simplicity, fast dynamic response and high robustness against model parameter mismatches are the benefits of the proposed method. Several simulation and experimental results were provided in which the THD% of the grid current decreased from 22% to 3% as well as full harmonic compensation. Also, model mismatched assessment confirmed high robustness of the proposed method. In addition, the IAE performance index show is decreased which validate better reference tracking. Hence, the superior performance of the proposed method is completely validated through these results.

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