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Hybrid silicon photonics DBR laser based on flip-chip integration of GaSb amplifiers and µm-scale SOI waveguides

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Abstract: The development of integrated photonics experiences an unprecedented growth dynamic, owing to accelerated penetration to new applications. This leads to new requirements in terms of functionality, with the most obvious feature being the increased need for wavelength versatility. To this end, we demonstrate for the first time the flip-chip integration of a GaSb semiconductor optical amplifier with a silicon photonic circuit, addressing the transition of photonic integration technology towards mid-IR wavelengths. In particular, an on-chip hybrid DBR laser emitting in the 2 µm region with an output power of 6 mW at room temperature is demonstrated. Wavelength locking was achieved employing a grating realized using 3 µm thick silicon-on-insulator (SOI) technology. The SOI waveguides exhibit strong mode confinement and low losses, as well as excellent mode matching with GaSb optoelectronic chips ensuring low loss coupling. These narrow line-width laser diodes with an on-chip extended cavity can generate a continuous-wave output power of more than 1 mW even when operated at an elevated temperature of 45°C. The demonstration opens an attractive perspective for the on-chip silicon photonics integration of GaSb gain chips, enabling the development of PICs in a broad spectral range extending from 1.8 µm to beyond 3 µm.

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1. Introduction

Photonics integration technologies are rapidly emerging as a major vehicle fostering a wide penetration of light-based solutions into an increasing number of applications, spanning from datacom to miniaturized systems for gas sensing, or lab-on-chip wearable devices for health monitoring. Currently, the key building blocks driving the majority of these applications exploit photonic integrated circuits (PICs) incorporating silicon photonic (SiPh) and InP-based chips. These are deployed either in hybrid and heterogeneously integrated platforms [1], or using the monolithic InP integration platform [2]. These PIC technologies are mature and have already found their place in volume applications, with datacom being the most important driving force so far [3]. Therefore, the vast majority of PICs deployed in applications operate at the traditional 1.3 µm and 1.55 µm telecom wavelength bands exploiting InP-based light sources. However, many other emerging applications, for example, sensing of atmospheric pollutants [4,5] or real-time monitoring of glucose levels [6] would require wavelength extension to reach the mid-IR wavelength region beyond 2.5 µm, where the spectroscopic techniques are more sensitive [7]. For the sake of generality, we should note that at the other end of the wavelength span (< 1.1 µm), where silicon is not transparent, the alternative integration approach makes use of silicon nitride (Si_3N_4) components (which are transparent in the visible region) and GaAs-based light

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emitters. In any case, both silicon and Si_3N_4 technologies require light sources realized using III-V optoelectronics technology.

For light generation between 2–4 µm, GaSb-based optoelectronics appears to be ideally positioned to address wavelength versatility using GaInAlAsSb/GaSb-based type-I quantum well (QW) laser diodes that can reach an emission wavelength up to 3.7 µm [8]. We should note that the performance of stand-alone GaSb-based laser diodes compares favorably to InP technology also at a shorter wavelength range owing to the reduced Auger recombination [9] and high waveguide confinement. Exemplary demonstrations include distributed feedback lasers at around 2-µm [10] or the more recent demonstration at 2.3 µm region [11]. The initial study of the flip-chip integration of GaSb light-emitting diodes at 2 µm has been conducted on a silicon mount [12], yet, the advantages of GaSb platform for light sources are far from being leveraged to silicon-on-insulator (SOI) waveguides. Hybrid III-V/SOI lasers exploiting GaSb-based reflective semiconductor optical amplifier (RSOA) for wavelength-conditioning [13] and laser stabilization [14] have been demonstrated around 2 µm. Moreover, we have recently demonstrated tunable hybrid lasers exploiting SiPh tuning elements at 2.5–2.6 µm window [15]. However, these demonstrations are based on end-fire coupling between the gain chip and SOI waveguides, which are placed on separate carriers for active alignment, thus lacking the essential integration features that make PIC technology so appealing, i.e. compactness, cost-effectiveness, and large-scale on-wafer integration. Some preliminary studies have addressed wafer bonding of GaSb type-I gain materials on Si [16,17]. However, the Fabry-Perot (FP) lasers realized with this technique still lack in performance and in general require more specialized process steps compared to flip-chip integration at the components level. Moreover, monolithic growth of type-I GaSb-on-Si has also been studied, and promising laser results have been obtained [18], but this approach lacks a proven path on how to build the optical connection between active and passive waveguides and requires significant development to prove its application readiness. We should also note that InP-based lasers can reach emission wavelengths up to 2.6 µm using type-II QWs [19], yet they have inherent band-gap engineering limitations limiting the design approach. Thus, heterogeneous integration of InP-based lasers has been reported only up to 2.35 µm [20]. Table 1. summarizes the integrated single frequency demonstrated lasers in 2–3 µm wavelength range using InP and GaSb optoelectronic chips.

Table 1. Integrated III-V/Si single-frequency lasers operating at 2–3 µm wavelength range

Integration scheme	III-V material	Operating wavelength	Main disadvantage
Hybrid flip-chip	GaSb type-I	2 µm [This work]	• Early demonstration phase
End-fire on separate carriers	GaSb type-I	2 µm [13,21], 2.6 µm [15]	• Low integration density
Heterogeneous	InP type-II	2.3 µm [20,22]	• Wavelength limitation

In this work, we deployed a flip-chip integration approach to demonstrate for the first time an on-chip GaSb/SOI distributed Bragg reflector (DBR) laser. The 3D schematic of the flip-chip integrated hybrid DBR laser is shown in Fig. 1; it comprises a RSOA end-fire coupled with a thermally tunable DBR grating fabricated on SOI.

From a general perspective, the work aims at demonstrating the capability of GaSb/SOI technology for fabricating on-chip lasers for PICs, addressing applications up to 3.7 µm (maximum wavelengths demonstrated for type-I GaSb-based QW lasers). The stringent requirement of alignment accuracy to achieve low coupling loss between GaSb and SiPh waveguides is relaxed by exploiting 3µm-thick SOI waveguide technology, where mode size is readily matched without using a spot size converter (SSC) [23]. This integration approach has been widely used for hybrid external cavity DBR lasers demonstrated around telecom wavelengths using InP gain blocks [23,24]. We should also note that while the alternative evanescent coupling technology is well established at telecom wavelengths, the waveguides used should allow the optical mode to

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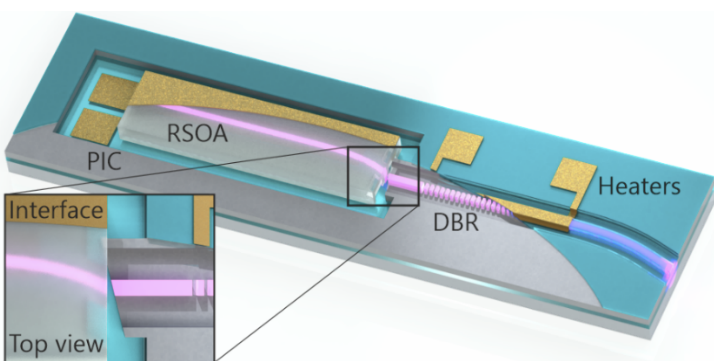

Fig. 1. 3-D model of the hybrid integrated DBR laser based on flip-chip integration and end-fire coupling between RSOA and SOI waveguides. The inset shows the top view of the optical interface between the waveguides.

partially propagate outside the waveguide layer. This is problematic at mid-IR because the SiO_2 claddings used in major integration platforms are lossy. The use of µm-thick SOI waveguides beyond 2 µm is more favorable in terms of transmission losses compared to the more conventional sub-micron SOI waveguides due to enhanced mode confinement in the thick Si waveguide. This helps to significantly reduce the losses at wavelengths beyond 2.5 µm originating from the SiO_2 cladding [25]. For technologically mature alternatives to SOI, only Si_3N_4 appears to be a suitable choice [26]. In fact, Si_3N_4 may exhibit low propagation losses even at mid-IR, but unfortunately making waveguides with thickness greater than 800 nm remains challenging due to tensile stress associated with this technology [27,28]. This leads to similar wavelength limits as observed with the sub-micron SOI platform. Moreover, Ge-on-Si waveguides [29] or suspended Si-waveguides [30] allow SiO_2-free claddings, but their maturity level does not compete with SOI. The advantage of Ge-on-SOI is more evident for wavelengths beyond 4 µm where SiO2 loss increases more than one order of magnitude, becoming significant in micron-scale waveguides.

Besides demonstrating the capability of the on-chip DBR laser, we theoretically analyze the optical coupling between the GaSb-based gain chip and the SOI waveguide, proving the good mode-matching features. The GaSb chip has an optical axis height that matches with the SOI-waveguide when the GaSb chip is flip-chip bonded. The optical axis position is adjusted with etched trenches that support the chip on SOI when integrated. While operated at room temperature the laser allows wavelength locked emission at 1.985 µm with a continuous wave (CW) output power of 6.12 mW.

2. Optical interface design

The detailed hybrid DBR laser cavity architecture used in this work is shown in Fig. 2 (a) while relevant parameters are summarized in Table 2. The optical interface is designed to minimize the parasitic reflections that could otherwise deteriorate the DBR performance. For this, the III-V waveguide and SOI facet were tilted. In addition, the waveguide facets were anti-reflection (AR) coated to further suppress the residual reflections. This coupling configuration limits the minimum coupling gap achievable between the SOI and RSOA waveguides, as shown in Fig. 2 (a), with a possible detrimental impact on coupling losses. To alleviate this limitation, grooves were etched along the RSOA waveguide front facet to reduce the minimum achievable gap between the facets by allowing the chips to overlap.

The crux of the flip-chip integration platform pursued here is the ability to achieve high end-fire coupling efficiency between the III-V and SOI waveguides, which is essential for high-performance hybrid lasers. The RSOA ridge width and epitaxially grown waveguide thickness

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Table 2. Important parameters of the optical interconnection

RSOA waveguide tilt angle θ_{RSOA} (degree)	7
SOI facet tilt angle θ_{SOI} (degree)	10
RSOA waveguide width W_{RSOA} (µm)	Variable or 5
RSOA waveguide etch depth t_{RSOA} (µm)	2.076
RSOA epitaxial waveguide thickness t_{WG} (nm)	Variable or 130
SOI waveguide width W_{SOI} (µm)	2.6
SOI height h (µm)	3
SOI slab thickness e (µm)	1.8

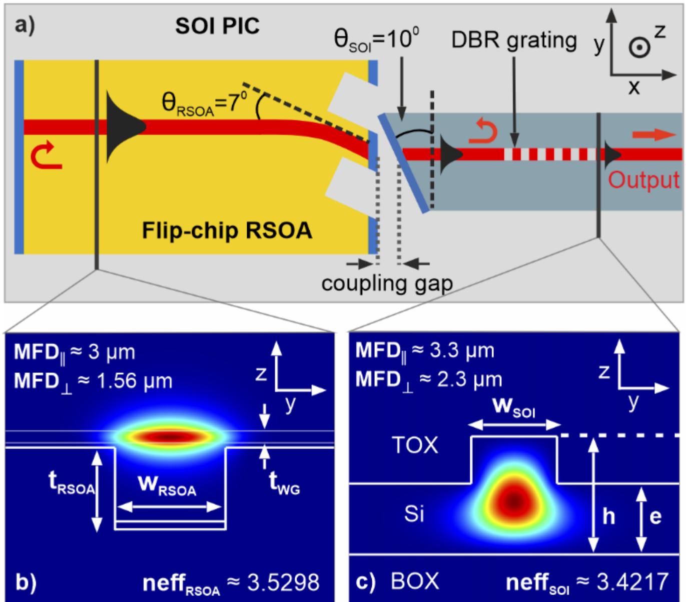

Fig. 2. a) Schematic of the flip-chip RSOA gain chip and SOI waveguide hybrid integration, and simulated 2D fundamental TE mode profiles of b) RSOA waveguide (W_{RSOA} = 3 µm, t_{RSOA} = 2076nm, t_{WG} = 130nm) c) SOI waveguide (h = 3 µm, e = 1.8 µm, W_{SOI} = 2.6 µm). neff = effective index of the TE mode, $MFD_{\perp}$ = mode field diameter vertical, $MFD_{||}$ = mode field diameter horizontal.

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were optimized to maximize the coupling efficiency and RSOA modal gain simultaneously. The SOI waveguide geometry had a thickness $h = 3\,\mu m$, and etch depth $e = 1.8\,\mu m$, while the waveguide width W_{SOI} was 2.6 µm to ensure a single TE-mode operation [31]. A finite-difference eigenmode (FDE) simulation was performed using Lumerical to analyze the mode mismatch loss between the RSOA and SOI waveguide modes; the results are shown in Fig. 3 (a). The simulation took into account the mode overlap between the RSOA and SOI waveguides assuming perfect alignment between both waveguides. Although such a low loss value may not be possible to achieve in practice, it is clear that the two waveguides have good mode-matching features. The mode mismatch loss is minimum when mode field diameter (MFD) is matched between both waveguides, as shown in the supplementary material. All the simulations in this work are performed at 2 µm wavelength unless otherwise specified. The quantum well confinement (QWC) factor, which in turn determines the modal gain, was also simulated using FDE and the results are shown in Fig. 3 (b). Based on this simulation model, we selected a waveguide thickness $t_{WG}$of 130 nm and ridge width $W_{RSOA}$of 5 µm. For these values, we achieve simultaneously a low loss coupling (0.6 dB) and a high QWC factor (2.4%). The single-mode transverse-electric (TE) near-field distribution of the III-V and SOI waveguides for optimized waveguide parameters are shown in Fig. 2 (b) and (c). SOI waveguide geometry is fixed by the fab and its optimization is given in the supplementary material.

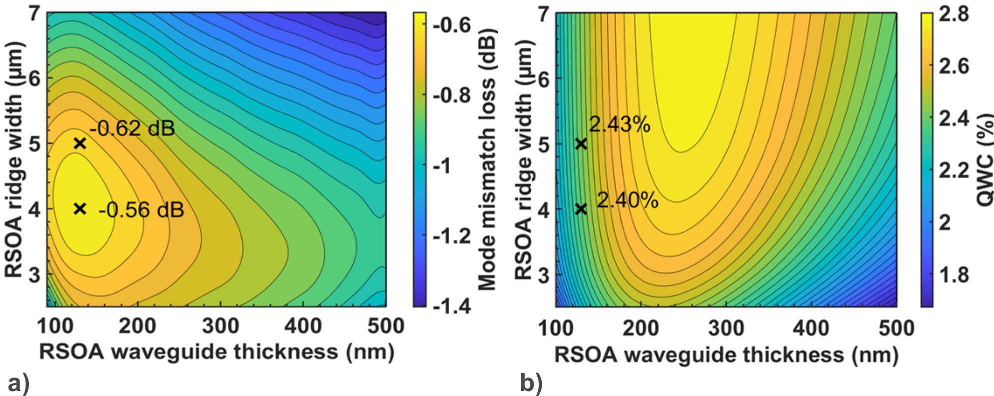

Fig. 3. a) FDE simulated mode mismatch loss (dB) between RSOA waveguide and SOI waveguide, assuming perfect alignment, and b) quantum well confinement factor (%) in RSOA, for varying RSOA epitaxial waveguide thickness and ridge width. SOI waveguide ($h = 3\,\mu m$, $e = 1.8\,\mu m$, $W_{SOI} = 2.6\,\mu m$) was fixed in a). Markers indicate the locations where mode-mismatch is minimum and the actual fabricated device.

The selected design was further analyzed using the Lumerical 3-D finite-difference time-domain (FDTD) solver. The fundamental TE mode field was launched from the tilted RSOA input waveguide and recorded at the tilted SOI output waveguide. The simulated insertion loss in Fig. 4(a) indicates that an increase in the coupling gap demands a y-shift to compensate for the misalignment caused by the tilted output beam from the RSOA. The minimum insertion loss of 1.8 dB is reported under perfect alignment conditions. The difference in the minimum insertion loss as compared to the case shown in Fig. 3(a) for the same ridge width is due to the fact that the FDTD propagation simulation considers the losses related to the reflection and waveguides tilt. The SOI tilt angle of 10° used in this work is not optimized and improved coupling efficiency is expected for 7° (shown in the supplementary material). The simulation in Fig. 4(b) shows that, with the given interface, the residual reflection could be suppressed up to 55 dB, which is paramount for narrow line-width lasers. In Fig. 5, the simulated misalignment loss in all axes reveals the stringent requirement for tight alignment accuracy. The coupling

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loss increases by additionally 1 dB from the minimum value with a misalignment of 0.97 µm in the horizontal direction, 0.45 µm in the vertical direction, and 1.46 µm along the x-axis. Given the state-of-the-art alignment tool used in this work, a sufficiently large misalignment tolerance should be possible. Hence, to achieve a low-loss optical coupling with the flip-chip bonding configuration, both mode-field matching at the interface and highly precise alignment of waveguides are crucial.

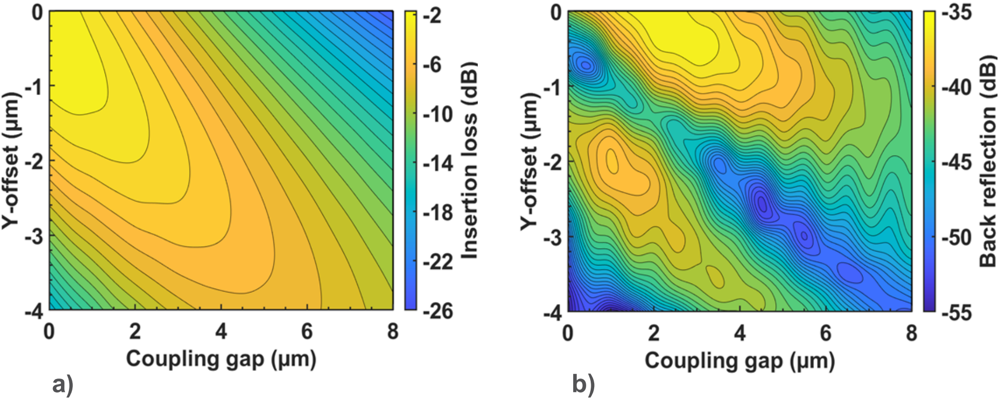

Fig. 4. a) 3D-FDTD simulation of insertion loss (dB) dependence on coupling gap and y-offset and b) back reflection (dB) as the function of coupling gap. Each data point in (b) corresponds to the optimum y-position where the insertion loss is at a minimum.

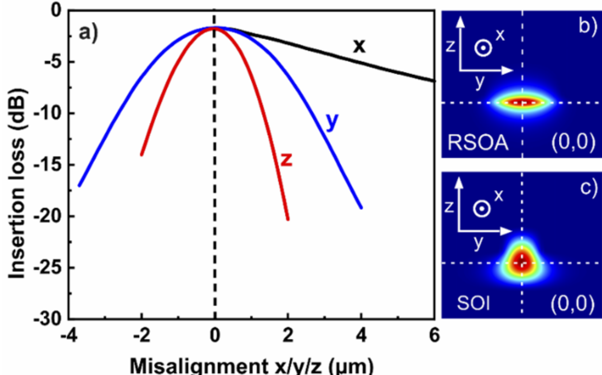

Fig. 5. a) Simulated SOI chip-RSOA insertion loss as a function of misalignment (x/y/z), b) near-field distribution of the TE mode in the RSOA, and c) SOI waveguides on the y-z plane.

3. RSOA fabrication and superluminescent properties

The epitaxial structure of the RSOA was grown on a (100) n-GaSb substrate via molecular beam epitaxy (MBE). The structure was similar to the one used in the Refs. [32,33] for the state-of-the-art superluminescent diodes. However, contrary to the high-power devices reported previously, the PIC integration limited the length of the gain chip to 1 mm. The wafer was afterward processed into a ridge waveguide (RWG) geometry. The ridge was defined using UV-lithography and inductively coupled plasma (ICP) dry etching. Simultaneously, etched flip-chip alignment marks were created during this step that is automatically aligned in relation to the waveguide. A similar dry etching step was subsequently used to define the features facilitating

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the high-precision integration: *1) the etched trench that is used to fine-tune the optical axis vertical alignment (z-axis),* and *2) the grooves surrounding the waveguide to allow the SOI waveguide to overlap with the RSOA facet for a minimal gap between the facets*. After the ridge etching, an insulating SiN layer was applied through plasma-enhanced chemical vapor deposition (PECVD). An electric contact window at the center of the ridge was defined by employing UV-lithography and reactive ion etching (RIE). Ti/Pt/Au ohmic contact was deposited on the p-side using electron beam evaporation. Afterward, the wafer was thinned down to approximately 140 µm and the backside Ni/Au/Ge/Au n-contact was evaporated on the sample. The wafer was cleaved into 1 mm long bars for the flip-chip integration. The rear and front facets were coated with high-reflection (HR) and AR coatings, respectively. For process validation and pretesting, chips from the same process were mounted on AlN-ceramic sub-mounts that were soldered to copper heatsinks. The design of the RSOA was based on the J-shaped ridge waveguide (RWG) geometry, where the front end of the RWG was tilted at an angle θ, to suppress the lasing, while the back end was left perpendicular to the facet to form a double-pass cavity. The tilt angle ($\theta = 7°$) was optimized, to reduce the fundamental TE mode reflection, for a smooth broadband gain spectrum.

The RSOAs were characterized under CW operation by measuring power-current-voltage (L-I-V) characteristics using a Thorlabs PM400 photodiode-integrating sphere (PIS), far-fields (using an in-house setup), and spectra Yokogawa 75 optical spectrum analyzer (OSA). Without an external optical input, these devices operate in a superluminescent mode. The results are summarized in Fig. 6. The measured L-I-V curve at room temperature and 45°C recorded the power up to 20 mW and 4 mW from the front facet. The room temperature spectra measured at different currents exhibit redshift in the range 1928–1985nm, with the full-width-at-half maximum (FWHM) in the range 61–71 nm. The stable slow- (divergence ~ 24°) and fast-axis (divergence ~ 51°) far-field (FF) of the same device at varying currents are shown in Fig. 6 (c). These characteristics confirm the suitability of this RSOA as an III-V gain chip for high-performance hybrid lasers.

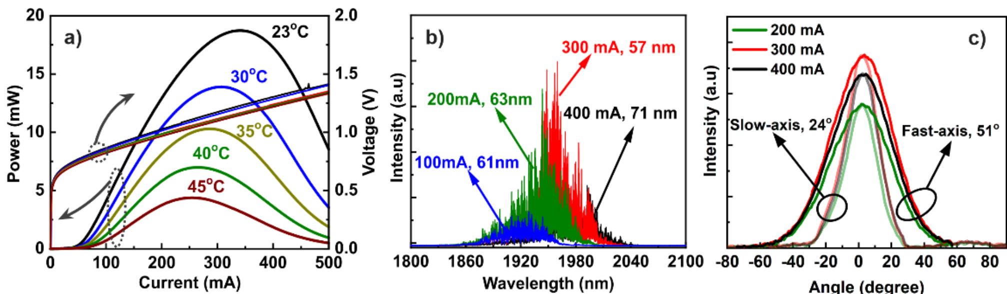

Fig. 6. a) ILV at different temperatures, b) Room temperature spectra at different currents, and c) FF at different currents.

4. Hybrid laser integration and testing

The RSOA was flip-chip bonded on the SOI platform using a commercial photonics integration line. For improved thermal conductivity, RSOA was rested on the recess etched through buried oxide up to the Si substrate. The electrical contact between RSOA and SOI was formed through AuSn contact pads on the SOI, which correspond to the p-contacts on the RSOA. The correct z-alignment between the chips is determined by the etched trenches on the RSOA with corresponding contact sites on the SOI. The etched grooves meant to minimize the x-axis gap between the facets suffered from insufficient etch depth and the minimum gap condition was

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not met, leading to an increase in the x-axis coupling loss. y-axis control depends on the etched alignment marks created for the integration tool. However, as the RSOA waveguide is tilted, the alignment mark's relative position to the facet changes when the facet location changes. Due to the limited accuracy of the dicing tool, the final facet position is not well defined, thus also affecting the alignment mark accuracy. Due to the above-mentioned constraints, we were able to estimate the misalignment along the x-axis only. The misalignment was observed to be 4 µm through scanning electron microscope imaging, which translates to ~5 dB coupling loss based on the estimation shown in Fig. 5 (a).

The hybrid laser was placed on a thermoelectrically cooled heatsink, and CW current was injected into the laser with needle probes. The output power was measured with a Thorlabs PM400 PIS, and the spectrum was measured by edge coupling the laser with a multimode (MM) fiber into Yokogawa 75 OSA. The output power of the hybrid laser as a function of injection current at different operating temperatures is shown in Fig. 7 (a). The maximum output power of 6.12 mW was achieved at 23°C with an injection current of 352 mA, and the output power of 1.55 mW at 45°C was achieved at an injection current of 225 mA. The maximum wall-plug efficiency and the slope were measured up to 2% and 0.03W/A. The laser series resistance was measured to be around 1Ohm.

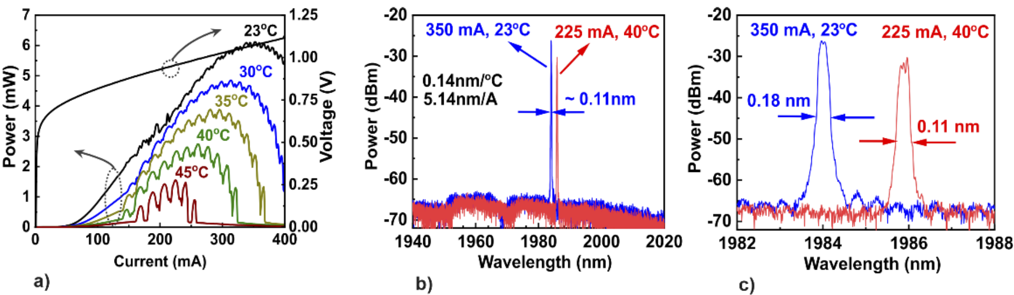

Fig. 7. (a) Output power and forward biased voltage of the hybrid laser as a function of the injection current at different operating temperatures. b) extended view and (c) close-up spectra of the hybrid laser at two different temperatures at currents giving the maximum output powers.

The oscillations in the output characteristic are caused by the laser locking into the DBR mirror: at the peaks, the cavity mode matches the resonance peak of the DBR, and in the dips, there is a maximum mismatch between the cavity mode and DBR resonance. The height of the modulations seems to increase with increasing operating temperature. In addition, the onset of the oscillations moves to a lower injection current value. This is because the peak of the RSOA gain is red-shifted closer to the DBR resonance, as the laser is heated, increasing the gain and decreasing the threshold current that is achieved when the cavity mode is aligned to the DBR resonance peak. Overall, the output power decreases at higher temperatures due to increased thermal losses in the RSOA.

Figure 7 (b) and (c) show the broad overview and closeup spectrum of the hybrid laser at 23°C and 40°C with an injection current of 350 mA and 225 mA respectively. The maximum wavelength at 23°C is ~1984nm with the FWHM of 0.18 nm and the single-mode suppression ratio (SMSR) of 37 dB, whereas for 40°C the maximum wavelength is ~1986nm with the FWHM of 0.11 nm, which corresponds to a slope value ~0.14 nm/°C. The emission wavelength is close to the nominal resonance wavelength of the DBR, meaning that the hybrid laser is locking to the DBR even with a relatively large detuning. The shift in wavelength is caused by the increased effective index of the DBR due to increased temperature. The difference between the optical signal strength of Fig. 7 (b)/(c) and Fig. 7 (a) was due to the fiber-to-chip and fiber-to-spectrum

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analyzer coupling loss. The lasing wavelength tuning was also performed by driving the DBR heaters through applied voltage for the fixed RSOA bias current of 340 mA. The peak wavelength was tuned between 1983nm – 1990nm, as shown in Fig. 8, where the maximum wavelength tuning was limited by the DBR response. The SMSR in the range of 32 dB – 37 dB was measured in the entire tuning range.

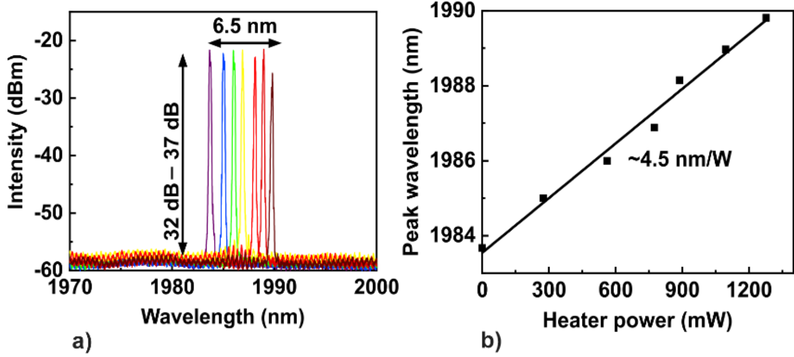

Fig. 8. (a) Lasing wavelength spectrum and b) peak lasing wavelength as a function of DBR heater power. The heater is tuned such that the peak wavelength spacing is 1nm.

5. Conclusion

Chip level integration between a µm-scale SOI and GaSb type-I QW waveguide was demonstrated by a flip-chip mounting technique. The realized hybrid DBR laser emits at around ~2 µm with slightly more than 6 mW CW output power. Peak lasing wavelength tuning by incorporated heaters was demonstrated between 1983nm to 1990nm. Simulation reveals that the use of the µm-scale SOI platform could enable optical interface losses as low as 0.6 dB without additional spot-size converters and when perfect alignment conditions are met. However, for successful integration, high precision control of the x-, y- and the z-axis is imperative. To match this condition, etched features for improved x, y, and z-axis alignment control were utilized. The precision for z-axis control was assessed to be sufficient, while x and y axes alignment control requires further improvements. The low insertion-loss and strong mode confinement in the µm-scale SOI waveguide open the access to a window of more exotic wavelengths (2–3.5 µm) for spectroscopic and healthcare applications, while using on-chip integration.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental document. See Supplement 1 for supporting content.

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