Power Electronic Converters Simulation Model Verification for Grid Code Compliance Testing

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***Abstract*— With increasing the diffusion of Power Electronic Converters (PEC) in modern and smart grid systems, the academic and industry R&D researchers rely more and more on the accurate and efficient modelling and simulation of PECs for both hardware and controller design. This paper focuses on the PEC simulation model verification for (time consuming and costly) grid code compliance tests. The simulation model developed based on a full-power laboratory test bench and the waveforms of fault ride through (FRT) tests were compared. The results show that the modelling approach based on averaged inverter captures the dynamic behavior with a good accuracy. Hence, the dynamic behavior of the inverter in FRT tests can be assessed using the simulation approach saving the time and cost required by full power testing.**

Keywords—Power Electronic Converter, Grid Code, Simulation Model, Fault Ride Through.

I. INTRODUCTION

Recently the number of Distributed Energy Resources (DER), including Renewable Energy Resources (RES), High Voltage Direct Current (HVDC) applications and Flexible Alternating Current Transmission System (FACTS) devices in the power grid have been increased significantly and it tends to increase even more in upcoming years [1, 2].

This implies the importance of Power Electronics Converters (PEC) used for control, management and grid integration of these energy resources and control apparatuses. Already today the number of PECs in power systems is high and it is expected that, future modern and smart grid will need to host much more PECs in different voltage levels and power range. In this regard, academic and industry R&D researchers rely on the accurate and efficient modeling and simulation of PECs for both hardware and controller design [1].

Nonlinear nature of power electronic switching has been a big challenge from PEC simulation models accuracy and reliability point of view. Currently, there does not exist any standard method to deal with the nonlinearity of power electronic switching in simulation platforms. Therefore, new methods for modelling and dealing with nonlinearities including, iterative and non-iterative solutions, have been proposed and implemented [3, 4].

In order to study both transient and steady-state behavior of such systems, one needs to compromise between accuracy (time step) and the speed of the simulation. Different new topologies for PECs have been introduced (multilevel and cascaded converters) and the number of power electronic switching devices in the power system has also increased [5]. Therefore, detailed analysis of future power system with more complexity requires more powerful control and simulation tools in order to meet the requirements for speed and accuracy [3]. The simulation time frame of the interest can vary depending on the application from microseconds, associated with power electronics switching, to minutes or even to hours [6 - 8].

A PEC system consists of two main parts; the power circuit part and the controller part. Power circuit includes the power electronic switches (diode and thyristors/transistors), switching inductance and grid side LC-/LCL-filters, DC bus capacitor and, depending on the application, also grid side coupling transformer. The main challenge here is to model the switching components and verify the correctness and accuracy of the simulated model when compared to the real PEC system.

Controller part includes measurement and signal processing parts, which measures voltages and currents from the power circuit and interacts with digital processor through I/O ports. The main control is usually implemented in a Digital Signal Processor (DSP) from where the control actions and PWM signals are sent back to the power circuit. In this case, the main challenge is to verify the simulated controller responses in the real application and power circuit.

Real time simulator (RTS) offers great potential for analyzing and studying the behavior of PECs during different power system events (e.g. disturbances). It can be considered as a complementary tool for traditional offline PEC simulation programs [6]. Hence, with recent advancement in digital RTS systems, it is possible to accurately and efficiently simulate the power circuit interaction with the real controller for testing the system behavior with the controller hardware-in-the-loop (CHIL) configuration [9]. CHIL testing can substantially reduce the design and development cost, human resources, power consumption, and physical space, while providing safety to the actual equipment e.g. in case of malfunction of the controller [9]. CHIL testing is a well-established approach and has been widely used to test control platforms in research institutes and industry [10]. Power hardware in the loop (PHIL) is another versatile method which has been suggested in IEEE standard for DER units' conformance test [11].

In this framework, the modeling of the PEC is a particular challenge due to the high frequency operation and the required accuracy and precision considering the gating signals coming

from the digital controller [9]. In these systems, the accuracy (time step) is the main issue since speed of simulation should be in real time while providing the required accuracy to simulate the dynamics of the power system. Field-Programmable Gate Array (FPGA) has also a lot of potential and it is being used to decrease the time steps to the range of microseconds [12] in such system simulations. Otherwise, if implemented on CPU, the time step would be in the range of milliseconds [6].

When it comes to modelling of a system involving PECs, it is not practical to simulate entire system at very detailed circuit level because of the large computation time and huge amount of generated information which is difficult to be handled. Instead, the common approach is to simplify parts of the circuits to be able to focus on portion of the circuit which is of the interest [13]. Hierarchical five level simulation approach, which at first level starts from very detail model (only few cycles), in second level uses ideal switches for several cycles, and then in third level averaged PWM model with closed loop controller for tens of cycles is used. Fourth and fifth levels are dedicated for longer simulations purposes. This is a common approach to study different levels of system in transient and steady-state conditions [13].

Concerning the grid code compliance testing, only few works have been discussed the issues since the full power (or on-site) testing is the primary accepted mechanism, e.g. where the study results for wind turbine systems is reported in [14]. The main challenge that industry faces now is the time consuming and costly full power testing required for grid code compliance testing which due to versatile development in simulation tools and techniques can be performed with alternative methods saving the time and cost required by full power testing.

This paper focuses on the PEC simulation model verification for grid code compliance tests and proposes the possibility of using simulation model for grid code compliance testing. The laboratory test bench and the Device Under Test (DUT) are simulated in Matlab/Simulink Simscape toolboxes meeting the accuracy needed and achieving reasonable speed of the simulation model. Simulation model results are compared with the experimental results in order to verify the model.

The main contribution of the paper is to demonstrate that for the grid code compliance and performance testing, a very detailed simulation of the system is not required. Instead several simplifications can be done to reduce the complexity of the model keeping the simulation time and its accuracy within acceptable range. Especially the speed of the simulation (and time steps) is crucial for further improvement and implementing the simulation model on RTS for CHIL verifications.

The rest of the paper is organized as follows: Section II describes the experimental laboratory test bench and simulation model. Section III compares the results from laboratory experiments and simulations. Finally, conclusions are stated in Section IV.

II. Experimental Test Bench and Simulation Platform

Fig. 1 shows the simplified schema of the laboratory test bench implemented for grid code compliance testing. The voltage source connected to the primary winding of the transformer is a three-phase grid emulator based on voltage-source inverter technology. The grid emulator provides programmable voltage magnitude and frequency. For fault ride through (FRT) testing purposes it produces symmetrical and asymmetrical voltage sags without zero-sequence component as required in [15]. The DUT is connected to the secondary winding of the transformer and it is supplied from the DC bus system via a DC-DC converter which can be used to adjust DUT's DC bus voltage. The DC bus voltage of the test bench is regulated by the active rectifier supplied from the external network (see Fig. 1 Active front end – AFE converter). The test bench components are operated and programmed via a PC interface.

The DUT is a three-phase two-level inverter of 310 kVA rated power. An LCL filter is used as a line filter and the inverter switching frequency is 3.6 kHz. During the tests, the DC bus voltage of the inverter is adjusted at 1080 V by means of DC-DC converter depicted in the Fig. 1. The line voltage generated with the grid emulator is 690 V.

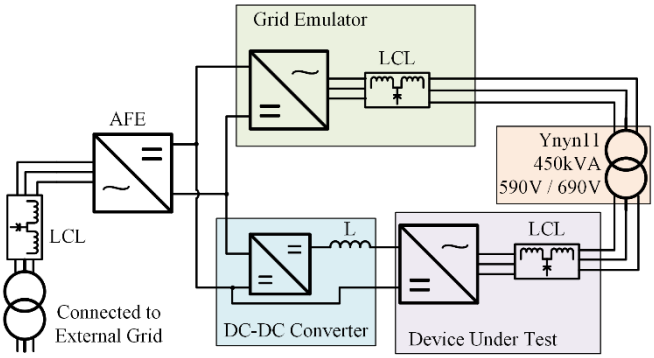

Fig. 1. Simplified schema of the test system.

The simulation model has been developed using Matlab/Simulink and Simscape toolboxes based on Fig. 1. The grid emulator was reduced to an ideal voltage source behind impedance and the DUT was supplied from a fixed DC voltage source (this simplification is verified later). The transformer was assumed to be linear and was simplified to a series impedance calculated based on its nameplate values. The passive circuit components were also modelled based on their nameplate values. All primary side elements were reduced to the secondary side. The hypothesis was that for dynamic simulations, the inverter can be modelled on the average basis without switching components and pulse-width modulated control signals. This simplification is valid in most grid compliance tests (e.g. active and reactive power capability, response to voltage and frequency disturbances and FRT response), since grid code test requirements usually provide rise time and the tolerance for short circuit current, FRT response and in most cases there is no information or requirements about the quality of the injected current by PEC [16].

Moreover, as it is reported in the literature and as a common accepted approach, network operators are using models that could represent the plant performance with sufficient accuracy and are simple and fast enough to be included in large network simulation runs [17]. In this regard, different software systems are being used with normally averaged model with time step in the range of milliseconds [17]. Hence, the inverter was modelled as controlled voltage source. The inverter control system and output control signals

were modelled in very detailed manner and were parametrized similarly as the DUT.

Details on the adopted control method is out of scope of this work, indeed the results can be expanded and validated to different PEC devices, other configurations, and systems with different ratings.

III. Verification of The Simulation Model with Experimental Results

The modeling accuracy is assessed by comparing the simulated waveforms with the experimental test data. First the experimental testing was carried out in the laboratory and the results were recorded using Tektronix DPO50XX oscilloscope, Tektronix P5200A differential voltage probes and CWT PEM Rogowski coils. Then the simulation model was initialized with same inverter settings and the AC voltage source was configured to produce fault voltages corresponding to the laboratory test. Finally, the time axes of experimental and simulated waveforms are shifted to coincide the fault periods.

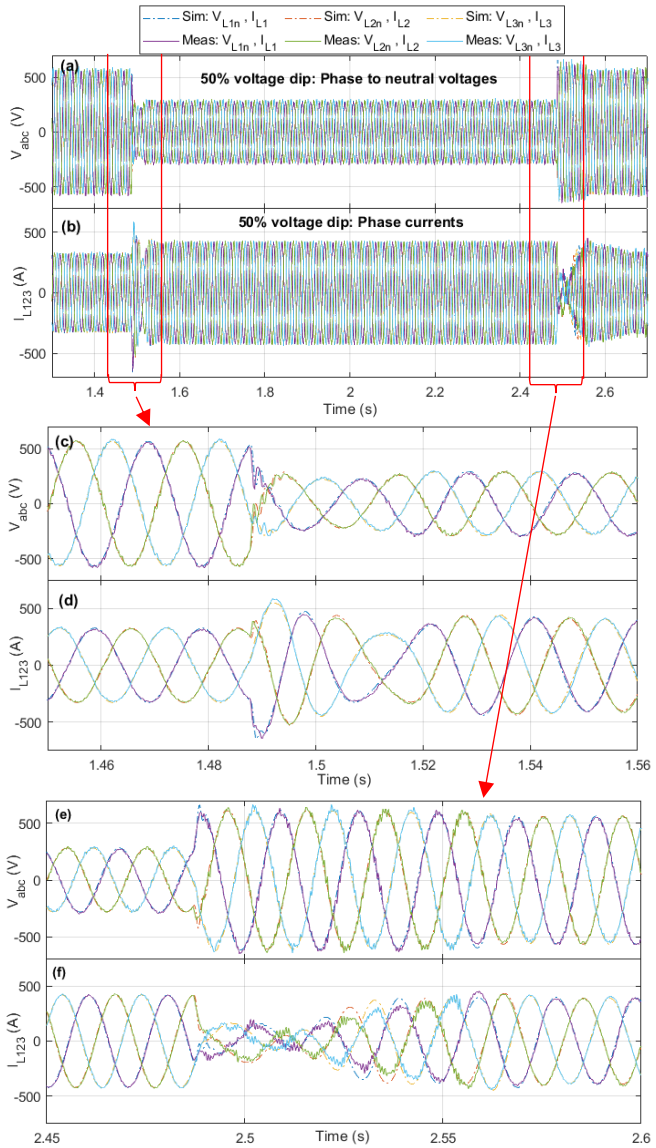

Fig. 2. Results for symmetrical 50% voltage sag under full inverter current (a), (b) phase voltages and currents whole event, (c), (d) phase voltages and currents for starting the 50% sag, (e), (f) phase voltages and currents for ending the 50% sag.

The waveforms of symmetrical 50% voltage sag under full inverter current are shown in Fig. 2, indicating that the model's response is closely similar to the experimental test.

Fig. 2(a), (c) and (e) depict that voltage waveforms of experimental and simulation tests match very well. Therefore, the simulation model can reflect the dynamics of the real test with very good accuracy. Concerning Fig. 2 (b), (d) and (f), which show the converter current waveforms, the results from experimental test and simulation model are in very good agreement during fault steady-state time which again is the proof that simulation model is valid and it can represent the experimental setup behavior.

However, during transients (during starting and ending of 50% voltage sag; Fig. (d) and (f) zoomed versions of Fig. 2 (b)), it can be noticed some deviations between current waveforms coming from experimental test and simulation model results. The mismatch can be specially noticed in Fig. 2 (f) which shows the currents during ending the 50% sag when the system recovers from 50% voltage sag.

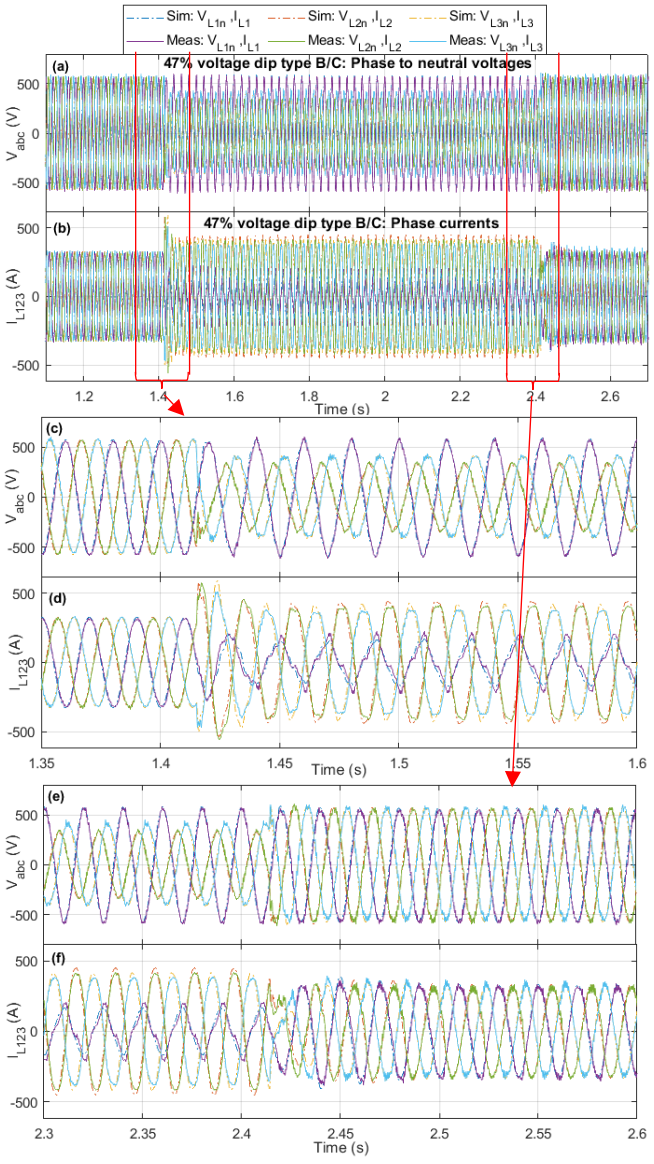

Fig. 3. Results for 47% asymmetrical voltage sag of type C (a) phase voltages, (b) phase currents, (c), (d) phase voltages and currents for starting the 47% asymmetrical voltage sag, (e), (f) phase voltages and currents for ending the 47% asymmetrical voltage sag.

Fig. 3 presents the results for a 47% asymmetrical voltage sag of type C [15]. Similar observation can be noticed having closer look to Fig. 3. In Fig. 3(a), (c) and (e), which show the voltage waveforms, it can be noticed very good match between the experimental and simulation tests results. Likewise, in Fig. 3 (b), (d) and (f), the current waveforms form experimental test and simulation model, although are in very good agreement, but some deviation specially during starting and ending transient of 47% asymmetrical voltage sag can be noticed. Overall, the waveforms are in a good agreement indicating that the model is valid also for the investigation of asymmetric faults.

Here the deal is that some simplifications have been done in the simulation model. One important simplification is done replacing DC-DC converter of experimental setup with ideal voltage source in simulation model. In the experimental setup, the DC-DC converter will contribute to the DC bus voltage dynamics during load changes (FRT testing) which completely ignored in the simulation model. To quantify the effect of these factor theoretically, it could be a complex matter however, simulation model can be updated adding a DC-DC converter which could have very similar response to the experimental setup. In other hand, as it has been mentioned earlier, models with good accuracy yet simple and fast enough are very much appreciated and needed to be employed by network operators. If we reflect to the simulation accuracy requirements set in some grid codes such as German or Spain, this accuracy easily exceeds the requirement.

From DUT prospective, the dynamics of the DC bus voltage in experimental test (due to the DC-DC converter dynamics which has been ignored in simulation model) can contribute to control dynamics and in this case, it will affect the modulation signal. Since during the operation, the DUT was working in linear modulation range, the dynamics has little effects (probably same as it is seen in Fig. 2 and Fig. 3) on voltage and current waveforms.

Therefore, simplification of DC-DC to the constant DC voltage source in simulation model can be considered as a valid simplification to reduce the complexity of the model in this example test bench. The important observation is that, although some minor differences exist, the results are very close and have the same shape which is the proof for the validity of the simulation model.

The waveforms of symmetrical >95% voltage sag under full inverter current are shown in Fig. 4, where Fig. 4(a), (c) and (e) show the voltage waveforms of experimental and simulation test results. It can be noticed that voltage waveforms from simulation model match very well the experimental results. A short duration mismatch can be noticed in Fig. 4 (e) which shows the voltage waveform during ending of the >95% voltage sag or system recovering from almost 100% voltage sag. However, during this large disturbance, still the simulation model can represent very well the experimental setup dynamics with good accuracy.

Fig. 4(b), (d) and (f) show the results from experimental test and simulation model of the converter current waveforms. The results show that likewise the symmetrical 50% voltage sag case, current waveforms result of simulation model during transients (starting the fault and ending, system recovering form fault) are not in perfect agreement with experimental results. Like converter voltage, the biggest error can be noticed when the system recovering from the fault.

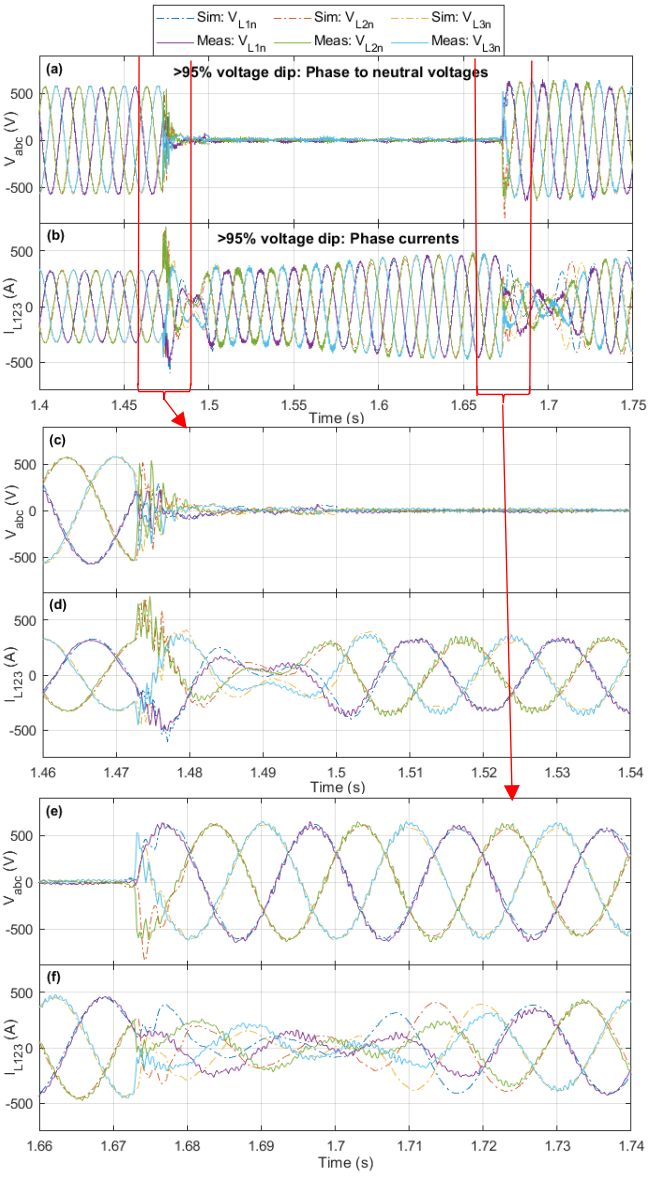

Fig. 4. Results for symmetrical >95% voltage sag under full inverter current (a), (b) phase voltages and currents whole event, (c), (d) phase voltages and currents for starting the >95% sag, (e), (f) phase voltages and currents for ending the >95% sag.

This mismatch is due to the simplifications that have been done in simulation model specially the average modeling of the converter and also utilizing ideal voltage sources in simulation model instead of DC-DC converter to regulate DUT DC bus in experimental test bench. The simulation model recovers faster than experimental setup from >95% voltage sag because it does not include switching devices, and moreover, the dynamics of the DC-DC converter is ignored in simulation model. The important factor is that signals have the same shape and moreover, after very short period, the current waveforms from simulation match very well experimental results.

Fig. 5 shows the results for >95% asymmetrical voltage sag of type B/C [15]. More specifically, Fig. 5(a), (c) and (e) show the voltage waveforms of experimental and simulation test results. It can be noticed that voltage waveforms from simulation model match very well the experimental results. A short duration mismatch can be noticed in Fig. 5 (e) which shows the voltage waveform during ending the >95%

asymmetrical voltage sag or system recovering from almost 100% asymmetrical type B/C voltage sag. Even during this big transient, the overall shape of the simulation results are following the shape of the experimental test results waveforms. Meaning that, during this large disturbance, still the simulation model can represent very well the experimental setup dynamics with sufficiently good accuracy.

Fig. 5(b), (d) and (f) show the results form experimental test and simulation model of the converter current waveforms during the asymmetrical event. The results show that likewise the symmetrical 50% voltage sag case, current waveforms result of simulation model during transients (starting the fault and system recovering form fault) are not in perfect agreement with experimental results. The biggest mismatch between current waveforms can be noticed when the system recovering from the fault, Fig. 5(f), where although the current waveforms reach different peak values but still are following the same transient to reach steady-state conditions.

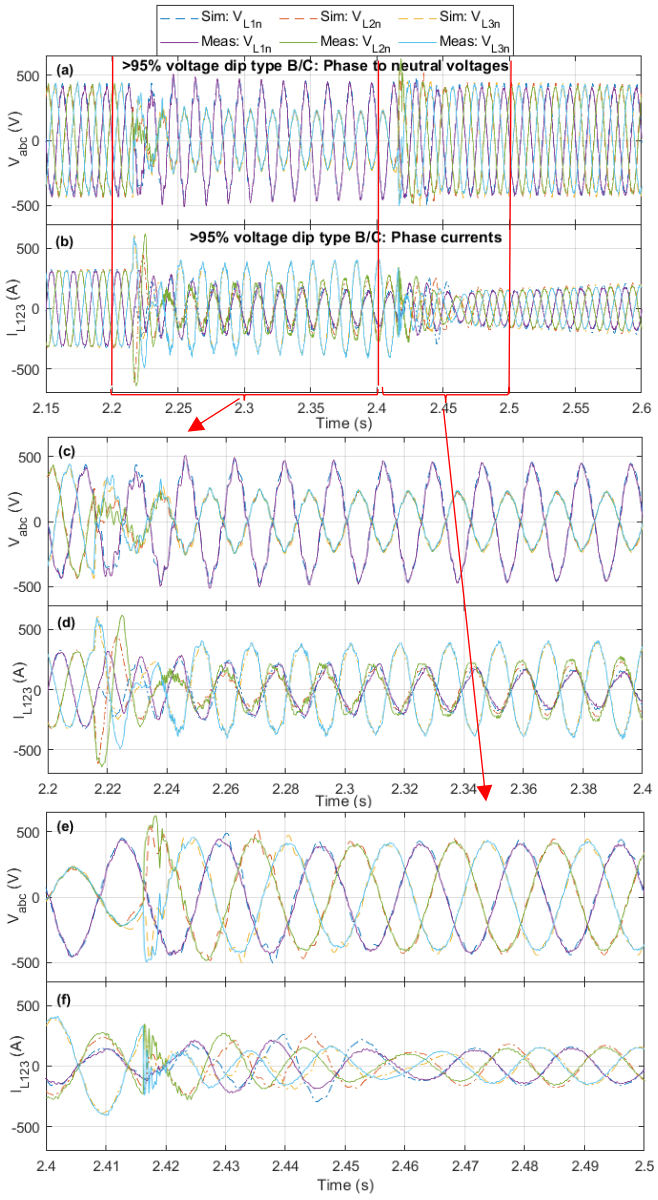

Fig. 5. Results for >95% asymmetrical voltage sag of type B/C (a), (b) phase voltages and phase currents, (c), (d) phase voltages and currents for starting the >95% asymmetrical voltage sag, (e), (f) phase voltages and currents for ending the >95% asymmetrical voltage sag.

Considering slight mismatch between simplified simulation model results and experimental results, one should notice that usually from the grid point of view the requirements concern mainly the capability of PEC to provide FRT with defined active and reactive power window. Thus, the grid code does not indicate the power quality requirements or in other words the exact waveforms of current (and voltage) [18, 19] are not specified. Therefore, the simulation model in under study cases can reflect very well the dynamics of the experimental setup with very good accuracy.

Indeed, as it has been discussed, the simulation model is simplified as much as possible to improve the speed of the simulation model which makes it appropriate to be implemented in RTS practices.

Hence, by effectively implementing the verified simulation model is RTS systems, it is possible to accurately and efficiently simulate the power circuit to interact with the real controller for testing the CHIL configuration. CHIL has been and is being utilized for system development and control verification. It can substantially reduce the design and development cost, human resources, power consumption, and physical space, while providing safety to the actual equipment e.g. in case of malfunction of the controller. If the model is developed properly and verified in laboratory test, it can be used for test evidence for the compliance of grid code requirements such as FRT. When the level of simulation accuracy is proven to be closely similar to the original equipment behaviour, it would be possible, from the technical point of view, to replace at least a part of the grid code compliance tests with fully rated equipment.

As it has been shown and discussed in this paper, the accuracy of simplified model exceeds the requirements for FRT tests since the grid code mandates certain amount of active and reactive power without any requirements for voltage and current power quality indices.

IV. Conclusions and Future Works

The suitability of computer aided simulations in the assessment of inverter's grid code compliance testing was examined. The model was developed based on a full-power laboratory test bench and the waveforms of FRT testing were compared with simulation results. The remarks show that the modeling approach based on averaged inverter model captures the dynamic behavior with a good accuracy. Hence, the dynamic behavior of the inverter in FRT tests can be assessed using the simplified simulation approach.

It is essential to mention that the modelling approach for the control system is essential for the good correspondence between the simulation and experimental results. Although simplifications were made on the circuit level, the simulated control system was close to the real device. The simulator is executing the same control routines as the control of the DUT. Hence the internal signal processing is the same as well as the behavior and response of the control algorithms. This yields to very similar behavior as the real DUT. On the other hand, simplifications have been made on the hardware level modelling by using the average model instead of PWM switching model. This way the simulation model computation speed can be improved but still very good correspondence with the real system can be achieved.

As future work, the verification of the CHIL and PHIL approaches will be examined in this collaboration project.

CHIL (and/or PHIL) will be used to verify the controller performance under several scenarios. There will be requirements for proper interfacing of the controller and real time simulator considering delays and time steps. This research collaboration is aimed towards a new (or an update) standardization for grid code compliance testing requirements.

Another proposal for future work is to stablish the standard simulation setups and procedures to be used for grid code compatibility tests. Where critical analysis of the verification results are needed. Recommendations of suitable standard setup and indication of the potential error sources and limitations of the approach are needed, and at the end probably some tests still need full scale testing to be revealed.

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