Investigation of Switching Time in GaN/AlN Resonant Tunneling Diodes by Experiments and P-SPICE Models

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***Abstract*—The experimental and simulated switching behavior across the negative differential resistance (NDR) region of GaN/AlN double-barrier resonant tunneling diodes (RTDs) is presented. The shortest 10-90% experimental switching time was ∼55 ps. The experimental results are also studied with P-SPICE circuit models, which show that the relatively low peak-to-valley current ratio (∼1.5) and relatively high specific series resistance ($\geq 1 \times 10^{-5} \Omega-$cm^2), both limit the switching time.**

***Index Terms*—GaN/AlN, heterostructure, RTD, switching time, measurement, modeling, P-SPICE.**

I. Introduction

GaN-based heterostructures have broad applications, with notable examples being field effect transistors [1] and light emitting devices [2]. These successes and the large bandoffset have motivated researchers to begin exploration of vertical GaN-based heterostructures as a platform for other types of devices. Recently, GaN/AlN/GaN resonant tunneling diodes (RTDs) have demonstrated highly repeatable operation at room temperature while suffering no obvious degradation from traps. This success is attributable to better design methodology that addresses the high polarization fields, high-quality growth methods and improved fabrication techniques [3]-[4]. However, questions remain on whether GaN/AlN RTDs are capable of being implemented as oscillators and switches with speeds that can compete with earlier RTDs based on GaAs/AlGaAs, InGaAs/AlAs, and InAs/AlSb materials. The wide bandgap and the excellent thermal conductivity of GaN allows very high current density operation of RTDs [5], but can these merits provide any advantages for GaN-based RTDs in high-speed applications? This letter reports our latest investigation into this issue, specifically the first switching time measurements on GaN/AlN RTDs. Additionally, we have conducted P-SPICE simulations to better explain the measured data. Together, the experiments and models presented here provide insight for designing next-generation high-speed, high-power GaN/AlN RTDs.

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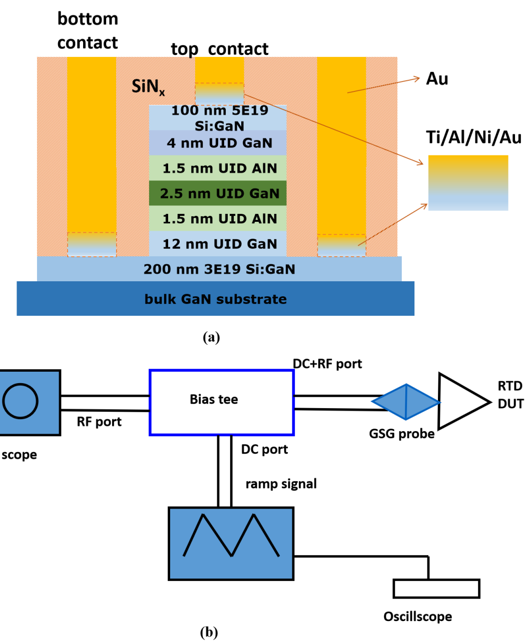


Fig. 1. (a) GaN/AlN heterostructure stack used for fabrication of GaN/AlN RTDs. (b) Experimental setup for switching time measurements.

II. Switching time measurements

The GaN/AlN/GaN RTD heterostructure studied in this research is shown in Fig. 1(a). Its growth and fabrication have been described in detail elsewhere [3], [6]. Figure 1 (b) displays the experimental set-up which was used to investigate the switching time of the GaN/AlN RTDs. This same setup was previously used to successfully measure the switching time of $In_{0.53}Ga_{0.47}As$/AlAs RTDs [7]-[8]. At the center of the set-up is an Anritsu bias tee with a risetime of $t_1 \sim$ 7 ps. The DC port of the bias tee is connected to a ramp signal generator, which produces a DC offset bias along with a triangular waveform that triggers the switching events. The RF port of the bias tee is connected to a fast oscilloscope, in this case, an Infiniium MSOS804A 8-GHz oscilloscope, via a SMA coaxial cable. The Infiniium oscilloscope has an internal

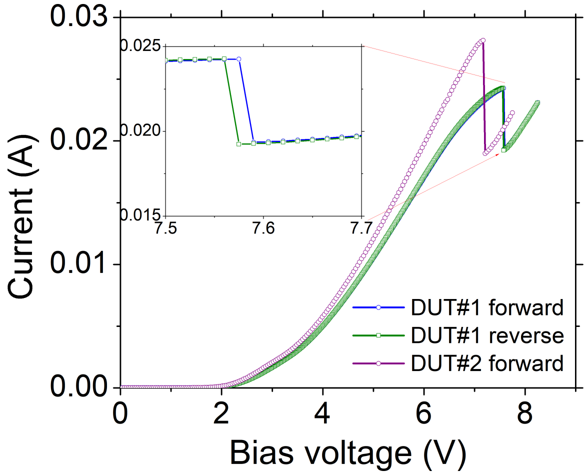


Fig. 2. The I-V characteristics of GaN/AlN RTD #1 including both sweep and backward sweeps. The inset is a zoom-in of the NDR region showing a hysteresis due to the effect of series resistance. Also plotted is the I-V characteristic of RTD #2.

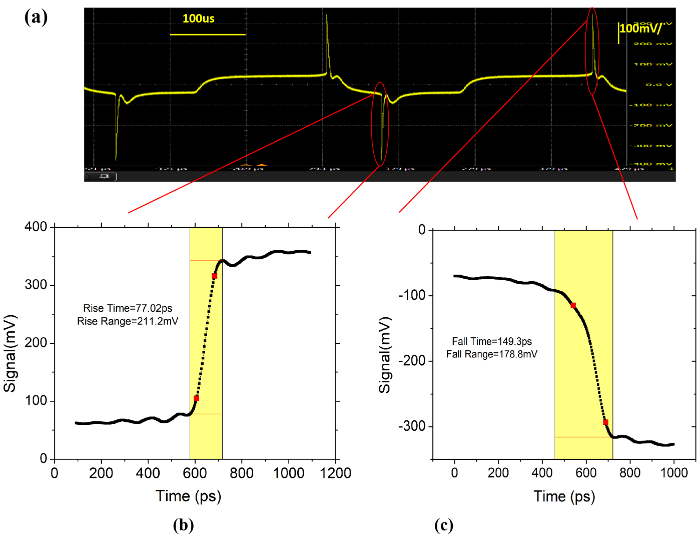


Fig. 3. (a) The voltage signal appeared on the Infiniium oscilloscope for GaN RTD device #2 and the zoom-ins of the switching events. The frequency of the ramp signal was set at 3 kHz. (b) The rise time measurement of the GaN/AlN RTD by zooming in the (front) edge of the spike, which is marked with the red line with arrows. Note the polarity of the voltage signal is reversed. (c) The fall time measurement.

rise/fall-time of t_2=53.8 ps [9], which needs be deducted from the total measured 10-90% switching time. The DC + RF port of the bias tee is connected to a GaN/AlN RTD device under test (DUT). The DC offset (V_{dc}) and ramp signal ($V_{ramp}(t)$) bias voltages are applied to the DUT via a ground-signal-ground (GSG) probe having a 200-μm pitch and a bandwidth of 40 GHz. The total voltage, $V_{dc} + V_{ramp}(t)$, was monitored with a standard (low-speed) oscilloscope.

First, I-V characteristics (i.e. I_M vs. V_M) of the DUTs were taken with a Keithley 2400 source meter. For the first RTD (DUT #1), both forward and backward (voltage) sweeps were conducted. The plots are displayed in Fig. 2, and the zoom-in of the NDR region reveals a small hysteresis that is known to be associated with a significant series resistance, R_s. Similar studies were performed on a second RTD device (DUT #2) from the same batch of devices. Its NDR region displays a small hysteresis too. Figure 2 displays only the forward I-V plot of DUT#2, which will be studied in detail as it has a higher peak-to-valley ratio (PVCR). The I-V curve has a peak voltage of V_P = 7.17 V, and a valley of V_V =7.21 V. The peak current is I_P=28.1 mA, and the valley current is I_V=19.0 mA. The corresponding PVCR is estimated to be ∼1.48, which is much less than that of high-quality InGaAs/AlAs RTDs [7], but amongst the best performance of GaN/AlN RTDs reported in the literature so far. As shown later, a high PVCR is desired because it supports faster switching time.

From the I-V curve of DUT #2, the negative resistance across the NDR region, $R_{NDR}=(V_V - V_P)/(I_V - I_P)$, is estimated to be $R_{NDR} \approx$ -4.2 Ω. To induce switching events, the maximum of the voltage signal $[V_{dc}+V_{ramp}(t)]$ was tuned to be greater than V_V while the minimum was adjusted lower than V_P. No self-oscillation from the NDR, which could derail switching events, was observed.

Figure 3 (a) shows the screen shot of the switching events of DUT#2 on a 100 μs scale measured with the fast oscilloscope (e. g. the Infiniium). Note, the polarity of the measured voltage signal needs be reversed to extract the rise time and the fall time. In other words, the downward and upward spikes exhibit the rise and fall switching events, respectively. Then the edges of the spikes displayed in Fig. 3(a) were amplified with a finer time resolution. The 10-to-90% rise time was found to be $t_{tot,r}$ ≈77 ps (Fig. 3 (b)), while the 10-to-90% fall time was $t_{tot,f}$ ≈149 ps (Fig. 3 (c)). Measurements on DUT#1 and other devices from the same substrate produced similar results.

After subtraction of the oscilloscope's rise (fall) time as well as the bias tee's risetime through the relationship $\sqrt{t_{tot}^2 - t_1^2 - t_2^2}$, the intrinsic 10-to-90% rise time of the RTD switching is estimated to be $t_r \approx$ 55 ps, and the intrinsic 10-to-90% fall time is $t_f \approx$ 139 ps. Noticeably, the rise time is shorter than the fall time. This is a behavior that has been observed previously in InGaAs/AlAs RTDs, which had a rise time of ∼21ps compared to a fall time of ∼38ps [7], [8]. Despite the fact that the measured switching time of these GaN/AlN RTDs is slower than that of InGaAs/AlAs RTDs, this is the first direct measurement of the switching time in vertical GaN/AlN RTDs to the best of our knowledge, and illustrates that GaN/AlN RTDs are intrinsically capable of very high speeds.

Further, for a switching event from the peak-to-valley of any RTD, the 10-to-90% time has been estimated analytically [10],

$$t_R \approx 4.4\frac{\Delta V}{S} \tag{1}$$

where $S = \Delta J/C_A = (J_P - J_V)/C_A$ is called the speed index. $\Delta V = V_V - V_P$ is the voltage span of the NDR region. $\Delta J = J_P - J_V$ is the current span of the NDR region, where J_P and J_V are the peak and valley current densities, respectively. C_A is the specific capacitance with contributions from the accumulated emitter region, barrier-quantum-well-barrier region, and depleted collector region, in kind. Note that S can be also written as a function of PVCR and J_P ,

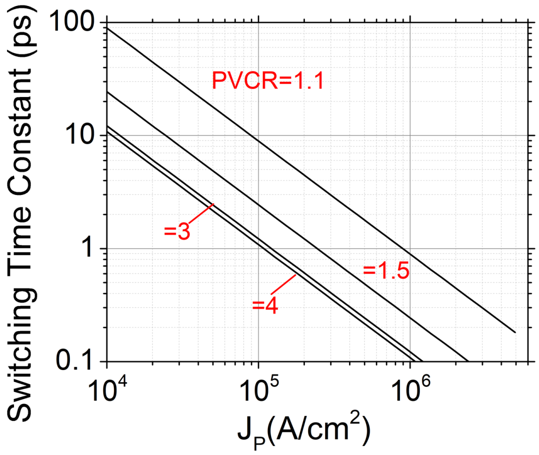


Fig. 4. Switching time vs peak current density.

$S = J_P(1 - 1/PVCR)/C_A$, which indicates that a larger PVCR enables a faster device speed.

Because the capacitance of the RTD was difficult to measure experimentally, we estimated it by evaluating the space charge vs bias voltage spanning over the entire RTD structure with a Poisson solver provided by Silvaco Atlas [11]. The significant effect from the polarization fields at the GaN/AlN hetero-interfaces was taken into account, and from this calculation, the specific capacitance was found to be $C_A \approx 4.8$ fF/μm^2. Given the device area of A≈11 μm^2, the capacitance for the RTD is C=C_AA ≈ 52.8 fF. The peak and valley current densities ($J_P = I_P/A$, $J_V = I_V/A$), and their PVCR are easily evaluated from the I-V curve #2 displayed in Fig. 2.

With the speed-index formula Eq. (1), the dependence of switching time t_R on J_P as well as PVCR are evaluated, and plotted in Fig. 4. Using the PVCR of $\sim$ 1.4 and the peak current density of J_P $\sim$2.6×10^{5}A/cm^2, we reach a theoretical value of t_R $\sim$1 ps, which is significantly less than the experimental data.

Furthermore, we considered an opposite scenario by testing a third RTD device (DUT #3) but from a different substrate with a lower current density of $\sim$9.6×10^{3}A/cm^2 and a smaller PVCR of $\sim$1.1 (Fig. 5 (a)). The 10-to-90% rise time was measured to be $\sim$317 ns, and the fall time was $\sim$ 342 ns. Both were much longer than that of DUT #2, as expected (Fig. 5 (b)). However, they are also significantly longer than the $\sim$ 90 ps predicted with Fig. 4.

Nevertheless, despite the quantitative differences, both the experimental and the modeling results of DUT #1,#2 and #3 confirm that large PVCRs and high peak current densities need be pursued to obtain high-speed switching.

III. P-SPICE Models for GaN/AlN RTDs

To gain a better understanding of the discrepancy between the experimental data and the modeling results of Eq. (1), we performed P-SPICE simulations on an equivalent circuit for RTDs, which is illustrated in Fig. 5. The RTD is modeled as an ideal diode, which is shown inside the dashed box of

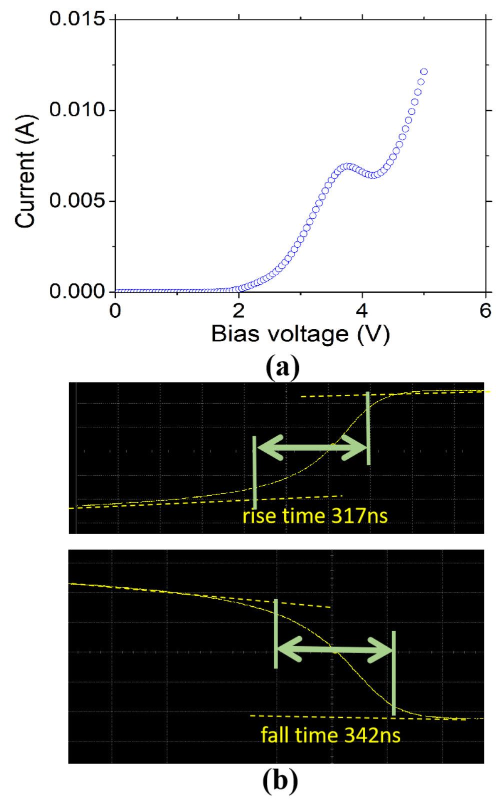


Fig. 5. (a) The I-V curve of DUT #3. (b)Switching time measurement results.

Fig. 6, along with several lumped elements: C and R_s. C is the capacitance; R_s is the series resistance. We make the assumption that R_s is mostly contact resistance. R_L is load line resistance.

The ideal diode has an I-V characteristic that can be described by the following equation [12], [13],

$$I = C_1 V^i \{\tan^{-1}[C_2(V - V_T)] - \tan^{-1}[C_2(V - V_N)]\} + C_3 V^j + C_4 V^k \quad (2)$$

where C_1, C_2, C_3 and C_4 are numerical constants. V_T is defined as the threshold voltage where the second-order derivative d^2I/dV^2 has a local maximum. V_N is defined as the bias in the NDR region where the current variation is the steepest. i, j and k are integer exponents ≥2.

Their values were set as i=3, j=5 and k=3, the same as in the modeling of InGaAs/AlAs RTDs [12]. The rest of the parameters of Eq. (2) are obtained by fitting the I-V curve of the ideal RTD diode, which is corrected by subtracting the voltage drop across the series resistance R_s from the experimental I-V curve through the Kirchhof's law

$$V = V_M - I_M R_s \quad (3)$$

$$I = I_M \quad (4)$$

where V_M and I_M are the measured voltage and current shown in Fig. 2. This correction is necessary based upon the analysis that a tiny hysteresis loop appears on forward and backward sweeps because of series resistance. The value of

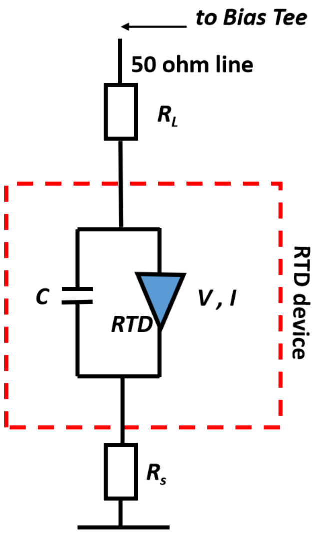


Fig. 6. A circuit model for GaN/AlN RTD devices used in P-SPICE simulations.

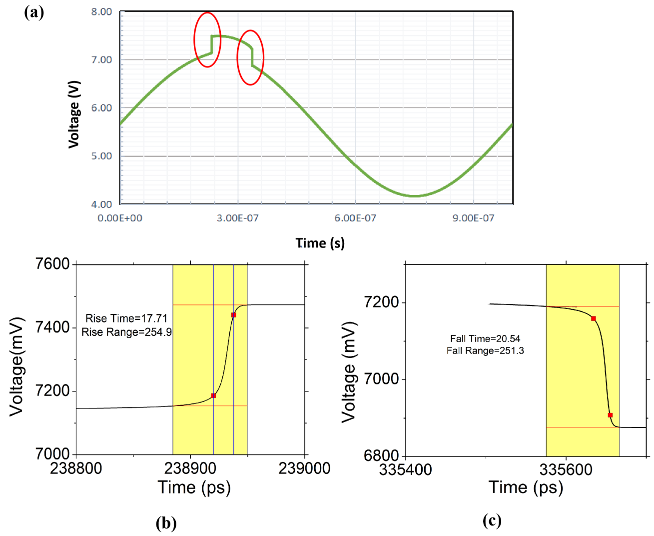


Fig. 7. (a) Simulation of a switching event with the P-SPICE models. (b) Zoom-in of the rise time. Unit used in the rise time extraction: ps (c) Zoom-in of the fall time.

R_s is estimated in the range of 50-75 Ω by adjusting the value of R_s until the hysteresis begins to disappear on the corrected I-V curves of Fig. 2.

The circuit model of Fig. 6 was implemented in a schematic in P-SPICE along with a script programmed for Eq. (2) [14]. A sinusoidal waveform was selected to mimic the triangular ramp signal used in the experiments because it is easier to be realized in the software. Figure 7 (a) shows a P-SPICE simulation with the following parameters: V_{dc}=6.5V, V_{ramp}=3 V, $R_s = 50\Omega$ and $R_L = 50\Omega$. The transient resolution was set to 1 ps in order to evaluate accurately the switching time while maintaining acceptable computing time. As displayed in Fig. 7 (a), the switching behavior of both rising and falling events is reproduced by the simulation. From the zoom-ins of (a), the 10-to-90% rise time is estimated to be ∼19 ps while the fall time is ∼ 23 ps. Both are shorter than the experimental values (Figs. 7 (b), (c)).

Next, we studied the influence of R_s on t_R by treating it as a variable. The results are plotted in Fig. 8 (a). The plot confirms that a large R_s indeed could slow down the switching speeds. And R_s may be responsible for why the rise time is the shorter one compared to the fall time in both GaN/AlN and InGaAs/AlAs RTDs. On the other hand, surprisingly, the R_s-dependence isn't monotonic. The switching time t_R becomes shorter once the value of R_s is greater than 50 Ω, for example, $R_s = 75\Omega$. This is likely caused by an increase of the NDR voltage span, $\Delta V = \Delta I \times R_s$, which would reduce t_R according to Eq. (1).

In our GaN-based devices, both the top and bottom contacts were a Ti/Al/Ni/Au stack (Fig. 1). With this type of Ohmic contact stack, the minimum contact resistance (i.e. the best) obtained so far from TLM structure data was $\sim 1\times 10^{-5}$ Ω-cm^2, from which the smallest R_s was estimated to be ∼9.1 Ω. This corresponds to a rise time of ∼6.2 ps according to Fig. 8 (a). Thus, reducing the contact resistance is critical to accelerate future switching speeds, which may be achieved in two ways: (i) to optimize the Ohmic metal stack, and/or (ii) to increase the thickness of metal films.

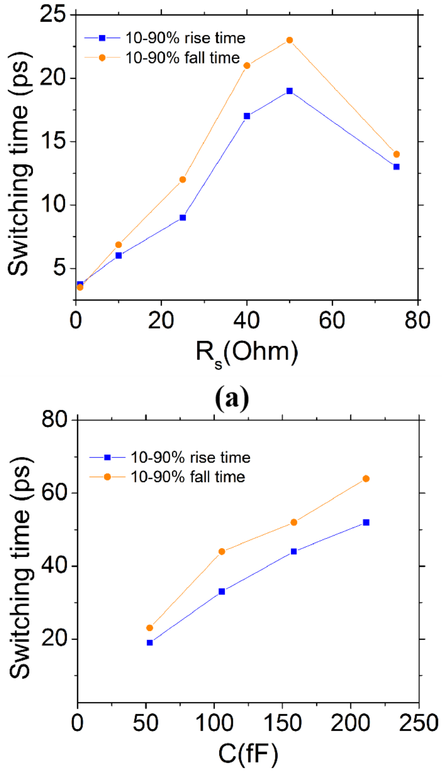
Another factor likely contributing to the difference between the experimental data and the SPICE models is the capacitance C, which may be underestimated in the Silvaco calculations. The actual area (A_{act}) for the GaN/AlN stack could be greater than the one designed for the device (A≈11 μm^2), which was used in the capacitor calculation. The fringe effect of the planar structure and the isolating Si_3N_4 layer may contribute additional unaccounted capacitance (Fig. 1). Therefore, we investigated the C dependence of the switching time following the same procedure above. The results are plotted in Fig. 8 (b). As expected, the switching time becomes longer as the capacitance increases. If the capacitance is set to C∼211 fF, and the series resistance R_s is set to 50 Ω, the rise time is ∼54 ps, close to the experimental data.

IV. Summary

We measured the 10-90% switching time of GaN/AlN RTDs and conducted detailed modeling with a speed-index formula as well as P-SPICE models. While the ∼55ps switching time (peak-to-valley) is slower than reported in InGaAs/AlAs RTDs (i. e. ∼21 ps), our results show great promise for GaN/AlN RTDs as high-speed, high-power oscillators.

The speed-index formula indicates either peak current densities or PVCRs need be increased to achieve a short switching time. This has been confirmed by the experiments. However, there is a significant discrepancy between the model and the experimental data remaining to be explained. This is different from the previous studies on InGaAs/AlAs RTDs, where the speed-index formula easily gave a satisfied agreement with the experimental data [7].

The P-SPICE analysis reveals that the series resistance –mostly from the contacts of the devices –is an important factor contributing to this discrepancy, and it explains why the fall time is longer than the rise time. And the series resistance



(b)

Fig. 8. Simulation on the influence of R_s on 10-90% switching time.

could diminish adversarially the NDR voltage span, which is important to high speed and high power output. Thus, to obtain shorter switching time, it is worth putting effort into reducing contact resistances in GaN/AlN RTDs. We also investigated the specific capacitance that could be another factor capable of slowing down the switching speed of GaN/AlN RTDs.

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