Advanced grid concept with external busbars applied on III–V multijunction solar cells

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***Abstract*—We report on the development of an advanced front contact grid design applied on GaInP/GaAs/GaInNAsSb solar cells. Unlike in a conventional grid pattern, the busbars are placed outside the active area of the solar cell. This enables minimizing the shadowing effect caused by the contact grid pattern as well as reaching smaller-active-area solar cells for concentrated photovoltaics, ultimately leading to higher conversion efficiencies. The quality of the solar cells was characterized by electroluminescence and current-voltage measurements. The concept was proven as a viable option for boosting the performance of multijunction solar cells.**

Keywords—contact grid design, front contact, III–V heterostructures, multijunction solar cell, CPV

I. Introduction

To date, compound semiconductor solar cells have been the utmost performers when it comes to high-efficiency solar cell technologies – the highest conversion efficiency of 47.1% has been achieved with a metamorphic six-junction III–V solar cell under concentrated light [1]. In order to reach high-efficiency performance with multijunction devices, not only the solar cell materials and the choice of heterostructures need to be developed, but also all the other aspects affecting the photovoltaic conversion must be carefully optimized. These include grid optimization where the contact grid related power losses [2] should be minimized. In this respect, one important loss mechanism originates from the shadowing effect where the metal grid partly covers the area of the cell surface. Since the shadowing related losses are directly proportional to the grid area, reducing the grid area has an immediate effect on the conversion efficiency. However, grid optimization is an interplay of several factors, such as resistive losses originating from the emitter, the grid metals and pattern, and the contact between them.

The limits for minimizing the finger shadowing arise from the technical limitations of the grid fabrication, i.e., how narrow fingers can be fabricated, and especially in concentrated photovoltaics (CPV) the fingers must have a sufficiently large cross-sectional area in order to conduct all the photogenerated charge carriers also under high photogeneration levels. Thus, ideally, high aspect ratios resulting from narrow and thick fingers are desirable in CPV. Since there is only little improvement concerning the minimizing of the finger shadowing, grid optimization focuses usually on optimizing the grid pattern with respect to the finger spacing.

However, losses can be further reduced by minimizing the shadowing effect associated to the busbars. As an ultimate option, the busbars can be removed from the solar cell active area partly [3] or even completely [4, 5, 6], resulting in a busbarless grid concept. This would not only have a positive effect on the conversion efficiency by reducing the area of the unilluminated solar cell, but also enables fabrication of solar cells with smaller areas since busbars are not limiting the solar cell size. This would ultimately decrease the III–V material use and could be beneficial especially for micro-scale CPV [7], which aims at increasing cost-effectiveness by downscaling the module size.

Here we report on the operation of triple-junction solar cells fabricated with an advanced front contact grid design in which the busbars are located outside the solar cell active area. The quality of the device components was characterized both by electroluminescence (EL) and current-voltage (*I-V*) measurements.

II. Experimental

A. Concept design

The present contact grid concept differs from a conventional front contact grid pattern which is fully located on top of the

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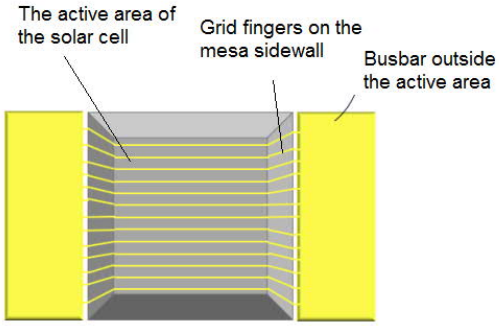

Fig. 1. A schematic of the grid concept.

mesa structure. Here, the busbars, i.e., the contact areas for current extraction, are placed outside the solar cell active area as shown in Fig. 1. The grid fingers are collecting the charge carriers from the emitter and further conduct the current to the busbars across the mesa sidewalls. Thus, an insulating dielectric layer is implemented between the metal fingers and the mesa sidewall in order to preserve the solar cell performance. Plasma enhanced chemical vapor deposition (PECVD) was used for dielectric fabrication since it is a low-cost, widely used, and scalable fabrication method.

B. *Electrical isolation study*

Prior to device fabrication, dielectric insulation was investigated using a p-doped GaAs substrate. Subsequent to mesa etching, several different designs of dielectric layers of SiO_x and SiN_x with varying layer thicknesses and number of layers were deposited on the front surface of the sample and a planar metal layer on top of it. The samples were characterized using dark *I-V* measurements with a Metrohm Autolab potentiostat.

C. *Device fabrication*

The solar cell structures comprised monolithically stacked GaInP/GaAs/GaInNAsSb heterostructures that were grown on a p-GaAs substrate with a Veeco GEN20 molecular beam epitaxy system. A more detailed description of the growth can be found in [8]. Mesa structures were fabricated by etching. For isolation, a SiO_x/SiN_x (300 nm / 300 nm) coating was deposited on the mesa sidewalls by PECVD. The dielectric bilayer was overlapping with the front surface either 5, 10, or 20 µm. The front contact metallization consisting of Ni/Au (10 nm / 200 nm) and back metallization of Ti/Au were deposited by electron beam evaporation. The front metals were partly deposited in tilted angle in order to assure the continuity of metal fingers also on steep mesa sidewalls. Lastly, contact GaAs was etched and a TiO_x/SiO_x antireflection coating was deposited by electron beam evaporation.

Photolithographic fabrication processes were used for sample masking during the device fabrication. For reference, similar device components were fabricated with a conventional H-pattern grid with two busbars located on top of the mesa structure. The sidewalls of the reference solar cells did not have an isolating coating. The active area of the studied and the reference solar cells was 4 mm^2.

D. *Device characterization*

In order to study the electrical performance of the device components, their *I-V* performance was characterized with a 7 kW OAI Trisol solar simulator at one-sun (AM1.5D, 1 000 W/m^2) at 25 °C. *I-V* under dark conditions was measured with a Bio Rad DL8000 instrument. The quality of the device processing was assessed by EL imaging, using a power supply and a microscope attached to a computer. Imaging was conducted at different current values and with two different filters: a Thorlabs shortpass filter (FES800) with a cut-off wavelength of 800 nm and a Thorlabs longpass filter (FEL850) with a cut-off wavelength of 850 nm enabling to detect EL from GaInP and GaAs subcells, respectively. In addition, the device components were imaged by scanning electron microscopy (SEM).

III. Results and Discussion

Based on the electrical isolation study, the design of a SiO_x/SiN_x (300 nm / 300 nm) was chosen for the actual solar cell components. As presented in Fig. 2, it was the only design that did not conduct measurable current at bias voltages between -4 V and 4 V. The whole measurement range is not shown in the figure. The results from the isolation tests indicate that a thick enough dielectric layer is required between the metal and the semiconductor mesa sidewall for proper electrical isolation.

The averaged parameters obtained from the light-biased *I-V* measurements are summarized in Table I. The open-circuit voltage (V_{OC}) values of the studied samples are comparable to the reference value. This indicates that all the three junctions are functional and thus the dielectric layer was sufficiently insulating the metal fingers from the mesa sidewalls and prevented shunting effects. However, slightly decreased fill factor values imply a slightly degraded cell performance.

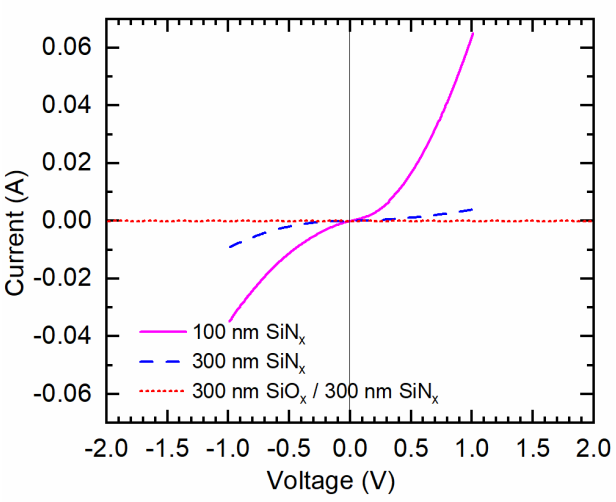

Fig. 2. Dark *I-V* results of the electrical isolation study.

TABLE I. PARAMETERS OF CURRENT-VOLTAGE PERFORMANCE

Sample	Parameters		
	Dielectric offset (µm)	V_{OC} (V)	Fill factor (%)
S1	5	2.58	60
S2	10	2.61	69
S3	20	2.60	66
Ref.	-	2.63	78

In order to further investigate the electrical performance, the dark *I-V* data shown in Fig. 3 was analyzed. Logarithmic scale was used for the absolute value of current in order to detect any differences for low current levels. The samples with the 10 µm and 20 µm wide offsets show lower leakage current than the reference, and the current values go even below the measurement limit of ~1 nA. This indicates a non-shunting behavior. The sample with the 5 µm wide offset however shows an increased leakage current compared to the reference, which explains the lowered V_{OC} and fill factor values for sample S1. Except for this one sample, all the other device components with a 5 µm wide dielectric offset were heavily shunted. Most likely the shunting behavior of the 5 µm was due to a non-successful lithography process in which the dielectric layers were not completely covering the sidewalls and thus resulted in shunting electrical contacts between metal and the mesa sidewall.

In order to further investigate the cell performance, the spatial distribution of EL was analyzed. Fig. 4 shows EL detected from GaInP (using FES800) and GaAs (using FEL850) subcells. The GaAs subcell shows similar behavior to the reference cell where the EL signal seems very even throughout the device. This indicates that the current is spread evenly and no shunting is present. However, the EL from the GaInP subcell shows slightly degraded behavior. EL in the middle area of the device is slightly weaker compared to the areas closer to device facets. On the other hand, small bright areas right next to the

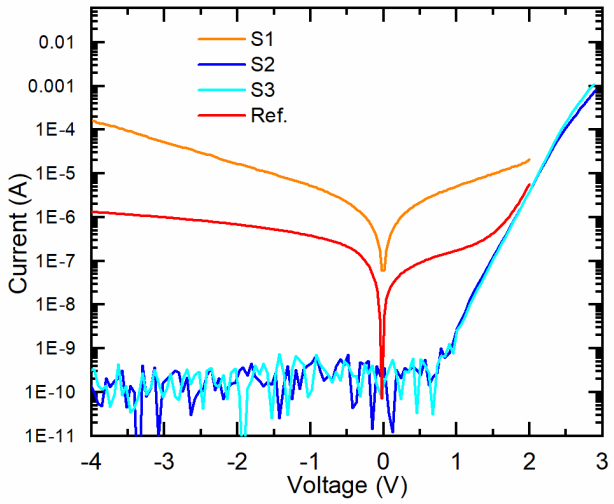

Fig. 3. Dark *I-V* results of the device components.

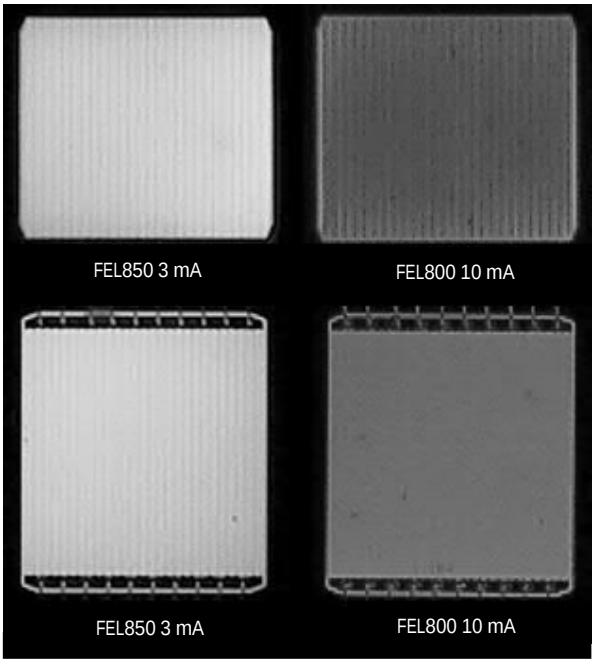

Fig. 4. EL images of GaAs (left) and GaInP (right) subcells. Upper images correspond to sample S3 and lower images to a reference sample.

device sidewalls indicate radiative perimeter recombination or edge emission. Based on the EL data, it is concluded that the smaller fill factor values are associated with decreased shunt resistance of the GaInP top cell, which is seen as a nonuniform EL pattern.

Overall, based on the imaging of the devices shown in Fig. 5, the fabrication was of high quality. With dielectric offsets wider than 5 µm the fabrication was proven to be successful also in terms of photovoltaic operation. Moreover, the metal fingers on the steep mesa sidewalls were continuous. In order to ease the fabrication and to reduce the shadowing losses caused by the dielectric overlapping offset, the dielectric could be first fabricated with wider overlapping offset and then etched away from the top of the mesa. This approach could be further studied in the future.

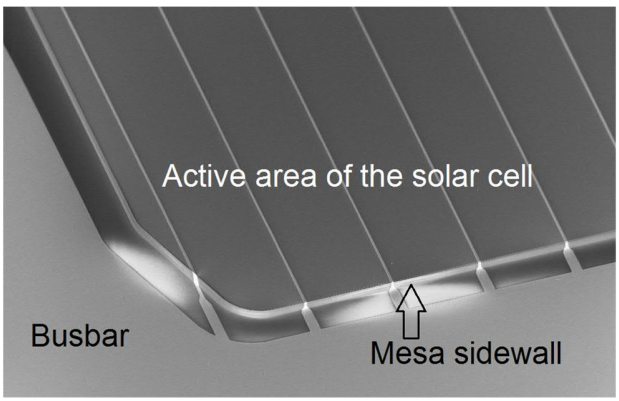

Fig. 5. A SEM image of a fabricated device.

IV. Conclusions

A proof-of-concept of an advanced grid design was demonstrated where the busbars were successfully placed outside of the active area of a multijunction solar cell. The achieved open-circuit voltage values were comparable to the reference value. This suggests that the dielectric insulation was adequate between the metal fingers and the mesa sidewall in order to prevent shunting. However, there is still room for improvement concerning the device performance. In summary, the concept was proven to work and can be considered as a viable option for boosting the performance of multijunction solar cells by reducing the shadowing losses.

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