Direct Model Predictive Power Control of a Series-Connected Modular Rectifier

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***Abstract*—This paper presents a direct model predictive power control for a series-connected modular rectifier. The topology combines a diode rectifier and an active-front-end (AFE) converter to achieve a medium voltage target. A voltage control loop regulates the total dc voltage, providing the power references to the inner direct model predictive control. Operation under the desired real and reactive power is achieved, while minimizing the converter switching frequency. Moreover, successful operation and control of the AFE converter is guaranteed thanks to a hard constraint included in the optimization problem.**

I. Introduction

A standard (non-modular) ac-dc conversion system, either fully passive, or active, has the advantage of a lower number of components (i.e., lower cost maintenance) compared to a modular solution. High-voltage semiconductors are usually needed to handle medium voltage (MV) applications. On the other hand, modular topologies employ lower voltage/current rating semiconductors to achieve the same MV target [1].

This paper adopts the topology initially proposed in [2], [3], where the dc links of two independent ac-dc modules are connected in series, i.e., the total dc-link voltage is the sum of each dc contribution. As a result, redundancy with respect to the output dc voltage (i.e., higher reliability) is introduced as well as power/voltage scalability. In particular, a diode rectifier (DR) is combined with an active-front-end (AFE) converter, which adds voltage controllability against dc-link voltage fluctuations. Both modules are connected via a dual-winding transformer, with equal secondary windings, to the point of common coupling (PCC), which acts as the connection point of the conversion system to the grid. Moreover, *L*-filters are employed to reduce current and voltage harmonics at the PCC.

With regards to the control of the modular rectifier, a cascaded controller is utilized. Specifically, the outer loop regulates the dc-link voltage of the AFE converter along its reference; the latter is calculated based on the steady-state dc-link voltage of the DR and the targeted voltage on the dc side. In doing so, the real power is manipulated and its desired value is fed into the inner loop designed in the framework of model predictive control (MPC). The adopted optimal control scheme — designed as a direct controller, i.e., a modulator is not used — aims at minimizing the real and reactive power errors by manipulating the converter switches.

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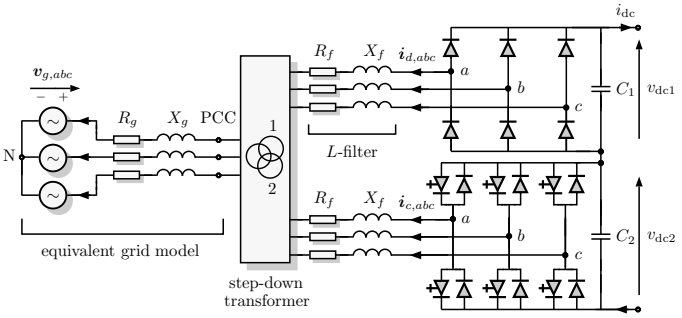


Fig. 1. Grid-tied series-connected modular rectifier based on two modules (a DR and a AFE converter) with *L* input filters.

Regarding the latter, several direct MPC-based strategies for the power control of a grid-tied two-level converter have been proposed in [4], [5], [6]. However, for MV applications the power electronic converter has to be operated at a low switching frequency because the switching losses typically dominate the conduction losses. Therefore, minimization of the switching effort constitutes another control objective, as proposed in [7], [8]. Therein, the power control problem is not formulated as a reference tracking one. Instead, the notion of hysteresis control is employed to keep the real and reactive powers within predefined bounds while the switching effort being the only term to be minimized. Such an approach, being a derivative of direct power control (DPC), was aptly named model predictive direct power control (MPDPC).

In this paper, the instantaneous powers are directly controlled to track their desired values. By minimizing an appropriate cost function in real time, the desired system behavior, in terms of real and reactive power reference tracking, is achieved, while a reasonably low switching frequency results. Furthermore, the introduced weighting factors are adjusted to operate on the tradeoff between the (competing) terms of the cost function. Moreover, owing to the constrained nature of the proposed MPC algorithm, an explicit output hard constraint is implemented to deal with the inherent limitation of the system controllability. By doing so, the minimum condition which ensures that the AFE converter is not disabled (i.e., turned off) is always met. The presented simulation results highlight the effectiveness of the proposed direct model predictive power control for the series-connected modular topology in question.

II. Case Study

We refer to a modular rectifier which comprises of a six-pulse DR and a two-level AFE converter as shown in Fig. 1. Each module has an *L*-filter at its input and a filter capacitor at its output. In general, additional loads may be connected to the PCC, thus, strict grid standards are imposed at this point. For industrial applications, the IEEE 519 [9]

TABLE I
MV SYSTEM PARAMETERS

Rated values		Parameters	
input voltage V_R	1.2 kV	grid inductance L_g	0.19 mH
input current I_R	833 A	grid resistance R_g	3.02 mΩ
apparent power S_R	1.73 MVA	leakage inductance L_t	0.77 mH
grid frequency f_g	50 Hz	leakage resistance R_t	5.1 mΩ
dc-link voltage $V_{\rm dc}$	3.6 kV	filter inductance L_f	1.1 mH
dc-link current $I_{\rm dc}$	718 A	filter resistance R_f	4 mΩ
		output capacitor $C_{1,2}$	3.2 mF

and IEC 61000-2-4 [10] standards — which impose upper bounds on the magnitude of individual current and voltage harmonics, respectively — are considered[1]. Due to the series configuration, the modules share the same dc current $i_{\rm dc}$, which is imposed by the load. The total dc-link voltage is $v_{\rm dc}(t) = v_{\rm dc1}(t) + v_{\rm dc2}(t)$, where $v_{\rm dc1}(t)$ refers to the (fixed) DR contribution, while $v_{\rm dc2}(t)$ is the controllable variable[2].

Throughout the paper, we normalize all SI variables to the rated values of the step-down transformer. From Table I, the p.u. system is established using the base quantities $V_B = \sqrt{2/3}V_R$, $I_B = \sqrt{2}I_R$, $S_B = S_R = (3/2)\,V_B I_B$, and $\omega_B = \omega_g = 2\pi f_g$, where V_R and I_R denote the (rated) rms line-to-line voltage and rms line current referred to the secondary side of the transformer.

III. CONTROLLER MODEL

In the sequel, a mathematical description of the converter dynamics is derived in the $\alpha\beta$-reference frame. All variables given in the abc-plane $\boldsymbol{\xi}_{abc} = [\xi_a \;\; \xi_b \;\; \xi_c]^T$ are mapped into two-dimensional vectors $\boldsymbol{\xi}_{\alpha\beta} = [\xi_\alpha \; \xi_\beta]^T$ via the Clarke transformation matrix $\boldsymbol{K}$ (without the common-mode).

$$\boldsymbol{K} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{1}$$

Hereafter, to simplify the notation, the subscript $\alpha\beta$ is dropped from all vectors, unless otherwise stated.

Consider the grid voltage $\boldsymbol{v}_g(t)$ as shown in Fig. 1. The distribution lines are approximated by the grid resistance R_g and reactance X_g (computed from the inductance as $\omega_g L_g$). Likewise, the step-down transformer can be represented by its split series resistance R_t and leakage reactance X_t, while the *L*-filter by the reactance X_f and its internal resistor R_f. All resistances and reactances are lumped into the equivalent quantities $R = R_g + R_t + R_f$ and $X = X_g + X_t + X_f$. At the right of PCC, we define the input current $\boldsymbol{i}_c(t)$ and voltage $\boldsymbol{v}_c(t)$ of the AFE converter, while $\boldsymbol{i}_d(t)$ and $\boldsymbol{v}_d(t)$ refer to the corresponding quantities of the DR. Currents flowing towards the grid are assumed to be positive.

A. Grid Sensitivity to Power Electronics Insertion

The grid sensitivity to the insertion of power electronic systems is characterized by the impedance ratio $k_{\rm XR}$ and the short-circuit ratio $k_{\rm sc}$. The IEEE 519 limits are given as function of $k_{\rm sc}$ [9].

[1]Note that, for MV applications, an *LCL* filter is more suitable than an *L* one due to the better attenuation of the high-frequency harmonics and its smaller size, i.e., lower cost.

[2]Such a connection may require semiconductor devices with a higher reverse blocking voltage (i.e., higher cost, conduction losses).

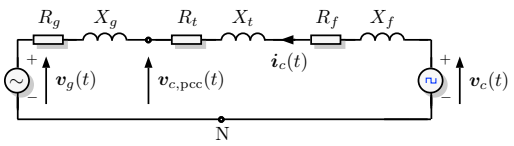


Fig. 2. Equivalent circuit of the grid-connected AFE converter in the $\alpha\beta$-plane. The PCC is denoted by the voltage $\boldsymbol{v}_{c,\rm pcc}(t)$.

$$k_{\rm XR} = \frac{X_g}{R_g} \qquad k_{\rm sc} = \frac{S_{\rm sc}}{S_R} = \frac{V_R^2}{\sqrt{R_g^2 + X_g^2}}\frac{1}{S_R} \tag{2}$$

Based on the parameters in Table I it can be found that the short-circuit power at the PCC, i.e., the maximum power that the grid can provide at this point, is $S_{\rm sc} = 23.84\,$MVA while $k_{\rm XR} = 19.98$. Moreover, $k_{\rm sc} = 41.34 \geq 20$, meaning that the considered grid is a strong one, i.e., the power of the rectifier is much smaller than the available $S_{\rm sc}$ [11].

B. Physical Model of the Grid

The evolution of a balanced three-phase grid voltage in the $\alpha\beta$-plane can be described by the differential equation

$$\frac{{\rm d}\boldsymbol{v}_g(t)}{{\rm dt}} = \omega_g \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \boldsymbol{v}_g(t) \tag{3}$$

The secondary side of the step-down transformer is characterized by the real $P_{{\rm in}x}$, reactive $Q_{{\rm in}x}$, and apparent $S_{{\rm in}x}$ power, where $x \in \{1, 2\}$ denotes the power of the DR ($x = 1$) and the AFE converter ($x = 2$). At rated operation it holds that $P_R = \sqrt{3}\,V_R I_R \cos(\phi)$, $Q_R = \sqrt{3}\,V_R I_R \sin(\phi)$, and $S_R = \sqrt{3}\,V_R I_R = (3/2)\,V_B I_B$, where ϕ is the phase angle between voltage and current waveforms. Finally, the power factor is ${\rm pf} = |\cos(\phi)| = P_{{\rm in}x}/S_{{\rm in}x}$.

C. Physical Model of the AFE Converter

Given the equivalent circuit in Fig. 2, the AFE converter dynamics in the $\alpha\beta$-plane are given by

$$X\frac{{\rm d}\boldsymbol{i}_c(t)}{{\rm dt}} = -R\boldsymbol{i}_c(t) - \boldsymbol{v}_g(t) + \boldsymbol{v}_c(t) \tag{4}$$

The voltage $\boldsymbol{v}_c(t)$ is determined by the three-phase switch position $\boldsymbol{u}_{abc}(t) = [u_a \; u_b \; u_c]^T$, where u_z is the switch position on each phase $z \in \{a, b, c\}$, and the rated dc-link voltage $V_{\rm dc2}$, i.e.,

$$\boldsymbol{v}_c(t) = V_{\rm dc2}\boldsymbol{K}\boldsymbol{u}_{abc}(t) = V_{\rm dc2}\boldsymbol{u}(t) \tag{5}$$

For a two-level topology u_z is restricted to the set $\mathcal{U} = \{0, 1\}$, with $\mathcal{U} \subset \mathbb{Z}$ (integer-valued). It follows $\boldsymbol{u}_{abc} \in \boldsymbol{\mathcal{U}} = \mathcal{U}^3$, which includes the following $2^3 = 8$ elements (i.e., three-phase switch position combinations)

$$\mathcal{U}^3 \triangleq \left\{ \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \right\} \tag{6}$$

The controller model used by the MPC algorithm predicts the evolution of the real and reactive powers in the $\alpha\beta$-plane [11]. From the instantaneous power theory, it follows that[3]

$$P_{\rm in2}(t) = v_{g\alpha}(t)i_{c\alpha}(t) + v_{g\beta}(t)i_{c\beta}(t) \tag{7}$$

$$Q_{\rm in2}(t) = v_{g\alpha}(t)i_{c\beta}(t) - v_{g\beta}(t)i_{c\alpha}(t) \tag{8}$$

[3]Note that, due to the p.u. normalization, the factor $3/2$ is neglected from (7) and (8).

Both $P_{\mathrm{in2}}(t)$ and $Q_{\mathrm{in2}}(t)$ refer to the PCC, but for the sake of simplicity, they refer to the grid voltage sources.

By defining the state vector $\boldsymbol{x}(t) = \left[\boldsymbol{i}_c^T(t)\ \boldsymbol{v}_g^T(t)\right]^T \in \mathbb{R}^4$, the output vector $\boldsymbol{y}(t) = [P_{\mathrm{in2}}(t)\ Q_{\mathrm{in2}}(t)]^T \in \mathbb{R}^2$, and the three-phase switch position $\boldsymbol{u}_{abc}(t)$ as the input to the system, the continuous-time state-space representation is

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{dt}} = \boldsymbol{F}\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}_{abc}(t) \tag{9}$$

$$\boldsymbol{y}(t) = \boldsymbol{h}\left(\boldsymbol{x}(t)\right) \tag{10}$$

where $\boldsymbol{F} \in \mathbb{R}^{4\times4}$, $\boldsymbol{G} \in \mathbb{R}^{4\times2}$, and $\boldsymbol{h}(\boldsymbol{x}(t)) \in \mathbb{R}^{2\times1}$ are

$$\boldsymbol{F} = \begin{bmatrix} -\frac{R}{X} & 0 & -\frac{1}{X} & 0 \\ 0 & -\frac{R}{X} & 0 & -\frac{1}{X} \\ 0 & 0 & 0 & -\omega_g \\ 0 & 0 & \omega_g & 0 \end{bmatrix} \tag{11}$$

$$\boldsymbol{G} = \begin{bmatrix} \frac{V_{\mathrm{dc2}}}{X} & 0 & 0 & 0 \\ 0 & \frac{V_{\mathrm{dc2}}}{X} & 0 & 0 \end{bmatrix}^T \boldsymbol{K} \tag{12}$$

$$\boldsymbol{h}(\boldsymbol{x}(t)) = \begin{bmatrix} x_1(t)x_3(t) + x_2(t)x_4(t) \\ x_2(t)x_3(t) - x_1(t)x_4(t) \end{bmatrix} \tag{13}$$

As can be seen from (7) and (8), the system output $\boldsymbol{y}(t)$ is a nonlinear (component-wise) combination of the state. The state-dependent output function $\boldsymbol{h}(\boldsymbol{x}(t))$ in (10) performs the mapping from $\boldsymbol{x}(t)$ to $\boldsymbol{y}(t)$.

MPC requires the prediction model of the system to be in the discrete-time domain. Since $\boldsymbol{F}$ and $\boldsymbol{G}$ are assumed to be time-invariant matrices, the system dynamics, given by (9) and (10), are discretized by using the exact Euler discretization with the sampling interval T_s. This yields

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\boldsymbol{u}_{abc}(k) \tag{14}$$

$$\boldsymbol{y}(k) = \boldsymbol{h}\left(\boldsymbol{x}(k)\right) \tag{15}$$

with $\boldsymbol{A} = \mathrm{e}^{\boldsymbol{F}T_s}$ and $\boldsymbol{B} = -\boldsymbol{F}^{-1}\left(\boldsymbol{I}_4 - \boldsymbol{A}\right)\boldsymbol{G}$, since $\boldsymbol{F}$ is nonzero. $\boldsymbol{I}_4$ is the four-dimensional identity matrix, e the matrix exponential, and $k \in \mathbb{N}$ denotes the discrete-time step.

IV. Direct MPC with Power References Tracking

The proposed direct model predictive power control aims to regulate the real and reactive power along their reference values, while minimizing the switching effort, and meeting the grid codes. The total dc-link voltage $v_{\mathrm{dc}}(t)$ is controlled via $v_{\mathrm{dc2}}(t)$. A reference calculation block provides the desired trajectory $v^*_{\mathrm{dc2}}(t)$ for $v_{\mathrm{dc2}}(t)$ by estimating the DR contribution. The reference $P^*_{\mathrm{in2}}(t)$ is set by an outer voltage loop, while $Q^*_{\mathrm{in2}}(t)$ is set to zero to achieve $\mathrm{pf} = 1$ operation. Finally, the inherent controllability limitation of the system is explicitly described by a (hard) output constraint. The complete block diagram of the proposed algorithm is depicted in Fig. 3.

A. Reference Calculations

Neglecting the *L*-filter and C_1 (i.e., ideal conditions), the dc-link voltage of a six-pulse DR consists of six segments within one fundamental period $T_g = 1/f_g$. Each segment results from the combinations of $\boldsymbol{v}_{g,abc}(t)$ and the conduction of the diodes. By normalizing the time axis to ωt, the average dc voltage in rated operating conditions is given by

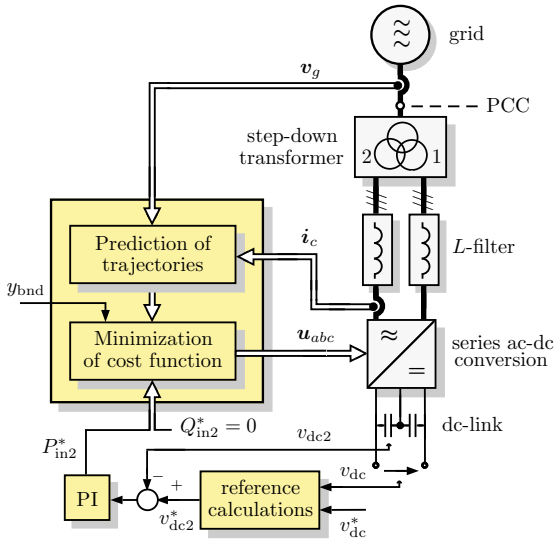


Fig. 3. Direct MPC with power reference tracking for the series ac-dc conversion system shown in Fig. 1.

$$\widehat{V}'_{\mathrm{dc1}} = \frac{3}{\pi}\int_{-\pi/6}^{\pi/6} \sqrt{2}V_R \cos\left(\omega_g t\right)\ \mathrm{d}\left(\omega t\right) = \frac{3}{\pi}\sqrt{2}V_R \tag{16}$$

When considering the voltage drop on the equivalent reactance X and resistance R of the ac side of the system, (16) becomes

$$\widehat{V}_{\mathrm{dc1}} = \widehat{V}'_{\mathrm{dc1}} - \frac{3}{\pi}\left(R + X\right) i_{\mathrm{dc}} \tag{17}$$

All intermediate steps which lead to (16) and (17) are described in [12]. Since i_{dc} is constant, the DR is assumed to be working at rated condition for every operating point. Given the dc-link voltage reference $v^*_{\mathrm{dc}}(t)$, the targeted value for the dc-link voltage of the AFE converter is $v^*_{\mathrm{dc2}}(t) = v^*_{\mathrm{dc}}(t) - \widehat{V}_{\mathrm{dc1}}$. Note that, C_1 dampens the high-frequency harmonics resulting in a smooth $v_{\mathrm{dc1}}(t)$ voltage.

B. Controllability Constraint

The modular topology in Fig. 1 has an inherent limitation in its controllability. If the input power of the AFE converter is less than a minimum required value $P_{\mathrm{in2,min}}$ then it cannot be actively controlled. In such a case, it behaves as a DR due to its freewheeling diodes. Consequently, its minimum dc-link voltage value $V_{\mathrm{dc2,min}}$ is computed similarly to (17).

To avoid such a situation, and given that the proposed MPC aims to operate the system with $\mathrm{pf} = 1$ — the dc-link power is given by real power only, i.e., $P_{\mathrm{in2}}(k) = S_{\mathrm{in2}}(k) = P_{\mathrm{dc2}}(k)$ — the minimum processed power is $P_{\mathrm{in2,min}} = V_{\mathrm{dc2,min}} i_{\mathrm{dc}}$. Defining the latter as a lower bound, the condition that needs to be met so as the AFE converter does not behave as a passive rectifier can be expressed as

$$[1\ 0]^T\, \boldsymbol{y}(k+1) \geq y_{\mathrm{bnd}} \tag{18}$$

where the nonnegative scalar $y_{\mathrm{bnd}} > P_{\mathrm{in2,min}} \in \mathbb{R}^+$ defines the boundary value of the real power. Such value must be strictly greater than $P_{\mathrm{in2,min}}$ otherwise $\mathrm{pf} \neq 1$ leading to $P_{\mathrm{in2}}(k) \neq S_{\mathrm{in2}}(k)$. Therefore, the to-be-formulated optimization problem needs to compute the optimal switch position while respecting (18). To do so, (18) can be added as a hard (output) constraint to the optimization problem. This, however, implies that the input feasible set is restricted.

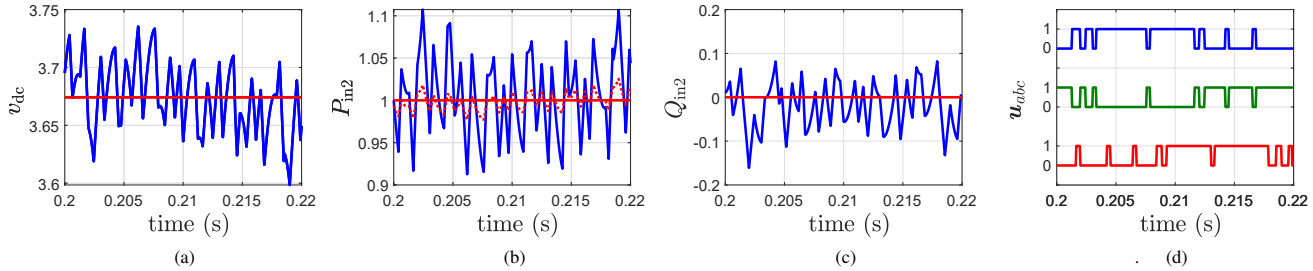


Fig. 4. Simulated waveforms produced by the direct model predictive power controller during steady-state operation at rated power. (a) Total dc-link voltage $v_{\rm dc1}(t) + v_{\rm dc2}(t)$ (blue line) and its reference (red line). (b) Real power (blue line) and its reference (red line) provided by the outer PI controller. (c) Reactive power (blue line) and its reference (red line) set to achieve pf $= 1$. (d) Three-phase switch position (control input) $\boldsymbol{u}_{abc}(t)$.

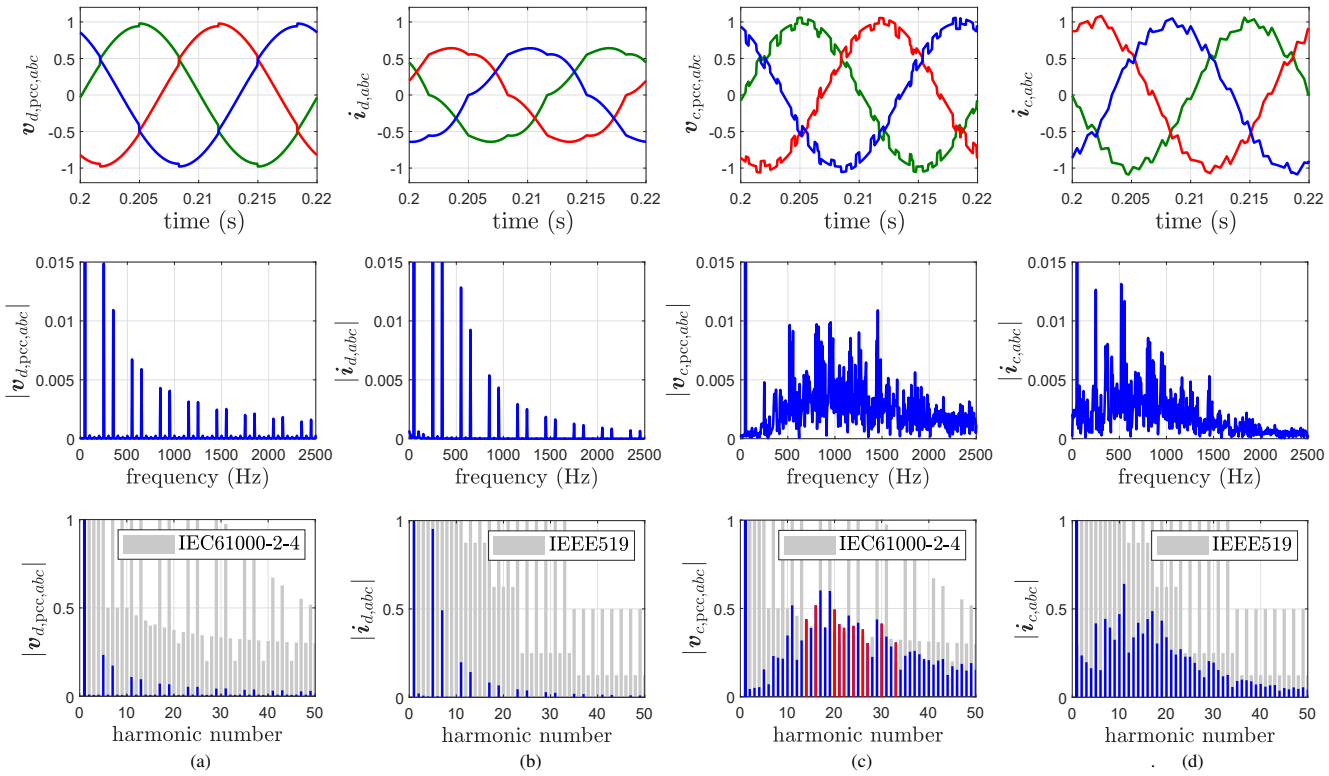


Fig. 5. Simulated waveforms of the three-phase voltage and current at the PCC, spectrum analysis and comparison with the relevant grid standards (integer components multiples of f_g): IEEE 519 (for $k_{\rm sc} = 41.34$) and IEC 61000-2-4 (for Class 2). (a) Three-phase voltages of the DR side. (b) Three-phase currents of the DR side. (c) Three-phase voltages of the AFE converter side. (d) Three-phase currents of the AFE converter side.

C. Optimization Problem Formulation

The inner loop, designed in the framework of MPC, tackles the aforementioned control objectives by mapping them into a scalar through the cost function $J(k) : \mathbb{R}^2 \times \boldsymbol{\mathcal{U}} \to \mathbb{R}^+$

$$J(k) = \lambda_q J_Q(k) + (1 - \lambda_q)\, J_P(k) + \lambda_u J_{\rm sw}(k) \tag{19}$$

which comprises the following three terms

$$J_Q(k) = \left(Q^*_{\rm in2}(k+1) - Q_{\rm in2}(k+1)\right)^2 \tag{20}$$

$$J_P(k) = \left(P^*_{\rm in2}(k+1) - P_{\rm in2}(k+1)\right)^2 \tag{21}$$

$$J_{\rm sw}(k) = \|\Delta \boldsymbol{u}_{abc}(k)\|_1 \tag{22}$$

Note that (19) is a quadratic function (rather than absolute value function) to increase the closed-loop stability of the system [13]. The first two terms $J_Q(k)$ and $J_P(k)$ in (19) relate to the power tracking performances (i.e., the deviation of actual values from their references). The third term evaluates the AFE converter switching effort, defined as the difference between two consecutive switch positions, i.e., $\Delta \boldsymbol{u}_{abc}(k) = \boldsymbol{u}_{abc}(k) - \boldsymbol{u}_{abc}(k-1)$. Note that, the use of ℓ_1- or ℓ_2-norm does not make any difference since $\Delta \boldsymbol{u}_{abc}(k) \in \{-1, 0, 1\}$. Thus, the term $J_{\rm sw}(k)$ directly relates to the device (average) switching frequency, defined as

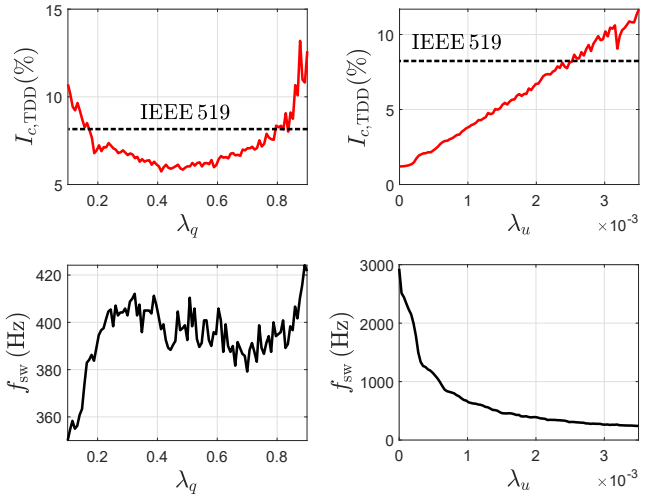
$$f_{\rm sw} = \lim_{N\to\infty} \frac{1}{6NT_s} \sum_{\ell=0}^{N-1} \|\Delta \boldsymbol{u}_{abc}(\ell)\|_1 \tag{23}$$

where N is a time window within compute $f_{\rm sw}$[4].

The weighting factors $\lambda_q, \lambda_u \in \mathbb{R}^+$ are tuning parameters which adjust the tradeoff between the tracking accuracy of the controller and the switching effort. Specifically, by using the p.u. system, the real and reactive power values are of the same magnitude, thus $\lambda_q \in [0, 1]$. Regarding λ_u, it is tuned such that a low switching frequency $f_{\rm sw}$ results without compromising the tracking performance of the controller.

To compute the optimal control input $\boldsymbol{u}_{{\rm opt},abc}(k)$ which minimizes (19) the following integer optimization problem needs to be solved in real time

[4]It is common to consider a finite value for N, e.g. aimed to cover at least 5-10 periods of T_s, referring to a specific steady-state time window.



(a) Curves for $\lambda_u = 0.00183$ (b) Curves for $\lambda_q = 0.4$

Fig. 6. Effects of the weighting factors on the current TDD, $I_{c,\mathrm{TDD}}$, and the switching frequency, f_{sw}. The black dashed lines refer to $I_{c,\mathrm{TDD,max}} = 8\%$ given by the IEEE 519 standard

$$\boldsymbol{u}_{\mathrm{opt},abc}(k) = \arg\underset{\boldsymbol{u}_{abc}(k)}{\text{minimize}}\ J(k) \tag{24}$$

$$\text{subject to } \boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\boldsymbol{u}_{abc}(k) \tag{25}$$

$$\boldsymbol{y}(k+1) = \boldsymbol{h}\left(\boldsymbol{x}(k+1)\right) \tag{26}$$

$$[1\ 0]^T\, \boldsymbol{y}(k+1) \geq y_{\mathrm{bnd}} \tag{27}$$

$$\boldsymbol{u}_{abc}(k) \in \boldsymbol{\mathcal{U}} \tag{28}$$

The dynamic evolution of the system is predicted for one time step ahead in time — i.e., $\boldsymbol{x}(k+1)$ and $\boldsymbol{y}(k+1)$ — by applying each feasible three-phase switch position $\boldsymbol{u}_{abc}(k)$. The optimal solution $\boldsymbol{u}_{\mathrm{opt},abc}(k)$, i.e., the switch position applied to the AFE converter, is found by *enumerating* all feasible $\boldsymbol{u}_{abc}(k)$ and choosing the one which leads to the minimum value of $J(k)$. It is worth mentioning that since a one-step horizon is considered in this paper, the size of the resulting integer optimization problem is small, and thus the brute-force approach of exhaustive enumeration is computationally feasible (e.g. 2^3 candidate cost functions to be evaluated within T_s). Nevertheless, the proposed MPC algorithm is expected to improve the system performance — in terms of grid current total demand distortion (TDD) — when extending the length of the prediction horizon [14]; such a direction is currently under investigation.

V. Simulation Results

The performance of the direct model predictive power control of the modular rectifier are evaluated trough MATLAB simulations, with a sampling interval $T_s = 50\,\mu$s. The system parameters are given in Table I. The rate of dc link controllability depends on the power routing among the modules [1]. A simple PI-based controller is used in the outer loop. The voltage contribution at the PCC is computed based on the equivalent circuit shown in Fig. 2. All results are presented in the normalized p.u. system.

A. Steady-State Operations

To evaluate the steady-state performance of the system, one period of the fundamental frequency $T_g = 1/f_g = 20\,$ms is examined. First, the weighting factors are set to $\lambda_q = 0.4$ and $\lambda_u = 0.00183$, which results in an average device switching frequency of $f_{\mathrm{sw}} = 393\,$Hz. The simulation results for this scenario are shown in Fig. 4. As can be seen in Fig. 4(a), the total dc-link voltage (blue line) accurately track its reference (red line). Moreover, the real and reactive power tracking are depicted in Figs. 4(b) and (c), respectively. As can be observed in Fig. 4(c), $Q_{\mathrm{in2}}(t)$ presents an offset with respect to its reference. This is a side-effect of MPC which does not include a proper integral action [15]. The latter is included in the voltage controller which achieves a zero steady-state error. Note that the red dashed line in Fig. 4(b) indicates the real power reference computed based on the measured dc voltage of the DR output. As can be seen, this value is very close to the reference (red line) estimated based on the expression (17). Finally, Fig. 4(d) shows the three-phase switch positions. Note that the voltage reference matches the rated value $V_{\mathrm{dc}} = 3.67\,$p.u., while $\widehat{V}_{\mathrm{dc1}} = 1.23\,$p.u. and $v^*_{\mathrm{dc2}}(t) = V_{\mathrm{dc2}} = 2.44\,$p.u. Therefore, the AFE converter controls about 66% of the total dc-link, meaning that the modules are not equally loaded. Finally, the real power $P_{\mathrm{in2}}(t)$ equals the apparent power $S_R = 1\,$p.u. (pf $= 1$), and the total dc-link power is $P_{\mathrm{dc}}(t) = P_{\mathrm{in1}}(t) + S_R$, where $P_{\mathrm{in1}}(t) < S_R$ since pf $\neq 1$ holds for the DR.

The ac side performances are assessed in terms of current $I_{\mathrm{TDD}}(\%)$ and voltage $V_{\mathrm{TDD}}(\%)$ TDD [11]. Fig. 5 shows the ac-side current and voltage waveforms of the DR and AFE converter along with their relative spectra. In particular, Figs. 5(a) and (b) refer to $\boldsymbol{i}_{d,abc}(t)$ and $\boldsymbol{v}_{d,\mathrm{pcc},abc}(t)$. As can be seen, both have discrete harmonic spectra with mainly non-triplen odd components, with the resulting TDD being $I_{d,\mathrm{TDD}} = 7.21\%$ and $V_{d,\mathrm{TDD}} = 2.33\%$, respectively. Figs. 5(c) and (d) depict the $\boldsymbol{i}_{c,abc}(t)$ and $\boldsymbol{v}_{c,\mathrm{pcc},abc}(t)$. Due to the absence of a modulator and the consequent variable f_{sw}, both signals have nondeterministic spectra, with the energy being distributed over a wide range of frequencies. The produced TDD is $I_{c,\mathrm{TDD}} = 6.08\%$ and $V_{c,\mathrm{TDD}} = 7.77\%$, respectively, relatively low considering the very low switching frequency.

Regarding the grid standards, given $k_{\mathrm{sc}} = 41.34$, the IEEE 519 standard indicates a maximum $I_{\mathrm{TDD,max}} = 8\%$ and the harmonics limits depicted in Figs. 5(b) and (d) as light gray bars. In the same figures, integer harmonics of $\boldsymbol{i}_{d,abc}(t)$ and $\boldsymbol{i}_{c,abc}(t)$ that meet these limits are shown as blue bars, while each violation as a red bar. Harmonics of noninteger order are lumped to the closest integer harmonic by computing an equivalent rms value. It can be deduced that thanks to the L-filters, the currents fulfill the standard. As for the voltage harmonics, we refer to the Class 2 electromagnetic environment of the IEC 61000-2-4 standard. The relevant limits are superimposed on $\boldsymbol{v}_{d,\mathrm{pcc},abc}(t)$, and $\boldsymbol{v}_{c,\mathrm{pcc},abc}(t)$ in Figs. 5(a) and (c). It can be observed, that limits on high-order triplen odd components are particularly stringent. Consequently, several harmonics of $\boldsymbol{v}_{c,\mathrm{pcc},abc}(t)$ violate the grid code (e.g., the 16th harmonic exceeds its limit by a factor of 1.32), thus, a more effective filter is needed to meet such a standard. In contrast, the $\boldsymbol{v}_{d,\mathrm{pcc},abc}(t)$ components are easily meet such requirements.

In a next step, the weighting factors λ_q and λ_u are varied in order to investigate the tradeoff between the current distortion

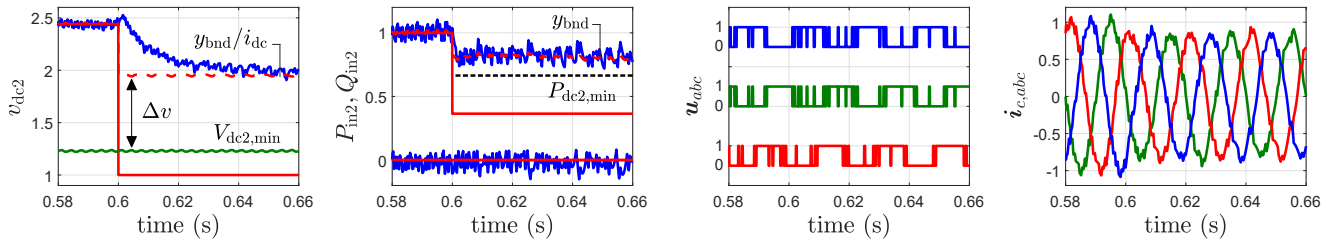


Fig. 7. Simulated waveforms for a voltage reference step change from rated operation to a nonfeasible voltage level (red line). (a) The dc-link voltage $v_{\mathrm{dc2}}(t)$ (blue line) is clamped to $y_{\mathrm{bnd}}/i_{\mathrm{dc}}$ (red dashed line). (b) The real power voltage $P_{\mathrm{in2}}(t)$ (blue line) is clamped to y_{bnd} (red dashed line), above $P_{\mathrm{in2,min}}$ (black dashed line). (c) Three-phase switch position with constrained behavior. (d) Three-phase input currents $\boldsymbol{i}_{c,abc}(t)$.

and the average switching frequency. Fig. 6(a) shows the tradeoff curves for $\lambda_u = 0.00183$ while λ_q is varied between 0.1 and 0.9, with a resolution of 100 points. As can be observed, $I_{c,\mathrm{TDD}}$ changes in a nonlinear fashion with λ_q. For example, when $\lambda_q < 0.45$ $I_{c,\mathrm{TDD}}$ decreases with an increasing λ_q ($I_{c,\mathrm{TDD}} = 5.96\,\%$ at $\lambda_q = 0.45$), while the monotony of the curve changes for $\lambda_q > 0.45$. Likewise, f_{sw} changes nonlinearly with λ_q. Fig. 6(b) shows the tradeoff curves for $\lambda_q = 0.4$ while λ_u is varied between 0 and 0.0035 (100 points). In this case, $I_{c,\mathrm{TDD}}$ depends almost linearly on λ_u, with $I_{c,\mathrm{TDD}}$ varying between $1.2\,\%$ and $11.7\,\%$. As for f_{sw}, this steeply decreases from $f_{\mathrm{sw}} = 2.9\,\mathrm{kHz}$ to $241\,\mathrm{Hz}$.

B. Transient Operations

The transient performance of the proposed algorithm is examined for a critical voltage reference, stepwise change, to highlight how (27) affects the optimal switch position selection. For the same choice of λ_q and λ_u as in Section V-A, the system response is shown in Fig. 7. The voltage tracking is depicted in Fig. 7(a), while Fig. 7(b) shows the power tracking performance of the controller. At time instant $t = 0.6\,\mathrm{s}$, $v^*_{\mathrm{dc2}}(t)$ decreases from 2.44 to 1 p.u. From (17) it is derived that $V_{\mathrm{dc2,min}} = \widehat{V}_{\mathrm{dc1}} = 1.23\,\mathrm{p.u.}$, thus, $v^*_{\mathrm{dc2}}(t) < V_{\mathrm{dc2,min}}$. Likewise, the real power decreases from 1 to $0.4\,\mathrm{p.u.}$, which is lower than $P_{\mathrm{dc2,min}} = 0.75\,\mathrm{p.u.}$ Given $y_{\mathrm{bnd}} = 0.8\,\mathrm{p.u.}$, it is implied that the switch positions $\boldsymbol{u}_{abc}(k)$ that lead to a violation of (27) (i.e., $P_{\mathrm{in2}}(k+1) > y_{\mathrm{bnd}}$) at every time step k are considered infeasible, thus they do not constitute candidate solutions of the optimization problem. In doing so, the AFE converter can be actively controlled. Moreover, the dc-link voltage is limited to a new steady-state value $y_{\mathrm{bnd}}/i_{\mathrm{dc}} = 1.3\,\mathrm{p.u.}$, giving rise to a protection gap of $\Delta v = 0.3\,\mathrm{p.u.}$ Fig. 7(c) shows the resulting switch positions, while Fig. 7(d) shows the dynamic response of the three-phase current $\boldsymbol{i}_{c,abc}(t)$. Based on these results, it can be concluded that both steady-state and transient performance of the modular rectifier are relatively good.

VI. Conclusions

This paper presented a one-step direct model predictive power control for a series-connected modular topology including L-filters. By appropriately modeling the system dynamics, an accurate prediction model was derived. The optimization problem underlying MPC with power reference tracking was formulated as a constrained one by incorporating a hard constraint resulting from the inherent controllability limitation of the topology in question. The effectiveness of the proposed strategy was evaluated through simulations both at steady-state and transient operation. When comparing the ac waveforms at the PCC with the industrial standards, like IEEE 519 and IEC 6000-2-4, it was concluded that when operating the converter at a switching frequency of a few hundred Hz the grid current standards can be met, but it is particularly difficult to abide by the grid voltage requirements.

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