

### 13.5 A 0.35-to-2.6GHz Multilevel Outphasing Transmitter with a Digital Interpolating Phase Modulator Enabling up to 400MHz Instantaneous Bandwidth

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Advanced wireless radio standards set stringent requirements on the bandwidth, frequency range and reconfigurability of base-station transmitters. Recently, the outphasing concept has shown promise of wide bandwidth while taking advantage of process scaling with extensive exploitation of rail-to-rail signaling. Recent outphasing transmitter designs have often focused on power-amplifier (PA) and power-combiner implementations while omitting the phase modulator [1,2]. Moreover, previously reported transmitters with integrated digital phase modulators have only shown bandwidths up to 40MHz [3,4], although 133MHz has been demonstrated at 10GHz carrier frequency utilizing phase modulators based on conventional IQ-DACs [5]. Thus, digital-intensive outphasing transmitters capable of modulation with hundreds of MHz bandwidth at existing cellular frequency bands have not yet been published. To address the aforementioned challenge, this paper introduces a multilevel outphasing transmitter with four amplitude levels, including the first prototype implementation based on the digital interpolating phase modulator concept [6]. The transmitter is targeted for 5G picocell base stations and has been verified to operate with instantaneous bandwidth up to 400MHz. In addition, the developed phase modulator eliminates the need for complex on-chip frequency synthesizers by introducing digital carrier frequency generation, demonstrated between 0.35 and 2.6GHz, while utilizing a single 1.8GHz reference clock.

The wide bandwidth and digital carrier generation of the developed phase modulator are enabled by digital phase interpolation, illustrated in Fig. 13.5.1. The sinusoidal phase-modulated RF waveform  $S(t)$  is estimated during every sample period  $T_s$  by its digital phase equivalent  $\rho[n]$ , which consists of a constant carrier-frequency-dependent phase increment  $\alpha$  and the phase modulation component  $\Phi[n]$ . The square-wave representation of the original waveform  $S(t)$  can be reconstructed from its zero-crossings ( $D_x$ ), equivalent to  $m\pi$  crossings of  $\rho$  during the period. The zero-crossings occurring between consecutive phase samples are calculated by using linear interpolation. As the carrier frequency is defined by a single variable  $\alpha$ , the modulator is able to upconvert the phase-modulated data to any carrier frequency. The range is only limited by the maximum number of transitions per sample period allowed by hardware, constrained in this prototype to four in order to enable instantaneous frequencies up to twice the sample rate. Thus, the on-chip DSP finds the zero-crossings by processing four linear equations per sample period with 8-stage binary search solvers.

The block and timing diagrams of the developed phase modulator are depicted in Fig. 13.5.2. The phase-modulated signal is formed with four digital-to-time converters (DTC). DTC control signals, provided by the solvers, indicate the time instants of output toggling ( $D_x$ ) with 8b resolution during each quarter of  $T_s$ . In order to guarantee that only rising edges defined by  $D_x$  propagate to the modulator output, the signals inside the DTC need to be in low state when data is updated. Therefore, each DTC is clocked one fourth of a clock period before rising edges arrive to the phase selector. The DTC output is generated by selecting one of four coarse phases with a multiplexer and increasing the phase resolution to 8b with a varactor-based digitally controlled delay line (DCDL). A pulse generator triggered by rising edges is used at the DTC output to decrease the duty cycle of the pulses and thus avoid overlap during combining at the following OR gate. The output of the OR gate drives a T flip-flop, reconstructing the phase-modulated square-wave signal based on  $S(t)$ .

The block diagram of the implemented transmitter, divided into digital and RF sections, is presented in Fig. 13.5.3. The digital front-end (DFE) performs tasks related to phase interpolation, control and interfacing. In order to achieve 1.8GHz sample rate, an FPGA feeds the four amplitude bits and phase modulation data to the DFE through a 57.6Gb/s deserializer with eight data lanes. The DFE in this prototype does not contain dedicated hardware required for predistorting the solver outputs, therefore all measurements are presented without predistortion. The clock feed circuitry in the RF section buffers the

7.2GHz clock for the deserializer and divides it into 1.8GHz for the rest of the system. The RF section also contains two phase-modulator cores, a phase generator producing 16 coarse phase signals with 50% duty cycle, and an output driver. The driver consists of four current-steering cells, controlled by modulator outputs and amplitude bits, and a wideband on-chip resonator. An adjustable delay element is included in the amplitude-bit signal path to account for intrinsic delay of the phase modulators.

The transmitter was implemented in 28nm FDSOI CMOS. The die micrograph is shown in Fig. 13.5.7, with active area of 2.2mm<sup>2</sup>. The transmitter's capability for wideband modulation was evaluated at 2GHz carrier frequency by aggregating multiple 20MHz OFDM LTE carriers to build up signals with 400MHz and 200MHz bandwidths, with measured spectra shown in Fig. 13.5.4. Digital carrier generation with constant 1.8GHz reference clock is demonstrated in Fig. 13.5.5 with a 20MHz signal measured with 150MHz steps between carrier frequencies of 0.35 to 2.6GHz. The results prove the feasibility of the approach, showing nearly flat ACLR behavior with slight degradation near the edges of the frequency range and integer fractions of the sample rate. At the measured center frequencies, the total power consumption of the prototype transmitter is 635 to 680mW, out of which 43 to 73mW is consumed by the phase modulator cores and the driver. The performance was also evaluated with a 20MHz OFDM signal with 64-QAM subcarrier modulation at 2GHz carrier frequency, achieving an ACLR of -40dBc and an EVM of -29dB.

Comparison to state-of-the-art transmitters with integrated phase modulators is presented in Fig. 13.5.6. The transmitter presented in this paper stands out with the widest instantaneous bandwidth, as well as being capable of digital carrier generation while utilizing a single reference clock frequency.

#### Acknowledgements

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#### References

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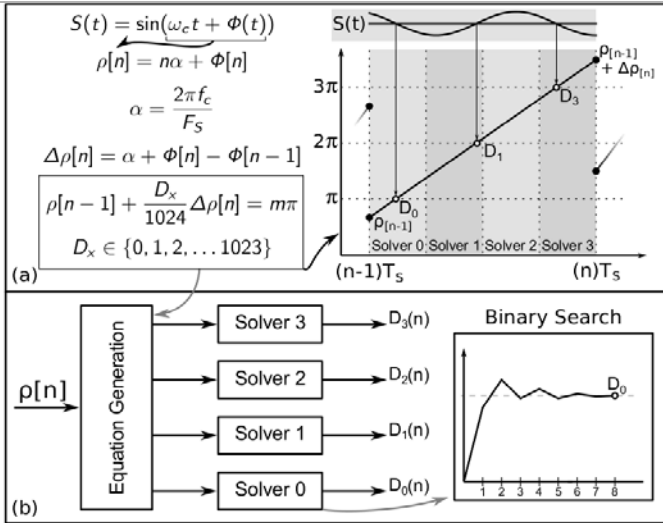


Figure 13.5.1: (a) The conceptual operation and (b) implementation of linear interpolation for the phase modulator.

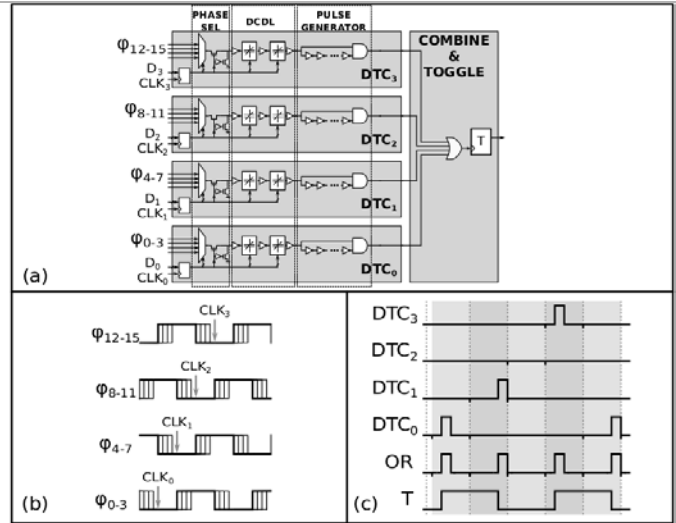


Figure 13.5.2: (a) Block diagram, (b) clocking scheme and (c) timing diagram of the phase modulator.

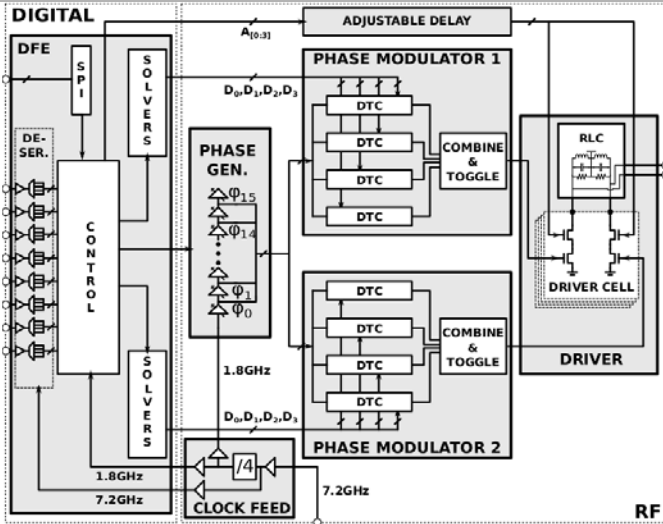


Figure 13.5.3: Block diagram of the transmitter.

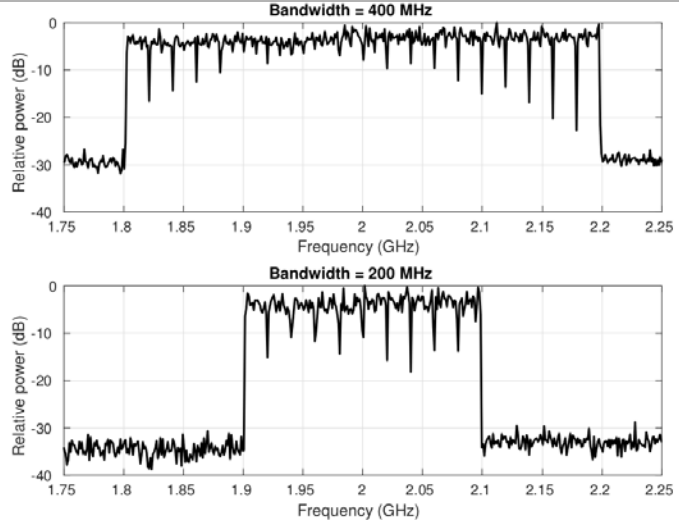


Figure 13.5.4: Measured spectra with 400 and 200MHz bandwidth signals at 2GHz carrier frequency.

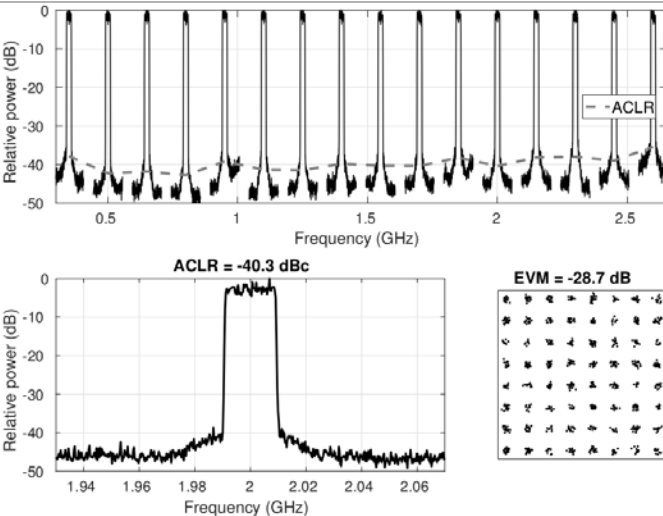


Figure 13.5.5: Measurement results with 20MHz bandwidth at carrier frequencies of 0.35 to 2.6 GHz with constant 1.8GHz sample rate.

	[3]	[4]	[5]	This Work
Transmitter Architecture	Outphasing	RF-PWM	Outphasing	Multilevel Outphasing
Techonology (nm)	32	40	45	28
Integration Level	Modulators + PA	Modulators + Driver	Modulators + Driver	Modulators + Driver
Digital Predistortion	LUT	No	No	No
Power Consumption (mW)	82 (w/o PA)	91 <sup>1</sup>	1720	670 <sup>1</sup>
Maximum Bandwidth (MHz)	40	40	133	400
Carrier Frequency Independent of Sample Rate	No	No	No	Yes
Carrier Frequency (GHz)	2.4	0.9–2.6	10	0.35–2.6
PAPR (dB)	8	7.3	6.6	8
ACLR (dBc, BW = 20 MHz) (64-QAM OFDM)	N/A	-30 <sup>1</sup>	-37 <sup>2</sup>	-40 <sup>1</sup>
EVM (dB, BW = 20 MHz) (64-QAM OFDM)	-32	-29 <sup>1</sup>	-33 <sup>2</sup>	-29 <sup>1</sup>

<sup>1</sup> Center frequency at 2 GHz

<sup>2</sup> Measured with 10 MHz signal bandwidth

Figure 13.5.6: Comparison to recently published transmitters with integrated phase modulators.

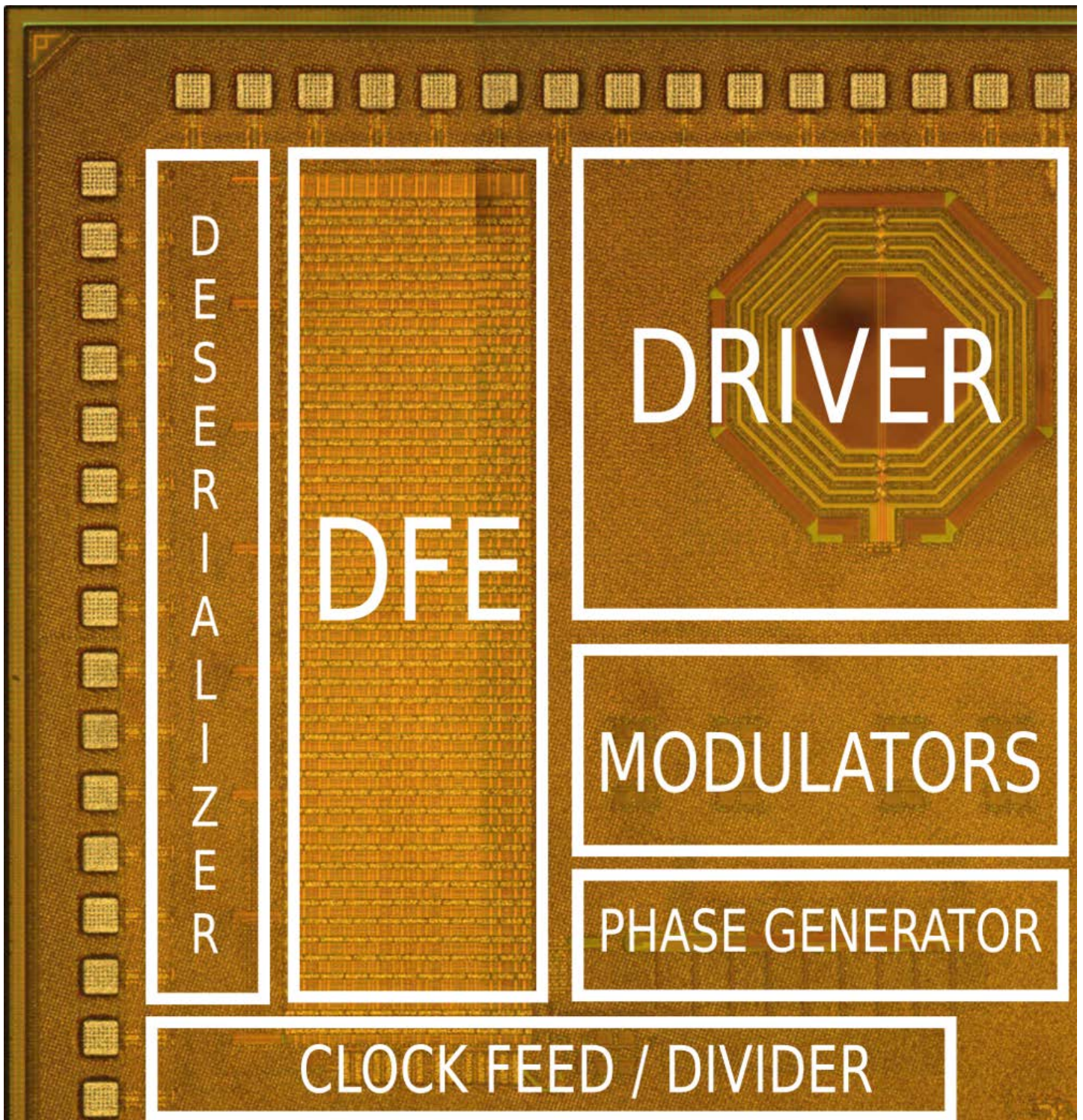


Figure 13.5.7: Die micrograph with highlighted circuit blocks.