Model Predictive Control of the Internal Voltages of a Five-Level Active Neutral Point Clamped Converter

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***Abstract*—In this paper, model predictive control (MPC) is introduced to control the internal voltages of an active neutral-point clamped five-level converter (ANPC-5L). The proposed control scheme aims to keep the neutral point and phase capacitors voltages of the converter within given hysteresis bounds while at the same time minimizing the switching frequency. An additional benefit of the controlled voltages is a reduced level of output current distortion. The large number of redundant states that exist in multi-level converters makes it possible for all the objectives to be achieved. A short horizon is employed in order to ensure a manageable level of complexity. At the same time extrapolation is used to bring the performance to the desired level. Simulation results that substantiate the effectiveness of the proposed approach are presented.**

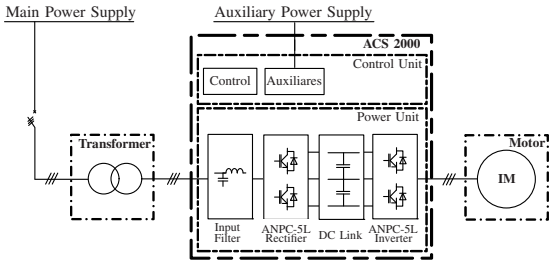
***Index Terms*—five-level converter, neutral-point clamped, model predictive control**

I. Introduction

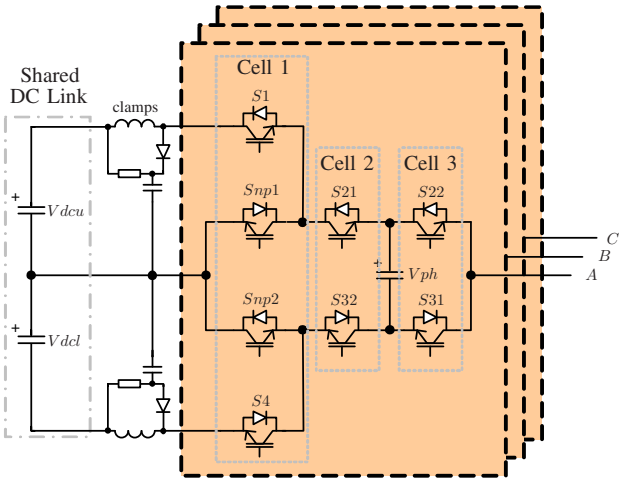
ABB has recently introduced the ACS 2000 shown in Fig. 1(a) for medium-voltage (MV), low power applications such as fans and pumps. The ACS 2000 is based on the five-level active neutral-pointed clamped (ANPC-5L) topology [1], [2] with all the inherent advantages of multi-level converters such as reduced harmonic distortion and lower ratings of the semiconductor switching devices. One of the primary control issues of this converter is the balancing of the voltages of the phase capacitors (PC) and neutral point (NP) (Fig. 1(b)) while at the same time producing the desired output voltage. The proper handling of these often conflicting objectives must be performed within the switching frequency constraints of the semiconductor devices and the output harmonic distortion limits of the driven machine.

Most balancing algorithms in the literature for split DC link converters, such as NPC-3L, are based on carrier based pulse width modulation (PWM), e.g. [3], [4]. In these methods the balancing transitions are part of the PWM process, so the switching frequency is not affected, but a relatively high switching frequency is assumed. In [5], methods of explicitly controlling the NP voltage and common mode current are developed but still space vector modulation (SVM) is assumed, thus it is not obvious how to apply these concepts to a precalculated pulse pattern. Another method was introduced in [6] to balance the NP with no added switchings. Some approaches specifically for the ANPC-5L have also been reported [7], [8], but no mechanism is described for including constraints that would arise in a commercial MV drive.

There are two critical points that determine the total amount of capacitance allowed in MV drives. One is the limitation imposed by the capacitor technology (typically film type) which have a lower capacitance/volume than the electrolytic types used in low voltage converters. Second the stored energy is very high due to the medium voltage level and must be



(a) Drive configuration.



(b) Simplified circuit diagram of an ANPC-5L phase leg showing dv/dt clamp shared by all three phases.

Fig. 1: The ACS 2000 from ABB.

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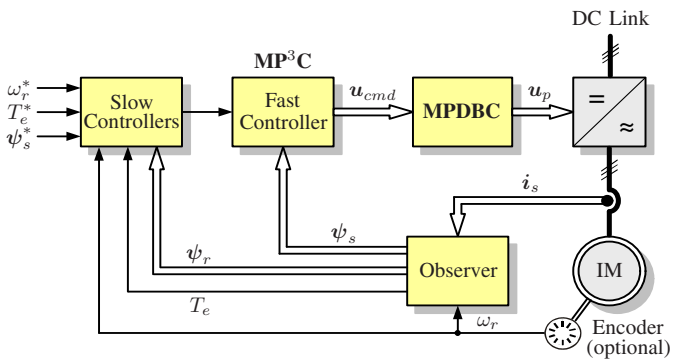


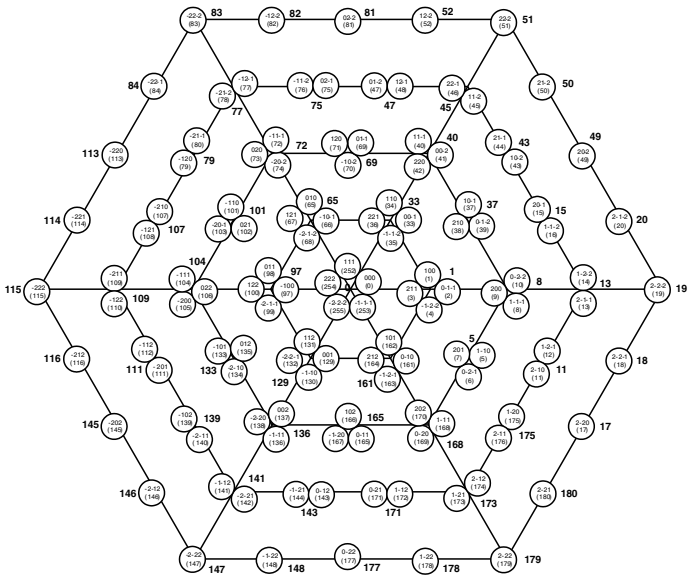
Fig. 2: The simplified controller showing where the internal voltage controller fits into the overall control loop.

limited to avoid device failures during emergency shutdown. As an example, the PC value from the prototype converter in [1] is 300 μF, where in LV drives the value could easily be in the mF range. The voltage balancing task becomes much more challenging with the dual restrictions of low switching frequency and low capacitance values. In addition, it can often be the case that the NP and PC voltages require conflicting phase states to maintain their balance.

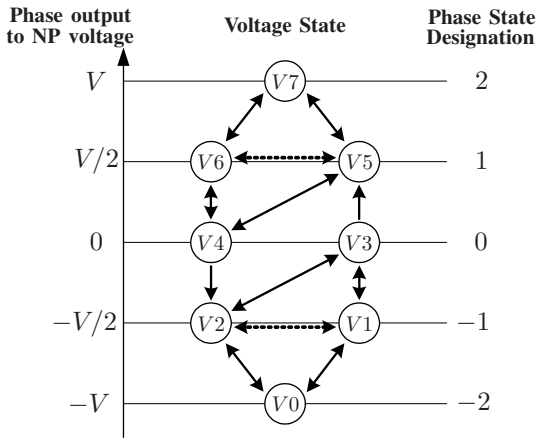
A suitable choice to handle this control problem is model predictive control (MPC) [9], [10]. MPC has been successfully employed in the process industry for more than 30 years, however in power electronic applications it has only recently been gaining more widespread attention [11], [12]. The benefits of MPC include straightforward design, inherent robustness, explicit inclusion of restrictions and very fast transient response. For the remainder of this paper, the term model predictive direct balancing control (MPDBC) will be used.

In this paper, MPC is applied to the control of the internal voltages of the converter. Based on a mathematical model of the circuit an objective function is solved in real-time. At each time-instant the manipulated input is determined by minimizing the objective function of the optimization variable. The sequence of control inputs that results in the best performance is considered to be the *optimal* solution. Only the first element of this sequence is applied to the plant. The remaining elements are discarded and the procedure is repeated at each successive sampling instant based on the most recently acquired measurements, while the horizon is shifted forward by one sampling interval. This procedure forms the feedback loop for the controller and is known as the *receding horizon policy*.

The scope of this paper deals specifically with the last step in the multi-level converter modulation process (i.e. the phase state commands to be sent to the converter switches). In other words, MPDBC selects among the redundant phase states to control the internal voltages and come as close as possible to the commanded output voltage vector $\boldsymbol{u}_{cmd}$. The position of MPDBC in the overall controller scheme is shown in Fig. 2. The single- and three-phase redundancies arising from the ANPC-5L topology are taken into account in order



(a) 3-phase $\boldsymbol{v}$-vectors of the 5-level converter in the $\alpha - \beta$ plane.



(b) Phase states, output voltages and the allowed state transitions of the ANPC-5L.

Fig. 3: Three-phase and single-phase redundancies.

to minimize the switching frequency while satisfying hard and soft constraints imposed on the optimization problem to limit the output voltage distortion and protect the converter circuit. Finally, the horizon is chosen based on a trade-off between the computation time of the proposed algorithm and the system performance.

II. Five-Level Active Neutral Point Clamped Converter

The ANPC-5L multilevel converter contains both single-phase and three-phase redundancies. The inverter unit can produce 61 unique line-to-line output voltage vectors, ($\boldsymbol{v}_{\alpha\beta}$). These unique vectors are produced from the $5^3 = 125$ possible three-phase voltage vectors ($\boldsymbol{v}$-vectors, see Fig. 3(a)). Each set of $\boldsymbol{v}$-vectors ($\boldsymbol{u}_{abc}$) which produce the same output voltage is termed a three-phase redundancy. The normalized $\boldsymbol{v}$-vectors have values in the range: $\{-2, -1, 0, +1, +2\}$. The $\boldsymbol{v}$-vectors are produced at the modulator level and serve as inputs to the

algorithm introduced in this paper. As an example, consider the node labeled 133 in Fig. 3(a). It consists of the following three $\boldsymbol{v}$-vector redundancies: $\{012, -101, -2-10\}$.

Single-phase redundancy exists at the level of the converter phase leg. Two (or more) different phase states can produce the same phase voltage but have different effects on the NP and/or the PC voltage. In other words, if one state causes the indicated voltage to increase, the other state (for the same current sign) decreases it. Fig. 3(b) graphically displays the phase states of the ANPC-5L topology relative to the output voltage of the phase leg of the converter. The five output voltage levels are produced by the eight regular states $\{0-7\}$. Considering the three phases of the inverter, $8^3 = 512$ three-phase vectors or $\boldsymbol{p}$-vectors ($\boldsymbol{u}_{p,abc}$) can be produced by an ANPC-5L converter.

The $\boldsymbol{p}$-vectors contain both the single-phase and three-phase redundancies and are the basis for balancing the internal converter voltages. Consider again node 133 in Fig. 3(a) and further consider the $\boldsymbol{v}$-vector $\{012\}$; it can be produced by any one of the following set of redundant $\boldsymbol{p}$-vectors: $\{457, 467, 357, 367\}$. The $\boldsymbol{v}$-vectors $\{-101\}$ and $\{-2-10\}$ can be decomposed in a similar manner to yield a total of 16 redundant $\boldsymbol{p}$-vectors for one output voltage vector value.

The importance of the redundant vectors, again, is the fact that they can have opposite effects on the capacitor voltages in the inverter. Thus the output voltage can remain unchanged while switching to a state which reverses the voltage slope on a PC or on the NP. Table I shows the relationship between the phase states of Fig. 3(b) and the sign of the voltage slope on the internal voltages. Assuming a positive current in phase x where $x = \{a, b, c\}$, the sign of the slope for the PC voltage is noted by p_{phx} and for the NP voltage by p_{np}. It is important to note that the NP voltage depends on all three phases while the PC voltage depends only on its own phase current.

In the existing balancing algorithm, hysteresis bands are used to limit the NP voltage error without introducing excessive switchings in the process. The behavior is as follows: if the NP voltage error is within the innermost band, nothing is done; the commanded voltage vector is forwarded to the modulator. If it crosses the first band, a vector is selected to balance the NP without an additional switching. Once the NP voltage error crosses the second band an additional switching is forced to keep the voltage in bounds.

The PCs must also be taken into account at each vector selection according to an additional set of upper and lower bounds. To keep the error in bounds the redundant phase state which minimizes the error is chosen, if possible. If there is a conflict with that required for the NP then a prioritization is done.

The choice of modulator is not considered in this paper although the simulation results are produced using MP^{3}C [13], [14] (see Fig. 2). Any desired modulation method, such as direct torque control (DTC), PWM, optimal pulse patterns (OPPs) can be used, provided that the future outputs can be predicted and passed to the switching state selection algorithm introduced in this paper. The next section describes the model which is used to evaluate the effect of a set of voltages states on the internal voltages and the proposed MPC method.

TABLE I: Phase states and effects on PC and NP for positive phase current

$\boldsymbol{p}$-vector	p_{phx} $i_{phx} > 0$	p_{np} $i_{phx} > 0$
$V7$	0	0
$V6$	$+1$	0
$V5$	-1	-1
$V4$	0	-1
$V3$	0	-1
$V2$	$+1$	-1
$V1$	-1	0
$V0$	0	0

III. Modeling for Controller Design

The discretized NP and PC voltage error evolution serve as the internal prediction model. The general error voltages are defined as

$$v_{m,err} = v_{m,ref} - v_m \,, \tag{1}$$

where v_m is the measured voltage and $v_{m,ref}$ is the reference value of the voltage and m can be np for the NP or phx for the PC of phase x where again $x = \{a, b, c\}$.

Using forward Euler approximation the discrete-time NP voltage error is given by:

$$v_{np,err}(k+1) = v_{np,err}(k) + K_{cnp}\boldsymbol{p}_{np}(k)\boldsymbol{i}_{ph}(k) \,, \tag{2}$$

where $v_{np,err}$ is the NP voltage error, and $K_{cnp} = T_s/C_{\text{dc}}$ is the capacitor constant, where T_s is the sampling time and C_{dc} the effective dc link capacitor value. The 1×3 vector $\boldsymbol{p}_{np} \in \{-1, 0\}$ takes into account the effect of each phase current on the NP voltage, where "0" corresponds to the case where $v_{np,err}$ is unaffected, and "-1" to the case where $v_{np,err}$ decreases with a positive phase current. In Table I the effect of each p-vector on the NP voltage is summarized. Finally $\boldsymbol{i}_{ph}$ is a 3×1 vector representing the three phase currents.

The PC voltage error is modeled in a similar fashion. Here the equation is shown for phase a:

$$v_{pha,err}(k+1) = v_{pha,err}(k) + K_{cph}p_{pha}(k)i_{pha}(k) \,, \tag{3}$$

where $v_{pha,err}$ is the PC voltage error of phase a; the capacitor constant K_{cph} is given by $K_{cph} = T_s/C_{\text{ph}}$, where C_{ph} is the PC value. For $p_{pha} \in \{-1, 0, +1\}$, "0" corresponds to the case where the PC is not affected, "-1" to the case where it discharges with positive phase current, and "$+1$" to the case where it charges with positive phase current (see Table I). Equation (3) is repeated for the other two phases, i.e. $v_{phb,err}, v_{phc,err}$.

IV. Model Predictive Control

The control objective of the described MPC algorithm in more precise terms is to keep the NP and PC voltages inside their bounds while producing the least possible volt-second error in the output voltage and operating the converter at the lowest possible switching frequency. In order to meet these control objectives the topology redundancies must be effectively taken into account. At each time step the previously

selected switching state command is the starting point for the controller. From this $\boldsymbol{p}$-vector an exhaustive search tree containing all the valid switching trajectories is generated. The primary goal is than to select an optimal trajectory containing the commanded next output voltage $\boldsymbol{u}_{abc,cmd}$.

A. Constraints

To properly formulate the control problem the control related constraints must be understood. The constraints are divided into two main categories: a) the switching constraints, and b) the NP and PC voltage constraints. The former are hard constraints, i.e. they cannot be violated under any circumstances, while the latter are soft constraints, i.e. they can be violated, but control effort should be applied to avoid such violations.

The switching constraints stem from the topology of the converter and the three main restrictions are described in brief below:

- **Minimum pulse time duration**: the on-time and off-time of each semiconductor switch cannot be less than a specified value.
- **Allowed state transitions of the converter phase leg**: the allowed transitions are indicated in Fig. 3(b) with arrows. Note that some transitions are only allowed in one direction.
- **DC link clamp restrictions**: the minimum allowed time between transitions affecting the clamp depends on how the clamp diode is affected. The range is between 0 and a specified value.

Any switching transition from one $\boldsymbol{p}$-vector to another that meets the above conditions is considered switching feasible (SWF). When considering a set of $\boldsymbol{p}$-vectors, all transitions in the set must meet the above conditions to be considered switching feasible.

The soft constraints on the internal voltages are implemented as two sets of bounds. The first bounds are defined by the desired maximum absolute deviation from the respective reference voltage values (*inner* bounds) and the second wider bounds are set by the allowed physical limits of the semiconductor devices (*outer* bounds).

Typically the upper and lower bounds on the PCs are set such that the devices of Cell 2 and 3 are protected from overvoltage. A better understanding of the issues involved can be gained by examining Fig. 1(b). The PC voltage V_{ph} is connected to the output either through $S22$ or $S31$. Thus from a physical point of view the allowable upper limit on this voltage depends on the safe limits of the devices, $V_{dev,max}$. In other words, the upper limit on the PC voltage must be less than $V_{dev,max}$. To set the lower limit, it must be ensured that $V_{dcu} - V_{ph}$ is less than $V_{dev,max}$ across $S32$, considering phase state $V6$ and assuming $V_{dcu} = V_{dcl}$. Therefore the limits on the range of the PC voltage are $V_{dev,max} > V_{ph} > V_{dcu} - V_{dev,max}$, if the NP is balanced. The NP bounds are made as large as possible to minimize the needed switching, but small enough to limit distortion on the output voltage [4].

B. Control Approach

In accordance with the MPC framework, the *switching trajectories* over the prediction horizon N_p are taken as the optimization variable. A switching trajectory is a sequence $\boldsymbol{U}_p$ of switch positions $\boldsymbol{u}_p = [u_{pa}\ u_{pb}\ u_{pc}]^T$, represented as a set of $\boldsymbol{p}$-vectors, i.e. $u_{px} \in \{0, 1, \ldots, 7\}$, with $x \in \{a, b, c\}$, over the time interval of length N_p, i.e. $\boldsymbol{U}_p(k) = [\boldsymbol{u}_p^T(k)\ \boldsymbol{u}_p^T(k+1) \ldots \boldsymbol{u}_p^T(k+N_p-1)]^T$. Based on (2) and (3), the evolution of the voltage errors is calculated over the prediction horizon N_p. The number of computations at each time step increases exponentially with the length of the horizon, thus the computational complexity must be taken into consideration at this point. The horizon must be kept relatively short, but must be long enough to accurately capture the dynamics of the variables of concern. To resolve this apparent contradiction the notions of the switching horizon N_s and extrapolation are introduced. The switching horizon is set equal to $N_s = 2$, implying that switching is considered only at time steps $k+1$ and $k+2$, followed by an extrapolation step where it is assumed that the switch position from $k+2$ to $k+N_p-1$ stays the same. This is referred to as SSE (for more details see [12], [15], [16]).

The proposed control algorithm comprises the following steps, executed at time instant kT_s.

Step 1: The set of switching trajectories to be evaluated is selected from the $\boldsymbol{p}$-vectors which can be reached from the previously commanded $\boldsymbol{p}$-vector (step $k-1$). All earlier commanded switchings are neglected in a first step and each phase is assumed to switch once in the two-step horizon. A consequence of this is that the minimum pulse width restriction and the allowed phase transitions (the first and second switching constraints, respectively) are taken *a priori* into account. The exhaustive search tree thus created always consists of 343 switching trajectories[1] greatly benefiting the implementation in hardware.

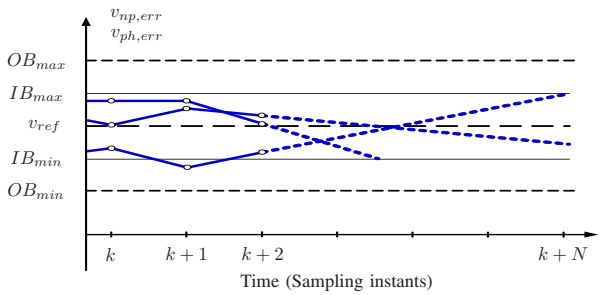
Next, each trajectory in the search tree is examined for violations of the restrictions that depend on measured data and the history of the converter states. Thus, the timing restrictions stemming from the commanded $\boldsymbol{p}$-vector at $k-2$ and the clamp transitions from the previous states of the upper and lower clamps are treated. These checks can only be done in real-time since they depend on either the measured current or the past states of the converter to identify a violation.

Step 2: The evolution of the NP and the PC voltages is calculated using (2) and (3), respectively, for each identified SWF trajectory.

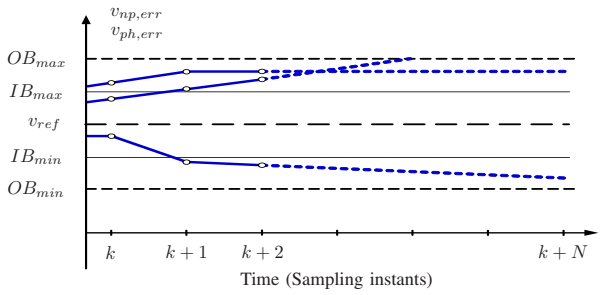
Step 3: The internal voltages are extended by linearly extrapolating the predicted voltage values from steps $k+N_s-1$ and $k+N_s$. The number of steps, $N_p - N_s$, after which the *first* crossing of the upper or lower *inner* bound will occur by the respective predicted voltage (see Fig. 4) is then estimated.

Step 4: The switching trajectories are then grouped hierarchically according to certain feasibility criteria. Each group can have different conditions of optimality, providing great

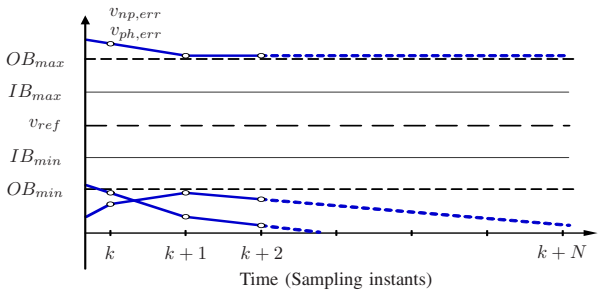
[1] In Appendix the derivation of the search tree is explained.



(a) Voltage switching trajectories illustrating (IBF or GD) or (IBF at step k and GD at step $k+2$).



(b) Voltage switching trajectories illustrating OBF and not GD over all horizon steps.



(c) Voltage switching trajectories illustrating neither OBF, nor GD over all horizon steps.

Fig. 4: Examples of internal voltage switching trajectories that illustrate the feasibility criterion and the effect of extrapolation ($N >> N_s$).

flexibility in the controller design. Four basic feasibility criteria are described here (see Fig. 4 for graphical examples):

- Inner bounds feasibility criterion (IBF): true when the voltages are inside the inner bounds.
- Outer bounds feasibility criterion (OBF): true when the voltages are inside the outer bounds.
- Zero volt-seconds error criterion (ZVS): true when the error between the switching trajectory $\boldsymbol{v}$-vectors and the $\boldsymbol{v}$-vectors commanded by the modulator is zero for all time steps.
- Good direction criterion (GD): true when the slopes of the NP and PC voltages are pointing towards their respective reference values.

The trajectories are grouped according to combinations of these criteria to best achieve the control objectives. To help demonstrate some grouping possibilities, in the remainder of this section two different approaches will be presented.

First Approach: In this approach the grouping criteria are designed such that the PC voltages will mostly stay within the inner bounds. The result of this choice is to increase the switching frequency. The selection criteria for the first approach are the following:

I. The top level of the hierarchy consists of the most desirable trajectories. They satisfy the following logical criteria: SWF, OBF, ZVS and (IBF or GD at all time-steps).
II. The second level is formed by the trajectories that are SWF, OBF and do not have GD but are ZVS.
III. The third level includes the trajectories that are OBF and SWF.
IV. Finally, all the remaining trajectories, i.e. those that are SWF and not OBF form the lowest level of the hierarchy.

Second Approach: For the second approach the bound constraints are relaxed; only the outer bounds are taken into consideration. As a result, the switching frequency will decrease relative to the first approach at the expense of a higher PC voltage ripple. The switching trajectories are grouped in the following way:

I. The top level of the hierarchy consists of the trajectories that are SWF, OBF, and ZVS.
II. The second level contains trajectories that are SWF, and ZVS, but outside the outer bounds, i.e. not OBF.
III. The third level is formed by the trajectories that are SWF and inside the bounds (OBF), but not ZVS.
IV. The lowest level of the hierarchy includes all the trajectories that are only SWF, i.e. the remaining trajectories.

The selection criteria for both approaches are summarized in Table II.

TABLE II: Selection Criteria

Level	First Approach	Second Approach
I	SWF & OBF & ZVS & (IBF or GD)	SWF & OBF & ZVS
II	SWF & OBF & ZVS	SWF & ZVS
III	SWF & OBF	SWF & OBF
IV	SWF	SWF

Step 5: Finally the optimal trajectory is selected starting from the highest possible level of the hierarchy in a mutually exclusive manner. If a trajectory meets all the corresponding feasibility criteria, then it belongs to the top level. If only one trajectory belongs to the top level, then it is selected as optimal. If others exist, then more criteria are taken into account to select the optimal trajectory. If there are no trajectories in the top level, then the optimal trajectory is selected from the second level. If this level is also empty, then the selection is made from the third level and so on.

C. Costs

Each level has one or more objective functions which are applied to the trajectories meeting the respective selection criteria in terms of costs.

First Approach: The cost functions for the first approach are the following:

- The cost function for the top level is the total number of weighted switch transitions Sw in the trajectory $\boldsymbol{U}_p$. The optimal trajectory is given by:

$$\boldsymbol{U}_p^*(k) = \text{argmin } Sw(k)\,, \tag{4}$$

where

$$Sw = s/N_p + q v_{np,err,extrap}^2\,, \tag{5}$$

and

$$s(k) = \sum_{\ell=k}^{k+N_s-1} ||\boldsymbol{u}_p(\ell) - \boldsymbol{u}_p(\ell-1)||_1\,, \tag{6}$$

is the total number of switch transitions in the switching trajectory $\boldsymbol{U}_p$. The variable q is a weighting factor on the NP voltage penalty [17], $v_{np,err,extrap}$, which is the NP voltage at N_p.

If the second level includes more than one trajectory and the top level is empty:

- The maximum exceedance of the inner bounds over all time steps and all voltages is taken into account. The optimal trajectory is the one which results in the smallest maximum exceedance, i.e.,

$$\boldsymbol{U}_p^*(k) = \text{argmin } ||\boldsymbol{v}_{ib,err}(k)||_1\,, \tag{7}$$

where

$$\boldsymbol{v}_{ib,err}(k) = \sum_{\ell=k}^{k+N_s} \boldsymbol{v}_{ib,err}(\ell)\,, \tag{8}$$

with

$$\boldsymbol{v}_{ib,err}(\ell) = \begin{cases} |\boldsymbol{v}_{m,err}| - \boldsymbol{v}_{m,ib}, \text{if } |\boldsymbol{v}_{m,err}| - \boldsymbol{v}_{m,ib} > 0 \\ 0 \qquad\quad , \text{otherwise} \end{cases} \tag{9}$$

where $\boldsymbol{v}_{m,ib}$ is the vector of the respective inner bounds and $\boldsymbol{v}_{ib,err}$ is the vector of all the internal voltages (m = np, pha, phb or phc) over N_s. All operations are completed element-wise on the vectors.

If the third level includes more than one trajectory and the higher levels are empty:

- The trajectory $\boldsymbol{u}_{abc,MPC}$ that has the least deviation from the voltage vectors that are commanded by the modulator, $\boldsymbol{u}_{abc,cmd}$, over all time steps is optimal, i.e.

$$\boldsymbol{U}_p^*(k) = \text{argmin } v_{vs}(k)\,, \tag{10}$$

where

$$v_{vs}(k) = \sum_{\ell=k}^{k+N_s} ||\boldsymbol{u}_{abc,MPC}(\ell) - \boldsymbol{u}_{abc,cmd}(\ell)||_1\,, \tag{11}$$

and $\boldsymbol{u}_{abc,MPC}$ are the $\boldsymbol{v}$-vectors of the examined switching trajectory and thus v_{vs} is equivalent to the volt-second error over the trajectory.

If the fourth level consists of more than one trajectory and the three upper levels are empty:

- The same cost function as that of the second level is reformulated in terms of the outer bounds (i.e. replace ib by ob in (7), (8) and (9)).

Second Approach: Repeating the same procedure the respective cost functions for this approach are:

- For the top level group, the optimal trajectory is again given by (4). If more than one trajectory results in the same minimum Sw, then the trajectory with the fewest switching events in the first time step is selected.
- If still no unique optimal solution is found, then the optimal trajectory is the one with the minimum NP voltage error at time-step $k+1$

$$\boldsymbol{U}_p^*(k) = \text{argmin } v_{np,err}(k)\,, \tag{12}$$

where $v_{np,err}$ is given by (2).

Following the same procedure as in the first approach, if the second level includes more than one trajectory and the top level is empty:

- The optimal trajectory is the one with the minimum sum of the absolute PC voltage exceedances of the inner bounds over the horizon for each horizon step, i.e. the trajectory given by (7), with only the PC voltages taken into account (m = pha, phb or phc). If there is still no unique optimal trajectory, then (7) is again used, but this time with only the NP voltage considered (m = np).

If the third level consists of more than one trajectory and the two upper levels are empty:

- The optimal trajectory is given by (10). If more than one optimal trajectory is found, then trajectory with the minimum number of switchings at time-step $k+1$ is selected (see (4)).

In the case where the fourth level includes more than one trajectory and the higher levels are empty:

- The first optimality criterion is again (10). However, if the optimal solution is not unique, then the optimal trajectory is given by (7), where all the voltages (m = np, pha, phb or phc) over the horizon for each horizon step are taken into account.

V. Computational Complexity

One of the difficulties in using MPC is the fact that the computational complexity increases exponentially with the length of the horizon. For example, with $N_s = 2$ the number of vectors to be searched is 343, but if it is increased to $N_s = 3$ the number of vectors becomes 6859 using the same tree building algorithm described in the appendix. But, even with only two steps in the horizon the algorithm must be implemented in a field-programmable gate array (FPGA) and a full pipelined approach must be used to minimize the use of the FPGA resources. Additional parallelization allows execution of the full algorithm in about $9.4\,\mu$s which is well below the $25\,\mu$s limit of the controller cycle time. The proposed algorithm also had to be compiled with the existing code including all other functionality required for the full MV drive.

Most modern MV drives have a digital signal processor (DSP) and FPGA combination on their controller boards. Furthermore FPGAs are becoming larger, faster and less expensive every year. Thus the required computational power for MPC is readily available in these power converters. In the

case of the current algorithm, the available controller board contains an FPGA with $33,000$ equivalent logic cells and 36 hardware multipliers.

VI. Delay Compensation

In any digital control system a delay exists between the time instant that measurements are made and the time instant that these values are delivered to the controller. In the implemented simulation model of the algorithm, the cycle time is assumed to be $25\,\mu$s as previously mentioned. This is used as the basis for correcting the delays in the measured inputs using the same model as described in (2) and (3). To achieve the best results from the predictive controller (any controller in fact) the measurement delays must be compensated and synchronized so that they correspond as closely as possible to current time instant.

As an example, the PC voltage compensation equation will be developed. If it is assumed that the delay in the voltage measurement is $75\,\mu$s (i.e. three samples) then the measurement corresponds to time-step $k-3$. The values of p_{phx} from $k-2$ and $k-1$ must also be saved as part of the algorithm so they are available for the calculation. The PC voltage equation in (3) is modified using the same variables to give the following equation for predicting the value at step k by setting $n_{dly}=3$:

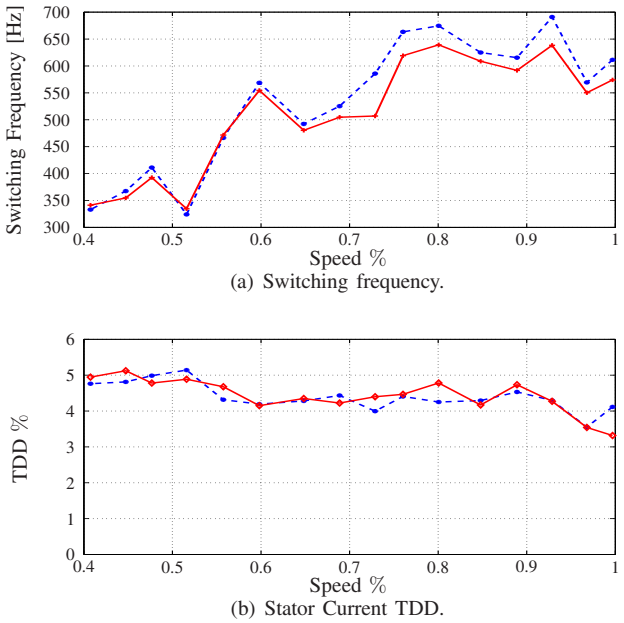
$$v_{phx}(k) = v_{phx}(k-n_{dly}) + K_{cph}\Big(\sum_{\ell=k-n_{dly}}^{k-1} p_{phx}(\ell) i_{phx}(\ell)\Big), \tag{13}$$

where x again represents the phase and $v_{phx}(k-n_{dly})$ corresponds to the measured voltage. The performance of this compensation block will be shown in simulation in the next section.

VII. Performance Evaluation

Simulation results are presented in Figs. 5 and 6. The performance of the new algorithm for the second approach is compared to the existing balancing algorithm (described in section II) in Fig. 5 in terms of the switching frequency and the total demand distortion (TDD) of the stator current. The control algorithm was operated with a sample time $T_s = 25\,\mu$s. The simulation conditions for all cases consist of an induction machine driving a quadratic torque load with flux and torque control provided by MP^{3}C [13], [14]. The type of machine used in the simulations is a general purpose motor with a relatively low per unit transient reactance of 18%, a rated current of $137\,$A and a rated frequency of $50\,$Hz. In Fig. 6 the waveforms of the voltages of the NP and the PC of phase a are shown.

The overshoot of the PC voltage seen in Fig. 6 is due to the uncompensated measurement delays in the simulation. For the NP voltage the delay is negligible because of its slower dynamics. This can also be seen in Fig. 6 since the NP voltage hardly violate the bounds despite the presence of the measurement delays. The delay compensation has only been implemented in the simulation for the PCs since they have the most critical dynamics. In Fig. 7 the actual PC voltage is



(a) Switching frequency.

(b) Stator Current TDD.

Fig. 5: Simulation results of the proposed control strategy over a range of operation comparing proposed balancing algorithm (red solid line) to the existing solution (blue dashed line).

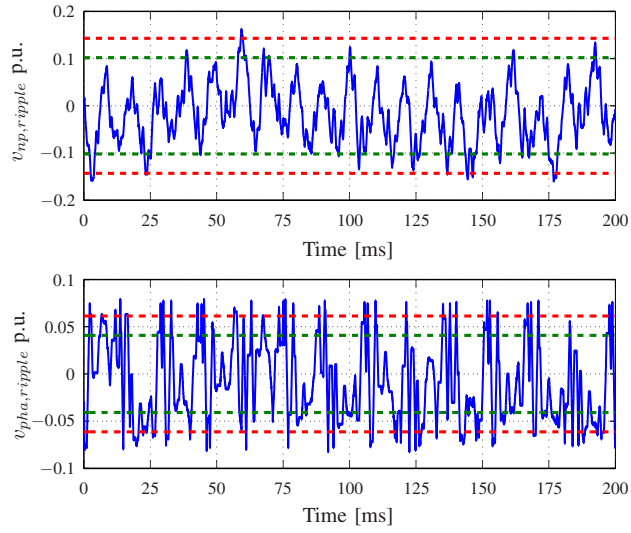


Fig. 6: Simulations results for per unit ripple of internal voltages with the inner (green) and outer (red) bounds. Operating point: 65% speed ($32\,$Hz), 42% load.

shown in comparison to the delayed and sampled data and the compensated data. It is clear that the compensated voltage is much closer to the real value. The PC voltage with the delay compensation enabled is shown in Fig. 8. It can be seen that the controller more accurately limits the voltage ripple inside the bounds. As a consequence the bounds have been increased to keep the switching frequency the same. Overall it can be seen that the voltages are kept close to the bounds and the switching frequency is reduced while maintaining the TDD of the current at an acceptable level.

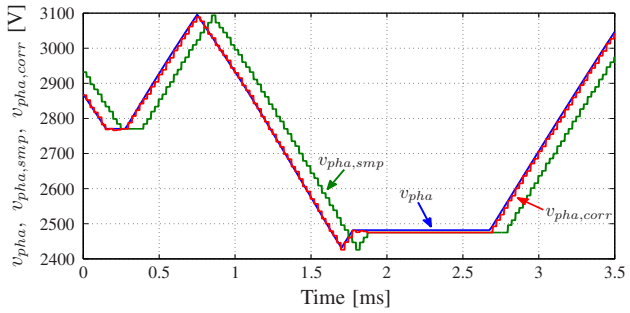


Fig. 7: The actual PC voltage of phase a, v_{pha} (blue), compared to the respective sampled phase voltage, $v_{pha,smp}$ (green), and the phase voltage after the delay compensation, $v_{pha,corr}$ (red).

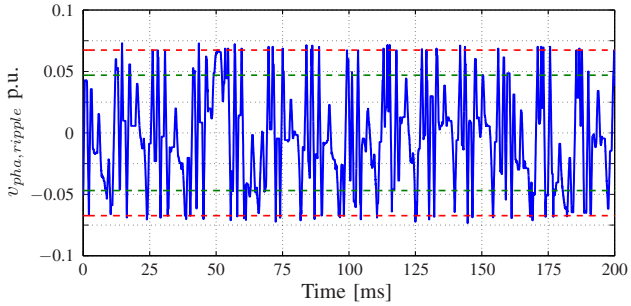


Fig. 8: Simulations results of inner voltages with delay compensation enabled for the PC voltages showing the inner (green) and outer (red) bounds. Operating point: 65% speed (32 Hz), 42% load.

VIII. Conclusions

This paper proposes a model predictive control algorithm for the internal voltages of a five-level active neutral-point clamped converter. The controller maintains the voltages of the NP and the PCs inside the imposed bounds, while reducing the switching frequency by effectively exploiting the redundancies. In addition the topology and implementation based constraints are easily taken into account. Two example design approaches are developed showing the straightforward design procedure. Finally, because of the short switching horizon used and a fully pipelined approach to the implementation, it has also been shown to be within the capability of the existing control hardware for a commercial MV Drive.

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Appendix

Starting from any single-phase state the phase leg can switch to a maximum of four different next states (including the present state). For example, if phase state $V3$ from Fig. 3(b) is examined, the next state can be $V1$, $V2$, $V3$ or $V5$. From the point of view of real-time VHDL implementation at each time step the number of examined states should always be the same so the execution time is fixed. Thus for phase state $V7$ the next state table will contain the following entries: $V5$, $V6$ and $V7$ repeated twice to keep four entries.

The search tree is calculated by taking into consideration eight different switching combinations within the two-step horizon: 1) at step $k+1$ all three phases switch, i.e. $4^3 = 64$ trajectories, 2–4) at step $k+1$ only one phase (a, b, or c) switches, while the other two phases (bc, ca, or ab, respectively) switch at step $k+2$, i.e. $3 \cdot 3 \cdot 4^2 = 144$ trajectories, 5–7) at step $k+1$ two phases (ab, bc, or ca) switch, while the other phase (c, a, or b, respectively) switches at step $k+2$, i.e. $3 \cdot 4 \cdot 3^2 = 108$ trajectories, 8) all three phases switch at step $k+2$, i.e. $3^3 = 27$ trajectories. In total, 343 trajectories are generated at each time step.

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