

The effect of USB ground cable and product dynamic capacitance on IEC61000-4-2 qualification

Pasi Tamminen, Prof. Leena Ukkonen, Prof. Lauri Sydänheimo

Electronics and Computer Technology department, Tampere University of Technology, Finland
tel.: +358-50-5262479, e-mail: pasi.kr.tamminen@microsoft.com

50 Words Abstract – IEC61000-4-2 discharge stress levels are studied with varying product capacitance and ground connections. Stress levels are evaluated based on the measured and simulated peak current, peak power, pulse rise time, and energy transfer along to the USB cable. These stress parameters can be significantly affected by adjusting the test setup.

I. Introduction

One part of electromagnetic compatibility (EMC) qualification of electronic products is the IEC61000-4-2 electrostatic discharge (ESD) immunity test [1]. The repeatability and accuracy of the test method has been extensively studied, as it is one part of electronic system EMC acceptance procedures [2]-[7]. It has been found that different ESD generator models have variation between the stress levels, holding the pulse generator in different positions changes the stress level, calibration procedures have variation, and environment parameters, such as the relative humidity and air spark parameters, effects on the test results [3]-[7]. Based on these analyses a measured product immunity level can vary when different ESD generators and different test locations are used. However, the repeatability is better when the same user and generator is used with the qualification tests [6,7].

There is less information available on how physical construction and positioning of the product on the test bench effects the ESD stress levels [8,9]. Equipment under test (EUT) are placed on the test bench in different positions having varying materials facing towards the horizontal coupling plate (HCP) and the vertical coupling plate (VCP). The product can have also a power supply and data wire connections providing a ground path during the tests. These wires can lay directly on the HCP or be kept far away from the HCP and other ground reference planes. On the other side, battery operated equipment are not grounded via cables, and the only way to stress these devices with ESD pulses is to have a capacitive coupling between the generator, coupling plates and the EUT. Care must also be taken to return capacitively coupled EUTs to ground potential between stresses. Therefore, ESD stress level depends both on the used test setup and construction of the EUT.

In this paper we study with simulation and measurement methods how the IEC61000-4-2 ESD stress level is

affected when different Universal Serial Bus (USB) ground cables and a capacitance of the EUT is varied on the test bench. The study is based on an ESD failure case where small changes in a product's metallic enclosure design changed the results of the ESD immunity test. The failure occurred only when the EUT had a certain USB data cable placed in a specific position on the test bench. The failure type was due to the excess discharge energy content with the USB interface components, and it was questioned whether the failure was based on test method uncertainties, variation of the test setup or due to product design changes. The fast initial part of the IEC discharge is not studied in detail in this work as the focus is with the effect of the high energy content pulse flowing through the EUT ground contact.

Test setups, simulation and measurement methods are presented in Chapter II and the measurement and simulation results are presented in Chapter III. Finally, the results are summarized and conclusions given in Chapters IV and V.

II. Measurement and Simulation Setups

A. IEC61000-4-2 measurements

In the IEC61000-4-2 test method the discharge source is an ESD generator having 150 pF source capacitance, and the charge is discharged through the EUT into the electrical ground. Along the discharge path is a 330 Ω series resistor. The discharge current waveform has two main phases. In the first phase is a fast initial peak current from parasitic capacitances of the generator simulates ESD from a small metallic object kept in hand, and the following residual waveform represents a discharge through the tool from the source capacitance of a human body. The first 0.5-10 ns period of the pulse produces a high current and high power stress event with strong electromagnetic interference (EMI)

emissions. The following pulse from 10 ns onwards has a high total energy content possibly damaging and disturbing electronics [2].

To minimize test variations we use one Noiseken ESS-2000AX discharge generator with 150 pF source and 330 Ω serial resistor, the same test bench, and maximum 2 kV discharge voltages to avoid excess radiated noise. Measurements are made in 20 - 30 % RH environment with contact discharges. Discharge current waveforms are measured with a 1 Ohm shunt resistor placed between the end of the USB cable and the conductive surface of the HCP. Current is measured also by using a Tektronix CT1 current probe between the EUT and USB cable.

The waveforms are captured with an 8 GHz bandwidth oscilloscope having 40 GSa speed. In addition, a TREK Model 520 and 541 electrostatic voltmeters and Monroe 284 Nanocoulomb meter are used to measure static voltages and charges.

More than 15 different USB2 cables were analyzed, and in this paper we present results for six of those cables. The shortest 13 cm long cable has no ferrite beads and the longest 2 m cable has two beads attached. 78 cm and 110 cm long cables both have two versions with and without a ferrite bead. The 13 cm long cable represents a short ground connection without extra EMC filtering and the 2 m long cable with two ferrite beads provides the strongest filtering. In addition, the type of ferrite beads vary between the USB cables. This was observed from the filtering response of the beads between similar cables from different suppliers. The beads should be used to filter only the power Vbus and ground signal lines, and even then with care [10,12]. USB3 type of cables cannot have ferrite beads anymore due to the signal integrity requirements.

USB2 cables can have major variation in the internal construction due to the different ground connections between the metallic shields and the end connectors. Only three of the tested cables; 13 cm, 2 m and 78 cm long without a ferrite, had the shield strap connected on the USB connector on both ends of the cable. This is according to the cable specification as the shield can be connected to an equipment chassis also via a shunt capacitor. However, in this study the signal ground and the shield are connected together at the one ohm shunt resistor connection point, and the two USB data lines and voltage supply wires are kept electrically floating.

In addition to the different cable lengths, the capacitance of the USB cables above the HCP surface is varied. The measurements are made by taping the cables in contact with a 0.8 mm thick dielectric sheet on the HCP, and with the cable raised 3.3 mm above the HCP by using an additional 2.5 mm thick Polyethylene (PE) sheet with a dielectric constant of $\epsilon_r = 2.5 \pm 0.2$. Similar PE sheets are used to vary the capacitance of the EUT on the HCP. The 0.8 mm thick dielectric sheet had the dielectric constant of $\epsilon_r = 2.0 \pm 0.1$.

EUTs are modelled with stainless steel metal plates having a size of 12x12 cm and 12x21 cm. These represent electronic products such as hand held computers with large size displays facing down on the HCP. The metal plates are

used instead of real products for easier modeling of the conductivity and dynamic capacitive coupling phenomena, and to avoid variation caused by product construction [9]. The test setup is shown in Figure 1.

EUTs with USB cables may not have good ground contact during IEC qualification. For example, the cable may be connected into a power supply with mega ohm level resistance to ground. In that case there will be only limited charge transfer along the cable due to the parasitic capacitance of the cable. In contrast, the cable can be connected into a system where the USB port is hard grounded to the system chassis. In this study the cable is always grounded to the HCP to get the maximum energy transfer along the ground connection.

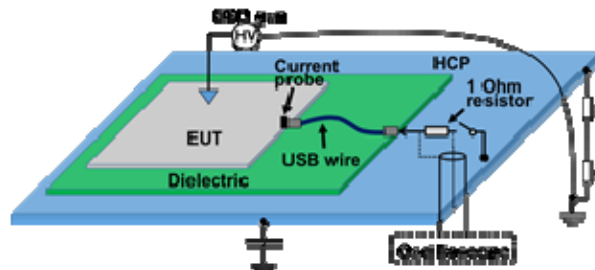


Figure 1: Test setup.

B. Simulation Methods

Test setups are simulated with SPICE and CST Microwave Studio software. Here the target is not to try to produce exactly the same waveforms as found with measurements. This would be challenging as the detailed discharge waveforms vary between different ESD generators, between the cables and type of EUTs used. Instead, the purpose of simulations is to verify the results seen with measurements and to study how different test setup changes should effect the discharge waveforms. Still, the simulation models are built to represent the measured scenarios on a general level.

To produce a realistic simulation with SPICE we need to know resistance-inductance-capacitance (RLC) parameters of the test setup. In this study the RLC values are calculated from measured underdamped discharge current waveforms when a charged metal plate with an USB cable is grounded. In addition, voltage and charge measurements are used to calculate source capacitances and to monitor repeatability of the testing.

A simplified SPICE simulation network is presented in Figure 2 for the USB cable and metal plate combination. The parameter C_{EUT} is the capacitance of the EUT on the test bench, L_{usb} is the distributed inductance, and C_{usb} is the distributed parallel capacitance of the USB cable. Resistors R_{serial} and R_{usb} are selected so that the pulse amplitude and attenuation follow the measured results. The simulation model includes also the USB cable ferrite bead L_3 . The behavior of the ferrite can be simulated by adjusting RLC parameters of the circuit. The HCP is grounded via two 470 kOhm bleed resistors R_{bleed} and inductance L_{bleed} , and the HCP plate has a 180 pF ground

capacitance C_{hcp} . The current through the USB is measured with the resistors R_{1ohm} and $Current_sense$.

The ESD generator is set to give about the same output to a 2 Ohm target as the Noiseken ESD generator used in this study. The generator model is based on two parallel RLC source networks and a gun tip matching circuit.

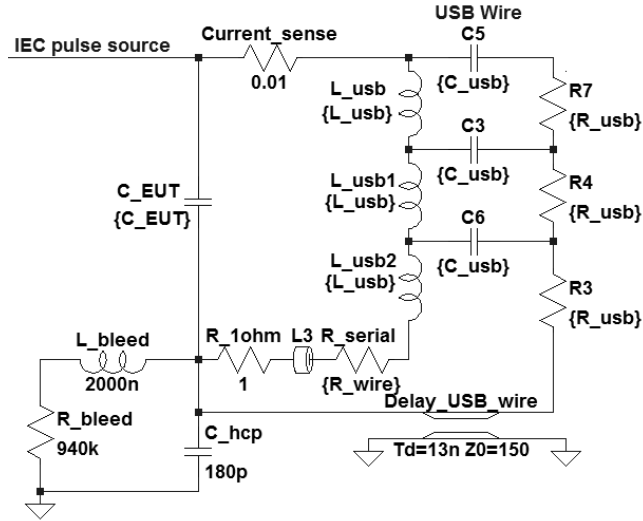


Figure 2: A simplified SPICE simulation circuit for the EUT and USB wire on an IEC61000-4-2 test bench.

Figure 3 shows the 3D model used with CST Microwave time domain co-simulations. The source circuits of the ESD generator and grounding parameters are set on the schematic side. USB cables are modelled with a copper wire on the HCP. The CST co-simulation method is used to construct the test environment. This gives more control over the discharge circuits and reduces the complexity of 3D model.

One of the benefits of 3D simulation is that it can include a detailed mechanical construction of the EUT, and thereby, it can predict how the current and voltage travel through the test setup. In addition, detailed RLC circuit parameters are not required. Instead, a detailed CAD file of the EUT is typically needed and electrical properties of all materials must be known. Non-linear materials such as ferrite beads can be challenging to model in details and these materials may significantly increase simulation time. A test setup with physically long cables requires a large simulation space. To limit the number of mesh cells the space must be shrunk to minimum and that increases uncertainties with simulations.

Complete IEC discharges with slow current attenuation need to be simulated even up to 200 ns, and running through just one simulation may require time from a few hours up to more than one day. Thereby, SPICE based simulations running within just a few seconds can be more practical if the effect of product construction is not part of the study. In this study the EUT is a simple metal plate and the total 3D co-simulation time for one test setup stays below one hour by using a distributed calculation network.

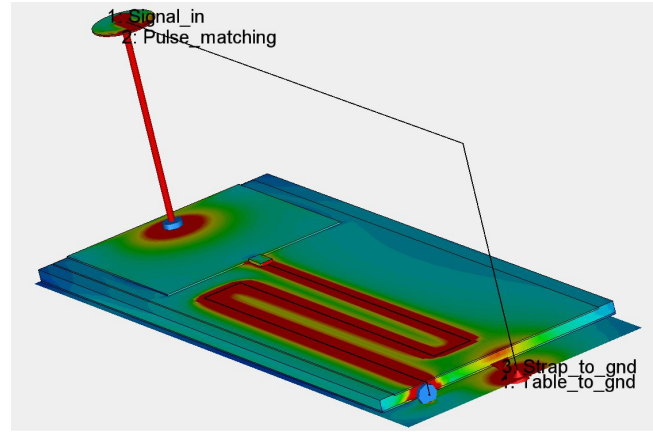


Figure 3: A simplified CST Microwave Studio simulation setup including the ESD source, EUT and USB cable.

C. Uncertainties

An IEC test bench uses 0.5 mm thick dielectric between the EUT and HCP [1]. Different test setups with varying dielectric thickness between the EUT and HCP were tested to analyze uncertainties. A test setup with 0.1 mm dielectric has the real gap between 0.1 mm and 0.2 mm with the 12x12 cm plate and between 0.1 mm and 0.3 mm with the larger 21x12 cm plate. This is due to the small variation with the flatness of the metal plates and USB cables as those are not always laying fully flat against the dielectric. This variation was difficult to avoid and even the use of magnets to pull the plates together was not successful. Finally, 0.8 mm was selected as the thinnest dielectric sheet in this study. With this sheet the EUT capacitance varies less than $\pm 15\%$. With the 0.5 mm dielectric the variation was more than 20%. Figure 4 presents measured quasi-static capacitances for the two metal plates with the 0.8 mm dielectric and with the additional 2.5 mm and 4.5 mm thick sheets. Variation of the EUT capacitance effects mainly the fast coupling currents during the initial part of the IEC61000-4-2 testing [9].

The ESD generator used in the study has ± 100 V variation on the output voltage with 1-2 kV test level. Therefore, the voltage and charge is controlled with the TREK voltage meter and by integrating the total charge transfer from the measured current waveforms. Current waveforms are averages of four ESD pulses for each test setup. Thereby, the total estimated uncertainty is less than $\pm 10\%$ for the measured charges and voltages.

The current has more high frequency bouncing between the EUT and USB cable connection point than between the HCP and cable connection point, and therefore, the 1 Ω shunt resistor is mainly used to capture the current values. The current waveforms are more or less the same in these two points when the cable has a ferrite or when the capacitance of the EUT is high. For cables without ferrites high frequency oscillations may change the waveform, and in that case the current bases on CT1 probe measurements. The peak current and rise time calculation from 10% to 90% has the uncertainty around $\pm 25\%$ due to the ringing of

the waveform during the initial part of the ESD event. The estimated uncertainty with all the other measured values is $\pm 20\%$.

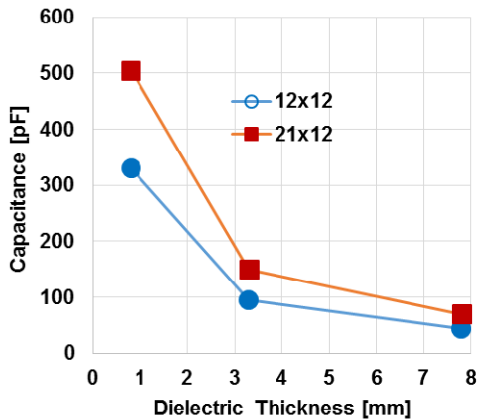


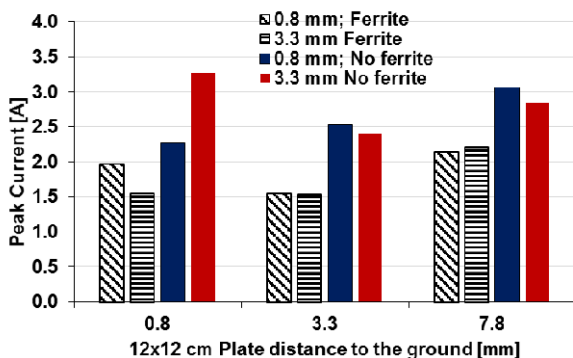
Figure 4: Measured quasi-static capacitance values with 12x12 cm and 21x12 cm plates.

III. Measurement and Simulation Results

ESD can damage electronics in several ways depending on the shape of the current waveform [11]. In this study the main focus is with the current waveform going through the cable. Therefore, we choose the following parameters to compare the severity of the events; peak current, peak power, pulse rise time between 10% and 90%, and the time to transfer 50 % of the total discharge energy.

A. Measurement results

The average discharge peak current, rise time and energy transfer results are presented for the 78 cm long USB cables



in Figures 5, 6 and 7. Results for the 110 cm long cables are presented in Figures 8, 9 and 10. These cables are set at 0.8 mm and 3.3 mm distances from the HCP, and both the 12x12 cm and 21x12 cm size metal plates are set at 0.8 mm, 3.3 mm and 7.8 mm distances from the HCP.

When the plate or USB cable is in a high capacitance position at the 0.8 mm distance to the HCP, the peak current and power are typically less than when they are raised up. The peak power over the one Ohm shunt resistor varies accordingly based on the I^2 of the current value. In addition, raising up only the USB cable can increase the peak current depending on the capacitance of the EUT. The biggest changes can be seen between 0.8 mm and 3.3 mm distances for the plates. The effect of capacitance on the peak current and power is supported also by SPICE simulation results. However, simulations are not always able to predict correctly waveform reflections and non-linear behavior of the ferrites.

The peak current decreases 20 % - 60 % when the cable has a ferrite bead attached. On top of that, the distance between a cable and HCP has less effect on the peak current if there is a ferrite along the cable.

Pulse rise times are faster when the capacitance of the plate and USB cable decreases. This is the case both with and without a ferrite bead, but the type of ferrite bead and the capacitance of the EUT can change the results. For example, the ferrite along 110 cm long cable has only minor effect on the rise time when the EUT capacitance decreases. In addition, the bead along 110 cm cable operates well only with higher frequencies above 20 MHz, which is more than the main frequency of the measured pulses.

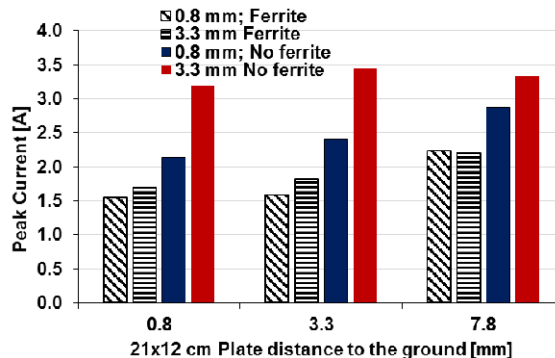


Figure 5: Discharge peak current values with 78 cm long USB cables. 12x12 plate on the left and 12x21 cm plate on the right.

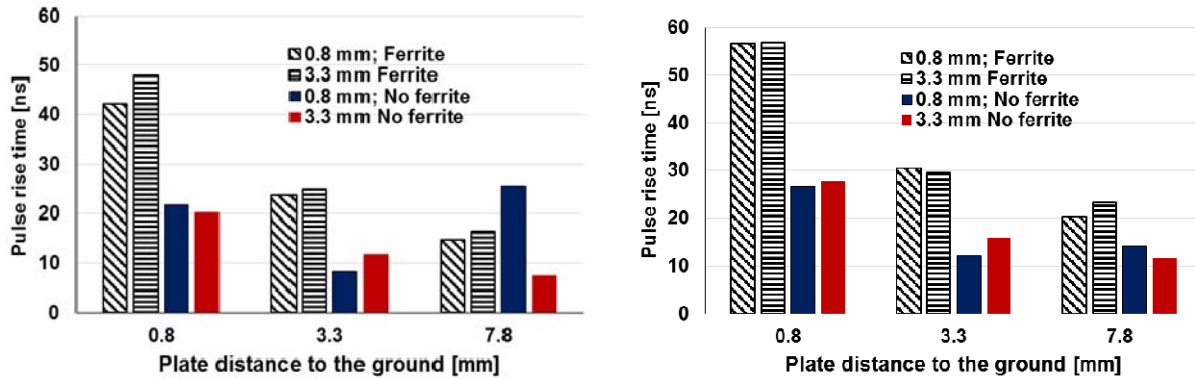


Figure 6: Pulse rise time with 78 cm long USB cables. 12x12 plate on the left and 12x21 cm plate on the right.

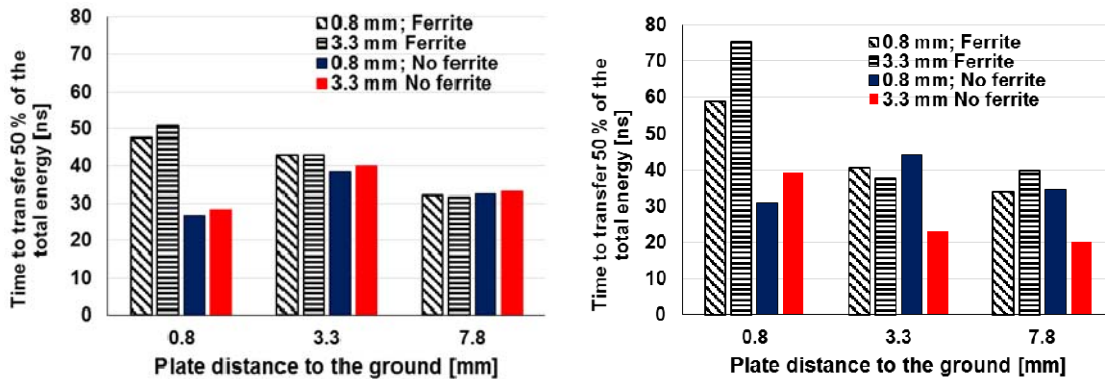


Figure 7: Energy transfer with 78 cm long USB cables. 12x12 plate on the left and 12x21 cm plate on the right.

An energy transfer time up to 50 % of the total value depends on the used test setup, but generally the transfer time increases when the plate or USB cable with a bead is in a high capacitance position close to the HCP. A ferrite bead can slow down the energy transfer time about 50 %, but this depends once again on the oscillation frequency and the type of the ferrite. For example, if the transfer time is measured up to 60 % with a fast current oscillation the

transfer time can vary more than 30 % depending on the case.

Without a ferrite the energy transfer time will vary between discharge scenarios. It is hard to define any systematic trends based on the results of 78 cm long cable, but the transfer time decreases with 110 cm and 2 m long cables when the capacitance of the test setup decreases. Here the EUT capacitance has more effect than the cable capacitance.

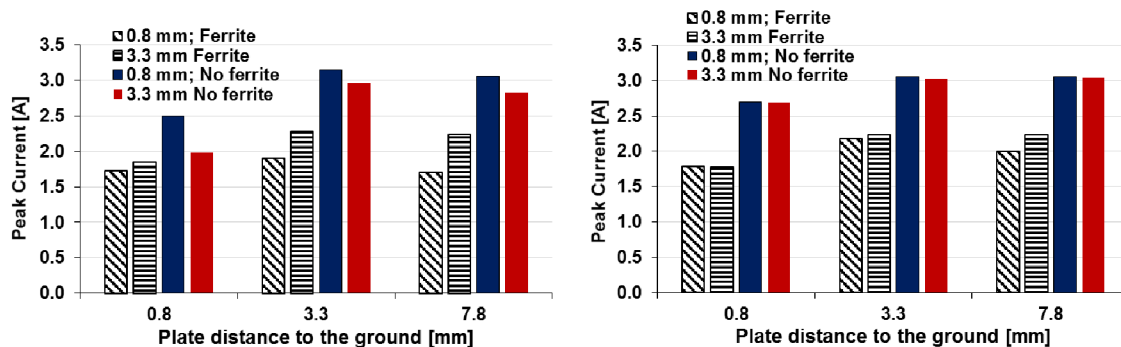


Figure 8: Peak current values with 110 cm long USB cables. 12x12 plate on the left and 12x21 cm plate on the right.

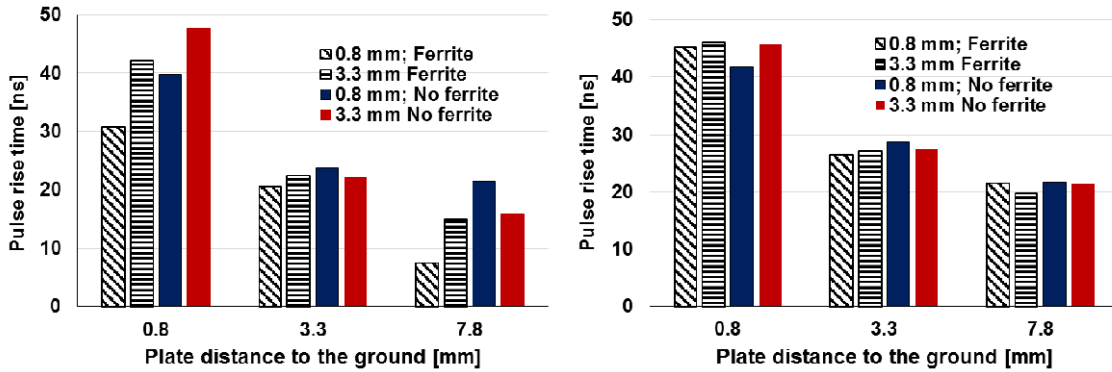


Figure 9: Pulse rise time with 110 cm long USB cables. 12x12 plate on the left and 12x21 cm plate on the right.

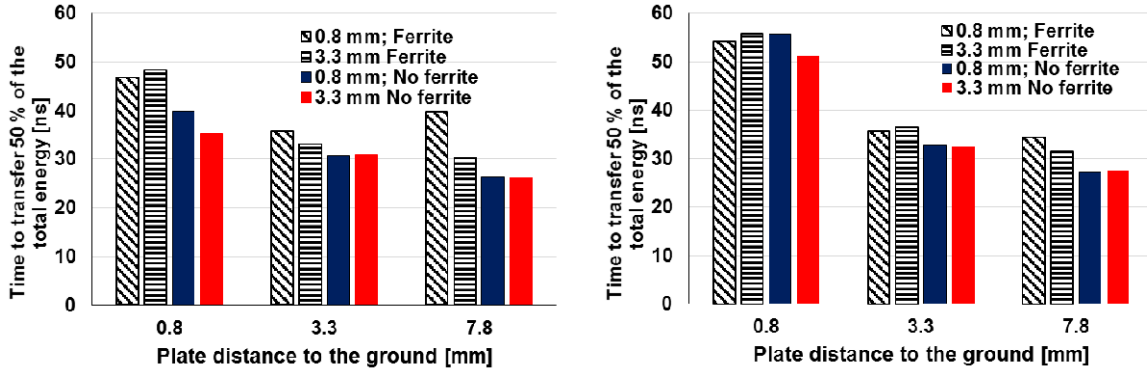


Figure 10: Energy transfer with 110 cm long USB cables. 12x12 plate on the left and 12x21 cm plate on the right.

Figure 11 shows a peak current values for both 12x12 cm and 21x12 cm plates with different capacitance settings both with the shortest 13 cm, without ferrites and longest 200 cm, with two ferrite beads, USB cables. The plates are set at 0.8 mm, 3 mm and 7.8 mm dielectrics sheets, and the cables are kept constant on the 0.8 mm thick sheet. Peak currents depend mainly on the cable length, whereas the effect of plate capacitance on the HCP is less than about 20 %. However, the rise time of the pulse can be about three

times faster with a short ground cable when the capacitance of the plate decreases. The 200 cm long cable with two ferrite beads slows down the rise time and the rise time variation is less than 25 % with all test scenarios. The energy transfer rate varies more depending on the oscillation of the current waveform with the 13 cm long cable. Similar to the results with 110 cm cable, the transfer time is faster with the 200 cm long cable when the plate capacitance decreases.

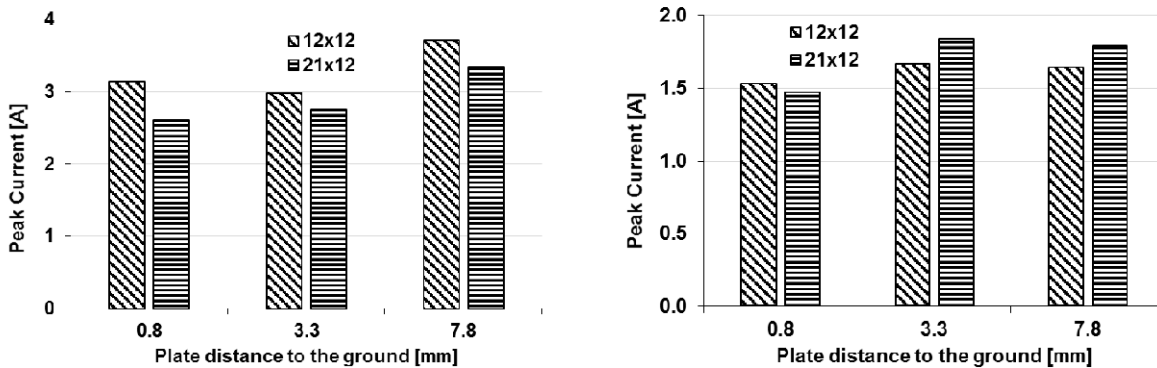


Figure 11: Peak discharge current and power values for the 13 cm (left side) and 200 cm long (right side) USB cables when the cables are at 0.8 mm distance from the HCP.

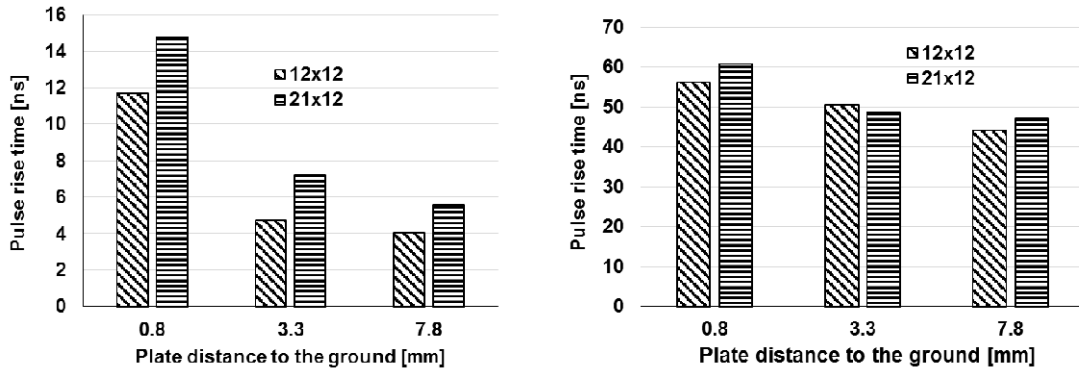


Figure 12: Pulse rise time with 13 cm without ferrites (left side) and 200 cm long with two ferrite beads (right side) USB cables.

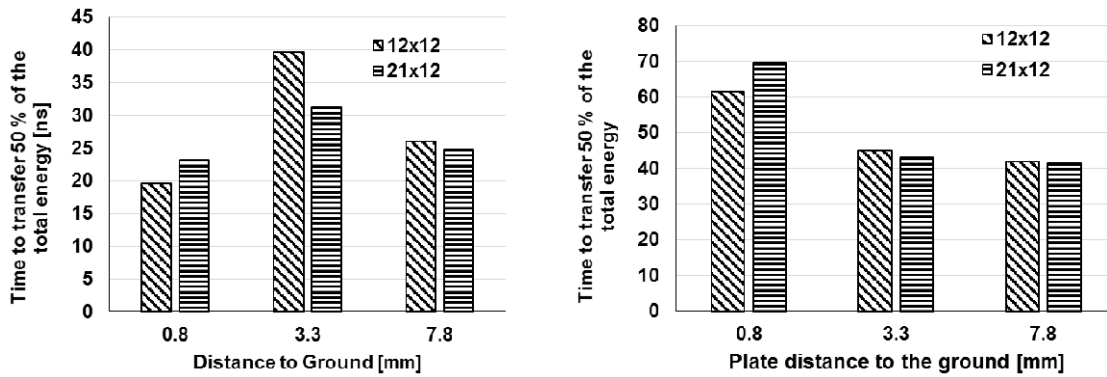


Figure 13: Pulse rise time with 13 cm (left side) and 200 cm long (right side) USB cables.

A few typical measured discharge current waveform are presented in Figure 14 for the 12x12 cm and in Figure 15 for the 21x12 cm size plate with three different USB cables. The transferred total charge of all these pulses is 150 ± 5 nC with the 150 pF source and 1 kV initial potential.

The 13 cm long cable has the fastest and highest current flow with the smaller plate. The 110 cm long cable slows down the current, but produces the highest peak current and power values with the larger plate size. Therefore, the realized ESD stress depends on the combination of EUT and cable properties on the test bench.

The effect of ferrite beads can be seen in Figure 16 and Figure 17 where the peak current decreases and the pulse rise time increases with a ferrite and when the length of the cable increases. The main oscillation frequency is also more than two times slower with a ferrite.

The discharge current was measured also at the EUT and ESD source contact point with a 10 mm long wire going through the CT1 current probe. The capacitance of the EUT and cable was varied on the HCP. Based on the measurements the discharge peak current depends mainly on the size and capacitance of the

EUT on the HCP. The type, capacitance and length of the ground wire had only minor effect on the peak current. Therefore, the effect of cable properties is the highest with components close to the cable ground connection. In addition, components close to the ESD current injection point may have little effect if the ground connection is varied.

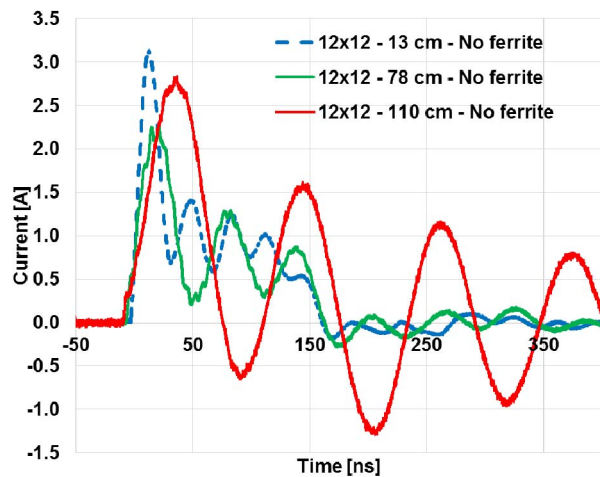


Figure 14: Discharge waveforms for the 12 cm x 12 cm metal plate above 0.8 mm thick dielectric.

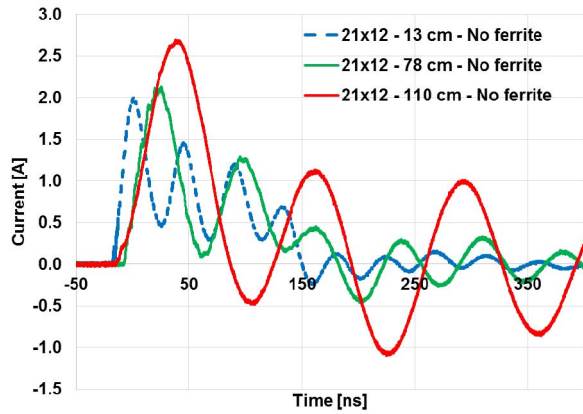


Figure 15: Discharge waveforms for the 21x12 cm metal plate above 0.8 mm thick dielectric.

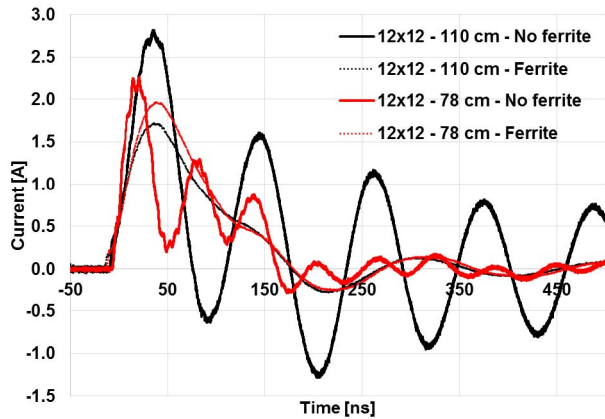


Figure 16: Comparison of discharge waveforms with and without a ferrite.

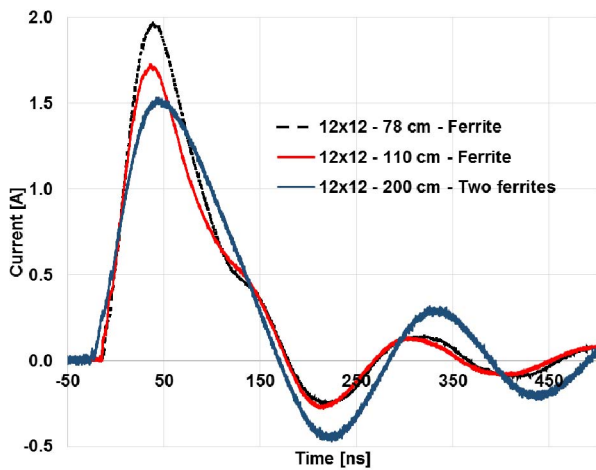


Figure 17: Comparison of discharge waveforms with a ferrite.

B. Simulation results

Both SPICE and 3D simulation tools can be used to predict discharge waveform changes. However, a detailed simulated waveform would require a well modelled ESD source and ground path. Pulse reflections and initial high frequency oscillations of the IEC pulse bring variation to

the results. Therefore, it is challenging to tune simulation models without measurement data as a starting point.

3D simulations can predict similar types of current waveforms as found with measurements, but the exact peak current, power and rise time values don't always match with the measured values without several test setup iteration rounds.

Figure 18 show the results of 3D simulation for the 12x12 cm plate and 35 cm long USB cable without a ferrite. The distance between the plate and HCP is 0.8 mm and the cable is at 0.8 mm, 1.5 mm and 4.1 mm distances from the HCP. Measured results for similar test setups can be seen in Figure 5, Figure 6, Figure 7 and Figure 15. The cable has an additional 0.75 mm thick dielectric around the shield metal conductor. This will increase the minimum distance between the HCP and the conducting wire. The simulation predicts that small changes in cable position will affect the ESD stress along the EUT ground point. In this case the rise time and energy transfer have the largest parameter changes. However, the simulated current waveform at the ESD injection point has only minor changes.

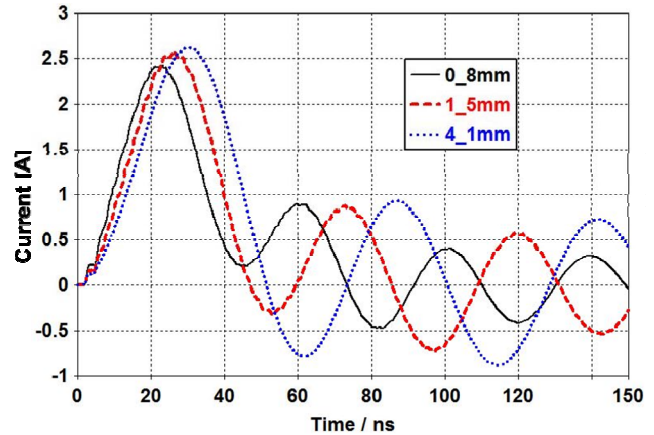


Figure 18: Simulated discharge waveforms with CST Microwave with three USB cable capacitances.

SPICE simulation is also able to predict similar peak current and rise time trends, but requires similar iteration as with 3D tools to get a good match with the measurements. Based on SPICE simulations several parameters have a major effect on the discharge current waveform. The most sensitive values are C_{EUT} , L_{usb} and the delay of the reflected waveforms. Unfortunately, these values are also challenging to measure exactly and simulations with a simplified circuit may give too ideal results.

Figure 19 shows an example SPICE simulation and measurement result for the 110 cm long cable without a ferrite. By using the measured RLC values it is possible to get a close match for the initial part of the pulse. However, this requires trials to tune delay values correctly.

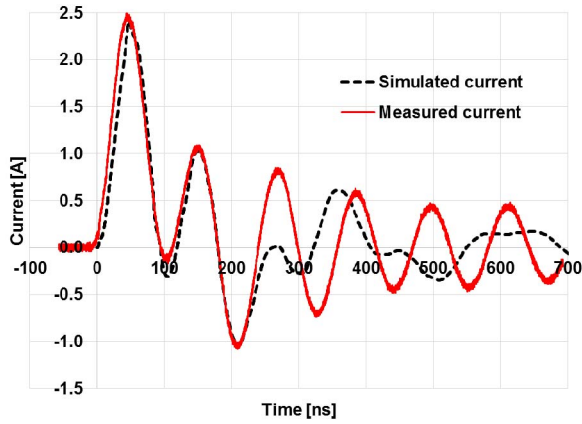


Figure 19: SPICE simulation and measured discharge waveforms for 110 cm long cable without the ferrite bead.

Figure 20 presents SPICE results to study how parameter changes may affect the rise time and peak current. The waveforms show the initial part of the pulses with high frequency oscillation. When the capacitance of the EUT decreases the waveforms have more reflections, thus, making it challenging to predict the exact stress level at the monitored circuit node. In addition, SPICE simulation may not give realistic results anymore if the metal plate representing the EUT is replaced with a real product. Real products have non-linear electrical materials and internal reflections from their physical construction. In that case 3D simulation tools may produce more realistic results.

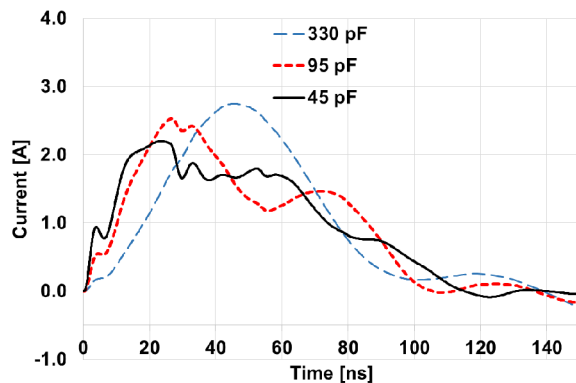


Figure 20: SPICE simulation for a case study where the capacitance of the EUT vary between 45 pF and 330 pF.

IV. Summary of the results

Differences between the maximum and smallest observed values are presented in Table I for all the monitored discharge parameters. The table includes the following parameters: peak current, pulse rise time, peak power and the time to transfer half of the total energy through the ground connection. In addition, there is the variation of the transferred charge at the point of 50 ns and 100 ns.

The values reported in Table 1 are valid only for the used test setups and may change if different ESD generators, USB cables and real products are used. The rise time and peak current are especially sensitive to high frequency

oscillations of the ESD pulse. Larger and smaller size EUTs may also produce different test results.

Based on the measurement and simulation results discharge waveforms can have major variation depending on the type of the cable and the way the cable is placed on top of the HCP. In addition, the capacitance of the EUT and length of the ground cable can give different resonance combinations leading to unpredicted stress levels during ESD tests. Capacitance of the EUT and USB cable will also easily vary when they are placed on top of the 0.5 mm thick dielectric on the HCP. It can be especially challenging to keep rigid cables flat against the dielectric. These uncertainties related to the ground path current should be also considered when doing IEC61000-4-2 qualification tests.

Generally, ground cable positioning has less effect with large size EUTs with higher capacitance on the HCP. A ferrite bead along the cable decreases variation between the test setups and a short cable increases most of the stress parameters.

Table 1. The maximum observed variation with the discharge parameters in percentage. The parameters are compared between discharges observed with 10 USB cables and two EUTs with varying capacitance.

Parameter	Varying [%]
Peak Current	40
Rise time 10-90%	70
Peak Power	80
Energy Transfer up to 50%	60
Charge transfer at 50 ns	30
Charge transfer at 100 ns	10

To improve repeatability and coverage of IEC qualification tests the following methods could be used. These apply to EUTs with a ground connection.

- Keep the ground cable well above the HCP so that small variations with the cable positioning will not change test results. Another option would be to tape the ground cable on top of the dielectric sheet. This is required especially with small size EUTs.
- Test EUTs both with the shortest and longest practical ground cables. Place these cables both close and in far distance from the HCP.
- Test EUTs with several different USB cables if the end user is able to select the type of the cable.
- Use long fixed USB/ground/power cables with an integrated ferrite bead, if possible.
- Estimate ESD stress levels by using simulation tools.
- Increasing the thickness of the 0.5 mm thick dielectric on the HCP would most likely improve repeatability of IEC61000-4-2 standard qualification with small size EUTs.

V. Conclusions

In this paper we study with measurement and simulation methods how small changes with the IEC61000-4-2 test setup may change ESD stress parameters along the EUT ground cable connection. The stress level is evaluated based on the; discharge peak current, peak power, pulse rise time, and energy transfer along the USB cable. Tests were made by using different USB2 cables and two different size EUTs with varying capacitance to the HCP.

Discharge parameters were found to have major changes when the type and length of the USB cable changes. In addition, by changing the capacitance of the EUT or cable on top of the HCP may significantly change some of the discharge parameters. The most sensitive parameters to changes were the pulse rise time, peak power and the amount of charge transferring through the cable during the initial part of the pulse. These parameters may vary more than 50 % when small dimensional changes are made on the test setup or when different USB cables are used for EUT grounding. It was also challenging to define simple rules to better predict discharge parameter changes. Discharge waveforms are a complex combination of ESD sources, EUTs, ground connection and environment.

We show also that SPICE and 3D simulation tools can be used to model the behavior of ESD pulses with different test setups, but it is challenging to get a good match with real life ESD current waveforms even when using simplified physical test setups. Simulations can still be used to estimate uncertainties related to the IEC61000-4-2 qualification.

There are some basic methods available to minimize the effect of test setup variation, but these are easily underestimated during product qualification. Therefore, it is recommended that test setup variations should be taken into account when estimating uncertainties of IEC61000-4-2 ESD qualification.

Acknowledgements

We appreciate valuable support given by Robert Ashton Ph.D., ON Semiconductor, while mentoring the paper.

References

- [1] IEC 61000-4-2, "Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test", 2008.
- [2] L. Lou,"SPICE Simulation Methodology for System Level ESD Design",EOS/ESD Symposium Proceedings, 1B.3, 2010.
- [3] Z. Xijun,et.al.,"Study on the effects of relay switch of ESD simulator to ESD immunity test", Proceedings of Environmental Electromagnetics CEEM, 2003.
- [4] J. Koo,"The Repeatability of System Level ESD Test and Relevant ESD Generator Parameters", IEEE International Symposium on Electromagnetic Compatibility, 2008.
- [5] M. Borsero,"A New Proposal for the Uncertainty Evaluation and Reduction in Air Electrostatic Discharge Tests", IEEE International Symposium on Electromagnetic Compatibility, 2008.
- [6] K. Muhonen,et.al.,"Best Practices for System Level ESD Testing of Semiconductor Components", Compound Semiconductor Integrated Circuit Symposium (CSICS), 2013.
- [7] K. Muhonen,et.al.,"HMM round robin study: What to expect when testing components to the IEC 61000-4-2 waveform", Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2012.
- [8] J. Xiao,et.al.,"Model for ESD LCD Upset of a Portable Product", IEEE International Symposium on Electromagnetic Compatibility, 2010.
- [9] P. Tamminen,"System level ESD discharges with electrical products", Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2012.
- [10] Application Note AN_146, "USB Hardware Design Guidelines for FTDI ICs", Document Reference No.: FT_000292, 2013-11-01.
- [11] White Paper 3 System Level ESD Part II: Implementation of Effective ESD Robust Designs, Industry Council on ESD target Levels, 2011.
- [12] Universal Serial Bus Specification, Revision 2.0, April 2000, <http://www.usb.org>