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NORCHIP and International Symposium of System-on-Chip (SoC)

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Welcome to NORCAS 2018

On behalf of the Organizing Committee, we would like to welcome all of you to Tallinn and to the Fourth IEEE Nordic Circuits and Systems Conference (NorCAS 2018). The conference is a merge of the well-established conferences NORCHIP and the International Symposium on System-on-Chip (SoC).

We have a high-quality program with keynotes and papers to be presented as well as a pre-conference tutorial. Research covering a wide range of topics within circuits and systems in the digital, analog and mixed domains will be presented.

From in total 85 papers submitted, 41 papers were selected for oral presentations and an additional 12 papers for poster presentations. There will be four invited speakers who will share their view on emerging key technologies in the circuits and systems field. In the opening session Dr. Dag T. Wisland, the CTO of Novelda AS, Norway will present innovative wireless sensor solutions based on Ultra-Wideband (UWB) technology. Later in the afternoon Prof. Leonel Sousa from Instituto Superior Técnico, Portugal, will give insights to modular arithmetic based circuits and systems for emerging technologies and applications, in particular the timely deep neural networks and cryptography. In the second morning, Dr. Christoph Hagleitner of IBM Research Zürich, Switzerland, will present transprecision computing circuits and how they can be exploited for energy efficiency. The final talk is given by Dr. Mikkel Høyerby, Merus Audio, Denmark, introducing solutions for cooler, smaller, lighter and better sounding audio products. The day before the official opening of the conference there will also be an exciting tutorial on “Combined Effects of Ionizing Radiation and Electromagnetic Interference on Integrated Circuits and Systems” by Fabian Vargas, PUCRS, Brazil.

The electronics industry in Estonia is not a big one but represented are both international and local companies. The best known from international ones are ABB and Ericsson but there are more. The local companies are not big ones but are known also at international level – Artec Design, Stoneridge Electronics, Testonica – to name only very few of them. In Tallinn, many startups have been gathered into science parks – Tehnopol at Mustamäe, next to the Tallinn University of Technology, and Technopolis at Ülemiste.

Furthermore, we would also like to put forward our great thanks to IEEE Circuits and Systems Society (CAS) for financial co-sponsoring of the conference. We are also thankful to all the Program Committee members and reviewers who have put time and effort into reviewing the submitted papers. Moreover, we are grateful to the NorCAS steering committee for helpful advice and their contribution in the paper selection process. Finally, sincere thanks to Ivan Ring Nielsen from Technoconsult for the technical organization of the event. Starting with NORCHIP in 1985, he has after 33 years, decided to cease his conference organization.

We hope that you will enjoy your time in Tallinn. Although Tallinn is not a big city with population of 450,000, it is known for its famous Old Town – one of the best preserved medieval cities in Europe and listed as a UNESCO World Heritage Site. Tallinn was first mentioned in 1219 and received city rights in 1248 but the earliest settlements date back 5000 years. Today, Tallinn is a mixture of old and new – you can walk between medieval buildings, churches and towers, visit bastions from few centuries old, and shop in different boutiques, supermarkets, etc. Thanks to the compactness of Tallinn, very many points of interests are in the city center and reachable by just walking. In addition to the Old Town, in the western part of Tallinn is Rocca al Mare – the open-air museum where buildings and farmhouses preserve aspects of Estonian rural culture. We wish you an inspiring conference where your knowledge is increased and friendships are both established and strengthened.

Jari Nurmi

General Chair

Peeter Ellervee

Conference Chair

Technical program committee chairs

Analog: Juri Mihhailov

Digital: Maksim Jenihhin

SoC: Kalle Tammemäe

Programme 30 October 2018

09.00 **Opening and welcome**

Jari Nurmi, Tampere University of Technology, FI

Peeter Ellervee, Tallinn University of Technology, EE

1. Plenary session

Chair: Tor S. Lande, University of Oslo, NO

09.15 **Invited talk: UWB Radar Sensor**

Dag T. Wisland, Novelda AS, NO

10.00 A RF Pulse-Width and Pulse-Position Modulator IC in 28 nm FDSOI CMOS

Markus Grözing¹, Johannes Digel¹, Thomas Veigel¹, Robert Bieg¹, Jianxiong Zhang¹, Simon Brandl¹, Martin Schmidt¹, Christoph Haslach², Daniel Markert², Wolfgang Tempel²

1 University of Stuttgart, DE; 2Nokia Bell Labs, DE

10.20 A 0.0186 mm², 0.65 V Supply, 9.53 ps RMS Jitter All-Digital PLL for Medical Implants

Arjun Ramaswami Palaniappan^{1,2}, Lites Siek¹, 1 School of Electrical and Electronic Engineering, VIRTUS, Nanyang Technological University, SG; 2 NXP Semiconductors, SG

10.40 Unleashing the full power of feed-forward opamps: a 200MHz, fully differential, conditionally stable, 36dB gain PGA, using a four-stage multi-path 2.5V amplifier with double feed-forward compensation.

Vahur Kampus¹, Martin Trojer¹, Robert Teschner², 1 Intel Austria; 2 IMST, AT

11.00 **Coffee break**

2.1 Power/Amplifiers

Chair: Kari Halonen, Aalto University, FI

2.2 Network-on-Chip

Chair: Peeter Ellervee, Tallinn University of Technology, EE

11.30 A 24 GHz, 18 dBm, Broadband, Three Stacked Power Amplifier in 28nm FDSOI

Imad ud Din¹, Stefan Andersson¹, Therese Forsberg², Henrik Sjöland^{1,2}, 1 Ericsson AB, SE; 2 Lunds Tekniska Högskola, SE

Multi-Swarm based NoC Configuration and Synthesis

Muhammad Obaidullah, Gul Nawaz Khan, Fei Yuan, Ryerson University, CA

- 11.50 A Design Approach for SiGe Low-Noise Amplifiers Using Wideband Input Matching
Zhe Chen, Hao Gao, Peter Baltus, Eindhoven University of Technology, NL
- 12.10 Design of Stacked-MOS Transistor mm-Wave Class C Amplifiers for Doherty Power Amplifiers
Mohammad Hassan Montaseri, University of Oulu, FI
- 12.30 **Lunch**
- Fault-Tolerant and Energy-Efficient Communication in Mixed-Criticality Networks-on-Chips
Adele Maleki, Hamidreza Ahmadian, Roman Obermaisser, University of Siegen, Germany
- A Distributed DoS Detection Scheme for NoC-based MPSoCs
Cesar G. Chaves¹, Siavoosh Payandeh Azad², Thomas Hollstein^{1,2}, Johanna Sepúlveda³, ¹ Frankfurt University of Applied Sciences, DE; ² Tallinn University of Technology, EE; ³ Technical University of Munich, DE

3.1 Data Converters

Chair: Kari Halonen, Aalto University, FI

- 13.40 Flying-Capacitor Bottom-Plate Sampling Scheme for Low-Power High-Resolution SAR ADCs
Dmitry Osipov, Steffen Paul, ITEM, DE
- 14.00 A Configurable Hysteresis Comparator for Asynchronous Sigma-Delta Modulators
Olaitan Olabode, Vishnu Unnikrishnan, Ilija Kempf, Andreas Hammer, Marko Kosunen, Jussi Ryyanen, Aalto University, FI
- 14.20 A Row-Column Accessed Dynamic Element Matching DAC Architecture for SAR ADCs
Mustafa Kilic, Selman Ergunay, Yusuf Leblebici, EPFL, CH

3.2 Test and Fault Tolerance

Chair: Gert Jervan, Tallinn University of Technology, EE

- Mitigating Multi-bit Soft Errors in ASIC Registers Using ECC-aware Register Clustering
Keisuke Inoue, International College of Technology, Kanazawa, JP
- On Designing PUF-Based TRNGs with Known Answer Tests
Yang Yu, Elena Dubrova, Mats Näslund, Sha Tao, KTH Royal Institute of Technology, SE
- Semiconductor Component Fault Assessment and Probability Impact Estimation on Application Level
Jonas Stricker¹, Clemens Kain², Jerome Kirscher², Andi Buzo², Linus Maurer¹, Georg Pelz², ¹ Bundeswehr Universität München, DE; ² Infineon Technologies AG, DE

4. Poster session I

Coffee break

- 14.40 A Comparison of Polar and Quadrature RF-PWM
Muhammad Fahim Ul Haque¹, Muhammad Touqir Pasha², Tahir Malik¹, Ted Johansson², ¹ NED University of Engineering and Technology, PK;² Linkoping University, SE
- A Radiation Hardened 16 GS/s Arbitrary Waveform Generator IC for a Submillimeter Wave Chirp-Transform Spectrometer
Philip Ostrovskyy¹, Oliver Schrape¹, Klaus Tittelbach-Helmrich¹, Frank Herzel¹, Gunter Fischer¹, Peter Boerner³, Alexander Loose³, David Hellmann³, Paul Hartogh³, Dietmar Kissinger^{1,2}, ¹ IHP, DE;² TU Berlin, DE;³ Max Planck Institut for Solar System Research, DE
- Insertion-Loss Optimization of Transformer-based Matching Networks for mm-Wave Applications
David Bierbüsse, Renato Negra, RWTH Aachen, DE
- FPGA Based Hybrid Computing Platform for ESS Linac Simulator
Arun Jeevaraj¹, Emmanuel Laface², Maurizio Donna², Fredrik Edman¹, Liang Liu¹, ¹ Lund University, SE;² ESS, SE
- Analysis of Synchronous-Asynchronous NoC for the Dark Silicon Era
Reem Walid Etman¹, Salma Hesham¹, Diana Goehringer², Mohamed AbdElGhany¹, Klaus Hofmann³, ¹ GUC, EG;² TU-Dresden, DE;³ IES TU-Darmstadt, DE
- Master-Clone Placement with Individual Clock Tree Implementation – a Case on Physical Chip Design
Oliver Schrape¹, Alexey Balashov¹, Aleksandar Simevski¹, Carlos Benito², Milos Krstic^{1,3}, ¹ IHP, DE;² Arquimea Deutschland GmbH, DE;³ University of Potsdam, DE

- 15.30 **Invited talk: Modular Arithmetic based Circuits and Systems for Emerging Technologies and Applications: Deep Neural Networks and Cryptography**

Leonel Sousa, Instituto Superior Técnico, PT

5.1 High Frequency

Chair: Juri Mihhailov, Tallinn University of Technology, EE

- 16.15 A 15-50GHz Multiplexer Circuit in 130nm SiGe BiCMOS Technology for Ultra-Wide Frequency Ramps in FMCW Radar

5.2 SoC Applications

Chair: Jari Nurmi, Tampere University of Technology, FI

- Three-Dimensional Dynamic Programming Accelerator for Multiple Sequence Alignment

Ruei-Ting Chien¹, Yi-Lun Liao¹, Chien-An Wang², Yu-Cheng Li², Yi-Chang Lu^{1,2}, ¹

- Frank Herzel¹, Arzu Ergintav¹, Johannes Borngräber¹, Dietmar Kissinger^{1,2}, IHHP, DE;²Technische Universität Berlin, DE*
- National Taiwan University, TW;² Graduate Institute of Electronics Engineering, National Taiwan University, TW*
- 16.35 Building lumped models for measured passive mm-wave components
- Eero Sankila, Veeti Kiuru, Janne P. Aikio, Timo Rahkonen, University of Oulu, FI*
- Design and Implementation of 2D IDCT/IDST-Specific Accelerator on Heterogeneous Multicore Architecture*
- Mohammad Ali Pourabed, Sajjad Nouri, Jari Nurmi, Tampere University of Technology, FI*
- 16.55 A 4.3-mW mm-Wave Divide-by-Two Circuit with 30% Locking Range in 28-nm FD-SOI CMOS
- Therese Forsberg, Johan Wernehag, Henrik Sjöland, Markus Törmänen, Lund University, SE*
- Embedded Programmable Processor for Compressive Sensing Applications*
- Mehdi Safarpour, Ilkka Hautala, Olli Silven University of Oulu, FI*
- 17.15 Break
- 19.00 **Dinner**

Programme 31 October 2018

09.00 **Invited talk: Transprecision Computing Circuits for Energy Efficiency**

Christoph Hagleitner, IBM Research, CH

6. Poster session II

Coffee break

09.45 Time-gated CMOS SPAD and a Quantum Well Laser Diode with a CMOS driver for Time-Resolved Diffuse Optics Imaging

Jan Nissinen, Ilkka Nissinen, Sahba Jahromi, Tuomo Talala, Juha Kostamovaara, University of Oulu, FI

Analysis and Design of ESD Protection for Robust Low-Power Pierce Crystal Oscillator Startup

Kim B. Östman¹, Erlend Strandvik², Phil Corbishley², Tor Ø. Vedal², Mika Salmi¹, ¹ Nordic Semiconductor Finland Oy, FI; ² Nordic Semiconductor ASA, NO

An 87% Peak Efficiency, 37W, Class H Audio Amplifier with GaN Output Stage

Nardi Utomo¹, LITER Siek¹, Heng Goh Yap¹, Don Disney², Lawrence Selvaraj², Lulu Peng², ¹ Nanyang Technological University, SG; ² GlobalFoundries Inc

Comparison of Ultra Low Power Full Adder Cells in 22 nm FDSOI Technology

Somayeh Hossein Zadeh, Trond Ytterdal, Snorre Aunet, NTNU, NO

Dynamically Reconfigurable Gearbox Switched-Capacitor DC-DC Converter

Dennis Øland Larsen^{1,2}, Martin Vinter², Ivan Jørgensen¹, ¹ Technical University of Denmark, DK; ² GN Hearing A/S, DK

Characterization and Considerations for Upset in FPGA

Christian Johansson, Torbjörn Månefjord, Saab AB, SE

6. Plenary session

Chair: Atila Alvandpour, Linköping University, SE

10.30 Design and Implementation of Multi-Purpose DCT/DST-Specific Accelerator on Heterogeneous Multicore Architecture

Sajjad Nouri¹, Ramin Ghaznavi-Youvalari², Jari Nurmi¹, ¹ Tampere University of Technology, FI; ² Nokia Technologies, FI

10.50 VELs: VHDL E-Learning System for Automatic Generation and Evaluation of Per-Student Randomized Assignments

Martin Mosbeck, Daniel Hauer, Axel Jantsch, TU Wien, AT

7.1 Data Converters

Chair: Timo Rahkonen, Oulu University, FI

- 11.10 A 10b SAR ADC with Widely Scalable Sampling Rate and AGC Amplifier Front-End
Ayca Akkaya¹, Firat Celik¹, Armin Tajalli², Yusuf Leblebici¹, 1 EPFL, CH; 2 The University of Utah, US
- 11.30 Design Considerations and Evaluation of a High-Speed SAR ADC
Victor Åberg, Christian Fager, Lars Svensson, Chalmers University of Technology, SE
- 11.50 On the Noise Considerations of the Pulse-Shaping Based TIA Channel Designed for a Pulsed TOF Laser Radar Receiver
Aram Baharmast, Juha Kostamovaara, University of Oulu, Oulu, FI
- 12.10 **Lunch**
- 13.15 **Invited talk: Solutions for cooler, smaller, lighter and better sounding audio products**
Mikkel Høyerby, Merus Audio, DK
- 14.00 **NorCAS 2019 announcement and Best Paper Award**

8.1 Power Amplifiers

Chair: Tor S. Lande, University of Oslo, NO

- 14.15 Low-Power Regulator for Micro Energy Harvesting Applications
Tapani Antero Nevalainen¹, Esteban Ferro², Víctor Manuel Brea², Paula López², Ari Paasio¹, 1 University of Turku, FI, 2 Universidade de Santiago de Compostela, ES

7.2 Extra Functional Design Aspects

Chair: Maksim Jenihhin, Tallinn University of Technology, EE

- Energy-Delay Trade-offs in Instruction Register File Design
Joonas Iisakki Multanen, Heikki Olavi Kultala, Pekka Olavi Jääskeläinen, Tampere University of Technology, FI
- Towards Multidimensional Verification: Where Functional Meets Non-Functional
Maksim Jenihhin, Xinhui Lai, Tara Ghasempouri, Jaan Raik, Tallinn University of Technology, EE
- Power Intent from Initial ESL Prototypes: Extracting Power Management Parameters
David Lemma¹, Mehran Goli¹, Daniel Große^{1,2}, Rolf Drechsler^{1,2}, 1 University of Bremen, DE; 2 DFKI GmbH, DE

8.2 Application-Specific Design Optimizations

Chair: Peeter Ellervee, Tallinn University of Technology, EE

- GPU-enhanced Multimodal Dense Matching
Nicolai Behmann, Max Mehlretter, Sebastian P. Kleinschmidt, Bernardo Wagner, Christian Heipke, Holger Blume, Leibniz University Hannover, DE

14.35 Application Specific Integrated Gate-Drive Circuit for Driving Self-Oscillating Gallium Nitride & Logic-Level Power Transistors
Jacob Elias Fæster Overgaard, Jens Christian Hertel, Jens Pejtersen, Arnold Knott, Technical Univ. of Denmark, DK

A Low-Power Hardware Stack for Continuous Data Streaming from Telemetry Implants
Ilia Kempfi, Nouman Ahmed, Andreas Hammer, Olaitan Olabode, Vishnu Unnikrishnan, Marko Kosunen, Jussi Ryyanen, Aalto University, FI

14.55 Design of Multi-Stacked CMOS mm-Wave Power Amplifiers for Phased Array Applications Using Triple-Well Process
Mohammad Hassan Montaseri, University of Oulu, FI

Implementation of an Area Efficient Crypto Processor for a NB-IoT SoC Platform
Luis Cavo, Sebastien Fuhrmann, Liang Liu, Lund University, SE

15.15 **Coffee**

9.1 Biomedical Systems

Chair: Dag T. Wisland, University of Oslo, NO

15.40 Current Readout Circuit for Point-of-Care Infectious Disease Diagnostics in Animal Health
Kathy Hanley¹, Aidan Murphy¹, Niamh Creedon², Alan O' Riordan², Daniel O' Hare¹, Ivan O' Connell¹, ¹ (MCCI), Tyndall National Institute, IE;² (NTG), Tyndall National Institute, IE

9.2 Data Processing Systems

Chair: Jari Nurmi, Tampere University of Technology, FI

16.00 High-speed Sampling System in CMOS
E. Ulvestad, K. G. Kjelogård, T. Moradi Khanshan, D. T. Wisland, T. S. Lande. University of Oslo, NO

Low-latency Packet Parsing in Software Defined Networks
Hesam Zolfaghari¹, Davide Rossi², Jari Nurmi¹, ¹ Tampere University of Technology, FI;² University of Bologna, IT

16.20 CMOS LIDAR for Biosensing
Tohid Moradi Khanshan, Kristian Gjertsen Kjelogård, Emil Ulvestad, Dag T Wisland, Tor Sverre Lande, University of Oslo, NO

Time-predictable Distributed Shared Memory for Multi-core Processors
Simon Thye Andersen, Morten Borup Petersen, Anthon Vincent Riber, Martin Schoeberl, DTU, Denmark

Goal Formulation: Abstracting Dynamic Objectives for Efficient On-chip Resource Allocation
Elham Shamsa¹, Anil Kanduri¹, Amir M. Rahmani^{2,3}, Pasi Liljeberg¹, Axel Jantsch³, Nikil Dutt², ¹ University of Turku, Turku, FI;² University of California, Irvine, US;³ TU Wien, AT

16.40 **Finish**